ELECTRIC FIELD ENERGY HARVESTING FROM MEDIUM VOLTAGE POWER LINES

A thesis submitted in fulfilment of the requirements for the degree of Doctor of Philosophy

by

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Kind regards,

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Declaration

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ABSTRACT

The Smart Grid is the response of the Electrical Engineering discipline to challenges of the 21st century such as global warming and the gradual depletion of energy resources. The vision of a smart electricity grid is an automatic entity in charge of generating, dispatching and consuming electrical energy in the most efficient way and with as small an ecological impact as possible. This new model of electrical energy management is currently being materialized with continuous research and development efforts of technical engineers all over the world, who are in the process of creating and evaluating the best technologies that will contribute to the construction of a more sustainable electrical grid.

As renewable generation resources have gained greater popularity in the last two decades as a measure to address environmental challenges, their introduction to the electricity grid is now changing the paradigm of how the tasks for achieving safe and efficient management of electricity should be carried out. Hence the deployment of technologies around different sections of the grid are becoming increasingly important, in particular in distribution power lines, which are the large conductors in charge of the last stages of electricity dispatch to households and industry, usually at 11 kV or 22 kV in Australia and New Zealand. For the task of continuously monitoring vital parameters of distribution power lines, the most effective approach is the sensing and transmission of the data using embedded wireless communication technologies.

The development of the electronic devices in charge of power line monitoring tasks requires a cost-efficient deployment, as their number will be considerable given the large distances that distribution lines usually cover. Hence, self-powering of these electronics is essential in the design of line monitoring technologies. The research field that deals with this problem is Energy Harvesting, which addresses the transfer of low amounts of energy taken from environmental sources to feed low-power-consumption loads. For the specific environment of distribution power lines, the discernible environmental source is within the strong electric fields produced by the high voltages in these lines. The topic that addresses this problem is called Electric Field Energy Harvesting (EFEH) and the literature around this subject has defined its principles. Nonetheless, previous work has not yet adequately defined the basis that underlays this energy transfer concept.

This thesis addresses electric field energy harvesting from medium voltage distribution power lines, focusing on an optimal solution both in terms of its adaption to the grid and of the most adequate energy conversion strategy for maximum power transfer. A non-contact technique for EFEH from medium-voltage lines using power line insulators is introduced, and the specific conditions under which the energy obtained using this EFEH principle is maximised are determined. Under such conditions, the limitations that a solid-state switching converter has when transforming the EFEH supply to usable levels for low-power loads has, are identified and then addressed by the proposal of a pulsed transfer-mode flyback conversion strategy. The implementation of a self-powered, pulsed-mode energy conversion strategy is demonstrated theoretically and then practically through the development of physical prototypes. The results obtained from the experimental investigations indicate that this conversion strategy can outperform previous works, being able to harvest higher levels of power with a reduced volume and a weaker coupling capacitance.

The contribution of this research work to the scientific community is the proof of concept that a better solution for Electric Field Energy Harvesting can be achieved that will enrich the set of technologies for the upcoming Smart Grid and hence contribute to achieving a more sustainable future for our society.

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Juan Carlos Rodríguez
February 2017

PUBLICATIONS

Some parts of the work and ideas presented in this thesis have been published by the author during the course of the research. These publications are listed below.

[1] J. C. Rodriguez, D. G. Holmes, B. P. McGrath, and R. H. Wilkinson, "Maximum energy harvesting from medium voltage electric-field energy using power line insulators," in *IEEE Australasian Universities Power Engineering Conference (AUPEC)*, September 2014, pp. 1-6.

[2] J. C. Rodriguez, D. G. Holmes, B. P. McGrath, and C. Teixeira, "Energy Harvesting from Medium Voltage Electric Fields using pulsed flyback conversion," in *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 3591-3598.

[3] J. C. Rodriguez, D. G. Holmes, B. P. McGrath, and R. H. Wilkinson, "A Self-Triggered Pulsed-Mode Flyback Converter for Electric Field Energy Harvesting," submitted for review to *IEEE Journal of Emerging and Selected Topics in Power Electronics* on February 2017.

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Glossary Of Terms

AC	Alternating Current
ADC	Analogue-to-Digital (DSP converter unit)
AFE	Active Front End (converters)
ALTIUM	Circuit simulation and design software package
AMI	Advanced Metering Infrastructure
C	Capacitive (impedance)
CCM	Continuous Conduction Mode
CN	Coordinator Node
CPT	Creative Power Technologies (company)
CPU	Central Processor Unit
CRO	Cathode-Ray Oscilloscope
CSI	Current Source Inverter
CSR	Current Source Rectifier
CT	Current Transformer
CVT	Capacitive Voltage Transformer
DA	Distribution Automation
DAP	Data Aggregation Point
DBR	Diode Bridge Rectifier
DC	Direct Current
DCM	Discontinuous Conduction Mode
DCS	Distribution Control Centre
DER	Distributed Energy Resource
DG	Distributed Generator
DIAC	Diode for Alternating Current
DMS	Distribution Management Systems
DPF	Displacement Power Factor
DPLSN	Distribution Power Line Sensor Network
DR	Demand Response
DS	Distribution Substations

DSM	Demand-Side Management
DSP	Digital Signal Processor
DTR	Distribution Transformer
ECVT	Electronic Capacitive Voltage Transformer
EFEH	Electric Field Energy Harvesting
EH	Energy Harvesting
ELV	Extra Low Voltage
EM	Electromagnetic (field)
EMC	Electromagnetic Compatibility
emf	Electromotive Force
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
EV	Electric Vehicle
FAN	Field Area Network
FCI	Fault Current Indicator
FEA	Finite Element Analysis
FEM	Finite Element Method
FET	Field-Effect Transistor
FFD	Full Function Device
FFT	Fast Fourier Transform
GSE	Generalised Steinmetz Equation
HAN	Home Area Network
HF	High Frequency
HV	High Voltage
HVDC	High Voltage Direct Current (power lines)
I	Current
i2GSE	Improved-Improved Generalised Steinmetz Equation
ICT	Information and Communication Technology
IDE	Integrated Developed Environment
IED	Intelligent Electronic Device
iGSE	Improved Generalised Steinmetz Equation
IT	Information Technology
LAN	Local Area Network
LV	Low Voltage
MATLAB	Computer software package
ME	Magnetoelectric
MEC	Microenergy Cell
MEMS	Microelectromechanical Systems
MFEH	Magnetic Field Energy Harvesting

mmf	Magnetomotive Force
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MV	Medium Voltage
mW	Milliwatts
NAN	Neighbourhood Area Network
NSE	Natural Steinmetz Equation
PAN	Personal Area Network
PCB	Printed Circuit Board
PEG	Power and Energy Group (RMIT University)
pF	Picofarad
PLA	Polylactic Acid
PLL	Phase Locked Loop
PLM	Power Line Monitoring
PLSN	Power Line Sensor Net/Network
PMU	Phasor Measurement Unit
PSIM	Circuit simulation software package
PV	Photovoltaic
PWM	Pulse Width Modulation
R	Resistive (impedance)
RAM	Random Access Memory
RC	Resistive-Capacitive (impedance)
RET	Renewable energy target
RF	Radio Frequency
RMS	Root Mean Square
RS-232	Standard for Serial Communication
Rx	Reception
SDK	Software Developer's Kit
SIMULINK	Part of the MATLAB Software package
SM	Smart Meter
SMPS	Switched Mode Power Supply
SN	Sensor Node
T	Temperature
T&D	Transmission and Distribution
TEG	Thermoelectric Generator
Tx	Transmission
V	Voltage
VA	Volt-Ampere
VSI	Voltage Source Inverter
VSR	Voltage Source Rectifier

VT	Voltage Transformer
WAN	Wide Area Network
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WSN	Wireless Sensor Network

LIST OF SYMBOLS

a	Turns ratio of flyback transformer
A_p	Area product of a magnetic core
A_w	Cross-sectional area of the winding conductor
A_x	Various areas (of body x)
α	Frequency exponent for a given core material
B	Flux density
β	Flux density exponent for a given core material
C_1	High voltage EFEH capacitance
C_2	Low voltage EFEH capacitance
C_b	Added bus capacitance
C_f	CSR topology parallel input capacitor
C_{th}	Thévenin equivalent input capacitance
d_x	Various diameters (of conductor x)
D_I	Duty cycle of current
δ	Skin depth
δ_x	Various phase angles (of voltage/current x)
ΔB	Peak-to-peak flux density of overall hysteresis loop
ΔV	DIAC dynamic breakover variation
ΔV_o	Output voltage ripple
ε	Permittivity of a material
$\mathbf{E}$	Electric field vector
E_x	Various energies (of element x)
f_c	Carrier frequency
f_o	Fundamental line frequency
f_r	Resonance frequency
f_s	Switching frequency
$\mathbf{H}$	Magnetic field intensity
$\mathbf{I_x}$	Various current phasors (of element x)
I_x	Various AC, RMS or DC, average currents (of element x)

j	$\sqrt{-1}$
J_x	Various current densities (of element x)
k_i	Derived core loss constant (iGSE)
K_c	Core loss constant
K_u	Window utilisation factor
L_x	Various inductances (of element x)
m	Modulation command signal
M	PWM linear modulation index
μ	Permeability of a material
n	Number of energy transfer pulses
$\overline{N}$	Average number of turns between two successive layers of windings
N_x	Number of turns of a winding x
P_x	Various average powers (of element x)
φ	Phase angle of the input line voltage
R_x	Various resistances
R_{xcyl}	Distances from the centre of the bobbin to the layer x
ρ	Resistivity
σ	Conductivity of a material
T	One generic switching period
T_o	Fundamental line period
T_s	Switching period
t_x	Various time intervals (of action x)
$\mathbf{V_x}$	Various voltage phasors (of element x)
V_{th}	Thévenin equivalent input voltage
V_x	Various AC, RMS or DC, average voltages
Vol_x	Various volumes (of body x)
W_a	Total window area destined for windings in a bobbin
W_m	maximum energy stored in a magnetising inductor
ω_o	Fundamental line angular frequency
Z_x	Various impedances (of element x)

The use of an asterisk (e.g. V^*) denotes a reference or target value.
The use of an overline (e.g. $\bar{t}$) denotes an average value.

Chapter 1

INTRODUCTION

1.1 Background

The past several decades have witnessed the development of renewable energy generation resources as a measure to address the urgent environmental challenge that has been set by the increase of the concentration of carbon dioxide (CO_2) in the atmosphere [4--6]. However, the introduction of all kinds of renewable resources into the electricity grid (e.g. solar panels and wind turbines) has the potential to conflict with the conventional functions of the grid [7, 8].

To manage this conflict an emerging concept is the Smart Grid, which can be broadly defined as the modernization of the existing electric power grid infrastructure with efficiency, safety and reliability optimized for a gradual integration of renewable energy resources, using the most advanced instrumentation, automation and communication technologies [9]. A modern smart grid strives for an interactive transfer of energy between suppliers and consumers that are now capable of injecting energy back to the grid through renewable generation resources [10]. This is done by the integration of functions such as smart metering (that allows load management at times of high demand) and remote control of grid assets (which will allow efficient utilisation of renewable energy). With this scenario, the supply and load conditions vary substantially and continuously, making it much more challenging to control the power balance and reliability of this new grid [11]. Figure 1.1 gives a conceptual representation of a smart grid.

Investment in the smart grid encourages the penetration of renewable forms of energy, as a means of coping with an increasing electricity demand [12--17]. Thus, the implementation of an upgraded grid depends on the development of technologies at different levels of the electricity grid infrastructure. This includes the Transmission and Distribution (T&D) level, where the continuous monitoring of

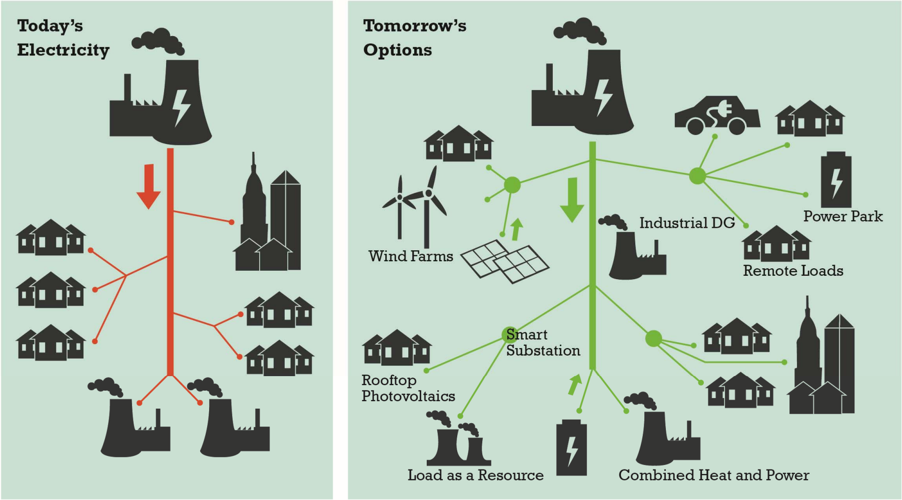


Figure 1.1: The smart grid.

vital parameters such as voltages, currents, fault codes, temperature, etc., is crucial to manage electrical energy transfer [18, 19]. The administration of such prescribed grid functions requires the use of a highly capable communications network that can provide guaranteed levels of performance into a smarter transmission system, but which also can be expanded to the distribution network level [12, 17, 20]. An extension of communications coverage to the distribution network can support a variety of distribution automation functions such as the control of switchgear to achieve rapid restoration and self-healing properties, and extensive monitoring of distribution-network assets to actively manage feeder voltage profiles with automated tap changes or VAR support [21].

Power Line Monitoring (PLM) [20, 22--24] is a concept within the smart grid that uses wireless communication networks to assist smart grid developments such as Distribution Automation (DA), Advanced Metering Infrastructure (AMI) and Demand-Side Management (DSM) [15, 25]. Within the distribution network, these technologies aim to allow the last mile integration of customers and their loads with central grid assets (e.g. Distribution Control Centres in the case of the AMI) through state-of-the-art communication concepts such as Neighbourhood Area Networks (NAN) and Home Area Networks (HAN) [10, 26, 27].

Wireless Sensor Networks (WSNs) are often addressed in the literature as the roadmap for the implementation of PLM [17, 24, 28, 29]. A WSN comprises a set of spatially distributed autonomous sensor nodes (SNs) in charge of sensing and communicating different parameters to coordinator nodes (CNs) wirelessly. In the context of MV distribution power lines, this type of network aims to use low cost communication devices for the sensing and communication of vital power line data, which are extensively distributed in overhead and underground transmission and distribution lines. These technologies are referred in this study as Distribution Power

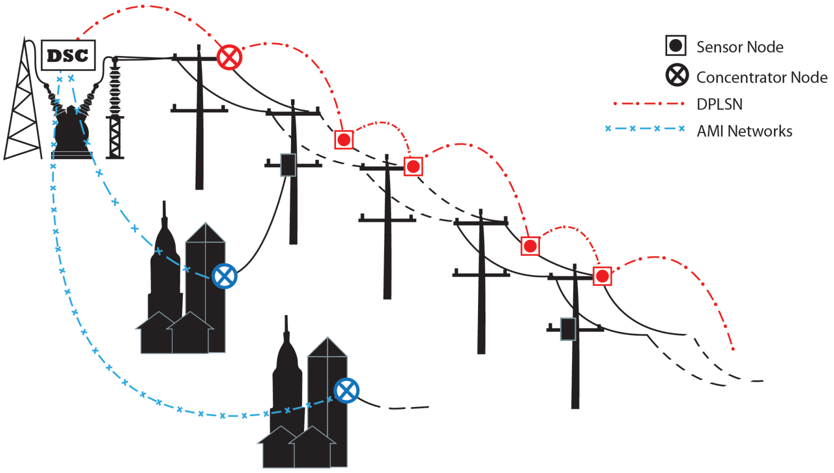


Figure 1.2: A distribution power line sensor network (DPLSN).

Line Sensor Networks (DPLSNs). An example is depicted in Figure 1.2, where it is envisioned as a large number of sensor nodes located both on the MV lines and on the supporting poles. Information from each node is transmitted peer-to-peer back to a data concentrator node away from end devices which provides an interface with the rest of the smart grid via Distribution Control Centres (DSC), in parallel operation with other smart grid communication substructures such as the AMI.

One of the key enabling technologies for DPLSNs, as is the case for other smart grid developments based on the AMI [21, 30--32], is ZigBee® [23, 28, 29, 33--36], a communication technology based on the IEEE 802.15.4, implemented for wireless devices requiring low data rate communications and ultra-low power consumption [37]. DPLSNs based on this and similar communication technologies have demonstrated their effectiveness in spite of the performance challenges in the medium-voltage environment [24, 28, 38--46]. However, the large geographic range that distribution grids encompass compels the deployment of a large number of such devices. This means that the design has to be optimized for large-scale deployment, which, in turn, requires the technologies to be: of small physical dimensions, of low power consumption, of low cost and able to self-power from the environment [19, 47, 48].

The optimal self-powering of electronic devices deployed within the distribution grid MV environment is a subject for the field of Energy Harvesting (EH). An exemplary energy harvesting system for DPLSNs is shown in Figure 1.3, illustrating the obtainment of low levels of energy from surrounding environmental sources to feed low-energy consumption loads. From a medium-voltage environment, the most straightforward harvesting option is to take advantage of the strong electric fields generated in the MV power lines. This type of energy scavenging is known as Electric Field Energy Harvesting (EFEH) [12], and it is the main focus of this thesis.

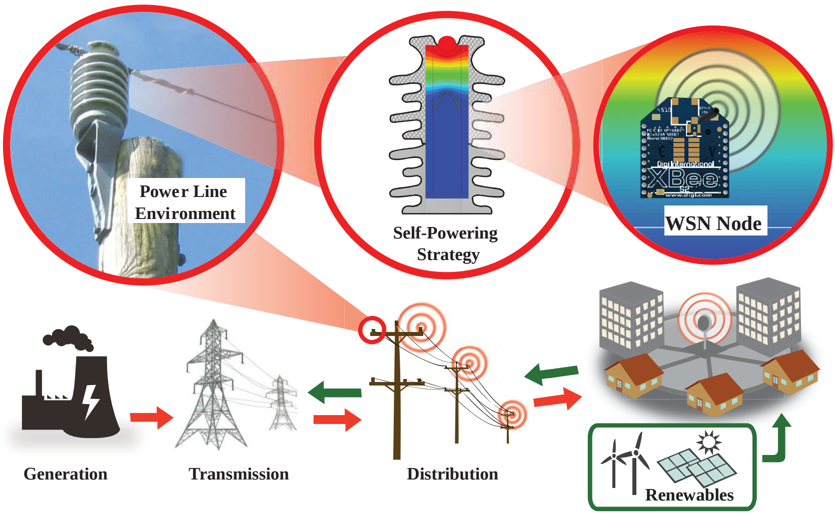


Figure 1.3: Energy harvesting for DPLSNs.

EFEH systems use the capacitive coupling between the medium or high voltage power lines of an electrical grid and a nearby electrode in order to provide power for the low-energy-consumption distributed electronic measurement systems that are needed to monitor these lines for Smart Grid operation. The energy is collected by the capacitive displacement current that flows from the conductor to earth. Energy scavenged in this way has the advantage of always being available as long as the distribution line is energised, without depending on variable load currents flowing through the line itself. Another attractive feature is that it provides the opportunity of a minimally invasive implementation with the power line.

Being a relatively new topic, the literature in EFEH [28, 45, 49--51, 51--63] has demonstrated that the challenge is to extract useful amounts of energy while avoiding close proximity to (or even galvanic contact with) the power line. Previously reported approaches and outcomes have only provided limited exploration of the specific operating and loading conditions that are required to achieve the maximum possible power transfer. In addition, the high impedance weak capacitive coupling between the power line and the harvesting system severely limits the input current magnitude and hence makes any form of switched conversion strategies using semiconductor devices challenging. As a result, only a very small power output is typically achieved because of the methodologies proposed to deal with these limitations.

The present study contributes to the field of Power Line Monitoring for the Smart Grid, by exploring an approach to enhance the energy transfer that is possible to achieve using EFEH to energize electronic the devices that are in charge of the measurement and communication of electrical variables such as voltages, currents, temperatures and fault codes of the Medium Voltage (MV) feeders (11 kV to 22 kV in Australia and New Zealand).

1.2 Objectives

This thesis addresses the following research questions and objectives relating to Electric Field Energy Harvesting:

1. *How to implement a non-intrusive Electric Field Energy Harvesting coupling from Medium Voltage power lines?*
   The challenge with EFEH is to extract useful amounts of energy and also avoid close proximity (or even galvanic contact) to the power line, in order to assist a low-cost, large-scale deployment of wireless sensor networks (WSNs) fed by this self-powering strategy. This thesis will explore a new approach that couples the EFEH system to the power line avoiding direct contact, hence making the harvesting technique more efficient in terms of both cost and large-scale deployment for the Smart Grid.

2. *Under what conditions does Electric Field Energy Harvesting coupling provide optimal energy extraction?*
   Previously reported EFEH strategies do not focus particularly on exploring how to optimise their power transfer, which is essential for practical systems since the available energy from EFEH is invariably quite small. This thesis identifies the loading conditions that maximise the extracted energy by EFEH, and studies how a power electronic conversion system can maintain these load conditions for maximum possible energy extraction.

3. *What is an effective power electronic conversion strategy to achieve optimal energy transfer in an Electric Field Energy Harvesting system?*
   Energy harvested from an MV, AC supply has to be converted to an appropriately extra-low DC voltage (ELV) level for use by an electronic load. The high impedance, weak capacitive coupling between the power line and the EFEH system severely limits the input current magnitude and hence makes switched conversion strategies using semiconductor devices challenging. This thesis studies an appropriate scheme for the practical implementation of a power electronic converter to transform the supply of an EFEH system into usable energy for low-power loads.

4. *How to practically realize an effective, self-powered Electric Field Energy Harvesting conversion strategy?*
   This thesis investigates the implementation of a power electronic converter that is able to efficiently convert the energy of an EFEH supply that is not in direct contact with the power line, without requiring an auxiliary power

supply. A compact, efficient and completely self-powered solution for the energy conversion stage in an EFEH system represents an important contribution to the field.

1.3 Thesis Structure

The content of each chapter in this thesis is outlined below.

Chapter 1 (this chapter) introduces the context of this research and presents the research objectives addressed in this work. It also provides a description of the contributions made by this research.

Chapter 2 presents a literature review on distribution power line monitoring for the smart grid and its present-time technologies and requirements, as the context for the topic of Electric Field Energy Harvesting. The chapter includes a review of the methods available for EFEH, underscoring their limitations and identifying the need for a more fundamental understanding to facilitate power transfer optimisation and power electronic converter design.

Chapter 3 introduces a non-contact approach for Electric field Energy Harvesting that uses the parasitic capacitance between the medium-voltage power conductor and an inner electrode inside the supporting power line insulator. The chapter then develops an analytical study to determine how to maximise the power harvested with the previously defined EFEH technique, deriving the loading conditions that are necessary to obtain maximum power. The proposed EFEH coupling is studied and quantified, and the feasibility of implementing the conditions for maximum power transfer using a solid stage converter are addressed using analytical and experimental investigations.

Chapter 4 applies the ideas from Chapter 3 to develop a novel two-stage conversion strategy that rectifies the weakly-coupled MV, AC EFEH supply into a DC bus capacitor, and then uses a flyback converter operating in discontinuous pulse mode to extract the energy from the capacitor and transform it down to a useful low DC voltage level. The pulsed methodology handles the inherent challenges presented by the coupling conditions in EFEH, and is able to harvest more power from medium voltage distribution feeders than previously reported. Detailed theoretical analysis, computer simulations and experimental results are presented to confirm the concept and underscore its accomplishments and limitations in terms of efficiency.

Chapter 5 builds on the concepts of Chapter 4 to deliver a self-triggered implementation of the previously featured EFEH energy conversion strategy. The chapter develops the theoretical analysis and the practical implementation of a flyback converter in pulsed energy-transfer mode whose switch is self-triggered from the EFEH input supply. Experimental results are presented to investigate the operation of the design.

Chapter 6 describes the simulation systems used in this study to obtain the simulation results presented in the previous chapters.

Chapter 7 describes the experimental systems developed to validate the simulated and analytical results presented throughout the thesis.

Chapter 8 concludes the thesis. Important contributions are reviewed and suggestions for future research work in this area are made.

1.4 Identification of Original Contributions

This thesis presents a number of novel contributions to the field of Electric Field Energy Harvesting as follows.

The first contribution is the demonstration of a methodology for the design of Electric Field Energy Harvesting solutions. The proposed EFEH approach presented in this thesis is a non-contact solution that uses a power line insulator with an inner electrode to provide capacitive coupling to the power line, to harvest the energy. The parameters of this coupling are estimated and validated, and the techniques applied for these tasks can be used for further EFEH implementations, that are less invasive with the power line.

The second contribution is a more fundamental understanding of the maximisation of the power extracted by EFEH, to facilitate the design of an efficient energy conversion scheme. The principles for achieving optimal energy transfer from any EFEH methodology are developed. The theoretical analysis identifies specific loading and operating conditions that allow maximum power transfer. The maximum possible energy to be harvested is specifically characterised.

The third contribution is the assessment of the limitations of solid-state-based switched converters in this type of application and the overcoming of such limitations by using a conversion scheme that uses a rectified DC-bus voltage feeding a flyback type converter operating in pulsed transfer mode, to achieve maximum energy transfer. The presented analysis, simulation and matching experimental results demonstrate the viability of the concept, even with the limitation of a weak coupling to the power line.

The fourth contribution is the introduction of a compact power electronic converter in pulsed energy transfer mode, with the main switch self-triggered from the weakly coupled input supply to avoid the need for an auxiliary supply in the control stage of the system. The detailed design strategy for the flyback converter under the unusual input conditions of an EFEH supply has the benefit of improved efficiency for the EFEH context and potential applications in other smart grid technologies.

1.5 Publications

Several parts of the work presented in this thesis have been published by the author during the course of the research. These publications are listed below:

[1] J. C. Rodriguez, D. G. Holmes, B. P. McGrath, and R. H. Wilkinson, ”Maximum energy harvesting from medium voltage electric-field energy using power line insulators,” in *IEEE Australasian Universities Power Engineering Conference (AUPEC)*, September 2014, pp. 1-6.

[2] J. C. Rodriguez, D. G. Holmes, B. P. McGrath, and C. Teixeira, ”Energy Harvesting from Medium Voltage Electric Fields using pulsed flyback conversion,” in *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 3591-3598.

[3] J. C. Rodriguez, D. G. Holmes, B. P. McGrath, and R. H. Wilkinson, ”A Self-Triggered Pulsed-Mode Flyback Converter for Electric Field Energy Harvesting,” submitted for review to *IEEE Journal of Emerging and Selected Topics in Power Electronics* on February 2017 (under revision).

Chapter 2

LITERATURE REVIEW

Electric Field Energy Harvesting (EFEH) [12] is a particularly attractive option for energy scavenging from the environment of medium-voltage (MV) power lines, since it obtains its energy directly from the electric field produced by the voltages in these lines. Interest in EFEH has grown over the last few years, with a number of recent publications covering the areas of harvester coupling design and conversion of the available energy into usable levels for low-power electronics near the power lines. The review of the material in this area is presented in two sections.

Section 2.1 explores the challenges that EFEH encounters as a self-powering technology for sensor nodes (SNs) in distribution power line sensor networks (DPLSNs), in the environment of 11/22 kV MV power lines. The key conclusions from this section are that:

- The requirements for real-time power line sensor networks and large-scale deployment need a generalised optimisation of EFEH.
- EFEH is a strong contender when compared against other options for energy harvesting.

Section 2.2 reviews the solutions that have been proposed for EFEH, exploring the importance of the coupling to the power line and various energy conversion strategies that have been provided. The key conclusions from this section are that:

- There are fundamental input conditions that limit the power transferred with EFEH, which need to be analysed for power optimisation.
- An effective power electronic conversion system is a key element in the attainment of optimal power, and as such, it requires considerable in-depth analysis, to be viable.

2.1 The Challenges of EFEH

One of the most important factors for the implementation of power line monitoring via WSNs is the availability of a reliable auxiliary power supply for the electronic apparatus that is used to measure various line parameters [24, 64]. Such equipment includes all types of sensors and communication hubs attached to the power line. In order to attain inexpensive deployment of these electronic systems, one important requirement is for them to be self-powered [12, 29, 48, 63, 65--67].

While batteries offer a convenient power supply option to test and demonstrate line monitoring systems, in the literature they are usually seen as a maintenance problem at the system level. Hence the consensus is to use environmental power sources in lieu of, or in conjunction with, batteries [32]. The collection of small amounts of energy (less than 1 W) from such environmental sources is the general topic of Energy Harvesting (EH) [47]. In the environment of medium-voltage power lines, different options for EH are available, including EFEH.

The challenges that EFEH faces as a self-powering technology for smart-grid DPLSNs are common to other EH technologies available in the power line environment. The most important challenges of EFEH are thus reviewed first.

2.1.1 Energy Requirements

An electronic embedded system is at the heart of any WSN sensor node. Typically, the electronics inside an embedded electronic system consume more energy than an EH source is able to deliver at a given time. This is because a SN can operate continuously only if the energy production is equal or superior to the consumption, which is challenging for any EH supply.

Hence, the merit of using EH as a reliable power supply for line-monitoring SNs depends on the implementation of low-power management strategies. In essence, energy optimisation is achieved by re-arranging different processing cycles. This is the principle behind the development of low-power-consumption communication technologies that modify specific communication periods [68], or implement customised scheduling of sleeping times which is referred to as duty-cycling operation [69]. More low-energy consumption schemes appear as technologies in circuit design, microelectronics, storage and communications evolve [70--78].

Low-power management strategies are broadly applied in the literature of EFEH, as in any other EH technology. The most common approach is the use of duty-cycled operation of the target low-power load, with transmission of data implemented only every several seconds or even minutes [58, 63]. Under these constraints, an energy rate of some tens of milliwatts has been identified as a sufficient target [79].

However, this energy requirement increases sharply as real-time monitoring is considered. In fact, the implementation of future smart grid technologies ascribed to power line monitoring calls for real-time operation, such as, for example synchrophasor measurements via Phasor Measurement Units (PMUs) [19]. Typical grid operations towards which smart grid operation is aimed (such as fault-current response and partial discharge detection) require tight accuracy and short response times ranging from some hundreds of milliseconds to several seconds [11, 80].

Under the constraint of real-time monitoring, the energy rate required from an EH supply can be estimated from the existing literature. The figure is obtained as the equivalent power required from a SN with duty cycles approximately equal to one, as this illustrates continuous sensing and communication of variables, avoiding long sleep intervals. The total continuous power requirement then ranges from some hundreds of milliwatts to nearly 2W [23, 36, 52, 63, 81]. A second source for this estimation is the survey presented in Table 2.1, which shows a comparative analysis of the approximate continuous power consumption of the microprocessors typically used in low-power WSNs [82--88].

2.1.2 Competing Technologies

From the environment of medium-voltage power lines the available sources for energy scavenging, other than electric-fields, are surveyed next.

Vibrational-Based Energy Harvesting

This technique is based on the principle of exploiting the oscillation of a proof mass resonantly tuned to the dominant mechanical frequency of the applied environment [48]. In power lines, low level vibrations vary widely in frequency and amplitude. There are three methods typically used to convert mechanical motion into electricity: Piezoelectric, Electromagnetic and Electrostatic.

Electromagnetic power conversion uses Faraday's law of electromagnetic induction, and it is highly limited by output voltages below 100 mV [67]. Electrostatic generation on the other hand takes advantage of the varying energy in a capacitor caused by the motion of the proof mass. This is the principle basis of Micro-electromechanical Systems (MEMS). Its primary disadvantage is the requirement of a separate voltage

Table 2.1: Estimation of commercial low-power processors peak energy consumption.

Device	Power Consumption	Peak Power Estimation (mW)
MSP430F2274 [82]	-Active mode:270μA@1MHz/2.2V -Standby mode:0.7μA -Off mode(RAM retention):0.1μA	9.504
FM32TG840F32 [83]	-Run mode:150μA/MHz@3V -Sleep mode:51μA/MHz@3V -Deep sleep Mode:1μA@3V -Stop mode:0.6μA@3V -Shutoff mode:20nA@3V	14.4
ATMega 128RFA1 [84]	-Rx/Tx:18.6 mA(1.8-3.6 V) -Deep Sleep mode:250nA@25°C -CPU Active mode (16MHz):4.1 mA -2.4GHz Transc:RX12.5mA/TX14.5mA	66.96
JN5148-001 [85]	-35.3mA active mode@2-3.6V - 5.6μA sleep mode -100nA deep sleep mode	127.08
MC1322x [86]	22 mA RX radio/MCU active -0.8mA MCU idle(radio off) -29mA TX radio/MCU active -3.3mA MCU active(radio off) -0.85μA typical hibernate	79.2

source to charge the capacitor to an initial voltage for the implementation of a conversion process [89].

As a consequence, the most common EH vibrational method in the environment of power lines is in fact the piezoelectric generator [67]. Piezoelectric materials produce an electrical charge when mechanically deformed. A cantilever beam made of a piezoelectric material with a magnet attached to its edge is kept in the varying magnetic field of the AC current of a nearby MV power line, as in Figure 2.1 As the magnet oscillates, a time varying deflection at the line frequency is produced and this yields a subsequent AC voltage to be processed by power electronics [52].

Due to its very high source impedance, Piezoelectric EH provides low continuous output power ranging from some hundreds of microwatts to less than one milliwatt [79, 90--92], even at high currents through the power line (around 1kA) [93]. Recent

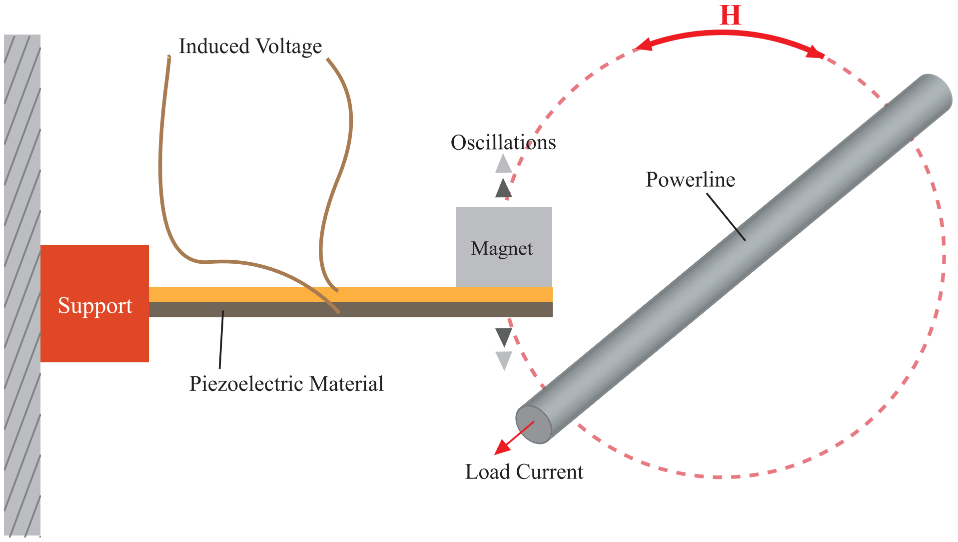


Figure 2.1: Piezoelectric energy harvesting from power lines.

improvements on the cantilever design and multi-cell, and multi-modal operations achieve power levels up to 10 mW, with the constraint that the EH device has to be installed directly on the source of vibration [94, 95] i.e. the MV power line.

Thermal Energy Harvesting

Thermoelectric generators (TEGs) take the energy from the electric potential created from a temperature gradient [96]. Recent developments show a broad range of applications including WSNs to monitor electrical assets, and promising power densities of up to 40 μW/cm^3 [53, 91, 97, 98]. It has been demonstrated to supply a peak of 31.8 mW when a temperature difference of 34°C is applied across multiple TEG cells [99].

However, the efficiency of the method is highly dependent on temperature difference changes, and reduces drastically for small gradients [52]. In the environment of power lines this is a big limitation, since in mild-weather the temperature differences in conductors will not exceed 10°C [100]. Furthermore, the temperature patterns are not consistent, and hence the reliability of the power supply will not be guaranteed.

Solar Energy Harvesting

Whereas energy harvested from the sun could also be seized with the TEG principle in overhead distribution lines, Solar Energy Harvesting in the literature refers mainly to the energy harnessed with the help of a photovoltaic (PV) cell that converts incident solar radiation into electricity. In principle, it is considered as a feasible alternative to power autonomous field devices. A common continuous power output is 160 mW for a 16 cm^2 cell in outdoors applications [101].

However, solar energy harvesting systems behave as voltage-limited current sources, making it difficult to power the load directly from the cell [52]. Also, solar radiation is only available during the day time within the environment of overhead power lines, which adds the requirement of storage technologies, whose implementation at this level is challenging due to thermal constraints [96, 101]. Another disadvantage that limits the application is the low efficiency of the method, from as low as 20% for high-end research solar cells by themselves [53, 76].

Energy Harvesting from Radio Electromagnetic Waves

This approach harnesses energy from far-field ambient radio signals. The incident radio-frequency (RF) radiation has the potential of powering wireless autonomous devices. An antenna connected to a rectifier (called rectenna) is used to convert the incident RF power into usable DC power.

In general, the technique shows consistently low energy density. In a DPLSN environment where smart grid wireless local area networks are deployed, scattered RF signals create power densities that go up to 0.3 $\mu\text{W/cm}^2$, which in a standard application yields around 100 μW before any energy loss due to power processing. This is generally inadequate for powering sensor networks [102, 103].

One recent development with regards to this type of energy harvesting is the deliberate transmission of RF energy, solely for the purpose of powering RF devices. This is called RF Energy Transport [52]. Even with this approach, the average power supply levels range from 100 μW at 940 MHz and at 2 meters from the source [104], to a theoretical maximum of 1 mW at 20 km from the transmitter [103]. New communication sources born from WSNs in the Smart Grid, such as modulated backscattering radiation, have the potential to enhance this method [105]. However, at the present time, the energy levels obtained do not seem to be comparable to other EH options.

Magnetic Field Energy Harvesting

Magnetic Field Energy Harvesting (MFEH) is by far the most popular energy harvesting technique for power line monitoring devices, and has been used in multiple applications involving WSNs [28, 29, 52, 53, 58, 96, 106--109]. The magnetic field near

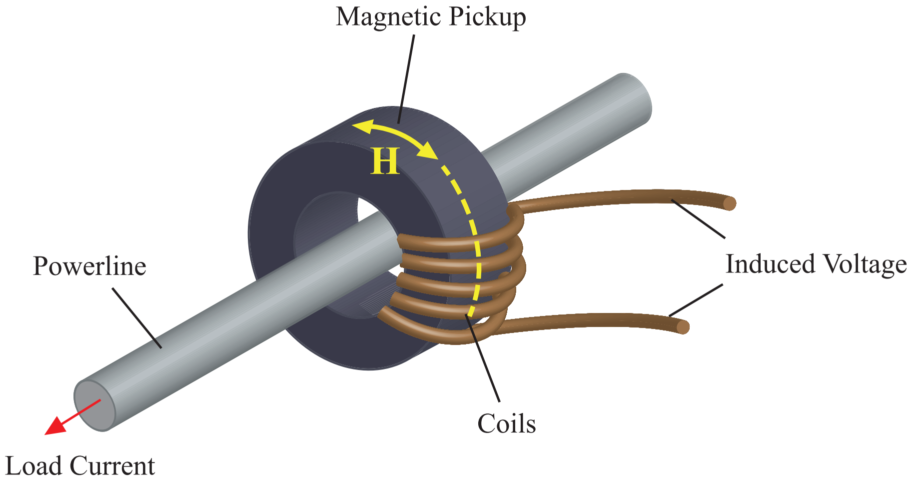


Figure 2.2: Magnetic field energy harvesting from power lines.

distribution lines produced by the AC current flowing through the main conductor can be used as a source of energy caused by electromagnetic induction in a nearby coil. This is the same principle used in a current transformer (CT), and it is shown in Figure 2.2.

It is well recognised that the main limitation of MFEH is the need for large currents through the main conductor. For instance in [110], conductor currents larger than 100 amperes can harvest up to 330 mW; however, below 26 amperes the supply fails in sustaining its output voltage. Important improvements to the design have been developed through the years. In [111] a multi-winding CT and more sophisticated power conversion are used to achieve a continuous power of around 1 mW CT with a primary current of 1 A, hence opting for a duty-cycle mode of operation of the load. The method is also reliable up to 40 metres of distance. Further attempts to maximise the power at low currents by placing the core in saturation have also been proposed [112].

Another important limitation of MFEH method is that it usually needs a core clamped around the power line. Direct contact with MV conductors raises concerns about insulation requirements and safety. To address this issue, some MFEH methodologies not in direct contact with the line have been proposed instead. For instance, the magnetic noise around the power lines has been used instead as a source of energy and around 6 mW were harvested with air-core coils in this way in [113],

In [33, 114], the authors introduce a flux concentrator based on an open core, not wrapped around the line but at a certain distance from it. Additional conversion techniques are included and the method shows to be successful in powering a load in a duty-cycle mode of operation with a period of one minute. However, the continuous power drawn is again highly dependent on the power line current. The figures are as much as 116 mW at 900A of conductor current but only 1.25 mW with 100 A conductor current. An additional limitation is the distance of the harvester from the power line, which rapidly decreases the maximum available power to only 5% at 15 cm. Another implementation with the harvester placed just above the ground collects only 360 μW of continuous power, confirming the high dependence with the distance from the power line too [103].

Hybrid Harvesting Methods

Harvesting the energy from several sources simultaneously is the approach taken by several authors and commercial applications. In this context, the integration of a battery as a storage element is not unusual.

Hybrid solar and piezoelectric energy harvesting has shown to power SNs with up to a continuous 86 μW, without the need for batteries [92]. Hybrid harvesting from solar energy and electromagnetic radio waves has demonstrated an improvement over each individual technique by producing up to 32 μW of continuous power [115].

Another technology integrating EH designs is small-scale wind energy harvesting, either by itself [116] or as part of hybrid implementations with other technologies such as high-frequency wireless magnetic power transfer [117] and linear generators for EH from HVDC power lines usually acting as a battery charger [55].

2.1.3 Devices Deployment

Ultimately, any form of EH will be integrated into a composite solution for power line monitoring, along with the sensing, processing and communication blocks. How easy the deployment of these solutions is within a DPLSN will depend on their size and thus their cost [20].

For example, the network of a distribution company that accounts for only one fifth of the maximum demand in the state of Victoria in Australia, would require nearly half-million sensor nodes for the deployment of WSN technology in a DPLSN. This represents a considerable challenge given its relatively small capital budget for asset development in one fiscal year [118].

Quite often, the cost and size of the monitoring solution depends in turn on the EH methodology applied. Commercial monitoring solutions with some form of energisation from the power line have evolved through the years, from simple voltage detectors [119] and fault circuit indicators (FCIs) [120], to patented self-contained solutions including measurement, communications and self-powering [121]. Representative off-the-shelf solutions for self-sustained distribution power line monitoring that can be found commercially to this date have been surveyed and are presented in Table 2.2.

It can be seen that current solutions feature large measurement spans in MV/HV conductors and successfully integrate the most up-to-date communication and self-powering technologies. However, they are invariably bulky and energy-hungry, so that none of them show complete independence from batteries. Also, the implementation of real-time waveform monitoring does not seem to be in place yet, except for particular events such as line faults. A quick market-cost research indicated their prices in the range of AUD 1000.0 to AUD 9500.0. These limitations still hinder large-scale deployment, which is needed for DPLSNs.

The most popular technology for self-powering in these commercial devices is MFEH, which often requires a device wrapped around the power line conductor. Direct contact with the line presents additional requirements of insulation and safety, requirements that drive the increased sizes and higher costs. Clearly, there is a big benefit in reducing the bulk and the proximity of the EH technique to the line.

Table 2.2: Commercial power line monitoring solutions.

Device	**Main Specs.**	**Measurements**	**Comms.**	**Power Supply**	**Comments**
Gridsense's LineIQ [122]	-315×180×140 mm, 2kg -5 to 138 kV range -196 KB memory -Hot-stick live installation to bare 6-32mm conductors -Includes conductor mounted sensor LIQ-60	-Time-averaged Current, Voltage, Temperature, Displacement Power Factor in 2 minute intervals -Rogowsky coil CT-based current meas. -Voltage meas. based on capacitive current -Temperature meas. based on Pt resistance thermometers, -20 to 90°C range	-IEEE 802.15.4, 2.4GHz. -Range of 30 m, line of sight -200ms logs of fault current waveforms up to 25kA	-Sealed lead acid 2V battery, 10Ah capacity -Solar panel to recharge battery -Current consumption with no RF transmission 5mA	-Not accurate voltage measurement due to missing ground reference and skewed field by adjacent conductors -More accuracy requires additional sensor -Typical life span 10 to 15 years -Charging the flat battery requires optimal sunlight for up to 50 hours
SEL's WSO-11 [123]	-4.16 to 34.5 kV range -Min. load current required 5A - Wire diameter clamping range 4 to 38mm -600g	-Current, conductor temperature. -Max fault current 25kA for 10 cycles -Tripping setup according to IEEE 495-2007 pt.4.4.2	-Part of On-Ramp ULP wireless network (2.4 GHz ISM band) protocol for low-energy consumption [124]	-3.6 V, 19 Ah lithium battery	-Minimum continuous load current requirement is of 5A. Provides EMC standards compliances -Ten year op. life based on assumptions 24-hour periodic reporting50 asynchronous events per year

Table 2.2: (continued) Commercial power line monitoring solutions.

Device	**Main Specs.**	**Measurements**	**Comms.**	**Power Supply**	**Comments**
CET's CSM-SCO [125]	-6 to 35 kV range -360A max. current rating -Fault location -116×130×116 mm, 500g	-Faults of up to 1.5kA, 5% accuracy -Data sent once per minute	-RF of 470 to 510MHz -Less than 10mW Tx power -500 kbps rate -Min. 200m range -Star/Mesh topologies	-3.6V, 4Ah battery - 200mW of self-created power. -Super capacitance storage of 2.7V, 25F - Dynamic power consumption 800muA/3.6V	-Minimum load current is 2A in wired cable.
ABB's GridSync SCC-125 [126]	-443×813mm, 60kg	-Based on SCC-125 split-core combination current and voltage transformer -ANSI C57.13 revenue grade accuracy	-	-	-

Table 2.2: (continued) Commercial power line monitoring solutions.

Device	**Main Specs.**	**Measurements**	**Comms.**	**Power Supply**	**Comments**
NEXANS' CAT-1 [127]	-40 to 60°C range -2A charging current	-Mechanical tension, network radiation, ambient temperature - Temperature resolution of 0.1°C	-Spread-Spectrum Data RF band 902-928MHz - 0.1 to 1W output	-Two 20W solar panels -Pack unit of two high-temperature sealed lead-acid batteries, with solar charging unit, able to power the system for up to one week	-Robust system with little maintenance -High power consumption -Battery replacement every 5 years
USI's Power Donut 2 [128]	-Range up to 500kV -320×140 mm, 9.2kg - Allows hot stick installation	-Current, voltage, temperature and inclination	-GSM/GPRS/Edge wireless data service to communicate with the customers' data concentrator/server	-Self powered from the power line -Typical consumption of 10W -5Ah backup battery	-Requires 50 to 70A for continuous operation - Up to 5 years life

2.2 EFEH Solutions

The energy harvesting technologies for powering wireless sensor nodes in DPLSNs in the literature still face the challenge of achieving the higher levels of power necessary for real-time operation. Additionally, large-scale deployment of these SNs requires more compact EH solutions that are not too invasive to the power line conductors.

EFEH systems take advantage of the strong electric fields radiated by MV/HV power lines [129] to enable a low-power supply when these fields are capacitively coupled from the line to a nearby load. This represents an advantage against other harvesting strategies such as MFEH, because the energy is collected via the capacitive displacement current that flows from the conductor to ground, not the load current flowing through the primary conductor. Hence it is independent of the load currents. This also has a great potential for reducing the distance of the harvester to the power line.

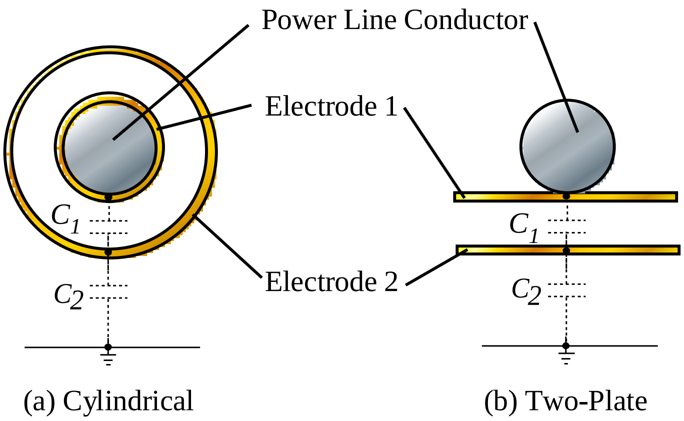
The way EFEH couples to the power line, the strategies for converting the available energy to usable levels, and the power achieved by this technique are reviewed in this section.

2.2.1 Power Line Coupling

The principle of EFEH as a self-powering technology for line monitoring was first introduced by Zangl et al. [45, 49]. It was presented as part of a system able to determine temperature, distance to ground, and degree of icing for preventing the occurrence of sags and increased vibrations in HV power lines. The structure forms a cylindrical EFEH topology, shown in Figure 2.3a. The power is usually extracted by connecting a subsequent energy conversion system in parallel to C_1, from the capacitive divider formed by the strategy.

The cylindrical EFEH topology has been used widely throughout the literature. In [55], [66] and [90], it is used to power devices in a WSN for the monitoring of temperature, the inclination of power lines, and their current load, as an industrial application for controlling losses related to conductor deterioration. In [56], its successful integration with wireless communication schemes was demonstrated, showing as well that the operation of the harvester and communication channel are not negatively affected by the harsh environment of the HV line.

One unattractive feature of using C_1 as the harvester medium is the direct contact of the EFEH system to the power line. The investigations in [50] and [63] use a



(a) Cylindrical (b) Two-Plate

Figure 2.3: Topologies for EFEH harvesters (cross-sections).

variation of the cylindrical topology, where the energy is extracted between two concentric electrodes around the power line, thus avoiding direct contact.

The cylindrical topology has also been applied in EFEH from low-voltage conductors. In [57] and in [60] the topology was composed using metallic foil wrapped around insulated, single-phase, three-wire household power chords (rated for 220V line-to-line). The energy is extracted from C_2 rather than from C_1, thus forming an EFEH system that is earthed through a conductor plate on the concrete floor of the edification on which it is mounted.

Moghe, et al. [52] proposed a different form of coupling, using a two-plate topology, as showed in Figure 2.3b. In this geometry, the top plate is in direct contact with the power line and the bottom plate is 5 cm below. The two-plate system is at a certain height from the ground, thus forming an EFEH capacitive divider. The energy here is extracted from C_1, which again has the disadvantage of a direct contact with the power line. The use of this topology with energy extraction from C_2 has been proposed as well [58]. Finally, a modification to this geometry has been proposed in [53] where the two-plate system is not in contact with the HV conductor, but at a distance about 10 cm below it.

The most important parameters for the characterisation of the coupling to the power line are the capacitances in the parasitic capacitive divider formed under the principle of EFEH i.e. C_1 and C_2. The identification of these values depends in turn on the characterisation of the electric field near the power lines. For simple geometries, this identification can be done deterministically using electromagnetic theory. For more complicated structures, however, numerical methods are required. The different methodologies available for this task [130--132] are mainly based on the Finite Elements Method (FEM) also known as Finite Element Analysis (FEA) [133]. In general, the high accuracy of FEA in the estimation of electromagnetic field patterns around power lines has been proven and documented [45, 49, 55, 61] .

In both the cylindrical and the two-plate EFEH topologies it has been observed that the values of the capacitances depend greatly on the dimensions of the harvester, as well as on the distance from the ground reference. The values for both C_1 and C_2 have been shown consistently to be in the range of some tens of picofarads [28,45,49--51,51--63].

The extremely low values of the capacitances in the system translate into very large input impedances. It has been determined that the equivalent input circuit of the EFEH system resembles an AC current source with a large input impedance [45, 49, 134]. This causes the input AC current to be invariably low (some few hundreds of micro amperes), with an input voltage that is highly dependent on the load presented to the system. These features severely limit the available power transfer. For methods that are not in direct contact with the power line this situation is worsened, as the input capacitances drop further [50, 53, 58, 63].

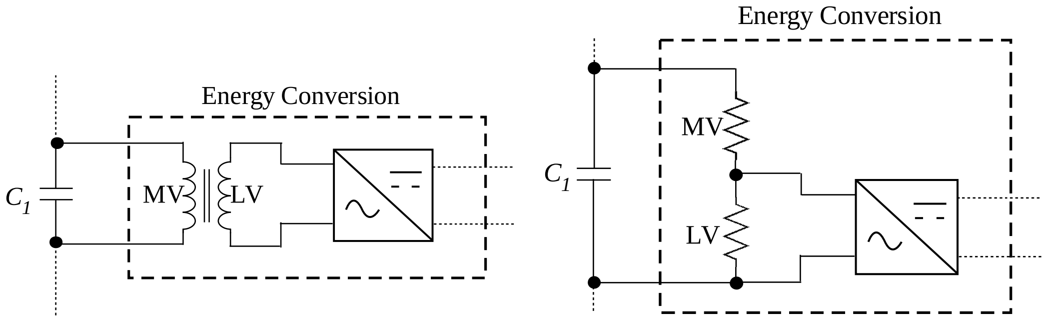
One direct consequence is that the maximum continuous input power available to the EFEH system depends strongly on the loading presented to the capacitive divider. The experimental quantification of this input has been somewhat explored in the literature. However, there is no clear exploration of the explicit conditions for maximum power transfer for any particular load.

There are additional challenges related to the capacitive coupling that are specific to EFEH. For instance, the total parasitic impedance of the circuitry between the conductor and the harvester shell has to remain below 500 pF, as an increase in C_1 deviates the displacement current towards it, thus decreasing the available power to the load. In addition, there is a requirement for decoupling of the measurement and communication circuits from the harvesting circuitry. These limitations were explored in [56].

2.2.2 Energy Conversion

In order to deal with the difficulties in power transfer presented by the capacitive coupling, it is a common identification in the literature that the design of the power conversion circuit is the key element to an efficient use of EFEH.

To manage the limited AC input current of the EFEH divider and the rapid increase of the input voltage with the load, some of the most representative energy conversion methodologies in the literature implement tapping of the input MV, in their first stage. This has been tried either by an input, line-frequency, voltage transformer [45,49--51,56], or an input resistive divider [59,62], as shown in Figure 2.4a and Figure 2.4b respectively.



(a) Transformer **(b)** Resistive divider

Figure 2.4: Tapping in EFEH conversion strategies.

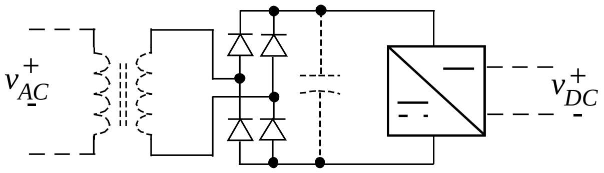
The use of a MV/LV tapping transformer increases the size of the EFEH system due to the requirement for a high magnetising impedance to limit the excitation current demand from the low-current supply [61, 63]. On the other hand, the use of a resistive divider is inefficient and hence reduces the available harvested energy. The requirements of a strategy for direct energy conversion, without reducing the initial MV, have not been analysed experimentally in depth.

A subsequent AC-to-DC power electronic converter is then required to make the energy usable by a low-power load. The varied conversion topologies proposed in the literature are summarized in Figure 2.5.

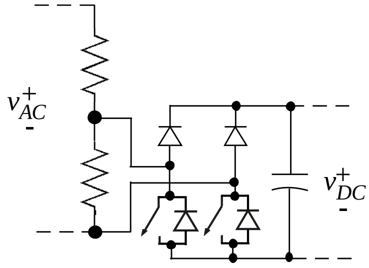
Simple linear power supplies (2.5a) used in [45,49--51,56,58] have the disadvantages of increased size and low efficiency. Furthermore, the use of batteries for supporting the conversion system is not unusual.

An alternative switching topology was presented in [59, 62], which is based on a semi-controlled, full-wave bridge rectifier. This option uses asymmetrical switching control in low-frequency, and it is depicted in Figure 2.5b. The switching operation was illustrated in computer simulations, but there was no detail on the practical switching waveforms nor on the design and power consumption of the gate drivers for the switches.

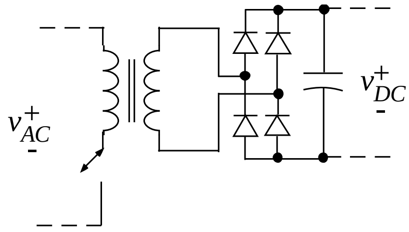
Another option is the so-called up-conversion oscillatory circuit presented in [63] and illustrated in Figure 2.5c. This topology works with the premise of optimising the efficiency by using the principle of resonance. Its main challenge is that matching the impedance formed by the low input capacitance and the equivalent inductance of a subsequent transformer at 50 Hz requires a magnetising inductance in the level of kilohenries [61], which is impractical. Hence, it uses a switch working at a very low duty cycle (5% at 200 Hz), which oscillates at higher frequencies such that resonance can be achieved with smaller magnetics. The method succeeds in improving the efficiency, however the total output power is very low (less than 1 mW), despite the



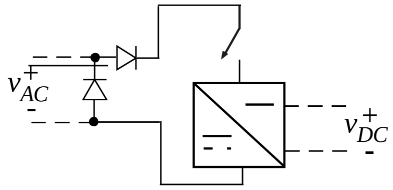
(a) Linear power supply



(b) Semi-controlled full wave bridge rectifier



(c) Up-conversion oscillatory circuit



(d) Switched voltage doubler (low-voltage EFEH)

Figure 2.5: Energy conversion topologies used in EFEH.

increased complexity. In fact, it is acknowledged in [135, 136] that higher efficiency does not necessarily mean more power transferred.

Finally, alternative control methods based on hysteretic triggering have been proposed in low-voltage EFEH applications, with a general representation as shown in Figure 2.5d. In [57] this topology is used to store the energy from the voltage-doubler in a capacitor. In [60], the energy conversion is implemented using a MOSFET triggered by a MEMS switch which uses the electrostatic force in the field created in the EFEH system. It turns the main switch on for a higher threshold and turns it off when the input voltage falls a below a lower threshold. Its application to MV power lines however is limited due to the low MEMS switch voltage ratings.

One important realisation is that the reasoning behind the choice of the different energy conversion methodologies proposed in the literature is not clear. In addition, the underlying principles for power maximisation, the detailed switching operation and the process of selecting the most optimal topology have limited coverage. As a result, it is uncertain whether the power achieved from existing EFEH techniques is in fact the best that is possible.

2.2.3 Power Output

The practical output power levels that EFEH is able to deliver make it a strong contender as a self-powering technology for MV power line monitoring. However, its optimal level is not clearly identified yet.

Using the cylindrical EFEH topology, up to 370 mW of continuous power have been extracted from a 150 kV line in [45, 49, 56]. It was described that the power can be increased by increasing the coupling with the MV line i.e. C_1. Also, the power decreases slowly with the increase of the distance to ground.

For the cylindrical topology used in [50, 51], an output power level of about 16.4 mW is obtained from a 60 kV power line. This application includes power matching circuitry, storage with supercapacitors and a low-power energy management system that implements duty-cycled operation that measures variables every 15 minutes, in normal state. However, batteries are still included for initialisation.

The non-contact cylindrical EFEH system with up-conversion oscillatory circuit in [63] achieves up to 663 μW of continuous power from a 10 kV power line, with a high efficiency of 90.5%. In this reference, another demonstration of the low-power management system was presented, where a WSN node composed of low-power embedded electronics was duty-cycled for 620-millisecond transmission every 4 minutes, to make the power usable. In addition, the gate driver of the main switch was implemented with low-power elements, consuming up to 6 μW.

The two-plate geometry in direct contact with the power line proposed in [59] and [62], with a tapping input resistive divider and semi-controlled full wave bridge rectification obtains nearly 17 mW of continuous power from a 35 kV power line. In contrast, the same topology without direct contact to the line achieves only up to some hundreds of microwatts [53, 58]. Again, this energy rate is demonstrated to be enough for duty-cycled WSN node operation, but not necessarily enough for a real-time implementation.

Finally, low-voltage EFEH techniques can achieve only as much as 57 μW, hence requiring the use of duty-cycled operation of their low-power loads, with RF data transmission happening only every 42 seconds [57, 60].

In general, the power obtained with EFEH is too low for real-time operation. Table 2.3 presents a comparison between the most representative EFEH approaches reviewed in this section. The comparison uses the common standards of power per unit of volume (power density in μW/cm^3), power per unit of voltage in the power line in mW/kV (since the harvested power increases with higher line voltages) and the main strengths/limitations of each technique.

It can be seen that EFEH systems with direct contact with the MV/HV power line, i.e. connected across C_1, can harvest more continuous power. This requirement, however, hinders a large-scale deployment of the associated low-power sensor nodes that EFEH aims to energize, as it is more invasive to the power line for installation. In addition, the power harvested in this form involves close proximity of the outer electrode to ground too, as the power decreases with the height of the power line conductor.

Another observation is the two-plate EFEH harvester topology displays a superior power density compared to the cylindrical topology. This shows that a less invasive geometry does not necessarily reduce the efficiency. On the other hand, the cylindrical topology in contact with the power line still achieves the highest EFEH per kilovolt.

Less-invasive EFEH techniques with improved power transfer are yet to be explored, as well as paying closer attention to the design of the power electronic converter.

Table 2.3: Comparison between EFEH methodologies.

Study	**Harvester Volume** (m^3)	**Power Line Voltage** (kV)	**Input Capacitance** C_{th} (pF)	**Continuous Power Harvested** (mW)	**Power per Volume** ($\mu W/cm^3$)	**Power per Line Voltage** (mW/kV)	**Power per Input Capacitance** (mW/pF)	**Comments**
[45, 49, 56]	3.89×10^{-2}	150	520	370	9.52	2.47	0.71	Cylindrical; Line contact; Transformer tap; Linear pow. supply; Batteries.
[52, 59, 62]	6.47×10^{-4}	35	110	17	26.29	0.49	0.15	Two-plate; Line contact; Res. Divider tap; Semi-CSR conversion.
[57]	4.71×10^{-5}	0.13	80	0.057	1.21	0.45	0.00071	Cylindrical; Non-contact; For household LV conductors.
[50, 51]	1.57×10^{-3}	110	172	17.3	11.014	0.16	0.101	Cylindrical; Line contact; Transformer tap; Linear pow. supply; Batteries.
[63]	3.77×10^{-2}	10	215	0.66	0.018	0.066	0.0031	Cylindrical; Non-contact; Up-conversion oscillation method with smaller magnetics.
[53]	3.14×10^{-3}	7	4	0.18	0.056	0.025	0.044	Two-plate; Non-contact; Switching plates in short circuit.

2.3 Summary

This chapter has been presented in two sections. The first section reviewed the challenges that EFEH faces as a technology for power line monitoring. The second section reviewed the solutions for EFEH presented in the literature.

Much of the literature in energy harvesting proposes the use of low-power management strategies for duty-cycled operation of the target loads in WSNs for power line monitoring. However, a more holistic application in smart-grid developments requires real-time operation of SNs, which has the more demanding requirements of continuous power, in the order of some hundreds of milliwatts.

The different EH alternatives to EFEH in the environment of MV power lines either have a very low power delivery or are unreliable. The most prominent option is Magnetic Field Energy Harvesting (MFEH), which is the choice for many commercial, off-the-shelf solutions for power line monitoring at the moment. However, MFEH techniques have the limitations of requiring close proximity to the power line, and variable power outputs as the line current changes. The former drawback, in particular, drives increased sizes and higher costs, which hinders the application of large-scale deployment of SNs in DPLSNs.

EFEH takes its energy from the strong electric fields produced in MV lines and does not require load current flowing through the power line. The harvester couples to the power line as a capacitive divider from which the energy can be extracted both with and without direct contact to the line. In either case, the low values of the coupling capacitances limit the power that can be extracted with this technique to some tens of milliwatts, even from HV lines.

There is scope to resolve many of these issues associated with the optimisation of the energy transferred with EFEH. hence of particular focus in this thesis are:

- The exploration of less-invasive EFEH techniques, able to avoid galvanic contact to the power line, in order to assist a low-cost, large-scale deployment of the sensor nodes to be powered using this strategy.
- The determination of the precise electrical conditions needed for the optimisation of the energy transfer in EFEH, which are not clear yet from the literature.
- A detailed analysis of the switching operation within an energy conversion strategy that is able to maximise the power obtained with EFEH.

- The continuous energy transfer rate obtained with the current EFEH methodologies can be greatly improved by an adequate implementation of the energy conversion stage.

Chapter 3

MAXIMUM ELECTRIC FIELD ENERGY HARVESTING USING POWER LINE INSULATORS

The challenge of EFEH is to extract useful amounts of energy but to also avoid extreme close proximity (or even galvanic contact) to the power line. In this chapter [1], a novel, non-contact option for EFEH is proposed, which uses the parasitic capacitance of the medium-voltage power cable supporting insulator. Then, a detailed study of the conditions of the capacitive divider and loading conditions for maximum power transfer is developed. Supporting simulation and experimental results are included.

The first section of this chapter presents the first contribution of this thesis, which is the demonstration of a novel technique for EFEH. The approach is a non-contact solution that uses a power line insulator with an inner electrode to provide capacitive coupling to the power line, to harvest the energy. The parameters of this coupling are estimated and validated experimentally. The approach applied for these tasks can be used for further EFEH implementations that are less invasive with the power line.

The second section of this chapter presents the second contribution of this thesis, which is a more fundamental understanding of the optimisation of the power extracted by any EFEH system. The theoretical analysis identifies specific loading and operating conditions that allow maximum power transfer. By using this

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[1] Many of the contributions contained in this chapter were first published by the author in:
[1] J. C. Rodriguez, et al., Maximum energy harvesting from medium voltage electric-field energy using power line insulators, in *Australasian Universities Power Engineering Conference (AUPEC)*, Perth, Australia, 2014, pp. 1-6.

understanding, the maximum energy harvested from an EFEH system is specifically characterised and validated in simulation.

The third section of this chapter explores the feasibility of building a power electronic converter that is able to implement the conditions that allow maximum power transfer. The switching operation of candidate topologies is studied and conclusions are drawn about the most adequate conversion strategy.

3.1 EFEH with Power Line Insulators

3.1.1 The Principle of Electric Field Energy Harvesting

The general theoretical principles of EFEH are reframed first. EFEH is based on the principle that any conductor, energised at some voltage level, emits a radial electric field that contains energy. Following electromagnetic theory, an energized AC power line conductor in steady state has its excess charge distributed on its surface. Radial electric field lines are thus produced that emanate from this outer surface.

In an EFEH system, an electrode located at a distance from the conductor creates a structure in which the charge available in the conductive elements, in relation to the potential distribution (associated with the electric field pattern) can be seen as a capacitive voltage divider network. This capacitive divider network based on one single electrode is depicted in Figure 3.1, where capacitor C_1 represents the coupling between the power line and the electrode. Capacitor C_2 represents the coupling between the electrode and the ground reference.

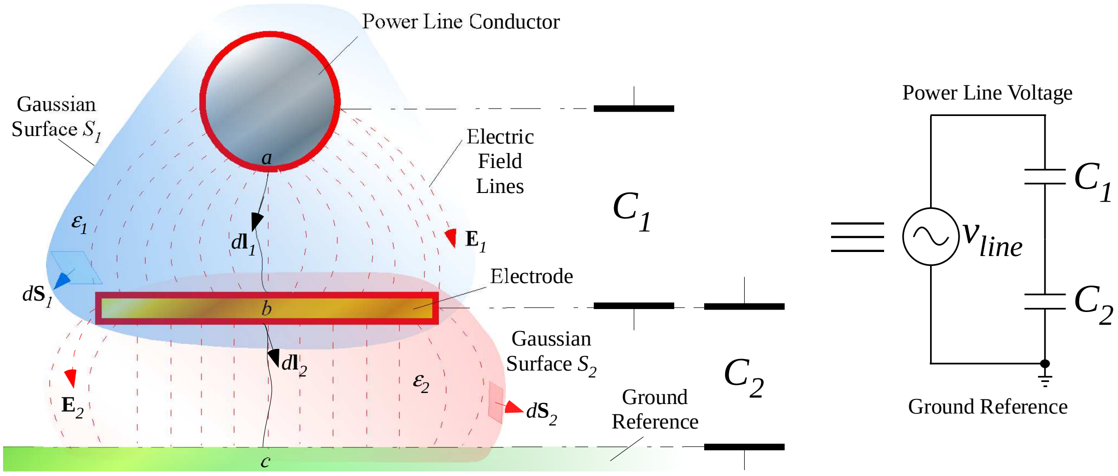


Figure 3.1: EFEH from power lines.

The value of the capacitors will be dependent on both the magnitude of the electric field in the power line and the geometry of the complete coupled system. For instance, the value of capacitor C_1 -expressed in general electromagnetic terms in (3.1a)- depends on the electric field intensity $\mathbf{E_1}$, the electric-flux-coupling Gaussian surface S_1, the total distance between the electrode and the power line l_1, as well as the permittivity of the dielectric material between the power line and the electrode ε_1, according to [137]. A similar expression can be obtained for C_2 and is given in (3.1b).

$$C_1 = \frac{\varepsilon_1 \oiint_{S_1} \mathbf{E_1} \cdot d\mathbf{S_1}}{\int_a^b \mathbf{E_1} \cdot d\mathbf{l_1}} \tag{3.1a}$$

$$C_2 = \frac{\varepsilon_2 \oiint_{S_2} \mathbf{E_2} \cdot d\mathbf{S_2}}{\int_b^c \mathbf{E_2} \cdot d\mathbf{l_2}} \tag{3.1b}$$

The energy available in the capacitive divider can be collected by deviating the displacement current from the conductor into a target load (instead to ground where it normally flows to). This is done by connecting in parallel to either C_1 or C_2 an EFEH system as shown in Figure 3.2. The EFEH system is composed of the following blocks:

- *Harvesting capacitive divider*: Formed by two or more equivalent capacitors in series, depending on the number of electrodes used. The energy is harvested by connecting the following blocks to any of the capacitors.
- *Energy conversion topology*: Transforms the AC voltages developed across the chosen capacitor down to appropriately extra-low DC voltage (ELV) levels for use by a low-power load.
- *Low-Power management system*: Electronic schemes in charge of efficiently matching the low power harvested to the consumption of the load, within some limited operation schedule, as discussed in Section 2.1.

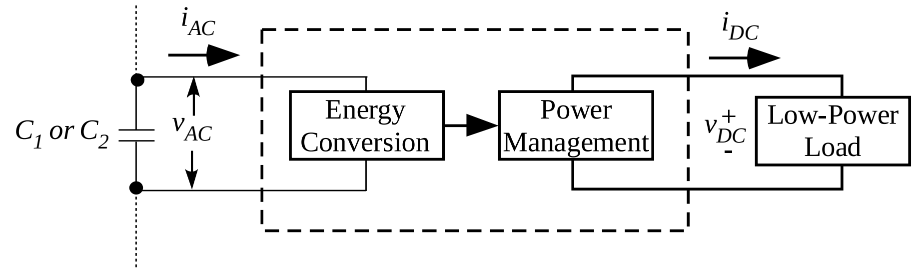


Figure 3.2: A full EFEH system.

Figure 3.3: Overhead distribution power line insulators.

- *Low-power load*: The final electronic load such as a WSN node and its peripheral devices.

A non-contact solution that uses a power line insulator with an inner electrode to provide capacitive coupling to the power line, to harvest the energy, is presented in the next section.

3.1.2 Power Line Insulators in the Smart Grid

Overhead power line insulators (Figure 3.3) are an integral part of power transmission and distribution systems. Their objective is to both support the overhead conductors and provide electric insulation between the higher-voltage line and the earth. Hence, they must be able to withstand high-voltage stress. There are several types according to the application (pin, suspension, strain, hollow-core etc.), as well as a variety of materials such as porcelain, toughened glass, polymers and composite materials.

It is well recognised that the presence of insulators in the power lines produces a leakage current to ground. Usually, leakage current in insulators is referred to as the current passing through the DC resistance path on its surface, which is more dominant than the current passing through the parallel leakage capacitance of the insulator [138].

The maximum allowed levels of leakage current are not well defined by standards organisations, but are specified instead by local power companies. These limits depend on the insulator type and voltage rating, quality of service and line losses. An empirical limit is acknowledged at 100 milliamperes [138, 139]. However, practical studies have observed leakage currents up to 1.5 amperes [140] in heavily contaminated MV devices, with the insulator operation still not compromised. Given the fact that EFEH from MV lines usually extracts currents in the level of some hundreds of microamperes [61], their use for EFEH should not affect their normal operation in power lines.

The idea of using insulators in the context of smart power line monitoring has been presented before in the literature. In [141], trending non-conventional smart grid voltage and current measurement technologies as in [12, 142] are integrated into a hollow insulator. A follow-up work [143] includes a self-powering strategy for powering the electronic circuits embedded in the sensors that uses the principle of Magnetic Field Energy Harvesting. The results indicate that such a power line monitoring system offers the benefit of being non-invasive, while keeping high accuracy and broad frequency range.

In [144], a system for monitoring insulators leakage currents in WNSs is proposed. The system uses high conductivity copper rings installed on the surface of the insulators themselves to collect the leakage current through the insulator DC resistance and transmit it as part of a sensors network. The energy consumption of the system is designed to be low, so it can be powered from an EH method.

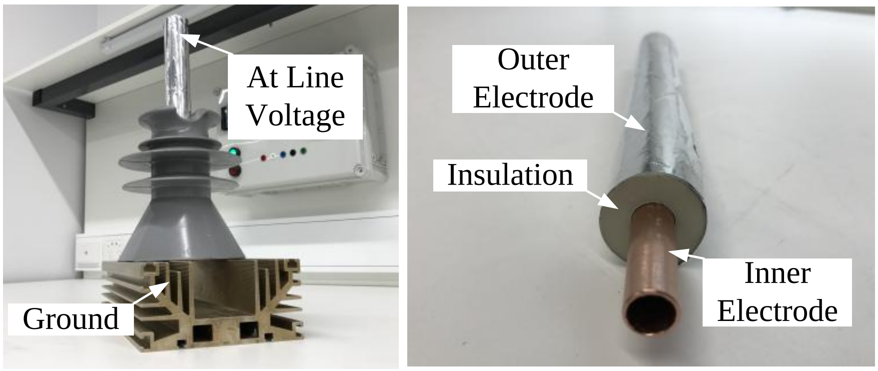
In [145], studies on smart grid non-conventional methods for MV power line voltage measurement via C and RC dividers and current measurement via inductive pickups, indicate that such sensors can be incorporated inside support insulators, with examples provided of the integration of the topologies.

Commercially, industrial projects such as [146] have proposed systems that replace conventional high voltage pin-type insulators with others of the same size that incorporate coupling electrodes, thus composing a voltage testing system where the capacitor voltage divider translates the applied phase-to earth voltage into a measurement voltage proportional to the high voltage. The application aims to retrofit a medium voltage switching system for power line control operations.

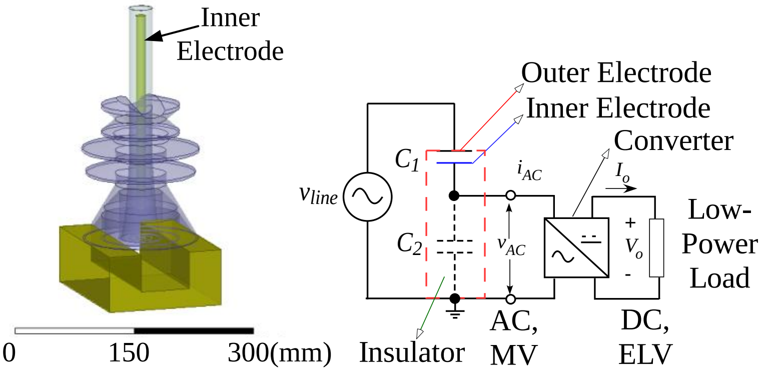
To the best knowledge of the author, power line insulators themselves have not been used as the medium for EFEH. However, the literature shows that the reported electric-field distribution patterns of power line insulators are in the same levels as the studies in EFEH [147], which encourages an EFEH application. An additional benefit is the non-invasive nature that smart grid developments using insulators have demonstrated. Finally, since insulators are an inherent requirement for the power line, using them has the advantage of reducing installation and deployment requirements in the distribution system, which is one of the challenges of power line monitoring regarding large-scale deployment.

3.1.3 Proposed Insulator-Based Harvester

The physical structure of MV power line insulators is a cascaded set of epoxy sheds that are linked by an internal connecting pin. For the proposed EFEH system, this pin is now extended beyond the top of the main insulator, surrounded by a cylindrical insulation extension, and then sheathed by an outer electrode which connects to the power line conductor. A physical proof-of-concept of this arrangement is shown in Figure 3.4a. Note that the overall geometry of the proposed harvester is not substantially different from a composite insulator for overhead power lines, which makes it a viable implementation for electrical distribution systems. A complete description of the construction of the experimental harvester is presented in Chapter 7.



(a) Harvester construction.



(b) 3D FEA model. **(c)** Conceptual conversion scheme.

Figure 3.4: Power line insulator-based EFEH system.

The structure forms a parasitic capacitive divider network as shown in Figure 3.4c, where C_1 represents the capacitive coupling between the outer electrode sheath and the inner electrode pin, and C_2 represents the (parasitic) coupling of the inner electrode pin to the pole earth. Note that in this arrangement there is no direct contact between the line and the inner coupling electrode.

Energy can be scavenged from this capacitive divider by connecting a conversion system in parallel to C_2. A stylised conversion system is shown in Figure 3.4c where a power electronic converter transforms the AC voltage developed across C_2 down to an appropriately extra-low DC voltage (ELV) level for use by a generic low-power load.

As it was identified in Chapter 2, the EFEH strategies that scavenge the energy from the high voltage capacitor of the capacitive divider i.e. C_1 are able to obtain more power. However the challenge that this creates is to have the conversion system in direct contact with the power line. The use of C_2 instead of C_1 as the connection element of the harvesting system has more limited exploration in the literature. Besides providing galvanic isolation, the use of this type of connection has the benefit of having its reference to the earth of the system rather than to the active conductor, which has the potential of reduced installation requirements and costs. The challenge with parallel connection to C_2 is to understand the conditions that will allow an increase of the available energy. The first step towards this knowledge is to recognise the input impedance of the system. In the next section, simulation and experimental studies performed in order to estimate the capacitances of this EFEH system are presented.

3.1.4 Experimental Investigations

In EFEH capacitive dividers made up of electrodes with varied geometries, Finite Element Analysis (FEA) is often used to investigate the field distribution of the experimental structure and hence to estimate the values of capacitances C_1 and C_2 in the divider. The Ansoft Maxwell 3D FEA software [148] was used in this study to analyse the system proposed in Figure 3.4, where the materials used to emulate the insulating rod and power line insulator have a relative permittivity of 2.2 and 4.4, respectively.

The FEA simulation model in Figure 3.4b includes the 3D representations of the inner Copper electrode, the insulating Polypropylene rod, and the epoxy power line insulator. In addition, the Aluminium cylindrical wrap that holds the line voltage of 12.7 kV (phase-to-ground voltage from a 22 kV distribution system), and a Copper structure that holds the ground potential, are included in the model as the excitations of the electrostatic simulation.

The resultant electric field distribution is presented in Figure 3.5 and the estimated capacitances based on the analysis are: $C_1 = 43.111\text{pF}$ and $C_2 = 0.1437\text{pF}$. The FEA results confirm that the maximum field intensity is well below the material dielectric breakdown of the insulating rod and the power line insulator i.e. 30 and 19.7 Megavolts/metre respectively. The value of capacitance C_1 is similar to other studies in the literature, some tens of picofarads, as identified in Chapter 2.

In order to validate the estimations of the FEA simulation in practice, an experiment was designed. An AC voltage of 1.14 kV (RMS) at 50 Hz was connected between the Aluminium wrap and the ground plane. The distance between the medium voltage potential and the inner electrode electrode is 10 mm, which is more than enough to sustain the test voltage according to the dielectric strength levels of the insulating materials mentioned above.

Different known resistive loads R_L were connected between the harvesting electrode (Copper tube) and the ground reference, i.e. across capacitor C_2. The steady state, RMS voltage across the resistor R_L was then measured for each load. The equivalent circuit of this arrangement is shown in Figure 3.6a. The experimental setup is shown in Figure 3.6c.

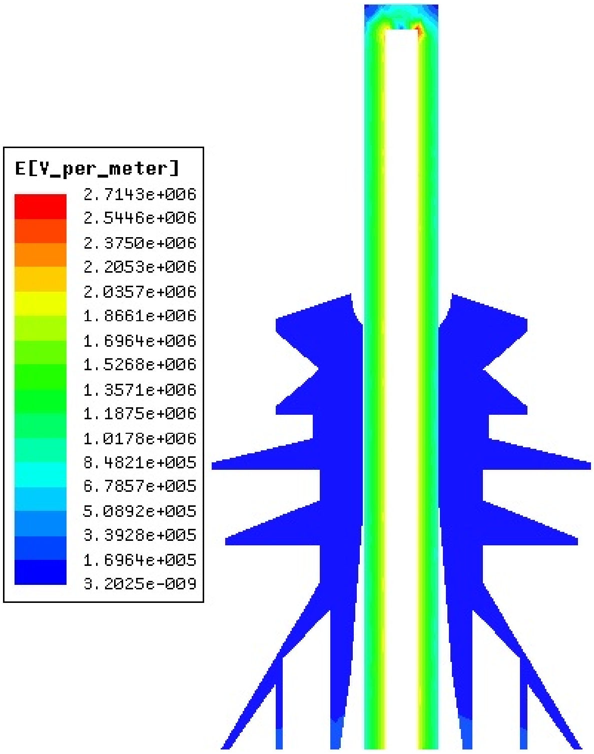
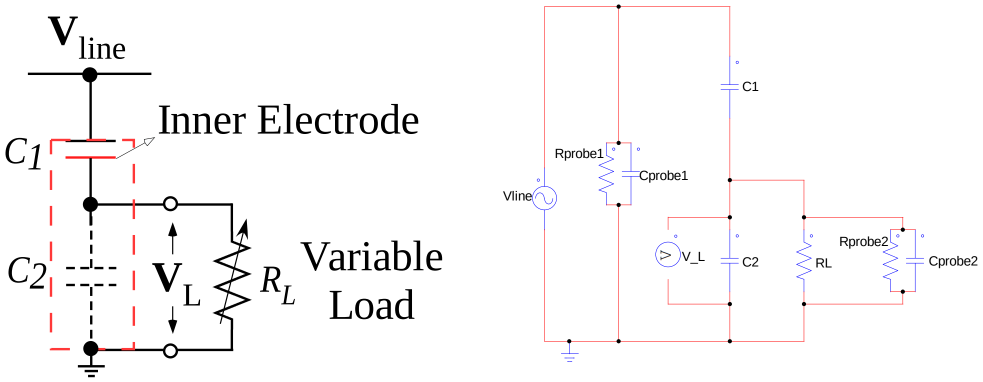
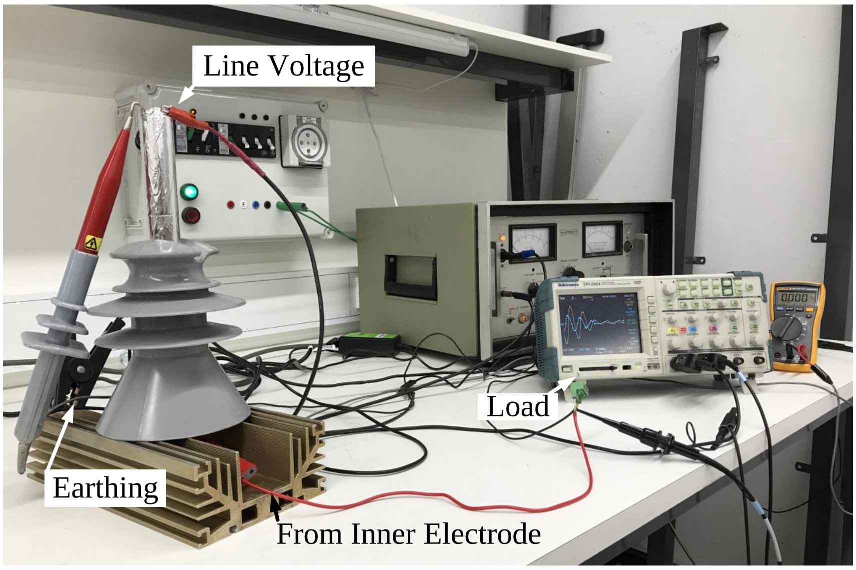


Figure 3.5: Electric field distribution FEA results.



(a) Equivalent circuit.

(b) Simulation.



(c) Experimental setup.

Figure 3.6: Experimental validation methodology.

In this experiment, the input impedances of the capacitive divider at the line frequency are in the range of several Mega-ohms. Hence, the load voltage drop is very low for loads with impedances lower than this input impedance, making it difficult to make test measurements. On the other hand, the use of high impedance loads will inevitably influence the measurement of the load voltage because these impedances will be comparable to the impedance of the voltage probes used for the measurement i.e. they will produce loading effects.

To address this issue, high-impedance loads were used and the experimental measurements of the load voltage V_L were compared to analytical models that take into account all the impedances present in the circuit. A simulation of the experimental circuit was implemented using the PSIM software package. The simulation utilizes the values of C_1 and C_2 that were predicted by FEA. It includes models of the TEKTRONIX P5100A voltage probe, which was used for the measurement of both the line voltage and the load voltage, to take into account

Table 3.1: Experimental validation results of the proposed EFEH system.

R_L	V_L **experiment (V)**	V_L **simulation (V)**	**Error (%)**
$100.00k\Omega$	1.65	1.66	0.71
$2.19M\Omega$	33.70	34.29	1.73
$3.99M\Omega$	59.00	59.87	1.45
$7.07M\Omega$	94.70	98.92	4.27
$8.32M\Omega$	110.00	114.20	3.68
$23.98M\Omega$	220.00	242.39	9.24
$61.98M\Omega$	342.00	380.10	10.02

the loading effect that the probe introduces in the circuit. As per the information in [149] the model of the voltage probe P5100A is a 40 MΩ resistor (value assigned to *Rprobe*1 and *Rprobe*2) in parallel with a 1.5 pF capacitor (value assigned to $Cprobe1$ and $Cprobe2$). The simulation model is presented in Figure 3.6b.

Table 3.1 shows the experimental results versus the simulated V_L voltages. The discrepancies that are observed are due to second order effects of the voltage probes that are more relevant in this study due to the test impedances being comparable to the impedances of the probes. Overall, the experimental results match the simulation with an average difference error of 4%, which is sufficiently close to validate the capacitance predictions made by the FEA software.

3.2 Maximum Power Transfer

In the EFEH system proposed in Figure 3.4c, a follow-on energy conversion stage connected across C_2 is required to transform the energy from the MV system into extra-low DC voltage levels that are usable by a subsequent low-power load. To maximize the power obtained with this configuration is one of the challenges in this field of study.

Some previous works in the literature have considered that the energy available from the EFEH systems is simply the energy in the capacitor used for harvesting, in this case C_2. However, the AC voltage divider (considered to be composed of ideal capacitances in this model) transfers various amounts of active power depending on the load connected across one of its arms. Because of the sensitivity of this system to loading effects, which was identified in the previous section, a closer look at the effect of the load connected across C_2 is required.

This section will firstly analyse the effect of resistive loads on the power transfer as a basis for understanding the system under loading, and then will derive the

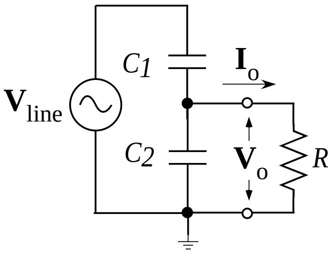


Figure 3.7: EFEH system with a resistive load.

conditions needed for power transfer maximisation in the more general case of a converter acting as the load of the divider.

3.2.1 Resistive Load Analysis

The steady state AC circuit analysis of the capacitor divider shown in Figure 3.7 for a load resistor R was performed. Eqn.(3.2) defines the resultant RMS output load voltage V_o , RMS output current I_o, and average delivered power P_o.

$$V_o = \frac{RC_1\omega_o V_{line}}{\sqrt{1+R^2{\omega_o}^2(C_1+C_2)^2}} \tag{3.2a}$$

$$I_o = \frac{C_1\omega_o V_{line}}{\sqrt{1+R^2{\omega_o}^2(C_1+C_2)^2}} \tag{3.2b}$$

$$P_o = \frac{RC_1^2{\omega_o}^2 V_{line}^2}{1+R^2{\omega_o}^2(C_1+C_2)^2} \tag{3.2c}$$

In these circuit analysis results, the angular frequency ω_o is a stiff grid parameter. Capacitor C_1 depends on the geometry of the harvester only, as in eqn. (3.1a). With respect to C_2, although its minimum value depends on the geometry of the harvester, any element connected across its terminals will in fact add more capacitance, so it cannot be considered constant. Hence, for a given line-to-ground reference voltage V_{line}, R and C_2 are the degrees of freedom considered in this study.

Figure 3.8 shows the variation in RMS output voltage and current, as well as the average power as functions of the two independent variables R and C_2. A 22 kV, 50 Hz distribution system was considered (12.7 kV line-to-earth) with C_1=40 pF, which is the approximate value estimated for the EFEH system proposed in Section 3.1.4.

The results show that a reduction in the value of C_2 results in an increase of all the output variables. This is in fact obvious when it is recognised that reducing C_2 to zero is equivalent to removing this capacitor from the circuit, which diverts the

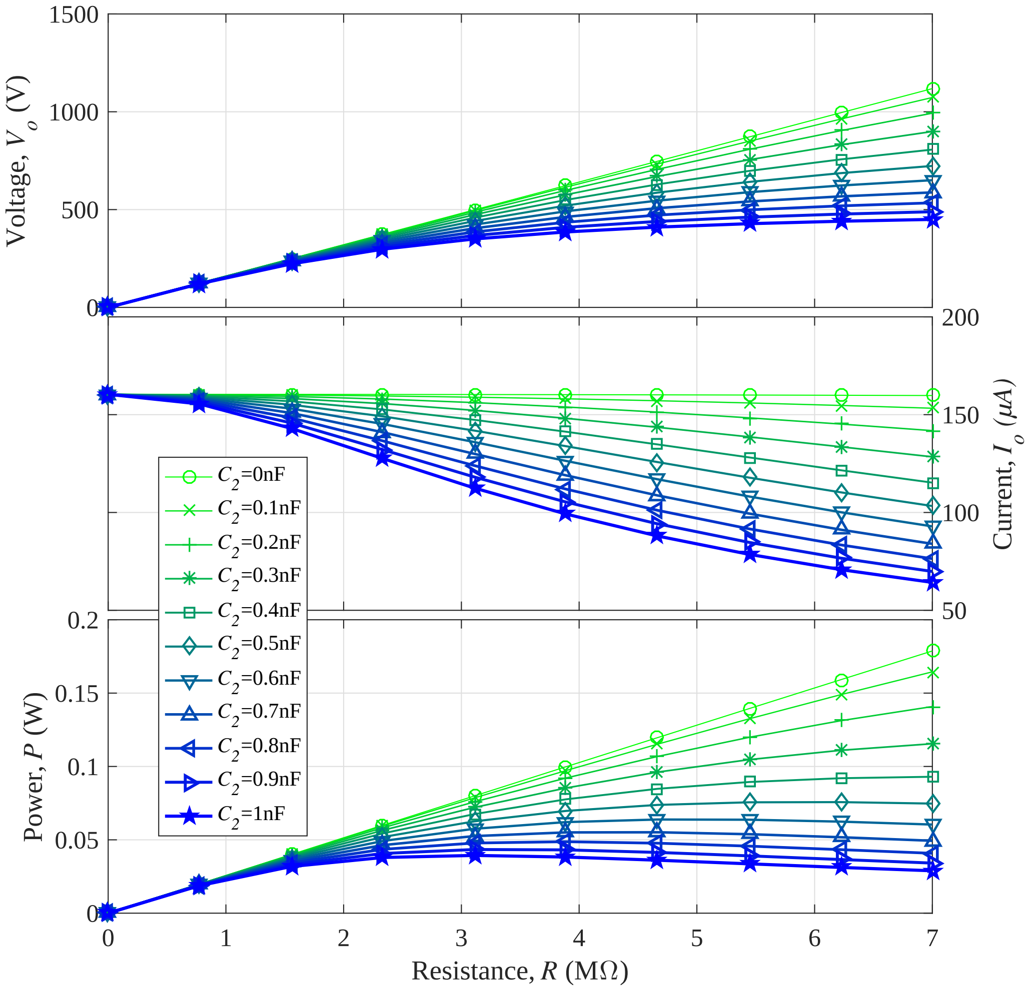


Figure 3.8: System variables under resistive load.

displacement current from the capacitive divider directly to the resistive load and hence maximises the output power transfer.

For the case where C_2 is essentially zero, increasing R causes both the voltage and power to rise, while the current remains practically unchanged. Thus the capacitively coupled line acts effectively as a current source.

One conclusion from this load analysis is that in order to maximise the power obtained from an EFEH system, the capacitance across which it is connected has to be reduced ideally to zero, while the load presented to the system has to look like an ideal resistor.

Since the source current effectively stays constant, increasing the load resistance increases the load voltage and thus the available power. However, in practice the load voltage will be developed across the input terminals of the subsequent conversion system in Figure 3.4c, and hence it cannot be higher than it is sustainable for the components of the converter. Therefore, the problem of maximising the power

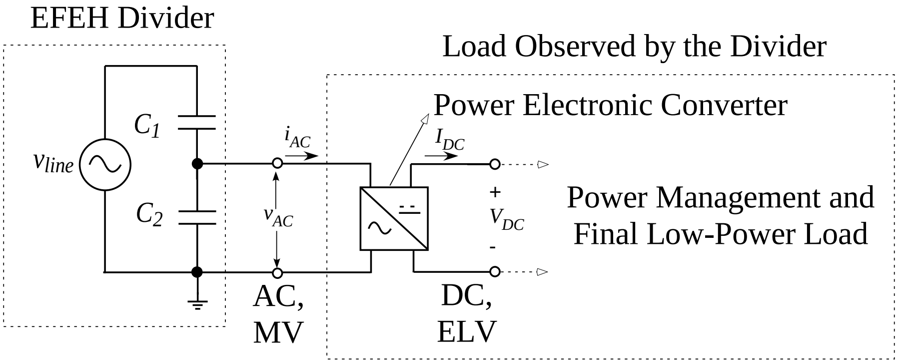


Figure 3.9: EFEH system loaded with an energy conversion system.

extracted from the EFEH system is bounded by the value of the maximum output voltage allowed in the conversion system.

The results in Figure 3.8 show that for the proposed EFEH system with an input impedance Z_1 of nearly 80 MΩ, and assuming a capacitance C_2 equal to zero, nearly 118 mW can be extracted from a 22 kV power system into a resistive load of 4 MΩ, if a maximum of about 687 Vrms (970 Vpeak) is allowed to develop across this load. A current of around 170 μA then circulates through C_1 and R. A more general analysis for non-resistive loads is discussed in the next section.

3.2.2 General Load Analysis

In more practical terms, the overall objective of the EFEH system is to deliver an appropriate power supply for the final load, which is conceptually a WSN node in charge of power line monitoring. An exemplary load of this nature is a ZigBee®power line monitoring mote in [82], based on a MSP430 microcontroller with an input supply requirement of ˜3.6 VDC.

Depending on the instantaneous power requirement of the final load, the energy conversion stage of the EFEH system will be an AC-to-DC converter with varying input AC voltages of potentially high values (up to the kV range), that is able to deliver regulated DC extra-low-voltage (ELV) to a low-power load (which in the context of Figure 3.9 includes any necessary power management system and the final load itself). The power electronic converter in Figure 3.9 is based around semiconductor devices (diodes or/and transistors) that are connected to the terminals of C_2.

As it was shown in the previous section, in order to maximise the power obtained from the divider, capacitance C_2 has to be minimised, ideally to zero; the load presented to the divider has to be close to an ideal resistor; and the higher the output voltage, the more energy can be harvested. However, in the system in Figure 3.9:

- Making C_2 equal to zero is not really practical, since it depends on the environmental conditions inside the pin cavity and, more importantly, it will be enlarged by any system connected in parallel.
- The AC divider does not necessarily see a resistive load.
- The semiconductors implementing the conversion stage are limited by their breakdown voltage. Hence, the voltage at the output of the harvester, $v_{AC}(t)$, cannot exceed the semiconductor breakdown voltage (around 1 kV).

It is clear that a more general analysis should include the limit of the voltage across the converter input and the nature of its current consumption.

In Figure 3.10, the EFEH capacitive divider has been replaced with its Thévenin equivalent and the load at the harvester output terminals has been replaced by a virtual dependent source which draws from the harvester a current $i(t)$ while keeping a voltage $v(t)$ across its terminals. In this steady state AC system, the reference source is the phasor $\mathbf{V_{line}}$ of Figure 3.9.

The Thévenin equivalent voltage source and its input equivalent impedance (which is simply a series capacitor) are given by:

$$V_{th} = \frac{C_1}{C_1 + C_2} V_{line} \tag{3.3a}$$

$$C_{th} = C_1 + C_2 \approx C_1 \tag{3.3b}$$

For a steady state output voltage limited to an RMS value of V, represented by the phasor: $\mathbf{V} = V\underline{/\delta_V}$, the power injected into the virtual load can be expressed using:

$$P = \omega_o C_{th} V_{th} V \sin(\delta_V) = \omega_o C_1 V_{line} V \sin(\delta_V) \tag{3.4}$$

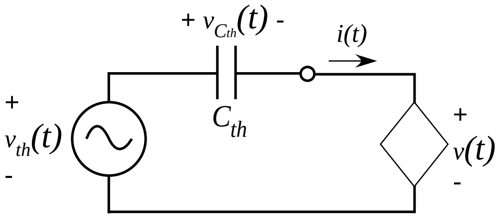


Figure 3.10: Thévenin equivalent of the EFEH system.

This power relationship states that, in order to get the maximum power from the harvester:

(a) The line angular frequency and voltage must be maximised. These conditions are usually fixed.

(b) Capacitor C_1 has to be as large as possible. In EFEH strategies, this condition implies manipulating the geometry of the harvester, as discussed in Section 3.1.4.

(c) The voltage V at the load terminals has to be kept high, but below the semiconductor breakdown levels.

(d) The phase angle between the line voltage and the load voltage has to be 90°.

Note that according to (3.4), the maximum harvested power does not depend on the value of C_2. The conditions that lead to maximum power transfer are represented in the phasor diagram of Figure 3.11. In particular, condition (d) is fulfiled by a specific magnitude and phase angle of the circuit current, which can be calculated analytically.

For a given AC supply $[V_{line}, \omega_o]$, with a harvester coupling capacitance C_1 and a pre-selected load voltage V, the current that is being drawn from the harvester, $\mathbf{I} = I\underline{/\delta_I}$ can be calculated by simple circuit analysis. Assuming $\mathbf{V} = V\underline{/90^\circ}$ in order to fulfil condition (d) for maximum power transfer, the solution for the magnitude and phase of the current is given in (3.5).

$$I = \omega_o C_{th}\sqrt{V_{th}^2 + V^2} \tag{3.5a}$$

$$\delta_I = \arctan(V_{th}/V) \tag{3.5b}$$

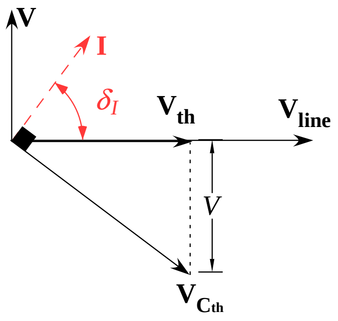


Figure 3.11: Phasor diagram at maximum power transfer.

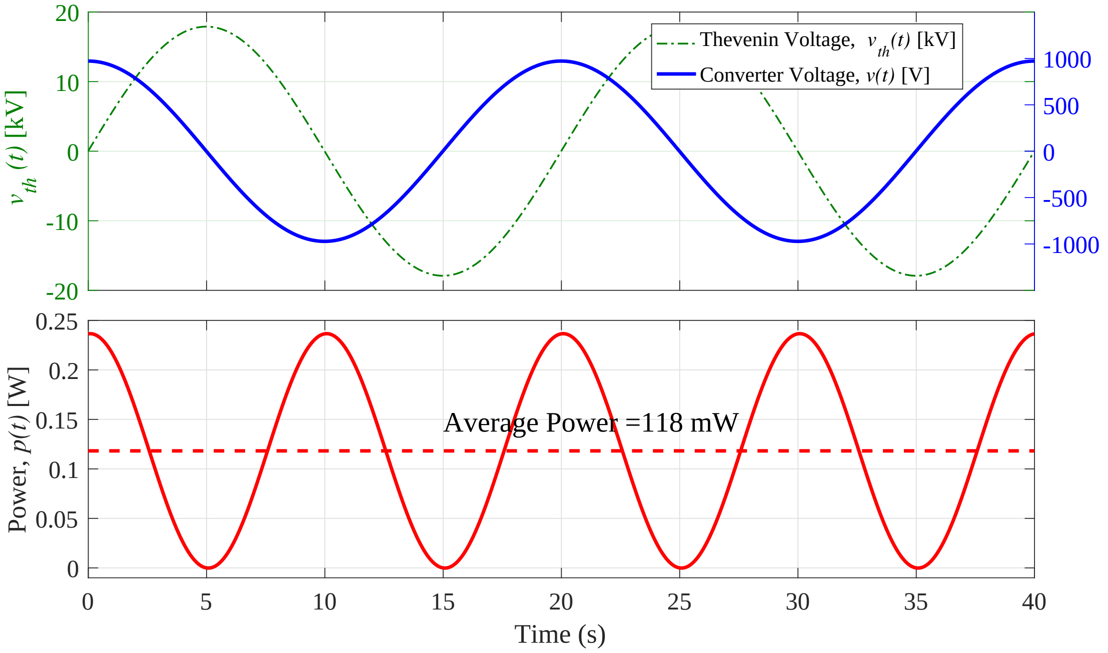


Figure 3.12: Simulation results for optimal power transfer.

In order to illustrate this principle, a PSIM simulation was performed. A 22 kV/50 Hz distribution system and the harvester capacitances predicted by the FEA in Section 3.1.4 are considered i.e. $C_1 = 43.11$ pF and $C_2 = 0.144$ pF. The working voltage at the harvester terminals was selected to be 687V(RMS) (peak of 970V) as a realistic, safe voltage for any semiconductor chosen to implement the system conversion stage. These conditions are similar to the ones used in Section 3.2.1, to allow a comparison to be made.

From (3.5), the current required for maximum power tracking in this case study is $\mathbf{I} = 172.3\underline{/86.9^\circ}[\mu A]$. This current value was programmed in an ideal dependent current source, which acts as the AC load in the circuit simulation. Simulation results over two cycles are presented in Figure 3.12. The load voltage is orthogonal to the Thévenin source voltage and is limited to about 970 V(peak), as required by condition (d) for maximum power transfer. The average power transferred to this virtual load is 118 mW, which is close to the result in Section 3.2.1 for a pure resistive load of 4 MΩ.

These results indicate that about the same power from an output-voltage-limited EFEH system with a purely resistive load, can be achieved with a non-resistive current-controlled load, without requiring C_2 to be reduced to zero.

The maximum power that can be harvested from the insulator-based EFEH system under study is about 110 mW, which in theory can be achieved by synthetising a 170 μA load with a power factor of $\cos(90^\circ - 86.4^\circ) = 0.998$, while keeping a voltage of 970 V(peak). This voltage is a safe level for any semiconductors that are connected at the terminals of the harvester output that are part of the subsequent conversion system, which is investigated in the next section.

3.3 Implementation in Solid-State Converters

In the last section, the fundamental conditions for the optimisation of the power transfer in a non-contact EFEH system were developed. The power extracted from an EFEH capacitive divider is maximised if the load presented to it looks essentially resistive, with an AC voltage that is orthogonal to the line voltage. Also, the power obtained is proportional to the amplitude of the AC voltage of the load.

The AC-to-DC power electronic converter that will ultimately be in charge of implementing these conditions (depicted in Figure 3.4c), in practice should limit its input AC voltage v_{AC} to about 1000V (peak) in order to operate with realistically rated semiconductors that could be sensibly used in the conversion system.

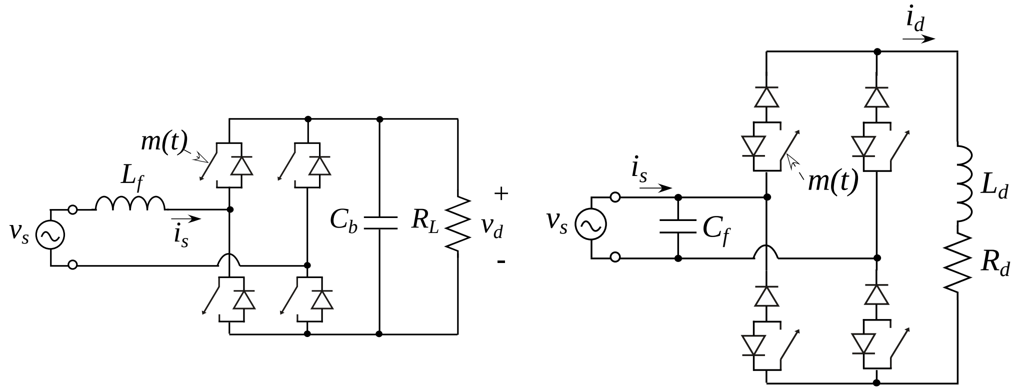
The first aim is to manage this input medium-voltage directly, in constrast to previous studies where an initial voltage reduction stage was used. With this constraint, the input AC current to the converter i_{AC} will have very low magnitudes (˜microamperes). These overall input conditions are unusual for a standard power electronic converter.

This section will explore the feasibility of implementating the conditions for maximum EFEH power transfer using a solid stage converter. First, single-stage, active front end rectification will be considered. Then a more traditional passive front end, double-stage conversion scheme will be studied.

3.3.1 Active Front End Rectification

The objective of an AC-to-DC, single-stage converter is to directly transform the input medium-voltage (˜1000 Vpeak), low-current (some hundreds of microamperes) AC supply, to DC voltage levels that are appropriate to energize the subsequent blocks in the EFEH system (Figure 3.2), which are in the extra-low-voltage (ELV) range i.e. lower than 120VDC.

At the same time, in order to achieve maximum power transfer the proposed converter has to absorb the power in such a way that its input voltage v_{AC} is orthogonal to the line voltage v_{line}. As it was shown in Section 3.2, this can be accomplished by shaping the input current i_{AC} to have a pre-determined magnitude and phase-shift with respect to the line voltage.



(a) Voltage source rectifier **(b)** Current source rectifier

Figure 3.13: Active Front Converter Topologies.

AC-to-DC converters (rectifiers) can be classified between topologies working with low switching frequency (line-commutated) and other circuits which operate with high switching frequency. From the latter group, pulse width-modulated (PWM) regenerative rectifiers, also known as active front end (AFE) converters integrate switches to change the waveform of the input current actively [150, 151]. Hence, these type of rectifiers have potential for the conversion problem under study.

An active front converter is nothing more than an inverter working with reverse power flow, controlling the DC voltage (or current). They can be classified as Voltage-Source Rectifiers (VSR) and Current-Source Rectifiers (CSR), and their basic topologies are depicted in Figure 3.13a and Figure 3.13b respectively.

A single-phase VSR bridge includes in its topology an input filter inductor L_f for its operation as it relies on inductive coupling to the input power supply. Hence, this topology is clearly not appropriate for the conversion of an EFEH supply, which offers capacitive coupling. Furthermore, for appropriate operation of a VSR, its DC output voltage must be greater than the input voltage at any time, since the nature of such a topology is that of a boost-converter. However, the application under study requires the output DC voltage to be at ELV levels, which means that the peak value AC input voltage could not exceed, say 20V. Since the power obtained via EFEH was found to be proportional to the AC input voltage (eqn. 3.4), then the use of a VSR would also reduce dramatically the power harvested.

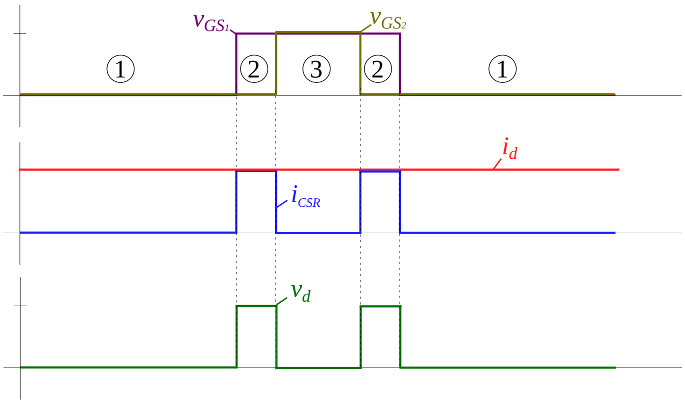
Current Source Rectifiers (CSRs) are the dual of VSRs [151, 152]. A CSR bridge uses four controlled power switches with diodes in series with each of these switches, to produce a controlled DC output. Since CSRs rely on capacitive coupling to the power supply (represented by C_f) and are by nature voltage-buck-converters, they are more appropriate for the study of active front end conversion from an EFEH input.

The input current in a CSR can be controlled using modulation techniques and control strategies completely analogously to the ones used in VSIs [153, 154]. Therefore, in theory the conditions for maximum power transfer from EFEH derived in Section 3.2 can be practically realized with the use of CSRs by using control strategies to regulate either the current or the voltage at the input of the converter.

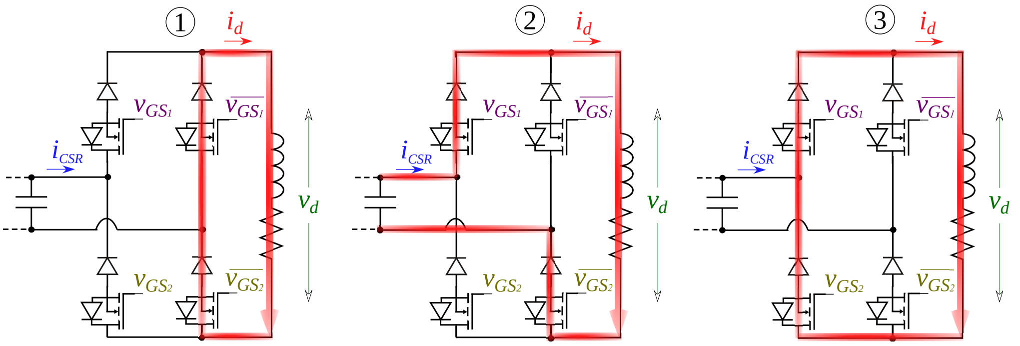
The switching patterns of a PWM-controlled CSR for one carrier cycle are shown in Figure 3.14a, with the equivalent circuits of each switching interval depicted in Figure 3.14b. The output voltage of a CSR changes from zero to positive as the phase legs of the converter do and do not create a short circuit through a pair of non-complementary switches.

In practice, maximum power transfer conditions require semiconductors with the highest voltage breakdown as possible (˜1000V in commercial devices). At the same time, they have to operate at very low switching currents (some hundreds of microamperes). The question of how well high-voltage-rated switches perform at currents well below their ratings is essential for assessing the viability of an active front end rectifier in an EFEH application.

To address this question, the experiment shown in Figure 3.15 was conducted. A CSR bridge is supplied from a low-voltage AC input v_i of 100 V (RMS) at 50 Hz,

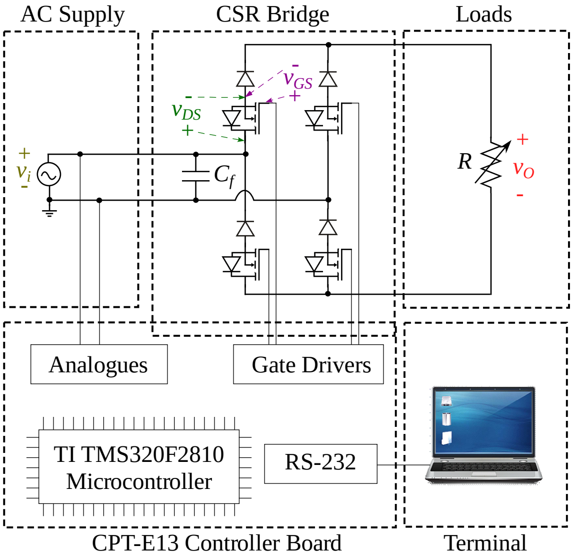


(a) Switching waveforms

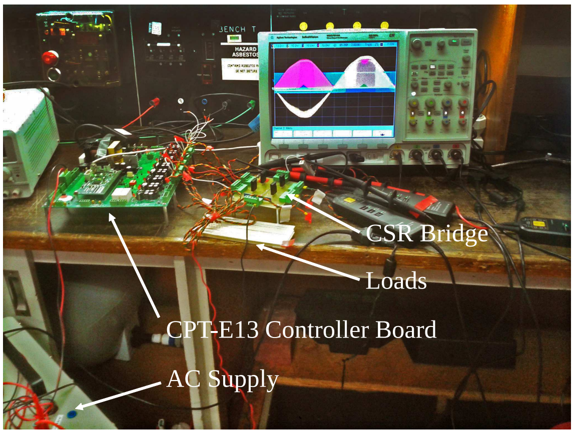


(b) Equivalent circuits

Figure 3.14: CSR PWM switching patterns in one carrier cycle.



(a) Circuit



(b) Experimental setup

Figure 3.15: Low-current switching experiment.

producing a low-voltage DC output v_o. The experimental setup was implemented with state-of-the-art semiconductors chosen for their high-voltage-breakdown ratings and low leakage currents (see Chapter 7). The switching converter was commanded with asymmetrical PWM with a fundamental frequency of 50 Hz. The range of test load resistors was designed for currents that range between 4 μA and 300 mA. The parameters of the experiment are summarised in Table 3.2.

The objective of the experiment was to observe the relationship between the Gate-to-Source $v_{GS}(t)$ and the Drain-to-Source $v_{DS}(t)$ voltages of the MOSFETs, during the ON/OFF transitions of high-frequency switching, at different load currents. Two significant results are presented in Figure 3.16a and Figure 3.17a, that show commutation events for currents of 300 mA and 20 mA, respectively.

In both cases, the OFF-to-ON transition occurs at the expected rate i.e. when the switches are commanded a positive v_{GS} , v_{DS} decays to zero within the expected time

Table 3.2: Low-current switching experimental parameters.

Variable	**Value**	**Comments**
V_i	415V(RMS)	Max. voltage in LV lab.
ω_o	$2\pi \times 50$ rad/s	Nominal line frequency
M	0.93	For linear modulation, no pulse dropping
f_c	20kHz	Common PWM carrier frequency
δ_I	0°	Phase-shift with respect to v_i
R	[32.5Ω, 8.06MΩ]	Load resistors

interval (100 ns in these devices). However, the ON-to-OFF transition for 20 mA switching current is much slower than for 300 mA. As switches command a negative v_{GS}, the voltage v_{DS} in Figure 3.17 rises much more slowly than in Figure 3.16, following a first order response with a delay time much longer than the expected standard OFF time (25 ns in these devices).

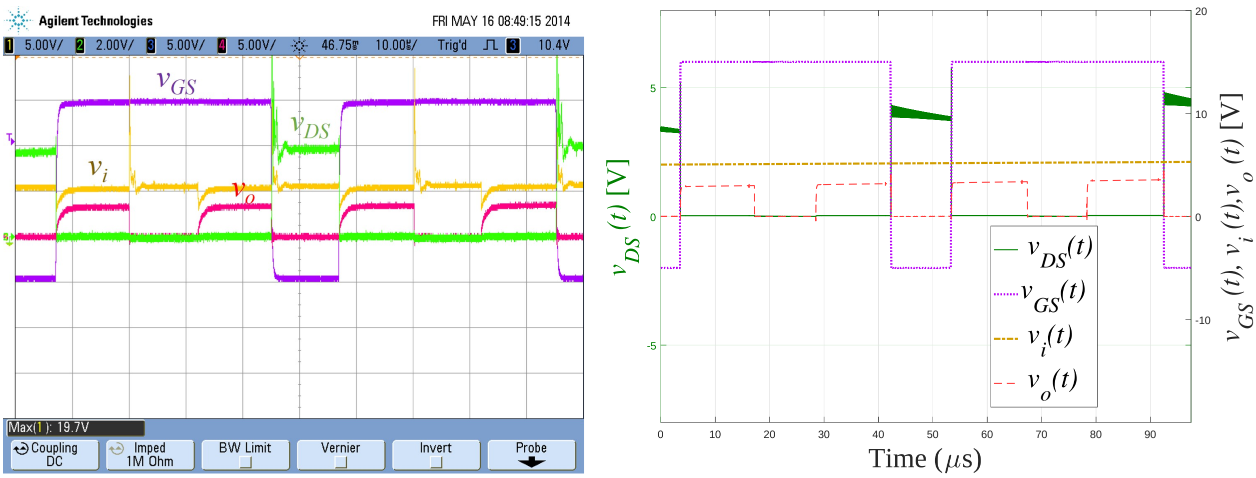
Further observations confirmed that for currents lower than 20 mA, v_{DS} takes even longer to build up from zero during the OFF switching interval. This deteriorates the switching operation, which has a direct impact in the quality of the output response, as it can be confirmed by observing $v_o(t)$ in Figure 3.17.

The explanation for this commutation behaviour can be found by exploring in more detail the physical characteristics of the MOSFETs. The construction of this type of semiconductor gives rise to parasitic capacitances between: Gate and Drain C_{gd} (Miller capacitance), Gate and Source C_{gs}, and Drain and Source C_{ds}. These parasitic capacitances are shown in Figure 3.18.

The displacement charge due to ON/OFF voltage transitions at the gate of each MOSFET are represented by the processes of charge and discharge of these non-linear parasitic capacitances [155, 156]. Essentially, during the OFF interval, capacitance C_{ds} recharges slowly from the source due to the large circuit resistance that in this case represents the low switching current (larger time constant).

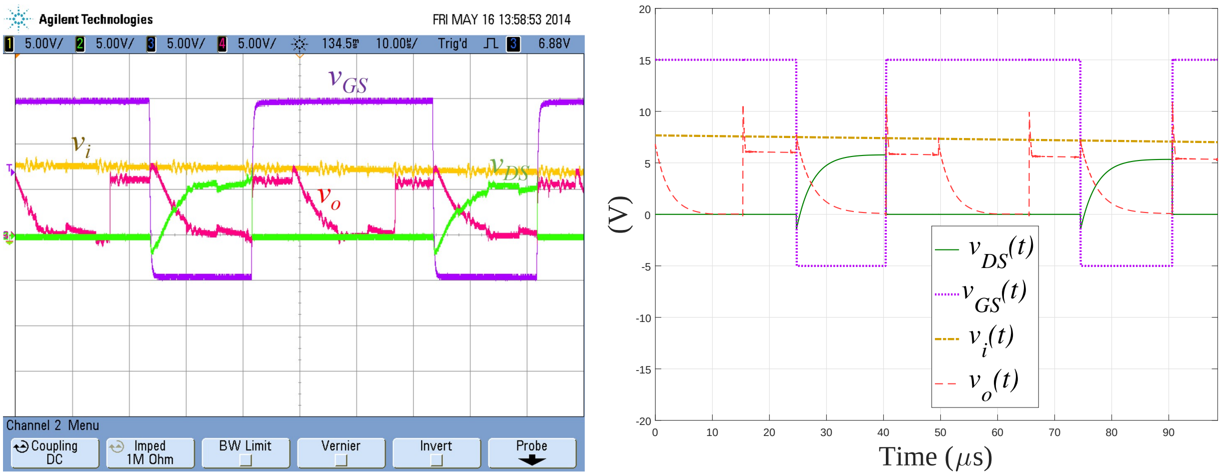
In order to validate this hypothesis, a meticulous PSIM simulation model of the experiment was developed, taking into account the parasitic impedances of the MOSFETs, measurement probes and peripheral circuitry to reproduce the experimental setup. A complete description of the model is presented in Chapter 6. The simulation results are presented in Figure 3.16b and Figure 3.17b, next to the experimental results for comparison, where a good match between experiment and simulation can be seen. This confirms the understanding as to why the switching times of the devices dramatically increase as the source current reduces.

In conclusion, semiconductor devices with ratings that meet high voltage requirements generally have parasitic capacitances of similar magnitude as the extremely



(a) Experiment **(b)** Simulation

Figure 3.16: Low-current switching experiment results at 300 mA.



(a) Experiment **(b)** Simulation

Figure 3.17: Low-current switching experiment results at 20 mA.

small values of the AC input capacitor divider in EFEH. For example, if an active front end AC-to-DC converter were to be directly connected across C_2, the (say) 1700V FET devices that would be appropriate to block the 970V+ AC input voltage have parasitic drain-source capacitances of 100 pF. If two of these devices are configured as a phase leg across the AC input voltage, the available 170 μA AC input current would lead to a phase leg commutation time of nearly 0.5 milliseconds, as the parasitic capacitances of each phase leg device charge/discharge.

Clearly any form of high frequency switching process is impossible with such a long phase leg transition time, which means that a continuously switched high-frequency active converter system will be quite ineffective in this context.

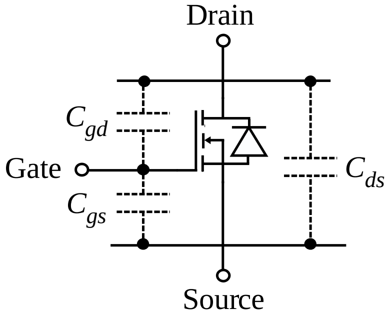


Figure 3.18: MOSFET equivalent circuit with parasitic capacitances.

3.3.2 Passive Front End Conversion

The alternative to single-stage, high-frequency active front end rectification is a more traditional conversion system composed of two stages: an AC-to-DC line-commutated rectifier to transform the MV supply at low-frequency switching; and a DC-to-DC voltage regulator to transform the relatively high-voltage DC bus to the ELV range. This topology is shown in Figure 3.19.

The conditions for maximum power transfer from an EFEH input are initially determined by the front end converter in the scheme of Figure 3.19. This converter is line-commutated, meaning that the rectification is not controlled i.e. passive front end conversion. The simplest implementation of this scheme is a diode bridge rectifier(DBR). The prospect of a DBR for the conversion of the low-current EFEH input is better than for an active front end converter because the switching occurs at low-frequency, ensuring that the slow commutation times have less impact on the switching process.

With respect to the implementation of the follow-up DC-to-DC conversion stage, the conventional theory of switched-mode power supplies (SMPSs) can be considered [157] since it makes a good prospect for the needed voltage regulation. However due to the requirement of high-frequency switching, this type of DC-to-DC regulation still

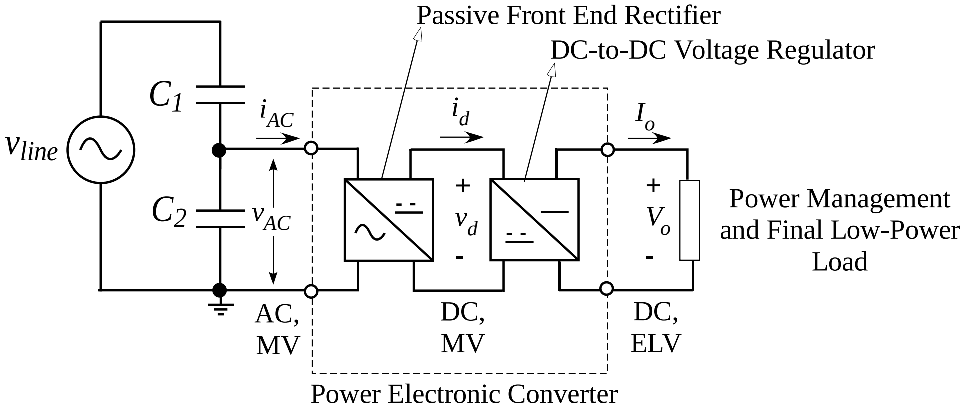


Figure 3.19: Two-stage conversion system for EFEH.

faces the same conversion challenges of continuously switched high-frequency active converters discussed in Section 3.3.1. In the next chapter, a conversion methodology that addresses these limitations will be presented.

3.4 Summary

This chapter has been presented in three sections. The first section introduced a novel strategy for EFEH from medium voltage distribution feeders, with no galvanic line contact required. The approach uses a power line insulator with a cylindrical structure that provides the capacitive coupling to the power line, to harvest the energy. The parameters of this coupling have been estimated in FEA simulations and then experimentally validated. The capacitive divider that couples the power line with the harvesting system is in the order of magnitude of 40 pF for C_1.

The second section of this chapter has developed a novel study of the fundamental conditions for the optimisation of the power obtained from an EFEH system. Theoretical analysis identify specific loading and operating conditions that allow optimum power transfer. An AC-to-DC power electronic converter in practice should limit its input voltage to about 970 V(peak). It was shown that if the converter is able to present to the divider an AC load voltage that is orthogonal to the line voltage, maximum power will be transferred. This condition can be achieved by synthetising an input current of deterministic values of magnitude and phase. The maximum possible energy that could be harvested with the insulator-based EFEH system, from a 12.7 kV line, is approximately 110 mW, while maintaining a 170 μA load with a power factor of 0.998, for a load voltage of 970 V(peak).

The third section studied the feasibility of the implementation of a practical conversion system for EFEH that is able to keep the proposed conditions for optimal power transfer. The study of active front end rectification with a Current Source Rectifier (CSR) illustrated that any form of high-frequency conversion under the input constraints of EFEH is impractical. This is mainly because semiconductor devices with ratings that meet the high input voltage requirement have parasitic impedances that lead to extended phase leg commutation times, degrading the switching performance.

On the other hand, the study of a more traditional passive front end conversion scheme showed that while the AC-to-DC conversion of the EFEH input using a diode bridge rectifier (DBR) is feasible, the subsequent DC-to-DC regulation still faces the same conversion limitations of direct active front end AC-to-DC conversion. A

DC-to-DC conversion strategy that is able to tackle these challenges will be presented in the next chapter.

Chapter 4

Pulsed-Mode Flyback Conversion For Electric Field Energy Harvesting

In Chapter 3 the conditions for maximum power extraction from a galvanically isolated EFEH system were derived. Essentially, the scavenged energy is maximized by allowing the voltage developed across the input capacitor divider to be as large as possible because the weakly coupled MV supply essentially acts as a current source. Any power electronic converter with the task of making this energy usable therefore has to resemble a large resistance comparable to the EFEH input impedance.

The practical implementation of a converter that can fulfil these requirements is limited to passive front end rectification, because any form of high-frequency, active front end strategy is impractical for this type of system. In addition, the low input current of an EFEH supply does not allow for any subsequent DC-to-DC conversion scheme to switch continuously. Hence, any form of conventional, continuous DC voltage regulation is impractical too.

This chapter [1] now presents a novel energy conversion approach for EFEH that rectifies the weakly coupled AC supply into a high voltage DC source, and then uses a flyback converter operating in discontinuous mode to transform this voltage down to levels that are useful for electronic systems. The investigation has identified that up to 17 mW of continuous power from a 12.7kV MV line can be extracted using this principle. Matching simulation and experimental results are presented to validate this performance.

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[1] Many of the contributions contained in this chapter were first published by the author in:
[2] J. C. Rodriguez, et al., Energy Harvesting from medium voltage electric fields using pulsed flyback conversion,in *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Hefei, China, 2016, pp. 3591-3598.

4.1 Discontinuous DC Voltage Regulation

The principle of discontinuous conversion is shown in Figure 4.1, where the AC EFEH supply of Section 3.2.2 is once again considered (V_{line}=12.7 kV, C_1=40 pF). Following the basis of low-frequency front end conversion, the input is rectified using a DBR. On the DC side a virtual, controlled current source absorbs pulses (or bursts) of current with peak values I_{DC} only during time intervals t_{ON}, wih a frequency f_s. Because the load is not absorbing power continuously, but rather intermittently, the operation is regarded as discontinuous. The bus capacitor C_b is considered to be zero for this case study.

This duty cycle D_I of discontinuous current absorption is defined analytically with the familiar equation (4.1).

$$D_I = t_{ON} f_s \tag{4.1}$$

Hence, the average value of the DC current $i_d(t)$, I_d can be expressed as:

$$I_d = D_I I_{DC} \tag{4.2}$$

This scheme is investigated in a case study that uses current pulses of $I_{DC} = 100$ mA, which according to the experimental studies in Section 3.3.1 is a suitable value for any switching semiconductor to operate adequately in an EFEH application. Since the low current supplied from the EFEH system is in the level of microamperes, a sensible approximation to emulate this input is $I_d \approx 100\mu$A. From (4.2), this yields a test duty cycle of D_I =0.1%. Finally, an appropriate approximation for t_{ON} is the turn-on delay of a practical high voltage rated semiconductor device such as [158] i.e. t_{ON}=1 μs. From (4.1), this indicates f_s=1 kHz as an adequate test switching frequency.

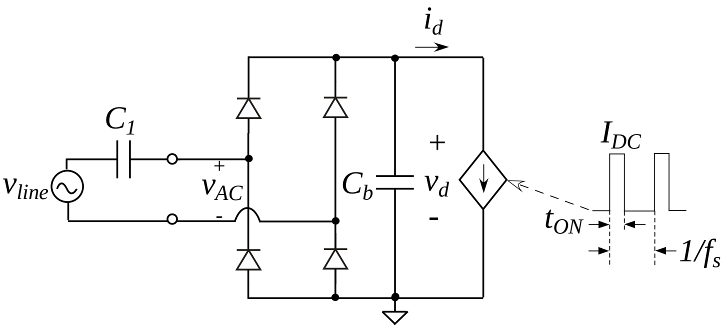


Figure 4.1: The principle of discontinuous conversion.

The results of this case study are shown in Figure 4.2. Every time a pulse of current is absorbed by the load, the DC bus voltage rapidly collapses, after reaching a peak of 13 kV (note that this is much more than the safe breakdown value of any present commercial semiconductor device), as shown in Figure 4.3. This drop occurs because the current demanded from the load surpasses the available input current from the EFEH supply, which is very low. Following the principle of conservation of energy, the DC bus voltage collapses in order to match this instantaneous requirement of power at constant current. Another way to understand this behaviour is to notice that since the rate of energy absorption is much higher than the incoming power flow from the AC side, the DC bus capacitor discharges, and the DC bus voltage collapses.

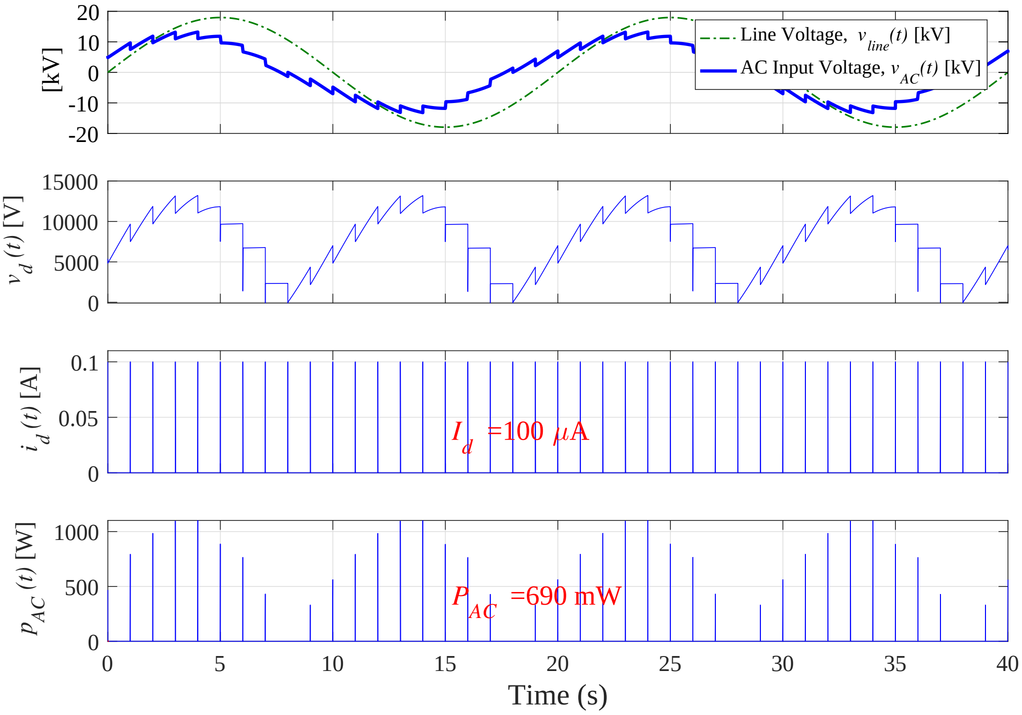


Figure 4.2: Simulation results for discontinuous regulation.

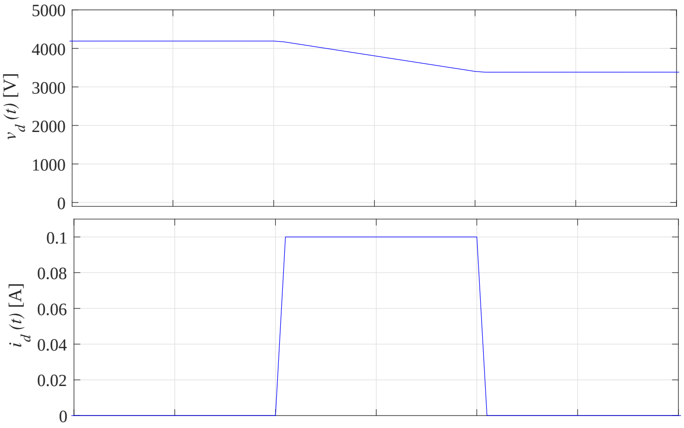


Figure 4.3: One current pulse.

This voltage drop only lasts for as long as the duration of the pulse i.e. t_{ON}. After this time interval, the load is removed and the DC bus voltage is able to reacharge slowly from the supply, until the next burst of curent. In contrast with linear DC voltage regulation, studied in Section 3.3.2, discontinuous regulation succeeds in maintaining a high peak DC bus voltage, which in turn assists the achievement of more power. Particularly in the present case study, more continuous power than predicted in Section 3.2 at a similar load current is achieved simply because the peak voltage in this case is more than the 970 V proposed in that section. The voltage used in this case study however is at an undesirable level, since it exceeds the safe breakdown value of commercial semiconductor devices.

Clearly, the application of the principle of discontinuous regulation requires the additional consideration of confinement of the bus voltage to safe values. In the next section, a complete conversion solution for EFEH that can implement in practice the principle of discontinuous conversion under the restraints analysed in this section is introduced.

4.2 Proposed Conversion Strategy

The findings that this thesis has presented so far suggest that an effective energy conversion strategy for EFEH integrates low-frequency rectification and discontinuous DC bus regulation, with the additional challenge of keeping the peak bus voltage below a maximum limit. However, the functional implementation of the power electronic converter has to consider further practical requirements, such as the isolation between the high voltage DC bus and the ELV end.

One topology that is able to realistically meet these insulation requirements is a flyback converter. Also, it has been recognised before that a flyback converter working in discontinuous conduction mode (DCM) can naturally accomplish the implementation of a load that looks like a loss-free resistor to the input supply [159], which is one of the requirements for maximum power transfer derived in Section 3.2 and also has the potential for the implementation of discontinuous DC voltage regulation, provided that an adequate voltage control method can be developed.

The use of these principles will now be applied to the implementation of a novel strategy for energy conversion using EFEH.

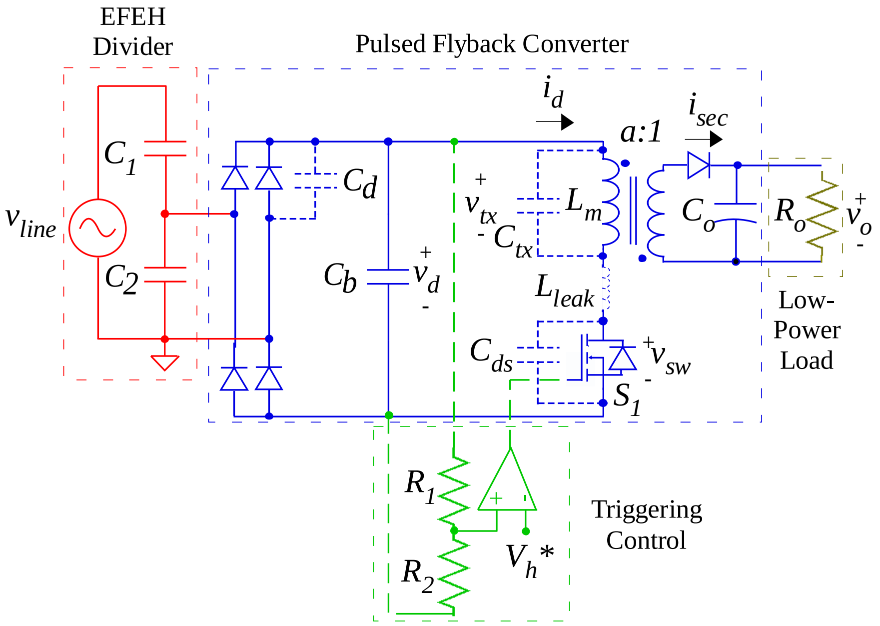


Figure 4.4: Proposed pulsed-mode flyback converter for EFEH systems.

4.2.1 Principle of Operation

A new energy conversion approach for a galvanically isolated EFEH system that uses the principles of the maximum possible power transfer is introduced in Figure 4.4. The approach uses a two stage conversion system comprising a simple diode rectifier to convert the 50 Hz AC voltage developed across C_2 into a relatively high DC voltage, followed by a second stage DC-to-DC converter to transform this voltage down to a useful ELV output.

However, the DC-to-DC converter also cannot switch continuously, since the maximum continuously available current that can be taken from the (nominally) 970V DC bus is at most 170 μA, given the theoretical maximum power transfer limit of 110 mW identified in Chapter 3. Once again, parasitic device capacitances will lead to phase leg transition times of several milliseconds for any form of continuously switched converter, which makes high frequency operation impossible.

To overcome this limitation, a single switch flyback converter operating in discrete pulse mode is used as the second stage energy conversion system. Each energy transfer pulse is initiated by activating the converter main switch S_1 when the DC bus voltage charges up to a defined trigger voltage V_h to transfer the energy stored in the bus capacitance into the coupled inductance magnetising circuit.

Since the rate of this energy transfer is much higher than the incoming power flow from the AC side, the DC bus capacitor discharges, and the DC bus voltage falls. When it reaches a lower threshold voltage V_l, switch S_1 is turned off, and the energy stored in the coupled inductance transfers to the secondary side rectifier and load

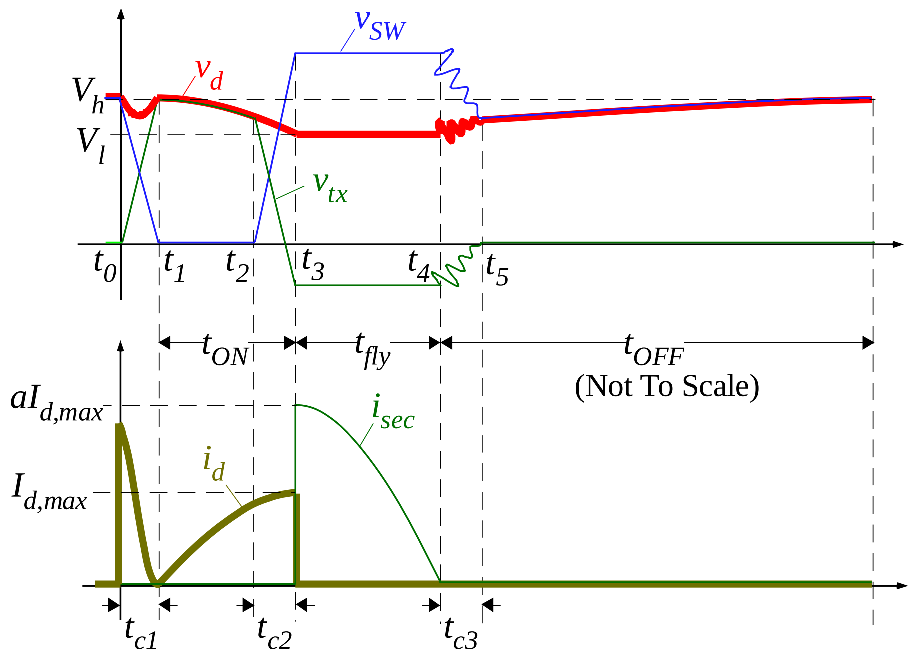


Figure 4.5: Switching intervals of the conversion system.

via a conventional flyback sequence. During this energy transfer burst, the diode bridge rectifier keeps conducting current to the DC bus, although it is only some hundreds of microamperes.

Once the energy transfer pulse cycle is complete, the HV DC bus voltage slowly recharges from the incoming AC supply until it again reaches the trigger voltage level, and another pulsed energy transfer cycle is initiated. Multiple pulse cycles occur over each half AC fundamental cycle, with the exact number depending on the AC input voltage magnitude and the various parasitic capacitances shown in Figure 4.4.

Figure 4.5 shows the switching sequence of one energy transfer pulse cycle which has a number of stages, described next. The cycle starts when switch S_1 is turned on at time t_0. This causes an initial surge of bus current during the period t_{c1} as the coupled inductor primary winding voltage v_{tx} increases to the DC bus voltage v_d by charging up the parasitic capacitance C_{tx} of this winding. Note that this initial current surge causes some energy loss from the main bus DC capacitance since it does not transfer energy into the magnetic circuit. This loss mechanism will be discussed in Section 4.3.

Once the primary winding voltage has established, the current through this winding increases during the period t_{ON}, transferring energy from the DC bus capacitance to the flyback transformer magnetizing inductance L_m. This causes the DC bus voltage to decay to the lower threshold V_l at time t_2, at which point the gate of switch S_1 is turned off. The transformer current continues to rise during the turn off period t_{c2} until the primary winding voltage v_{tx} reaches zero, just before t_3.

At time t_3, the voltage across the coupled inductor has reversed, the voltage across the secondary winding has reached the LV DC output voltage, and the output rectifier diode turns on. This provides a discharge path to the output filter capacitor C_o, which transfers the energy stored in the magnetizing inductance to this capacitor. The primary current also ceases at t_3 as the secondary discharge current takes over.

The secondary current continues for the period t_{fly} until all the stored magnetic energy has been transferred to the output filter capacitor, and the energy pulse cycle is complete. The HV DC bus then slowly recharges from the input AC current over the period t_{OFF} until it again reaches V_h and another energy transfer pulse can be initiated.

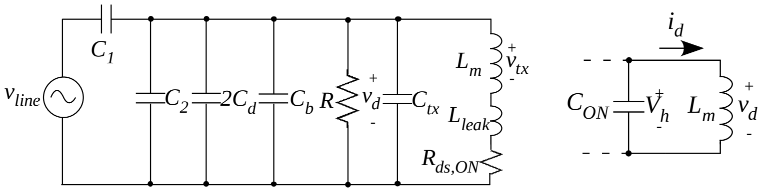
4.3 Theoretical Analysis of the System

4.3.1 Estimation of Energy Transfer

Conventionally for a flyback converter, the rise in the primary winding current during t_{ON} is approximated as a linear ramp. However for this application the significant change in v_d caused by the energy transfer process makes this approximation inadequate. Instead, during the switching interval t_{ON}, as soon as the bus voltage reaches the higher trigger voltage V_h, the switch S_1 is turned-on and becomes a low resistance path between its drain and source terminals $R_{ds,ON}$. Hence, the circuit in Figure 4.6a is formed, where the parasitic capacitances in Figure 4.4 are considered, including the measurement resistances (represented by $R = R_1 + R_2$).

The AC circuit analysis indicates that the contribution of the AC source during the considered t_{ON}, and the values of $R_{ds,ON}$ and L_{leak} are negligible. Therefore, as the switch Drain-Source voltage falls from V_h to zero, the DC bus voltage v_d is impressed across the primary winding of the flyback transformer L_m and the energy is transferred according to the equivalent system in Figure 4.6b to the flyback transformer, from the total consolidated capacitance of the DC bus given by

$$C_{ON} = C_1 + C_2 + 2C_d + C_b + C_{tx} \tag{4.3}$$



(a) Complete circuit **(b)** Equivalent circuit

Figure 4.6: Circuit during energy transfer interval t_{ON}.

Neglecting momentarily the measurement resistances represented by R, the change of bus voltage and primary winding current can be determined as the response of the approximate LC circuit in Figure 4.6b, by:

$$v_d(t) \approx V_h \cos(t/\sqrt{L_m C_{ON}}) \approx v_{tx}(t) \tag{4.4a}$$

$$i_d(t) \approx V_h \sqrt{C_{ON}/L_m} \sin(t/\sqrt{L_m C_{ON}}), t_1 < t < t_3 \tag{4.4b}$$

During each energy transfer pulse, the energy transferred to the magnetising inductance is given by

$$E_d = \int_0^{t_{ON}} v_d(t) i_d(t) dt \tag{4.5}$$

Substituting the values from (4.4) this integral solves to:

$$E_d \approx \frac{1}{2} {V_h}^2 C_{ON} \sin^2(t_{ON}/\sqrt{L_m C_{ON}}) \tag{4.6}$$

Expression (4.6) identifies the energy extracted from the DC bus consolidated capacitance for one energy transfer pulse at the end of each energy transfer pulse, when the DC bus voltage has decayed to the value V_l

During interval $t_f ly$, the energy stored in the magnetising inductance is transferred to the output capacitor C_o via conventional flyback operation. For the moment, it is considered that this process is lossless. The losses will be considered in Section 4.3.2.

At the end of the flyback interval, the approximate equivalent circuit of the system (again neglecting momentarily the effect of the measurement resistances R) is depicted in Figure 4.7. Essentially the DC bus circuit reverts to an ideal capacitor divider fed from the rectified incoming AC line voltage, comprising C_1 and the total consolidated capacitance C_{OFF} of the DC bus, which is given by

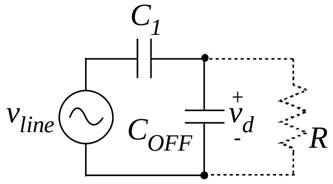


Figure 4.7: Equivalent circuit during recharge interval t_{OFF}.

$$C_{OFF} = C_2 + 2C_d + C_b + C_{ds} \tag{4.7}$$

The voltage across C_{OFF} is readily identified as a sinusoidally increasing voltage with an initial voltage of V_l at time t_4, i.e.

$$v_d(t) = V_{OFF,peak} \sin(\omega_o t) + D, t_4 < t \tag{4.8}$$

where:

$$V_{OFF,peak} = V_{line,peak} \frac{C_1}{C_1 + C_{OFF}} \tag{4.9}$$

and:

$$D = V_l - V_{OFF,peak} \sin(\omega_o t_4) = V_l - V_{OFF,peak} \sin(\varphi) \tag{4.10}$$

The variable φ is the phase angle of the AC input voltage (with an angular frequency ω_o) at which each DC bus recharging cycle starts.

Equation (4.8) can be linearized over each t_{OFF} period as:

$$v_d(t) \approx V_l + \frac{dv_d}{dt}[t - t_4] = V_l + \omega_o V_{OFF,peak} \cos(\varphi)[t - t_4], t_4 < t < (t_4 + t_{OFF}) \tag{4.11}$$

Note that (4.11) is always linearly increasing for each recharge interval over the range $-\pi/2 < \varphi < \pi/2$, which is the period where one diode pair of the input rectifier is conducting (since the input current through C_1 leads the AC input voltage by $\pi/2$). As the cycle of discharge and recharge repeats symmetrically for each AC half cycle, the recharge sequences now only need to be analysed over this half cycle period.

The total energy harvested in one AC source half cycle is nE_d, where n is the number of pulses which occur during that period, and depends on the value of t_{OFF}. For each pulse t_{OFF} can be solved from (4.11) by setting $v_d(t_{OFF}) = V_h$. However, it is also clear that t_{OFF} will not be constant but rather a function of φ, varying as the magnitude of the incoming AC voltage changes.

An average value for t_{OFF} can be found by recognising that

$$v_d(t_4 + \overline{t_{OFF}}) = V_h = V_l + \omega_o V_{OFF,peak}\overline{\cos(\varphi)} \times \overline{t_{OFF}} \tag{4.12}$$

over the period $-\pi/2 < \varphi < \pi/2$.

Hence, since $\overline{\cos(\varphi)} = \frac{1}{\pi}\int_{-\pi/2}^{\pi/2}\cos(\varphi)d\varphi = \frac{2}{\pi}$, then (4.12) becomes

$$v_d(t_4 + \overline{t_{OFF}}) = V_h = V_l + \omega_o V_{OFF,peak}\frac{2}{\pi}\overline{t_{OFF}} \tag{4.13}$$

which gives a solution for the average DC bus recharge time interval t_{OFF}:

$$\overline{t_{OFF}} = \frac{\pi}{2}\frac{V_h - V_l}{\omega_o V_{OFF,peak}} \tag{4.14}$$

Finally, since $t_{OFF} >> t_{fly} > t_{ON}$ the number of recharge cycles that occur during each half-cycle can be approximately estimated as:

$$n \approx \frac{T_o}{\overline{t_{OFF}}} = \frac{\pi}{\omega_o}\frac{2\omega_o V_{OFF,peak}}{\pi(V_h - V_l)} = 2\frac{C_1}{C_1 + C_{OFF}}\frac{V_{line,peak}}{(V_h - V_l)} \tag{4.15}$$

where $T_o = 1/f_o$ is the period of the input AC line voltage. The total energy harvested per half cycle is given by nE_d, which gives a continuously scavenged power of:

$$P = 2f_o nE_d = (\omega_o/\pi)nE_d \tag{4.16}$$

Expression (4.16) defines the relationship between the high voltage threshold V_h and the DC bus capacitance C_b, for maximum power extraction, as shown in Figure 4.8. For the experimental system described later in this chapter, the predicted energy in one pulse from this analysis is E_d =22.7 μJ, the theoretical number of pulses is n=27, and thus the maximum harvested power is about 61 mW. However, this estimation does not take into account the quite significant converter losses, which now have to be considered.

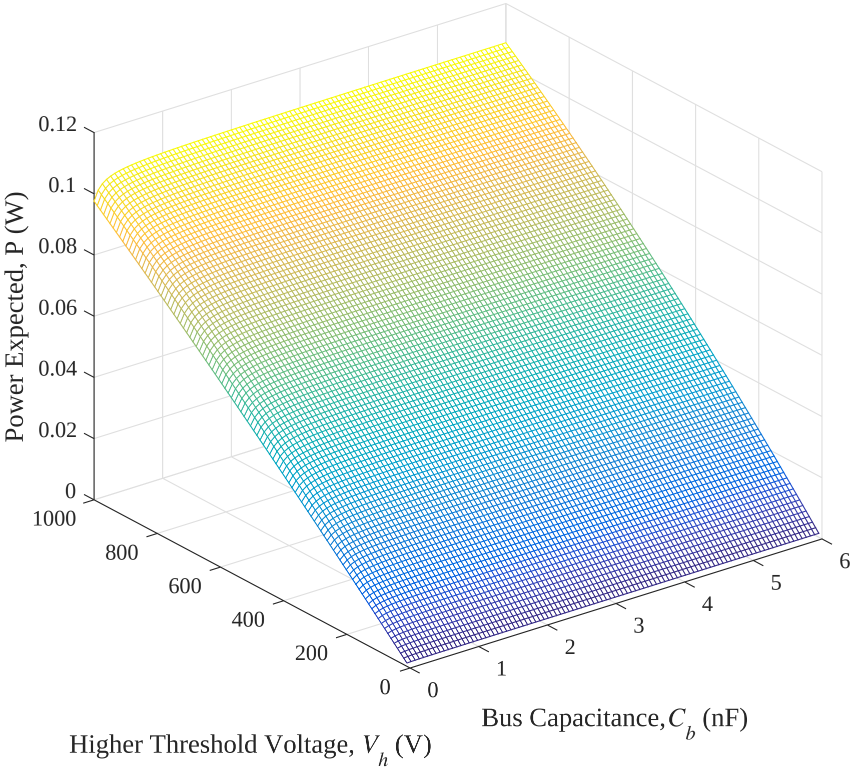


Figure 4.8: Available power versus threshold voltage and bus capacitance.

4.3.2 Estimation of Converter Losses

Unlike a more conventional converter operation, the losses of the burst mode conversion system dissipate a substantial fraction of the theoretically available energy, and significantly reduce the available output power as a consequence. The analysis of the conversion circuit in the present chapter assumes a lossless gate-driver capable of driving S_1 rapidly into conduction, so it does take into account additional losses in the Drain-Source channel resistance. This assumption is relaxed in Chapter 5. Aside from that, there are three major loss contributors in this system: switching losses, coupled inductor magnetic losses and parasitic resistance losses. Each loss type will now be considered.

Switching Losses

As shown in Figure 4.5, when S_1 turns on, there is an initial surge of current as the switch charges the primary transformer winding parasitic capacitance C_{tx} during t_{c1}. Figure 4.9 shows a simplified representation of this situation, where two loss components can be identified.

The first loss mechanism can be identified as the energy dissipated in the switch as a consequence of conducting the current required to charge the winding capacitance from the effective equivalent bus capacitance during t_{c1}, C_{bus} which is given by

$$C_{bus} = C_1 + C_2 + 2C_d + C_b \tag{4.17}$$

This loss can be derived as

$$E_{loss,C_{tx}} \approx \frac{1}{2}(C_{bus}||C_{tx})V_h^2 \tag{4.18}$$

and has a value of 6 μJ for the experimental system described later in this chapter.

Secondly, there is some energy loss caused by the discharge of the energy stored in the switching device drain-source capacitance C_{ds}, $E_{loss,sw}$, at the point of turn-on. This energy can be determined from the data sheet for the C2M1000170D SiC FET [158] used in this work, which specifies the energy stored in C_{ds} for a given Drain-Source voltage. In this case, the energy stored in this capacitor that is lost at the point of turn-on is about 2 μJ per pulse, for a Drain-Source voltage of 545V (more detail in Section 4.5).

On the other hand, during the flyback interval t_{fly} of Figure 4.5, some energy is lost through the secondary diode which is forward-biased with a voltage $V_{Dsec,fw}$, as shown in the equivalent circuit of Figure 4.10. This energy can be approximated as

$$E_{loss,Dsec} = \int_{t_{fly}} V_{Dsec,fw} i_{sec}(t)dt \tag{4.19}$$

The evaluation of this quantity depends on an estimation of the secondary current $i_{sec}(t)$ and the duration of the flyback interval t_{fly}. From Figure 4.5, the secondary winding discharge current i_{sec} decays as all the energy previously stored in the magnetising inductance L_m during t_{ON} is transferred to the output capacitor at the end of t_{fly} in the form of the charge

$$q_{fly}(t) = \int_0^{t_{fly}} i_{sec}(t)dt = C_o\Delta V_o \approx \frac{t_{fly}Isec(max)}{2} \tag{4.20}$$

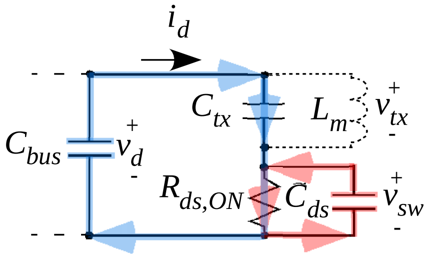


Figure 4.9: Equivalent circuit during interval t_{c1}.

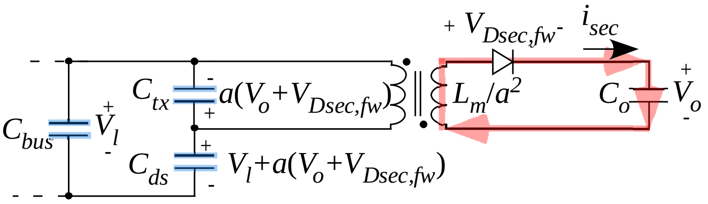


Figure 4.10: Equivalent circuit during interval t_{fly}.

which is derived using the conventional flyback converter assumption of a triangular approximation for the shape of $i_{sec}(t)$.

Since $i_{sec}(t) = ai_d(t)$ due to mmf balance in the flyback transformer, then $I_{sec}(max)$ can be determined from (4.4) as

$$I_{sec}(max) = aI_d(max) = aV_h\sqrt{C_{ON}/L_m}\,\sin(t_{ON}/\sqrt{L_mC_{ON}}) \tag{4.21}$$

where a is the turns ratio of the transformer.

Without considering other losses, the energy stored in the magnetising inductance during t_{ON} is equal to the energy transferred to the output capacitor i.e.

$$E_o = V_oC_o\Delta V_o \approx E_d \tag{4.22}$$

Combining (4.6), (4.20) and (4.21) then gives an estimate of t_{fly} as

$$t_{fly} \approx \frac{V_d\sqrt{L_mC_{ON}}}{aV_o}\sin(t_{ON}/\sqrt{L_mC_{ON}}) \tag{4.23}$$

Now, the expression in (4.19) can be evaluated considering that the waveform of the secondary current $i_{sec}(t)$ can be approximated as a triangle of height $I_{sec}(max)$ and base t_{fly}, as per the conventional theory for flyback converters [157]. Hence, using the approximations (4.21) and (4.23) for $I_{sec}(max)$ and t_{fly}, respectively, the value of this loss solves to

$$E_{loss,Dsec} \approx \frac{1}{2}\frac{V_{Dsec,fw}V_h^2}{V_o}C_{ON}\sin^2\left(\frac{t_{ON}}{\sqrt{L_mC_{ON}}}\right) \tag{4.24}$$

This loss is dependent on the forward voltage drop of the secondary diode and the maximum DC bus voltage and, for the experimental system that will be presented in Section 4.5, is 2.7 μJ per pulse.

Magnetic Losses

Magnetic hysteresis is the lead mechanism for the losses in the core of the flyback trasnformer in this application, associated with the magnetic flux density swing ΔB, which is the maximum gradient of the instantaneous magnetic flux density $B(t)$. This variable can be defined using Faraday's law of induction as a piecewise expression of the electromotive (emf) developed across the primary of the transformer v_{tx}, with

$$B(t) = \left(\frac{1}{N_1 A_c}\right) \int_0^t v_{tx}(t)dt \tag{4.25}$$

where N_1 is the number of turns in the primary of the transformer and A_c is the effective core area.

From Figure 4.5, the interval that contributes predominantly to the gradient of $B(t)$ is t_{ON}. Hence the integral in (4.25) can be solved by defining $v_{tx}(t)$ for t_{ON}. According to the approximation in Figure 4.6b during t_{ON}, v_{tx} is approximately equal to the decaying bus voltage v_d, i.e.

$$v_{tx}(t) \approx V_h \cos\left(\frac{t}{\sqrt{L_m C_{ON}}}\right), t \in t_{ON} \tag{4.26}$$

Hence, applying (4.25), the approximate magnetic flux density during t_{ON} is given by

$$B(t) \approx \left(\frac{V_h}{N_1 A_c}\right) \sqrt{L_m C_{ON}} \sin\left(\frac{t}{\sqrt{L_m C_{ON}}}\right), t \in t_{ON} \tag{4.27}$$

and the maximum value it reaches i.e. the magnetic flux density swing is

$$\Delta B \approx \frac{\sqrt{L_m C_{ON}} V_h}{N_1 A_c} \sin\left(\frac{t_{ON}}{\sqrt{L_m C_{ON}}}\right) \tag{4.28}$$

The extensive literature in the topic of core losses identifies the improved generalised Steinmetz equation (iGSE) [160] as a good method to estimate the hysteresis losses for non-sinusoidal waveforms. It defines the energy per switching cycle, which in this case is approximately $\overline{t_{OFF}}$ according to the analysis in Section 4.3. Using the iGSE, the energy loss in one switching cycle is thus approximated as

$$E_{loss,hys} \approx Vol\overline{t_{OFF}} \frac{k_i |\Delta B|^{\beta-\alpha}}{{N_1}^{\alpha} {A_c}^{\alpha}} \langle |v_{tx}(t)|^{\alpha} \rangle \tag{4.29}$$

where

$$k_i = \frac{K_c}{2^{\beta-1}\pi^{\alpha-1}\left(1.1044 + \frac{6.8244}{\alpha+1.354}\right)} \tag{4.30}$$

Vol is the effective volume of the core, and $[K_c, \alpha, \beta]$ are coefficients associated with the core model obtained from curve-fitting, respectively: core loss constant, frequency exponent and flux density exponent. Appropriate coefficients for frequencies more than 500 kHz and the experimental core presented later in Section 4.4 are K_c=0.0032, α=1.46 and β=2.75 [161].

In general, (4.29) indicates that larger core sizes as well as higher bus voltage triggering levels increase the losses in the core of the trasnformer. The estimation of the core loss for the example system in this study, in each pulse, is of 50 nJ.

Taken together, the total losses per energy transfer pulse add up to $6.0 + 4.0 + 2.7 + 0.05 = 12.8\mu$J , which from the ideal switching prediction, leaves ˜10 μJ of energy per pulse available for energy transfer. This translates to a transferred power of nearly 27 mW for an ideal pulse number of n=27.

Parasitic Resistor Losses

The bus voltage sense resistors R_1 and R_2 shown in Figure 4.4 also contribute a significant standing energy loss for the converter system. While these resistors have been made as high as possible for the experimental system, they still constitute a $R = R_1 + R_2 = 50M\Omega$ load across the DC bus, which in this case study creates a standing load of almost 6 mW. In addition, this standing load will also constrain the rate of recharge of the DC bus voltage during t_{OFF}, which will reduce the number of energy transfer pulses for each half cycle.

The current drawn by the sense resistors is $545V/50M\Omega = 11\mu A$ which is about 10% of the anticipated DC bus charging current of 110 μA at this bus voltage. Hence the pulse rate could be expected to reduce by about 10%, down to n=24 pulses per half cycle. This reduces the transferred energy to 23.9 mW according to (4.15) and (4.16). Subtracting the 6 mW standing loss of the sense resistors from this transferred energy leads to a predicted continuous output power of about 18 mW available from the conversion system of the EFEH energy scavenging system.

These loss calculations suggest that over 70% of the theoretical transferred energy will be dissipated in losses, which is very high. Since these losses are substantially dependant on the average DC bus voltage, this further suggests that the EFEH converter could be more efficiently operated at lower V_h and V_l threshold voltages.

This will reduce the transferred energy according to (4.6), (4.15) and (4.16) but will also reduce the losses (particularly the device drain-source stored energy $E_{loss,sw}$).

This section has analytically derived an expectation of the energy transferred with the proposed conversion system. However, theoretically predicting the energy transfer and the optimum operating conditions for its attainment is extremely difficult, given the substantial level of losses associated with the pulsed switching converter, and the difficulty in accurately determining these losses because of the influence of various practical parasitic effects. Hence, the figures resulting from the analyses have to be regarded as estimations. Complementary experimental investigations are presented over the next sections.

4.4 Verification of the Theory

A theoretical estimation of the power transferred by the proposed converter system was derived in the previous section. It was found that there is a relationship between the harvested power and two degrees of freedom: V_h and C_b, according to (4.6), (4.15) and (4.16). The theoretical, optimal values of these parameters for maximum energy could be inferred from Figure 4.8. However, not only is there a substantial level of loss associated with the pulsed switching converter but also these losses are difficult to quantify analytically because of the influence caused by the highly non-linear parasitic impedances of the switching devices.

Therefore, the actual power harvested by the proposed conversion system, as well as the optimal parameters V_h and C_b for maximum power transfer need to be verified experimentally. Firstly, the EFEH conversion system has been investigated using a detailed PSIM computer simulation model in order to verify the correctness of the analytical equations derived in Section 4.3. Then, a low voltage (LV) proof-of-concept experimental investigation was developed to verify the complete range of switching waveforms in the conversion system. Finally, the efficacy of the proposed conversion system was validated through full rating medium voltage (MV) experiments. The results of these experiments are presented in this section.

4.4.1 Computer Simulation Model

The detailed PSIM model includes the semiconductor junction impedances, the transformer inter-winding capacitance C_{tx} and other essential parameters of the MV EFEH system under study, as listed in Table 4.1. The values of the parameters in the table were used in the numerical computations of the equations in Section 4.3.

Table 4.1: EFEH circuit experimental parameters.

Parameter	**Value**	**Description**
ω_o	$2\pi 50$ rad/s	Input AC supply angular frequency
$V_{line,RMS}$	4.5 kV	Peak AC line input voltage
C_1	100 pF	EFEH High voltage capacitor
C_2	17 pF	EFEH Low voltage capacitor
C_d	2 pF	Diode BYG10Y parasitic capacitance
C_b	1 nF	DC bus capacitor
C_{ds}	13 pF	MOSFET C2M1000170D output capacitance
C_{tx}	28 pF	Flyback transformer inter-winding capacitance
L_m	561 μH	Flyback transformer magnetising inductance
L_{leak}	1 nH	Flyback transformer leakage inductance
a	46/23	Flyback transformer turns ratio N_1/N_2
A_c	125 mm^2	Effective area core ETD34, grade 3C90
Vol	11500 mm^3	Effective volume core ETD34, grade 3C90
R	50.22 MΩ	Combined measurement resistance $R_1 + R_2$
V_h	545 V	Maximum threshold voltage
t_{ON}	300 ns	Min. response time of fast comparator ADCMP609
C_o	47.1 μF	Load capacitor
R_o	10 kΩ	Low-power load
$V_{Dsec,fw}$	1.53 V	Secondary diode forward voltage drop

The proof-of-concept experimental prototype on which the simulation model of Table 4.1 is based, is shown in Figure 4.11. The AC supply is based on the medium-voltage system described later in Section 4.5. The threshold voltage triggering control device is a low-power consumption ADCMP609 fast comparator [162], which has a short time response of around 300 ns. This is the time that was used for t_{ON} in the theoretical development presented in Section 4.3. The DC bus voltage measured input for the comparator derives from the R_1/R_2, 50 MΩ resistive divider in Figure 4.4.

The input diode bridge rectifier uses 1600V BYG10Y [163] diodes while the flyback conversion stage switch is a 1700V SiC C2M100170D MOSFET [158]. SiC semiconductors were the devices that presently present the highest breakover voltage while maintaining low leakage currents. The rectifier in the secondary of the flyback transformer is an ultrafast diode rated to block a peak of 800V reverse voltage (MURS480ET3G [163]). These semiconductor devices were selected as the forefront technologies for such a high-voltage switching converter.

The flyback transformer was designed with a small magnetising inductance to increase the transferred energy per pulse. With the same aim, the number of turns N_1 and N_2 were kept as small as possible. An ETD34 grade 3C90 [164] core was used, which is appropriate for such low power applications but still of sufficient size to avoid high voltage arcing. The turns-ratio $a = N_1/N_2$ was selected to keep the

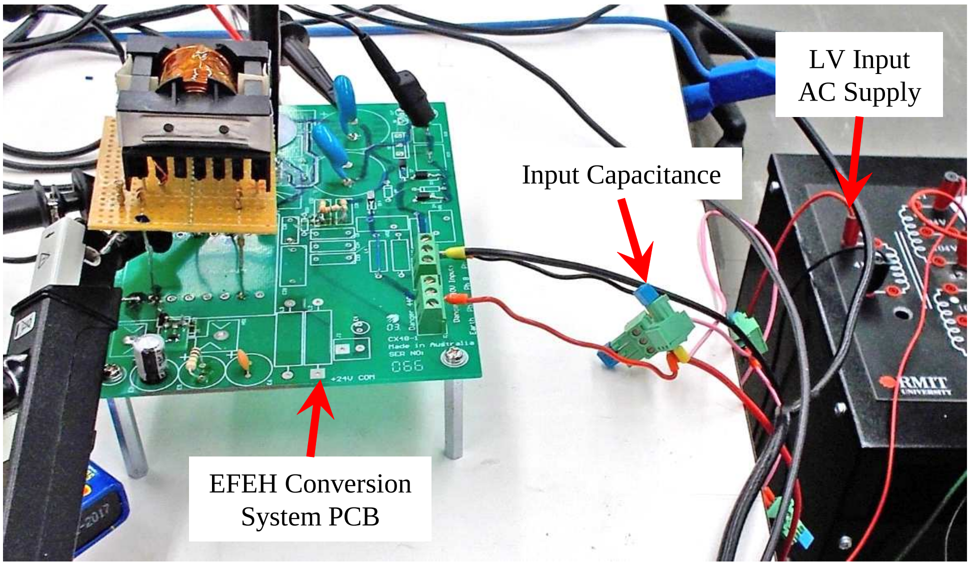


Figure 4.11: Low-voltage experiment.

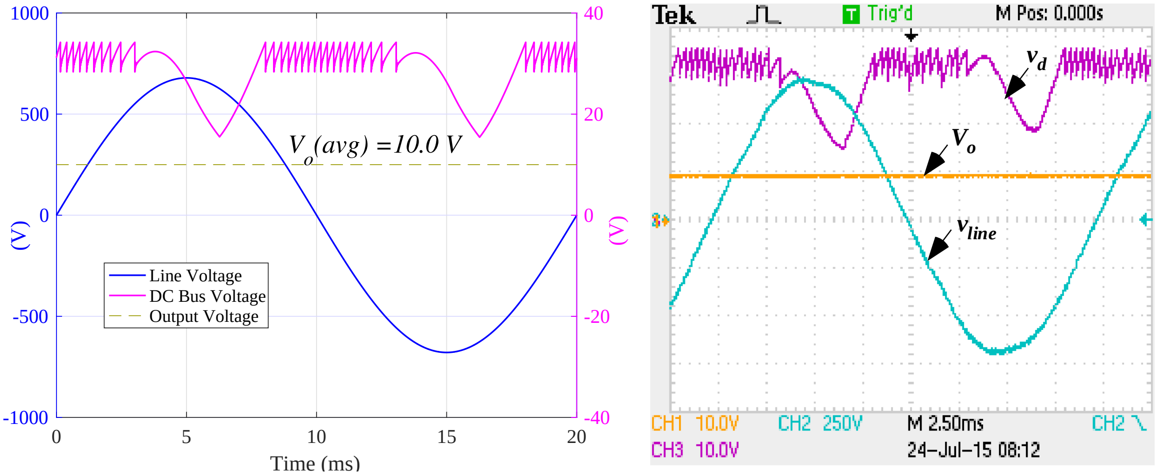
AC magnetic flux density swing represented in (4.28) well below 200 mT and hence minimize core losses. A sandwich winding construction was used to improve the MV insulation level between the primary and secondary windings.

The full PSIM simulation model based on the prototype is described in Chapter 6. The results obtained using this model will be compared against the experimental results, for both LV and MV real-life experiments.

4.4.2 Low Voltage Experimental Results

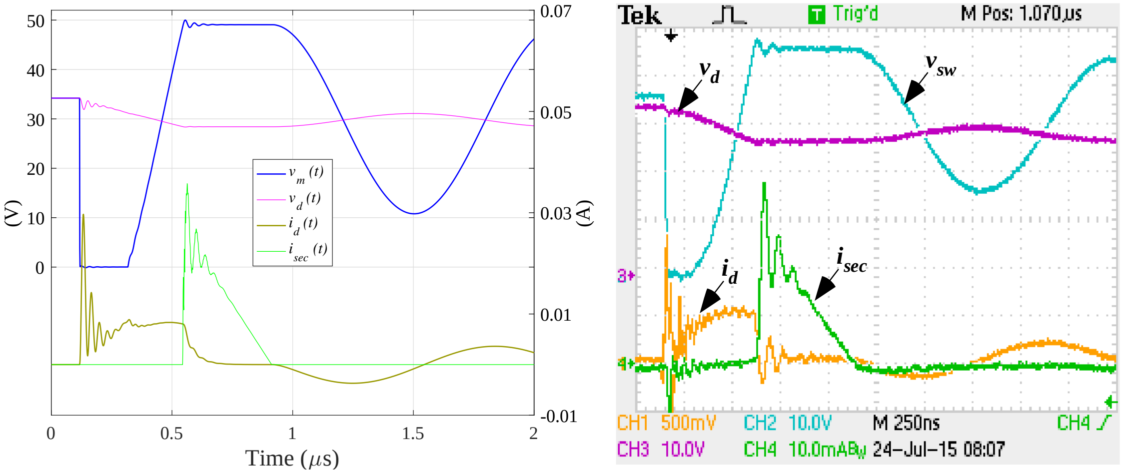
The proof-of-concept experimental EFEH system was tested with a low AC input of 415V(RMS) to validate the two stage EFEH concept. The experimental setup is shown in Figure 4.11. This LV experiment was used to get around the limitations that the MV experimental setup has in relation to the measurement of the different switching waveforms in the system. This issue was noticed before in Section 3.1.4, i.e. the conversion system is extremely sensitive to the influence of any parasitic impedance.

For instance, in this experiment the TEK P5120 [165] voltage probe used to measure voltage waveforms has an input impedance 5MΩ/11pF, which is comparable with the bus impedance of around 36 pF without any added C_b and can significantly influence some of the measured waveforms. This problem is even more pronounced in a MV setup. Therefore, the observation of switching waveforms is easier in a LV setup. A more detailed description of the low-voltage experimental setup built for this experiment is presented in Chapter 7.



(a) Simulation **(b)** Experimental

Figure 4.12: Low-voltage experimental verification - AC input cyle.



(a) Simulation **(b)** Experimental

Figure 4.13: Low-voltage experimental verification - Single pulse.

Figure 4.12 and Figure 4.13 show simulation and matching experimental results for the LV system: for a complete AC input cycle and for a single switching pulse, respectively. The figures show the collapse of the DC bus voltage as i_d charges the magnetising inductance, and the slow turn-off of the switch during the period t_{c2}. The flyback action of energy delivery can be seen in the secondary current i_{sec}, up to the end of the t_{fly}, interval.

The shape of all the experimental waveforms match the theoretical expectations in Figure 4.5 very well. Approximately eighteen energy transfer pulses occur in each half fundamental cycle, creating an output load voltage of 10V across a load resistor of 1 MΩ. This translates to nearly 100 μW of continuously harvested power, with a measured converter input power of 196 μW. Hence the conversion efficiency at low-voltage is just over 50%.

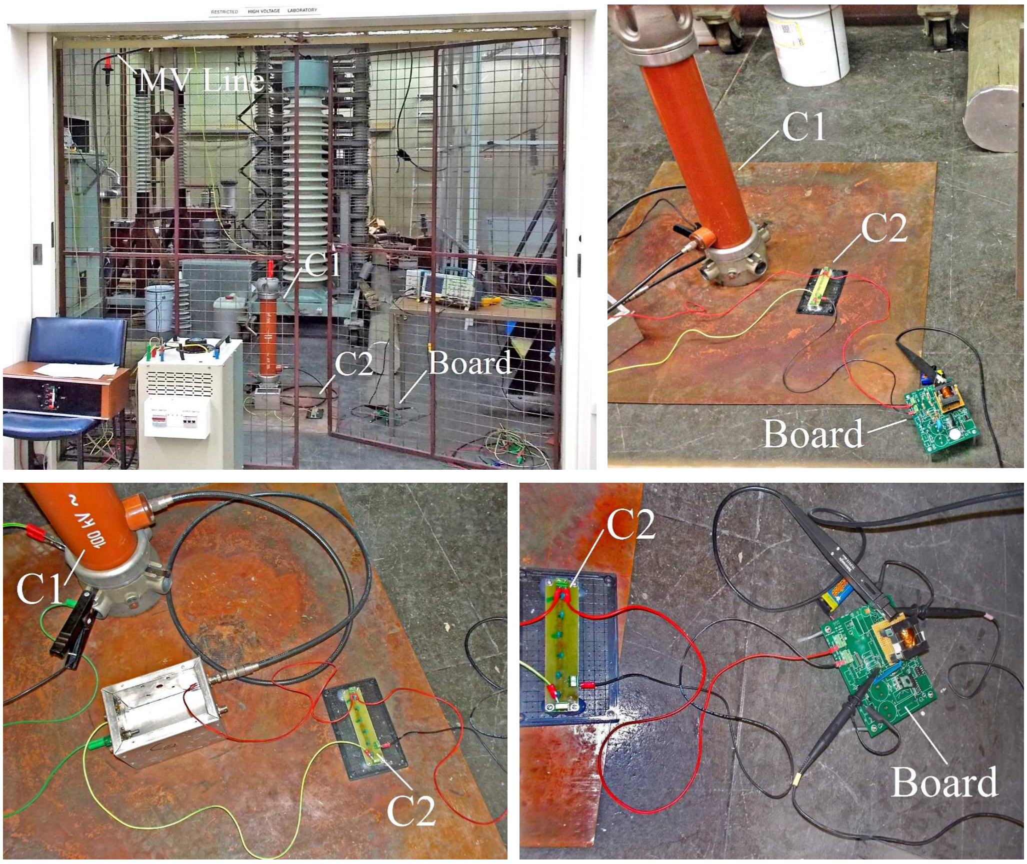


Figure 4.14: Medium-voltage experimental setup.

4.5 Medium Voltage Experimental Validation

The experimental prototype presented in the previous section was tested under full scale operating conditions with a MV AC supply to confirm the operation of the energy harvester under realistic operating conditions. However, the 12.7kV line voltage was represented using the 4.5 kV(RMS) AC supply available in the laboratory, feeding through a 100 pF HV coupling capacitor. This generated a maximum input current of 150 μA, which is the same order of magnitude as for the full line voltage system discussed in Section 3.2. Hence the proposed converter was working essentially at the designed maximum input AC voltage and current levels (approximately 1kV and about 170 μA, respectively), so the study results matched what could be expected for a full field conditions. The parameters of the experimental setup are summarised in Table 4.1, without losing any generality in the study. A complete description of this experimental arrangement is presented in Chapter 7. The MV experimental setup studied in this section is shown in Figure 4.14.

As was anticipated in the analysis of Section 4.3, the system proved to be extremely sensitive to the different capacitances around the setup i.e. the identification of the precise values of V_h and C_b for maximum power had to be tested in situ.

Table 4.2: Results from the MV investigations (powers in miliwatts).

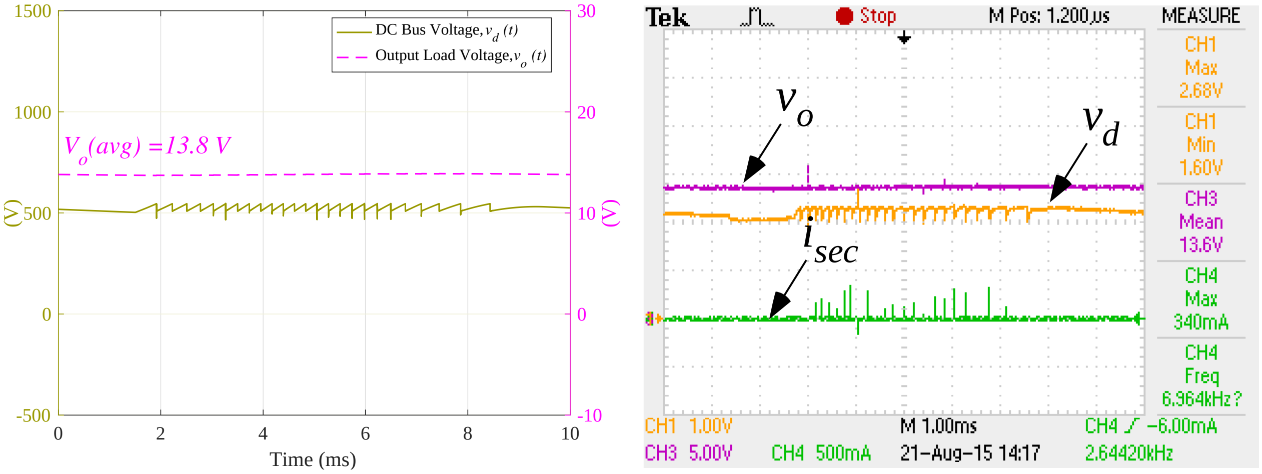
V_h \ C_b	**0**	**500 pF**	**1 nF**	**10 nF**	**100 nF**
296 V	8.5	9	9.4	8.3	1.6
545 V	12.3	14	17.1	10.6	7.6
880 V	16.2	10.7	10	4.2	-
1200 V	11.7	4.9	-	-	-

The power values obtained for different tested values of V_h and C_b are presented in Table 4.2. The cases with no result mean that no pulses were observed in half-cycle period for that condition. The presented results confirm the notion that a higher triggering voltage V_h increases the available power but also the losses in the system. This means that for a given added bus capacitance C_b there is a specific triggering voltage V_h for which the power is maximised, above which the power decreases due to increased losses. In this experience, maximum power transfer was achieved for a V_h=545 V, with a DC bus capacitor C_b=1 nF.

For this condition, Figure 4.15 and Figure 4.16 show simulation and matching experimental results for the MV system: for a complete AC input cycle and for a single switching pulse, respectively. The results show up to 24 energy transfer pulses, which matches the final theoretical prediction of Section 4.3.2. The DC bus voltage (measured with a resistive divider ratio of 223/1) rises to the specified V_h of 545V and discharges back to about 500V for each t_{ON} interval. The measurement of the secondary current i_{sec}, confirms correct flyback operation, in accordance with the theory and simulation study.

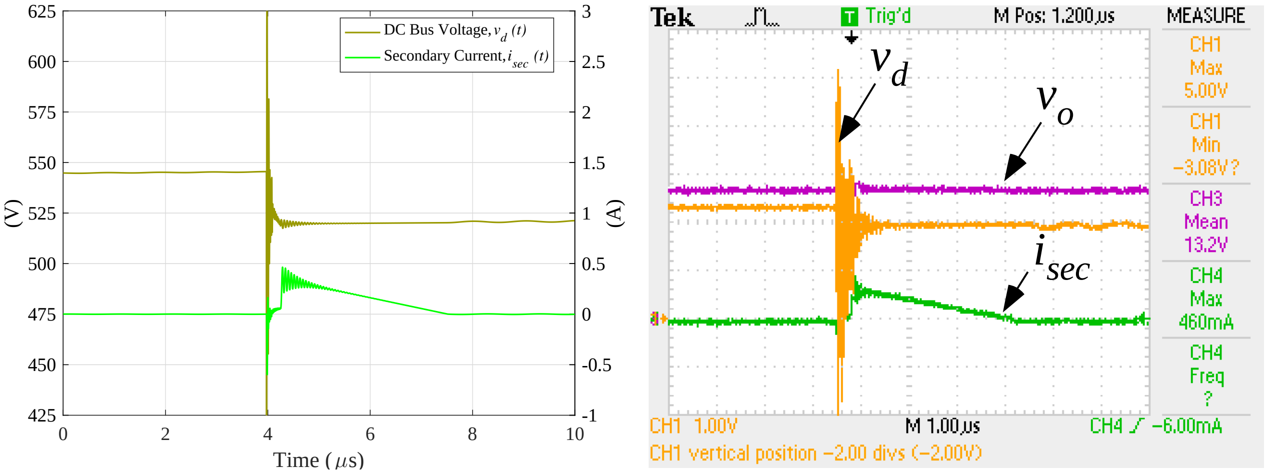
Other voltage waveforms such as the switch voltage v_{sw} and the input current i_d are not displayed because the inclusion of the additional measurement probes in the circuit disturbs the operation of the circuit due to loading effects, as was discussed in Section 4.4.2. Also, a second order ring can be seen imposed on the waveforms. This effect is caused by the coupling of the measurement equipment to earth. This hypothesis was validated by reflecting such a capacitive coupling to earth in the simulation model, to make it exhibit this response too. Again, these effects reflect the sensitivity of the system at MV to the addition of any further impedance.

The final result is an output load voltage of more than 13V across the low-power load resistor of 10 kΩ to harvest a total power of 17.1 mW. This figure closely matches the predicted expectations for the system in Section 4.3, confirming a low efficiency of the conversion system of around 25%, which is inherent to the switching behaviour. Nonetheless, the level of continuous power attained with this conversion topology outperforms the state-of-the-art figure of 2 mW at 15 kV in [62], with



(a) Simulation **(b)** Experimental

Figure 4.15: Medium-voltage experimental verification - AC input cyle.



(a) Simulation **(b)** Experimental

Figure 4.16: Medium-voltage experimental verification - Single pulse.

the additional benefit of being viable for a non-contact EFEH system. Hence, the proposed conversion system has been validated in concept.

This section has presented the experimental validation of the novel conversion solution for EFEH introduced in this chapter. The conversion scheme uses a flyback converter working in pulsed energy transfer mode. The design limits the maximum DC bus voltage to adequate levels for the operation of the semiconductor devices.

This conversion strategy was implemented in practice using a low-power consumption fast comparator. The continuous power requirement of the device is of around 10 μW. In theory, this power quota can be met by the EFEH system, but the conditions to feed back the power supply to the gate-driver have not been addressed in these investigations. Hence the experimental prototype presented in this section used a battery to power the control circuitry. Clearly, there is an advantage in self-triggering the switching circuit to produce a completely self-powered EFEH conversion solution. This is the topic of the next chapter in this thesis.

4.6 Summary

This chapter has presented a novel energy conversion strategy for EFEH systems. The approach does not tap the input voltage but instead uses a single diode bridge rectifier to directly process a DC bus voltage of higher values than in previous strategies found in the literature. A subsequent DC-to-DC conversion stage composed of a flyback converter operating in a non-conventional pulsed energy transfer mode is able to deliver a suitable power supply for low-power electronic devices in charge of power line monitoring.

The proposed conversion scheme is able to tackle the challenging limitations that the extremely small values of EFEH input capacitor dividers present i.e. the impracticality of high-frequency continuous conversion due to high commutation times produced by the parasitics in the switching system. Detailed circuit analysis, computer simulations and experimental results are presented to confirm the viability and success of the idea. The concept was tested for the galvanically isolated, insulator-based EFEH capacitive divider system presented in Chapter 3. An extraction of 17.1 mW from a 12.7 kV power lines was demonstrated experimentally, which outperforms previous achieved levels of power using a non-contact EFEH strategy.

Compared to the total input power available from the EFEH divider (analysed in Chapter 3) the efficiency of the conversion system is about 25%. A theoretical analysis identified the origin of this low efficiency as the high switching and resistive losses that are inherent to the weakly coupled system and its added parasitic capacitances. Detailed experimental waveforms corroborated this hypothesis and explained successfully the energy transfer process.

The system has the main disadvantage of not having its control circuitry self-powered, as the gate driver of the main switch is powered by an auxiliary battery. This constraint means that there are additional losses associated with the gate-driver of the main switch, which is similar to the case of several previous studies in the literature. In order to address this issue, the concept of a power electronic converter with self-triggered switching operation is now introduced in the next chapter of this thesis.

Chapter 5

A SELF-TRIGGERED FLYBACK CONVERTER FOR EFEH

Chapter 4 has validated the principle of a flyback converter working with pulsed energy transfer as an effective energy conversion strategy for Electric Field Energy Harvesting. However, as in any conversion topology, the control circuitry that triggers the main switch requires its own auxiliary power supply. In an EFEH application the limited amount of power available from the main supply makes the accomplishment of this demand more challenging. In the literature, this problem is usually solved by the use of a battery, which is suboptimal.

This chapter now introduces a triggering control strategy for the flyback converter topology that is self-powered from the EFEH input supply. The operation of the overall self-triggered flyback converter is then explored. A complete analytical study of the structure is developed and the operation of the system is validated in a medium-voltage environment.

The investigation presented in this chapter identifies that more than 20 mW of continuous power can be extracted from a 12.7kV MV line using this design, with a very low input capacitive coupling to the line. The overall features of this system outperforms previous work presented in the literature.

5.1 Principle of Operation

Following the principles of Chapter 4, the converter presented in Figure 5.1 is composed of two main stages. The first section uses a simple diode rectifier to convert the 50 Hz AC input voltage developed across C_2 into a relatively high DC voltage. The second stage uses a pulsed-operation DC-DC flyback converter to transform

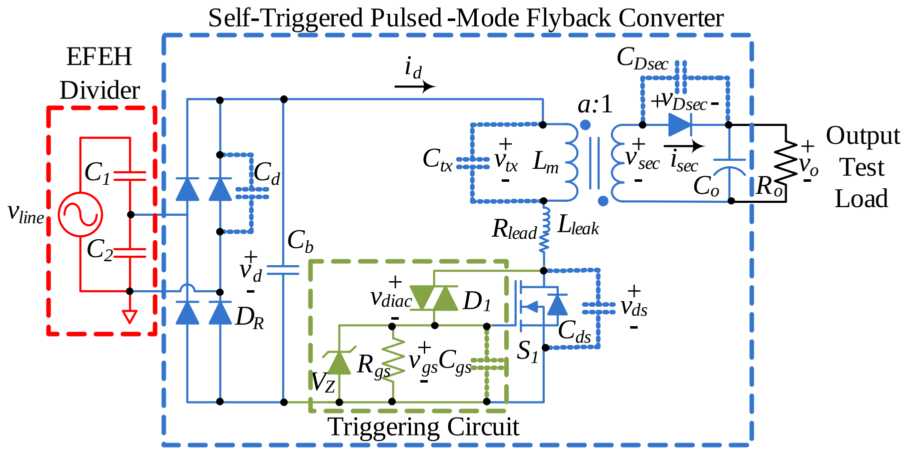


Figure 5.1: Self-triggered pulsed-mode flyback converter for EFEH systems.

this voltage down to a useful low voltage output for low-power electronic devices. A triggering circuit is now added to control the main switch S_1. The basic converter operation is then as follows.

Each energy transfer pulse is initiated by turning on the converter main switch S_1 when the DC bus voltage charges up to a defined trigger voltage V_h, to transfer the energy stored in the DC bus capacitance into the coupled inductance of the flyback converter. Since the rate of this energy transfer is much higher than the incoming power flow from the AC side, the DC bus capacitor discharges, and the DC bus voltage collapses.

When the DC bus voltage reaches a sufficiently low value, switch S_1 turns off and the energy stored in the coupled inductance transfers to the secondary side rectifier and load via a conventional flyback sequence. Once the energy transfer cycle is complete, the HV DC bus voltage slowly recharges from the incoming AC supply until it again reaches the trigger voltage level, and another energy transfer pulse is initiated. More than one energy pulse may occur over each half AC fundamental cycle, depending on the AC input voltage magnitude and the various parasitic capacitances shown in Figure 5.1.

A primary target for this system is to directly trigger S_1 using energy taken from the DC bus, without requiring any auxiliary supply. This is achieved by connecting DIAC D_1 across the drain-gate of the main MOSFET S_1. When the DC bus voltage charges up to the DIAC breakover voltage V_{bo}, it triggers and becomes a low resistance element. This dumps stored DC bus stored charge via the transformer parasitic capacitance C_{tx} into the gate of S_1, which turns it on to begin the pulsed energy transfer cycle.

DIAC D_1 remains in conduction until its current drops below its minimum holding threshold, which happens very rapidly as the drain-to-source voltage of S_1 falls.

Switch S_1 then remains on until the DC bus voltage has discharged to zero. After this, the energy stored in the coupled inductance transfers to the secondary output to complete the energy pulse cycle.

For an appropriate design of the system, it is required first to understand the behaviour of the circuit. Over the next section, the switching waveforms of the system will be described as observed in a Low-Voltage (LV) triggering experiment.

5.2 Detailed Circuit Response

To conveniently study the circuit response in detail, the conversion system described in the last section was fed from a 500V DC supply feeding through a 10MΩ resistor, which allowed the rectified dc bus voltage v_d to slowly charge up towards 500V over several seconds. The DIAC string breakover voltage was reduced to 284V (8 individual DIACs in series) so that the flyback converter would trigger at this lower dc bus voltage. This arrangement allowed detailed switching waveforms to be captured without the difficulty of measuring them at full operating voltages. Figure 5.2 shows the experimental results, with switching waveforms presented over three different time scales to show the various stages of the energy transfer cycle.

- DIAC Breakover Interval (t_{bo}): The first 50 nanoseconds of switching in Figure 5.2 (left), where the MOSFET is triggered through the DIAC-based triggering.
- Energy Storage Interval (t_{ON}): The first 2 microseconds of switching in Figure 5.2 (centre), where the energy is transferred to the primary of the flyback transformer.
- Flyback Interval (t_{fly}): The first 40 microseconds of switching in Figure 5.2 (right), which is the normal flyback sequence for energy transfer into the secondary.
- Bus Recharge Interval (t_{ch}): The interval beyond Figure 5.2 (right), where the DC bus is slowly recharged from the low-current AC supply.

These intervals will now be discussed in detail.

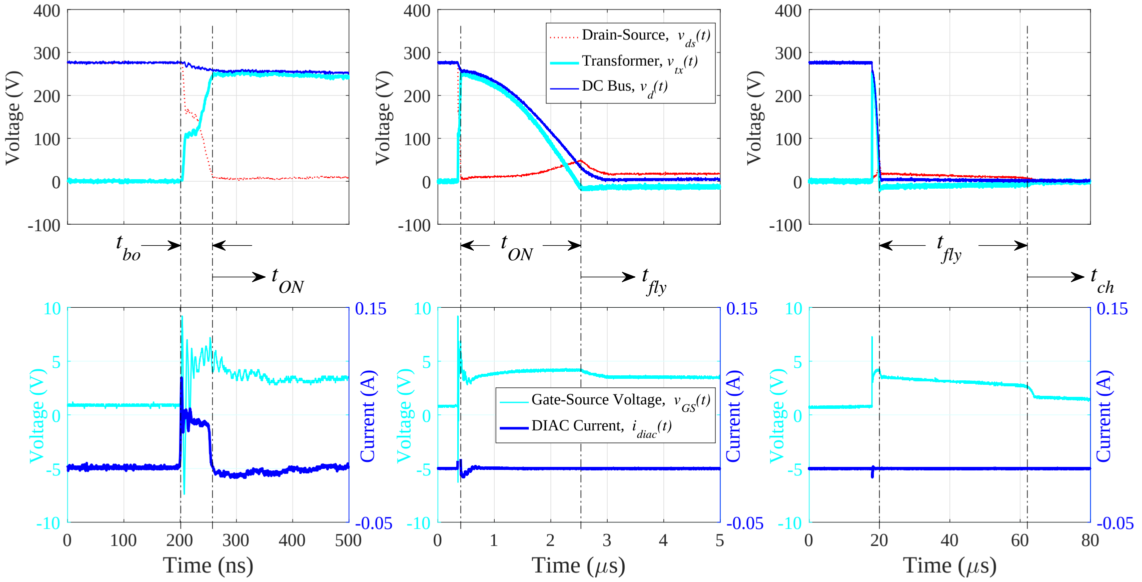


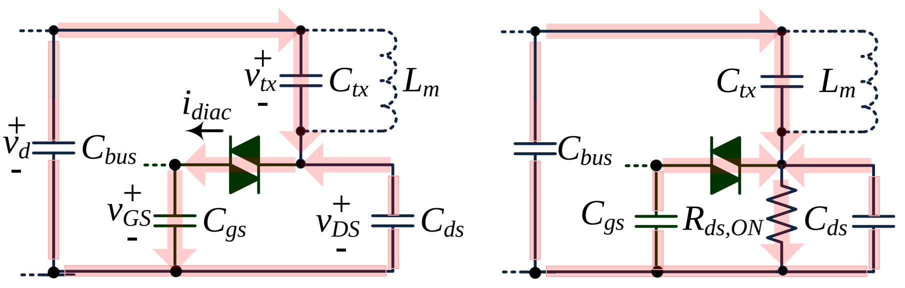
Figure 5.2: Switching waveforms for one energy transfer pulse in the scale of 500ns(left), 10μs(centre) and 100μs(right).

5.2.1 DIAC Breakover Interval

This stage starts when the DC bus voltage reaches the breakover voltage of the DIAC string, V_{bo} and becomes a low resistance. This makes it conduct a pulse of current to transfer charge from the overall DC bus capacitance C_{bus} combined with the S_1 drain-source capacitance C_{ds}, into the S_1 gate-source capacitance C_{gs} as per the equivalent circuit shown in Figure 5.3a.

The overall DC bus capacitance is defined with the parasitic capacitances shown in Figure 5.1 as:

$$C_{bus} = C_1 + C_2 + 2C_d + C_b \tag{5.1}$$



(a) Gate charge **(b)** Gate equilibrium

Figure 5.3: Equivalent circuits during the DIAC breakover.

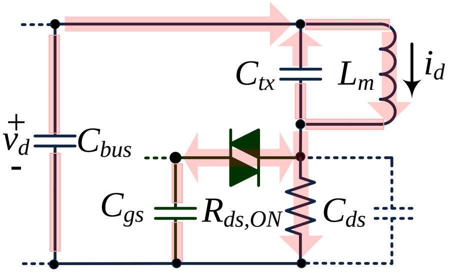


Figure 5.4: Equivalent circuit during the energy storage interval.

Consequently, the gate voltage of S_1 rises to its threshold level, turning it on to create a low resistance path between its drain and source terminals, $R_{ds,ON}$ as shown in Figure 5.3b.

In the response of Figure 5.2 (left) it can be seen that as S_1 turns on, its Drain-Source voltage falls to zero, impressing the DC bus voltage across the primary winding of the flyback transformer and thus starting the energy transfer cycle. When this drain-source voltage reaches zero, the current flowing through D_1 ceases since it is now short circuited by the S_1 on-resistance $R_{ds,ON}$. This completes the turn-on process, with enough charge stored in the gate capacitance of S_1 for it to continue to conduct for the next t_{ON} period.

From Figure 5.2, it can also be seen how the total gate charge needed to turn the MOSFET on, q_{gs} is transferred from C_{bus} to C_{gs} during t_{bo}, while reducing the DC bus voltage from its original value V_{bo} to V_h, which is determined from the charge redistribution process as

$$V_h \approx \frac{C_{bus}}{C_{bus} + C_{tx}} \left(V_{bo} - \frac{q_{gs}}{C_{bus} + C_{ds}} \right) \tag{5.2}$$

The voltage V_h is thus established across the transformer primary winding at the start of the next switching interval, t_{ON}.

5.2.2 Energy Storage Interval

During this second stage, the flyback transformer magnetising inductance L_m remains connected across the DC bus through the channel resistance $R_{ds,ON}$ of S_1 as shown in Figure 5.4.

This creates an LC circuit through which the energy from the DC bus total paralleled capacitance C_{ON} transfers to the magnetising inductance L_m as a quarter cycle oscillation. The DC bus total paralleled capacitance during this switching interval is defined as

$$C_{ON} = C_1 + C_2 + 2C_d + C_b + C_{tx} = C_{bus} + C_{tx} \tag{5.3}$$

From the upper trace in Figure 5.2 (centre), it can be seen how the current through S_1 created by this response increases its drain-source voltage. This is because the channel resistance of S_1 is relatively high as it is not turned on particularly well.

Furthermore, and somewhat paradoxically, it is interesting to see that this increasing drain-source voltage slightly increases the gate-source voltage of S_1 as can be seen in the lower trace of Figure 5.2 (centre), via coupling through the drain-gate capacitance. However, this second order effect has little influence on t_{ON}.

The response of the LC circuit during t_{ON} can be approximately determined using simple AC circuit theory (ignoring the increasing drain-source voltage across S_1) as

$$v_d(t) \approx V_h \cos(t/\sqrt{L_m C_{ON}}) \approx v_{tx}(t) \tag{5.4a}$$

$$i_d(t) \approx V_h \sqrt{C_{ON}/L_m} \sin(t/\sqrt{L_m C_{ON}}) \tag{5.4b}$$

The switching interval t_{ON} finishes when the voltage across the transformer primary winding passes through zero, and changes polarity. Using the approximation that the DC bus voltage is essentially zero at this point, t_{ON} can calculated by determining when (5.4 a) reaches zero, i.e.

$$t_{ON} = (\pi/2)\sqrt{L_m C_{ON}} \tag{5.5}$$

The energy transferred to the magnetising inductance during the energy pulse can then be calculated by

$$E_d = \int_0^{t_{ON}} v_d(t) i_d(t) dt \tag{5.6}$$

which, substituting from (5.4) and (5.5), solves as

$$E_d = \frac{1}{2} C_{ON} {V_h}^2 \tag{5.7}$$

Eqn. (5.7) identifies the maximum energy that can be extracted from the DC bus consolidated capacitance for one energy transfer pulse, without taking losses into account.

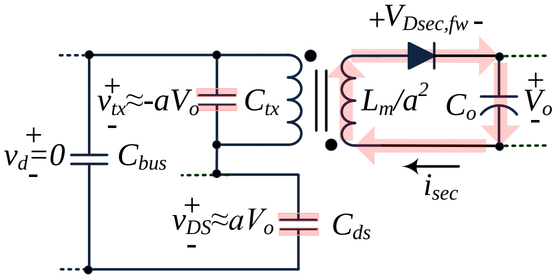


Figure 5.5: Equivalent circuit during the flyback interval.

5.2.3 Flyback Interval

Figure 5.2 (right) shows waveforms for the flyback interval t_{fly}, which begins when the voltage across the flyback transfer primary winding reverses and the secondary winding rises to the voltage $V_o + V_{Dsec,fw}$ (i.e. sufficient to turn on the secondary rectifier diode with a forward voltage of $V_{Dsec,fw}$). This provides a discharge path to the output filter capacitor C_o, as shown in the equivalent circuit of Figure 5.5, which allows the energy stored in the magnetising inductance to transfer to this capacitor.

As the secondary winding current increases at the start of t_{fly}, the primary winding current correspondingly decreases by transformer action. This can be seen by the reducing drain-source voltage of S_1 in the upper plot of Figure 5.2 (centre) at the start of t_{fly}. This reducing voltage decreases the gate-source voltage of S_1 through drain-gate capacitance coupling, as shown in the lower plot of Figure 5.2 (centre), which usefully helps turn it off in preparation for the flyback energy transfer to the secondary side.

The secondary winding discharge current i_{sec} now continues until all the stored magnetic energy has been transferred to the output capacitor at the end of t_{fly}, i .e.

$$q_{fly}(t) = \int_0^{t_{fly}} i_{sec}(t)dt = C_o \Delta V_o \approx \frac{t_{fly} Isec(max)}{2} \tag{5.8}$$

using the conventional flyback converter assumption of a triangular approximation for the shape of $i_{sec}(t)$.

Since $i_{sec}(t) = ai_d(t)$ due to mmf balance in the flyback transformer, then $I_{sec}(max)$ can be determined from (5.4) as

$$I_{sec}(max) = aI_d(max) = aV_h \sqrt{C_{ON}/L_m} \tag{5.9}$$

where a is the turns ratio of the transformer.

Without considering losses, the energy stored in the magnetising inductance during t_{ON} is equal to the energy transferred to the output capacitor i.e.

$$E_o = V_o C_o \Delta V_o \approx E_d \tag{5.10}$$

Combining (5.7), (5.8) and (5.9) then gives an estimate of t_{fly} as

$$t_{fly} \approx \frac{V_h \sqrt{L_m C_{ON}}}{a V_o} \tag{5.11}$$

At the end of this interval, the secondary rectifier diode turns off, the primary and secondary transformer winding voltages become zero (matching the discharged DC bus voltage) and the HV DC bus is ready for recharge.

From Figure 5.2 (right), it can also be seen how the gate capacitance of S_1 has significantly discharged during this period, via the gate discharge resistance. Note that the time constant of this RC circuit has to be set to make sure the gate voltage is sufficiently low at the end of t_{fly} to ensure that S_1 remains turned off as the HV DC bus now recharges in the next interval.

5.2.4 DC Bus Recharge Interval

At the end of each energy transfer pulse, the DC bus circuit reverts to an ideal capacitor divider, comprising C_1 and the total consolidated capacitance of the DC bus at this interval, defined as

$$C_{OFF} = C_2 + 2C_d + C_b + C_{ds} \tag{5.12}$$

which is fed from the rectified incoming AC line voltage.

The voltage across C_{OFF} (the DC bus) begins rising from zero at the start of this recharge interval t_{ch}, and can be expressed as the offset sinusoid of

$$v_d(t) = V_{OFF,peak} \sin(\omega_o t + \varphi) - V_{OFF,peak} \sin \varphi \tag{5.13}$$

where $V_{OFF,peak} = V_{lines,peak} C_1/(C_1 + C_{OFF})$, and $\varphi = \omega_o t$ is the phase angle of the AC input voltage at which each DC bus recharging cycle starts. Eqn.(5.13) can be linearized over each t_{ch} period as

$$v_d(t) \approx t\omega_o V_{OFF,peak} \cos \varphi, t \in t_{ch} \tag{5.14}$$

Note that (5.14) is always linearly increasing for each recharge interval over the range $-\pi/2 \leq \varphi \leq \pi/2$ since the input current through C_1 leads the AC input voltage by $\pi/2$), which is the period where one diode pair of the input rectifier is conducting. Furthermore, since the cycle of discharge and recharge repeats symmetrically for each AC half cycle, the recharge stage only needs to be analysed over one half cycle period.

At the end of t_{ch}, the DC bus voltage will reach the breakover voltage of the DIAC string again and start a new energy transfer cycle. Hence the number of energy transfer pulses that occur in each AC half cycle depends on the value of t_{ch}. For each pulse cycle, t_{ch} can be solved from (5.14) by setting $v_d(t_{ch}) = V_{bo}$.

However, it is also clear from (5.14) that t_{ch} is not constant but is instead a function of φ which varies as the incoming AC voltage magnitude changes. Hence an average value for t_{ch} needs to be found by recognising that

$$v_d(t_{ch}) = V_{bo} = \omega_o V_{OFF,peak} \overline{\cos\varphi}\,\overline{t_{ch}} \tag{5.15}$$

over the period $-\pi/2 \leq \varphi \leq \pi/2$. Since

$$\overline{\cos\varphi} = (1/\pi) \int_{-\pi/2}^{\pi/2} = 2/\pi \tag{5.16}$$

then $\overline{t_{ch}}$ can be solved as

$$\overline{t_{ch}} \approx \frac{\pi V_{bo}}{2\omega_o V_{OFF,peak}} \tag{5.17}$$

which provides an estimate for the average duration of the recharge interval. This allows the number energy pulses expected for each fundamental half cycle to be predicted, as will be shown in the next section.

5.2.5 Energy Transferred

Ignoring losses for now, the total energy transferred through the flyback transformer in one AC source half cycle is nE_d, where n is the number of pulses which occur during that period. Since $t_{ch} >> t_{fly} > t_{ON}$, the number of recharge cycles that occur during each half-cycle can be approximately estimated as the greatest integer of the expression $(T_o/2)/\overline{t_{ch}}$ where $T_o = 1/f_o$ is the period of the input AC line voltage. Using (5.17), this gives

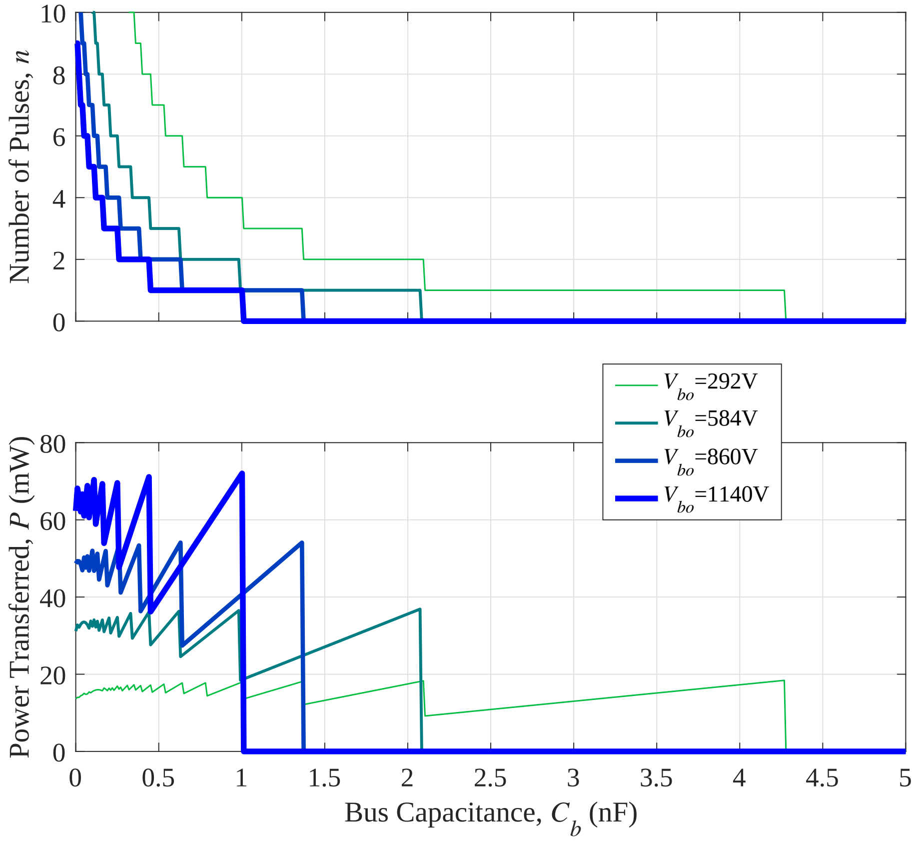


Figure 5.6: Number of energy transfer pulses in half-cycle (top) and power transferred to the flyback transformer (bottom).

$$n \approx \left\lfloor \frac{2C_1 V_{line,peak}}{C_{OFF} V_{bo}} \right\rfloor \tag{5.18}$$

With a total energy harvested per half cycle of nE_d, the total continuously scavenged power is then given by

$$P \approx nE_d \omega_o / \pi \tag{5.19}$$

Equations (5.7), (5.18) and (5.19) define the relationship between the output power, the pulse transfer breakover voltage V_{bo} and the DC bus capacitance C_b. Figure 5.6 depicts this relationship for values of C_b up to 5 nF, and for four break over voltages V_{bo} = [292, 584, 860, 1140] V, without considering any losses in the system.

As can be seen in Figure 5.6 (top), the discrete number of energy transfer pulses in each AC source half-cycle drops with larger breakover voltage levels and larger bus capacitances. In-between each band given by the discrete values of n, the obtained power shown in Figure 5.6 (bottom) varies proportionally to the changes in added bus capacitance C_b over a narrow range of picofarads. The maximum possible achievable power for each band at a given triggering voltage V_{bo}, however, is constant. In addition, the power increases as the triggering voltage gets higher, provided that the given bus capacitance is not high enough to bring the number of pulses to zero, in which case the power collapses to zero too.

As a result, the power transfer is extremely sensitive to the changes in bus capacitance. For instance, with a breakover voltage of 292 V, the power reaches a maximum of 18 mW for about 4.3 nF capacitance. However, for a slightly larger capacitance the power abruptly collapses to zero as the number of half-period pulses drops below one (zero).

From this analysis, it is generally preferable to keep the bus capacitance as low as possible to achieve maximum power transfer. However, even with a zero DC bus capacitance, in practice there will always be parasitic capacitances in the system which limit the number of energy transfer pulses that can be achieved. This issue will be discussed further in Section 5.4. Furthermore, another important consideration for maximising the extracted power are the system losses, which will now be addressed.

5.3 Circuit Losses

This section discusses the loss mechanisms that showed to be the most relevant to the system, according to the experimental studies presented later in Section 5.4, namely the bus capacitance charge redistribution, MOSFET and secondary diode losses. Additional losses in other elements in the circuit of Figure 5.1 such as: the protection Zener V_Z which, while not in breakover, dissipates only 14 nW via its leakage current; the reverse bias junction capacitance of the secondary diode C_{Dsec}, which reflecting back through the coupled inductor produces dv/dt losses related to sudden changes of primary voltage of less than 1% of the total bus energy; and the magnetic, hysteresis losses of the core of the coupled inductor, which were estimated to be of around 0.4% of E_d; are considered negligible.

5.3.1 Charge Redistribution

The first loss mechanism in the system is the charge redistribution process that takes place during the DIAC breakover interval. As was discussed in Section 5.2.1, the charge necessary for S_1 to turn-on is transferred from the DC bus, which loses energy in the process. As a result, the bus voltage drops from V_{bo} to V_h according to (5.2). The energy in the DC bus per energy-transfer pulse of the converter has thus been reduced from an initially available amount of

$$E_i = \frac{1}{2}(C_{bus} + C_{ds}){V_{bo}}^2 \tag{5.20}$$

to E_d in (5.7). Part of this energy contributes to the turn-on of the main switch S_1, which while necessary, is of course a loss. The rest of this energy is dissipated in other elements of the triggering circuit in Figure 5.1, namely the DIAC string and gate-source resistance. This loss represents around 3% of the total theoretically available energy, E_i.

From here, the energy left E_d is diluted by additional losses, which will be quantified for each energy-transfer pulse. Essentially the most significant losses in the circuit occur in the MOSFET S_1 and in the secondary diode of the flyback transformer D_{sec}.

5.3.2 MOSFET

For this circuit, the soft turn-on of the MOSFET during the energy storage interval t_{ON} produces a significant resistive loss. This is because the channel resistance $R_{ds,ON}$ is much larger than is usual since the gate-source voltage during t_{ON} is only just above the minimum gate threshold $V_{GS(th)}$. Identifying this resistance from data sheets is not straightforward, since the gate voltage is very hard to determine. Instead an estimated value for $R_{ds,ON}$ was found as follows:

Using the experimental results presented in Section 5.2, the drain-source voltage $v_{ds}(t)$ during t_{ON} was directly measured from Figure 5.2 (middle), while the drain current $i_d(t)$ was approximately determined using (5.4b), since its direct observation using a measurement probe is challenging due to loading effects. The instantaneous value of $R_{ds,ON}$ was then calculated as

$$R_{ds,ON}(t) \approx v_{ds}(t)/i_d(t) \tag{5.21}$$

which was then averaged over t_{ON}, which is the interval of interest. This gave a value of $\overline{R_{ds,ON}} \approx 620\Omega$. Using again the expression of $i_d(t)$ in (5.4b), as well as the approximation of t_{ON} in (5.5), this leads to an energy loss on the switch over t_{ON} of

$$E_{loss,sw} \approx \int_0^{t_{ON}} {i_d}^2 \overline{R_{ds,ON}} dt = \frac{\pi C_{ON} \overline{R_{ds,ON}} {V_h}^2 \sqrt{C_{ON}/L_m}}{4} \tag{5.22}$$

Equation (5.22) defines the energy per pulse dissipated in $R_{ds,ON}$ during the energy storage switching interval t_{ON}. Note that this loss is proportional not only to $R_{ds,ON}$

but also to the peak DC bus voltage V_h and capacitance C_{ON}. Experimentally, it accounts for about 44% of the total theoretically available energy, as will be seen in Section 5.4.

5.3.3 Secondary Diode

During the flyback interval t_{fly}, the secondary current through the diode D_{sec} causes an energy loss because of the diode forward voltage $V_{Dsec,fw}$ on the device. The expression for this loss is given by

$$E_{loss,Dsec} = \int_0^{t_{fly}} V_{Dsec,fw} i_{sec}(t) dt \tag{5.23}$$

The expression in (5.23) can be evaluated considering that the waveform of the secondary current $i_{sec}(t)$ can be approximated as a triangle of height $I_{sec}(max)$ and base t_{fly}, as per the conventional theory for flyback converters [157]. Hence, using the approximations previously developed in Section 5.2.3, (5.9) and (5.11) for $I_{sec}(max)$ and t_{fly}, respectively, the value of this loss solves approximately to

$$E_{loss,Dsec} \approx \frac{V_{Dsec,fw} {V_h}^2 C_{ON}}{2V_o} \tag{5.24}$$

This loss is dependent on the forward voltage drop of the secondary diode and the maximum DC bus voltage. Experimentally, it accounts for 25% of the total theoretically available energy, as will be seen in Section 5.4.

5.4 Experimental Validation in MV

The coupled inductor (flyback transformer) and other major system components of the switching system in Figure 5.1 were implemented in an experimental prototype on a PCB. The main design parameters are summarised in Table 5.1. A more detailed description of the implementation is given in Chapter 7, which in turn follows the design principles detailed in Appendix A.

The experimental prototype was tested under full scale operating conditions with a MV AC supply to confirm the operation of the energy harvester under realistic operating conditions. However, the 12.7kV line voltage was represented using the 4.5kV (RMS) AC supply available in the laboratory, feeding through a 100 pF HV coupling capacitor. This generated a maximum input current of 150 μA, which is the

Table 5.1: Main design parameters.

Element	Parameter	Value
Flyback transformer		
Turns-ratio	a	4.47
Number of primary turns	N_1	148
Magnetising inductance	L_m	5.5mH
Inter-winding capacitance	C_{tx}	30.7pF
Core/Material		RM12/N41
DBR Diodes		BYG10Y
OFF Capacitance	C_d	2 pF
MOSFET (nominal)		C2M1000170D
Drain-Source capacitance	C_{ds}	50pF
Gate-Source Capacitance	C_{gs}	170pF
Secondary diode		MURS480ET3G
Forward voltage	$V_{Dsec,fw}$	1V
DIACs (each)		SMDB3
Individual breakover	V_{bo_i}	32V
Designed lead resistance	R_{diac}	470Ω
Output Circuit		
Output capacitor	C_o	5.6mF
Tested output load	R_o	820Ω

same order of magnitude as for the full line voltage system discussed in Section 3.2. Hence the proposed converter was working essentially at the designed maximum input triggering voltage and current levels (approximately 1kV and about 150 μA, respectively) so the study results matched what could be expected for a full field conditions, without losing any generality in the study. A complete description of this experimental arrangement is presented in Chapter 7.

Figure 5.7 shows the experimental arrangement, which was found to introduce some additional capacitance C_{extra} to the DC bus. This capacitance was determined experimentally to be 660 pF, and adds to the parameter C_b identified in the theoretical analysis of Section 5.2. Such considerations are critical to evaluate a converter such as this, since the various conducted tests and the analysis shown in Figure 5.6 have shown that the overall system is highly sensitive to any change in the effective bus capacitance.

To identify the best possible power transfer conditions, different combinations of V_{bo} and C_b were then evaluated. V_{bo} was adjusted by setting a link on the PCB, to choose between the four series strings of eight DIACs each, as detailed in Chapter 7. This allowed the response of the four triggering voltages of V_{bo} = [292, 584, 860, 1140]V to be evaluated. Overall bus capacitances (C_b) of up to 1nF (i.e. the sum of the actual C_b and C_{extra} were then tested at each trigger voltage to determine the maximum possible power transfer that could be achieved).

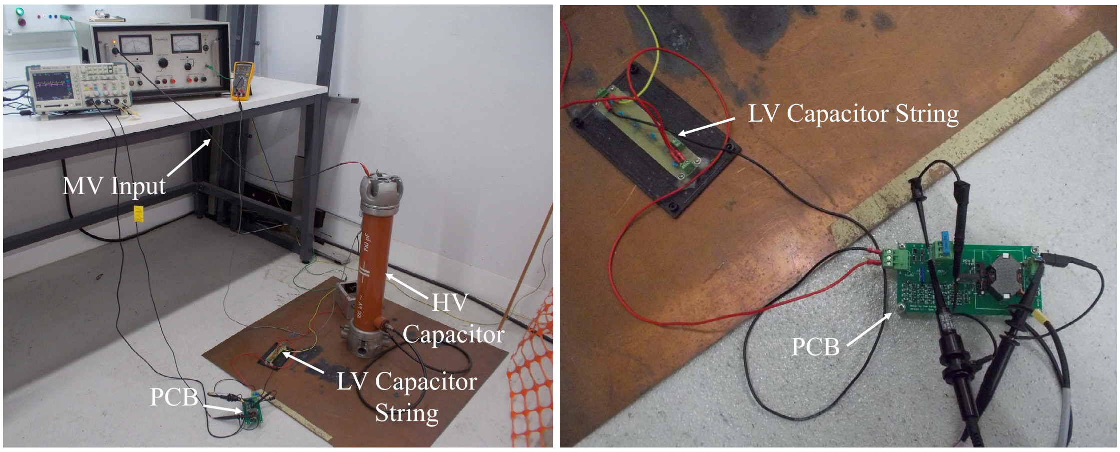


Figure 5.7: MV experimental setup.

From these tests, it was found that maximum power transfer was achieved with all four DIAC strings in series (a triggering voltage of V_{bo} =1.14kV), with a total effective bus capacitance of $C_b + C_{extra}$ = 1nF. These conditions were then used for theoretical power transfer calculations based on the concepts presented in Section 5.2. The results are shown in Table 5.2, and predict a continuous output power of 21.7mW. This represents a power transfer efficiency of 31%, with about 44% losses in the main MOSFET switch and 25% losses in the secondary diode.

Experimental waveforms for this condition are shown for two different time scales in Figure 5.8 (left) and Figure 5.8 (centre), for one energy transfer pulse. As can be seen in Figure 5.8 (left), when the DC bus voltage rises to 1.14 kV, the diac string triggers, and the DC bus discharges in about 3 μs as predicted by the theoretical analysis. The secondary current i_{sec} can be seen for the flyback period in Figure 5.8 (centre), with its waveform showing the anticipated triangular discharge shape over a period of about 60 μs, again in accordance with the theoretical analysis presented in Section 5.2.

Note that the high frequency ring during the initial DIAC breakover period is primarily an artefact of common-mode voltage probe coupling, and illustrates the difficulty of making measurements for this type of application because the measurement probe loading effects are quite significant since measurement probes

Table 5.2: Theoretical energy transfer.

Parameter	Value	Description
E_d	713.4μJ	Energy available in the DC bus
n	1	Number of pulses per half-grid cycle
P	71.3mW	Power before losses
$E_{loss,sw}$	317μJ	MOSFET losses
$E_{loss,Dsec}$	178.3μJ	Secondary diode losses
P_o	21.7mW	Actual power harvested

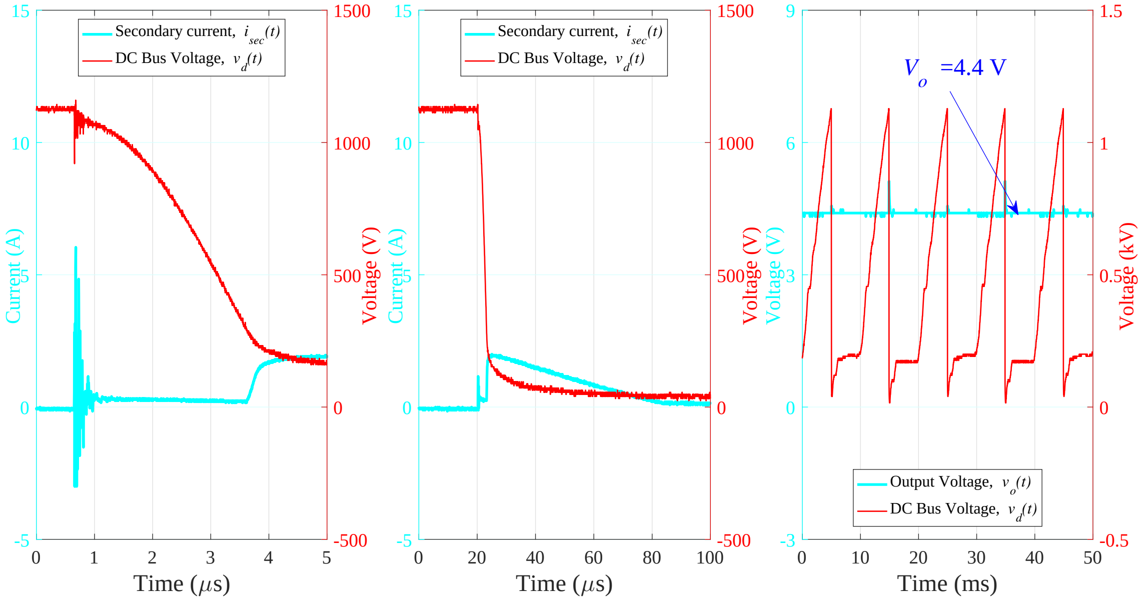


Figure 5.8: Experimental results at medium-voltage. (left)Scale of 5μs. (centre)Scale of 100μs. (right)Scale of 50ms

have nominal input impedances in the range of mega ohms (parasitic capacitances in the levels of picofarads), which are comparable with the capacitances of the EFEH divider. Hence their presence influences the measured waveforms at various points of the circuit, and often also disturbs the system operation.

Figure 5.8 (right) shows that the system achieves one energy transfer pulse for every 10 ms (half-grid cycle), and delivers an average output voltage of 4.4 V across the 820 Ω output load resistor. This represents a harvested output power of P_o =23.6mW, which matches very well with the theoretical expectations as presented in Table 5.2. Note that in general and as predicted by (5.7), larger triggering voltages V_{bo} manage to harvest more power. However they also produce larger losses, so that the best overall efficiency of the system that can be achieved remains at about 33%.

5.5 Summary

This chapter has presented a conversion system for non-contact electric field energy harvesting based on a flyback converter topology working in pulsed energy-transfer mode, which is completely self-triggered from the EFEH input supply. The proposed system does not require any additional auxiliary power supply for the control stage.

A detailed analytical study of the switching circuit and the power transferred was introduced. It was found that in general the switching circuit is extremely sensitive to added parasitic capacitances. The main loss mechanisms in the system were also identified.

Experimental results were presented to confirm the theoretical analysis and physical viability of the concept, in a medium-voltage experimental setup. The experimental study identifies that almost 24 mW of continuous power can be transferred from a 12.7kV MV line using a non-contact EFEH supply based on a power line insulator. This figure outperforms previous work in the literature in this field, not only for its larger power density but also for the features of a self-powered triggering cicuit and its design for a non-contact EFEH methodology.

Compared to the system proposed in Chapter 4 the conversion circuit presented in this chapter does not have additional losses related to the gate-driver of the main switch since this sub-circuit is self-powered. On the other hand, the nature of the gating circuit of this chapter does not allow for a higher number of pulses per half grid cycle, unlike in the system of Chapter 4. As a result, the principles of one system cannot be directly translated to the other and a precise comparison between both solutions is not possible beyond the evident benefit of the gate-driver self-powering in the design of the present chapter.

Chapter 6

Description of the Simulation Systems

In the investigation of the energy conversion topologies for Electric Field Energy Harvesting, the extremely low currents and high voltages associated with the application made the influence of parasitic elements around the circuitry of the systems much more relevant than in standard conversion applications. This difficulty has been identified throughout the thesis.

Therefore, suitable simulation models that take into account the parasitic impedances in the switching circuits were essential to verify the response of the experimental systems. Hence, the hypothesis that any particular waveform in the system (e.g. the peak value of a current) is influenced by one particular group of impedances in the system (e.g. the parasitic capacitance in the DC bus) can be readily verified by the modelling of this parasitic element in a computer simulation. This validation strategy has been used extensively throughout the experimental sections of the thesis.

In this work, MATLAB was used for the analytical design of the different proposed conversion systems, and basic simulation studies. Ansoft Maxwell 3D [148] was used for the Finite Element Analysis (FEA) of the EFEH harvester proposed in this study. The software package ALTIUM [166] was used for the design of the circuit boards built in the experimental sections, and for the simulation of various switches used in the proposed systems. However, the PSIM software package [167] was the predominant simulation tool in this work. It supports discrete time analysis of the electrical and electronic circuits that are part of switching systems with their corresponding logical controllers.

In the simulation environment, the use of standard models of switching devices showed limitations due to the unusual input conditions of EFEH, so alternative models were constructed. In this chapter, the most important simulation models developed for the study of the proposed conversion systems studied in this thesis are described.

6.1 Finite Element Analysis of the Harvester

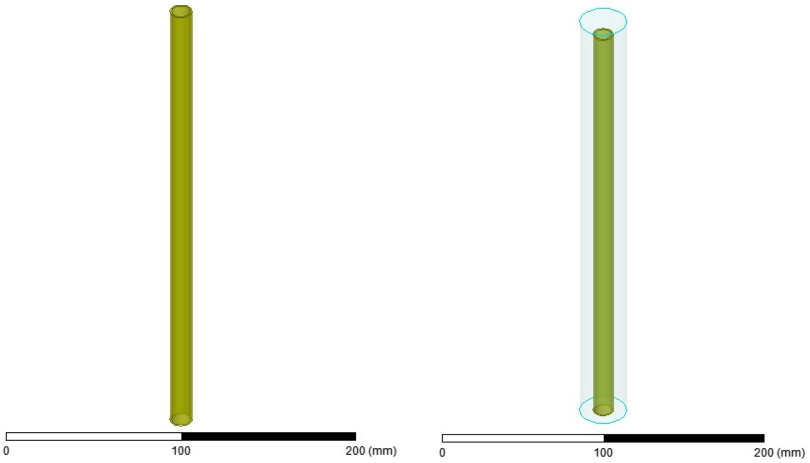
In the field of EFEH, Finite Element Analysis (FEA) is often used to investigate the field distribution of the varied geometries that form the capacitive dividers of the harvester structures and hence to estimate other field distributions like the electric flux density and parameters such as the values of capacitances in the dividers.

In this work, the Electrostatic type of solution analysis of the FEA software Ansoft Maxwell 3D was used. The first objective was to investigate the electric field distribution of the line insulator-based harvester proposed in Section 3.1.3, in order to verify that the field intensities in the structure at 12.7 kV are within safe levels, below the dielectric breakdown of the insulating media. The second objective was to estimate the values of the capacitances of the parasitic capacitive divider that is created by the proposed harvesting structure, and hence to establish the electrical nature of the input AC supply that is considered throughout the studies developed in this thesis.

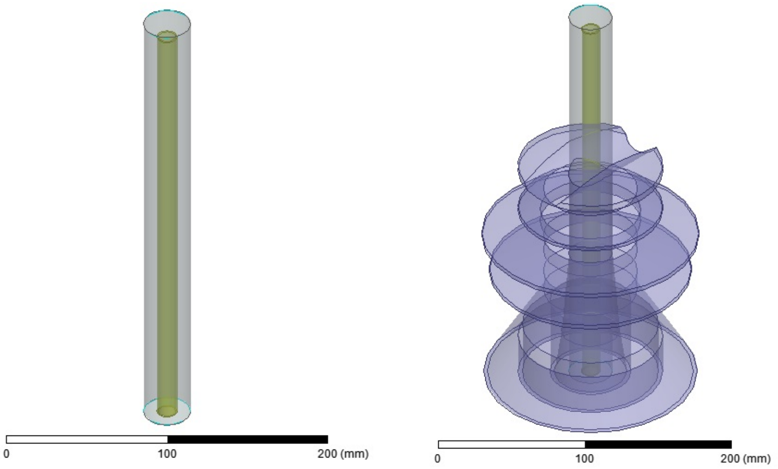
A 3D model of the harvester proposed in Section 3.1.3 and described in more detail in Section 7.1 was created. The steps of construction are described in Figure 6.1. The inner electrode is a Copper (Cu) tube with 12.7mm of outer diameter, which is inserted into an 30mm-diameter insulating Polypropylene (PP) rod represented with a semi-hollow cylinder i.e. filled with a disc at the top that provides 10mm of insulation (Figure 6.1b). This insulating medium is assigned a relative electric permittivity of 2.2.

The 300mm-long plastic clylinder is then surrounded by a very thin (0.2mm) Aluminium (Al) sheath, which represents the outer electrode. This cylindrical structure is then inserted into a modified pin-type power line insulator, with an extended pin cavity to fit the structure, and whose model is shown in Figure 6.1d. The insulator, made of epoxy resin, is assigned a relative electric permittivity of 4.4. Finally, a Copper structure that works as the support of the harvester system in the experiments of Section 3.1.4 is modelled in Figure 6.1e.

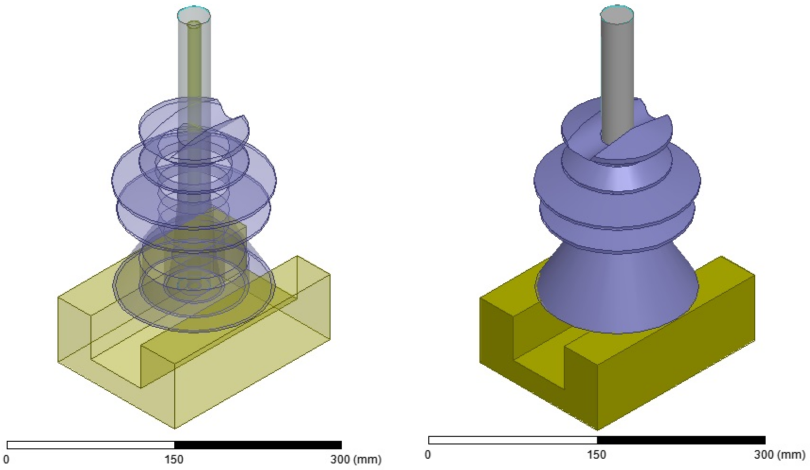
For the electrostatic analysis, the excitations of 12.7kV and 0V were assigned to the outer electrode and supporting structure respectively. The FEA was configured to run a maximum of 15 passes and 1% of error. The analysis for the results presented



(a) Inner electrode (Cu tube). **(b)** Insulating medium (PP rod).



(c) Outer electrode (Al sheath). **(d)** Power line insulator (Epoxy).



(e) Support structure (Cu). **(f)** Complete 3D model.

Figure 6.1: 3D model of proposed the insulator-based harvester.

in Section 3.1.4 converged after 3 adaptive passes with a 0.5% of energy error, and a total number of mesh elements (tetrahedra) of 43694. These results were validated experimentally in that section, which shows the accuracy of the model created.

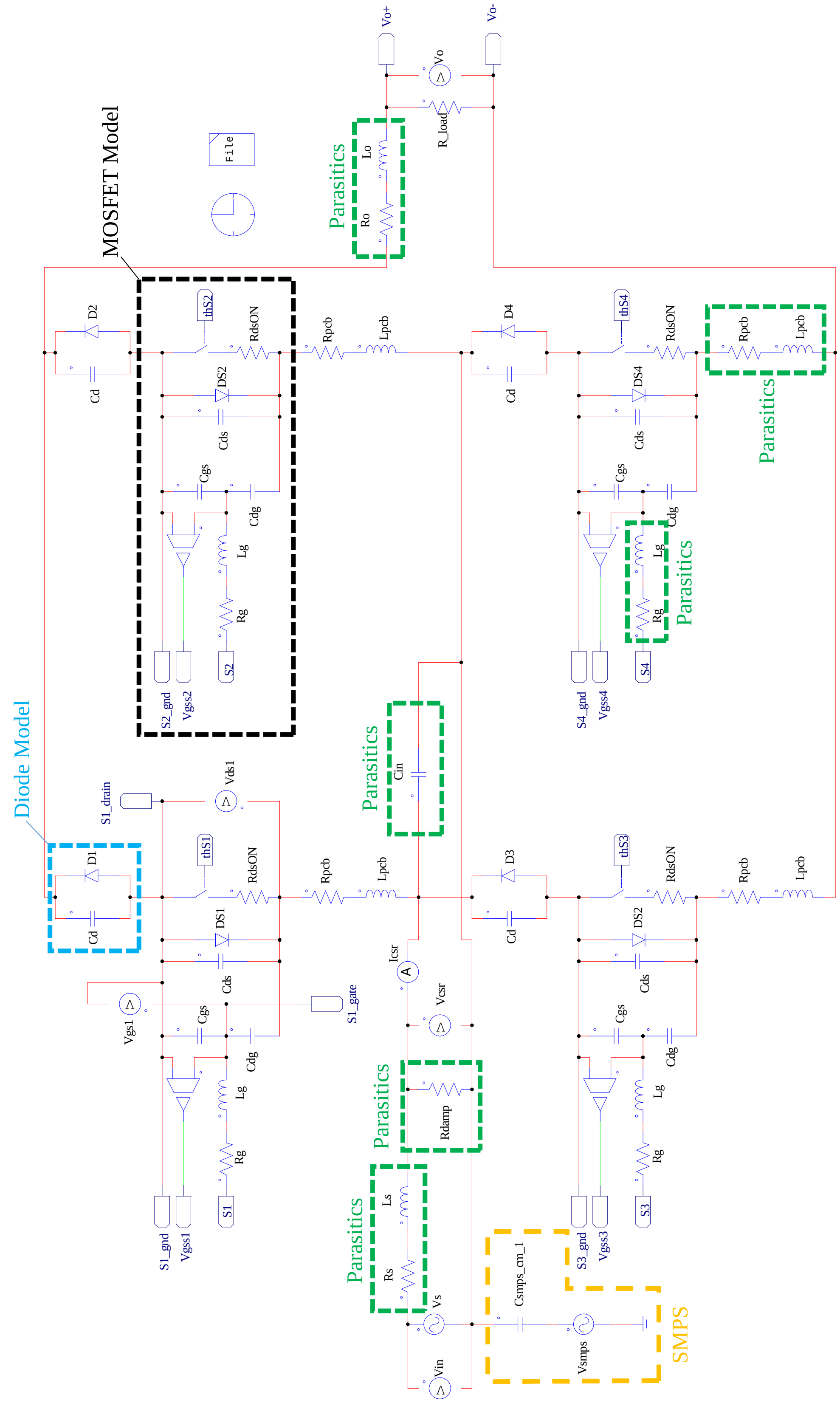
6.2 Current Source Rectifier Bridge

A PSIM simulation model of the CSR bridge investigated in Chapter 3 was used for the validation of the experimental waveforms in the low current switching setup presented in Section 3.3.1. The model is shown in Figure 6.2, and is divided into power and control stages. The power stage includes the following parts:

- A model for each one of the MV-rated C2M1000170D MOSFETs [158], which is composed of an ideal switch controlled by continuously comparing the Gate-Source voltage against the switch nominal threshold *Vth*. The model considers the MOSFET antiparallel diode *DS* with a voltage drop of 2 V, the MOSFET ON-resistance *RdsON* and its parasitic capacitances *Cds*, *Cgs* and *Cdg*. The latter capacitive elements are non-linear, which is challenging for an exact representation. Hence, the values were determined according to the curves provided in the respective datasheet, chosen depending on the input voltage levels under investigation.
- The parasitic parallel capacitances *Cd* of the blocking diodes of the CSR topology [168]. Again, its non-linear value is chosen according to the curves provided in the respective datasheet, depending on their working reverse voltage.
- The parasitic elements of the PCB, some components and wiring, whose values were either measured or estimated. These elements include: the AC input supply resistance *Rs* and inductance *Ls*, the parallel input damping resistance *Rdamp*, the parasitic capacitance across the input terminals of the CSR *Cin*, and the parasitic resistances and inductances of the output circuit (*Ro, Lo*), the gate driver circuitry (*Rg, Lg*) and PCB tracks (*Rpcb, Lpcb*). The parasitic capacitances between PCB traces were ignored because in practice they are swamped by the higher values of the capacitances of the switching devices.
- A voltage source *Vsmps* representing the coupling of the gate driver circuitry to the power circuit through the capacitance *Csmps_cm_1*, which was observed to add noise measurement in the execution of the experiments.

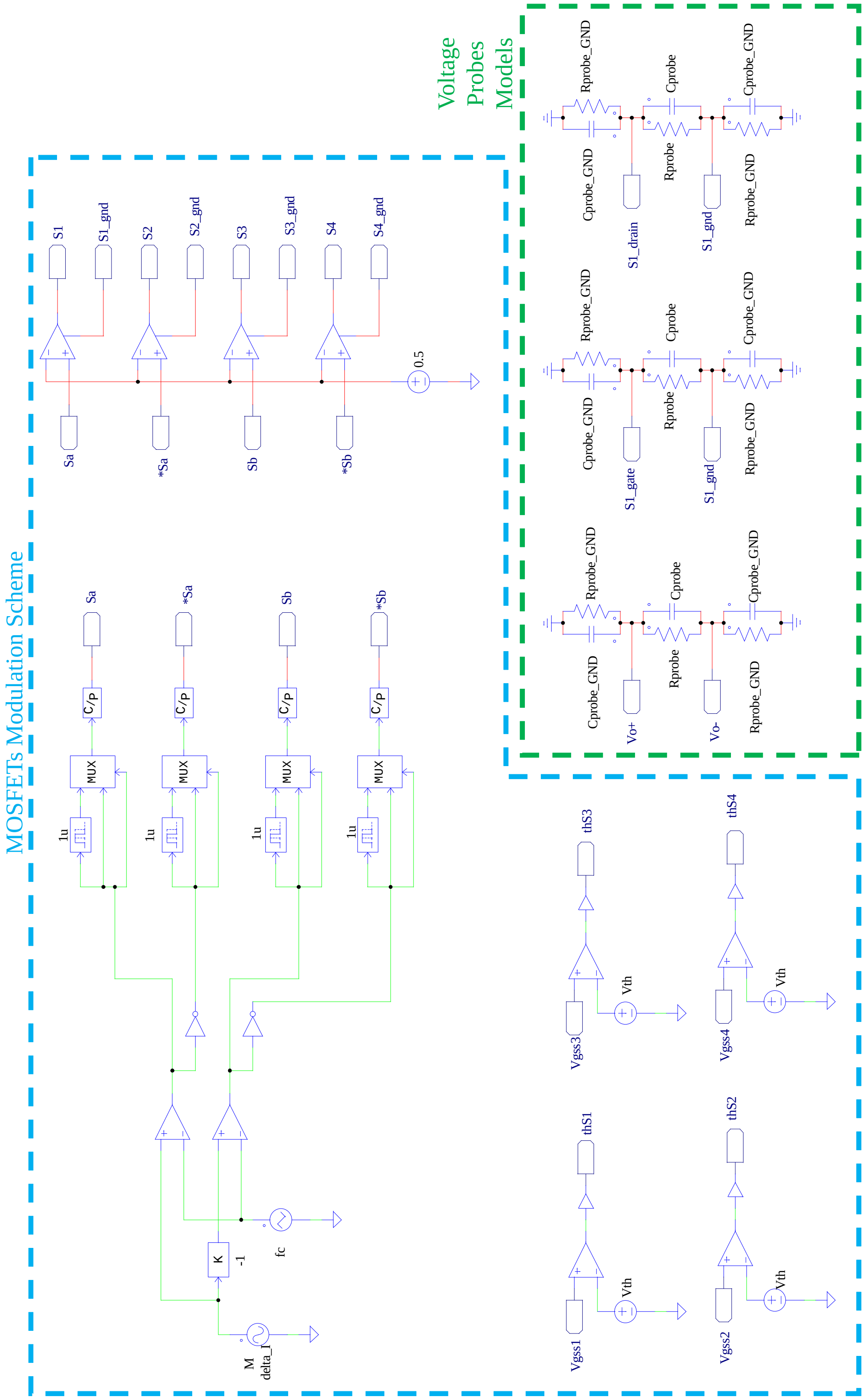
The control stage includes the following parts:

- A modulation scheme for each MOSFET that represents the floating circuitry of the gate driver that couples to the gate. It provides the option to program the standard modulation parameters i.e. modulation index *M* and carrier



(a) Power Stage

Figure 6.2: PSIM model of CSR bridge.



(b) Control Stage

Figure 6.2: (continued) PSIM model of CSR bridge.

Table 6.1: Referencial values of parameters of the CSR bridge PSIM model.

Parameter	Value	Description
Rs	0.22Ω	Input source resistance/Measured
Ls	300nH	Input source inductance/Measured
Rdamp	800MΩ	Damping resistor/Chosen
Cin	100pF	Input capacitance/Estimated
Rg	35Ω	Gate resistance/Datasheets
Lg	1nH	Gate inductance/Measured
Cdg	32pF	Drain-Gate cap/Estimated at 100V (OFF)
Cgs	4500pF	Gate-Source cap/Estimated at 100V (OFF)
Cds	1pF	Drain-Source cap/Estimated at 100V (OFF)
RdsON	1Ω	MOSFET ON resistance/Datasheet at 15V
Vth	3.5V	MOSFET Gate threshold voltage
Cd	2.5pF	Blocking diode cap/Estimated at 100V (OFF)
Rpcb	0.04Ω	PCB tracks resistance/Estimated
Lpcb	10nH	PCB tracks inductance/Estimated
Ro	0.15Ω	Output resistance/Measured
Lo	300nH	Output inductance/Measured
Vsmps	1V(peak)/100kHz	Common mode noise control board/Estimated
Csmps_cm_1	1pF	Coupling control board to ground/Estimated
Rprobe	11MΩ	P2220 voltage probe resistance/Datasheet
Cprobe	40pF	P2220 voltage probe capacitance/Datasheet
Rprobe_GND	5MΩ	Probe coupling to ground/Estimated
CProbe_GND	4pF	Probe coupling to ground/Estimated

frequency *fc*. Then it considers the switching differential voltage levels of the gate driver used for switching the MOSFET gate (+15V/-5V), as well as the 1 μs overlapping function of a CSR (analogous to the a dead-time in VSRs), programmed in the modulation technique. The gate driver excitation depends on the Gate-to-Source voltage surpassing the gate threshold voltage *Vth*, which is represented with comparators.

- The equivalent circuits of the voltage probes on the sections that were considered for measurements in the experiments. These include the inter-channel parasitic resistance and capacitance (*Rprobe, Cprobe*) of the CRO, and the parasitics of each one of the CRO's channel to ground (*Rprobe_GND, Cprobe_GND*).

Some reference values for the parameters in the model of Figure 6.2 are defined in Table 6.1.

The main limitation with the simulation of the CSR bridge presented in this section is the non-linearity of the majority of the parasitic elements found in the experimental setup. In particular, since the values of the parasitic capacitances in the MOSFETs depend on their instantaneous Drain-Source voltages, they are different for the ON and OFF intervals.

The consequence is that the accuracy of the model can be optimized only for OFF or ON intervals but not for both, as it is quite challenging to program a non-linear capacitance in PSIM. The values in Table 6.1 represent the optimisation for the OFF intervals, which was the focus of the study in Section 3.3.1 of Chapter 3, where the simulation model was useful for validating real observations of high-frequency switching at high voltage and low current.

6.3 Line-Frequency Conversion

The investigation of the switching characteristics of a HV-rated diode bridge rectifier under the unusual input conditions of EFEH studied in Chapter 3 were tested using standard diode models in PSIM. However, when comparing to analytical expectations, the AC input voltage and transferred power were dramatically reduced due to the inadequacy of the diode models.

It was determined that the reason for the inadequate response was the leakage current through the parasitic capacitors that PSIM uses to simulate the diodes when they are turned off, shown in Figure 6.3. Whereas in applications with larger currents, this leakage current is negligible and the final response of the circuit is accurate, in the present EFEH application (featuring some hundreds of microamperes at most) the leakage becomes more relevant. This situation is observed as well in MATLAB and in standard PSPICE models used in ALTIUM. In PSIM, the value of this parasitic capacitor cannot be programmed directly as a parameter of the diode.

The alternative representation that was used to circumvent this modelling limitation is shown in Figure 6.4. The diodes under study are the BYG10Y [163] rated for 1600V, and are represented by ideal switches with their parasitic capacitances *Cd*=2pF in parallel. The ideal switches are controlled by comparators to switch them ON and OFF according to their anode-to-cathode voltage state (i.e. forward junction voltage *Vfw*=˜2V), hence emulating the normal operation of the diode.

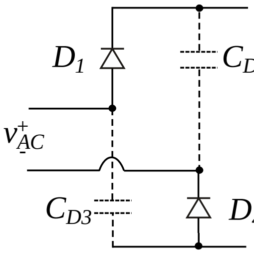
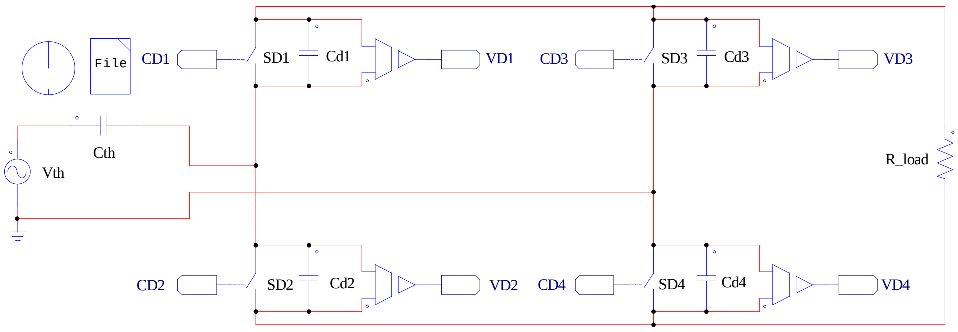
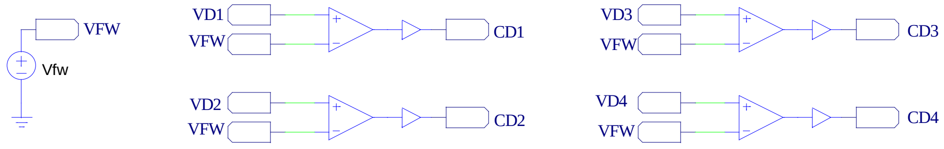


Figure 6.3: DBR turn-off parasitics for an AC input positive cycle.



(a) Power Stage



(b) Control Stage

Figure 6.4: PSIM model of a diode bridge rectifier for EFEH.

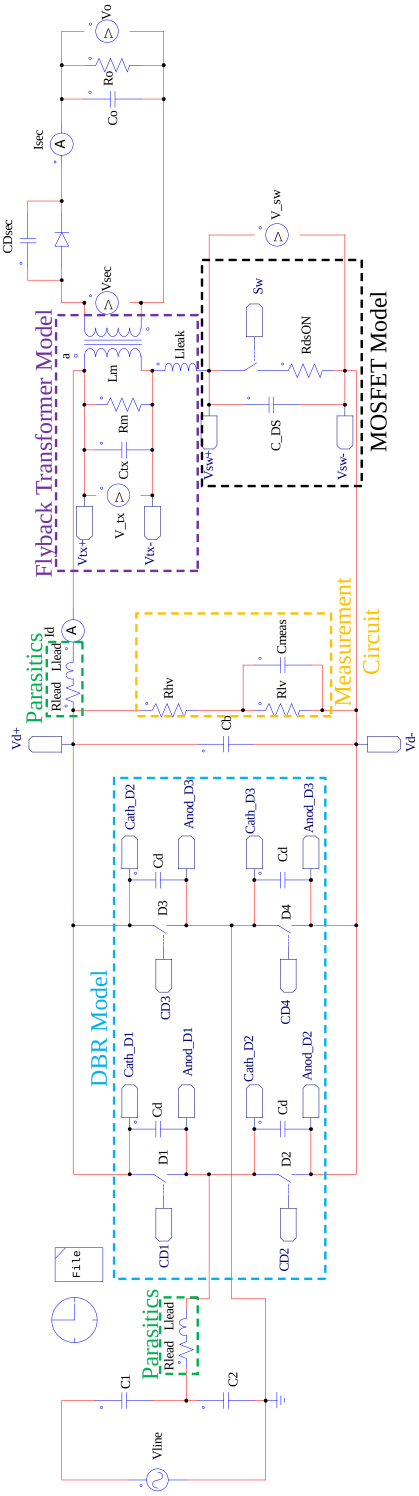
The parasitic capacitances can now be set to the levels that are appropriate for the simulation. In particular, it has been found that the parasitic capacitances of semiconductor devices rated for higher voltage (MV range) are lower than for standard devices. Hence the results yielded by this model were in better accordance with theory.

The basic model in Figure 6.4 has been extensively used in the exploration of the subsequent conversion strategies for EFEH that include a line-frequency switching stage in Chapter 4.

6.4 Pulsed-Mode Flyback Converter

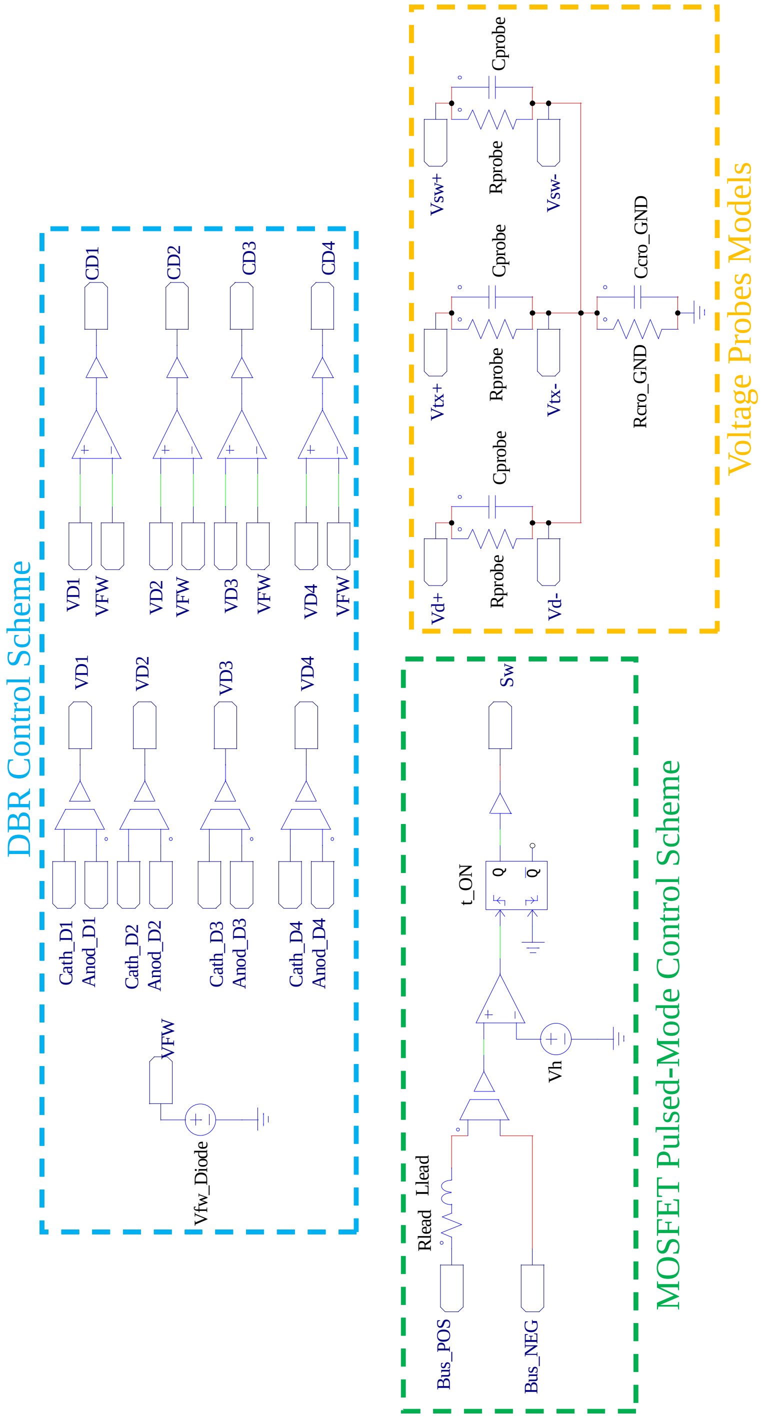
The PSIM simulation model of the novel pulsed-mode flyback converter for EFEH proposed in Chapter 4 was to validate the experimental waveforms in the LV and MV experiments proposed in Section 4.4.2 and Section 4.5 respectively. The model was described in Section 4.4.1 and is shown in Figure 6.5, where it is divided into power and control stages. The power stage includes the following parts:

- The alternative representation of a DBR model presented in Section 6.3. As this block is the first input to the EFEH divider, the currents through it are very small, as predicted in the analytical sections. Hence, standard diodes representation were not adequate and the advanced diode model was again necessary.



(a) Power Stage

Figure 6.5: PSIM model of the pulsed-mode flyback converter.



(b) Control Stage

Figure 6.5: (continued) PSIM model of the pulsed-mode flyback converter.

- A simplified model for the C2M1000170D MOSFET [158]. Since the recharge interval is the focus of study this time (Section 4.3) and because this is larger than the ON time, the Drain-to-Source capacitance only is included around the ideal switch. The ON resistance *RdsON* is still included to represent the loss mechanism. Capacitance *C_DS* is selected as per the datasheet, according to the respective voltage of the experiment, with the known limitation of its non-linearity.

- A model for the flyback transformer, which includes implicitly the definition of the magnetising inductance *Lm*. Explicit representations of the measured parasitic inter-winding capacitance *Ctx* and the resistor *Rm* (representing the calculated small core losses) were added, as well as the measured leakage inductance of the windings *Lleak*.

- The measurement circuit necessary for implementing the pulsed-mode control of the switch. This resistive divider is in parallel to the bus capacitor *Cb* and is composed of the high-voltage side and low-voltage side resistors *Rhv* and *Rlv*. The low-voltage resistor *Rlv* includes a parallel capacitor *Cmeas* representing the parasitic impedance of the circuitry of the subsequent control board in the PCB.

- The output circuit after the secondary of the flyback transformer has a simpler representation since the level of currents and voltages there are more conventional. However, the model of the secondary diode requires the inclusion of the OFF capacitance *CDsec* and the definition of its forward voltage.

- The parasitic resistance and inductance of the wiring using in the experimental setup (*Rlead, Llead*), with estimated values.

The control stage of the system includes:

- The control scheme for the DBR described in Section 6.3, with the anode-cathode voltage of each diode compared against the forward voltage *Vfw_diode*.

- A representation of the pulsed-mode control scheme for the MOSFET, made up of a comparator that implements the pulsed-mode control strategy. The bus voltage is continuously compared against the defined upper trigger voltage *Vh*. When the bus reaches this level, the signal for turning-on the MOSFET is held high for as long as the minimum response time of the comparator *t_ON* (taken from its datasheet), because the bus voltage drops almost immediately. This is represented by a monostable multivibrator with a pulse width *t_ON*.

Table 6.2: Pulsed-Flyback converter simulation parameters.

Parameter	Value	Description
Rlead	0.5Ω	Leads parasitic resistance
Llead	$1\mu H$	Leads parasitic inductance
Cd	2 pF	Diode BYG10Y parasitic capacitance
Rhv	50 MΩ	HV measurement resistance
Rlv	220 kΩ	LV measurement resistance
Cmeas	33 pF	Control stage equivalent loading, estimated
Rm	500kΩ	Emulating magnetic core losses
Lm	561 μH	Flyback transformer magnetising inductance
Lleak	1 nH	Flyback transformer leakage inductance
C_DS	13 pF	MOSFET C2M1000170D out. capacitance @500V
RdsON	1.4Ω	MOSFET Drain-Source resistance @500V
CDsec	30pF	Sec. diode junction capacitance @250V
Vfw_Diode	2V	Diode BYG10Y forward voltage
t_ON	300 ns	Min. response time comparator ADCMP609
Rprob	10MΩ	Voltage Probe TEKTRONIX P5100A
Cprob	16pF	Voltage Probe TEKTRONIX P5100A
Rcro_GND	14MΩ	CRO TEKTRONIX TPS200
Ccro_GND	37pF	CRO TEKTRONIX TPS200

- A model to represent the parasitic impedances of the voltage probes of the oscilloscope [165] (*Rprobe, Cprobe*), which also have a common single grounding rail coupled to earth through *Rcro_GND* and *Cro_GND*. This, again, models the loading introduced by the measurement devices in the circuit.

The values of the parameters were either measured or estimated and the most representative values are summarised in Table 6.2. Other values, for specific working conditions, have been defined in Section 4.4.1 of Chapter 4. Although the model has important limitations introduced by the non-linearity of the parasitic capacitive elements, the results that it yields are comparable with the experimental waveforms observed in practice (Sections 4.4.2 and 4.5), hence validating its effectiveness.

6.5 Summary

This chapter has presented an overview of the PSIM-based simulation system used throughout this thesis. The power and control stages of the different power electronic systems are represented using PSIM's built in power electronics discrete elements and blocks.

The simulation environments address the limitation of standard simulation models of switching devices, when used to represent the EFEH systems, by proposing alternative representations.

The simulations were developed to validate the experimental systems under the influence of several parasitic impedances. This is of particular importance in the field of EFEH, since the extremely low currents and high voltages manipulated within the circuits amplifies the influence of such parasitics.

Chapter 7

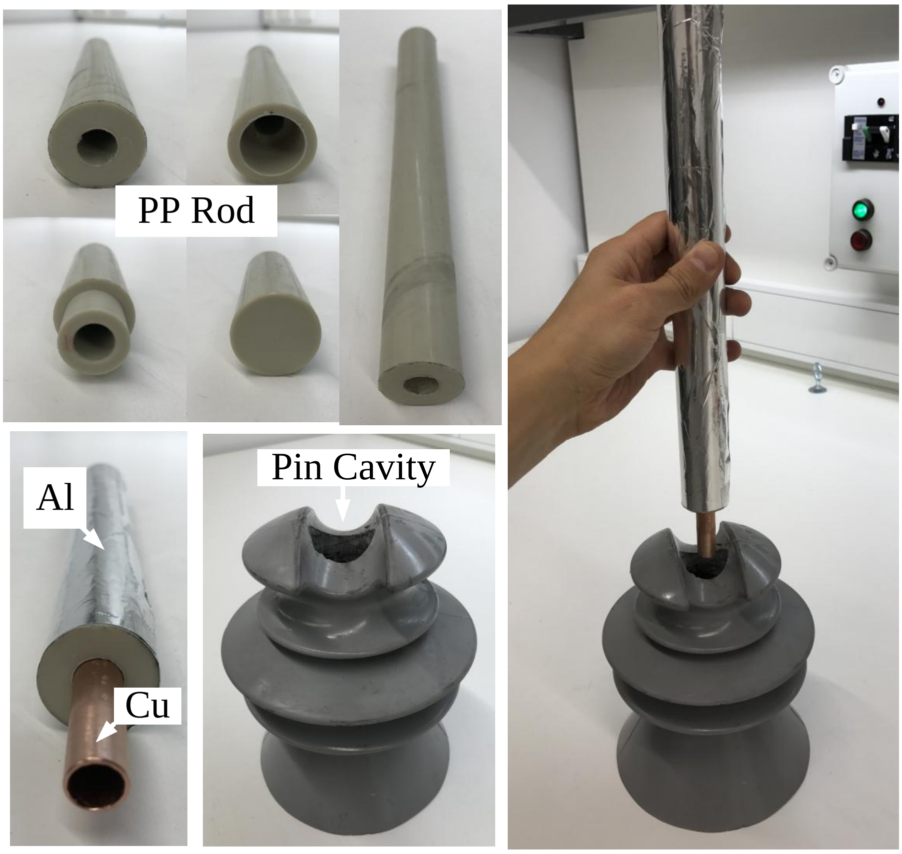
DESCRIPTION OF THE EXPERIMENTAL SYSTEMS

To validate the performance of the theoretical developments presented in this thesis, different experimental systems have been established in the RMIT University power electronics laboratory. The most important experimental implementations of the thesis are described in this chapter.

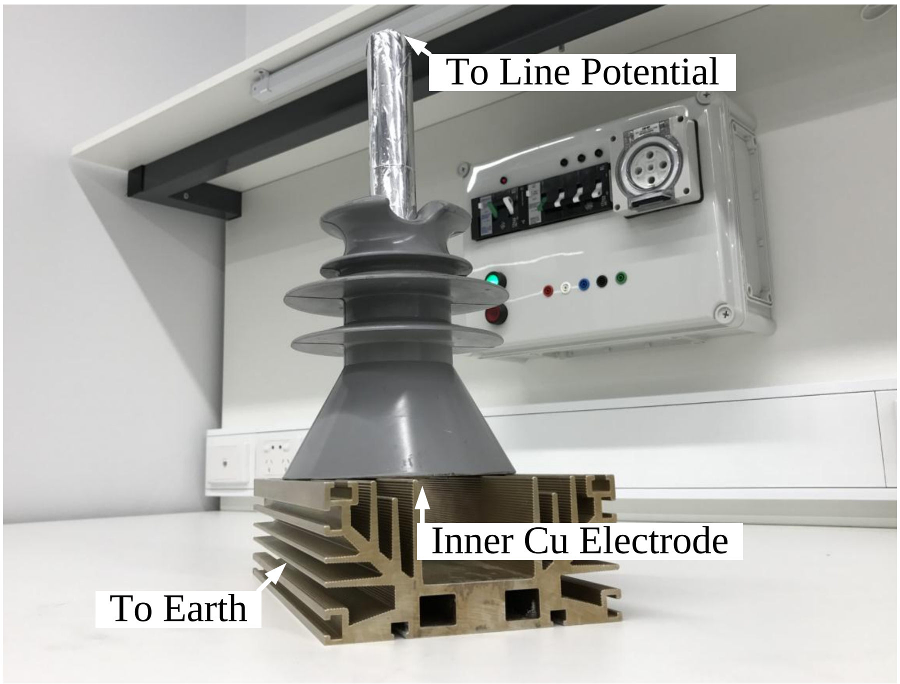
7.1 Power Line Insulator EFEH Harvester

The structure proposed in Section 3.1.4 of Chapter 3 for the exploration of the concept of EFEH, was built by modifying a standard pin-type power line insulator made of epoxy resin with a nano-filler. The alteration was made so that an electrode inserted within the grounded pin cavity of the insulator is allowed to form a capacitive divider with the power line voltage applied to an external conductive arrangement, having insulating material between the two electrodes. The harvester is depicted in Figure 7.1.

The inner electrode was chosen as a Copper tube with an outer diameter of 1/2 inch (12.7 mm). The Copper (Cu) tube was then inserted in a Polypropylene (PP) rod with a diameter of 30 mm, which was used as the insulating medium between the inner and outer electrodes. The PP rod was bored to fit the Cu tube within precisely. In order to meet the total length of the structure (300 mm), the bored rod was built in two pieces. The outer electrode was built as a 0.2mm-thickness Aluminium (Al) sheath wrapped around the plastic rod. Some steps of the construction process are shown in Figure 7.1a.



(a) Construction.



(b) Final experimental EFEH harvester.

Figure 7.1: Proposed insulator-based harvester.

The cylindrical structure was then inserted in a 30mm-diameter hole drilled in the centre of the epoxy insulator, in order to fit the structure in its pin cavity. The overall EFEH harvester was placed in the final experimental setup depicted in Figure 7.1b. In the experimental test, the voltage of the power line was applied to the outer electrode (*Al* foil), with the ground reference applied to an earthed metallic structure.

7.2 Pulsed-Mode Flyback Converter

This section presents details of the hardware used in the experimental system developed to investigate the operation of the Pulsed-Mode Flyback Converter for EFEH proposed in Chapter 4. First, the input AC supplies used for the validation of the experimental waveforms in the LV and MV experiments proposed in Section 4.4.2 and Section 4.5 respectively will be described. Then, the board implementing the pulsed-mode flyback converter topology will be described.

7.2.1 Input AC Supply

In the experimental sections of Chapter 4, both LV and MV experiments were used to validate the converter operation. The corresponding LV and MV EFEH AC input supplies are described first.

Low-Voltage Input AC Supply

The LV implementation that emulates the equivalent circuit of a weakly coupled EFEH divider system was realised by using the standard line-to-line grid voltage in Australia (415V, 50Hz) through a variac, and fed to an isolation transformer with a 1:1 turns ratio, in order to produce an appropriately grounded system. This AC supply feeds the LV system through a 117 pF coupling capacitor composed by a string of larger capacitors in series. This generated a maximum input current of about 15 μA, which is in the same proportion as the source voltage of the MV system discussed in the next sub section and the present LV source voltage (4.15kV/415V $\approx$ 150μA/15μA). These elements were connected as shown in Figure 7.2.

This input setup was used in the LV experimental validation of the pulsed-mode flyback converter in low-voltage mode, in Section 4.4.2.

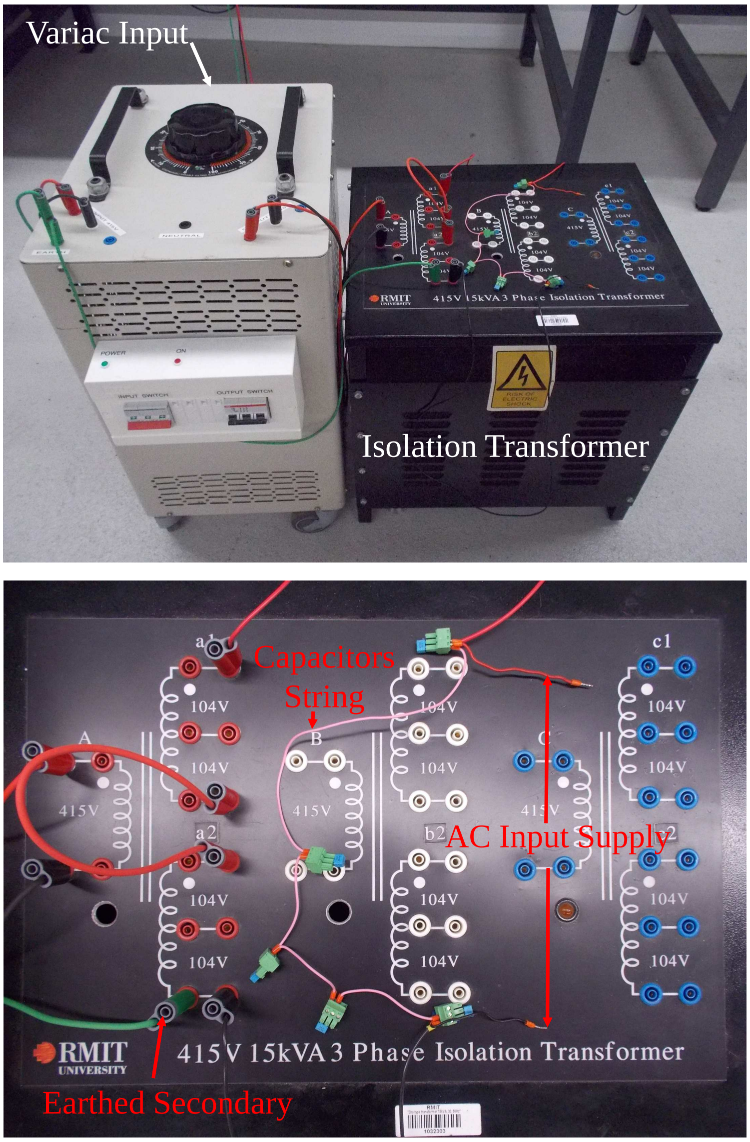


Figure 7.2: LV AC input supply arrangement.

Medium-Voltage Input AC Supply

As was noted in Section 4.5, due to practical limitations with the availability of the required 12.7 kV in the RMIT Laboratory, the EFEH capacitive divider system used for the validation of the pulsed-mode flyback converter in medium voltage was synthesised using the 4.5kV (RMS) AC supply available in the laboratory, feeding through a 100 pF HV coupling capacitor. This generated a maximum input current of 150 μA, which is the same order of magnitude as for the full line voltage system discussed in Section 3.2. Hence the proposed converter works essentially at the designed maximum input AC voltage and current levels (approximately 1kV and about 170 μA, respectively), without losing any generality in the study. The parameters of this input supply experimental setup are presented in Table 7.1.

Table 7.1: Target MV equivalent of the EFEH system.

Variable	Value	Comments
V_{line}	4.5 kV (RMS)	Available in the HV lab
ω_o	$2\pi \times 50$rad/s	Nominal line frequency
C_1	100 pF	HV capacitor available (rated for up to 100 kV)
C_{meas}	28 pF	For measurement

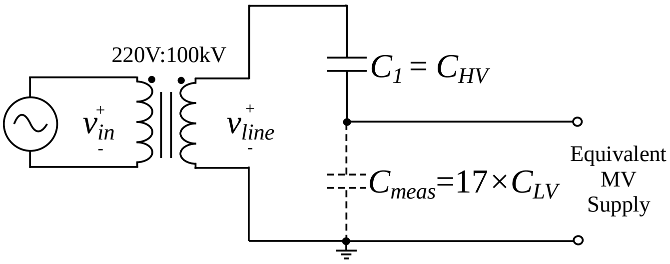


Figure 7.3: DBR MV experimental setup schematic.

The circuit in Figure 7.3 describes the physical implementation of the MV input supply system. The line-earth potential is obtained from a 50 Hz High Voltage (HV) test transformer, single-phase, with a turns ratio 220/100000 V. The transformer tap was set to achieve a line voltage $V_{line} = 4.5kV(RMS)$. Any input voltage measurements were thus obtained from the primary winding with a ratio of 1:417.

The shown capacitance divider was composed of the high-voltage (HV) capacitor $C_{HV} = 100pF$ that produces the maximum input current required to represent the EFEH system, and a string of 17 LV capacitors C_{LV} in series composing an input-volage measurement capacitor $C_{meas} = 28pF$. The extremely low value of C_{meas} does not affect the equivalent input current from this system. The HV capacitor was coupled to the LV array via coaxial cable.

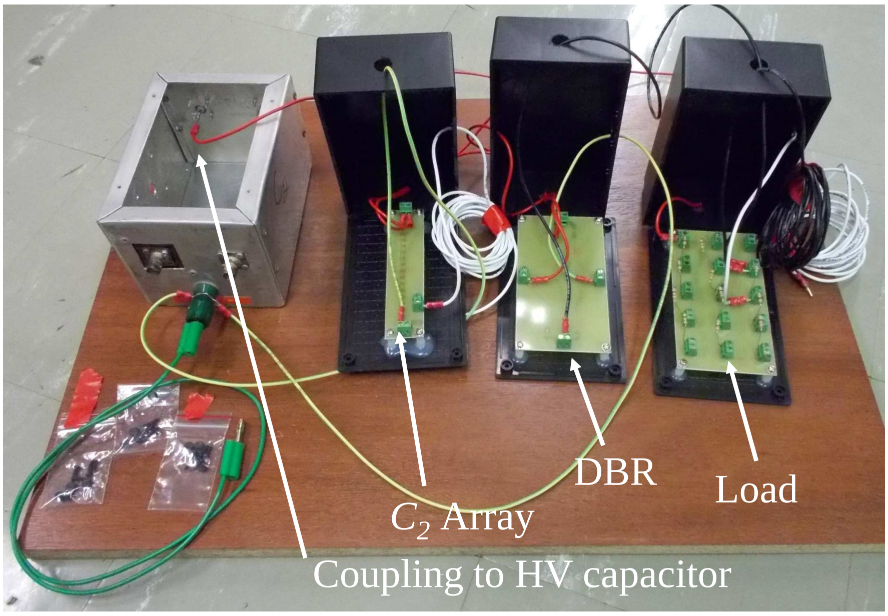
Photos of the setup with the experimental boards are shown in Figure 7.4, together with the additional boards of a DBR and some resistive loads. These boards were used to test independently several sections of the conversion system described in Section 4.3.

The required DC bus capacitances for the pulsed-mode flyback conversion system C_b were implemented with discrete film capacitors rated for high voltages of the order of kilovolts. Adequate clearance and creepage distances were considered in the design of the PCBs for the high voltage experiments.

The proposed equivalent of the EFEH system was extensively used in the MV experimental setups throughout this thesis.

(a) Input transformer

(b) HV capacitor



(c) Experiment boards

Figure 7.4: MV Experimental setup for the DBR.

7.2.2 Pulsed-Mode Flyback Converter

The two-stage converter introduced in Chapter 4 is composed of: an input DBR made of four 1600 V, 1.5 A diodes [168]; and a DC-to-DC regulation stage made of a 1700 V, 4.9 A, N-channel, enhancement MOSFET [158] which is the main switch of the system, and a flyback transformer designed for the energy transfer from the MV DC bus to the ELV DC load side.

The design of the PCB for the flyback converter topology was based on the auxiliary power supply CX48 supplied by Creative Power Technologies [169]. The original board implements a dual-flyback converter that is rated for a 3A/800V DC bus. The modifications performed on the original design to adjust it for this work are shown in Figure 7.5. From the original design, the original placement for the DBR, the bus capacitor, the DC bus voltage measurement resistors, the MOSFET (with grounded Source terminal), and the output circuit of the flyback after the secondary of the transformer (including secondary diode [166] and output RC circuit) were maintained. The benefit of using this platform is that the adequate clearance and creepage distances for 800 V are achieved by default. Additional terminals were added for interconnection with the flyback transformer and control circuitry.

The second main component in the power circuit is the flyback transformer. It was implemented in an ETD34 grade 3C90 [164] core, a turns-ratio of 46/23 with Copper enamelled wire AWG 23 for both primary and secondary windings, and an air gap of 0.02 mm. The transformer was constructed with a separate PCB and attached to the main CX48 board.

For the implementation of the pulsed-mode control strategy of the converter, a small PCB was designed and implemented. The schematic and footprint are shown in Figure 7.6. The control board is composed of the following elements:

- A linear voltage regulator TI LM78L05 [170], which takes a 9V DC input (from a standard alkaline battery) and regulates the voltage to 5 V to feed the subsequent comparator circuit.
- The fast comparator ADCMP609 [162] which takes the voltage signal from the resistive divider measurement circuit in the DC bus, and compares it against an adjustable scaled reference that corresponds to the higher threshold triggering voltage V_h. The hysteresis is provided naturally from the response time of the comparator, around 300 ns overall (obtained experimentally).
- The high-speed, low-side MOSFET gate driver FAN3122 [171]. It takes the input from the fast comparator and drives the MOSFET in the power stage

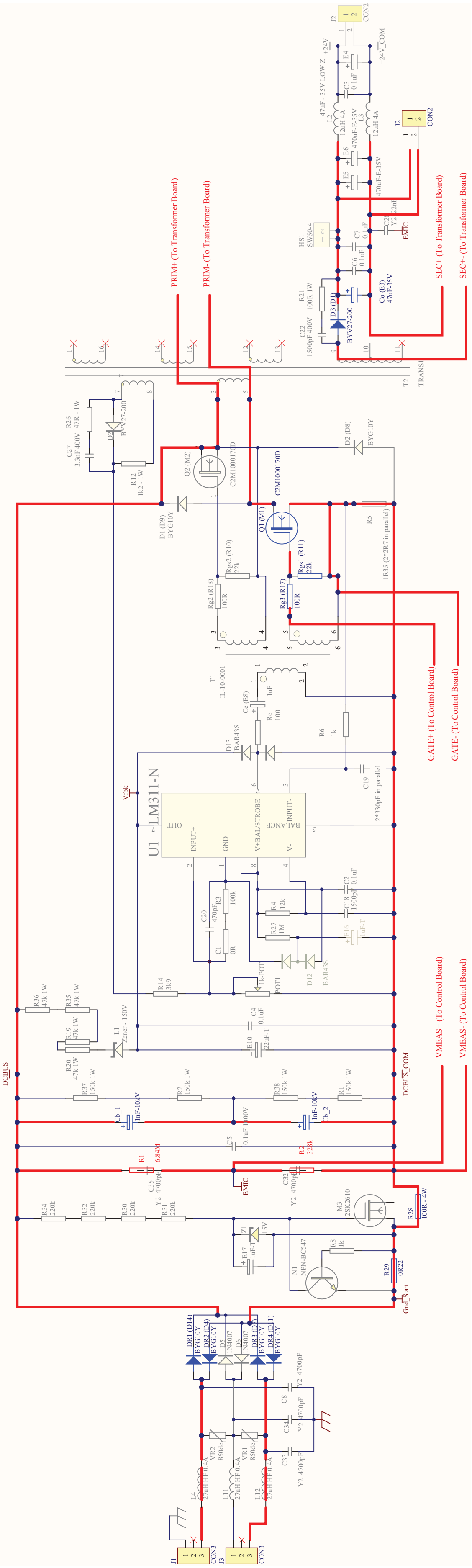
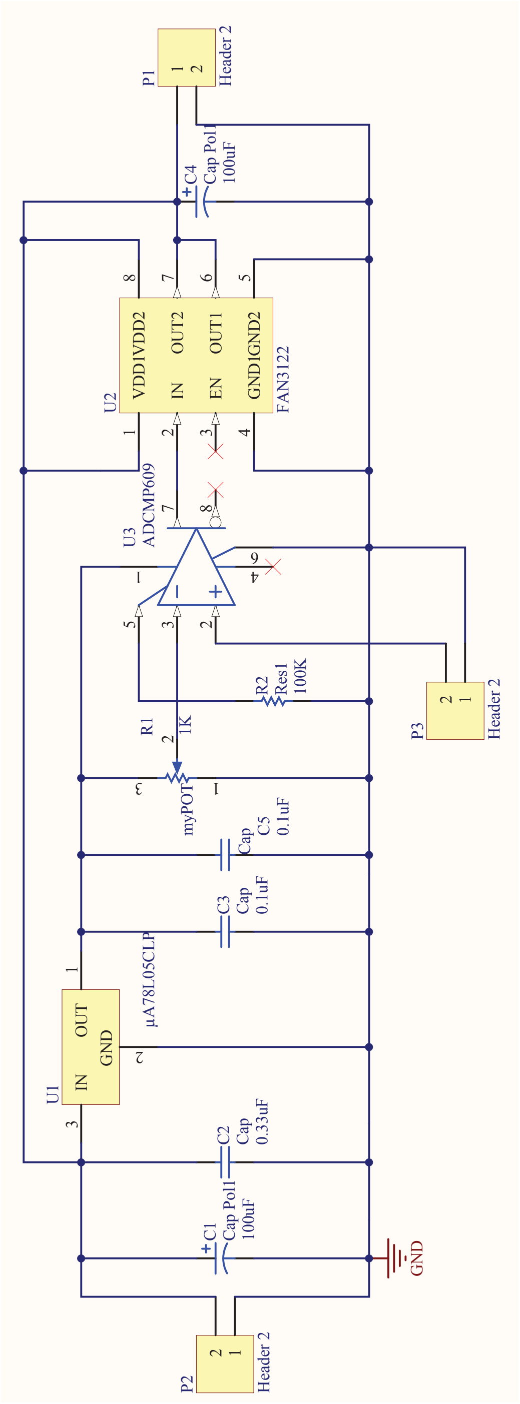
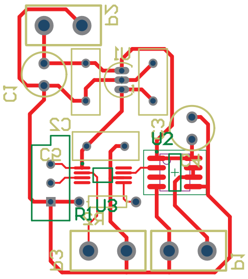


Figure 7.5: Modifications on the CPT-CX48 board to implement the flyback topology.

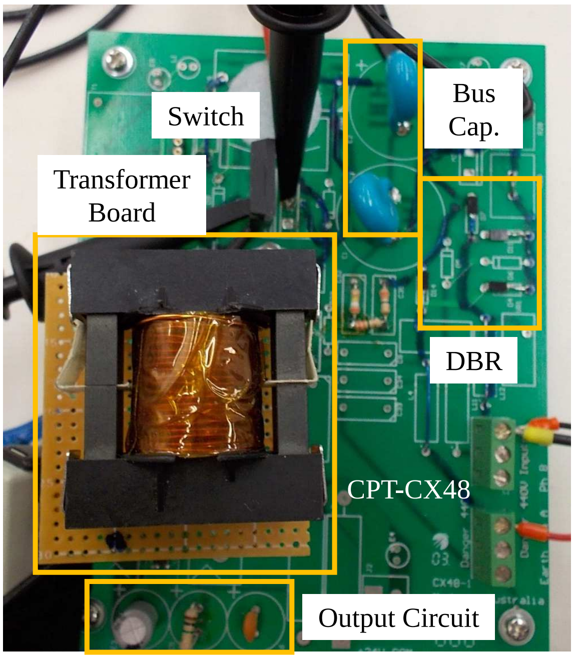


(a) Schematic

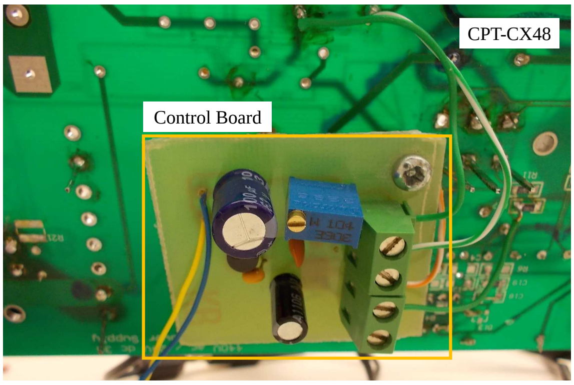


(b) Footprint

Figure 7.6: Flyback converter control board design.



(a) Power stage



(b) Control stage

Figure 7.7: Flyback converter experiment boards.

ON and OFF with respective 9 V and 0 V levels by providing high current pulses.

Photos of the boards in the full system are presented in Figure 7.7.

This experimental board was useful for a rapid and simple validation of the concept of a flyback converter system in pulsed-transfer mode as an effective methodology for the energy conversion from an EFEH supply, in Section 4.4.

7.3 Self-Triggered Flyback Converter for EFEH

This section presents details on the hardware used in the experimental system developed to investigate the operation of the Self-Triggered Pulsed-Mode Flyback

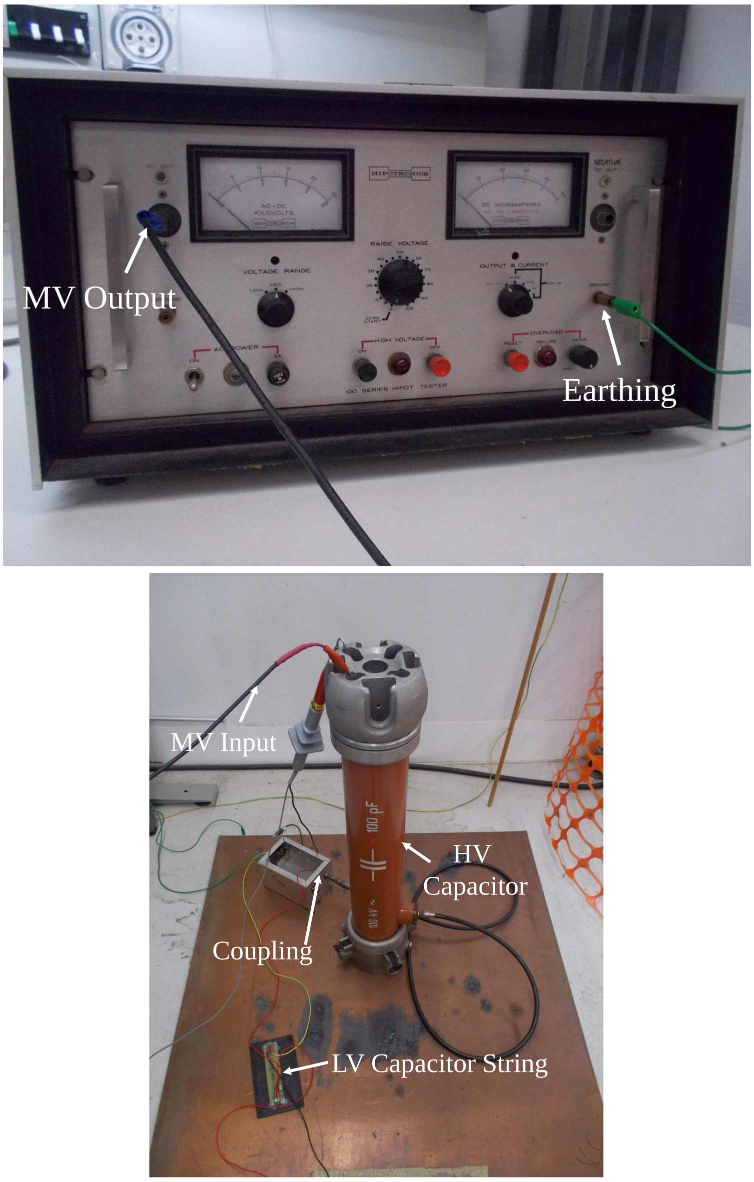


Figure 7.8: Input AC supply arrangement.

Converter for EFEH proposed in Chapter 5. The AC power supply used in the experimental investigations of Section 5.4 will be described first. Then, a complete description of the experimental board of the flyback converter will be given.

7.3.1 MV AC input supply

The experimental prototype of the self-triggered flyback converter topology proposed in Chapter 5 was tested to confirm the operation under realistic operating conditions using the MV input setup previously described in Section 7.2.1, with the difference that the 4.5 kV supply this time was taken from a HIPOTRONICS AC high voltage test set [172]. This interconnected AC supply system is shown in Figure 7.8.

7.3.2 Self-Triggered Converter Board

The two-stage conversion system introduced in Chapter 5 is composed of:

- An input DBR based on BG10Y diodes [168] to rectify the input AC supply into a flyback converter made of:
- The C2M1000170D SiC MOSFET [158] as the main switch of the system
- A MOSFET-triggering circuit composed of 32 SMDB3 LV-DIACs, with an individual breakover voltage of 36 V [173], for an overall breakover voltage of up to 1.14 kV in practice.
- The coupled inductor (flyback converter) for the implementation of the flyback topology, with the low-power circuit connected to its secondary winding.

In this work, the design of the coupled inductor of the conversion system is somewhat unconventional compared to a conventional flyback converter. Firstly, the magnetic core has to be selected as a choice between the minimum core size required to store the energy transferred in each energy transfer pulse without core saturation, and a larger core size that could accommodate more primary turns to increase the magnetising inductance L_m, and thus reduce the MOSFET conduction losses as identified in Section 5.3.2.

Consideration also needs to be given to the insulating capability of the selected core, recognising that the primary winding must withstand nearly 1kV until the diac string triggers. Taking these factors into account, an RM12 ferrite core was selected for the coupled inductor.

Next, the turns ratio a was selected as a balance between the required reverse blocking voltage of the secondary rectifying diode, and the peak current flowing through this diode as the flyback period commences. Consideration also needed to be given to the reverse bias junction capacitance of the secondary diode, since this capacitance reduces the converter efficiency because it reflects back through the coupled inductor to the primary side during the energy charging interval t_{ON}, as discussed in Chapter 5.

The secondary diode selected was a MURS480ET3G [163], because of its (relatively) low forward voltage drop and low reverse bias junction capacitance. Since this diode has a 400V reverse blocking voltage, the turns ratio was then set to $a = 4.47$. This limits the reverse voltage that the diode has to block to less than 200V, which is a comfortable margin compared to its rating.

Finally, the coupled inductor windings were wound using as thin a wire as possible (particularly for the primary winding), to fully fill the bobbin window and thus achieve the maximum possible primary inductance. The windings were arranged in a sandwich configuration using a standard U winding technique, to reduce proximity and leakage inductance effects [157].

To identify experimentally the best possible power transfer conditions, different combinations of V_{bo} and C_b were evaluated in Section 5.4. V_{bo} was adjusted by setting a link on the PCB, to choose between the four series strings of eight DIACs each forming the complete string of 32 DIACs linked to the Drain terminal of the main switch. The groups of DIACs are selectable via 4 taps that are linked to the transformers primary via a jumper in a discrete selector made up of 2 parallel strings of pin-headers. This allowed the response of the four triggering voltages of $V_{bo} =$ [292, 584, 860, 1140]V to be evaluated. A header across the DC bus is included for connection and testing of different bus capacitors C_b.

The lower side of the string of DIACs is connected to the gate of the MOSFET, in parallel with a 24V MMSZ4709T1G Zener diode [174] to keep the gate voltage below its maximum rating of 25 V. A resistor between the Gate-Source terminals is included for the discharge of the gate after the device is turned-off.

A more detailed description of the sequential steps taken for the design of the self-triggered flyback conversion system can be found in Appendix A.

The design parameters for the coupled inductor and values of the other major system components are listed in Table 7.2. The schematic and footprints of the board, implemented in ALTIUM [166], are presented in Figure 7.9 and Figure 7.10 respectively. Adequate clearance and creepage distances were considered in the design for up to 2000 V in the high voltage side. Testing points and measurement resistors are included in the design. Finally, photos of the boards are presented in Figure 7.11.

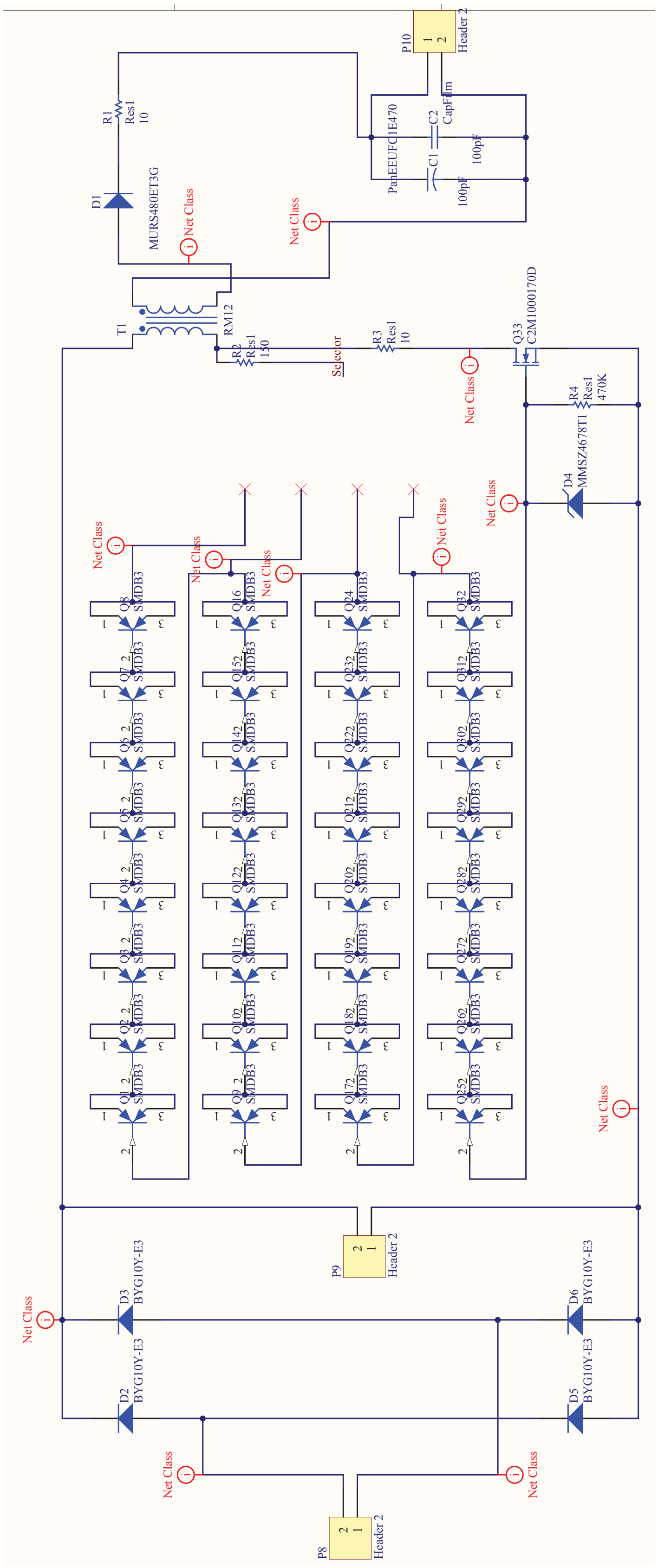
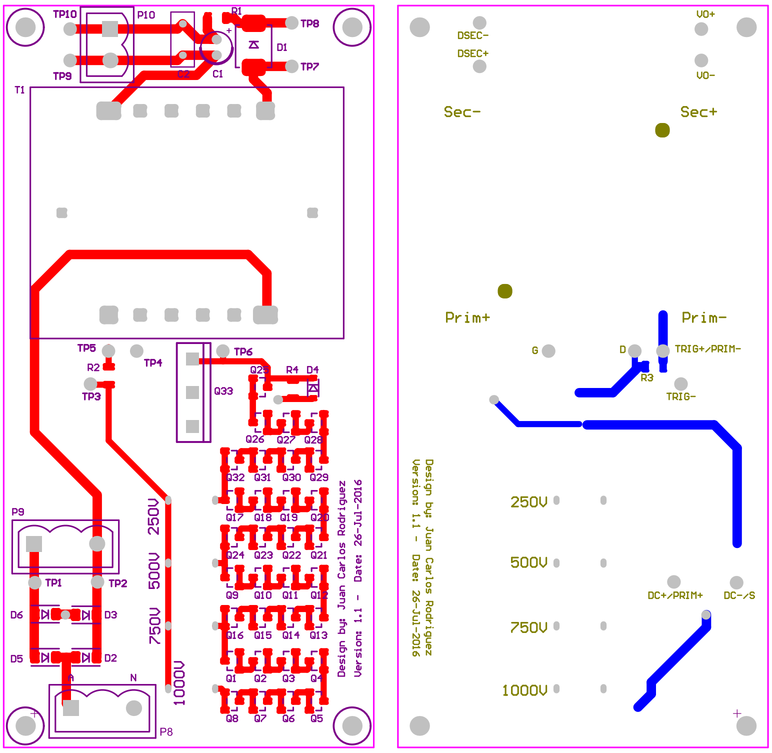
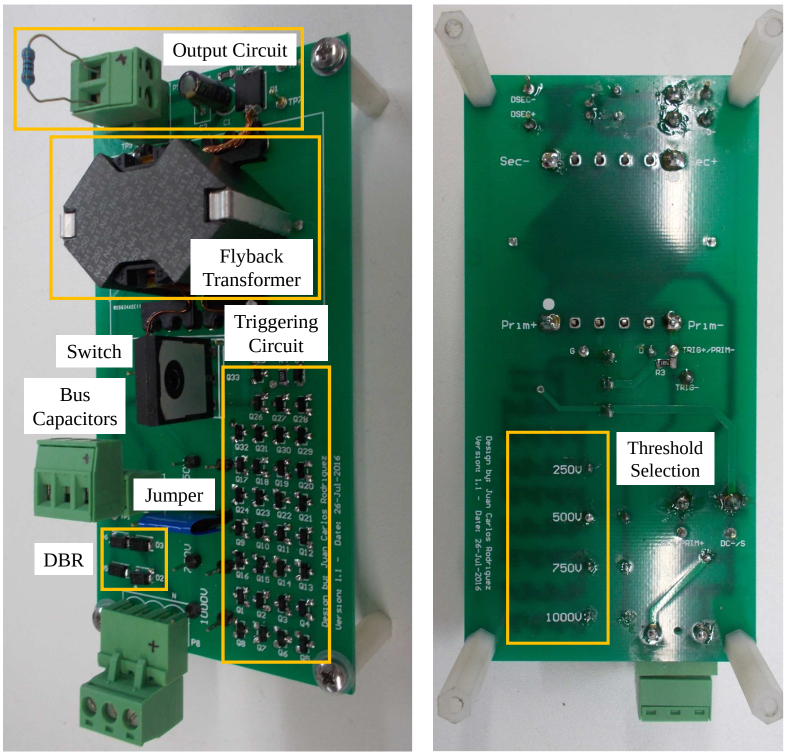


Figure 7.9: EFEH Self-triggered flyback converter schematic.



(a) Top layer (b) Bottom layer

Figure 7.10: EFEH Self-triggered flyback converter footprints.



(a) Top layer (b) Bottom layer

Figure 7.11: EFEH Self-triggered flyback converter photographs.

Table 7.2: Self-triggered flyback converter parameters

Element	Parameter	Value
Flyback transformer		
Turns-ratio	a	4.47
Number of primary turns	N_1	148
Magnetising inductance	L_m	5.5mH
Inter-winding capacitance	C_{tx}	30.7pF
Core/Material		RM12/N41
Primary/Secondary winding diam.	d_{prim}/d_{sec}	0.25/1.15 mm
DBR Diodes		BYG10Y
OFF Capacitance	C_d	2 pF
MOSFET (nominal)		C2M1000170D
Drain-Source capacitance	C_{ds}	50pF
Gate-Source Capacitance	C_{gs}	170pF
Protection Zener diode voltage	V_Z	25V
Gate-Source resistor	R_{gs}	500 kΩ
Secondary diode		MURS480ET3G
Forward voltage	$V_{Dsec,fw}$	1V
DIACs (each)		SMDB3
Individual breakover	V_{bo_i}	32V
Designed lead resistance	R_{diac}	470Ω
Output Circuit		
Output capacitor	C_o	5.6mF
Tested output load	R_o	820Ω

7.4 Summary

This chapter has provided details of the experimental systems used to validate the work presented in this thesis.

The experimental setup to test the coupling of an insulator-based EFEH strategy includes electrodes of different geometries that went through a metallisation process.

The experimental system for testing the proposed concept of a flyback converter in pulsed-mode for EFEH includes a power stage based on an altered CPT-CX48 board. The control of the board is based on a small board with fast comparator and gate-drive circuitry.

The realisation of the fully customised prototype of the flyback converter in pulsed mode with self-triggering integrates the flyback converter power stage with a control system that triggers the main switch based on a string of DIACs with different taps for selecting the triggering voltage level.

Chapter 8

CONCLUSIONS

Electric Field Energy Harvesting (EFEH) from medium voltage power lines is an emerging smart grid technology that aims at energizing low-power sensor nodes from the electric fields in the vicinity of such lines. The development of this technology will contribute to the improvement of the present day electricity grid by allowing the implementation of distribution power line sensor networks (DPLSN). DPLSN in turn will enable distribution automation (DA) operations that are becoming essential, in a grid with an increasing integration of renewable resources. Consequently EFEH has started to be the focus of significant research effort in recent years.

The challenge with EFEH systems is to extract useful amounts of energy while avoiding close proximity to (or even galvanic contact with) the power line. Since the input supply in a non-contact EFEH system is weakly coupled to the load, a thorough foundation in understanding of the loading conditions is required to implement optimal power transfer. The operation of the energy conversion stage is vital in realising the conditions that allow maximum energy transfer.

Knowledge and understanding from EFEH input supply conditions has been applied in this thesis to the energy conversion system, specifically with the aim of determining the limiting factors in the switching strategies to be used. In addition, optimal conversion strategies for non-contact EFEH have been studied.

The work carried out in this thesis provides substantial contributions to the field of EFEH. The contributions are summarised in the following sections, including both the use of a power-line insulator based strategy for non-contact EFEH and the development of an energy conversion technique for optimal power harvesting. There is scope to extend the switching converter principle to apply this knowledge to other grid and conversion technologies. This chapter also provides such suggestions for future work.

8.1 Summary of Research

8.1.1 Maximum Electric Field Energy Harvesting using Power Line Insulators

This thesis has demonstrated the use of power line insulators to bypass the limitation of having EFEH systems with galvanic contact to the power line. This direct contact between the conversion system and the MV power line is often used in the literature of wireless sensor nodes (WSN) that are powered by EFEH. This creates a limitation in the implementation of DPLSN as it restricts a large-scale deployment of sensor nodes, by making the power supply system bulky and expensive.

A pin-type power line insulator was proposed as the medium to create an EFEH capacitive divider between the power line, the insulating material, an electrode inside the power line insulator and the earthed pin, which is the ground reference of the system. The parameters of this coupling were estimated using Finite Element Analysis (FEA) simulations, for different electrode shapes. The estimated values of the capacitive voltage divider in the system were validated using an experimental setup in which the effects of measurement in the high impedance system, which make the investigation of an EFEH system challenging, were identified.

A novel study of the fundamental conditions for the optimisation of the power obtained from this EFEH system has been presented. Theoretical analysis identified that the nature of an EFEH supply is that of an AC current source. The line voltage is essentially coupled to the load by a series capacitance (in the picofarad range). Hence, while the AC load voltage (in the kilovolt range) is variable while the AC current is of a nearly constant amplitude (in the microamperes range). The power harvested from this EFEH input (in the milliwatts range) depends strongly on the load presented to the capacitive divider. Analytical and simulation studies demonstrated that for maximum power transfer, the load has to be seen by the EFEH supply as an ideal resistance of a large impedance, in the range of the series input impedance, while keeping as high a peak load voltage as is practical. The conditions for maximum power transfer from an EFEH input are then determined by the front end converter in the conversion scheme.

Furthermore, the methodology that was used for the investigation of this particular EFEH harvester can be used for the assessment of any EFEH harvesting strategy, particularly for a clear identification of the maximum theoretical energy available.

8.1.2 Pulsed-Mode Flyback Conversion for Electric Field Energy Harvesting

The feasibility of the implementation of a practical conversion system for EFEH that is able to keep the proposed conditions for optimal power transfer was studied. It was demonstrated that any form of primary high-frequency conversion, given the input constraints of EFEH, is impractical. This is mainly because semiconductor devices with ratings that meet the high input voltage requirement have parasitic capacitances that lead to extended phase leg commutation times, degrading the switching performance. It was determined that a more traditional conversion scheme using a passive front end AC-to-DC converter switching at line-frequency (i.e. a diode bridge rectifier) is a feasible strategy for EFEH. However, high-frequency continuously switched conversion for the subsequent DC-to-DC regulation required has the same limitations mentioned above.

The different conversion strategies for EFEH that are available from the literature often deal with these challenging input supply conditions by reducing the capacitively coupled input AC voltage to quite low voltage levels before its conversion to DC. This action, however, hinders the attainment of maximum power transfer. The use of a conversion system that switches the medium-voltage input directly has the potential of increasing the energy transfer.

This thesis then introduces a novel energy conversion strategy for EFEH systems that does not tap the input voltage. The proposed scheme is able to use a medium-voltage, low-capacitance DC bus by using a discontinuous DC-to-DC conversion strategy. First, a diode bridge rectifier is used to directly utilise a higher DC bus voltage than proposed in previous strategies found in the literature. A subsequent DC-to-DC conversion stage composed of a flyback converter operating in a non-conventional pulsed energy transfer mode is able to deliver a suitable power supply for low-power electronic devices in charge of power line monitoring.

One feature that is frequently missed from the literature in EFEH is the detail of the switching process in the conversion system. This work has presented meticulous circuit analysis of the switching waveforms that are relevant for the energy transfer process. The theory was further studied with the development of comprehensive simulation models that reflect with a good level of accuracy the various parasitic impedances that affect the behaviour of the system. Finally, experimental studies were carried out using both low-voltage and medium-voltage experimental systems to validate the switching operation via observation of the main waveforms in the real-life system, to match the simulation theoretical predictions.

The validation process confirmed the viability and success of the idea, demonstrating experimentally a conversion system that outperforms previous achieved levels of power, with a non-contact EFEH strategy. Up to 17.1 mW can be harvested from a 12.7 kV power line and an input capacitance of 40 pF. However, due to high switching losses that are inherent to the weakly coupled system, the efficiency of the conversion system is about 25%. This figure includes resistive losses associated with the measurement resistive divider that is necessary for the control of the switch.

The main limitation of the conversion system is that the triggering of the main switch in the flyback converter requires additional energy from an auxiliary power source. This limitation is consistent with other works in the literature of EFEH.

8.1.3 Self-Triggered Flyback Converter for Electric Field Energy Harvesting

A conversion strategy for non-contact EFEH with energy transfer optimisation can be realised by switching a medium-voltage DC bus that is directly rectified from the EFEH input supply, using a flyback converter working in a pulsed energy transfer mode. One limitation of the system that is common to any conversion strategy for energy harvesting is that the triggering circuit of the main switch requires additional energy. Several solutions in the literature opt for the use of batteries. This, however is a suboptimal solution that hampers the large-scale deployment of the low-power sensor nodes in DPLSNs that acquire the harvested energy.

In order to overcome this challenge, this thesis has introduced a technique for gating the main switch in the conversion system that does not require any additional auxiliary power supply for the control stage. The self-triggering circuit is based around DIACs that are able to trigger the main switch (a MOSFET) when the DC bus reaches their breakover voltage level.

An extensive analytical study of the switching system has been presented, with a focus on the effect of the operation of the DIACs in their region of negative dynamic resistance to gate the MOSFET through this low-resistance path. The knowledge of this process made it possible to understand the switching behaviour throughout the different switching intervals, as well as the loss mechanisms in the circuit.

The insight of the energy transfer mechanism in the proposed conversion scheme was applied to the design and the implementation of the prototype of a completely self-powered flyback converter working in pulsed energy transfer mode for non-contact EFEH. The successful operation of the practical system was validated in a medium-voltage experimental setup. The conversion system is able to harvest around 24 mW from a 12.7 kV power line and an input capacitance of 40 pF. The efficiency of the system is around 33%.

The results obtained in this research show clear advantages compared to other work presented in the literature of energy conversion for EFEH. A comparison of the features of this work, compared to the ones of other representative methods in the literature, is presented in Table 8.1. The highlights are that:

- Even the prototype of the conversion technique features a higher power density i.e. is able to yield more power per unit of volume. This makes it a more compact and inexpensive option, which supports the development of large-scale development of DPLSNs.
- The overall harvesting scheme attains more continuous power per available power line voltage than any other method that is not in direct contact with the power line, as well as most of the methods using direct contact with the line. The feature of avoiding galvanic contact with the power line further supports a large-scale deployment in DPLSNs.
- The presented conversion methodology features more power per input capacitance than most previous solutions, hence demonstrating one of the highest efficiencies, irrespective of the harvester topology used.
- Detailed switching waveforms has been presented in this work, which is usually missing in the literature.
- The triggering block of the main switch of the conversion strategy is completely self-powered from the harvesting supply, making the methodology independent of additional power supplies such as batteries.

Table 8.1: Various EFEH methodologies against the present work.

Study	**Harvester Volume** (m^3)	**Power Line Voltage** (kV)	**Input Capacitance** C_{th} (pF)	**Continuous Power Harvested** (mW)	**Power per Volume** ($\mu W/cm^3$)	**Power per Line Voltage** (mW/kV)	**Power per Input Capacitance** (mW/pF)	**Features**
[45, 49, 56]	3.89×10^{-2}	150	520	370	9.52	2.47	0.71	Line contact; Transformer tap; Linear pow. supply; Batteries.
[52, 59, 62]	6.47×10^{-4}	35	110	17	26.29	0.49	0.15	Line contact; Res. Divider tap; Semi-CSR conversion.
[57]	4.71×10^{-5}	0.13	80	0.057	1.21	0.45	0.00071	Non-contact; For household LV conductors.
[50, 51]	1.57×10^{-3}	110	172	17.3	11.014	0.16	0.101	Line contact; Transformer tap; Linear pow. supply; Batteries.
[63]	3.77×10^{-2}	10	215	0.66	0.018	0.066	0.0031	Non-contact; Up-conversion oscillation method with smaller magnetics.
[53]	3.14×10^{-3}	7	4	0.18	0.056	0.025	0.044	Non-contact; Switching plates in short circuit.
This Work	2.12×10^{-4}	12.7	40	23.6	111.29	1.86	0.59	Non-contact; Self-triggered; Detailed S/W waveforms.

8.2 Suggestions for Future Work

8.2.1 Peripheral Smart Grid Technologies for DPLSNs

There are many challenges associated with the topic of power line monitoring. Although having a power supply for the fundamental components of a DPLSN is vital, the research questions of the applications for DPLSNs are still open. Measurement, processing and communication technologies integrated within the wireless sensor nodes are an ongoing development from both academia and industry that can be looked at for future work. In addition, the computation needed for processing the obtained data from DPLSNs is still very complex and not very well understood. The specification of parameters of the monitoring and control functions in the data centres collecting the information from the sensor nodes is a broad area that needs attention in smart grid technologies.

8.2.2 Electric Field Energy Harvesting Coupling

The work presented in this thesis proposed a technique for EFEH that obtains its energy from a MV power line through a pin-type insulator-based harvester with an inner electrode that fits in the cavity of the pin. Although this strategy helped to provide a more compact solution for EFEH in large-scale deployed WSNs, if the volume of the harvester is not a limitation in the application then different geometries not limited to the boundaries of a line insulator can be explored that will produce even larger volumes of harvested power. By using the analytical and practical methodologies provided in this thesis, a clear idea of the available input power from each methodology can be used to explore more efficient energy transfer techniques. Additionally, the effect that peripheral impedance values has on the power transfer when the insulator-based or other EFEH strategies are mounted in the poles of distribution power lines, is a topic that requires further attention.

8.2.3 Applications to Auxiliary Power Supplies

In this work, it was determined that any form of high-frequency conversion is impractical for the objectives of Electric Field Energy Harvesting. This is because semiconductor devices with high-voltage ratings have parasitic impedances that are comparable to the ones of the input capacitive coupling of EFEH, which reduces the operational current levels and causes extended phase leg commutation times, hence degrading the switching performance. However, in applications with better coupling to the power supply i.e. with larger capacitance values of the input coupling element, the current levels can be placed in more standard values and the commutation times of the switches can be decreased back to values that allow any type of front end conversion. This could be realised for example by deliberately connecting a capacitor to an MV power line as the coupling medium. Under these circumstances, the implementation of the conditions for optimal power transfer presented in the thesis can be applied to a wider range of conversion strategies that are able to provide an auxiliary power supply for any subsequent application while maintaining galvanic insulation to the power line.

8.2.4 Self-Triggered Pulsed Mode Flyback Converter Applications

A completely self-triggered power electronic converter that is able to couple to a higher-voltage power line without requiring galvanic contact has been developed in this work. The efficiency achieved using this concept is 33%. Most of the losses in the harvesting system are related to the switching process in the most recent semiconductor devices. The continuous development of new semiconductor technologies is likely to improve this efficiency, so the exploration of new semiconductor devices within this technique is a topic that can be explored in the future. Additional switching techniques and topologies of conversion that are able to improve the efficiency of the system, are open topics for investigation too. Of particular interest is the exploration of alternative self-triggering circuits that are able to optimise the turn-on of the main switch and hence reduce its associated losses, while still avoiding the need for an additional power supply i.e. of extra-low power consumption. Finally, the presented conversion system has the important potential of being applicable to different technologies for power line maintenance and smart grid, beyond WSN powering. Some of the applications of this theory include (but are not limited to) auxiliary power supplies for larger conversion systems that require galvanic insulation from the power lines, high voltage presence detection and in-situ DC battery charging systems.

8.3 Thesis Closure

Electric field energy harvesting is an attractive strategy for powering wireless sensor nodes from communication networks in charge of operations needed for power line monitoring, in the context of the smart grid. However the close proximity with the power line and suboptimal energy transfer present a challenge for achieving large-scale deployment and the extraction of useful amounts of energy. These needs have driven substantial research into coupling techniques and optimal energy conversion design.

This thesis has presented an in depth analysis of the conditions for the realisation of an optimal strategy for electric field energy harvesting from medium voltage power lines, leading to the development of a non-contact coupling technique and power electronic conversion strategies aimed at optimising the energy transfer from the weakly coupled supply. With the conditions for optimal power transfer in place, the practical aspects of the power electronic converter were explored. The challenging supply conditions of high voltage and extremely low current were managed using a conversion strategy based on low-frequency rectification of the medium-voltage supply and pulsed-mode discontinuous flyback conversion of the rectified bus, into extra-low-voltage loads featuring low-power sensor nodes. The limitations of the technique were addressed by a self-triggering strategy that creates an autonomous conversion solution.

The control and design ideas presented in this thesis have provided a significant contribution towards the use of electric field energy harvesting from medium voltage power lines, promoting less invasive design and improved efficiency.

Appendix A

DESIGN OF A FLYBACK CONVERTER FOR EFEH

This appendix describes the steps necessary for the design of the self-triggered flyback converter that was conceived in Chapter 5 for the weakly-coupled input of an EFEH supply.

Similar to the design of a standard flyback converter-based SMPS, the central element of the design is the coupled inductor known as the flyback transformer. However, because of the challenging conditions of the supply in this application, the design process showed to be quite different than the conventional approach.

In the topic of design of magnetics for power electronic converters, there is a large amount of material in the literature. The following design has been based on the basic principles of example 4.5 (pp.130) in [157] and the theory in [175], as well as on the more up-to-date theory presented in [176].

Because the converter presented in this design is an emerging application, the design steps have been adjusted to the specific nature of the circuit under study. The schematic of the design is presented in Figure A.1. Each element in the circuit will be considered in the design steps described next.

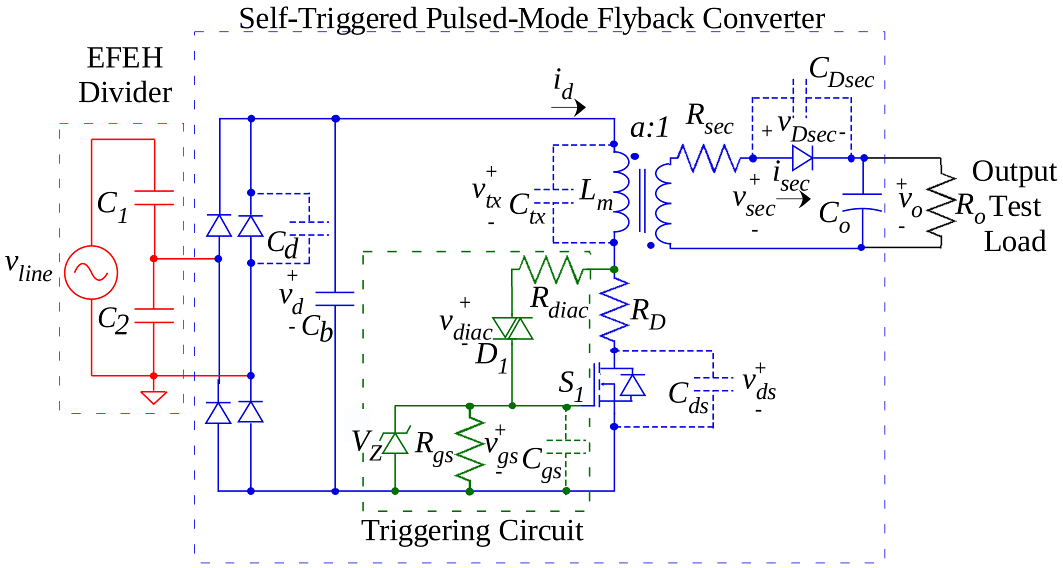


Figure A.1: EFEH Self-triggered flyback converter design circuit.

A.1 Design Requirements

In this design, the magnetic core has to be selected as a choice between the minimum core size required to store the energy transferred in each energy transfer pulse without core saturation, and a larger core size that could accommodate more primary turns to increase the magnetising inductance L_m. The use of a small core is enforced since the application of the conversion system to EFEH for power line monitoring devices requires a compact design for large-scale deployment, as was discussed in Chapter 2. On the other hand, an increased value of L_m is necessary in order to reduce the losses in the system, as investigated in Chapter 5. Additional consideration also needs to be given to the insulating capability of the selected core, recognising that the primary winding must withstand more than 1 kV until the diac string in the design of Chapter 5 triggers.

Whereas in a conventional flyback converter design the turns ratio is decided based on the ratings of the main switch, in this application the turns ratio has to reflect a balance between the required reverse blocking voltage of the secondary rectifying diode, and the peak current flowing through this diode as the flyback period commences.

In addition, special attention has to be given to the winding topology used in the design of the transformer, in order to achieve the maximum possible primary inductance in a small geometry, while at the same time reducing unwanted parasitics in the design, which have demonstrated to affect the response and efficiency of the system in Chapter 5.

A.2 Turns-Ratio and Secondary Diode

In a standard flyback converter design, the primary/secondary turns ratio is chosen first to reduce the voltage stress in the main switch during its turn-off process. In this application, however, the MOSFET does not reach a higher voltage during turn-off than it does under turn-on.

The semiconductor whose rating has to be checked, in this application, is the diode in the secondary of the flyback transformer. Over the interval t_{ON}, the maximum reverse voltage stress on the secondary diode will be $V_o + V_h/a$. Therefore, the first requirement for the turns-ratio is its reverse voltage rating to be more than this value. This translates into a requirement for the turns ratio as in (A.1).

$$V_{Dsec,rev,rating} > V_o + \frac{V_h}{a} \Leftrightarrow a > \frac{V_h}{V_{Dsec,rev,rating} - V_o} \tag{A.1}$$

During the flyback interval t_{fly}, from the *mmf* balance in the transformer it follows that the maximum output peak current in the secondary winding is $I_{sec}(max) = aI_d(max)$. From the equations in the theoretical analysis of Chapter 5, this means that $I_{sec}(max) = aV_h\sqrt{C_{ON}/L_m}$. Hence, a second requirement for the turns-ratio is the diode current rating to fulfil:

$$I_{sec,rating} > aV_h\sqrt{C_{ON}/L_m} \Leftrightarrow a < \frac{I_{sec,rating}}{V_h\sqrt{C_{ON}/L_m}} \tag{A.2}$$

The working design parameters to solve equations (A.1) and (A.2) are:

- $V_h = V_{bo}(max) = 1.14kV$, the worst case of breakover voltage.
- $V_o = V_o(max)$, the maximum expected output voltage, around 10V.
- C_{ON} is chosen by considering that the total value of the DC bus capacitance is varied in the experiments performed in Section 5.4, as different bus capacitors C_b (up to 1 nF) are tested to find the level for maximum power transfer in the range up to some nanofarads. Hence, 1 nF is chosen for C_{ON} as the worst-case-scenario value.
- L_m is chosen as 5.5 mH, as the maximum value that makes the conductors fit in the selected core, given the considerations presented in Section A.3 and Section A.4.

Table A.1: Options for the secondary diode specification.

Devices	**VS-30EPH06PbF**	**MURS480ET3G**	**6A05G**
Reverse Voltage Rating	600V(pk)	800V(pk)	600V(pk)
Capacitance			
Nominal	33pF@600V	8pF@200V	60pF@4V
In the Application	33pF@768V	8pF@768V	15pF@768V
Current Rating	30A(avg)	4A(avg)	6A(avg)
Forward Voltage			
Nominal	2V@30A	1.75V@3A	1V@6A
In the Application	1V@1A	0.97V@1A	0.85V@1A
Max. Reverse Recovery Time	77ns@30A(fw), 200V(rev)	100ns@1A(fw)	-
Reverse Current	1μA@700V(rev)	1μA@730V(rev)	0.6μA@700V(rev)

Given that the number of turns depends on the ratings of the chosen secondary diode too, it is preferable to specify this device now.

The loss analysis of the system in Chapter 5 indicated that in order to reduce the loss of energy in the secondary diode, its forward voltage at turn-on has to be minimised. Furthermore, its parasitic capacitance at turn-off should be kept small, to also reduce its losses.

A survey of the most viable, commercially available options for this device is summarised in Table A.1. It was clear from this survey that higher voltage diodes have less parasitic capacitance. The ultra-fast diode MURS480ET3G [163] was then chosen for its low forward voltage feature. Devices with even less forward voltage are usually rated for lower voltage, but this limits the range for the number of turns. Another reason for the selection is its higher-voltage rating, which provides a wider range of selection for the number of turns, as inferred from equations (A.1) and (A.2). Using the parameters of the selected semiconductor in Table A.1 the requirement for the number of turns is:

$$1.3 < a < 7.7 \tag{A.3}$$

While a larger a will reduce switching losses, if it is too large it will produce a larger current in the secondary, which will increase resistive losses. The target number of turns is therefore, the mean value of the range.

$$a = 5 \tag{A.4}$$

A.3 Core Selection

In general terms, the choice of the core within the context of magnetics design is based on the principle of minimising its losses by means of minimising the peak magnetic flux density excursion, in order to avoid saturation of the $B - H$ curve of the chosen magnetic material.

In switched mode power supply theory, the strategies to follow this action are the use of either magnetic powder cores, which naturally have a distributed gap, or ferrite cores with an added gap. The effect of such choices are to tilt the slope of the hysteresis loop such that is more difficult to saturate the core with larger ampere-turn excursions. In addition, it is considered that cores of smaller sizes are more difficult to saturate, since smaller cores can generally operate at a higher flux density [157].

Some of the smallest ferrite cores whose application is switched-mode power supplies are RM-type cores. RM cores represent a compromise between pot and EE cores. While the advantage of using a pot core is that the coil on the bobbin around the centre post is almost entirely enclosed by ferrite material hence minimizing EMI problems, the major disadvantage is the narrow slot in the ferrite through which the coil leads exit. This makes it difficult to use in multi-output supplies with many wires exiting. It also makes it a poor choice for a high-voltage supply, even at low power, where leads carrying a high voltage may arc because of the close spacing in the narrow exit notch in the ferrite [175]. An RM core is a pot core with a much wider notch cut out of the ferrite. It is thus easier to bring larger diameter or many wires in and out of the coil, so this core is usable for multi-output transformers and may increase its reliability with high-voltage supplies.

An RM type core is then chosen for this application. Some commercially available options for this choice are presented in Table A.2, where their main features of each core are listed.

Table A.2: Options for the core selection.

Type	**Material**	A_L $(H/turn)$	**Size** (mm)	A_c (m^2)	A_w (m^2)	A_p (m^4)	B_{sat} (mT)	$A_{p,req}$ (m^4)	B_{max} (T)
RM6-Ungapped	N87	2.4×10^{-6}	17.9×14.7×12.5×	3.1×10^{-5}	1.5×10^{-5}	4.65×10^{-10}	256	5.41×10^{-9}	2.11
RM8-Ungapped	N87	3.3×10^{-6}	23.2×19.7×16.5×	5.5×10^{-5}	3×10^{-5}	1.65×10^{-9}	256	5.41×10^{-9}	1.39
RM10-Ungapped	N87	4.2×10^{-6}	28.5×24.7×18.7×	9×10^{-5}	4.15×10^{-5}	3.74×10^{-9}	256	5.41×10^{-9}	3.04
RM12-Gapped-0.7mm	N41	2.5×10^{-7}	37.6×29.8×24.6×	1.25×10^{-4}	7.2×10^{-5}	9×10^{-9}	210	6.59×10^{-9}	0.169
RM14-Gapped-1.9mm	N41	1.6×10^{-7}	42.2×34.8×30.2×	1×10^{-4}	1.06×10^{-4}	1.8×10^{-8}	210	6.59×10^{-9}	0.0993

The selection of the material and size of the ferrite core based on the Area Product method is studied next.

A.3.1 Selection using the Area Product Concept

The Area Product method is regarded as a powerful tool in magnetic design, based on the fact that the area product figure of merit has been shown to be a good indicator of the power rating of the core [157]. The Area Product A_p of a magnetic core is defined in (A.5).

$$A_p = W_a A_c \tag{A.5}$$

where W_a is the total window area destined for windings of the bobbin, and A_c is the effective cross-area of the ferrite core. This equation can be expanded by considering:

- The definition of the window utilization factor

  $$K_u = N A_w / W_a \tag{A.6}$$

  which is the ratio of the total conductor cross-sectional area (equal to the total number of turns $N = N_1 + N_2$, times the cross-sectional area of the winding wire A_w) to the window area W_a.

- The definition of the current density in the conductors is

  $$J = I/A_w \tag{A.7}$$

  which can be particularly defined at the point of maximum primary current as

  $$J(max) = I_d(max)/A_w \tag{A.8}$$

- Following the theory developed in [177] the cross-section area is related to the maximum current and flux density according to:

  $$A_c = \frac{L_m I_d(max)}{N_1 B(max)} \tag{A.9}$$

Using the previous considerations, the Area Product is expanded to

$$A_p = \frac{NA_w}{K_u}\frac{L_m I_d(max)}{N_1 B(max)} \tag{A.10}$$

The left-hand side of (A.10) contains the mechanical core parameters (related to the current conduction capability), while the right-hand side of the expressions includes the inductor electrical parameters (related to the magnetic flux conduction capability). This is what makes the area product a good indicator of the power capability of a specific core for any application.

Now, considering the definition of the current density, (A.10) reduces to (A.11).

$$A_p = \frac{2W_m}{K_u J(max) B(max)}\left(1 + \frac{1}{a}\right) \tag{A.11}$$

where $W_m = (1/2)L_m I_d(max)^2$ is the maximum energy stored in the inductor.

The calculation of the required area product for the present application uses values of the parameters in (A.11) according to the following considerations:

- The energy W_m is the maximum energy handled by the circuit in one pulse, hence

  $$W_m = E_d = \frac{1}{2}C_{ON}V_h^2 \tag{A.12}$$

  For the design at the worst case scenario, the parameters in (A.12) are adjusted to the maximum possible values, taken from Chapter 5, and yield $W_m = 891$ μJ.

- In the literature, the window utilisation factor is usually recommended to be maximum 0.4 for flyback converter designs. Given that this application has a high primary voltage, there is an insulation requirement to be addressed. Under this condition, the recommended value of K_u=0.235 selected under approximately similar insulation condition in [176] will be used.

- A conservative practice in transformer design is to operate the windings at current-densities up to 1/300 amperes (RMS) per circular mils, while greater inverse-densities are avoided to avoid excessive copper losses and temperature rise [157, 175]. The maximum inverse-current-density is therefore chosen as 1/300 A (RMS)/cmils for this design, i.e. $J(max)$=6.58 A/mm^2.

- The maximum possible flux density excursion depends on the material of the ferrite. The two materials under consideration in Table A.2, N87 and N41

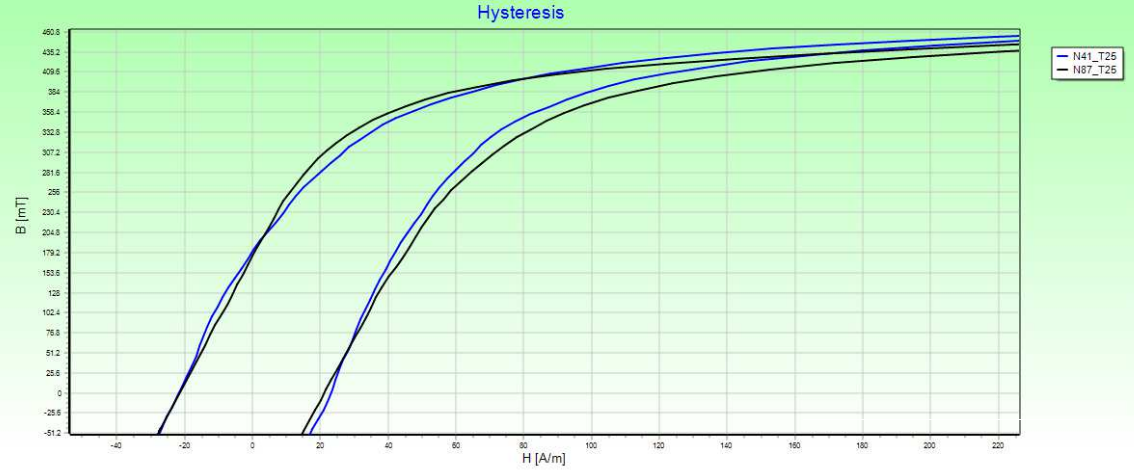


Figure A.2: Hysteresis curves of EPCOS materials N41 an N87 (using [178]).

have been compared using the design software provided by the manufacturer, EPCOS. This is the *Magnetic Design Tool* v.5.1.5851.28384 [178]. The first quadrant of the hysteresis curves of both materials at 25°C are presented in Figure A.2.

Following the principle of avoiding reaching the saturation region on the hysteresis curve, the maximum flux densities when the $B-H$ relationships stop being linear is 210 mT for material N41 and 256 mT for material N87. Such maximum values are included in Table A.2 as the parameter B_{sat}.

- The number of turns specified in the previous section a=5 will be used.

The minimum required area product for each material within the conditions of this application are listed in the column $A_{p,req}$ of Table A.2. From there, the cores whose area product A_p fulfils the required $A_{p,req}$ are the RM12 and the RM14 cores. To complete the core selection the maximum flux density before saturation is considered next.

A.3.2 Maximum Flux Density

Magnetic hysteresis is the lead mechanism for the losses in the core of the flyback transformer in this application, which is associated with the gradient of the magnetic flux density ΔB, that in turn is dependent on the (emf) developed across the primary of the transformer v_{tx} during the energy transfer interval, as was explored in Chapter 4.

The selection of the core has to take into account the fact that the switching process does not bring it to its saturation region through an excessive value of the maximum magnetic flux density swing ΔB. This requirement will be explored now.

In practice, the inductance of a ferrite core is determined by the inductance factor A_L, usually given by manufacturers as shown in Table A.2. Using this parameter, the primary inductance is defined as

$$L_m = A_L N_1^2 \tag{A.13}$$

On the other hand, the instantaneous magnetic flux density $B(t)$ can be defined using Faradays law of induction as a piecewise expression of the electromotive force (emf) developed across the primary of the transformer v_{tx}, throughout the intervals discussed in Section 5.2 of Chapter 5, with

$$B(t) = \left(\frac{1}{N_1 A_c}\right) \int_0^t v_{tx}(t) dt \tag{A.14}$$

where N_1 is the number of turns in the primary of the transformer and A_c is the effective core area. The integral can be solved by defining $v_{tx}(t)$ for each switching interval, however t_{ON} was shown to be the main contributor to the magnetic flux density swing. As it was determined in Section 5.2 during t_{ON}, v_{tx} is approximately equal to the decaying bus voltage v_d, i.e.

$$v_{tx}(t) \approx V_h \cos\left(\frac{t}{\sqrt{L_m C_{ON}}}\right), t \in t_{ON} \tag{A.15}$$

Hence, applying (A.14), the approximate magnetic flux density during t_{ON} is given by

$$B(t) \approx \left(\frac{1}{N_1 A_c}\right) \sqrt{L_m C_{ON}} \sin\left(\frac{t}{\sqrt{L_m C_{ON}}}\right), t_{ON} \tag{A.16}$$

and the maximum value it reaches is

$$\Delta B \approx \frac{\sqrt{L_m C_{ON}} V_h}{N_1 A_c} \tag{A.17}$$

Now, by replacing (A.13) into the expression for the magnetic flux density swing ΔB defined in (A.17), it can be seen that the peak magnetic flux density swing in this application is dependent directly on the A_L factor rather than on the exact number of turns, i.e.

$$\Delta B \approx \frac{V_h \sqrt{A_L C_{ON}}}{A_c} \tag{A.18}$$

Table A.3: Selected core parameters: RM14/N41 gapped, no centre hole.

Parameter	Value	Units	Description
FERRITE			
Type	RM12		Gapped, no centre hole
Material	N41		
$\Sigma l/A$	3.9×10^{-4}	m^{-1}	Magnetic form factor
l_e	0.057	m	Effective magnetic path length
A_e	1.46×10^{-4}	m^2	Effective magnetic cross section
A_{min}	1.25×10^{-4}	m^2	Minimum core cross section
Vol_e	8.32×10^{-6}	m^3	Effective magnetic volume
m	0.045	Kg	Weight per set
A_L	2.5×10^{-7}	H/turn^2	Inductor factor, ±3% tolerance
s	7×10^{-4}	m	Total air gap
μ_e	78		Relative effective permeability
BOBBIN			
Insulation	IEC 60085		
A_N	7.2×10^{-5}	m^2	Winding cross section
l_N	0.061	m	Average length of turn
A_R	2.87×10^{-5}	Ω	Resistance factor, $A_R = R_{Cu}/N^2$
Dimensions	33.02×25.4	mm	
A_p	1.0512×10^{-8}	m^4	Area product (calculated)

Using the same design conditions in Section A.3 (the worst case scenario of this application), the maximum flux density that will occur in each core is listed in the column labelled B_{max} in Table A.2. This maximum value is compared with the previously defined maximum saturation levels before the non-linear region of the hysteresis curve B_{sat}, for the respective material of each core in Table A.2.

The smallest core that simultaneously fulfils the requirements of area-product power capability and maximum flux density is the gapped RM12 core of material N41, with an air gap of 0.7 mm, which is the one with the largest A_L factor of the options left. Hence it will yield more inductance for the same number of turns than the other alternatives. The parameters of the chosen core are summarized in Table A.3, and they will be used for the rest of the design steps.

A.4 Number of Turns

For a given core with an inductance factor A_L, the required number of the primary winding turns to achieve the desired inductance L_m can be calculated from (A.13) as

$$N_1 = \sqrt{L_m/A_L} \tag{A.19}$$

Following the design requirement of as larger a magnetising inductance L_m as possible, eqn.(A.19) indicates that a larger number of primary turns will yield a larger inductance, depending also on the inductance factor A_L. For the selected turns-ratio in (A.4) and the parameters of the selected core in Table A.3, taking into account the utilisation factor described in Section A.3.1, an iterative process showed that in the selected core it is possible to fit as many turns as

$$N_1 = 248 \tag{A.20a}$$

$$N_2 = 28 \tag{A.20b}$$

The adjusted turns-ratio is then a=5.28, and this yields a magnetising inductance of L_m=5.48 mH, which will set an energy transfer interval of about $t_{ON} \approx 3\mu s$. The next step is the selection of the size of the conductors.

A.5 Size of Conductors

The main criterion for the selection of the size of the conductors is the definition of the current density J_w as the RMS current per unit of area A_w in the conductors of both primary and secondary windings:

$$J_w = I(RMS)/A_w \tag{A.21}$$

A standard practice is to operate at current-densities of maximum 1/300 RMS amperes per circular mils to avoid excessive copper losses and temperature rise [157]. Furthermore, it has been identified that the optimum distribution of current in the available area is to have the same current density in each winding, which leads to minimum power losses [176].

In this design, both primary and secondary windings will be operated at the same current density, which will not be greater than $J_w(max)$=1/300 A(RMS)/cmil (this is 6.58 A/mm^2).

From the equations derived in the analytical study in Chapter 5, the current through the primary winding can be approximated as a sinusoid during t_{ON} and zero elsewhere, with an RMS value of

$$I_{prim}(RMS) \approx \frac{V_h}{2}\sqrt{\frac{\pi {C_{ON}}^{3/2}}{T_s {L_m}^{1/2}}} \tag{A.22}$$

where T_s is the period of each energy-transfer burst. For one pulse, this is simply $T_s = T_o/2 = 10$ ms.

On the other hand, the current through the secondary can be described with the more conventional triangular approximation during t_{fly}, and zero elsewhere. Hence, its RMS value is given by

$$I_{sec}(RMS) \approx \sqrt{\frac{a{V_h}^3 {C_{ON}}^{3/2} {L_m}^{1/2}}{3V_o T_s}} \tag{A.23}$$

The areas of the conductors of respectively the primary and secondary windings, are developed by substituting the RMS primary and secondary currents in equations (A.22) and (A.23), into the current density equation in (A.21).

The values replaced in the parameters of these equations are chosen based on the following considerations:

- The values of V_h and C_{ON} are the same for the design at the worst case scenario in Section A.1.
- The current density J_w is never higher than 1/300 A(RMS)/cmils (3.947 A/mm^2). Different values lower than this limit were tested so that the largest possible areas of the conductors are achieved, within the requirement that the utilisation factor K_u is kept high enough so that the area product requirement in (A.11) does not exceed the rating of the core in Table A.2. This requirement is numerically $A_p = W_a A_c$ =2.12×10^{-8} m^4.

From the different trials, it was decided that the application is to operate with a current density of 1/11083 A (RMS)/cmil (0.1784 A/mm^2) in each winding. This yields an area product requirement of 4.55×10^{-9} m^4. This leads to conductor areas of A_{prim}=0.05 mm^2 and A_{sec}=1.04 mm^2 respectively.

Therefore, conductors of diameters: d_{prim}=0.25 mm and d_{sec}=1.15 mm respectively are required. The primary conductor, being very thin, is chosen as a single copper wire. The secondary is chosen as Litz wire to reduce any skin-effect-related loss mechanism.

Once the conductors have been chosen, the winding strategy is to be determined.

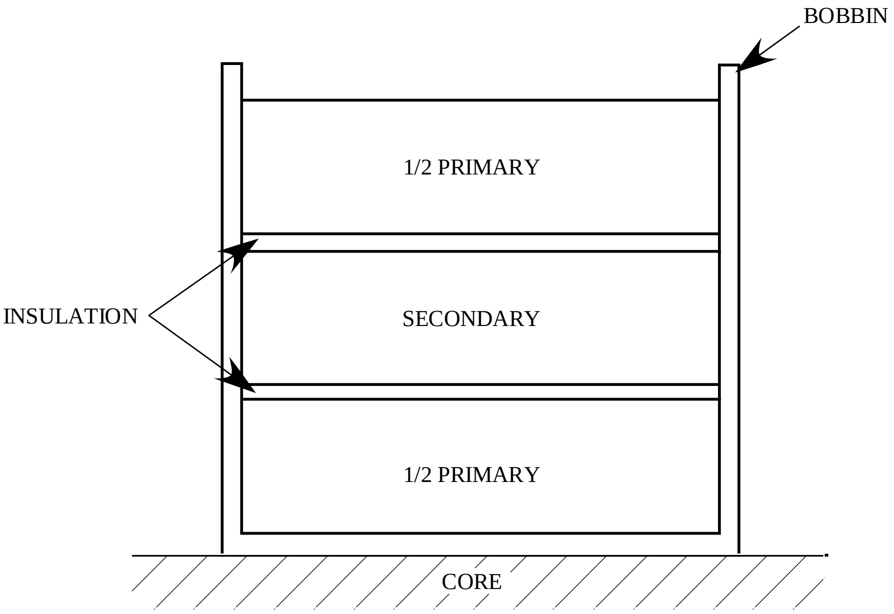


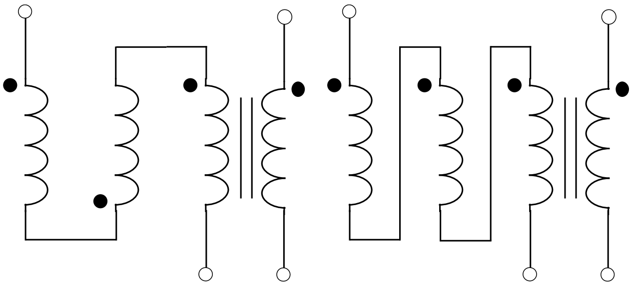
Figure A.3: Example of sandwiched winding topology.

A.6 Winding Topology

In a power electronics magnetic design, the physical spacing of the windings determine the parasitic leakage inductances and winding capacitances.

The winding capacitance appears due to the turns and how they are placed throughout the transformer. The net effect of the capacitance is what has been normally called C_{tx} throughout this thesis. In general, this capacitance can be reduced by keeping the number of turns low. However, the parasitic capacitance in reality can be separated into four categories [179]:

- *Capacitance between turns*, which is not relevant when operating at high frequency and with a small number of turns. It can be reduced by changing the conductor insulation to one with a lower dielectric constant.
- *Capacitance between layers*, which is the most important contributor to the overall lumped capacitance. To minimize this capacitance one could: (1) Divide the primary and secondary windings into sections, and then sandwich the other winding between them, as in Figure A.3; (2) Use the foldback winding technique as in Figure A.4b over the normal U type winding technique in Figure A.4a. This will also reduce the voltage gradient between the ends of the windings; (3) Increase the amount of insulation between windings.
- *Capacitance between windings*, related to the common-mode-signal-caused in-circuit noise. It can be reduced by increasing the amount of insulation



(a) Traditional U-Type winding **(b)** Foldback winding

Figure A.4: Winding types.

between windings as well as adding a Faraday Shield or screen between primary and secondary windings, which is usually made of copper foil.

- *Stray capacitance*, whose presence can generate asymmetrical currents and high common mode noise, similar to winding-to-winding capacitance except that the capacitance is between the winding next to the core and the outer winding next to the surrounding circuitry. It can be minimized by using a balanced winding, or using a copper shield over the entire winding.

On one hand, the overall transformer lumped capacitance is detrimental for the application in the sense that it could drive the transformer into premature resonance, produce large current spikes (refer to Chapter 4), and introduce electrostatic coupling to other circuits.

On the other hand, transformer leakage inductance and capacitance have an inverse relationship: decreasing the leakage inductance results in an increase of the winding capacitance [179]. Thereby it seems to be an extra benefit in keeping the winding capacitance relatively large, as the leakage inductance, in turn, is detrimental to the application as it causes voltage spikes in the main switch and second order effects throughout the operation of the circuit.

Comparatively, some criteria for reducing the leakage inductance (i.e. increasing the winding capacitance) are:

- To wind the primary on long bobbins and to keep the secondary winding as close as possible, using a minimum of insulation.
- To divide the primary winding into sections, and then to sandwich the secondary winding between them (Figure A.3), in order to reduce the maximum mmf values. This is beneficial as well for reducing proximity effects.

- In order to minimize the leakage inductance as well as to have a balanced DC resistance, it is recommended to wind bifilar in the secondary. The choice of Litz wire for the secondary is justified by this concept.

In this application, the minimum level of insulation needed has to be carefully considered too, since the primary of the transformer must withstand a voltage up to 1.14kV. The insulation to be used between layers is Tesa ® 51408 (Kapton ® backing with silicone adhesive) adhesive tape, whose datasheet [180] shows to have a dielectric breakdown voltage of 7500V and a total thickness of 65 μm.

The maximum voltage between layers in the application is roughly: $1.14(-1.14/a)$ kV, i.e. 2.28 kV. Therefore, the insulation tape will provide enough insulation between windings. The PCB tracks will have to consider the appropriate insulation level as well.

In order to keep the winding capacitance at an adequate value while reducing the leakage inductance, the transformer design will be implemented based on the following guidelines:

- Number of turns in the primary maximised, in this case to 248.
- The insulation coating of the conductors is made of Polyurethane, with a dielectric strength of 24kV/mm. This means that the coating can sustain 2.28kV before breakdown, which is rather sufficient.
- The sandwiched winding topology in Figure A.3 will be used to reduce the proximity effect and leakage inductance.
- The standard U-type winding technique in Figure A.4a will be used to limit a further reduction in winding capacitance.
- The insulation between windings/layers will be provided simply by layers of the adhesive tape Tesa ® 51408. Hence 65 μm$\times$6 total layers gives 390 μm of total thickness, which is negligible in the space taken in the bobbin.
- The selection of RM-type core will reduce the stray capacitance as the ferrite surrounding the windings has this property.
- Litz wire is used in the secondary. In the primary, in order to maximise the number of turns a reduced diameter is necessary, so a single wire will be used.

Based on this principle the designed winding topology is illustrated in Table A.4 and the schematic of the designed disposition of the winding topology to be used is shown in Figure A.5.

Table A.4: Selected conductors specifications.

Winding:	**Primary**	**Secondary**
Type	Unifilar	Litz
External Diameter (mm)	0.25	1.144
Area(mm^2)	0.0491	0.4846
Number of Strands	1	120
Current density at 20°C(Ω/m)	0.3628	0.0414
Length needed (m)	10.93	1.04

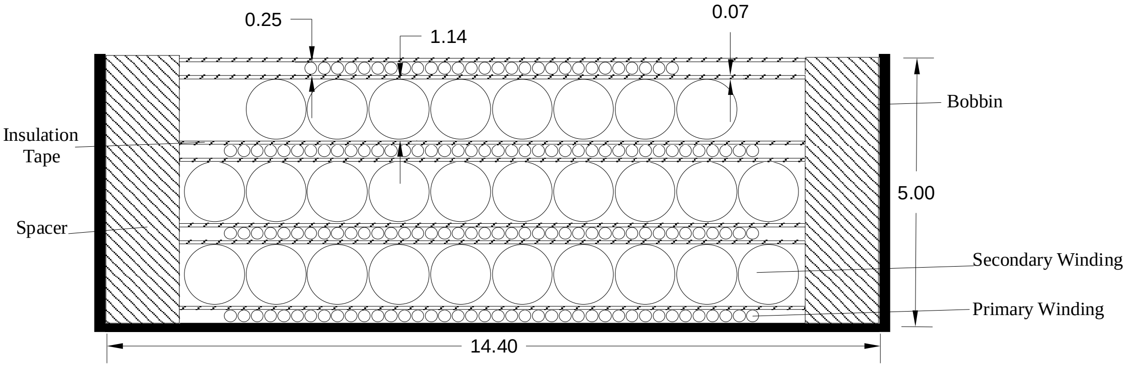


Figure A.5: Winding topology design (values in mm).

For the winding topology defined, an estimation of the parasitic winding capacitance C_{tx} will be provided next.

The greatest contributor to the lumped winding capacitance C_{tx} is the layer-to-layer capacitance. A strategy for the calculation of the layer-to-layer capacitance is presented in [179]. It is assumed that the layers of the winding are equipotential surfaces, thus two successive layers of the winding can be approximated by a parallel-plate capacitor. With the further assumption that the distance between layers is approximately zero, a rule of thumb for a first guess of the parasitic capacitance between each pair of successive layers of windings could be given by (A.24).

$$C_{tx} \approx 60\overline{N}\pi(R_{1,cyl} + R_{2,cyl})[pF] \tag{A.24}$$

where $\overline{N}$ is the average number of turns between the two successive layers of windings, and $R_{1,cyl}, R_{2,cyl}$ are the distances to the centres of conductors as described in Figure A.6.

Eqn. (A.24) is applied 6 times for the 6 in-series interleaved winding capacitances that compose the topology in Figure A.5. The resultant equivalent inter-layer capacitance is 17.7 pF. Accounting for the other lumped effects, the total estimation for the lumped capacitance will be around C_{tx}=20 pF.

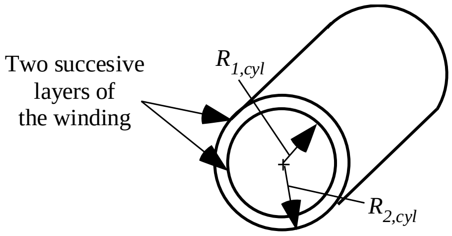


Figure A.6: Cylindrical capacitor model for layered windings [179].

The design of the peripheral elements of the flyback converter system will be addressed next.

A.7 Other Circuit Parts

The last part of the design is the specification of other essential elements in the flyback topology presented in Figure A.1. The elements are specified as follows:

- The diode bridge rectifier (DBR), will be again composed of 4 BYG10Y, 1600V-reverse-voltage rated diodes, as specified in Chapter 7.
- The DIAC D_1 is composed of a string of up to 32 SMDB3 LV-DIACs, with an individual breakover voltage of 36 V [173], to be able to have a tripping voltage of up to 1.14 kV in practice.
- The main switch of the application S_1 is the C2M1000170D SiC MOSFET [158] rated for a 1700V breakover voltage.
- The series resistance R_{diac} is in charge of protecting both the DIAC string and the Zener diode connected to the gate of the MOSFET. Considering the analysis in Section 5.2.1 of Chapter 5, during the DIAC breakover interval t_{bo} each one of the Q DIACs in the DIAC string of the triggering circuit enters a region of negative dynamic resistance as soon as the DC bus voltage reaches the overall breakover voltage of the string. Hence, at the beginning of that interval the current through the DIACs builds up quickly and, according to the characteristic curve of this type of device, the voltage across them drops. From the datasheet of the devices used [173], the forward voltage of each individual DIAC in the string is

$$V_{F_i} = V_{bo_i} - \Delta V \tag{A.25}$$

where ΔV is the dynamic breakover voltage variation under triggering at 10 mA (min.), with a value of 10V in this DIAC model, and V_{bo_i} is the individual breakdown voltage of each DIAC.

The initial value of the current through the DIACs is then approximately

$$I_{diac}(max) \approx \frac{V_{bo} - QV_{F_i}}{R_{lead}} \tag{A.26}$$

where V_{bo} is the overall breakover voltage, Q is the number of DIACs in the string, and R_{lead} is the resistance of the leads in the circuit R_{lead}.

The protection resistor R_{diac} is added in series with the DIAC string, so its value replaces the value of w R_{lead}. Hence, in (A.26), so that the maximum current is re-written as

$$I_{diac}(max) \approx \frac{V_{bo} - QV_{F_i}}{R_{diac}} \tag{A.27}$$

From the datasheet of this device [173], the maximum repetitive on-state current that the DIACs accept is 1 A and the forward voltage of each DIAC is $V_{F_i} = V_{bo_i} - \Delta V$, where ΔV is the dynamic break over voltage variation under triggering at 10mA, with a value of 10 V in this DIAC model. V_{bo_i} is the individual LV breakdown of each DIAC.

Applying (A.27) for the maximum rated current of 1 A, the minimum resistance that guarantees this rating is not exceeded is $R_{diac} = (1.14 \times 10^3 - 32 \times 26)/1 = 308\ \Omega$. A safe value of 470 Ω is chosen.

- The Zener diode of V_Z reverse voltage is in charge of preventing the MOSFET gate voltage to exceed its maximum rating of 25V, and will be selected as an element of extra-low energy consumption. The 24V MMSZ4709T1G Zener diode [174] is chosen, as it features a 10 nA leakage current at 18.2V, and as low as 50 μA test current.

- The Gate-Source resistance R_{gs} connected at the gate of the MOSFET has to be chosen large enough not to represent any significative power loss at the gate. At the same time, since this resistor is the mechanism of discharge of the energy used in the gate to turn the MOSFET on, during the OFF period, the settling time of this process will depend on the resistors value, so that the gate voltage is properly discharged before the next switching pulse.

  The settling time is defined then as ˜5 times the time constant (R_{gs} times the MOSFET Gate-Source capacitance at a voltage close to the output voltage V_o). This value has to be less than the total switching period, i.e. $5R_{gs}(C_{gs}@V_o) <<$

T_s. Replacing the values specified from this application, the condition is then: $5R_{gs}(197pF) << 10ms$, hence $R_{gs} << 10M\Omega$. The chosen resistance is 500 kΩ.

- The output capacitor C_o at the secondary side of the converter is designed based on the equations of the analysis in Chapter 5, from which the output voltage ripple can be derived as

  $$\Delta V_o \approx \frac{2E_o}{V_o I_{sec}(max) C_o} \tag{A.28}$$

  The maximum voltage ripple requirement of 57% is considered to emulate a realistic requirement for a low-power load [82]. Based on previous design values, the voltage considered is the maximum of the application (10V), the maximum secondary current is 1.47A, and the secondary energy from the application is maximum 900 μJ.

  With these values, the minimum requirement is: $C_o > (2 \times 900 \times 10^{-6})/(1.47 \times 0.57 \times 10^2) = 21.5$ μF.

  However, it is recognised in the literature that a higher capacitance has less equivalent series resistance (ESR) so it is an element that could eventually lead to extra losses. Therefore, the capacitance chosen is the 25V, 5.6 mF Panasonic EEUFC1E470, with the feature of 29 mΩ ESR and low leakage current (3 μA) [181].

- Finally, the low-power output resistive load R_o is adjusted to get an output voltage in the range 5V to 10V. If the predicted available output power P_o is calculated with the theory in Chapter 5, then the output resistance can be approximated with $R_o = V_o^2/P_o$. Using this criterion, the allowed resistances are approximately in the range of 560 Ω to 2.2 kΩ. A load of 820 Ω is then chosen.

A.8 Design Test

The design of the self-triggered flyback switching system presented in this appendix was implemented on a printed circuit board (PCB) which is described in Chapter 7.

In order to confirm the fulfilment of the design requirements proposed in this appendix, the following tests were made:

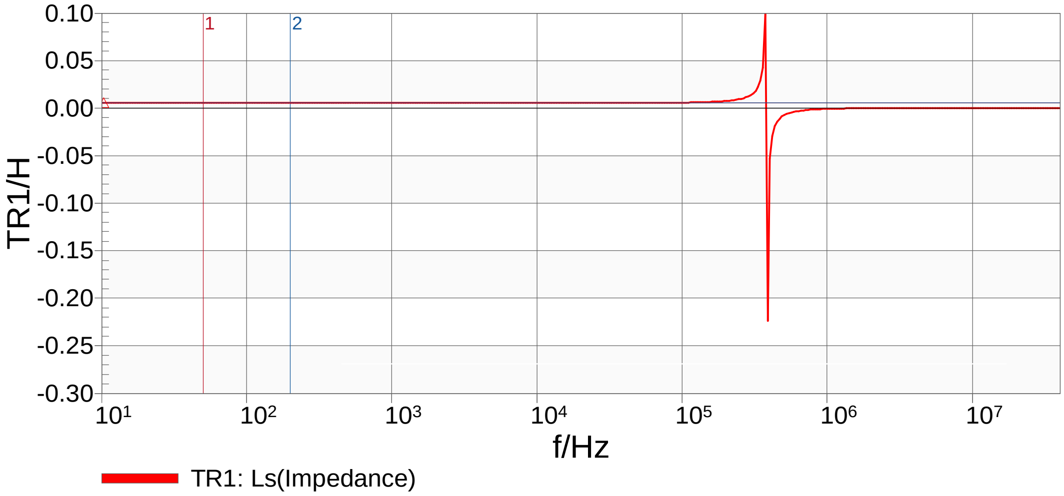


Figure A.7: Series inductance analysis of the flyback transformer primary coil.

- Voltage measurements were made across the primary and secondary of the flyback transformer of the design for frequencies in the expected range. They yielded an average turns-ratio of a=6.08V/1.36V=4.47 which is close to the requirement of 5.

- The Bode Analyser 100 Suite [182] was used to investigate the magnetising inductance of the primary coil of the flyback transformer. The results of the analysis are presented in Figure A.7.

  The measured magnetising inductance of the primary coil is L_m =5.485 mH, for 50Hz and 200 Hz. This is very close to the 5.5 mH requirement.

- The response in Figure A.7 shows a resonance peak at f_r=387.615 kHz. According to theory in [183], the parallel winding capacitance C_{tx} can be calculated with this resonance frequency using

$$C_{tx} \approx \frac{1}{4\pi^2 f_r^2 L_m} \tag{A.29}$$

  The expression yields C_{tx}=30.74pF, which is close to the 20 pF predicted in the design. In addition, the series windings resistance of the transformer is R_{lead}=2.746 Ω, which is low as expected.

The measurements performed in the last section of this appendix, as well as the experimental results depicted in Chapter 5 confirm the achievement of the design requirements.

REFERENCES

[1] J. C. Rodriguez, D. G. Holmes, B. P. McGrath, and R. H. Wilkinson, ‘‘Maximum energy harvesting from medium voltage electric-field energy using power line insulators,’’ in *Australasian Universities Power Engineering Conference (AUPEC)*, Sep. 2014, Conference Proceedings, pp. 1--6.

[2] J. C. Rodriguez, D. G. Holmes, B. P. McGrath, and C. Teixeira, ‘‘Energy harvesting from medium voltage electric fields using pulsed flyback conversion,’’ in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, Conference Proceedings, pp. 3591--3598.

[3] J. C. Rodriguez, D. G. Holmes, B. McGrath, and R. Wilkinson, ‘‘A self-triggered pulsed-mode flyback converter for electric field energy harvesting,’’ *IEEE Journal of Emerging and Selected Topics in Power Electronics*, February 2017, submitted for review.

[4] Intergovernmental Panel on Climate Change, ‘‘Climate change 2013: The physical science basis,’’ IPCC, Tech. Report. IPCC Fifth Assessment Report, 2013. [Online]. Available: https://www.ipcc.ch/pdf/assessment-report/ar5/wg1/WG1AR5_Chapter02_FINAL.pdf

[5] T. Flannery, *Here on Earth: An Argument for Hope.* Text Publishing, 2011. [Online]. Available: https://books.google.com.au/books?id=VnXQUF2T_bAC

[6] K. Richardson, S. W, S. HJ, A. J, and B. T, ‘‘Synthesis report. climate change: global risks, challenges and decisions,’’ *University of Copenhagen*, no. Copenhagen, Denmark, 2009.

[7] L. Xie, P. M. S. Carvalho, L. A. F. M. Ferreira, J. Liu, B. H. Krogh, N. Popli, and M. D. Ilic, ‘‘Wind integration in power systems: Operational challenges and possible solutions,’’ *Proceedings of the IEEE*, vol. 99, no. 1, pp. 214--232, 2011.

[8] A. G. Boulanger, A. C. Chu, S. Maxx, and D. L. Waltz, ‘‘Vehicle electrification: Status and issues,’’ *Proceedings of the IEEE*, vol. 99, no. 6, pp. 1116--1138, 2011.

[9] V. C. Gungor, D. Sahin, T. Kocak, S. Ergut, C. Buccella, C. Cecati, and G. P. Hancke, ‘‘Smart grid technologies: Communication technologies and standards,’’ *Industrial Informatics, IEEE Transactions on*, vol. 7, no. 4, pp. 529--539, 2011.

[10] Z. Ziming, S. Lambotharan, C. Woon Hau, and F. Zhong, ‘‘Overview of demand management in smart grid and enabling wireless communication technologies,’’ *Wireless Communications, IEEE*, vol. 19, no. 3, pp. 48--56, 2012.

[11] Y. Ye, Q. Yi, H. Sharif, and D. Tipper, ‘‘A survey on smart grid communication infrastructures: Motivations, requirements and challenges,’’ *Communications Surveys & Tutorials, IEEE*, vol. 15, no. 1, pp. 5--20, 2013.

[12] R. Moghe, ‘‘Smart sensors for utility assets,’’ Ph.D. Dissertation, Georgia Institute of Technology, 2012.

[13] R. Chang, Y. Yuan, H. Lv, W. Yin, and S. X. Yang, ‘‘Selling the smart grid; part 1: Why consumers must buy in for the smart grid to succeed,’’ *IEEE Consumer Electronics Magazine*, vol. 1, no. 2, pp. 24--31, 2012.

[14] Australian Government: Deparment of the Environment and Energy. (2016) The Renewable Energy Target (RET) Scheme. [Online]. Available: https://www.environment.gov.au/climate-change/renewable-energy-target-scheme

[15] R. Das, V. Madani, F. Aminifar, J. McDonald, S. S. Venkata, D. Novosel, A. Bose, and M. Shahidehpour, ‘‘Distribution automation strategies: Evolution of technologies and the business case,’’ *IEEE Transactions on Smart Grid*, vol. 6, no. 4, pp. 2166--2175, 2015.

[16] Y. Hua, M. Oliphant, and E. J. Hu, ‘‘Development of renewable energy in Australia and China: A comparison of policies and status,’’ *Renewable Energy*, vol. 85, pp. 1044--1051, 2016.

[17] V. Madani, R. Das, F. Aminifar, J. McDonald, S. S. Venkata, D. Novosel, A. Bose, and M. Shahidehpour, ‘‘Distribution automation strategies challenges and opportunities in a changing landscape,’’ *IEEE Transactions on Smart Grid*, vol. 6, no. 4, pp. 2157--2165, 2015.

[18] S. Galli, A. Scaglione, and W. Zhifang, ‘‘For the grid and through the grid: The role of power line communications in the smart grid,’’ *Proceedings of the IEEE*, vol. 99, no. 6, pp. 998--1027, 2011.

[19] L. Peretto, ‘‘The role of measurements in the smart grid era,’’ *IEEE Instrumentation & Measurement Magazine*, vol. 13, no. 3, pp. 22--25, 2010.

[20] Y. Yang, ‘‘Power line sensor networks for enhancing power line reliability and utilization,’’ Ph.D. Dissertation, Georgia Institute of Technology, 2011.

[21] P. Wolfs and S. Isalm, ‘‘Potential barriers to smart grid technology in australia,’’ in *Australasian Universities Power Engineering Conference, AUPEC*, 2009, Conference Proceedings, pp. 1--6.

[22] Y. C. Wu, L. F. Cheung, K. S. Lui, and P. W. T. Pong, ‘‘Efficient communication of sensors monitoring overhead transmission lines,’’ *IEEE Transactions on Smart Grid*, vol. 3, no. 3, pp. 1130--1136, 2012.

[23] Y. Yi, D. Divan, R. G. Harley, and T. G. Habetler, ‘‘Power line sensornet - a new concept for power grid monitoring,’’ in *IEEE Power Engineering Society General Meeting*, 2006, Conference Proceedings, p. 8 pp.

[24] V. C. Gungor, L. Bin, and G. P. Hancke, ‘‘Opportunities and challenges of wireless sensor networks in smart grid,’’ *IEEE Transactions on Industrial Electronics*, vol. 57, no. 10, pp. 3557--3564, 2010.

[25] T. A. Papadopoulos, C. G. Kaloudas, A. I. Chrysochos, and G. K. Papagiannis, ‘‘Application of narrowband power-line communication in medium-voltage smart distribution grids,’’ *Power Delivery, IEEE Transactions on*, vol. 28, no. 2, pp. 981--988, 2013.

[26] C. Rodine, ‘‘The Field Area Network (FAN),’’ EPRI, Stanford University EE392n, Tech. Rep., 2011.

[27] Z. Fei, ‘‘Field area networks (fans),’’ University of Kentucky, Smart Grid Communications and Energy Efficient Computing (Fall 2015) Lecture Slides, Tech. Rep., 2015.

[28] Y. Yang, D. Divan, R. G. Harley, and T. G. Habetler, ‘‘Design and implementation of power line sensornet for overhead transmission lines,’’ in *IEEE Power & Energy Society General Meeting, PES ’09*, 2009, Conference Proceedings, pp. 1--8.

[29] D. M. Toma, J. del Rio, and A. Manuel-Lazaro, ‘‘Self-powered high-rate wireless sensor network for underground high voltage power lines,’’ in *IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, 2012, Conference Proceedings, pp. 1881--1885.

[30] A. Usman and S. H. Shami, ‘‘Evolution of communication technologies for smart grid applications,’’ *Renewable and Sustainable Energy Reviews*, vol. 19, no. 0, pp. 191--199, 2013.

[31] T. Lei, W. Kuang-Ching, H. Yong, and G. Fangming, ‘‘Channel characterization and link quality assessment of ieee 802.15.4-compliant radio for factory environments,’’ *Industrial Informatics, IEEE Transactions on*, vol. 3, no. 2, pp. 99--110, 2007.

[32] Electric Power Research Institute, ‘‘Future inspection and monitoring of underground transmission lines,’’ (EPRI), Report, 2009.

[33] R. Moghe, Y. Yi, F. Lambert, and D. Divan, ‘‘Design of a low cost self powered stick-on current and temperature wireless sensor for utility assets,’’ in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2010, Conference Proceedings, pp. 4453--4460.

[34] C. Buratti, I. Korpeoglu, E. Karasan, and R. Verdone, ‘‘Bluetooth or 802.15.4 technologies to optimise lifetime of wireless sensor networks: Numerical comparison under a common framework,’’ in *6th International Symposium on Modeling and Optimization in Mobile, Ad Hoc, and Wireless Networks and Workshops, WiOPT*, 2008, Conference Proceedings, pp. 539--543.

[35] E. Ferro and F. Potorti, ‘‘Bluetooth and wi-fi wireless protocols: a survey and a comparison,’’ *Wireless Communications, IEEE*, vol. 12, no. 1, pp. 12--26, 2005.

[36] P. Ferrari, A. Flammini, D. Marioli, and A. Taroni, ‘‘Ieee802.11 sensor networking,’’ *Instrumentation and Measurement, IEEE Transactions on*, vol. 55, no. 2, pp. 615--619, 2006.

[37] NXP. (2011, September) JN5148-EK010 Evaluation Kit. [Online]. Available: http://www.farnell.com/datasheets/866637.pdf

[38] Y. Xiaomei, Z. Shuibao, L. Fengjie, and X. Shouzhi, ‘‘Security of power line monitoring system based on wireless sensor network,’’ in *World Automation Congress (WAC)*, 2012, Conference Proceedings, pp. 251--254.

[39] A. R. Hirakawa, M. Martucci, T. C. G. Vilhena, S. M. Amancio, and J. C. V. Lemos, ‘‘Wireless image transmission in electric power hostile environment,’’ in *IEEE 35th Conference on Local Computer Networks (LCN)*, 2010, Conference Proceedings, pp. 760--763.

[40] L. Li, X. Hu, K. Chen, and K. He, ‘‘The applications of wifi-based wireless sensor network in internet of things and smart grid,’’ in *6th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 2011, Conference Proceedings, pp. 789--793.

[41] T. Pan and X. Liu, ‘‘Hybrid wireless communication system using zigbee and wifi technology in the coalmine tunnels,’’ in *Third International Conference on Measuring Technology and Mechatronics Automation (ICMTMA)*, vol. 2, 2011, Conference Proceedings, pp. 340--343.

[42] S. K. Tyagi, ‘‘Transient response of electronic devices and their failure mechanism,’’ in *International Conference on Electromagnetic Interference and Compatibility ’99*, 1999, Conference Proceedings, pp. 497--499.

[43] D. Liu and Y. Cheng, ‘‘Study of interference and damage experiments on electronic equipment in transient and stable em field,’’ in *3rd International Symposium on Electromagnetic Compatibility*, 2002, Conference Proceedings, pp. 308--313.

[44] D. C. Liu, L. Zhang, C. Li, G. Chang, Q. Wang, and J.-F. Zou, ‘‘Study on the failure mechanism of the electronic device in the transient electromagnetic field,’’ in *IEEE International Symposium on Electromagnetic Compatibility, EMC ’03*, vol. 2, 2003, Conference Proceedings, pp. 1036--1039 Vol.2.

[45] H. Zangl, T. Bretterklieber, and G. Brasseur, ‘‘A feasibility study on autonomous online condition monitoring of high-voltage overhead power lines,’’ *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 5, pp. 1789--1796, 2009.

[46] C. R. Valenta, P. A. Graf, M. S. Trotter, G. A. Koo, G. D. Durgin, W. G. Daly, and B. J. Schafer, ‘‘High-voltage-environment backscatter-channel measurements at 5.8 ghz,’’ *Antennas and Propagation Magazine, IEEE*, vol. 53, no. 4, pp. 231--240, 2011.

[47] N. Bui, A. Georgiadis, M. Miozzo, M. Rossi, and X. Vilajosana, ‘‘SWAP Project: Beyond the State of the Art on Harvested Energy-Powered Wireless Sensors Platform Design,’’ in *IEEE 8th International Conference on Mobile Adhoc and Sensor Systems (MASS)*, 2011, Conference Proceedings, pp. 837--842.

[48] J. A. Paradiso and T. Starner, ‘‘Energy scavenging for mobile and wireless electronics,’’ *Pervasive Computing, IEEE*, vol. 4, no. 1, pp. 18--27, 2005.

[49] H. Zangl, T. Bretterklieber, and G. Brasseur, ‘‘Energy harvesting for online condition monitoring of high voltage overhead power lines,’’ in *IEEE Instrumentation and Measurement Technology Conference Proceedings, IMTC*, 2008, Conference Proceedings, pp. 1364--1369.

[50] T. Keutel, X. Zhao, and O. Kanoun, ‘‘C6. 2-energy scavenging for monitoring of overhead power line networks,’’ *Proceedings SENSOR 2009*, vol. 2, pp. 207--212, 2009.

[51] Z. Xinming, T. Keutel, M. Baldauf, and O. Kanoun, ‘‘Energy harvesting for overhead power line monitoring,’’ in *9th International Multi-Conference on Systems, Signals and Devices (SSD)*, 2012, Conference Proceedings, pp. 1--5.

[52] R. Moghe, Y. Yi, F. Lambert, and D. Divan, ‘‘A scoping study of electric and magnetic field energy harvesting for wireless sensor networks in power system applications,’’ in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2009, Conference Proceedings, pp. 3550--3557.

[53] M. Zhu, P. C. Baker, N. M. Roscoe, M. D. Judd, and J. Fitch, ‘‘Alternative power sources for autonomous sensors in high voltage plant,’’ in *EEE Electrical Insulation Conference*, 2009, Conference Proceedings, pp. 36--40.

[54] Y. Yi, D. Divan, and R. G. Harley, ‘‘Power line vicinity monitoring via multiple displacement current measurement,’’ in *IEEE Power and Energy Society General Meeting*, 2010, Conference Proceedings, pp. 1--8.

[55] G. Feng, H. Hayat, and W. Jin, ‘‘Energy harvesting devices for high voltage transmission line monitoring,’’ in *IEEE Power and Energy Society General Meeting*, 2011, Conference Proceedings, pp. 1--8.

[56] M. J. Moser, T. Bretterklieber, H. Zangl, and G. Brasseur, ‘‘Strong and weak electric field interfering: Capacitive icing detection and capacitive energy harvesting on a 220-kv high-voltage overhead power line,’’ *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2597--2604, 2011.

[57] C. Keunsu, K. Sungmuk, P. Kyungjin, S. Seunghwan, K. Hyeong-Seok, and K. Hoseong, ‘‘Electric field energy harvesting powered wireless sensors for smart grid,’’ *Journal of Electrical Engineering & Technology*, vol. 7, no. 1, pp. 75--80, 2012.

[58] J. A. van Schalkwyk and G. P. Hancke, ‘‘Energy harvesting for wireless sensors from electromagnetic fields around overhead power lines,’’ in *IEEE International Symposium on Industrial Electronics (ISIE)*, 2012, Conference Proceedings, pp. 1128--1135.

[59] R. Moghe, A. Iyer, F. C. Lambert, and D. Divan, ‘‘A low-cost electric-field energy harvester for an mv/hv asset-monitoring smart-sensor,’’ in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2013, Conference Proceedings, pp. 2676--2683.

[60] K. Hoseong, C. Dongkil, G. Sungmin, and P. Kyungjin, ‘‘Stray electric field energy harvesting technology using mems switch from insulated ac power line,’’ *Electronics Letters*, vol. 50, no. 17, pp. 1236--1238, 2014.

[61] Z. Dongsheng, D. Dong, and L. Licheng, ‘‘Electric field energy harvesting for on-line condition-monitoring device installed on high-voltage transmission tower,’’ *Electronics Letters*, vol. 51, no. 21, pp. 1692--1693, 2015.

[62] R. Moghe, A. Iyer, F. C. Lambert, and D. Divan, ‘‘A low-cost electric field energy harvester for an mv/hv asset-monitoring smart sensor,’’ *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1828--1836, 2015.

[63] J. Zhang, P. Li, Y. Wen, F. Zhang, and C. Yang, ‘‘Management circuit with up-conversion oscillation technology for electric-field energy harvesting,’’ *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5515--5523, 2016.

[64] J. A. Sanchez, J. Arriola, and H. Baroja, ‘‘Key point for the future challenges of the smartgrids: The architecture of the smart t-station,’’ in *IET SmartGrids for Distribution, CIRED Seminar*, 2008, Conference Proceedings, pp. 1--4.

[65] H. Jinchi, H. Jun, Y. Yang, W. Zhongxu, S. X. Wang, and H. Jinliang, ‘‘A nonintrusive power supply design for self-powered sensor networks in the smart grid by scavenging energy from ac power line,’’ *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4398--4407, 2015.

[66] G. D. Szarka, S. G. Burrow, and B. H. Stark, ‘‘Ultralow power, fully autonomous boost rectifier for electromagnetic energy harvesters,’’ *Power Electronics, IEEE Transactions on*, vol. 28, no. 7, pp. 3353--3362, 2013.

[67] S. J. Roundy, ‘‘Energy scavenging for wireless sensor nodes with a focus on vibration to electricity conversion,’’ Ph.D. Dissertation, The University of California, Berkeley, 2003.

[68] S. Jiaying and T. Yen Kheng, ‘‘Energy consumption analysis of zigbee-based energy harvesting wireless sensor networks,’’ in *IEEE International Conference on Communication Systems (ICCS)*, 2012, Conference Proceedings, pp. 468--472.

[69] D. Pimentel and P. Musilek, ‘‘Power management with energy harvesting devices,’’ in *23rd Canadian Conference on Electrical and Computer Engineering (CCECE)*, 2010, Conference Proceedings, pp. 1--4.

[70] R. Dayal, S. Dwari, and L. Parsa, ‘‘Design and implementation of a direct ac-dc boost converter for low-voltage energy harvesting,’’ *IEEE Transactions on Industrial Electronics*, vol. 58, no. 6, pp. 2387--2396, 2011.

[71] T. Chi-Ying, S. Hui, K. Wing-Hung, and S. Feng, ‘‘Ultra-low voltage power management and computation methodology for energy harvesting applications,’’ in *Symposium on VLSI Circuits, 2005. Digest of Technical Papers.*, 2005, Conference Proceedings, pp. 316--319.

[72] A. R. Chandrakasan, N. Verma, and D. C. Daly, ‘‘Ultralow-power electronics for biomedical applications,’’ in *Department of Electrical Engineering and Computer Science.* Massachusetts Institute of Technology, Cambridge, 2008, vol. 10, pp. 247--274. [Online]. Available: http://www.scopus.com/inward/record.url?eid=2-s2.0-50249113200&partnerID=40&md5=bf61cb397296d1bd3d807bbed30adaf1

[73] M. D. Seeman, S. R. Sanders, and J. M. Rabaey, ‘‘An ultra-low-power power management IC for energy-scavenged Wireless Sensor Nodes,’’ in *IEEE Power Electronics Specialists Conference, PESC*, 2008, Conference Proceedings, pp. 925--931.

[74] W. Chia-Ling and Y. Hsiu-Hui, ‘‘Analysis and design of a step-down switched-capacitor-based converter for low-power application,’’ in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2010, Conference Proceedings, pp. 3184--3187.

[75] M. S. M. Resali and H. Salleh, ‘‘Comparison of energy harvesting power management techniques and application,’’ in *34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT)*, 2010, Conference Proceedings, pp. 1--5.

[76] C. Carvalho, J. P. Oliveira, and N. Paulino, ‘‘Survey and analysis of the design issues of a low cost micro power dc-dc step up converter for indoor light energy harvesting applications,’’ in *Proceedings of the 19th International Conference*

Mixed Design of Integrated Circuits and Systems (MIXDES), 2012, Conference Proceedings, pp. 455--460.

[77] R. Radzuan, M. A. A. Raop, M. K. M. Salleh, M. K. Hamzah, and R. A. Zawawi, ''The designs of low power ac-dc converter for power electronics system applications,'' in *IEEE Symposium on Computer Applications and Industrial Electronics (ISCAIE)*, 2012, Conference Proceedings, pp. 113--117.

[78] M. F. El-Kady, V. Strong, S. Dubin, and R. B. Kaner, ''Laser scribing of high-performance and flexible graphene-based electrochemical capacitors,'' *Science*, vol. 335, no. 6074, pp. 1326--1330, 2012.

[79] W. He, P. Li, Y. Wen, J. Zhang, A. Yang, and C. Lu, ''A noncontact magnetoelectric generator for energy harvesting from power lines,'' *IEEE Transactions on Magnetics*, vol. 50, no. 11, pp. 1--4, 2014.

[80] K. E. Martin, D. Hamai, M. G. Adamiak, S. Anderson, M. Begovic, G. Benmouyal, G. Brunello, J. Burger, J. Y. Cai, B. Dickerson, V. Gharpure, B. Kennedy, D. Karlsson, A. G. Phadke, J. Salj, V. Skendzic, J. Sperr, Y. Song, C. Huntley, B. Kasztenny, and E. Price, ''Exploring the IEEE Standard C37.118-2005 Synchrophasors for Power Systems,'' *IEEE Transactions on Power Delivery*, vol. 23, no. 4, pp. 1805--1811, 2008.

[81] L. Selavo, Z. Gang, and J. A. Stankovic, ''Seemote: In-situ visualization and logging device for wireless sensor networks,'' in *3rd International Conference on Broadband Communications, Networks and Systems, BROADNETS*, 2006, Conference Proceedings, pp. 1--9.

[82] Texas Instruments. (2012) MSP430 MIXED SIGNAL MICROCONTROLLER. [Online]. Available: http://www.ti.com/lit/ds/symlink/msp430f2274.pdf

[83] ENERGY Micro. (2012, September 11th) FM32TG840F32 MCU Datasheet. [Online]. Available: http://cdn.energymicro.com/dl/devices/pdf/d0011_efm32tg840_datasheet.pdf

[84] ATMEL. (2012, July) ATmega128RFA1. [Online]. Available: http://www.atmel.com/Images/8266S.pdf

[85] NXP. (2012, 12 September 2012) JN5148-001 IEEE802.15.4 Wireless Microcontroller Data Sheet.

[86] Microchip. (2011, March) PIC18F46J50 Data Sheet. [Online]. Available: http://ww1.microchip.com/downloads/en/DeviceDoc/39931d.pdf

[87] Freescale, ‘‘MC1322x Advanced ZigBe- Compliant SoC Platform for the 2.4 GHz IEEE 802.15.4 Standard Reference Manual,’’ January, 2012 2012. [Online]. Available: http://cache.freescale.com/files/rf_if/doc/ref_manual/MC1322xRM.pdf?fsrch=1&sr=2

[88] Samsung. (2004) S3C2440A 32-BIT CMOS MICROCONTROLLER USER'S MANUAL. [Online]. Available: http://arm9download.cncncn.com/datasheet/S3C2440.pdf

[89] S. Roundy, ‘‘On the effectiveness of vibration-based energy harvesting,’’ *Journal of Intelligent Material Systems and Structures*, vol. 16, no. 10, pp. 809--823, 2005.

[90] J. Qui, Y. Wen, P. Li, and Y. Jin, ‘‘Design and testing of piezoelectric energy harvester for powering wireless sensors of electric line monitoring system,’’ *Journal of Applied Physics*, vol. 111, no. 7, pp. 07E510--07E510--3, 2012.

[91] Q. Qingquan, X. Shouqiao, X. Liye, Z. Zhiqin, Z. Zhifeng, Z. Guomin, and D. Shaotao, ‘‘Stray energy based generator in electrical equipment to power wireless temperature sensor,’’ in *International Conference on Electrical Machines and Systems (ICEMS)*, 2011, Conference Proceedings, pp. 1--5.

[92] D. J. de Villiers, S. Kaplan, and R. H. Wilkinson, ‘‘Energy harvesting for a condition monitoring mote,’’ in *34th Annual Conference of IEEE Industrial Electronics, IECON*, 2008, Conference Proceedings, pp. 2161--2166.

[93] T. Hosseinimehr and A. Tabesh, ‘‘Magnetic field energy harvesting from ac lines for powering wireless sensor nodes in smart grids,’’ *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 4947--4954, 2016.

[94] L. Soobum and B. D. Youn, ‘‘A new piezoelectric energy harvesting design concept: multimodal energy harvesting skin,’’ *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, vol. 58, no. 3, pp. 629--645, 2011.

[95] J. Han, J. Hu, Y. Yang, Z. Wang, S. X. Wang, and J. He, ‘‘A nonintrusive power supply design for self-powered sensor networks in the smart grid by scavenging energy from ac power line,’’ *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4398--4407, 2015.

[96] Z. G. Wan, Y. K. Tan, and C. Yuen, ‘‘Review on energy harvesting and energy management for sustainable wireless sensor networks,’’ in *IEEE 13th International Conference on Communication Technology (ICCT)*, 2011, Conference Proceedings, pp. 362--367.

[97] C. Sravanthi and J. M. Conrad, ‘‘A survey of energy harvesting sources for embedded systems,’’ in *IEEE SoutheastCoN*, 2008, Conference Proceedings, pp. 442--447.

[98] M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, ‘‘A survey of thermal energy harvesting techniques and interface circuitry,’’ in *IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS)*, 2013, Conference Proceedings, pp. 381--384.

[99] S. Dalola, M. Ferrari, V. Ferrari, M. Guizzetti, D. Marioli, and A. Taroni, ‘‘Characterization of thermoelectric modules for powering autonomous sensors,’’ *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 1, pp. 99--107, 2009.

[100] A. Arroyo, P. Castro, R. Martinez, M. Manana, A. Madrazo, R. Lecuna, and A. Gonzalez, ‘‘Comparison between ieee and cigre thermal behaviour standards and measured temperature on a 132-kv overhead power line,’’ *Energies*, vol. 8, no. 12, p. 12391, 2015.

[101] A. Decker, ‘‘Solar energy harvesting for autonomous field devices,’’ *IET Wireless Sensor Systems*, vol. 4, no. 1, pp. 1--8, 2014.

[102] H. J. Visser and R. J. M. Vullers, ‘‘Rf energy harvesting and transport for wireless sensor network applications: Principles and requirements,’’ *Proceedings of the IEEE*, vol. PP, no. 99, pp. 1--14, 2013.

[103] B. Allen, T. Ajmal, V. Dyo, and D. Jazani, ‘‘Harvesting energy from ambient radio signals: A load of hot air?’’ in *Loughborough Antennas and Propagation Conference (LAPC)*, 2012, Conference Proceedings, pp. 1--4.

[104] S. Bellal, H. Takhedmit, and L. Cirio, ‘‘Design and experiments of transparent rectennas for wireless power harvesting,’’ in *IEEE Wireless Power Transfer Conference (WPTC)*, 2016, Conference Proceedings, pp. 1--4.

[105] A. O. Bicen, O. B. Akan, and V. C. Gungor, ‘‘Spectrum-aware and cognitive sensor networks for smart grid applications,’’ *Communications Magazine, IEEE*, vol. 50, no. 5, pp. 158--165, 2012.

[106] D. T. Silva, J. L. Silvino, and J. C. D. De Melo, ‘‘Power harvesting from shield wires for monitoring apparatus on overhead transmission lines,’’ in *9th IEEE/IAS International Conference on Industry Applications (INDUSCON)*, 2010, Conference Proceedings, pp. 1--5.

[107] J. P. Amaro, F. J. T. E. Ferreira, R. Cortes, x00E, and J. Landeck, ‘‘Energy harvesting for zigbee compliant wireless sensor network nodes,’’ in *38th Annual Conference on IEEE Industrial Electronics Society IECON*, 2012, Conference Proceedings, pp. 2583--2588.

[108] Z. Kolodziejczyk, P. Michalski, and W. Kardys, ‘‘Novel autonomous voltage and current measurement unit for smart grids,’’ in *International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2012, Conference Proceedings, pp. 780--784.

[109] S. Takahashi, N. Yoshida, K. Maruhashi, and M. Fukaishi, ‘‘Real-time current-waveform sensor with plugless energy harvesting from ac power lines for home/building energy-management systems,’’ in *2011 IEEE International Solid-State Circuits Conference*, Conference Proceedings, pp. 220--222.

[110] J. Cheang, W. Cheng, D. Gavrilov, B. Schiller, V. Smagin, and M. Gouzman, ‘‘High efficiency powering system for wireless sensor for ac monitoring in smart grid applications,’’ in *11th International Conference & Expo on Emerging Technologies for a Smarter World (CEWIT)*, 2014, Conference Proceedings, pp. 1--5.

[111] P. Li, Y. Wen, Z. Zhang, and S. Pan, ‘‘A high-efficiency management circuit using multiwinding upconversion current transformer for power-line energy harvesting,’’ *IEEE Transactions on Industrial Electronics*, vol. 62, no. 10, pp. 6327--6335, 2015.

[112] J. Moon and S. B. Leeb, ‘‘Analysis model for magnetic energy harvesters,’’ *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4302--4311, 2015.

[113] K. Tashiro, H. Wakiwaka, S. Inoue, and Y. Uchiyama, ‘‘Energy harvesting of magnetic power-line noise,’’ *Magnetics, IEEE Transactions on*, vol. 47, no. 10, pp. 4441--4444, 2011.

[114] R. Moghe, F. C. Lambert, and D. Divan, ‘‘Smart stick-on sensors for the smart grid,’’ *Smart Grid, IEEE Transactions on*, vol. 3, no. 1, pp. 241--252, 2012.

[115] K. Niotaki, A. Collado, A. Georgiadis, S. Kim, and M. M. Tentzeris, ‘‘Solar/electromagnetic energy harvesting and wireless power transmission,’’ *Proceedings of the IEEE*, vol. 102, no. 11, pp. 1712--1722, 2014.

[116] D. Porcarelli, D. Spenza, D. Brunelli, A. Cammarano, C. Petrioli, and L. Benini, ‘‘Adaptive rectifier driven by power intake predictors for wind energy harvesting sensor networks,’’ *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 2, pp. 471--482, 2015.

[117] W. Wang, X. Huang, L. Tan, J. Zhao, and C. Yan, "Hybrid wireless charging system for monitoring overhead 110 kv high-voltage power line equipment based on magneto-electric conversion," *IET Generation, Transmission & Distribution*, vol. 10, no. 5, pp. 1199--1208, 2016.

[118] United Energy, Australia, "Asset management plan 2016 - 2025," UE, Report, 2015.

[119] Ltd GL Mcgavin Pty. (2013) MODIEWARK Non-Contact & Contact Voltage Detectors Operation Manual. [Online]. Available: http://morristechnologygroup.com.au/gl/wp-content/uploads/sites/3/2013/07/Modiewark-Manual.pdf

[120] P. J. Frey, A. Vukojevic, and M. S. Smith, "BG&E Makes a Smart Grid Case," *T&D World Magazine*, December 2012. [Online]. Available: http://viewer.zmags.com/publication/90ebab7d#/90ebab7d/42

[121] W. R. Smith-Vaniz and R. L. Sieron, "Apparatus for measuring the potential of a transmission conductor," USA Patent EP Patent 0,218,221, 1991. [Online]. Available: https://www.google.com/patents/US4714893

[122] Gridsense. (2012) LineIQ User Manual. [Online]. Available: http://www.gridsense.com/wp/wp-content/uploads/downloads/2012/08/LineIQ-User-Manual-v2.0.pdf

[123] Schweitzer Engineering Laboratories (SEL) Inc. (2011) WSO-11 Wireless Sensor Datasheet. [Online]. Available: https://www.selinc.com/FCI/Overhead/WirelessSensor/

[124] NORDIC Semiconductor. (2010, 2010/06/24) What is ULP wireless connectivity? [Online]. Available: http://www.nordicsemi.com/eng/News/Press-Center/Press-Backgrounders/What-is-ULP-wireless-connectivity

[125] ZHUHAI GENE COSMOS ELECTRIC TECHNOLOGY. (2013) Overhead line fault indicator CSM-SCO. [Online]. Available: http://www.cosmos-electric.com/en/Products.asp?BigClassId=2&SmallclassId=7

[126] ABB. (2010) Type SCC-125 Split-core combination current and voltage transformer.

[127] NEXANS. (2013) CAT-1 Series 3.1 (Real-Time). [Online]. Available: http://www.nexans.us/eservice/US-en_US/navigatepub_0_-17373_1673_40_4932/CAT_1_Transmission_Line_Monitoring_System.html

[128] USI. (2012) Power donut systems for overhead electric power line monitoring. [Online]. Available: http://www.usi-power.com/Products%20&%20Services/Donut/Power_Donut2_Qualifications.pdf

[129] A. E. Tzinevrakis, D. K. Tsanakas, and E. I. Mimos, ''Analytical calculation of the electric field produced by single-circuit power lines,'' *Power Delivery, IEEE Transactions on*, vol. 23, no. 3, pp. 1495--1505, 2008.

[130] G. Ge, Z. Weidong, C. Xiang, and L. Rui, ''Analytical method of electromagnetic susceptibility of electronic equipments with enclosure in electric power system at system level,'' in *China International Conference on Electricity Distribution, CICED*, 2008, Conference Proceedings, pp. 1--4.

[131] J. Wu, D. Su, and H. Li, ''The effect of electromagnetic environment of high-voltage transmission line and ubstations on electronic equipment test,'' in *8th International Symposium on Antennas, Propagation and EM Theory, ISAPE*, 2008, Conference Proceedings, pp. 1216--1219.

[132] H. D. Bruns, C. Schuster, and H. Singer, ''Numerical electromagnetic field analysis for emc problems,'' *Electromagnetic Compatibility, IEEE Transactions on*, vol. 49, no. 2, pp. 253--262, 2007.

[133] K. Hameyer, R. Mertens, and R. Belmans, ''Numerical methods to evaluate the electromagnetic fields below overhead transmission lines and their measurement,'' in *First IEEE International Caracas Conference on Devices, Circuits and Systems*, 1995, Conference Proceedings, pp. 32--36.

[134] A. Bernadic, I. Juric-Grgic, and R. Lucic, ''Solution of electromagnetic compatibility problem in electrical power network using the finite element method,'' in *Conference Proceedings ICECom*, 2010, Conference Proceedings, pp. 1--4.

[135] J. C. McLaughlin and K. L. Kaiser, ''Deglorifying the maximum power transfer theorem and factors in impedance selection,'' *Education, IEEE Transactions on*, vol. 50, no. 3, pp. 251--255, 2007.

[136] C. S. Kong, ''A general maximum power transfer theorem,'' *Education, IEEE Transactions on*, vol. 38, no. 3, pp. 296--298, 1995.

[137] R. A. Serway, R. J. Beichner, and J. W. Jewett, *Physics for scientists and engineers with modern physics*, 6th ed. London: Brooks/Cole: Pacific Grove, Calif., 2003.

[138] M. Amin, S. Amin, and M. Ali, ‘‘Monitoring of leakage current for composite insulators and electrical devices,’’ *Rev. Adv. Mater. Sci*, vol. 21, pp. 75--89, 2009.

[139] T. Sorqvist, S. M. Gubanski, and A. E. Vlastos, ‘‘Field experience with non-ceramic hollow-core insulators,’’ in *Eleventh International Symposium on (Conf. Publ. No. 467) High Voltage Engineering*, vol. 4, 1999, Conference Proceedings, pp. 42--45 vol.4.

[140] G. Montoya, I. Ramirez, and J. I. Montoya, ‘‘Correlation among esdd, nsdd and leakage current in distribution insulators,’’ *Generation, Transmission and Distribution, IEE Proceedings-*, vol. 151, no. 3, pp. 334--340, 2004.

[141] E. Nishiyama, K. Kuwanami, M. Kawano, T. Matsuda, and I. Oota, ‘‘Development of portable equipment for monitoring currents and voltages of power transmission lines,’’ in *IEEE International Symposium on Industrial Electronics, ISIE*, vol. 3, 2002, Conference Proceedings, pp. 964--969 vol.3.

[142] M. F. Hussin, A. Haddad, and N. Harid, ‘‘Voltage transducer for monitoring of high voltage overhead lines,’’ in *45th International Universities Power Engineering Conference (UPEC)*, 2010, Conference Proceedings, pp. 1--5.

[143] E. Nishiyama, K. Kuwanami, M. Kawano, T. Matsuda, and I. Oota, ‘‘Development of monitoring equipment of currents and voltages of power-transmission lines,’’ in *Transmission and Distribution Conference and Exhibition 2002: Asia Pacific. IEEE/PES*, vol. 3, 2002, Conference Proceedings, pp. 2310--2315 vol.3.

[144] T. Zuo, T. Liu, K. Chen, and X. Hu, ‘‘On-line monitoring system of insulator leakage current based on arm,’’ in *6th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 2011, Conference Proceedings, pp. 365--369.

[145] V. Proca and N. Paduraru, ‘‘Methods for non-conventional measuring sensor integration in the medium voltage electrical equipment,’’ in *IEEE Russia Power Tech*, 2005, Conference Proceedings, pp. 1--6.

[146] DRIESCHER. (2013) Voltage Testing System for rated voltages 12 kV, 24 kV, 36 kV and 38.5 kV. [Online]. Available: http://www.mvtech.com.au/catalogues/Voltagetestingsystemfinal_Driescher.pdf

[147] J. Hrastnik and J. Pihler, ‘‘Designing a new post insulator using 3-d electric-field analysis,’’ *Power Delivery, IEEE Transactions on*, vol. 24, no. 3, pp. 1377--1381, 2009.

[148] ANSYS, 2017. [Online]. Available: http://www.ansys.com/

[149] Tektronix, ``Passive high-voltage probes.'' [Online]. Available: http://www.testequipmentdepot.com/tektronix/pdf/p5100a-tpp0850-p5120-p5122-p6015a.pdf

[150] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, ``A review of single-phase improved power quality ac-dc converters,'' *Industrial Electronics, IEEE Transactions on*, vol. 50, no. 5, pp. 962--981, 2003.

[151] J. R. Rodriguez, J. W. Dixon, J. R. Espinoza, J. Pontt, and P. Lezana, ``Pwm regenerative rectifiers: state of the art,'' *Industrial Electronics, IEEE Transactions on*, vol. 52, no. 1, pp. 5--22, 2005.

[152] A. K. Abdelsalam, A. Massoud, A. Darwish, and S. Ahmed, ``Simplified generic on-line pwm technique for single phase grid connected current source inverters,'' in *Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, Conference Proceedings, pp. 1398--1403.

[153] B. Wu, *High-Power Converters and AC Drives.* PWM Current Source Rectifiers, 2006, no. 11.

[154] G. Sorral, ``High performance voltage control of multilevel current source inverters,'' Ph.D. dissertation, RMIT University, School of Electrical and Computer Engineering, 2010.

[155] L. Balogh, ``Design And Application Guide for High Speed MOSFET Gate Drive Circuits,'' *Texas Instruments/Unitrode Corporation, Power Supply Design Seminar, SEM*, p. 32, 2001.

[156] Fairchild Semiconductor Corporation. (2000) AN-9010 MOSFET Basics. [Online]. Available: http://www.fairchildsemi.com/an/AN/AN-9010.pdf

[157] A. Pressman, K. Billings, and T. Morey, *Switching Power Supply Design*, 3rd ed. McGraw-Hill, 2009.

[158] CREE. (2013) Silicon Carbide Power MOSFET Z-FET N-Channel Enhancement Mode. [Online]. Available: www.cree.com/pow

[159] S. Singer, S. Ozeri, and D. Shmilovitz, ``A pure realization of loss-free resistor,'' *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 51, no. 8, pp. 1639--1647, 2004.

[160] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, ‘‘Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters,’’ in *IEEE Workshop on Computers in Power Electronics*, 2002, Conference Proceedings, pp. 36--41.

[161] Ferroxcube A Yageo. Design of planar power transformers application note. [Online]. Available: http://ferroxcube.home.pl/appl/info/plandesi.htm

[162] ANALOG DEVICES. (2014) ADCMP609 Rail-to-Rail, Fast, Low Power 2.5 V to 5.5 V,Single-Supply TTL/CMOS Comparator Datasheet. [Online]. Available: www.analog.com

[163] ON SEMICONDUCTOR. (2007) MURS480ET3G Ultrafast E’’ Series with High Reverse Energy Capability Datasheet. [Online]. Available: http://onsemi.com

[164] EPCOS AG, ‘‘ETD34 Product Specification,’’ 2013. [Online]. Available: https://en.tdk.eu/inf/80/db/fer_13/etd_34_17_11.pdf

[165] TEKTRONIX. (2013) TPS2000 Series Digital Storage Oscilloscope 071-1441-02 Datasheet. [Online]. Available: http://www.tek.com

[166] ALTIUM DESIGNER. (2016) User manual. [Online]. Available: http://www.altium.com/

[167] PowerSIM Inc. (2016) User manual. [Online]. Available: https://powersimtech.com/

[168] VISHAY. (2009) BYG10D thru BYG10Y Standard Avalanche SMD Rectifier Datasheet. [Online]. Available: www.vishay.com

[169] Creative Power Technologies(CPT). (2016). [Online]. Available: http://www.creativepower.com.au/

[170] Texas Instruments. (2016) TI LM78L05 Datasheet. [Online]. Available: http://www.ti.com/

[171] ON Semiconductors. (2016) FAN3122 Datasheet. [Online]. Available: https://www.fairchildsemi.com/

[172] HIPOTRONICS INC. (2016) HIPOTRONICS AC high voltage test set. [Online]. Available: http://www.haefely-hipotronics.com/

[173] ST Microelectronics. (2016) SMDB3 DIAC Datasheet. [Online]. Available: http://www.st.com/

[174] ON Semiconductors, ‘‘MMSZ4678T1 Zener Voltage Regulators,’’ 2016. [Online]. Available: http://www.onsemi.com/pub/Collateral/MMSZ4678T1-D.PDF

[175] K. Billings and T. Morey, *Switchmode power supply handbook.* McGraw-Hill, 2011.

[176] W. G. Hurley, ‘‘Design challenges for high frequency magnetic circuit design for power conversion,’’ 2016.

[177] M. K. Kazimierczuk and H. Sekiya, ‘‘Design of ac resonant inductors using area product method,’’ in *IEEE Energy Conversion Congress and Exposition*, 2009, Conference Proceedings, pp. 994--1001.

[178] TDK, 2016. [Online]. Available: http://en.tdk.eu/tdk-en/180492/design-support/design-tools/ferrites

[179] J. Biela and J. W. Kolar, ‘‘Using transformer parasitics for resonant converters; a review of the calculation of the stray capacitance of transformers,’’ *IEEE Transactions on Industry Applications*, vol. 44, no. 1, pp. 223--233, 2008.

[180] Tesa, 2016. [Online]. Available: http://www.tesa.com/industry/tesa-51408.html

[181] Panasonic, 2016. [Online]. Available: http://www.panasonic.com/au/

[182] OMICRON LAB. (2010) BODE 100 USER MANUAL. [Online]. Available: https://www.omicron-lab.com/fileadmin/assets/manuals/Bode_100_Manual_AE4_HR.pdf

[183] W. T. McLyman, *Winding Capacitance and Leakage Inductance.* 270 Madison Ave. New York, NY 10016: Marcel Dekker, Inc, 2006.