Fault Response of Grid-Connected Inverter Dominated Networks

C.A. Plet, M.Graovac, R.Iravani, T.C. Green

***Abstract*—The rapid increase in installed distributed generation (DG) has led to concerns about the impact on the proper operation of the protection system. In particular, the limited fault current capability of inverter interfaced distributed generation (IIDG) could lead to malfunctioning of the distribution network protection system which largely relies on overcurrent based protection techniques. The absence of tried and tested models and methods to calculate the inverter fault current contribution has been a significant challenge to the introduction of IIDG. This paper shows that with a few subtle changes, conventional analytical network analysis techniques can be used to analyse the fault response of inverter dominated distribution networks. The theoretical results are validated by PSCAD simulations and experimental results.**

***Index Terms*—inverter, fault response, load flow, distributed generation**

I. Introduction

CONCERNS about climate change, fuel prices and energy security have fuelled an increase in the amount of renewable energy sources connected to the electric power transmission and distribution grid. Many renewable energy sources employ power electronic interfaces e.g. inverters, to connect to the electrical distribution network either because their output is not directly compatible to the grid (photovoltaic panels, μTurbines) or because the flexibility of control of power electronics allows optimal energy extraction (wind turbines with doubly fed induction generators (DFIG) or full inverter interfaces). Due to the low thermal inertia of semiconductor switches, inverters are actively current limited and thus have a rather small fault current contribution ($\approx$ 1-2pu) compared to conventional generators ($\approx$ 5-10pu). It has been recognised that although the flexibility of control of inverters enables them to provide useful grid services during normal operation [1], their limited current capability can, during faults, lead to problems with the operation of the incumbent overcurrent based protection system.

One of the reasons hampering the integration of IIDG thus far, has been characterising inverter behaviour for short-circuit studies. Well known, proven and tested methods of representing conventional generators exist, but since the inverter's characteristics are dominated by its control strategy, protection engineers often have to resort to a full time-domain representation which is time consuming, computationally intensive and thus costly.

By analysing the fault response of a popular type of grid connected inverter control strategy, a load-flow based technique is proposed for analysing distribution networks containing inverter interfaced generation. The technique correctly identifies which inverters go into current limit mode and it correctly predicts the fault currents and voltages in the network for both balanced and unbalanced faults. The method can be used for transient, sub-transient, and steady-state periods to be compatible with conventional generator representations.

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II. Grid connected inverter control

The fault response of any inverter is dictated by its control strategy. Figure 1 shows the layout of a grid-connected inverter and its control system. It tracks the output complex power references by regulating the inductor currents. It is largely similar to the control strategy discussed in [2] except that current control is performed in the natural reference frame and the current limiting module is shown explicitly.

A. Grid Synchronisation

Independent control of real and reactive power output requires knowledge of the phase angle of the positive sequence fundamental component of the grid voltage i.e. the inverter must be synchronised to the grid. A three phase synchronous reference frame phase locked loop (SRF-PLL) [3] is used in this controller because of its simplicity. A 100Hz band-stop filter is used in the frequency feedback path to remove double harmonic oscillations due to the presence of negative sequence components. During a complete collapse of terminal voltage, the frequency reference is fixed to its pre-fault value to retain some form of phase angle estimate throughout the fault.

B. Current control

A filter inductor current control loop as shown in figure 2 is used to ensure balanced sinusoidal currents i.e. inductor current quality, even when the grid voltage is distorted. Zero steady-state error is achieved by implementing current control in the natural reference frame using proportional-resonant (P+R) compensators [4].

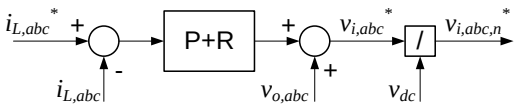

Figure 2. Current Controller

Feed-forward of the output voltage is applied to minimise disturbances due to a change in grid voltage. Decoupling can be applied to negate any transient errors due to coupling between any of the phases. Any disturbances caused by

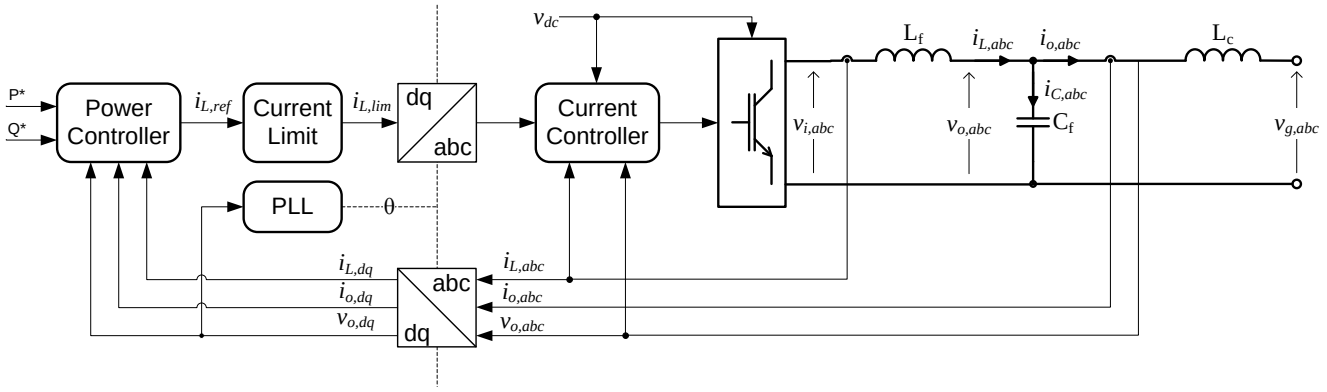

Figure 1. Grid connected inverter control system

variations in the DC link voltage are effectively dealt with by normalising the inverter bridge voltage reference with respect to the DC link voltage.

C. Power control

Control of the complex output power is performed in the synchronous reference frame by deriving output current references based on the output voltage using instantaneous power theory [2]. For a given complex power setpoint $S_{\rm ref} = P_{\rm ref} + j \cdot Q_{\rm ref}$ and an output voltage of $\vec{v}_o = v_{od} + j \cdot v_{oq}$, the required output currents can be calculated with

$$\begin{bmatrix} i_{od,\rm ref} \\ i_{oq,\rm ref} \end{bmatrix} = \frac{1}{v_{od}^2 + v_{oq}^2} \cdot \begin{bmatrix} v_{od} & v_{oq} \\ v_{oq} & -v_{od} \end{bmatrix} \cdot \begin{bmatrix} P_{ref} \\ Q_{ref} \end{bmatrix} \quad (1)$$

The current control loop regulates the filter inductor current. Given that $i_C = i_L - i_o$, and $i_{L,\rm ref} = i_{o,\rm ref} + i_C$ the inductor reference currents can be found from

$$i_{L,\rm ref} = i_{o,\rm ref} + i_L - i_o \quad (2)$$

Average power control rather than instantaneous power control is performed in order to achieve high inductor current quality. This is achieved by low-pass filtering the inductor current references as shown in figure 3. To achieve a satisfactory speed of response of the power controller, a cut off frequency of 5Hz is chosen. In steady state, the inductor current references are thus clean DC signals, devoid of any switching harmonics or any double harmonic ripple due to unbalance.

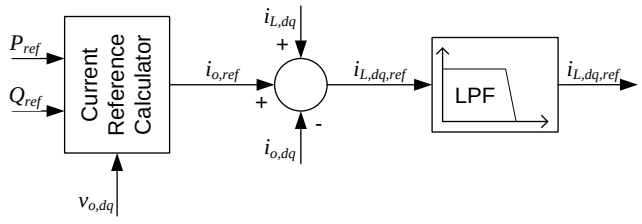

Figure 3. Power controller

An unbalanced grid voltage is characterised by the presence of positive, as well as negative and zero sequence components i.e. $v_o = v_o^+ + v_o^- + v_o^0$. Zero sequence components are not considered in the current reference calculations as only 3 phase 3 leg inverters are considered. The negative sequence component appears as a 2ω component in the synchrounously rotating reference frame and thus has a zero time average i.e. the current reference negative sequence component gets filtered out by the low pass filter. This means that the current reference calculation is based solely on the grid voltage positive sequence component and generates a positive sequence only current reference. The inductor current reference required to satisfy a given power reference as a function of the output voltage is given by

$$\vec{i}_{L,ref} = conj\left(\frac{\vec{S}_{ref}}{3 \cdot \vec{v}_o^{+}}\right) + \vec{v}_o^{+} \cdot j\omega C_f \quad (3)$$

This is of course subject to the ability of the PLL to generate 'clean' phase angle information of the grid voltage positive sequence component.

D. Current limiting

The power electronic switches in the inverter bridge typically exhibit rather low thermal inertia and thus need to be protected from overheating by actively limiting the filter inductor current. Several approaches to achieve this are listed below:

1) Instantaneous hard limits in the natural reference frame - limits the instantaneous magnitude of the sinusoidal inductor current reference on a per phase basis, resulting in clipping and distorted waveforms.
2) Instantaneous hard limits in the synchronously rotating reference frame - limits the instantaneous magnitude of the inductor current by freezing the inductor current reference direct and quadrature components once the inductor current magnitude exceeds a threshold $i_{\rm th}$. Since the inductor current reference only contains the positivie sequence component and thus no 2ω sinusoidal ripple, no distortion occurs.
3) Pre-defined inductor fault current in the synchronously rotating reference frame - limits the instantaneous magnitude of the inductor current by switching to a pre-defined inductor fault current reference $\vec{i}_{\rm f}$ once the inductor current reference has exceeded a threshold $i_{\rm th}$.

Since grid codes are likely to require grid support services of any generator connected to the grid, the last option has been chosen in this work since it allows the inverter to inject a pre-defined current (e.g. just reactive current) during faulty conditions. The absence of any integral action in the power controller means that the inductor current reference always inversely reflects the terminal voltage magnitude and exhibits no wind-up. Therefore, when the terminal voltage returns, the inductor current reference will drop below the threshold again and the inverter can resume power export.

It must be noted that current limiting in the synchronous reference frame is undesirable in microgrids [5] as fault currents are injected into healthy phases which can lead to overvoltages. For inverters connected to a large grid this should not pose any problems. Alternatively, rms current limiting on a per phase basis can be implemented in the natural reference frame. This is considered out of scope for this paper.

III. Fault response of a single inverter

Faults are characterised by a temporary decrease in the voltage magnitude on one or more phases. As shown in the previous section, the grid-connected inverter's natural response to this is to increase the output current in order to track the power setpoints. If the grid voltage magnitude before and after the fault are defined by $\vec{v}_o(0)$ and $\vec{v}_o(F)$, respectively, then the corresponding steady state inductor fault current references are calculated with (3) as $\vec{i}_{L,\mathrm{ref}}(0)$ and $\vec{i}_{L,\mathrm{ref}}(F)$. The presence of the first order low pass filter with a cut off frequency of ω_c in the power controller causes the inductor current to approach its new reference value in exponential fashion after a step change in output voltage in $t = F$ as dictated by:

$$\vec{i}_{L,\mathrm{ref}}(t) = \vec{i}_{L,\mathrm{ref}}(0) + \left(\vec{i}_{L,\mathrm{ref}}(F) - \vec{i}_{L,\mathrm{ref}}(0)\right) \cdot \left(1 - e^{-\omega_c t}\right) \tag{4}$$

If the output voltage sag is deep enough, then $|\vec{i}_{L,\mathrm{ref}}(F)|$ will exceed i_{th} at some time $t = D$ and the inverter current limiting module will switch to a pre-defined fault current reference $\vec{i}_{\mathrm{f}}$ as described in (5) and illustrated in figure 4 for a voltage sag of 66%, a threshold of $i_{\mathrm{th}} = 1.6\mathrm{pu}$ and a fault current reference of $\vec{i}_{\mathrm{f}} = 2\mathrm{pu}$. At rated power and at a pre-fault output voltage of $\vec{v}_o(0) = 1\mathrm{pu}$, the inverter inductor current reference is $\vec{i}_{L,\mathrm{ref}}(0) = 1\mathrm{pu}$. At time $t = F$ a fault occurs somewhere in the network, that causes the output voltage to drop to $\vec{v}_o(F) = 1/3\mathrm{pu}$. In order to track the output power setpoints, the power controller will attempt to track an inductor current reference which exponentially approaches $|\vec{i}_{L,\mathrm{ref}}(F)| = 3\mathrm{pu}$. At time $t = D$ the inductor current reference magnitude exceeds the threshold i_{th} and current limiting is triggered. The inductor current reference is now dictated by the current limiting module to be $|\vec{i}_{L,\mathrm{lim}}(D)| = 2\mathrm{pu}$ where it will stay until $|\vec{i}_{L,\mathrm{ref}}| < i_{\mathrm{th}}$.

Provided that the low pass filter sufficiently attenuates any negative sequence components, the above is valid also during unbalanced conditions. Note that if current control is performed in the synchronously rotating reference frame, the PI compensators are not capable of suppressing the 2ω sinusoidal ripple caused by unbalance, in which case the inverter can no longer be seen as a positive sequence current source.

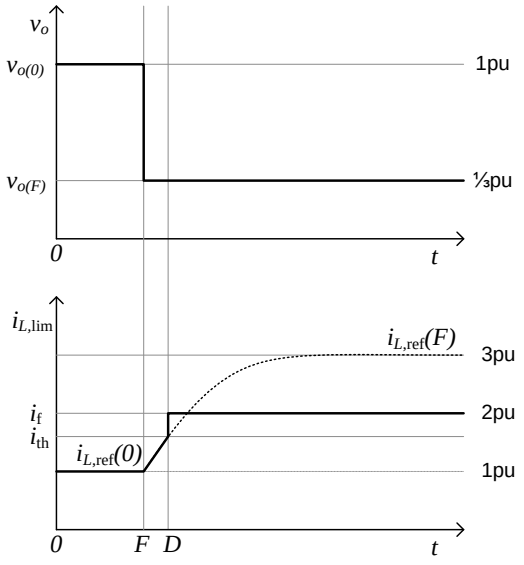

Figure 4. Single inverter fault response

From the above analysis, it can be concluded that during normal operation, the inverter can be represented as a positive sequence P&Q source behind a coupling reactance as shown in figure 5 (Note that the filter capacitor does appear in the negative sequence equivalent circuit, because the control system is unable to suppress the negative sequence current drawn by it).

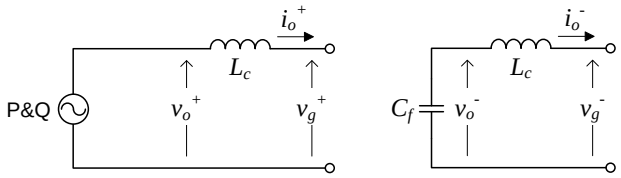

Figure 5. Equivalent positive sequence P&Q source during normal operation

During voltage sags when the current threshold is exceeded, the grid connected inverter can be represented as a constant positive sequence current source in parallel with the filter capacitor as shown in figure 6.

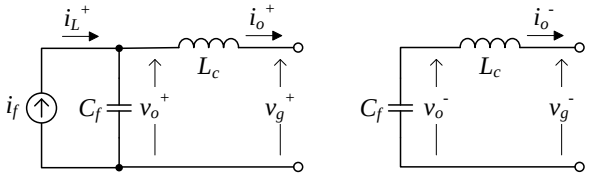

Figure 6. Equivalent positive sequence current source during operation under reduced output voltage

It can be seen that, much like conventional generators, the fault response of a grid-connected inverter can be divided into three distinct intervals: sub-transient ($t = F$), transient

$$\vec{i}_{L,\mathrm{lim}} = \mathrm{if} \begin{cases} t \leq F & \vec{i}_{L,\mathrm{ref}}(0) \\ F < t \leq D & \vec{i}_{L,\mathrm{ref}}(0) + \left(\vec{i}_{L,\mathrm{ref}}(F) - \vec{i}_{L,\mathrm{ref}}(0)\right) \cdot (1 - e^{-\omega_c t}) \\ t > D & \vec{i}_{\mathrm{f}} \end{cases} \tag{5}$$

($F < t < D$), and steady-state ($t \geq D$), with clearly defined behaviour during each period. This property is useful in the fault analysis of large networks containing both conventional as well as inverter interfaced generation.

The moment at which the threshold is exceeded can be calculated analytically from the time domain step response of the first order low pass filter in the power controller:

$$F - D = t_D = \frac{-1}{\omega_c} \cdot \ln\left(1 - \frac{i_{\mathrm{th}} - i_{L,\mathrm{ref}}(0)}{i_{L,\mathrm{ref}}(F) - i_{L,\mathrm{ref}}(0)}\right) \tag{6}$$

For higher order filters an analytical solution for t_D does not exist but its value can be found iteratively.

IV. Fault response of multiple inverters

The behaviour of multiple grid-connected inverters in a distribution network during normal operation can be analysed easily using conventional load flow techniques by representing them as PQ nodes i.e. nodes into which a constant P and Q are injected regardless of the bus voltage. Using the Gauss-Seidel load flow solution [6], the voltage of an arbitrary bus *i* can be found by iteratively solving:

$$\vec{v}_i^{k+1} = \frac{conj\left(\frac{P_i + j \cdot Q_i}{3\vec{v}_i^{+k}}\right) + \sum_{j=1}^{n} y_{ij} \cdot \vec{v}_{j^k}}{\sum_{j=0}^{n} y_{ij}} \qquad i \neq j \tag{7}$$

where the term $conj\left(\frac{P_i + j \cdot Q_i}{3\vec{v}_i^{+k}}\right)$ represents the phase current injected into that bus by a positive sequence PQ controlled source. Since the grid connection point absorbs any shortfall or excess in local generation, it is treated as slack bus, assuming that the voltage at this point is regulated using tapchangers or SVCs i.e. $v_i^{k+1} = v^k$. PV nodes can be represented by calculating the amount of reactive power needed to regulate the voltage at a defined real power setpoint and then using (8) to find the bus voltages eventhough the effectiveness of this method is questionable in distribution networks with a low X/R ratio.

Systematic fault analysis in large networks containing one or more generators is normally performed using the bus impedance short-circuit matrix method [6]. All generators in the network are assumed grounded and at the fault bus, a voltage source of equal magnitude but opposite polarity to the pre-fault bus voltage is connected in series with the fault impedance. The fault current is found by representing the network by its equivalent impedance in series with the fault impedance and the voltage source representing the fault. To find the voltages and currents in the rest of the network, this fault current is injected into the bus impedance matrix.

This type of analysis relies on a number of assumptions and approximations:

- Fault current drawn by the fault is significant in relation to nominal currents, justifying the assumption that load effects can be ignored.
- Generators are capable of maintaining their terminal voltage to some degree throughout the fault by injecting large fault currents.
- Non-linearities in conventional generator fault response are dealt with by replacing them with a linear approximation that is suitable for the type of study. E.g. a synchronous generator is usually represented by the series combination of a positive sequence voltage source with a magnitude equal to the pre-fault bus voltage and a reactance whose value differs for sub-transient, transient or steady-state studies.
- Constant power loads are ignored or approximated by their impedance at rated voltage which is not accurate during steady-state.
- Generator representation (sub-transient, transient, steady-state) is independent of the calculated bus voltage. This is not the case with inverters.

Instead, using the analysis presented in section III, a subtle change to the load flow method is proposed to analyse inverter dominated grid connected networks. Grid-connected inverters can be represented as current constrained PQ nodes. I.e. during normal operation, they are treated as PQ nodes but once their inductor current exceeds the threshold, they type-switch to current source node. The iteration for this type of node is given by:

$$\vec{v}_i^{k+1} = \frac{\vec{i}_{\mathrm{f}} + \sum_{j=1}^{n} y_{ij} \cdot \vec{v}_{j^k}}{\sum_{j=0}^{n} y_{ij}} \qquad i \neq j \tag{8}$$

If one inverter goes into current limit mode, the bus voltages elsewhere in the network may drop even further and force other inverters into current limit mode. Therefore, the load flow algorithm with current restrained PQ nodes needs to be repeated until the number of current limiting inverters does not change. For a network containing n buses and N lines, the algorithm is defined as follows:

1) Get line data and include the fault at bus k as an impedance to ground, the neutral, or another phase
2) Get bus data including all necessary data such as power and voltage setpoints and current thresholds and fault current references.
3) Construct bus admittance matrix **Y**
4) Calculate bus voltages using information from tables I and II and the formulas for different types of nodes below. Record the current injected into each inverter bus.

Table I
LINE AND FAULT DATA

Line	**Left** bus	**Right** bus	$\boldsymbol{R}_{\text{line}}$ [Ω]	$\boldsymbol{X}_{\text{line}}$ [Ω]
1	1	2	R_{12}	X_{12}
⋮				
fault	0	k	R_f	X_f
⋮				
N	i	j	R_{ij}	X_{ij}

Table II
BUS AND GENERATOR DATA

Bus	**Type**	**P** [W]	**Q** [VAr]	**V** [V]	$\boldsymbol{i}_{\text{th}}$ [A]	$\vec{\boldsymbol{i}}_{\mathbf{f}}$ [A]
1	slack	-	-	-	-	-
⋮						
i	PQ	P_i	Q_i	-	$i_{\text{th,i}}$	$\vec{i}_{\text{f},i}$
⋮						
n	PV	P_n	-	v_n	-	-

a) for a slack bus, the voltage does not change, so:

$$v_i^{k+1} = v_i^k$$

b) For a PQ bus use equation 7 to find the bus voltage
c) For a PV bus find the amount of reactive power required to maintain the terminal voltage with:

$$Q_i^k = \max \begin{cases} Q_{max} \\ -\text{Im}\left\{ v_i^{ref,k} . \sum_{j=1}^{n} y_{ij} v_j^k \right\} \end{cases} \qquad i \neq j$$

Then use equation 7 to find the bus voltage
d) For a current source bus the bus voltage can be found with:

$$\vec{v}_i^{k+1} = \frac{\vec{i}_{\text{f},i} + \sum_{j=1}^{n} y_{ij} \cdot \vec{v}_{j^k}}{\sum_{j=0}^{n} y_{ij}} \qquad i \neq j$$

5) Check if any inverters have exceeded current threshold i.e.

$$i_{L,\text{ref},i} > i_{\text{th},i}$$

a) if any new inverters have exceeded current threshold, switch their node type to current source bus and go to 4.
b) if no new inverters have gone into current limiting, go to 6.

6) Get line currents using calculated bus voltages and the system admittance matrix.

This algorithm can be implemented in per phase representation, sequence networks or single line representation. The worst case number of times the load flow procedure needs to be run is equal to the number of inverters in the network plus one. Speed of calculation can be improved by allowing larger error margins on all load flows except for the last one or by introducing an acceleration parameter. Both methods require a mention of caution as they can lead to convergence issues. It is assumed that with modern day computing power and existing computation acceleration techniques, the additional computational effort required by the proposed method is of no concern.

V. SIMULATION & EXPERIMENTAL RESULTS

The analysis presented in section III is validated by comparing analytical results calculated in MATLAB with experimental measurements for a simple network containing an emulated grid and a grid-connected inverter. To verify the analysis from section IV, the fault response of three grid-connected inverters in the CIGRE European Low Voltage Residential Distribution Network Benchmark [7] are simulated using PSCAD.

A. Experimental results for the fault response of a single inverter

The experimental set up to validate (5) is shown in figure 7. It comprises a 5kVA inverter with a 2pu overrating as the grid-connected inverter using first order low pass filters in the power controller. A voltage controlled 90kVA inverter with a 500Hz voltage control bandwidth is used as grid emulator. Both inverters are controlled through the TRIPHASE rapid prototyping environment [8], allowing all system measurements to be collected directly into SIMULINK for comparison with the current magnitude predicted by (5).

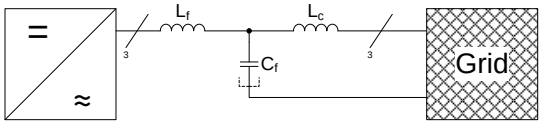

Figure 7. Experimental setup single line diagram

The parameters of the grid-connected inverter are shown in table III. To test the grid-connected inverter fault response, a type C voltage sag [9] consisting of 0.5 pu positive sequence and 0.2pu positive sequence is applied to the terminals of the LCL-filter as the grid-connected inverter is running at nominal power i.e. $S = (4 + j3)$kVA . A purely real fault current reference of $\vec{i}_{\text{th}} = 25A\angle 0°$ has been chosen arbitrarily. Various ways of choosing a fault current reference have been suggested in literature [10] considering current quality and power oscillations and are considered out of scope for this paper.

The grid emulator controls its terminal voltage to $\vec{v}_g(0) = \sqrt{2} \cdot 200V\angle 0°$. At time $t = F$, an unbalanced fault is applied and the positive sequence component dips to $\vec{v}_g^{+}(F) = \sqrt{2} \cdot 100V\angle 0°$ and a negative sequence component appears $\vec{v}_g^{-}(F) = \sqrt{2} \cdot 40V\angle 0°$. The PLL synchronises with the d-axis so the pre-fault capacitor voltage of the grid-connected inverter is measured as $\vec{v}_o(0) = \sqrt{2} \cdot 208V\angle 0°V$. The positive sequence component during the fault is measured as $\vec{v}_o^{+}(F) = \sqrt{2} \cdot 105V\angle 0°$. The voltage rise is caused by cabling and contactor resistance in the experimental setup but does not otherwise affect the results.

Table III
10KVA GRID-CONNECTED INVERTER PARAMETERS

Description	Symbol	Value	Unit
Nominal complex power	$S_{\rm nom}$	$4+j3$	kVA
Nominal terminal voltage	V_g	200	$\rm V_{rms,l-n}$
Filter inductor	L_f	2.3	mH
Filter inductor resistance	R_{L_f}	0.1	Ω
Filter capacitor	C_f	8.8	μF
Filter capacitor ESR	R_{C_f}	0.1	Ω
Coupling inductor	L_c	0.93	mH
Coupling inductor ESR	R_{L_c}	0.1	Ω
Switching frequency	f_s	10	kHz
Current control bandwidth	f_i	2	kHz
Power control bandwidth	f_P	5	Hz
Overcurrent threshold	$i_{\rm th}$	19	A
Fault current reference	$\vec{i}_{\rm f}$	$25+j0$	A

Using (3) the steady-state inductor pre-fault and fault currents can be found as $\vec{i}_L(0) = 10.76A\angle -33.1°$ and $\vec{i}_L^+(F) = 21.39A\angle -34.8°$. As the steady-state fault current magnitude exceeds the current threshold $i_{\rm th} = 19A$, current limiting is triggered at time $t = D$ which can be found using (6) as $t = 47.5$ms. From (5) it follows that the steady state fault current is now dictated by the current limiting module and set at $\vec{i}_L^+(F) = 25A\angle 0°$.

The experimental results are shown in figure 8 where the top plot shows the measured capacitor voltage and the bottom plot shows the inductor current. The thick black line in the top plot indicates the measured positive sequence peak voltage magnitude. In the bottom plot, the thick black line is the inductor current peak magnitude calculated with (5).

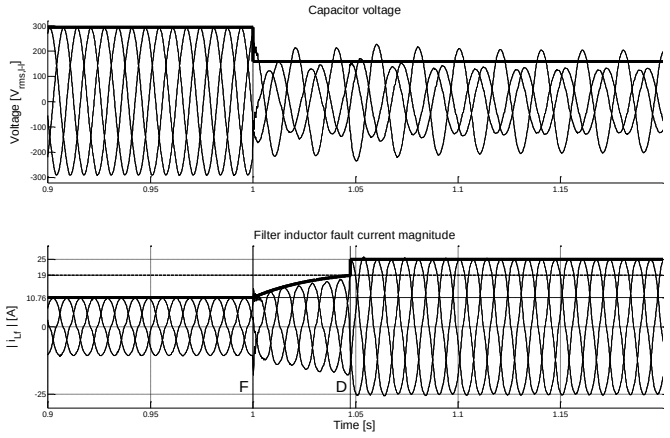

Figure 8. Analytical solution to (5) superimposed (thick black line) on experimental results for a 0.5pu dip in positive sequence magnitude in the presence of 0.2pu negative sequence.

B. Simulation results for fault response of multiple inverters

The CIGRE European Low Voltage Residential Distribution Network Benchmark is shown in figure 9. A full description of the network and its line data is given in [7]. For illustrative purposes, the network is adapted to a three wire system grounded only at the distribution transformer secondary and at the inverter filter capacitor star points. Three inverters with a control strategy as discussed in section III are connected to bus 16, 14 and 15, respectively, and are operating at nominal power i.e. $S = (4 + j3)$kVA. Their parameters are given in table III. At $t = 0.4s$ a double phase-to-ground fault is applied with a fault impedance of $R_f = 0.01\Omega$ at node 6.

Using the algorithm described in section IV, the bus voltages, line currents and fault current in the network are computed as well as the inverter inductor current and capacitor voltage. The predicted inductor currents of inverters 1, 2 and 3 are shown in table IV as well as the fault current seen by the distribution transformer secondary LV winding. The method predicts that inverters 1 and 3 will go into current limiting.

Table IV
FAULT CURRENTS AND VOLTAGES PREDICTED BY LOAD FLOW BASED ALGORITHM

	$\vec{i}_{L,1}$ [A]	$\vec{i}_{L,2}$ [A]	$\vec{i}_{L,3}$ [A]	$\vec{i}_{\rm tx,lv}$ [kA]
a	$25\angle 0°$	$15.3\angle 38.3°$	$25\angle 0°$	$3.69\angle -55.3°$
b	$25\angle -120°$	$15.3\angle -81.7°$	$25\angle -120$	$3.69\angle -175.3°$
c	$25\angle 120°$	$15.3\angle 158.3°$	$25\angle 120°$	$0.07\angle -139.5°$

For comparison, the results shown in table IV have been superimposed (thick black lines) on PSCAD simulation results in figure 10. It can be seen that the analytical method correctly determines which inverter goes into current limiting. Furthermore, it correctly computes the magnitudes of the fault currents in the network. For this example, two load flow runs were required to obtain the presented results. Experimental validation of the analytical method will be presented in future work.

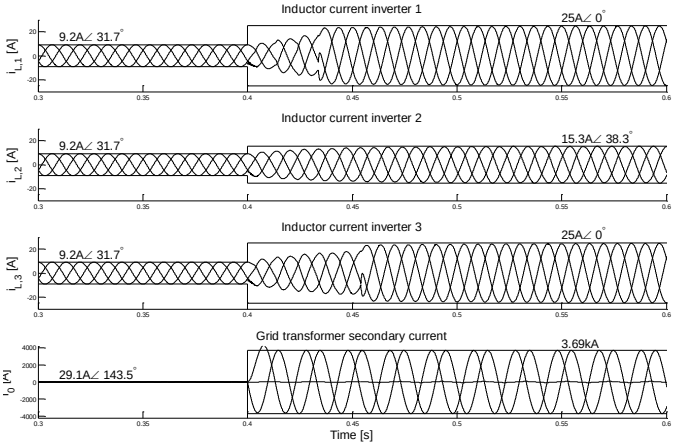

Figure 10. PSCAD simulation results for a faulty network containing multiple inverters

VI. CONCLUSIONS

The challenge in representing IIDG in fault studies and the need for suitable, tried and tested analytical inverter fault models has been discussed. It has been noted that an inverter's fault response is dictated predominantly by its control strategy. By analysing the fault response of a popular three-phase grid-connected inverter control strategy, analytical fault models for individual grid-connected inverters have been developed. Following from the properties of these fault models, shortcomings in traditional fault analysis methods have been discussed. An extension to existing load flow techniques has been

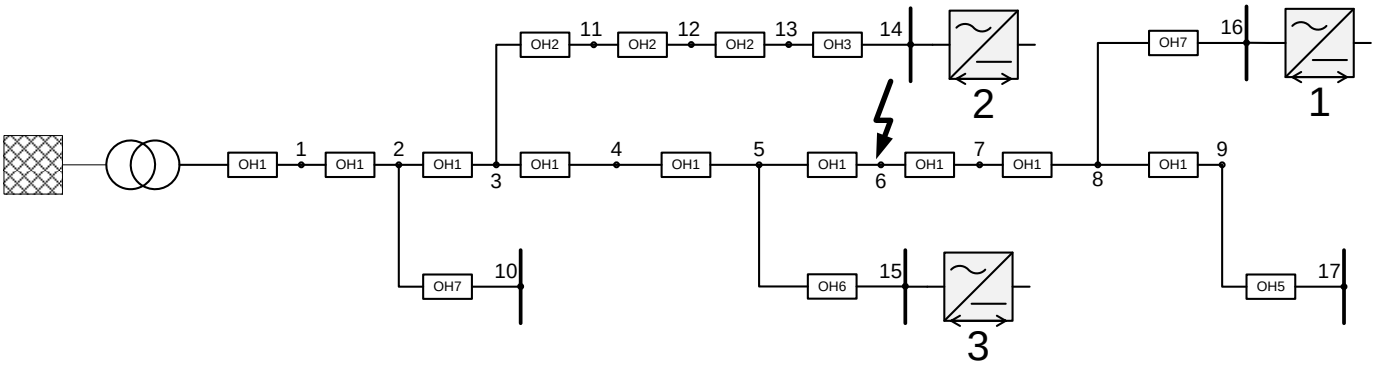

Figure 9. CIGRE European Low Voltage Residential Distribution Network Benchmark [7]

proposed to analyse networks containing multiple inverters, loads, and grid connection points. This allows protection engineers to continue using well known methods to find the fault current contribution of IIDG without the need of constructing full time domain models. Simulation in PSCAD and experimental results have been used to verify that the fault currents predicted by the analytical inverter fault models in MATLAB indeed are correct.

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