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Investigation of Plastic Package Related Failure Mechanisms in Plastic Encapsulated Integrated Circuits

by

Nicholas Mark Troop MSc. BSc. (Hons)

A Doctoral Thesis

Submitted in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy of Loughborough University of Technology.

9th May 1996.

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ABSTRACT

An experimental study has been conducted into the effects of package related failures in plastic encapsulated semiconductors. As a result of an extensive literature survey particular emphasis was placed on thermal and moisture related failure mechanisms. A number of accelerated life testing techniques including Highly Accelerated Stress Testing (HAST) were used to induced parameter drift and catastrophic failures. Examples of both insertion and surface mount package types were studied.

Observations were made on the parameter drift and catastrophic failure mechanisms of plastic encapsulated Bipolar Junction Transistors in dual in line packages. Gain degradation was observed to be the most sensitive parameter of those measured. It is proposed that this is a result of an increase in the extended surface depletion region area due to a degradation in the surface cleanliness. A theoretical analysis of the build up these traps is presented.

Package performance test chips were used to monitor the moisture resistance properties and thermal performance of Quad Flat Pack packages. Surface leakage path effects, corrosion onset and thermally induced stresses were monitored using this technique. A computer controlled measurement system was assembled for data acquisition and logging.

It is believed that these techniques will be of use in the investigation into the suitability of different package plastic styles for high reliability applications such as military and aerospace systems.
ACKNOWLEDGEMENTS

I would like to express my thanks to the following people for their help whilst conducting this research.

Firstly my colleagues at the International Electronics Reliability Institute in particular Jeff Jones for his invaluable technical advice and spontaneous brainstorming sessions over countless cups of tea. Mrs. Susan Dart for her help with such organisational aspects concerned with papers and conferences. Roger Tomlinson for reliability laboratory support. Rob Seager for his technical assistance and photography. My supervisor Mr. Joe Hayes for his advice.

Other members of the Departmental and University staff that have contributed to making this thesis possible; John Harry for his advice, encouragement and jokes. Frank Page for electron microscopy and EDX, Ann Jones for LIMA and advice on surface analysis techniques. The staff of the both the Electrical and Mechanical Departmental Workshops for all help and advice with the practical aspects of this research.

I would like to express my grateful thanks to the staff of several organisations external to LUT. In particular Mark Nichol of Mintec Semiconductors for his negotiations with the Malaysian packaging house which under took the encapsulation of the Package Performance Test Chips. Dr. Bob Newman of Lucas Electronics for conducting the leak testing of the Cerdip packages. Tony Howard of Towcester Technical Services for the acoustic microscopy. Ray Boorman of P.T.S. for his diligent regular service of our Hirayama autoclave and prompt expert attention in times of malfunction.

The late Professor Campbell the founder of I.E.R.I. whose vision made the Reliability Institute possible and the Professional Component Services division of the D.R.A. for sponsoring this research.

Finally my all my friends and family who have through their encouragement and support have boosted my determination. Especially my father and brother and in particular Amanda for putting up with me whilst I wrote up.
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List of Abbreviations

\( \alpha_r \) Base Transport Factor
A Ampere
a.c. Alternating Current
A_s Silver
A_j Area of Emitter-Base Junction
A_s Area of Space Charge Region Exposed to the Surface
Al Aluminium
A_u Gold
ASIC Application Specific Integrated Circuit
\( \beta \) d.c. Current Gain
BJT Bipolar Junction Transistor
Br Bromine
c Speed of light
C Celsius
Cl Chlorine
cm Centimetre
cte Coefficient of Thermal Expansion
CCD Charge Coupled Device
Cerdip Ceramic Dual in Line
Cl Chlorine
CMOS Complementary Metal Oxide Semiconductor
C-SAM Scanning Acoustic Microscopy
Cu Copper
CVD Chemical Vapour Deposition
DAC Digital to Analogue Converter
d.c. Direct Current
DGEBA Diglycidyl Ether of Biphenol A
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>ΔG</td>
<td>Gibb's Free Energy</td>
</tr>
<tr>
<td>D_{nβ}</td>
<td>Diffusion Coefficient of Electrons in Base</td>
</tr>
<tr>
<td>D_{pβ}</td>
<td>Diffusion Coefficient of Holes in Emitter</td>
</tr>
<tr>
<td>DID</td>
<td>Diffusion Induced Dislocation</td>
</tr>
<tr>
<td>DIL</td>
<td>Dual in Line</td>
</tr>
<tr>
<td>DIP</td>
<td>Dual in LIne</td>
</tr>
<tr>
<td>DoD</td>
<td>Department of Defence (US)</td>
</tr>
<tr>
<td>DRA</td>
<td>Defence Research Agency (U.K.)</td>
</tr>
<tr>
<td>DRAM</td>
<td>Dynamic Random Access Memory</td>
</tr>
<tr>
<td>e</td>
<td>Electron</td>
</tr>
<tr>
<td>E</td>
<td>(e.m.f) Electro-Motive Force</td>
</tr>
<tr>
<td>γ</td>
<td>Emitter Efficiency</td>
</tr>
<tr>
<td>E_a</td>
<td>Activation Energy</td>
</tr>
<tr>
<td>E^o</td>
<td>Standard Oxidation Potential</td>
</tr>
<tr>
<td>ECL</td>
<td>Emitter Coupled Logic</td>
</tr>
<tr>
<td>EDX</td>
<td>Energy Dispersive X-ray</td>
</tr>
<tr>
<td>EED</td>
<td>Emitter Edge Dislocation</td>
</tr>
<tr>
<td>EOS</td>
<td>Electrical Overtress</td>
</tr>
<tr>
<td>EPROM</td>
<td>Erasable Programmable Read Only Memory</td>
</tr>
<tr>
<td>ERA</td>
<td>Electrical Research Association (U.K.)</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
</tr>
<tr>
<td>eV</td>
<td>Electron Volt</td>
</tr>
<tr>
<td>F</td>
<td>Faraday Constant</td>
</tr>
<tr>
<td>Fe</td>
<td>Iron</td>
</tr>
<tr>
<td>FIC</td>
<td>Film Integrated Circuit</td>
</tr>
<tr>
<td>FIT</td>
<td>Failures in 10⁹ Hours</td>
</tr>
<tr>
<td>GaAs</td>
<td>Gallium Arsenide</td>
</tr>
<tr>
<td>H</td>
<td>Hydrogen</td>
</tr>
<tr>
<td>HCMOS</td>
<td>Highspeed Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>h_{FE}</td>
<td>Hybrid Parameter - Forward Gain in Common Emitter Configuration</td>
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<tr>
<td>HAST</td>
<td>Highly Accelerated Stress Test</td>
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<tr>
<td>HP</td>
<td>Hewlett Packard</td>
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</table>
g  Gramme
GPIB  General Purpose Instrument Bus
HIC  Hybrid Integrated Circuit
HPP  High Performance Packaging
I_B  Base Current
I_C  Collector Current
I_E  Emitter Current
I_CBO  Collector Base Leakage Current
I_CEO  Collector Emitter Leakage Current
IC  Integrated Circuit
IDC  Insulation Displacement Connector
I/O  Input / Output
IRPS  International Reliability Physics Symposium
J  Joule
JEDEC  Solid State Products Engineering Council
k  Boltzmann's constant
K  Kelvin
Kg  Kilogramme
\lambda  Failure Rate
L.I.M.A.  Laser Ionisation Mass Analysis
LCC  Leaded Chip Carrier
Li  Lithium
M  Mega (10^6)
MCM  Multi Chip Module
MESFET  Field Effect Transistor
MIL-STD  Military Standard (USA)
m  Metre
mm  Millimetre
MOS  Metal Oxide Semiconductor
MOSFET  Metal Oxide Field Effect Transistor
MOST  Metal Oxide Transistor
NMRC National Microelectronics Research Centre (Ireland)
MSFC Marshall Space Flight Centre
MTBF Mean Time Between Failures
N Newton
Na Sodium
$N_A$ Concentration of Acceptors in Base
$N_D$ Concentration of Donors in Emitter
$n_i$ Intrinsic Carrier Density
$N_0$ Initial Number of Components
$N_f(t)$ Number of Components Failed After Time $t$
$N_s(t)$ Number of Components Surviving After Time $t$
$N_T$ Trap Density in Bulk
$N_s$ Trap Density at Surface
nA Nano-amp
NMOS n-channel Metal Oxide Semiconductor
O Oxygen
$\Omega$ Ohm
P Phosphorous
pA Pico-amp
p.p.b. Parts Per Billion
p.p.m. Parts Per Million
PC Personnal Computer
PCB Printed Circuit Board
PGA Pin Grid Array
PLCC Plastic Leaded Chip Carrier
PMOS p-channel MetalOxide Semiconductor
ppm Parts Per Million
PSG Polysilicate Glass
psu Power Supply Unit
PTFE Polytetrafluoroethylene
QFP Quad Flat Pack
$\pi_{ij}$ Piezo resistive Coefficient
R  Gas Constant
RADC  Rome Air Development Centre
RH  Relative Humidity
R(t)  Reliability Function
RTV  Room Temperature Vulcanising
\( \sigma_x \)  Normal Stress
\( \sigma \)  Capture Cross Section for Electrons and in the Bulk
\( \sigma_s \)  Capture Cross Section for Electrons and Holes at Surface
\( \sigma_T \)  Base Transport Factor
SEM  Scanning Electron Microscopy
SIL  Single in Line
SMD  Surface Mount Device
SMT  Surface Mount Technology
SOP  Small Outline Package
T  Absolute Temperature
\( \tau \)  Shear Stress
\( T_g \)  Glass Transition Temperature
Ti  Titanium
t_{sat}  Time to Saturation
TAB  Tape Automated Bonding
THB  Temperature Humidity & Bias
TTL  Transistor-Transistor Logic
V-SOP  Very Small Outline Package
\( \mu m \)  Micron
US  United States
V_{ce}  Voltage Collector Emitter
VHF  Very High Frequency
VHSIC  Very High Speed Integrated Circuit
VLSI  Very Large Scale Integration
\( v_{th} \)  Thermal Velocity of Electrons and Holes
W  Tungsten
\( W_B \)  Base Width
\( W_E \) \hspace{1em} \text{Emitter Width} \\
\( W_{EB} \) \hspace{1em} \text{Width of Emitter-Base Depletion Region} \\
\( x_{ds} \) \hspace{1em} \text{Thickness of Field Induced Space-Charge Region at the Surface} \\
\( ZIF \) \hspace{1em} \text{Zero Insertion Force}
CHAPTER 1

INTRODUCTION

1.1 Historical Perspective

The invention of solid state electronic devices has been one of the major innovations of the 20th century. It has been responsible for major advances in telecommunications and computing that has lead to the Information Technology Revolution. The consequences of which are still being felt in many aspects of western life.

The history of semiconductor active devices began in 1947 which Shockley, Baedeen and Brattain successful fabrication of the first "transfer resistor" or transistor as it became known. This early form of semiconductor amplifier was known as the point contact transistor and was fabricated from germanium. The possibilities of amplification with semiconductor materials had been realised several decades earlier. Lillienfield had filed a number of patents during the 1920's for devices whose principles of operation were similar to the modern MESFET and MOSFET but he had been unable to demonstrate an operating device.

Initially the packaging technology used to package these new amplifying devices made use of the same techniques and materials as those employed in thermionic device packages. Early commercial transistors such as the OC71 had their germanium dies encapsulated in glass envelopes with the terminating leads brought out through the glass base. As the demand from the domestic electronics industry grew for low cost semiconductors cheaper alternatives were developed for semiconductor device packaging. The breakthrough in this area was the invention of the transfer moulded plastic package. In this technique the die and leads are encapsulated in a plastic resin which is moulded at high pressure and temperature around the device. Packages of this type are not considered as being hermetic but are considered to
provide many years of useful device life under benign conditions, and are thus ideal for consumer applications.

The invention of the Integrated Circuit (I.C.) was the next major step in the development of microelectronics. Instead of fabricating a single transistor per die many transistors were fabricated simultaneously, in this way whole circuits could be produced on one piece of silicon. This had the effect of reducing both the cost and size of electronic equipment and, as internal device connections are more reliable than those at the board level, increased reliability.

Plastic package styles were developed that meant that the cheap transfer moulding technique could be employed to encapsulate I.C.s. This technique has since been developed to the point where it is now used to package almost all plastic encapsulated devices from transistors to complex integrated circuits such as microprocessors and application specific integrated circuits (A.S.I.C.s).

1.2 Trends in Integrated Circuit Development

Since the introduction of the first I.C.s there have been several clearly observable trends in the development of microelectronic devices. These are all due to the ever increasing level of integration of active devices within I.C.s. This trend towards increased integration has greatly reduced the size of devices and has been the stimulus for the development of ever smaller package styles. In addition to the trend for miniaturisation, a phenomenal reduction in cost has occurred along side an incredible increase in the level of complexity. This has lead to an explosion in the number of applications to which the technology can be cost effectively applied.

A key element in this revolution has been the ability to develop packages for these every more complex devices that meet the technical requirements at low cost. This has been possible because of developments in materials science, assembly, and processing techniques.

Predictions of the future complexity and reliability of VLSI devices [1][2] suggest that by the turn of the century devices with over 100 million transistors will be in production. This increase in the level of integration, is illustrated in Figure 1 (after Rymaszewski et al. [3]) which shows the increase in the number of logic gates.
per chip over the last twenty years. For example the storage capacity of Dynamic
Random Access Memories (D.R.A.M.s) has increased one thousand times from 4 kilo-
bytes in 1973 to 4 mega-bytes over twenty years.

This drive for ever greater integration has had its consequences at the package
and board level that have manifested themselves in the following ways;

*Increase in Number of I/O Terminals* - As the number of gates per chip increased so
did the requirement for increasing the number of terminals to the device. This has
required that packages with an ever increasing number of terminals be developed.
Figure 2 [4] illustrates the increase in the number of electrical connections with date.

![Figure 1 Increase in the Level of I.C. Integration (After Rymaszewski et al [3])](image)

*Decreased Bondpad Spacing* - To meet the requirements for increased input/output
connections (I/O) the spacing between bondpads on the chip has had to be reduced.
This places ever more stringent requirements on the accuracy of the bonding process.
Figure 2 The Increase in the Number of Terminations per I.C. (After Tummala et al. [4])

Decreased Track Width - To accommodate the increased number of gates possible on a single semiconductor die the width of the interconnecting metallisation tracks has deceased. As a consequence of the reduction in I/O spacing and the general increase in board complexity the copper tracks on printed circuit boards has also had to become finer. The extent of the decrease in track width for both these interconnect mediums is shown in Figure 3 [5].

Reduction in Package Thickness - As the density of gates per die has increases so has the concentration of I.C.s on PCBs. Many new products, particularly mobile phones and lap top personnel computers, consist of several boards closely sandwiched together. Products such as these demand low profile components and consequently very thin packages have been developed such as the Quad Flat Pack (QFP) and Very Thin Outline Package (V-SOP).
1.3 Improvements in Package Reliability

These trends have set rigorous demands on IC package performance. Improved performance in terms of reliability has come about by the improvements in materials and processes. The trend towards increasing integration with its need for ever decreasing feature size, increased circuit complexity and high I/O count of newly introduced package styles could be expected to contribute towards a decrease in reliability of I.C.s. During the same period the processes and materials used in the packaging of plastic encapsulated semiconductors have improved greatly such that, as is shown later, the general picture is one of continued improvements in reliability.
1.4 Study Synopsis

The work presented in this thesis relates to a study of environmental effects on plastic encapsulated devices. Accelerated life testing techniques were employed so that both parametric drift and catastrophic failures could be studied in standard I.C.s. The processes that cause this degradation was observed by employing package performance test chips specially encapsulated in industry standard packages.

The thesis consists of six chapters a brief description of each is given below.

Chapter 1 - This chapter describes a brief history of the major innovations in electronics and outlines the role played by device packaging in the success of microelectronics. It outlines how packaging technology has had to develop for the improvements in device performance to be realised economically.

Chapter 2 - This chapter states the functions of packaging and discusses the requirements and the considerations in their design. The types of package available are briefly reported. A full description of the materials and processes used in plastic package fabrication are given together with a brief description of alternative types.

Chapter 3 - In this chapter the failure mechanisms of I.C.s are presented and discussed with particular emphasis on those associated with the use of plastic encapsulations. The use of accelerated life testing techniques for reliability assessment of package related failure mechanisms is presented. In particular elevated temperature and humidity techniques such as the 85°C/85% relative humidity test and Highly Accelerated Stress Testing (HAST) are covered. A survey of reported reliability is presented along with an analysis of the reasons for the improvements observed in plastic package performance over the last two decades.

Chapter 4 - Describes a series of accelerated life test experiments on plastic encapsulated bipolar transistor arrays designed to induce package related failure mechanisms. Observations of parameter degradation, in particular d.c gain, were reported and an explanation of the degradation mechanism was proposed. Later
catastrophic failure mechanisms were observed and failure analysis was undertaken to identify the failure mechanisms.

Chapter 5 - This chapter describes the use of package performance test chips to measure the physical conditions experienced at the die of plastic package devices that are subjected to accelerated life testing. The particular processes monitored were moisture ingress by leakage resistance measurements, track corrosion of passivated and un-passivated structures, and package related mechanical stress. The stress experienced by the die as a result of differential thermal expansion between package materials was measured using on chip piezo-resistive gauges.

Chapter 6 - A mathematical description of the gain degradation observed in bipolar junction transistors due to exposure at high temperature and humidity is presented. An explanation of the moisture ingress process is suggested along with a mathematical description of its dependence on exposure time. A possible model for the package related stress measured by piezo-resistive stress sensors encapsulated in plastic Quad Flat Pack packages is discussed.

Chapter 7 - This chapter contains the conclusions of this study and suggestions for further work.

1.5 References


1-7
CHAPTER 2

ELECTRONIC PACKAGES

2.1 Introduction

The process by which the silicon die of a semiconductor is protected, mounted and interconnected to other components in any equipment is a complex process with several levels of packaging required for the device to be integrated into a working system. These levels are often referred to as a packaging hierarchy. This hierarchy begins with the encapsulation of the die into a device package for protection and interconnection. This is considered to be the first level of packaging. Many of these packages are then mounted onto printed circuit boards or substrates where electrical interconnections and made between them. This card level interconnection is considered to be the second level of the packaging hierarchy. The third level is where several of these cards are connected together, usually by plugging them into motherboards or backplanes, and the forth level is the assembly of the mother-boards or backplanes into a box or cabinet. The content of this thesis is concerned solely with the packaging of the semiconductor chip into a device package and its affect on reliability, the so-called first level of the packaging hierarchy.

2.2 Package Function

The package of an electronic device forms a barrier between the electronic device and the hostile outside world. It perform a number of functions which are; Power Distribution, Signal Distribution, Heat Dissipation and Circuit Protection.
Power Distribution - The package must provide an electrical connection from the outside world and distribute the required power supplies to the appropriate connections on the die.

Signal Distribution - The package must provide electrical connections to and from the die to the outside world, often referred to as input/output connections or simply I/O.

Heat Dissipation - The package has to provide a path for the heat produced at the die by its operation and to transfer it to the outside world. The heat is dissipated at the package surface by a combination of radiation, conduction or convection.

Circuit Protection - The package has to provide protection to the die and its bonding wires from mechanical damage such as impact, scratching, and abrasion. It also provides strength and rigidity to the die. It must also protect the die from moisture and chemical attack by corrosive vapours or liquids. In some applications the package would have to screen the device from light or other wavelengths of electro-magnetic radiation. In addition the package also provides a means of device identification; part number, date code, batch number, manufacturer etc, and also a means of indicating orientation in the circuit for connection, and assembly. They also facilitate device handling during the assembly of boards and device testing.

2.3 Package Requirements and Considerations

In designing a package to provide the four functions described above several considerations have to be taken into account.

Electrical Connection - Not only should the package provide all necessary electrical connections to the outside world it must also provide the connections in such a way as to be able to withstand the magnitude of all voltages and current experienced during normal operation and with suitable impedances. It must do this within the limits of acceptable propagation delays and crosstalk. The connections should be presented in such away as to make electrical connections compatible with other devices and the
mounting substrate or boards.

*Process Considerations* - The package should be compatible with manufacturing constraints and considerations. For example plastic resins, if used, should have cure times which are compatible with the other production requirements.

*Cost* - The packaging technique must not unduly effect the cost of the finished devices. It should be appropriate and consistent with the device's intended market. For example the moulded plastic packages used in the highly competitive consumer electronics market are considerably cheaper to produce than their hermetic counterparts used in military and aerospace applications.

*Environmental Considerations* - The device package must be capable of providing the necessary environmental performance and protection across the whole of the operating temperature range in the presence of high levels of humidity, chemical solvents, vibrations, shock and radiation. These requirements should be met without degradation of the package. For example all the constituent materials in the device and package should have closely matched coefficients of thermal expansion (c.t.e) so as to avoid package cracking or delamination or damage to the die during thermal cycling.

*Signal Propagation Delay* - Increasingly in High Performance Package (HPP) applications, used for high-speed digital circuits, the propagation delay between the die and the device pins is an ever more important consideration. Much of the impetus for high performance packaging has come from the defence and computer industries. Layden [1] reports on the VHSIC (Very High Speed Integrated Circuit) programme of the US DoD. These applications require packages with very high I/O counts (>200) and small propagation delays (<1 ns). An excellent review of the current state of High Performance Packaging (HPP) is given in [2].

*Reliability* - The package must impart to the integrated circuit a level of reliability consistent with the application and cost of the device. For this reason applications where high reliability is paramount, such as aerospace applications, use hermetic
packages devices with full traceability on all components and materials. Non safety critical systems however, such as domestic video recorders, exploit cheap packaging technologies of allegedly lower reliability.

2.4 Package Types

The need to satisfy the often contradicting requirements of electronic package design have lead to the large range of package types and styles. There are two methods of connecting semiconductor packages to boards. The insertion of pins through the board via mounting holes, where the package's electrical connections are made via pins, which are inserted through the printed circuit board and are soldered on the opposite side of the board to the package. The other method of mounting is surface mount where the devices are terminated in pads which are soldered to the same side of the board as the package. Surface mount technology is rapidly growing in popularity in consumer and small systems markets. It has a number of advantages over through-hole technology. The packages can be produced with pads at the very tightest of spacings (0.65mm), thus allowing more electrical connections per unit area of the package. This also allows a greater packing density of devices on printed circuit boards, thereby lowering the cost and size of the system. The higher packing density is accompanied by problems with heat dissipation, increased cross-talk and difficulties with the reworking of boards. This technology is expected to continue to increase its share of the market.

2.4.1 Insertion Mounted Packages

The insertion mounted or through-hole package is the oldest example of integrated circuit packaging. Originally introduced as the Dual-in-Line package, it has dominated the through hole market. With the drive towards ever increasing packaging densities of devices onto boards, smaller packages with less plastic surrounding the die has been developed. Several different styles of package are available in this package technology as illustrated in Figure 1 and Table 1.
Figure 1 Insertion Mounted Packages
## Table I Insertion Mounted Package Styles

<table>
<thead>
<tr>
<th>Package Style</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual-In-Line Package (DIP)</td>
<td>Most popular and oldest package style in common use. Rectangular package with leads originating from the two longest sides. Lead counts from 8 to 64 with 28 to 40 leads being used for processor and VLSI applications 14 to 20 lead for memory devices and logic devices.</td>
</tr>
<tr>
<td>Shrink-DIP (SH-DIP) &amp; Skinny-DIP (SK-DIP)</td>
<td>Similar to DIP packages but occupying an exceptionally small surface area. This is achieved by using a fine lead pitch, special leadframe design, and an extra thin plastic moulded body.</td>
</tr>
<tr>
<td>Single-In-Line (SIP)</td>
<td>The SIP package uses only a single row of leads from one side of the package. This style of package sits perpendicular to the board and so occupies little board area. This allows the use of a heatsink with this package. Used for DRAMs, audio power amplifiers and SIL resistor packs.</td>
</tr>
<tr>
<td>Zig-Zag In-Line (ZIP)</td>
<td>A variation on the SIP package where the leads emerge staggered in a zig-zag pattern. This increases the lead density in a given linear distance. Popular in consumer applications for audio amplifier and switching circuits as it can be mounted to a heatsink.</td>
</tr>
<tr>
<td>Pin Grid Array (P.G.A.)</td>
<td>In the style of package the electrical connections are made via pins mounted on the underside of the package. It is frequently implemented as a ceramic package with the die located in a cavity in the centre. Electrical interconnection between pins and cavity is made by a metallised fan-out pattern fired into the ceramic material.</td>
</tr>
</tbody>
</table>
2.4.2 Surface Mounted Packages

The need for high component densities, which led to the development of surface mount components, has been the driving force behind the creation of a range of package styles for this technology. Some examples of this type of package are shown in Figure 2. The significant parameters of the packages discussed are summarised in Table II.

Figure 2 Surface Mount Packages
### Table II: Surface Mount Package Styles

<table>
<thead>
<tr>
<th>Package</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small Outline Package (SOP)</td>
<td>Commonly referred to by the acronyms SO, SOP, SOIC. Available with lead counts from 8 to 28 leads, and are used for SSI, MSI and analogue devices. Their compactness is achieved by employing a fine lead pitch, and an exceptionally small amount of moulding compound.</td>
</tr>
<tr>
<td>Leadless Chip Carrier (LCC)</td>
<td>DIL &amp; SOP packages are inefficient in use of board area once their I/O count &gt;48 therefore the chip carrier was developed. Packages of this general style, with leads on four sides rather than two, are known as quads. The chip carrier is available in ceramic, as a leaded chip carrier (LCC) with J-leads, or a leadless chip carrier (LLCC) with solder pads. Ceramic leadless chip carriers are available in 28 to 156 lead versions (JEDEC A &amp; B packages, 1.27mm lead spacing) and with 16 to 96 leads (JEDEC C packages, 1.00mm lead spacing).</td>
</tr>
<tr>
<td>Plastic Leaded Chip Carrier (PLCC)</td>
<td>The plastic chip carrier is the most common of the quad packages and are available with lead counts from 20 to 90, a smaller range than their ceramic counterparts. They are terminated with J-leads at a pitch of 1.3mm.</td>
</tr>
<tr>
<td>Quad Flat Pack (QFP)</td>
<td>The QFP is the fine-pitch thin-body version of the LCC. The leads are of the gull-wing variety as opposed to the J-lead of the PLCC and the package can be of either plastic or ceramic. QFPs are available in two designations; the JEDEC version with bumpers, (corner projections designed to help protect package leads) and metric leads pitches of 1.0, 0.8, and 0.65mm, and the EIAJ version (without bumpers) with a lead pitch 0.65mm.</td>
</tr>
</tbody>
</table>
Table III Parameters of Common Integrated Circuit Packages

<table>
<thead>
<tr>
<th>Package Style</th>
<th>I/O Count</th>
<th>Material</th>
<th>Lead Pitch</th>
<th>Package Thickness (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP</td>
<td>8-64</td>
<td>C,P</td>
<td>100MIL (2.54mm)</td>
<td>3.3</td>
</tr>
<tr>
<td>S-DIP</td>
<td>20-64</td>
<td>P</td>
<td>70MIL (1.778mm)</td>
<td>1.5</td>
</tr>
<tr>
<td>SK-DIP</td>
<td>24-32</td>
<td>C,P</td>
<td>100MIL (2.54mm)</td>
<td>2.3</td>
</tr>
<tr>
<td>SIP</td>
<td>3-25</td>
<td>P</td>
<td>100MIL (2.54mm)</td>
<td>3.3</td>
</tr>
<tr>
<td>ZIP</td>
<td>16-24</td>
<td>P</td>
<td>100MIL (2.54mm)</td>
<td>3.3</td>
</tr>
<tr>
<td>PGA</td>
<td>64-312</td>
<td>C,P</td>
<td>100MIL (2.54mm)</td>
<td>2.3</td>
</tr>
<tr>
<td>SOP</td>
<td>8-40</td>
<td>P</td>
<td>50MIL (1.7mm)</td>
<td>1.4</td>
</tr>
<tr>
<td>LCC</td>
<td>44-132</td>
<td>C</td>
<td>50 &amp; 25MIL (1.27 &amp; 0.65mm)</td>
<td>2.15</td>
</tr>
<tr>
<td>PLCC</td>
<td>28-144</td>
<td>P</td>
<td>50 &amp; 25MIL (1.27 &amp; 0.65mm)</td>
<td>3.0</td>
</tr>
<tr>
<td>QFP</td>
<td>84-288</td>
<td>P</td>
<td>1.00, 0.8, 0.65mm</td>
<td>2.15</td>
</tr>
<tr>
<td>SOJ</td>
<td>20-32</td>
<td>P</td>
<td>50MIL (1.27mm)</td>
<td>2.7</td>
</tr>
</tbody>
</table>

2.5 Package Properties

When integrated circuits first became commercially available their cost was, allowing for inflation, considerably higher than today. Therefore was it justified that high quality packaging techniques were used for this new high cost technology. Hermetic packaging techniques using glass metal seals were well established in the packaging of electronic valves. The first semiconductor packages were of the metal can variety with electrical connection made via wires fed through glass-metal seals. This is a highly effective encapsulation method providing very good hermetic properties, however it is relatively expensive. Later a cheaper alternative, the CERDIP package, which exploited developments in ceramic technology, became available. This type of package, which employs a ceramic plate sandwich, relies on a metal-ceramic seal. These packages are considered hermetic but are cheaper to produce than their metal can counterparts. Both these techniques provide high levels of reliability (despite...
early problems with out-gassing of moisture in CERDIPs [3]) and are almost exclusively used in systems where high reliability is of paramount importance such as in military and aerospace applications. Ceramic packages are also extensively used for packaging devices with high dissipation where the heat generated in operation would raise the package temperature above that which can be safely handled by the equivalent plastic package. Applications, where heat developed in the operation of the integrated circuit could be too great for plastic encapsulation components, are; fast microprocessors, floating point co-processors and certain digital signal processing devices.

The growing introduction of semiconductor devices into consumer electronics during the nineteen sixties, led to a requirement for low-cost devices for this highly competitive sector of the electronics industry. This requirement was the driving force behind the development of the low cost plastic package. The plastic package satisfies the requirements for semiconductor packaging although it is not considered to be hermetic. Worries over their reliability in high humidity environments have been expressed for many years [4][5][6][7][8][9]. Despite thirty years of continuing development doubts remain over their reliability and so they are prohibited by the US DoD for use in military applications.

Comparison of package properties, in particular gas permeation, shows the metal can and ceramic packages to be superior. The rate of moisture permeation through different materials is shown in Table IV [10]. One of the major functions of the package is to protect the device from the effects of moisture. Moisture, especially if contaminated with certain ionic species (Cl-, Br-) is a source of corrosion in electronic packages, other failure mechanisms associated with the presence of moisture are electro-oxidation and metal migration. The rate of moisture diffusion into the package depends on the packaging material and process. The materials used can be divided into two types: plastics, such as epoxy-novolac resins, silicones, and polyimides, and hermetic materials such as glass, metal and ceramics.
Table IV Rates of Moisture Permeation for Materials used in Electronic Packaging

<table>
<thead>
<tr>
<th>Material</th>
<th>Diffusion Rate (g/cm second Torr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicone</td>
<td>$10^{-6}$</td>
</tr>
<tr>
<td>Epoxies</td>
<td>$10^{-10}$</td>
</tr>
<tr>
<td>Glasses</td>
<td>$10^{-14}$</td>
</tr>
<tr>
<td>Metals</td>
<td>$10^{-16}$</td>
</tr>
</tbody>
</table>

2.6 Plastic Encapsulation

The word plastic is defined by the Oxford English Dictionary as "Any of a large and varied class of substances which are polymers of high molecular weight based on synthetic resins or modified natural polymers and maybe obtained in a permanent or rigid form following moulding, extrusion, or similar treatment at a stage during manufacture or processing when they are mouldable or liquid." [11]. Today plastic is used as a generic term for a range of man-made organic polymers. One of the earliest applications of plastics was in electrical equipment where they rapidly exploited for their good electrical insulating properties. The first commercial transistors were encapsulated in hermetic packages but by the late fifties they were available in the first plastic packages, known as the "glob top". In this package the die was attached to a ceramic header and was wirebonded to its leads. A drop or "glob" of epoxy resin was then placed over the die to protect it. In the early nineteen sixties integrated circuits became available. These were initially encapsulated in a package known as the "flat-pac". This was a rectangular box of metal, glass, or ceramic. The die was bonded, wired and sealed into a central cavity. These packages had to be surface mounted onto the printed circuit board. At the time assembly technology was not very advanced and these packages had to be hand soldered to printed circuit boards. It is ironic that this initial form of mounting known as "surface mount" is now
becoming the dominant assembly technology due to advances in handling and mounting processes. This package style was soon superseded by the DIP which, like most other PCB components of the time, were through-hole mounted. This meant that one soldering process could be used for both integrated and discrete components. Early DIPs, like their flat-pac counterparts, were available solely in metal, glass and ceramic packages.

The next step in the development of the IC package was the introduction of the plastic dual-in-line package. This was a major break-through as it led to significant cost savings and used inexpensive materials, and mass production techniques in its assembly. All the moulded plastic packages available today (SOPs, QFPs and PLCCs) all use a similar construction to the DIP, and share several common features; a die bonded to a leadframe, wire bonds between the die and leadframe, and a moulded plastic coat over the whole assembly. The purpose of the component parts of a moulded plastic IC package (metal leadframe, die bonding material, die, gold bonding wires, plastic moulding material) will now be explained.

The components of the dual-in-line package are shown in the cut-away view Figure 3.

![Figure 3 Cut-Away View of a Plastic Dual-In-Line Package](image)

The function of these components is as follows;

*The leadframe* - This the central supporting structure which forms the backbone of the package to which every other element of the package is attached. It is stamped out of
thin sheet metal and forms the "paddle" which supports the die. The region of the leadframe that is not covered with moulding compound is bent to form the legs of the package that make electrical connections with the circuit board, or substrate.

*The die bonding material* - Bonded to the leadframe's central platform or paddle is the die. This is the silicon chip on which is fabricated the microcircuit. It is this delicate device that the device package serves to protect and connect to the outside world. It is bonded to the leadframe either by silicon/gold eutectic bonding or with a die bonding compound, usually a conducting polymer adhesive, such as silver-filled epoxy or polyimide adhesive paste.

*The die* - The die is usually a square of silicon or gallium arsenide anything from 1mm to 10mm square. It's thickness is usually 250 or 400 microns. The surface is protected against light scratching, abrasion and chemical attack by a passivation layer. This is either silicon dioxide doped with 2% phosphorus, or silicon nitride. Holes are left in the passivation layer around the bonding pads so that bond wires may be attached.

*Bonding wires* - Electrical connection between the die and leadframe is accomplished by thin gold or aluminium bonding wires. Typical bond wire diameters are 25 microns to 32 microns for gold and 50 microns for aluminium. Gold wire can be bonded by thermo-compression, ultrasonic, or thermosonic methods. Aluminium however can only be ultrasonically bonded. In gold wire bonding, the bond at the die's bond pad is usually formed by flame softening the tip of the wire and then pressing it against the bondpad. The wire is looped out and formed into a wedge bond on the leadframe finger. Aluminium wire bonding requires both wedge bonding on pad and lead finger. This process is automated today and typical bonding rates are as high as 200 per minute. Bond lengths and loop heights are carefully controlled from 1.5 to 3.0mm in length. Loop heights as high as 0.75mm above the plane of the device are possible.
**Plastic moulding compound** - The whole structure is protected by a covering of a thermoset plastic by a process known as transfer moulding. The chip and bonded leadframe assemblies are loaded into a mould where hot liquid moulding compound from a reservoir is forced over them. The equipment used for this process is known as a transfer moulding press. The moulding plastics come from a family of organic polymers known as Epoxy Novolacs. These compounds are solid at room temperature, have high cross-linking density and functionality. High cross-linking density gives the resin a low moisture-absorption rate (for a plastic) and high functionality imparts heat stability and a correspondingly high glass transition temperature. The resin is only part of the moulding compound (25.5-29.0%) other constituents are inert filler (68-72%), flame retarder (2%), colourant (0.5%), mould-release agent, and trace amounts of compounds to promote and accelerate curing.

The constituent materials of a moulded plastic package will now be discussed along with the compromises that are involved in the selection of these materials.

2.6.1 Leadframe Materials

The leadframe has many purposes; it serves as a holding fixture during package assembly, as a chip attach substrate, as a support matrix on to which the plastic may key, and as an electrical and thermal conductor from the die to the board. Many leadframe materials are available and selection depends on a number of factors including, cost, manufacturing considerations, thermal conductivity, etc. In general there are three classes of leadframe material. The physical properties of several common leadframe materials are shown in table Table V.

**Nickel-Iron Alloys** - This is the most widely used form of leadframe material and was originally developed for use as a glass-seal alloy for the pin material of vacuum devices. It is an alloy consisting of 42% nickel and 58% iron, hence its name, Alloy 42. Its c.t.e. is very close to that of silicon making it an excellent choice for paddle material. Furthermore it may be heat treated to obtain optimum tensile strength and ductility for the stamping and lead-forming operations. It can also be plated or solder-dipped without a nickel barrier but it has the draw back of relatively low thermal conductivity.
Table V The Physical Properties of some Typical Leadframe Materials

<table>
<thead>
<tr>
<th>Leadframe Material</th>
<th>Alloy 42</th>
<th>Kovar</th>
<th>Alloy 151</th>
</tr>
</thead>
<tbody>
<tr>
<td>Composition</td>
<td>Iron 58%</td>
<td>Iron 53%</td>
<td>Copper 99.9%</td>
</tr>
<tr>
<td></td>
<td>Nickel 42%</td>
<td>Nickel 53%</td>
<td>Zirconium 0.1%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cobalt 17%</td>
<td></td>
</tr>
<tr>
<td>Thermal Conductivity W/m°C</td>
<td>15.89</td>
<td>17</td>
<td>359.8</td>
</tr>
<tr>
<td>Electrical Conductivity (μΩ cm)</td>
<td>52</td>
<td>47</td>
<td>1.7</td>
</tr>
<tr>
<td>Linear Expansion (10^-7/°C)</td>
<td>43</td>
<td>53</td>
<td>177</td>
</tr>
</tbody>
</table>

**Clad Materials** - These materials were developed to produce the desirable mechanical properties of Alloy-42 whilst increasing its poor thermal conductivity. Thermal conduction along the leadframe to the board is an important method of heat flow from the die to the printed circuit board. Increasing the leadframe conductivity increases the amount of heat that can safely be dissipated in the device. Clad materials are fabricated by rolling copper foil onto a stainless steel strip under high pressure and annealing the composite to form a solid weld.

**Copper Alloys** - Copper has excellent thermal and electrical conductivity properties making it an increasingly popular choice for high dissipation devices in plastic packages. Its c.t.e. is considerably greater than that of silicon which can cause stresses in the package and even chip failure. Copper alloys have been developed to overcome this problem [12]. Another consideration is that the c.t.e. of copper and silicon are so dissimilar that silicon/eutectic bonding cannot be used. This has led to the development of silver-filled epoxies and polyimide chip-attach adhesives which are flexible enough to absorb the strain developed between the die and leadframe over the operating temperature range of the IC.
2.6.2 Leadframe Design

Consideration has to be given to a number of factors in leadframe design. For ease of manufacture, leadframes are either stamped or etched from a rolled strip. The strip is typically 0.25mm thick, but can be thinner on high pin-out packages such as PLCCs. Stamping is the major method of fabrication as unit costs are cheaper than etching, although the initial tooling costs of stamping are far greater.

The design of the leadframe has to take into account not only its role as part of the package but must also consider its role in package assembly. Along the edges of the leadframe are located tooling holes which mate with transfer-mechanism pins that are part of the assembly equipment such as chip bonders, wire bonders and trim and form equipment. The leadframe must also exhibit some lead locking and moisture ingress inhibiting features. Anchor holes are stamped through the leadframe pins inside the package to lock the leads into the cured moulding compound. Other locking and moisture ingress prevention features are included such as anchor ears where the leadframe pins are flared out [13].

In designing the leadframe consideration has to be given to the problem of stress relief. Two forms of stress are present at the leadframe. Firstly stress due to the mismatch in the coefficients of thermal expansion of the plastic moulding compound and the metal leadframe. In severe cases thermal shock can cause bending of the package which induces stresses that can cause malfunction the of device. Obviously the larger the die, die paddle, leadframe and package the greater the stress. The other stress concentration points are located on the bottom edges of the leadframe. When the stamping punch forms the leadframe there is a tendency to form a burr along the bottom edge. The burrs are sharp and act as stress concentrators. The high stress concentrations can cause cracking that may propagate from the leadframe to the underside of the package providing a moisture ingress channel. The burring can be removed by using coining equipment after the stamping process where the burr is forged into an edge chamfer.

Another purpose of the leadframe is to support the plastic moulding compound while the package is formed. The ability to inhibit water penetration along the plastic/leadframe interface is a function of plastic shrinkage around the metal leadframe members. Generally the more plastic coverage, the greater will be the
compressive forces. An ideal plastic to metal ratio for leadframe design is given by

\[ \frac{A_m}{A_p} \leq 1 \]  

(1)

The leadframe also provides the thermal path that will connect the package to the printed circuit board. There are four lead configurations used on moulded plastic packages: Integral standoff, gull wing, J-bend, and butt joint. The standoff lead is used in DIP packages, and the others in surface mount.

### 2.6.3 Die Bonding

Die bonding, or chip attach, is the method by which the silicon die is anchored to the paddle of the leadframe. This can be either by silicon gold eutectic bonding, polymer bonding by adhesives or by silicone gels.

Silicon/gold eutectic bonds are often used in the bonding of dies to Alloy-42 leadframes. A small square of silicon/gold alloy is cut from a feed ribbon and transferred to the chip support platform. An optical scanner detects a good chip on the sawn wafer causing a probe to push the chip above the wafer plane where a collet picks it up, and transfers it to the heated chip support platform. Chip and eutectic are now scrubbed together by the collet, forming a hard alloy bond. Heater temperature is approximately 420°C and the total time taken for eutectic bonding is about 6 to 8 seconds.

Polymer bonding is faster than eutectic bonding and can be completed in approximately 2 seconds. It is often used in the production of packages containing copper leadframes as it has some stress absorbing properties. The feed equipment is the same as for eutectic bonding, however the chip support is no longer heated. Silver loaded epoxy or polyimide adhesive is transferred to the chip support platform by a print head, and the chip is pressed into the paste. The adhesive-bonded dies are cured in ovens before wirebonding.

More recently, improved silicone gels have been introduced as a alternative means of anchoring the silicon die to the support platform. It has been reported that this method has been successfully used to bond large chips onto the epoxy bases of

2-17
plastic PGA packages [14] where, after wirebonding, the entire PGA cavity was encapsulated with the same gel. This meant that the die was embedded in a compliant medium, which was able to withstand both thermal and environmental stresses.

2.6.4 Moulding Compounds

The type of moulding compounds used for IC packaging come from a family of plastics known as thermosetting plastics. Phenolic, bis-phenols epoxy, and silicone polymers have all been used in the past for IC packaging. The moulding characteristics of each of these types of plastics are excellent, however each of these compound types have had problems which caused the device to fail under stress testing and in the field.

Phenolic encapsulated ICs produced an unacceptable high level of corrosion failures on high temperature humidity stress testing. This was caused by the generation of ammonia within the compound during post-mould cure, as well as high levels of ionic contaminants such as chlorine and sodium, and a tendency for a high level of moisture absorption. Moulding materials based on diglycidyl ether of biphenol-A (DGEBA) were popular in the 1960's. DGEBA was made by reacting epichlorohydrin with biphenol-A. The epichlorohydrin was produced by reacting propylene with chlorine. During the DGEBA reaction excess chlorine was liberated, most of which was removed by reacting the resin with sodium hydroxide. The chlorine content was further reduced in the formulation process by the addition of other compounds to the resin. Despite this the best levels of hydrolysable chlorine that could be produced were around 400 ppm. This is too high a level for the reliable operation of plastic encapsulated ICs, also Bis-A resin based moulding compounds have a glass transition temperature \((T_g)\) between 100-120°C. This is relatively low and is below the temperature range (-55 to 125°C) specified for professional electronic equipment. Consequently they were disposed to producing failures during temperature cycling. As the c.t.e. of the moulding compound increases rapidly above \(T_g\) these devices failed due to excess stress on their bondwires. In fact they would display an effect known as "windowing" where, as the equipment's temperature rose, the ICs would pass through \(T_g\) and the resulting stress would pull the bond wires away from the bond pads resulting in an open circuit. As the equipment cooled the plastic would contract
and the electrical connection would be re-established. This effect led to biphenol-based moulding compounds being phased out in the early 1970's.

Silicone based resins have many properties that make them good moulding compounds. They are synthesised from silicones and so contain virtually no ionic species, such as chlorine and sodium, however they possess a low Tg and exhibit very poor adhesion properties. Devices packaged in these materials were susceptible to flux penetration during wave soldering, and had the same windowing failure mode as biphenol packaged devices.

Clearly what was needed is a compound that had a high Tg, low moisture permeability, low levels of ionic impurities, exhibits good adhesion and was readily mouldable. Epoxy Novolac resins have these attributes.

Epoxy novolacs resins are made from epichlorohydrin via the same route as biphenols. The resins are solid at room temperature, have high cross linking density and functionality. High cross linking gives the resin a low moisture absorption rate, when compared with earlier plastics. High functionality imparts heat stability and high Tg. Novolac based moulding compounds have Tg's of 150°C and higher. Epoxy Novolac based moulding compounds consist of several materials and the particular formulation depends on the application.

Semiconductor-grade compounds consist of:

1. Novolac epoxy resin (26 - 30%)
2. Accelerator
3. Curing agent
4. Inert filler (68 - 72%)
5. Flame retarder (2%)
6. Mould-release agent
7. Colourant
8. Stress-relief additives
2.6.4.1 Resin

The epoxy novolac resin is the key material upon which the moulding compound is built. It is an organic binder that, when cured, holds the constituents together and imparts the inherent characteristics of high $T_g$, curing shrinkage, low moisture absorption, and chemical inertness. Modern IC moulding resins possess levels of extractable chlorine of less than 30ppm. Cresol-novolac epoxies resins are the most common resins in use today for microelectronic packaging. The structure of cresol-novolac epoxy is shown in Figure 4.

![Figure 4 Chemical Structure of Polyglycidyl Ether of o-Cresol-Formaldehyde Novolac Epoxy.](image)

2.6.4.2 Curing Agent (Hardeners)

Curing agents or hardeners are used to cross-link the epoxy-novolac resin molecules. This affects the viscosity and reactivity of the cured compound. The choice of hardener governs the nature of the chemical bonds established and the final extent of cross linking obtained. The cross linking of an epoxy network can proceed via three general, well characterised, routes;

a. Cross linking of the matrix via various functional groups of the hardener.
b. Linkage between the epoxy groups with aliphatic or aromatic hydroxyl.
c. Direct linkage between the epoxy groups through self-polymerisation.
Amines, acid anhydrides or phenols can be used to produce the cross-linking of the epoxy resin. The cross linking process is different depending on the hardener used as the reactions proceed by different routes. Ring opening is the predominant mechanism for amine hardeners, whereas the anhydrides and phenols hardeners produce cross linking via pendant hydroxyl groups. In conventional novolac resins aliphatic amines are generally used to produce room-temperature curing systems as they cure rapidly at low temperatures. Aromatic amines, however can be blended to yield products with higher thermal performance and chemical resistance however acid anhydrides and aromatic amine curing agents require accelerators because of their lower reaction rates even at elevated temperatures. Phenol novolac and cresol novolac hardeners have become the dominant hardeners in microelectronics packaging owing to their excellent mouldability, electrical properties, heat and humidity resistance. The structure of a cresol-novolac hardener is shown in Figure 5.

In amine hardeners the functionality of the amine is determined by the number of active hydrogen atoms. Each hydrogen atom attached to a nitrogen atom opens up an epoxy ring. In the process primary amines are converted to secondary amines with the corresponding hydroxyl. These secondary amines react in turn with other epoxy groups to form tertiary amines.

Liquid anhydrides are also widely used as curing agents in electronic applications. There is typically no reaction between the anhydride and the epoxy group until the ring is opened. An ester or an ether anhydride can be established from the combination of an epoxide with a carboxylic group or a hydroxyl group respectively. Alternatively, the anhydride ring may be opened by an hydroxyl group. These reactions are slow at room temperature. The process is speeded up using an accelerating compound. The accelerator is usually a tertiary amine which is used in very small concentrations to accelerate gel and curing times. The accelerator works by acting as a catalyst to initiate the cross linking of hardeners at the appropriate moulding conditions.
2.6.4.3 Accelerators

The moulding compounds are supplied in two parts which are mixed on moulding. One part contains the resin and filler, the other is a mixture of resin hardener and accelerator. In the case of acid anhydride and phenol cured resins accelerators are needed. These compounds act as catalysts to initiate and accelerate the cross-linking of the epoxy when heat and pressure are applied by the moulding process hence the accelerators have the effect of shortening the in-mould cure time of the moulding compound. Tertiary amines are often employed for this purpose.

2.6.4.4 Filler

The epoxy resin cannot be used alone as a packaging material and a filler material is added to impart the necessary properties to the moulding compound the most commonly used filler is inert silica particles. The effects of the addition of the filler are;

*Lowering of the peak curing temperature* - Silica particles have a relative high specific heat capacity (0.8 J/g°C) compared to the resin (0.3 J/g°C) therefore much of the heat generated by the exothermic polymerisation phase is absorbed by the filler.

*Improved thermal conductivity* - The addition of silica filler particles increases the thermal conductivity of the moulding compound once a certain volume fraction of filler has been reached. This is because the filler particles must be in contact with each
other if effective heat transfer is to be achieved. The shape, size, concentration and
distribution are all important considerations in optimising heat transfer.

**Improved thermal shock resistance of the moulding compound** - The filler occupies
a large volume of the system and has a low coefficient of thermal expansion this
causes the overall c.t.e. of the moulding compound to be reduced. This improves the
thermal stability and thermal shock resistance of the moulding compound during
temperature excursions however the high level of filler reduces the tensile strength of
the compound and increases the permeability to moisture.

2.6.4.5 Flame Retarder

To reduce the flammability of the plastic moulding compound a flame retardant
is added when the resin is formulated. Compounds employed include
tetrabromobiphenol-A and antimony trioxide. Tetrabromobiphenol-A is reacted with

![Figure 6 Chemical Structure of Tetrabromobiphenol-A Flame Retardant Compound](image)

materials such as diglycidyl ether of biphenol-A (DGEBA) to produce a brominated
epoxy resin that is added to the moulding compound. The proportion of brominated
resin to novolac epoxy is approximately 10%, the reaction is shown in Figure 7.
Although the bromine atoms are attached to aromatic rings and are therefore not
mobile or hydrolysable, the covalent bond with the aromatic ring has only limited
stability. This can lead to the liberation of the highly reactive bromine ions at high
temperatures. In the late 1970's halogenated biphenols were beginning to be replaced
by brominated novolacs which display improved heat stability [15].

![Reaction between Tetrabromobiphenol-A and Epichlorohydrin to produce a Brominated Epoxy for use as a Fire Retardant.](image)

**Figure 7** Reaction between Tetrabromobiphenol-A and Epichlorohydrin to produce a Brominated Epoxy for use as a Fire Retardant.

### 2.6.4.6 Mould-release Agent

Epoxy resins are generally excellent adhesives and this can make release from the moulding equipment difficult. It is therefore necessary to use a mould release agent which has to be carefully selected to provide ready release from the mould. The release process is conducted through the softening and functioning temperature of the release agent. The materials are mixed at approximately 100°C and then moulded at 175°C. Often two different release agents are used to provide release at each temperature. It is then possible to achieve adhesion at room temperature with a release agent that solidifies and is ineffective at lower temperatures. Additionally the moulded parts are designed with draft angles to facilitate removal from the moulds. Common mould release agents are silicones, hydrocarbon waxes, metallic salts of organic acids and fluorocarbons.
2.6.4.7 Colourant

Plastic packaged ICs are black in colour this is primarily for aesthetic reasons as the cured uncoloured resin is a translucent yellow. To produce the customary black appearance of plastic moulded ICs a colorant is added to the moulding compound. This is usually carbon black or an organic dye. Carbon black is made from the incomplete combustion of hydrocarbons. It is therefore possible that it may contain impurities such as sulphur and nitrogen-containing materials. The addition of carbon black is not without its problems. It is an electrical conductor, and too high a concentration or inhomogeneity in the mixing process could cause problems. Therefore the level of colorant and its dispersion has to be carefully controlled. The level of carbon black in modern semiconductor grade moulding compounds is typically 0.5%. Other colours can be obtained by the use of organic dyes. These compounds are not as stable as carbon black and they can compromise the high temperature properties of the moulding compound.

2.6.4.8 Stress-relief additives

Epoxy materials are inherently brittle due to the high cross-linking density which confers the high temperature performance and solvent resistance that is so desirable. This same property is also responsible for decreased polymer chain mobility and relaxation. Flexibilising or stress relief agents are added to inhibit crack propagation and lower the thermo-mechanical shrinkage stresses that can initiate cracks in the moulding compound or in the passivation layer of the device. Stress relievers can be either reactive or unreactive. Unreactive plasticisers include phthalic acid ester and chlorinated biphenyl. The alternative is to use a flexibiliser. Fortunately the high reactivity of the epoxy group means that many different compounds can be used as reactive flexibilisers. Flexibilisers are additives that remain in the material as single phase additives. Flexibilisers are interpenetrating networks inserted to modify the moulding compound by improving the ductility and lowering its tensile modulus. If however the additive is segregated in a second dispersed phase, and there is little or no effect on the epoxy matrix properties, then it is termed a stress relief agent. There are two different types of stress relief agent. Those that are initially compatible with the epoxy matrix material and phase separate during curing, and those that are
readily formed into domains and then mechanically disperse within the epoxy prior to cure.

Stress relief agents induce several beneficial effects in the moulding compound. They reduce the tensile modulus of the two phase system by decreasing the cross sectional area of the hard epoxy phase and they are effective as crack propagation inhibitors. Crack propagation through the matrix phase may be stopped or the cracks can be branched upon reaching a "rubbery" domain. Silicones, acrylonitrile-butadiene rubbers, and polybutyl acrylate are the major stress relief agents used in epoxy moulding compounds. The size of the introduced domains are around 1 micron diameter. The addition of elastomers to epoxy moulding compounds can often provide significant improvement in the occurrence of passivation layer cracking, aluminium line deformation, and package cracking.

The addition of elastomers to epoxy moulding compounds has the effect of producing a relatively weak interfacial region as there is now a large difference in modulus between the epoxy and the soft elastomer. This interfacial integrity has been improved through the use of an interaction layer with a modulus between that of the epoxy and the modifier. Polymethyl-methacrylate has been used as an inter layer shell over the filler particles. When well dispersed through the epoxy they were found to improve the interaction of the particles with the epoxy matrix.

Despite these advantages plastic encapsulated devices still suffer from two disadvantages. Firstly, their power dissipation is limited by the need to maintain the package temperature below $T_g$. Secondly, the plastic is not hermetic allowing the ingress of moisture to the die. This process is accelerated as temperature and relative humidity increase.

2.6.5 Physical Properties of Moulding Compounds

Semiconductor moulding compounds should possess certain physical properties; those that are necessary during in the moulding process to facilitate production and those that are important properties of the finished product. Some of more important
properties of typical moulding compounds are summarized in Table VI.

2.6.5.1 Physical Properties of Moulding Compounds Required at the Production Stage

There are several physical properties that a resin must possess if it is to be used as an encapsulation material applied by the transfer moulding process. Unfortunately many of these properties are interrelated. The important properties are low resin viscosity, good wetting of the chip components, good adhesion to the components and a short cure time.

Low Resin Viscosity - The moulding compound must have a low viscosity at the moulding temperature so that it can flow quickly and evenly throughout the runners and gates of the mould. It must also flow over the leadframe and die without causing deformation, or breaking, of the bonding wires. It must also have a high deformation temperature in its cured state so as to be able to withstand the forces imparted on the package during the trim and form operations.

Rheologically complex fluids such as molten plastics display different dependencies of shear stress over different ranges of shear rate. They may display Newtonian behaviour at low shear rates providing what is known as a Newtonian Plateau on a plot of viscosity versus shear rate. At higher shear rates, and higher molecular weights their behaviour deviates from that of a Newtonian fluid. In a Newtonian fluid the shear stress is linearly proportional to the shear rate of laminar flow and the constant of proportionality is defined as the viscosity. The viscosity of the resin shows a dependence on molecular weight and temperature.

Good Wetting of the Package Components - The extent of wetting of the packages components is governed by the viscosity of the resin and the pressure applied during the moulding process.

Good Adhesion to Die and Package Components - The adhesion of the resin to the package components is a function of the chemistry of the moulding compound and of the chip and leadframe surface. For the formation of good bonds between the resin, the leadframe, and the die, good wetting is necessary. The adhesion of the resin is an
important property but it can be enhanced by pretreatment of the leadframe by methods such as texturing, cleaning and degreasing, as well as the provision of mechanical features such as lead-locking holes and depressions in the leadframe.

*Short Cure Time* - It is an important production requirement that the resin cures quickly to minimize the time it spends in the moulding equipment as this maximises output. The type of catalyst, nature of the cross-linking agent, the level of initiator, the level of pre-polymerization of the resin and the moulding temperature will all effect the rate of network formation. Frictional heating of the resin against the mould walls during moulding will speed up the polymerisation process further and so must be closely controlled by paying attention to the transfer pressure, rate of flow, and the shape of the mould.

2.6.5.2 Important Physical Properties required of the Moulded Package

The moulded plastic package must possess certain physical attributes if it is to provide successful encapsulation of the semiconductor die these are;

*Inherently Low Coefficient of Thermal Expansion* - The coefficient of thermal expansion (c.t.e.) of the moulding compound protecting the die has to be closely matched to the c.t.e. of the leadframe and die. It is the stress induced in the plastic compound that can cause cracking and delamination between plastic and leadframe during thermal cycling. The same stresses can also cause the die to shear from the leadframe and cause bonding wires to be broken. To control this the type and quantity of filler used has to be closely controlled. A high volume to weight fraction of fillers would also have the beneficial effect of enhancing the heat transfer properties of the encapsulating material, and improve its resistance to moisture and solvent absorption. Unfortunately, one of the undesirable consequences of this approach is the drastic rise in the moulding compound's viscosity. An increase in the viscosity of the moulding compound can cause severe problems in the moulding process due to poor flow.

*Good Dimensional Stability* - On curing the resin shrinks and a compressive force is exerted by the resin on the leadframe and die. The degree of shrinkage depends upon
the moulding compound and moulding conditions. This linear curing shrinkage is about 0.05 to 1.5% depending on resin and filler loading. The magnitude of such a stress in a particular package will depend on package design. In some cases the stresses locked within the device by the encapsulant can lead to a deviation in the values of resistors, fabricated on the die, of up to 15% from their un-packaged values due to the piezo-resistive effect. The deviation in value can be even higher if the resistor is located at the edge of the die, where the stresses are greatest. Consequently active circuits are usually fabricated in the centre of the die, away from the high stress concentrations at die's edge, and an unused margin is left around the edge of the die. The presence of stresses within the die can also affect active circuits. Mobility parameters such as transconductance in CMOS devices and signal current gain in bipolar devices are altered by the mechanical stress. The presence of high levels of internal stress on the device will be reflected in its mechanical integrity and electrical properties.

Low Moisture Permeability - Water and other solvents can penetrate to the resin/device interface through even the most non-porous polymer. This occurs either by filtering through micro-cracks or by capillary migration along the leadframe. Once moisture enters the package there is a risk of parametric drift and catastrophic failure due to corrosion. The failure mechanisms associated with ingress are discussed in Chapter 3.

Dielectric Properties - The dielectric properties of the encapsulating material play an important part in device performance. The relative permittivity of the dielectric material comprises of dielectric constant and dissipation factor terms, [4]. Encapsulants that have a low dielectric constant and low dissipation factor offer better performance as they provide faster signal propagation with less attenuation. The speed of propagation of an electromagnetic wave in a dielectric medium is inversely proportional to the square root of dielectric constant. The attenuation that the signal suffers is proportional to the dissipation factor of the dielectric material. In an integrated circuit package the leadframe passes through, and is embedded in for part of its length, the moulding compound. In very high performance packages the
dielectric properties of the encapsulating compound, be it plastic or ceramic, can be a consideration in the package design.

\[ e = e' + je'' \]  

Where \( e \) is permittivity and \( e' \) dielectric constant and \( e'' \) the dissipation factor

\[ v_p = \frac{c}{\sqrt{\varepsilon'}} \]  

\( v_p \) is the velocity of propagation in the dielectric and \( c \) is the velocity of propagation of light in a vacuum.

**Thermal Conductivity** - The thermal conductivity of a material is a measure of its ability to conduct heat energy through its bulk. This property is an important packaging criterion as it is this parameter which governs how the heat generated by a device is conducted through the package to the outside world where it can be dissipated. Polymers have lower conductivities than other materials commonly used in electronic packaging such as metals, glasses and ceramics. Devices with heat dissipation greater that 2 Watts/cm\(^2\) may require cooling fins or heatsinks to help dissipation. In general ceramic packaged devices have greater heat conducting properties than plastic packages and devices encapsulated in ceramic packages can therefore be allowed to dissipate more heat than polymers encapsulated ones. They may also run at higher temperatures. For this region the majority of fast processors are encapsulated in ceramic packages regardless of where a high degree of hermeticity is a consideration. However, there is considerable interest in increasing the thermal dissipation of plastic packages. Higher dissipation plastic packages which are capable of dissipating up to 3 Watts, in packages as small as 100 pin QFPs, are being developed [16].

**Specific Heat Capacity** - The specific heat capacity of a material is the amount of energy in the form of heat that must be absorbed by a given mass of material to raise its temperature by a given increment. It is an important property of packaging materials that one needs to be able to predict the rise in external temperature of a
device dissipating a given amount of power.

_A Low Concentration of Hydrolysable Ionic Species_ - Non hermetic materials such as polymers absorb moisture. The corrosive effects of the moisture on the metallic components of the package, such as the bondpads and chip metallisation, is greatly enhanced by the presence of ionic elements such as chlorine. Residual amounts of such ionic elements can be present in the moulding compound as a consequence of its method of manufacture, or a processing residues left behind in the production of the package.

_Low Alpha Particle Emission_ - The operation of charge sensitive devices such as Dynamic Random Access Memories (D.R.A.M.) can be effected by ionising radiation. This was first reported by May and Woods in 1978 [17]. In DRAMs the logical state of the memory cells of the device depend on the magnitude of a minute amount of charge stored on an MOS capacitor. If ionizing radiation impinges on such a cell altering the amount of stored charge then it can be forced to change state and the stored data will be corrupted. This form of data corruption, where the error in the data occurs randomly and does not damage the operation of the device, is known as a "soft error". This form of data corruption has been known in the past as "system noise" or "pattern sensitivity" [18][19]. The most troublesome form of radiation in this respect is alpha particle radiation.

    The alpha particles originate from the residual radioactivity of traces of uranium and thorium present in the packaging materials. The major source of such errors is the filler material. Early attempts to reduce this problem involved the careful sourcing of low alpha content fillers from certain mines. This was often used in conjunction with an "alpha coat" a thin coating of RTV silicone elastomer or polyimide resin over the die. This was superseded by the introduction of a process by which silica filler particles could be manufactured from fused quartz powder.
<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Manufacture's Code</th>
<th>Thermal Conductivity W/m°C</th>
<th>Thermal Expansion 10⁻⁷/°C</th>
<th>Flexural Strength GPa</th>
<th>Flexural Modulus GPa</th>
<th>Extractable Chlorine ppm</th>
<th>Glass Transition Temperature °C</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sumitomo</td>
<td>EME-6200</td>
<td>0.67</td>
<td>200</td>
<td>0.13</td>
<td>12.72</td>
<td>25</td>
<td>165</td>
<td>Low stress compound for large DIPs and PLCCs</td>
</tr>
<tr>
<td>Sumitomo</td>
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<td>200</td>
<td>0.14</td>
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<td>20</td>
<td>155</td>
<td>Low alpha particle compound for DRAMs</td>
</tr>
<tr>
<td>Hysol</td>
<td>MG35f</td>
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<td>260-750</td>
<td>0.13</td>
<td>14.44</td>
<td>10</td>
<td>160</td>
<td>Moulding compound for high power devices</td>
</tr>
<tr>
<td>Nitto</td>
<td>MP119</td>
<td>0.63</td>
<td>180-650</td>
<td>0.13</td>
<td>12.23</td>
<td>10</td>
<td>170</td>
<td>Low stress &amp; ionic content for SOIC packages</td>
</tr>
</tbody>
</table>

Table VI Physical Parameters of some Typical Moulding Compounds
2.6.6 The Plastic Encapsulation Process

There are many operations involved in the encapsulation of a silicon die in a plastic package the order of these processes is shown in Figure 8.

2.6.6.1 Die Attach and Wire Bonding

The die may be bonded to the paddle of the leadframe by eutectic solders, polymer adhesives or silver-filled resins. All these methods are conductive allowing an electrical connection to be made to the substrate. The most common attachment method is probably by means of silver loaded conducting epoxy adhesive. To improve bonding the die is sometimes scrubbed against the paddle to spread the adhesive. After this the leadframes pass through an oven to cure the adhesive.

Electrical connection between the die and leadframe is accomplished by thin gold or aluminium bonding wires. Typical bond wire diameters are 25 microns to 32 microns for gold and 50 microns for aluminium. In gold wire bonding, the bond at the die's bond pad is usually formed by flame softening the tip of the wire and then pressing it against the bondpad. The wire is looped out and formed into a wedge bond on the leadframe finger. Today wire bonding is automated and typical bonding rates may be as high as 200 wire bonds per minute. Aluminum wire has to be ultrasonically welded.

2.6.6.2 Moulding Compound Processing

Before a compound can be successfully used to encapsulate an IC it must undergo several processing steps.

_Moulding Compound Storage_ - The quality of the epoxy moulding compound is greatly affected by the temperature excursions that it is subjected to prior to moulding. To this end great care is taken in the refrigeration of the moulding compound in the storage and shipment phase. The drums are shipped in refrigerated containers surrounded by dry ice. Good shipping containers will have some form of temperature recorder so that batches that have been subjected to unacceptable temperatures during shipping can be rejected. This incoming inspection of the moulding compound is an important factor in the quality control of the packaging process and must not be
Process Steps in Producing a Moulded Plastic Package

- Wafer Sawn into Individual Dies
- Die Attach to Leadframe
- Wire Bonding
- Transfer Moulding of Package
- Dejunk/Dambar Removal
- Package Marking
- Post Mould Cure
- Solder Plating
- Trim & Form Leads
- Devices Packed & Boxed for Shipment

Figure 8 Typical Assembly Process for an Integrated Circuit Encapsulated in a Moulded Plastic Package
omitted. If the moulding compound is subjected to too high a temperature then premature polymerization may be initiated. Should polymerisation be initiated early then the viscosity of the material is increased and it will not flow satisfactorily in the moulding process owing to this increased viscosity and reduced flow length in the moulding tool.

*Moulding Compound Conditioning* - Moisture uptake by the uncured resin prior to moulding can have an effect on the quality of the finished moulded package. Water is absorbed by epoxy moulding compounds from the atmosphere and the amount absorbed increases with the relative humidity of the air up to a point where it absorbs 0.5% by weight of water at 100% Relative Humidity (RH). The absorbed moisture effects the material's viscosity, rheology and the quality of the finished moulded package. It reduces the viscosity of the resin in its molten state by as much as 40% compared with dry conditions [20]. Moisture uptake can also cause greater resin bleed and the possibility of an increased occurrence of void formation.

Moisture absorbed prior to moulding also has an effect on the ultimate properties of the moulded package. The glass transition temperature of the cured material can be lowered by moisture absorption in the uncured state indicating that the cross linking structure that forms in the presence of moisture is different from that formed in dry conditions. It also has an effect on the rate of polymerisation as it binds with the catalyst and reduces its effectiveness. Moisture absorbed after moulding can have a dramatic effect on surface mount components undergoing reflow soldering where the rapid expansion of the moisture absorbed in the bulk of the plastic causes cracking of the package body.

The ideal relative humidity for good moulding is between 20-50%. Material that has been removed from freezer storage is likely to have a moisture content near or below the acceptable range. Consequently moisture content conditioning of the preformed material must be conducted by allowing the resin to absorb a small amount of moisture in carefully controlled environmental conditions. Alternatively some moulding compound manufacturers supply resins that contain a carefully predetermined amount of moisture that corresponds to conditioning at 30-40% RH.
Preheating of the Moulding Compound - Preheating is conducted on the plastic moulding compound prior to moulding. The compound has its temperature raised to 90-95°C by radio frequency heating. This has the effect of softening the resin before its transferred to the moulds.

2.6.6.3 The Transfer Moulding Process

The plastic packages of integrated circuits are formed by a process known as transfer moulding. This process is conducted in a machine called a transfer moulding press. There are two basic types of press, the single piston and multiple piston type. In the single piston press a single large diameter piston forces the molten moulding compound into as many as 300 mould cavities. Each mould cavity forms the package around the die/leadframe assembly to form a encapsulated single integrated circuit. The alternative is a multiple plunger press where many small diameter plungers supply an array of anything from 1 to 6 cavities.

The moulding press is loaded with either a single pellet or multiple pellets of resin prior to charge. The resin is melted and once molten, a plunger compresses the resin charge and maintains it under pressure for 10-15 seconds, depending on the mould temperature and resin type. Once the resin has softened to a workable viscosity, the transfer to the cavities occurs in only a few seconds. The heat input into the pellets is via conduction from the press walls. Viscous heating does not occur until the charge is forced through the mould runners. Full transfer pressure is not applied until the moulding compound is partially transferred to achieve optimum mould residence time.

Transfer Moulding Machinery - Transfer moulding presses consists of several parts. The function of which is now be described.

Moulding Tools - Mould design is critical to the assembly process yield and to component reliability. Produced from tool steel, by electric-discharge machining, mould cavities define the size, shape, and surface finish of the plastic package. The moulds are made in two halves to receive the die and leadframe assembly prior to moulding and are clamped together during the moulding process. The mating surface is termed the parting line. A mould set would consist of a pair of platens and a pair
of chases.

The platens are massive steel blocks that are bolted to the base (bottom) and crosshead (top) of the moulding press. Corner pins align the two platens in the vertical plane. The bottom platen contains ejector pins that push the moulded parts from the cavities after moulding. Parallel holes containing cartridge heaters horizontally traverse each platen to maintain the chases at the specified temperature for moulding. The platens are designed to bear the several tons of clamping force that are exerted by the press crosshead.

Chases are the parts of a mould set that come into contact with the moulding compound and impart to the finished package its shape. Into the hardened surface of the chases are machined the runners and gates that transfer the hot viscous plastic to the mould cavities. The top and bottom chases are bolted to their respective platens and are aligned with steel locating pins. The surface of the chases are designed to provide a non-stick surface for easy part ejection and resist wear from the abrasive filler particles in the moulding compounds. Typically the finish is electroplated chrome. The chases consist of several elements; primary runners, secondary runners, and gates.

Figure 9 The Layout of a Typical Mould Chase

The layout of the runner system is balanced to provide for an even distribution
of moulding compound into each cavity. The objective is to fill every cavity with moulding compound of uniform density so that the device packages moulded close to the pressure ram have identical properties to those at the end of the runner. The layout of a mould chase is shown in Figure 9. There are two basic types of runners, primary and secondary. The primary runners are the main stems that allow resin flow through the mould and the secondary runners are branches which feed into the mould cavities. Figure 10 shows the layout of runners and cavities in a typical mould in cross section. The gates are the small openings into the cavities through which the moulding compound flows from the secondary runners.

Conventionally transfer moulding presses rely largely on a single plunger and relatively long runners to serve the most remote cavities. The reacted material that is left behind in the runners is wasted, and in high volume production the amount of waste can be substantial. Present trends in transfer moulding are towards machines with several pots and plungers that can reduce the amount of this waste. Shorter paths from the pots to cavities, complete filling is more likely. The shorter shot size used results in shorter gel and cure times, and the pressure distribution between cavities is more uniform. This leads to a better and more economically produced product.

Despite the trend away from European and North American packaged products to packaging in the cheaper countries of the Pacific rim, savings in the cost of plastic packaging are still being sought by the manufacturers. This has lead to much interest
in automated and robotic presses that can reduced labour costs still further.

2.6.6.4 Post-cure

The rate of the cross linking reaction is not constant and drops off with decreasing concentration of the remaining unreacted materials. Therefore it requires considerably longer for the reaction to proceed been the points were 70 to 90% of the reactants have reacted than it does to for the first 20% to react. Productivity would suffer if the packages were allowed to cure completely in the transfer moulding equipment. Therefore the moulded packages are removed before 100% conversion is reached and they are post-cured in ovens to complete the polymerisation process. Post-cure has to be conducted at temperatures above the $T_a$ of the cured plastic, typically 170-175°C for 4-5 hours. Post cure at high temperature reduces the time required to reach full conversion and is conducted in batches using large convective ovens that can contain many thousands of devices.

2.6.6.5 Deflashing

Deflashing is the name given to the removal of the moulding compound that has unintentionally flowed out of the mould and on to the leadframe. This is usually due to preventable short comings in the moulding process. The typical thickness of flash is only about 10 microns but if it were left on the packages it could cause processing problems further on in the packaging process, such as the trim and form operations.

Deflashers operate on several principles. Media deflashers utilise a shot blasting principle were soft inertial material such as plastic beads are fired at the leadframe to dislodge the flash. Solvent deflashers expose the leadframe to a hot solvent that reduces the adhesion of the flash to the leadframe. Water deflashers operate with jets of water and they cut away a very small portion of plastic in the vicinity of the leadframe and with it the flash.

2.6.6.6 Trim and Form

During the trim and form process the package is cut from the strip that has held it in place through the packaging process. The dam bars and shorting bars are cut
away. The legs of the package are then formed by the forming process. The type of lead that is formed depends on the package style.

2.6.6.7 Solder Dipping and Solder Plating

The leads are then coated with solder to facilitate their subsequent attachment during board assembly. The coating process can be carried out by either dipping or plating the leads.

2.6.6.8 Code Marking

Code marking adds information to the top, and sometimes the bottom, of the package. Such information as the part number, manufacturer, batch number, date of production, and country of origin is added. Packages are marked by printing or by laser. Printing is usually accomplished by rubber stamping in a machine.

2.6.6.9 Inspection

The principle criteria for inspection is the position and form of the leads. Leads are often improperly bent during the trim and form operation and subsequent handling. This is usually automated by the use of vision equipment.

2.6.6.10 Burn-in

Burn-in is a reliability test under accelerated life testing conditions at elevated temperature. It is conducted to screen out defective devices that would fail in the short term, the so called "infant mortality failures". These failures are indicative of process faults in manufacture which makes this form of testing useful in the confirmation of correct production techniques. Should an excessive dropout rate be observed at the testing stage then it could be indicative of a poor batch and the entire production run may have to be scrapped.

During burn in, the devices are connected to circuit boards and are stressed at elevated temperatures with bias applied. Typical conditions are 125-150°C for approximately 24 to 48 hours. Bias voltages up to 40% above the working voltage of the devices are sometimes employed to increase the acceleration factor. Burn-in can be applied to 100% of production or statistical quality control techniques can be
employed with sampling. The choice of which method to employ is dependant on the manufacturer and the confidence required in the reliability of the finished product.

2.6.6.11 Testing

Full functional testing of all semiconductor devices in a production run is standard practice in the electronics industry. This naturally contributes significantly to the cost of the devices. Testing is conducted by computer controlled testers that evaluate all device parameters to a prescribed algorithm prior to shipping.

2.7 Hermetic Encapsulation

Hermetic sealing implies that all external chemical species are permanently prevented from entering the package cavity. In practice however, a finite leakage rate occurs through diffusion and permeation, so that no package is ever completely hermetic. The leak rates of hermetic packages are usually very small, even under the most extreme environments. Acceptable leak rates are specified in MIL-STD-883 [21], together with test procedures for measurement by Helium bomb techniques. The principle environment related cause of device failure is ingress of moisture through the package although it is moisture that the hermetic package is specifically design to exclude.

In general hermetic packages are cavity packages constructed of ceramic or metal into which the semiconductor die is mounted. The package is then sealed with a lid or cap. Electrical connection to the device is via leads which must also be hermetically sealed to the package.

2.7.1 Metal Packages

Metal packages can offer very high degrees of hermeticity and reliability but at higher cost. They are therefore used in the most stringent of applications mainly in the military and aerospace industries. There are principally four styles of metal package. The round header, monolithic, flat-pack and platform. Both round header and platform are old styles used for pin counts up to 16 connections. The monolithic
packages are available with pin counts up to 88 pins. The flat-pack is a low profile package intended for VLSI devices and can be fabricated with up to 200 pins. The metal cans are usually pressed from sheet brass with their lids soldered, welded or brazed. The feed-through pins are made of Kovar alloy and are brought out through glass-to-metal seals in a metal plate or header. These seals have the advantages of being chemically inert, and are resistant to oxidation, they have a high electrical resistance, and are impermeable to water and gases. Their short comings however are low-strength, & brittleness. Strain on the pins can cause cracking of the glass and loss of hermeticity of the package. They can also suffer from fracture during sudden temperature variation. Their resistance to fracturing can be tested by a procedure prescribed in MIL-STD-883 [22][23]. The glass-to-metal seal is fabricated as a bead of glass on the feed through pin. They are of two types, the matched seal or the compression seal. In matched seals the coefficients of thermal expansion of the glass and metal are very similar. To ensure adhesion of the glass the metal surface is provided with an oxide layer. The compression seal does not involve the formation of a chemical bond between glass and metal. In this case the glass is chosen so that its c.t.e. is less than that of the metal. Once the assembly is sealed at the glass melting point, it is then cooled and the metal shrinks to a greater degree than the glass and holds it tightly in compression. Examples of metal packages are shown in Figure 11.
2.7.2 Ceramic Packages

Ceramic packages for the encapsulation of microelectronic devices exist in two forms. They are either produced as fired ceramic packages or as ceramic dual in-line packages, Cerdips fabricated from a ceramic/glass sandwich. The fired ceramic package, like plastic packages, are available in many styles.

2.7.2.1 The Ceramic Dual-in-Line (Cerdip) Package

These are the easiest to fabricate and are therefore the cheapest of the ceramic packages. They are typically used for packages with a small number of I/O, typically <=28. In these packages a Kovar leadframe is first attached to a glazed alumina platform by temporarily softening the glass. After die attach and wire bonding, the glazed ceramic cap is sealed to a sub-assembly in a conveyor furnace or in a "Hot Cap" sealer. Here the glass melts and fuses to the alumina shell. The glasses used are high lead content vitreous or de-vitrifying glasses with sealing temperature of about 400°C. Alternatively the Cerdip package can be fabricated with side brazed leads. In this configuration the die is bonded into an multilayer alumina box through which
metallised tracks connect to the outside of the package. At the outside Kovar legs are brazed to the sides of the package. The package is sealed by soldering to a metallisation layer deposited onto the top layer of the alumina sandwich which surrounds its opening.

2.7.2.2 Fired Ceramic Packages

The fired ceramic package is used to fabricate the higher I/O count ceramic packages such as the LCC and PGA. It is possible to fabricate either single or multilayer metallized interconnects through the package body with this technique. The single layer package is fabricated by the dry press technique. In this process alumina powder is pressed into shape and fired in air, followed by screening and sintering of one metallization layer. Multi-layer packages are fabricated from laminated sheets of ceramic and glass powder suspended in an organic binder. This tape is also known as "Green Sheet", it is the basic building block of fired ceramic packages and is available in thicknesses of 0.2 or 0.28mm. Computer controlled punches produce closely tolerated holes through the tape for interconnection. Interconnection is achieved by the use of an extruded metallisation paste which is loaded either with tungsten or molybdenum particles and is screen printed onto the tape. The tapes are laminated and fired. Nickel plating of the surface features follows with diffusion bonding to the molybdenum base metal to enhance adhesion. A layer of gold is applied over the nickel to prevent the formation of nickel oxide and improve wettability for the subsequent soldering and brazing operations. The bond pads receive a thicker layer of gold plating. In the case of packages that are terminated in pins, i.e. PGAs and DIPs, the pins can be brazed to the package at this stage. The chip carrier is then ready for die attach and wire bonding. The package is sealed by brazing a Kovar lid in place in a dry nitrogen atmosphere.

2.8 Other Packaging Methods

There are several other packaging styles which are employed in specific applications. These will be briefly mentioned to provide a more complete picture of the electronic package options available.
Hybrids - Hybrid Integrated Circuits (HICs) are, as the name suggests, relatively sophisticated circuits assembled into a single package from a number of packaging technologies. This is a well established technique which is used for small volume assembly of systems requiring high reliability. They consist of miniature circuit boards using a film integrated circuit (FIC) on a ceramic or epoxy substrate. Onto the substrate are assembled silicon devices and a mixture of thin and thick film components. These components are often tunable with laser trimming making this form of assembly particularly suitable for high performance devices such as filters and oscillators, which may need optimisation by fine adjustment after assembly. The small size of HICs prohibits the use of most prepacked semiconductor devices, thereby creating a need for direct chip attach. The introduction of small outline packages (SOP) offers the possibility of attaching prepackaged semiconductors to the substrate of hybrid circuits.

The hybrid circuit is usually encapsulated in a hermetic metal can, either singularly or in conjunction with other HICs, which may then be assembled as a through hole mounted component to a printed circuit boards.

Multi-Chip Modules - Multi-Chip Modules (MCMs) offer very high interconnect densities between several chips on ceramic (alumina) or silicon substrate. The module itself may then be assembled onto circuit boards via a smaller number of connections. It therefore provides a means of interconnecting several chips together in one module that requires very many interconnections between one another, but only a far smaller number to the rest of the circuit. In this respect MCMs resemble the older technology of HICs however they differ in that a much higher interconnection density is possible. MCMs are able to do this as they are assembled on multi-layer substrate. Their interconnection pattern on the substrate is usually produced by thin film deposition and etching techniques. The line spacings that can be produced by this method are of the order of one thousandth of an inch (25 microns), which compares to five thousandths of an inch (100 microns) which is the limit of the finest line width that can be produced on circuit boards.

The chips are interconnected to the conductor pattern on the substrate by through wire bonds, solder bumps, TAB or a combination of these technologies.

2-45
**Tape Automated Bonding** - Tape Automated Bonding (TAB) was developed in the mid 1970s [24][25] but did not assume commercial importance until the late 1980s [26]. The development of very high I/O devices has given this technology a new lease of life. The chip is connected via its bonding pads to through thermo-compression or eutectic bonds to an etched metal frame supported on a film carrier. The bond pads on the device are provided with solder bumps to aid thermo-compression bonding. Alternatively the bumps can be etched on the tape rather than deposited onto the device. The metal fan out pattern is attached to a continuous polymer tape to facilitate high volume assembly. The TAB process can be used to attach a fine fan-out pattern to a larger leadframe, a process known as inner lead bonding, or as a leadframe itself.

**Glob Top** - "Glob Top" coating is a very cheap, high volume production method used to seal a die from the environment. A single die is mounted on to an epoxy substrate with its electrical connections either solder-bumped or wire bonded to the board. The die is then coated and sealed to the board with a drop of setting sealant dispensed from a nozzle. Silicone rubber or epoxy compounds are used the major difference in these two approaches is that silicone compounds provide a rubbery compliant coat, whereas the epoxies provide a hard rigid coat. The epoxy glob-top coatings have a potential for greater thermal shrinkage stress because of the mismatch in c.t.e. with the board. The problem is much greater in epoxies designed for glob top coating than it is in epoxies used in transfer moulding. This is because the glob top epoxies have to be dispensed through a nozzle at relatively low pressures where as those used in transfer moulding are dispensed at much higher pressures, this means that the later can be loaded with higher concentrations of silica filler particles thereby imparting a lower c.t.e. to the compound.

### 2.9 Summary

This chapter has discussed the purpose of electronic packages, and the many functions that a package has to perform. Far from being a mundane "overcoat" for the electronic device inside it has been shown that the microelectronic package is a very sophisticate multi-functional engineered entity of some complexity which elegantly
overcomes the many mutually conflicting requirements that would otherwise compromises its design. An outline of the many different package types has been presented and the distinction between non-hermetic and hermetic packaging has been made. This is the choice between plastic and hermetic encapsulations, a choice which has historically been viewed as a choice between low cost or high reliability.

A number of relevant aspects of plastic packaging were expanded upon, the moulding compound type, its properties, constituents, and the moulding process itself. A brief outline of the choices available in hermetic packages, metal or ceramic, were also given as well as some of the more common package types for niche applications.

2.10 References


CHAPTER 3

MICROELECTRONICS
RELIABILITY

3.1 Introduction

The "Microelectronics Revolution" has occurred because of the availability of cheap, and widely available electronic devices. This would not have happened if the devices did not display a high degree of reliability. For electronic equipment to be highly reliable it is necessary for both component manufacturers and equipment designers to have an understanding of device failure mechanisms and their causes. Knowledge of these processes is also of importance to equipment procurement specialists so that they can predict the useful reliable lifetime of equipment which they may be considering purchasing. This knowledge would aid equipment manufacturers in choosing the correct level of device quality so as to assist in producing equipment with the required level of reliability. It is also necessary in the selection of the correct production and handling techniques so as to optimise product quality and competitiveness. Reliability has to be built into all levels of the manufacturing process from the device to the system level, it cannot be retrofitted.

This chapter reviews the failure mechanisms of microelectronic devices together with the improvements that have taken place in electronic package design and materials over the last two and a half decades. It is shown that these refinements have resulted in greatly increased device reliability. This information can aid the diagnosis of faults in microelectronic devices particularly those associated with packaging.
3.2 Failure Mechanisms

The failure mechanisms observed in microelectronic devices can be categorized into three classes:

1). Intrinsic - Built in defects
2). Intrinsic - Wear-out
3). Extrinsic - Electrical Overstress

**Intrinsic Failure Mechanisms** - These failure mechanisms may be considered as those inherent in the semiconductor device from the time of fabrication [1]. They maybe the result of built in defects resulting from poor manufacturing and so represent the weak population of devices in a batch, or they may be due to wear out mechanisms in perfectly manufactured components.

In the former case they are a result of, at best, sub-optimal and, at worst, poor manufacturing techniques or materials. These failure mechanisms exist from time zero and can result in a fault at anytime but are usually observed early in device operation and are responsible for the "infant mortality" failures seen in the well known "Bathtub curve". Such failures can be screened out by burn-in techniques after manufacture so that they do not find their way to the customer. Observation of "weak" devices in a batch of components can alert production engineering staff to the occurrence of problems at the manufacturing facility. Continual improvements in fabrication techniques should eventually eliminate such failures.

The second category of intrinsic failure mechanisms are where the device reaches the end of its useful life as a result of the chemical and physical processes inherent in its construction. Examples of this kind of failure are mirror degradation in laser diodes, loss of electrolyte in aluminium electrolytic capacitors and corrosion and interconnection failures in plastic packages.

**Extrinsic Failure Mechanisms** - Mechanisms of this type, such as electrical overstress, are a result of a random event that exposes the device to a transient voltage or current whose magnitude is greater than that which it is designed to withstand. This can be a result of inappropriate equipment design or the result of "load-dumps" on
supply rails or the interfaces to other equipment. One particular form of electrical overstress that can occur when devices are subjected to a transient electrostatic discharge is known as Electrostatic Discharge Damage (ESD). Such electrostatic discharges occur as a natural phenomenon in every day life. If a semiconductor device is subjected to a discharge of sufficient magnitude damage may result. Well established handling procedures for devices and circuit boards exist to protect against such failures. If ESD damage occurs it is likely to be the result of careless handling at the manufacturing, assembly or maintenance stages.

3.3 Defect Induced Intrinsic Failure Mechanisms

Although this study is primarily concerned with package related failure mechanisms in integrated circuits defect related failure mechanisms are briefly covered to help give a more complete understanding of semiconductor reliability. This can be useful in identifying failures during failure analysis. Defect related failure mechanisms are most usefully categorized according to the production stage at which they are introduced.

3.3.1 Substrate and Epitaxial Layer Failures

Cracks in the semiconductor die can occur during device fabrication particularly around the edge of the chip during the scribing and dicing stage. The silicon die is also prone to cracking in the region of the bond pads due to excessive pressure during the bonding process, which is can be aggravated if it occurs in the presence of oxide and bulk defects [2]. Such cracks can be difficult to identify as they are often hidden below the ball-bond or bond pad. These cracks can lead to low resistance leakage paths across p-n junctions, high resistance paths due to the interruption of metallised tracks and open circuits [3]. They may also act as channels for metal migration which can lead to short circuits.

The substrate can suffer from crystal defects such as dislocations, stacking faults and oxygen precipitates that can lead to excessive leakage currents in both MOS and bipolar devices, particularly if they are associated with metallic impurities [4][5]. Crystal defects have also been cited as responsible for the failure of devices operating
on a charge storage principle such as DRAMs and CCDs [6]. If the leakage current induced by these defects is large enough to collapse the depletion region of MOS transistors then the memory cell will not function and the stored information will be lost.

The presence of oxygen in silicon can cause the generation of "thermal donors" which can change the resistivity of the silicon wafer during processing which in turn alters the threshold voltage of MOS transistors. This is a significant factor when the dopant concentration of threshold-adjusting implants becomes comparable to the thermal donor concentration.

Inclusions, hillocks due to uneven etching, and scratches on the die surface, all contribute to increased failure rates. Defects can occur to the epitaxial layer due to preferential growth at substrate surface impurities, and can cause damage to oxides and masks causing pinholes.

3.3.2 Photolithographic Process Related Failures

Device failures due to errors in the photolithographic processes can occur at the die fabrication stage and can be the result of either contamination of the die or mask by foreign particles. This can be attributed to poor alignment of masks, or misuse of photo resist chemicals. Pin holes and oxide cracks can occur due to the presence of foreign particles on the photo-resist surface. These errors can manifest themselves as short circuits between metallisation either during production or during subsequent operation of the device at high temperatures [7]. Misaligned photo-resist patterns, and imperfect contact between mask and wafer can cause notches to be formed at the corners of the photo-resist. Poor adhesion of the photo-resist can lead to lifting during development and bridging of the photo-resist. These manifest themselves as poor production yield and poor reliability of the finished devices [7]. Poor adhesion of the photo-resist can cause undercutting of the etching process. Mask misalignment can prevent the alignment of metallisation layers through windows or via holes and so cause open circuits. Mask faults can cause the undesirable removal of oxide or metallization layers causing short or open circuits and poor ohmic contacts due to resist removal in the contact areas. Incomplete removal of resist can cause incomplete diffusion regions and short circuits. Poor etching of the oxide in the
contact areas leads to inadequate or non-existent contacts. Poor etching of the oxide layer in diffusion windows can lead to incomplete diffusion and incomplete etching of metallization can cause short circuits. Post etch cleaning is particularly important as the presence of residual etchant on the die can be responsible for the formation of leakage paths.

3.3.3 Diffusion Process Related Failures

Diffusion related failures can occur due to enhanced diffusion regions resulting from crystallographic defects [3][4][5]. This locally enhanced diffusion can result in spikes of dopant material diffusing into the semiconductor and can occur as a result of residual photo-resist. The presence of such diffusion spikes can cause high localized reverse leakage currents which are responsible for thermal degradation of p-n junctions [2]. Similarly, problems with photo-resist removal can cause incomplete diffusion [3]. Low breakdown voltages of p-n junctions have been reported due to extended diffusion which can result in under cutting of the oxide layer [2]. Oxide defects such as cracks and pinholes can result in the formation of undesired diffusion regions.

Impurity diffusion can cause two types of dislocations, diffusion-induced dislocations (DID) and emitter edge dislocations (EED), which appear around the edges of diffusion areas. In bipolar devices these dislocations cause excessive leakage currents in p-n junctions, due to an excess concentration of recombination-generation centres and localised tunnelling. They can also be responsible for the reduction in the current gain of transistors [8], short circuits due to enhanced diffusion at dislocations [9], and an increase in low frequency noise [10]. In MOS devices dislocations can cause a shift of threshold voltage [18] (due to an increase in silicon-oxide interface trap density), and a reduction in transistor transconductance [18], due to a reduction in surface mobility.

If metallic impurities such as gold, iron and copper are present in the diffusion system or the doping sources then these elements are likely to enter the silicon substrate during processing [11]. During cooling cycles these ions can form as precipitates which can cause the same effects to device characteristics as dislocations. Metallic ions tend to accumulate at the sites of dislocations, and their combined action is particularly troublesome. Owing to their high mobilities metallic impurities can
cause instabilities or device failures during operation at high temperatures [12].

3.3.4 Ion Implantation Faults

Ion implantation induced dislocations, which occur inside and around implanted areas, are similar to diffusion induced dislocations and their affect on device characteristics is almost identical [13]. Stacking faults can occur during ion implantation, or they can occur during subsequent oxidation. The effects of these stacking faults are the same as crystal defects, producing excessive leakage currents in both bipolar and MOS devices. As with diffusion faults, metallic impurities also tend to precipitate around stacking faults [6][14].

3.3.5 Oxide Faults

In MOS devices many of the reported failure mechanisms are attributed to failure of the oxide layer. If cracks in the oxide layer are present at the fabrication stage they can lead to the occurrence of undesirable diffusion layers and metallization short circuits to other areas of the device [15]. These metal to semiconductor contacts may be either Ohmic or Schottky. The formation of such short circuits can occurs when metallization is deposited through the crack during fabrication, or during device operation at high temperature, as the aluminum metallization reacts with oxygen from the oxide layer.

Time dependent breakdown of the oxide can occur at weak spots which may be a result of the etching process or from uneven oxide growth [16]. Time dependant breakdown can also involve the movement of contaminating alkali ions in the gate oxide. Where alkali ion contamination is the predominant failure mechanism the failure is associated with a high activation energy, other oxide breakdown mechanisms are only slightly affected by temperature. In either case the failure rate is affected by the applied voltage.

Oxide faults may occur due to thermal breakdown. This can occur at low voltages (10-15 volts), a much lower voltage than that associated with electrical breakdown, and is the result of oxide heating due to currents flowing through pores in the oxide [17]. Thermal breakdown, unlike electrical breakdown (for leakage
currents > 10nA), is reversible and usually occurs at the edge of the gate metallisation, or at the drain-to-channel diffusion edge, as here the electric field is greatest [18].

The presence of fixed positive charges in the oxide layer near to the silicon-oxide interface can affect the characteristics of both MOS and bipolar devices [19]. In MOS devices they can cause a shift in threshold voltage (observed as a reduction in n-channel and an increase in p-channel devices), a reduction in transconductance (particularly undesirable in switching circuits as it slows down switching time), and a shift in drain junction avalanche breakdown voltage (an increase in n-channel and a reduction in p-channel devices). In bipolar devices such fixed charges can cause a reduction in transistor current gain and a shift in collector junction avalanche breakdown voltage (a reduction in npn and an increase in pnp transistors). The density of such fixed charges may vary with time during the life of the device because of variations in temperature and applied bias. Unless the oxide layer is relatively free from alkali ions then ion drift will mask changes in fixed positive charge density.

The presence of neutral traps at the silicon-oxide interface affect the characteristics of both MOS and bipolar devices. In MOS devices their effects are to reduce transconductance, increase the drain junction leakage current, and increase low frequency noise. In bipolar devices they cause a decrease in transistor current gain, an increase in p-n junction leakage currents and an increase in low frequency noise. At sufficiently high values of temperature and gate bias, charges may accumulate at interface traps [20][21][22]. When compared with fixed positive charges, the effects on device characteristics of positively charged interface traps are seen to be the same, whereas negatively charged interface traps have the an opposite effect. The effects of interface traps are further complicated by the fact that their density can change with time over the life of the device. This changes in interface trap density can be masked by the drift of alkali ions.

The presence of alkali ions lead to the same effects as fixed positive charges. These mobile alkali ions are the ionic species Na⁺, Li⁺, K⁺, Cs⁺. They may be present as a result of a defective passivation layer, or residual etchant or photo-resist, and volatile species from the inside walls of the diffusion furnace [16][19].

In addition to the drift of alkali ions into the oxide bulk it is also possible for charge to spread out laterally from biased metal conductors [23]. The charges can
move either on the oxide surface or along the silicon-oxide interface. The effect of surface charge spreading is to invert the field region, this provides a conductive path between two diffused regions or it extends the p-n junctions through a high-leakage region. In this case leakage currents along the oxide surface can even be created between neighbouring conductors.

In scaled-down CMOS devices hot electron trapping can take place in the gate oxide layer, as process variations can lead to shorter channels than the design rules permit with the effect of threshold voltage shifts and source to drain breakdown. The effect may depend on circuit configuration, the most likely devices to be affected are enhancement pull-down transistors, whereas transfer gates and depletion pull-up transistors are less susceptible.

3.3.6 Metallisation Defects

The metallisation layer can sometimes be badly formed due to mask defects, or the presence of foreign particles or scratches. Cracks can occur in the metallisation during evaporation due to surface impurities, poor photo-resist, and mask defects all of which can cause open circuits. Poor adhesion of the aluminium metallization to the silicon can be due to evaporation of the metal on to a cold wafer or contamination on the wafer surface. Poor contact behaviour (open circuit, high resistance or rectifying behaviour) can be due to a reaction between the aluminium and a residual oxide layer present in the contact pads [24]. Poor execution of the metallisation alloying cycle can lead to large quantities of silicon entering the aluminium. This dissolved silicon can precipitate out at the aluminium grain boundaries causing increased contact resistance [20]. The diffusion of metallisation in to the thin oxide layer at gate regions can prevent the field effect and effect the action of MOS devices [3].

The alloying of aluminium and silicon can occur at "hot spots", such as thin the thin metallisation that can occur at window edges, and in contact pads with residual oxide, which forms a molten eutectic under the oxide layer thereby producing a short circuit.

3.3.7 Passivation Layer Defects
Holes in the passivation layer can be created during processing at points where the passivation comes into contact with hillocks in the aluminium [37]. Improper photo-resist coverage along the edges of aluminium conductors can result from a rounding of the oxide structure at this point. This can result in a gap in the passivation layer being formed during the opening of the contact pad area prior to etching [37]. To relieve the build-up of stresses in glass passivation layers phosphorous is added. The amount is carefully controlled at around 2%, as excess levels can lead to failures [25][26].

3.3.8 Bonding Defects

The gold of the bonding wire can become contaminated by carbon, causing several different types of defects. Carbon inclusions and absorbed carbon films can be formed during the bonding operation [27]. As part of the eutectic bonding process the aluminium diffusion front moves into the gold but it is likely to stop at carbon inclusions and at micro-voids. If this occurs the bond will be weakened and failure can occur at the point where the diffusion front stops. Impurities in the gold are expelled by the moving diffusion front. When the concentration of impurities becomes critical precipitation occurs and voids develop. These voids form over time and at increased temperature they can cause micro-cracks in the bond wire which results in eventual bond failure.

A similar process occurs where the migration of silicon into aluminium bonding wires increases their electrical resistance and causing embrittlement [3]. Failure of the thermo-compression ball bond can occur due to wire creep. This is a stress induced fracture of the bond wire which most frequently occurs within at a height of several wire diameters above the ball bond. The wire failure is characterised by braking along slip planes or fracture at grain boundaries [28].

Bonding wire failure, or shorts between bonding wires, can occur due to a process known as wire sweep. With the trend towards packages with ever greater numbers of I/O connections (>40) the pitch of the bond pads on the die decreases bringing the bond wire loops ever closer together. This can cause problems when the die is encapsulated in a moulded plastic package. The moulding compound flows under pressure over the die surface during the transfer moulding process exerting a
pressure on the bonding wires which may force them into contact with one another thereby causing short circuits. In some cases the bonding wires may even fail due to this stress.

3.4 Intrinsic Wear-out Failure Mechanisms

Intrinsic wear-out failure mechanisms are those that cause the failure of perfectly manufactured components at the end of their useful life. Examples of these processes are moisture permeation through packages and passivation layers, corrosion, electromigration and the degradation of materials with time. The extent to which these various processes contribute to device failures is the subject of some speculation. Stojadinovic [12] shows the percentage contribution of each type of failure mechanism to the results of two different test studies on CMOS ICs. The two sets of results differ dramatically in the percentages of failures attributed to different failure mechanisms. The data from a study conducted by the Marshall Space Flight Centre (MSFC) attributes the largest proportion of IC failures to package failure mechanisms (42.3%) whereas a similar study at the Rome Air Development Centre (RADC) attributes only 1.3% of failures to packaging faults. Instead the RADC report attributes the majority of failures to oxide faults. Clearly such conflicting data indicated the confusion that exists in ranking failure mechanisms. Clearly both oxide and package failure mechanisms needed further investigation.

3.4.1 Electromigration

Electromigration is the movement of metal atoms under the influence of high current densities. The effect is also dependant on temperature. At operating temperatures up to 230°C electromigration of the aluminium metallization can occur. This leads to the formation of holes near the negative poles and hillocks near the positive poles [29]. This is due to the continuous impact of electrons on the aluminium grain boundaries causing the grains to move in the direction of electron flow. This is known as the mass transport of aluminium migration and is controlled by the grain boundary diffusion mechanism. Electromigration is influenced by the metallisation grain size with smaller grain sizes being more easily transported with an activation
energy of 0.45eV being suggested. Analysis of this failure mechanism is usually conducted at an elevated temperature of 180°C and current density of $J>10^6$ A cm$^2$. This phenomena has been extensively researched for aluminium on silicon [30] and this failure mechanism has been almost eliminated.

At temperatures greater than 230°C the electromigration of silicon ions occurs leading to device failure due to the formation of pits in the silicon at the negative pole, and an increase in resistance in positive biased regions [29].

More recently it has been shown [31] for gold ball bonds that direct current stress of current densities over $10^8$ Am$^2$ causes electromigration effects at the Au-Al interface. It is claimed that the addition of 1% copper to the metallisation strongly retards void formation and hence open circuit failures.

Metal migration due to mechanical stress relief has also been reported. In this form of migration metal atoms are transferred from areas of high stress to areas of lower stress. This stress equalisation process results in "whisker growth", a failure mechanism that can result in short circuits. Once initiated the process will continue until sufficient metal has been moved to equalise the stress [32].

### 3.4.2 Radiation

There are two main sources of radiation that can effect semiconductor devices.

i) External Sources; Gamma, X, and Cosmic rays.

ii) Intrinsic Sources; alpha and beta radiation associated with the package materials.

The external sources of radiation are particularly relevant to semiconductor devices intended for use on board spacecraft. Intrinsic source are covered in section 3.4.3.6 on package related failures. Radiation effects semiconductor devices through the formation of electron-hole pairs within the bulk of the device. The way in which the radiation effects the device depends on the device type. Silicon bipolar and GaAs transistors display an increase in low frequency noise, higher leakage currents and a reduction in transconductance, with an increase in soft errors in digital devices [33]. GaAs MESFETs however are relatively radiation hard when compared to Silicon
devices. This is due to the fact that they are majority carrier devices and the absence of an oxide layer also makes them less sensitive to radiation [34].

3.4.3 Package Related Failure Mechanisms

There are many aspects of package design that have a bearing on device reliability. The failure mechanisms associated with package related failures depend very much on the type of package being considered (hermetic or plastic), however there are some mechanisms that are present in both classes but may be more severe in one type than another e.g. corrosion or intermetallic formation. The search for the optimum combination of package materials has been taking place over the last 25 years [35][36][37]. Plastic packages are considered to be non-hermetic and as such can allow the passage of moisture and other solvents, often bearing ionic species, through to the die. The presence of moisture either with and without certain ionic species can lead to a number of failure mechanisms.

3.4.3.1 Thermally Induced Stress Failure Mechanisms

Thermally induced stress in packages result from the necessary use of different materials with dissimilar coefficients of thermal expansion (cte). The presence of such stresses can lead to a number of failure mechanisms. Such failure mechanisms are most common in plastic encapsulated devices where the moulding compound is in contact with the device passivation layer and the bonding wires are embedded in its bulk. They are rare in hermetic packages as the die and bond wires tend to be housed in a cavity. The areas of the package that usually fail due to these types of stresses are, the passivation layer, the chip metallization and the bonding wires.

Passivation Layer - Cracks may occur in the passivation layer due to induced stresses resulting from mismatches in the coefficients of thermal expansion between passivation layer, metallisation, silicon and package material.
**Metallisation deformation** - In the late 1980s device features in CMOS technology reached the sub-micron level and today (1994) 0.5 micron line widths are possible. It has been predicted [38] that, by the end of the century, 0.25 micron devices will be in production and, with the advent of X-ray lithography, even 0.1 micron will be possible. With present materials the differential thermal shrinkage between moulding compound and silicon die can cause deformations of several microns, deformations that are approximately the same as the present width of conductor paths. This effect is observed at its most severe at the periphery of the chip and on aluminium conductors that run perpendicular to the shrink direction [39],[40]. To avoid deformations in conductor lines of even thinner width moulding compounds with even lower c.t.e will need to be developed. If such devices were encapsulated in the present generation of moulding compounds the package related stresses would deform such fine metallisation features that they would be displaced across the die surface possibly towards adjacent paths which could result in short circuits between conductors.

Other plastic package stress related metallisation failures, in opto-electronic component have been reported [41], as have open circuits in device metallisation [42]. This type of problem is amenable to stress modelling by computer using finite element analysis [43]. It is also possible to measure these package induced stresses by encapsulating piezoelectric sensors in moulding compound and cycling the assembly over the operating temperature range of the device [44].

**Bonding-Wire Failure** - Plastic encapsulated devices have been observed to display open circuit or intermittent open lead connections as a result of thermal cycling tests [45]. This is due to differences in c.t.e. of the silicon die and plastic moulding compound. These failures are observed as a fracture about the centre of the bond wire due to tensile stress. A combination of elevated temperature and tensile stress is required to achieve the grain growth which leads to this particular bond wire failure mechanism. A mechanically induced stress related bonding-wire failure occurring at the heel of the bond has been reported [46]. The problem of bonding-wire failure has also been observed in hybrid circuits [47].
Filler Particle Induced Stress - An interesting stress induced failure mechanism in the column-lines of dynamic random access memories has been observed [48]. The dice were reported as not having a coated surface and the encapsulating plastic resin contained conventional filler with a particle size of between one and one hundred and forty microns. When comparisons were made between DRAMs encapsulated in ceramic packages and those in plastic packages the plastic encapsulated devices showed an occurrence of cumulative failures of up to 40%. Furthermore the failed chips recovered once the encapsulating plastic resin was removed. It was concluded that the failed column-lines resulted from the presence of sharp filler particles pressing on the chip surface. The package is in compression at normal room temperature after the plastic resin has cured. This pressure causes piezoresistive effects in MOS devices, and the induced voltage change is sufficient to cause malfunction of the DRAM's sense amplifier circuits. If this sensitive part of the chip was to suffer from filler particle induced stress then a column line failure could occur. This effect can be alleviated by the use of smaller filler particles or the application of a coating over the chip surface.

3.4.3.2 Failures Due to Non-Hermetic Packaging

Owing to their non-hermetic nature dice encapsulated in plastic packages can suffer from a number of moisture induced failure mechanisms. Moisture may enter the package either by bulk absorption through the moulding compound or along the leadframe/moulding compound interface. The mechanism by which this occurs is complex but it may be broken down into four basic steps.

1. Permeation of the plastic moulding compound by moisture.
2. Diffusion of moisture either through the bulk of the passivation layer or through defects.
3. Transport of ionic species from the moulding compound, process residues and the external environment by the absorbed moisture.
4. Electrochemical reaction between the absorbed moisture which acts as an electrolyte and the metallisation resulting in corrosion.
Moisture Permeation Mechanisms - Moisture permeation is a relatively quick process when compared to the total time required for failure to occur [49]. Besides bulk absorption moisture can ingress along the plastic/lead frame interface. This can be due to poor adhesion between plastic and metal or due to slight separation induced by the lead forming process. In a humid environment moisture and external contamination can migrate along the leadframe, across the wire bonds and on to the die [50].

The process by which moisture penetrates a polymer is referred to as permeation as it describes the amount of one substance (water) passing through another (plastic) in a given time. The permeation process depends on a number of factors such as the shape and nature of the filler particles, relaxation of the polymeric matrix, the filler/matrix interface and the solubility of the components present in the package. The coefficient of transport varies through the material from one domain to another and is therefore said to be a discontinuous function of space.

The absorption of water in glassy unfilled epoxy resins can produce various kinds of anomalies. The transport mechanism exists in two forms, sorption and permeation. The difference between sorption and permeation is that permeation only makes use of connected pathways while sorption also fills the dead-end pathways.

In filled systems (such as the moulding compounds used for the encapsulation of integrated circuits by the transfer moulding process) the presence of a filler leads to a reduced cross-sectional area for diffusion and an increased path length. Hence permeation is considerably slowed down. The second factor known as the tortuosity factor describes the increased path length the moisture experiences in negotiating its way between all the filler particles in its path. It describes the ratio of path length through the maze of filler particles to the linear thickness of the encapsulation. The shape of the filler particles play a an important factor in controlling permeation. Shapes such as spheres or cubes are not as effective as thin platelettes lying perpendicular to the direction of moisture ingress.

Models exist that consider the increase in path length produced by filler particle loading whilst other models consider the absorption of penetrant by the filler or filler interface. Two important types of model are briefly described.
Polymer Filler Interaction Model - In this model the penetrant molecules travel through the media by jumping from hole to hole. The holes are created by random chain motions to accommodate the presence of other species. This mobility affects both the glass transition temperature and the relaxation behaviour of the polymer. It has been observed [51] that filling an epoxy resin with glass spheres raises the glass transition temperature $T_g$ of the material while reducing its permeation much more than could be predicted by previous theories based on the tortuosity concept for a given volume fraction of filler. In materials such as epoxies, where the matrices shrink on cooling, there is generally a long range state of compression about the filler particles. Hole formation would therefore be inhibited as a consequence of the reduction in free volume.

This approach to modelling permeation through a polymer only considers the morphology of the material in a rather limited way by considering the filler particles as either ideal random arrays of spherical particles in a continuous matrix or as completely ordered structures.

Percolation Theory - The simplification inherent in the filler interaction model is overcome in the percolation model [52][53][54][55][56]. In this model the structure of a composite can be characterised by geometric and topological parameters which describe the two phases A and B. The geometric parameter describes the shape of the second phase A (filler particles), while the topographical parameter describes the degree of contact of the phases within phase B. A composite material can then be described as a network in which clusters of phase A exist within a continuous matrix of phase B.

3.4.3.3 Corrosion

Corrosion occurs as a result of moisture ingress into plastic packages [57] and a number of chemical reactions are responsible for this process. The principles of corrosion which are applicable to electronic devices have been reviewed [58]. Corrosion can be defined as the destructive attack of a metal by a chemical or electrochemical process. Such reactions have to be considered from both their thermodynamic...
and kinetic aspects. The relative reaction tendencies are given by thermodynamic calculations, however these do not give a good idea of the actual rate of a reaction, a better estimate is available from the reaction kinetics. The emf of a corrosion cell is given by the Nernst equation (1), which describes the general chemical reaction (2).

$$E = E^0 - \frac{RT}{2.3nF} \log \frac{A_p A_q}{A_m A_l}$$

$$IL + mM \rightarrow pP + qQ$$

Where $E$ is the cell emf, $E^0$ is the standard oxidation potential, $A$'s are activities, $R$ is the gas constant, $T$ is absolute temperature, $n$ is the number of chemical equivalents, $F$ is the Faraday constant, and $l,m,p,q$ are the quantities of the reactants $L,M,P,Q$ in moles.

Whether a reaction will proceed or not is governed by the change in free energy (3).

$$\Delta G = -nFE$$

If $E$ is positive then $\Delta G$ is negative and the reaction can proceed as written at a rate determined by the reaction kinetics. If $E$ is negative however then $\Delta G$ is positive and the reaction can not proceed at any rate. Metals with large positive values of $E^0$ are very reactive whereas those with large negative values are inactive. The reference point for these values is hydrogen, the hydrogen electrode is taken to be 0.00 Volts. A corrosion cell will consist of an anode and cathode electrically connected by an external electron path and an internal electron path, the electrolyte. Such a corrosion can be microscopic in size with microscopic anode and cathodes sometimes present in a single metal strip.

There are essentially three types of corrosion cells; Galvanic (dissimilar metal cells), concentration cells, and anodic (impressed emf cells). The anodic cell is the type of most interest in semiconductor reliability. In this type of corrosion the cell consists of two essentially identical electrodes in contact with an electrolyte which has
the same concentration at each electrode. An external voltage (electrical bias) is impressed on the circuit and a potential difference between the electrodes is created. One electrode (the anode) is biased positive with respect to the other and anodic corrosion occurs at that electrode. This is seen in integrated circuits when a potential difference occurs between metallisation tracks in the presence of an electrolyte (moisture).

The rate at which the corrosion process takes place is governed by the reaction kinetics. In considering reaction kinetics two other factors have to be considered, the metallurgical and environmental conditions. The metallurgical conditions are electrode composition and morphology, conditions such as alloy content, impurities phases present, grain sizes are surface textures. Environmental conditions are temperature, relative humidity, ionic contamination and the applied electrical bias voltage.

Two phenomena which greatly affect the rates of corrosion are passivity and polarization. Aluminium is a good example of passivity, with a $E^0$ of +1.66 Volts aluminium would appear to be a reactive metal. However owing to the presence of an adherent native oxide film it is in practice naturally passivated and is consequently far less reactive than it would appear from its position in the electrochemical series. If the oxide layer is breached then corrosion can be severe. The other process that can be responsible for the anomalous rate of reactions is polarization of the electrolyte. This causes a change in electrode potentials from their equilibrium values and is a result of current flow in the circuit. There are two types of polarisation phenomena; concentration polarisation, which is a change in the ionic concentration of the electrolyte in the vicinity of the electrode, and activation polarisation which results from slow electrode reactions. The actual electrode potentials depend on the magnitude and direction of the external and internal cell currents. In practice both anodic and cathodic polarisation is possible. Decreases in the corrosion current and hence corrosion rate can be brought about by intentional polarisation.

**Corrosion of Aluminium Metallisation** - The aluminium metallisation in integrated circuits can suffer from both anodic and cathodic electrolytic corrosion. It may also
suffer galvanic corrosion in the presence of migrating metal ions. Fe$^{2+}$ and Cu$^{2+}$ can cause galvanic corrosion of aluminium by destroying its passivity, a process sometimes referred to as dissimilar metal corrosion. Most elements are cathodic with respect to aluminium when in direct contact. A critical factor in the corrosion of aluminium metallization, irrespective of the attacking chemical species, is the presence of defects in the passivation layer, [59][60][61]. These defects are usually in the form of either pinholes, as result of poor deposition, or stress induced cracks.

*Cathodic Corrosion of aluminium* - Cathodic corrosion of aluminium has been extensively studied, [58][62][63][64][65][66][67][68]. The following reaction has been suggested for the cathodic corrosion of aluminium by hydrated chloride ions [69].

\[
2Al + 6HCl \rightarrow 2AlCl_3 + 3H_2 \quad (4)
\]

\[
Al + 3Cl^- \rightarrow AlCl_3 + 3e^- \quad (5)
\]

\[
AlCl_3 + 3H_2O \rightarrow Al(OH)_3 + 3HCl \quad (6)
\]

*Anodic Corrosion of Aluminium* - The chemical reaction for the anodic corrosion of aluminium metallisation in plastic packages has been reported [70]. It is a four stage process:

1). The chloride anion (Cl$^-$) is adsorbed onto the passivating aluminium oxide film.
2). The chloride ion reacts with the aluminium ions in the oxide weakening its protective properties.

\[
Al^{+++} + 2(OH)^- + Cl^- \rightarrow Al(OH)_2Cl \quad (7)
\]

3). Thinning of the oxide by electrochemical dissolution.
4). Direct attack of exposed aluminium by chloride ions.

$$4\text{Al}^{+++} + 4\text{Cl}^- \rightarrow 4\text{AlCl}_4^-$$  \hspace{1cm} (8)

$$\text{AlCl}_4^- + 2\text{H}_2\text{O} \rightarrow \text{Al(OH)}_2\text{Cl} + 2\text{H}^+ + 3\text{Cl}^-$$  \hspace{1cm} (9)

The last equation illustrates the re-cycling of the chloride ions to initiate yet further corrosion. An important consequence of this is that only a small quantity of chloride ions (p.p.m. levels) are required to produce extensive corrosion. Hydrolysable chlorine may be present in the moulding compound as a residue of the reaction between novolac resin and epichlorohydrin which is used to produce epoxy novolac resin. Alternatively chloride ions may permeate into the package carried along with the ingress of moisture. One of the most important reasons for the decrease in occurrence of corrosion failures in plastic encapsulated semiconductor devices over the past two decades has been the reduction in hydrolysable chloride in the plastic moulding compounds and processing chemicals used in devices fabrication.

Improvements in the quality of passivation layers has reduced the occurrence of aluminium metallisation corrosion and corrosion is now more frequently observed at the bond pad [71]. This area of the die is left exposed to allow connection of the bond wires and is susceptible to corrosive attack by anodic corrosion. Normally the positively biased aluminium components would be protected by the aluminium's natural passivation, however chloride ions migrate to the positively biased bond pads where they break down the naturally occurring oxide film and expose the aluminium metal allowing corrosion to take place.

*Aluminium corrosion due to phosphorous* - Another potential source of corrosion is the hydration of phosphorous from the passivation layer to form phosphoric acid. Phosphorus is added to silicon dioxide passivation layers as a stress relief additive to prevent cracking during deposition and thermal cycling. The phosphoric acid produced by the action of absorbed water on the doped glass reacts with the device's aluminium metallisation and causes corrosion, in particular at the bond pads. The effects of
phosphorus doped glass on the corrosion of aluminum has been studied [72], and it was shown that the rate of corrosion was dependent on the concentration of phosphorus in the glass, the ambient relative humidity and temperature. The surface conductivity of moisture films in the presence of phosphorus doped polysilicate glass (PSG) and the rate of corrosion of aluminium metallization has been reported [73].

*Aluminium corrosion due to bromide ions* - Brominated biphenol compounds are added to the moulding compound to reduce flammability. At high temperatures (>150°C) these brominated fire retardant compounds break down and release bromine ions that can be hydrated in the presence of moisture. The presence of hydrated bromine ions can cause corrosion to exposed aluminium parts, the reaction is similar to that for chlorine.

*Corrosion of Aluminium by Sodium Ions* - The exposed aluminium components of the die are also susceptible to attack by sodium ions [65][74][75]. The chemical reaction responsible for this corrosion process is:

\[
2\text{Al} + 2\text{NaOH} + 2\text{H}_2\text{O} \rightarrow 2\text{NaAlO}_2 + 3\text{H}_2
\]  
(10)

\[
\text{Al} + 3\text{OH}^- \rightarrow \text{Al(OH)}_3 + 3\text{e}^-
\]  
(11)

\[
2\text{Al(OH)}_3 \rightarrow \text{Al}_2\text{O}_3 + 3\text{H}_2\text{O}
\]  
(12)

The rate of corrosion of aluminium has been shown to be related to the conductivity of the absorbed moisture film over the die [76].

**3.4.3.4 Intermetallic Compounds**

The wire bonding to the semiconductor die is one of the weakest areas in device packaging. The most widely known problem involves the Au-Al interface [77][78]. It has been noted [79] that intermetallic compounds between the gold and aluminium form at the Au-Al interface when gold wires are bonded to aluminium.
These intermetallic compounds are not harmful but their presence indicates that the bond integrity may have been degraded. These intermetallic compounds AuAl₂ (purple plague) and Au₅Al₂ (white) are brittle and any wire flexing coming from vibration or thermal cycling is more likely to result in failure if these compounds are present at the interface.

At elevated temperatures aluminium diffuses rapidly into the aluminium rich AuAl₂ phase and leaves behind voids (Kirkendahl voids) in the Al-Au₅ boundary. If excessive intermetallic compounds are formed the voids may increase to such a size that an open circuit may occur and bond pad lifting may take place. Some intermetallic compound formation is unavoidable if gold/aluminium junctions are heated above 400°C, as in sealing ceramic packages. Impurities in gold, such as thallium, have been shown to form low melting point eutectic that weaken grain boundaries in thermocompression ball bonds [28][80][81].

Catastrophic failure by this method may be prevented however by minimising the time spent at elevated temperatures, assuring the purity of the gold and aluminium and paying attention to the thickness of metallization layers. Shih [82] has observed that the formation of gold-aluminium intermetallic compounds at the bonding site is greatly reduced when the bond is heated in the presence of hydrogen.

Further complications arise in plastic encapsulated devices where the wire bonds are encapsulated in epoxy moulding compounds. It has been reported that Au-Al intermetallics at the bond interface undergo a structural change when heated in the presence of epoxy encapsulants [83][84][85][86]. These have been reported as associated with the Kirkendahl voiding mechanism and the formation of purple plague [87][88]. Ritz et al [89] showed that the decomposition reaction is accelerated when the bonds are aged in the presence of epoxy moulding compounds at temperatures of 175°C to 200°C. An analysis of the outgassing products from the epoxy linked the bond degradation to the presence of halogenated flame retardants. The activation energy associated with the release of the organic brominated compounds is very low 0.24eV, similarly the activation energy associated with the release of ionic bromides
(especially HBr) is also low (0.3-0.4eV) [90]. The bromine liberated from these compounds react with the gold rich intermetallics to form AlBr₃. This is then easily oxidised to Al₂O₃, with the release of free bromine ions. The reaction is therefore autocatalytic with the bromine free to start the corrosion cycle over again. Bond failure will then occur when enough aluminium oxide has formed between the gold ball and the intermetallic structure, whence bond lifting can occur.

This bond lifting effect in plastic packaged ICs has been studied at temperatures between 121-135°C using non saturated autoclave testing [91]. An almost complete loss of bond strength after 300-400 hours was observed. The bond lift effect is attributed to the presence of antimony trioxide (Sb₂O₃) in the moulding compound. This is present in the moulding compound as an aid to preventing the aforementioned bromine induced bond degradation by trapping the outgassed bromine species [92][93].

A further chemical induced failure mechanism brought about by high temperature stress has been reported [94] where packages assembled by the tape automated bonding (TAB) method have failed due to a chemical reaction between the epoxy moulding compound and the materials of the device support structure. In automated beam-tape assembly the wafer is modified by the addition of elevated bond pads which are firmly adhered to the underlying basic level of the interconnections. The beam tapes used in this process are fabricated by etching bare copper foil supported on a thin polyimide plastic film. At temperatures greater or equal to 150°C the copper support structure is corrosively attacked by constituents of the moulding compound and conductive paths are formed between oppositely biased conductors which result in electrical short circuits. No chemical reaction was suggested nor was the corrosive constituent of the moulding compound identified.

Khan et al. [95] report the high thermal stability of cresol epoxies which are brominated by specially tailored brominating agents. These impart a high C-Br bond energy making the plastic more thermally stable. This results in much longer times to decomposition at high temperatures. This increased stability of the moulding
compound reduces the risk of both aluminium metallization failures or Au-Al intermetallic formation.

3.4.3.5 Package Cracking in Surface Mounted Components

Several researchers have reported the cracking of plastic encapsulated surface mount integrated circuits during reflow soldering operations [96][97][98]. Anjoh and Nishi [97] attributed this to the absorption of moisture from the atmosphere prior to soldering. The moisture expands rapidly as the plastic is suddenly exposed to the soldering temperatures (typically 220°C) the resulting rapid evolution of steam inside the plastic cracks the package with explosive force. This phenomena has been named the "pop-corn effect". Calculations on the rate of moisture absorption and desorption for various moulding compounds over the range of humidity (50-100%RH) lead to the conclusion that there were no moulding compounds capable of guaranteeing crack free assembly so attention was turned to developing moisture proof packaging, the so-called "Dry Pack" for SMD storage and distribution. The devices are packaged in this medium immediately after production and the package is only opened prior to board assembly. It was reported that devices stored in this manner had ten times the shelf life of unprotected devices. Fukuzawa et al [98] reported serious package cracking in SOPs and PLCCs stored for a year under normal component storage conditions. When the devices were baked at 150°C for 16 hours prior to reflow soldering then no cracks could be detected in the packages suggesting that the absorbed moisture could be effectively driven back out of the package.

3.4.3.6 Radiation Induced Soft Errors

Alpha particle induced soft-errors were first described by May and Woods in 1978 [99]. They manifested themselves as a random, nonrecurring single-bit change in the information stored in a memory cells. They occurred in dynamic random access memory (DRAM) devices and were a result of the passage of an alpha-particle through an active region of the device upsetting the balance in electron-hole pairs and so altering the cell's logic state [100]. However no physical damage occurred and the cell operated correctly after the next read/write cycle.
The alpha particles originated from traces of uranium and thorium found as impurities in the filler particles of the plastic packaging materials. For this mechanism to occur the source of the alpha particle must be located close to an active region on the die typically within 50 microns. This is because the alpha particles have only a very short range in solids before absorption occurs. The original source of silica for filler particles was from certain mines in South America which exhibited naturally occurring low alpha particle counts. By the mid-nineteen eighties however synthetically produced silica filler particles were being manufactured with significantly lower alpha activity than was achievable from mined sources. In the mean time many manufactures provided the top surfaces of their DRAM dies with a very thin (typically 30microns) overcoat of silicone elastomers or polyimide resins to act as a barrier to alpha particles. The provision of extra electronic circuitry to provide parity checking on most memory applications also helped alleviate some of the problems associated with soft errors.

Hermetic encapsulated DRAMs are also at risk from alpha-particle induced soft errors. Here the sources of alpha particles emission are the lid in side brazed packages (gold-plated Kovar), the ceramic body materials and sealing glasses and potentially from air borne radon in the cavity which is in contact with the die surface [101]. Levels of the alpha-particle activity is extremely low and are at the limit of present counting equipment (>0.001 alpha particles/hour) [102]. Radiation induced soft-errors are not limited to emissions from package materials. Very rarely Cosmic Ray interactions with the active regions of MOS memories can also induce soft errors [103].
3.5 Extrinsic Failures

3.5.1 Electrical Overstress

Electrical overstress (EOS) results from improper handling or application of a device. Transient voltage and current pulses can cause brief temperature rises in the active regions of devices [104]. This failure mechanism is associated with the development of a "hot-spot" in the semiconductor active region which results from some external applied electrical stress. The hot-spot is a result of the current density being great enough to cause localised melting of the semiconductor, metallisation or oxide. The melting process can result in the formation of a low resistance path due to metal migration.

The resistivity of doped silicon as a function of temperature initially increases with increasing temperature until a point is reached where the material begins to exhibit a negative temperature coefficient of resistivity. The rapid decrease in resistivity above this transition temperature results in an increase in current and therefore current density to any silicon device subjected to constant voltage source at temperatures above this transition temperature. This leads to increased heat dissipation which further lowers the resistivity of the silicon. This heating effect due to this positive feedback process is known as thermal run-away. This process can cause irreversible damage and in the most extreme cases melt the silicon [105].

3.5.2 Electrostatic Discharge

Electrostatic discharge (ESD) is a particular type of EOS where electronic devices are damaged or destroyed by the discharge of naturally occurring static electricity through the device. It is possible for static build up in the working environment to induce voltages in the range of 100V to 20kV. The air is susceptible to charging as is human skin and many plastics. Studies have shown [106] that many simple movements under taken by people such as walking across a vinyl carpet, arising from a foam cushion, or even picking up a polyethylene bag can all induce voltages of several thousand volts, sufficient to cause device damage. In order that the risk of ESD damage be assessed and its effects modelled a human body discharge
model has been developed and a standard discharge model is defined in MIL-STD 883C [107]. This is used to model the build up of static electricity on the human body by a combination of triboelectric, induced and capacitive effects. The model consists of a capacitance whose value depends upon the charged area and the separation from ground, a series resistance, the value of which depends on the level of atmospheric moisture and conductivity of the leakage path. The capacitance has been reported to be in the range 50pF to 450pF, with 100pF being commonly used. The leakage resistance can range from 100 Ohms to over 100kOhms with 1.5k being commonly chosen. The capacitor can be charged up to the voltage of the required discharge and then discharged through various electronic devices to assess their susceptibility to ESD damage. Using this ESD human body model electronic components have been categorised into three levels of sensitivity according to the magnitude of the voltage required to damage them, this is shown in Table I.

Table I Component Sensitivities to ESD

<table>
<thead>
<tr>
<th>Class</th>
<th>Sensitivity</th>
<th>Components</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class 1: (0 to 1kV)</td>
<td>Unprotected MOS (ICs and Discrete)</td>
<td>Low power Si controlled rectifiers</td>
</tr>
<tr>
<td></td>
<td>Small geometry Schottky Logic</td>
<td>Precision IC voltage regulators</td>
</tr>
<tr>
<td></td>
<td>Junction field effect devices</td>
<td>Low power (&lt;1W) thin film resistors</td>
</tr>
<tr>
<td></td>
<td>Microwave and VHF transistors</td>
<td>VLSICs with dual level metal</td>
</tr>
<tr>
<td>Class 2: (1 to 4kV)</td>
<td>Protected MOS (CMOS, NMOS, PMOS)</td>
<td>Monolithic ceramic capacitors</td>
</tr>
<tr>
<td></td>
<td>Standard Schottky (Logic ICs and Discrete)</td>
<td>High speed bipolar logic (ECL)</td>
</tr>
<tr>
<td></td>
<td>Bipolar Linear ICs</td>
<td>Bipolar Linear ICs</td>
</tr>
<tr>
<td>Class 3: (4 to 15kV)</td>
<td>Low power diodes and transistors</td>
<td>Quartz and piezoelectric crystals</td>
</tr>
</tbody>
</table>

The physics of ESD damage to electronic devices depends on the family of device. MOS devices suffer breakdown of the thin oxide layer (typically 0.1µm) at
their gates and this results in a permanently degraded leakage characteristic. CMOS circuits when energised are susceptible to "Latchup". Latchup is a parasitic pnpn avalanche effect usually caused by the application of a transient on the input or output of a device which exceeds the supply voltages so that the parasitic device is triggered on. With both complementary transistors turned on the power supply is short circuited so that overheating and catastrophic failure can occur. In Schottky and PN (bipolar) devices ESD can cause destructive reverse breakdown where the instantaneous power of the discharge generates enough heat to melt the silicon and metallisation resulting in catastrophic failure. ESD failure of MOS structures [108] and GaAs MESFET structures [109] have both been extensively investigated.

3.6 Types of Failure

Device failures may be categorised as being of one of two types either a degradation failure or a catastrophic failure. It is important that failures are correctly categorised for correct analysis of reliability data.

3.6.1 Parameter Drift Failures

A degradation failure is where a device parameter changes or drifts with time to such an extent that the change is so great that the device no longer complies to its specification.

Parameter drift is often observed during accelerated life testing, but the nature of the degradation is often very device specific. Sometimes the rate or magnitude of parametric drift of a certain type of device may prove to correlate well with its time to failure so that early monitoring of drift can provide a useful method of reliability prediction.

For example it has been reported [110] that npn silicon transistors suffer from an increase in current gain with time at low bias current during high temperature storage. The drift in gain is correlated with the initial measurement of 1/f noise. This was attributed to the modulation of carrier traps at the Si/SiO₂ interface leading to Si surface recombination. It was suggested that measurement of initial 1/f noise may be used as a reliability indicator to predict $h_{fe}$ degradation in bipolar transistors. Similarly

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a correlation between gain drift and initial noise level in pnp silicon transistors under high temperature stress (150-275°C) with applied reverse bias has been observed [111]. In this study however gain was found to decrease with stress duration.

Changes in the capacitance and dissipation factor (measured at 10 KHz) of passivation layers subjected to HAST (159°C/85%RH) have been noted [112]. This process has been exploited to monitor the rate of moisture ingression through passivations layers of various compositions and thicknesses.

3.6.2 Catastrophic Failures

Catastrophic failures are characterised by the complete failure of the device to function. They are often the result of extensive degradation caused by the result of a single stress event such as electrostatic discharge or bond wire failure. They are often detected as electrical open or short circuits. Failures of this type are known as event dependant failures.

3.7 Reliability Measurement

Reliability is defined by British Standards [113] as; "The ability of an item to perform a required function under stated conditions for a stated period of time". Reliability as a function of time can be represented mathematically by a reliability function $R(t)$ which is the defined by equation (13).

\[
R(t) = \frac{N_s(t)}{N_o} = \frac{\text{Number of Surviving Components after Time t}}{\text{Initial Number of Components}}
\] (13)

The number of components failing in time $t$ is given by (14).

\[
N_f(t) = N_o - N_s(t)
\] (14)

The probability of a component failing is given by the mean time to failure MTBF and is given by (15) where the $i$th device fails after $t_i$. 

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\[ MTBF = m = \frac{1}{N_o} \sum_{i=1}^{N_o} t_i \] (15)

The failure rate \( \lambda \) is the reciprocal of the MTBF as is shown in (17).

\[ \lambda = \frac{\text{Number of Failures in a Specified Time}}{\text{Number of Surviving Components}} \] (16)

\[ = \frac{1}{N_s} \frac{\Delta N_f}{\Delta t} = \frac{1}{N_s} \frac{dN_f}{dt} = \frac{1}{MTBF} \] (17)

The failure rate is the negative of the survival rate so the expression for MTBF can be rewritten as (18).

\[ \lambda = -\frac{1}{N_s} \frac{dN_s}{dt} \] (18)

and substituting for reliability \( R \) produces an equation for MTBF in terms of the reliability (19),

\[ \lambda = -\frac{1}{N_o R} \frac{d}{dt}(N_o R) = -\frac{1}{R} \frac{dR}{dt} \] (19)

A solution to this differential equation is equation (20) which shows that the reliability of a component decreases exponentially with time as in the right hand side of the bathtub curve.

\[ R = \exp(-\lambda t) \] (20)

In practice the number of components failing per second is very small a more convenient measure of the failure rate is the number of failures in \( 10^9 \) component hours, commonly referred to as the FIT rate.
3.8 Accelerated Test Methods

3.8.1 Introduction

Accelerated life testing is a means of environmental testing where many hours, even years, of device operation are simulated by exposing devices to stresses far in excess of what they would experience in normal operation. When used with care such process will accelerate the degradation processes at work in the device and produce early failures representative of many hours of operation in the field. The environmental parameters that may be altered to induce accelerated aging depend on the failure mechanisms operating in the device to be stressed. Typical parameters are temperature (both extreme temperature and temperature excursions), humidity, and voltage.

There are several accelerated life test methods that are relevant to assessing package reliability. Operation at elevated temperature is a standard test for aspects of both device and package operation, procedures for its use are laid down in MIL-STD 883 [114]. The effect of temperature on the rate of a chemical reaction was discovered by Arrhenius [115] (1889). It was shown by Peck in the early 1960's that the relationship between temperature and reaction rate holds true for the acceleration of failure mechanisms in semiconductor devices [116]. Therefore the reliability of such devices can be modelled by the Arrhenius equation. This has led to the use of elevated temperature testing of electronic components as an accelerated life test.

Where the package of a device is not considered to be hermetic, humidity testing is important to assess the ability of the package to protect the die from moisture ingress. Humidity testing plays an important part in the evaluation of the reliability of plastic encapsulations. Such are useful in assessing the effects of the adherence of plastics to lead frames, the plastics permeability, the ionic content of the plastic and generally show the ability of the package to protect the die from moisture. The effects of high humidity are further accelerated when the tests are conducted at elevated temperatures, this is the basis behind the widely used Temperature Humidity Bias Test (THB). In the days of T.H.B. many different combinations of temperature and humidity were used, however it soon became apparent that a set of standard test conditions were required. This requirement was met with the 85°C/85%RH test, first
proposed by Western Electric [117]. As component reliability improved the stress testing time at 85°C/85%RH increased and by the late 1970's had reached such a duration that a more highly accelerated test was required. The solution was to increase the test temperature. Increasing it beyond 100°C would require the use of pressure vessels and so autoclaves were employed and modified for this purpose. If the steam atmosphere inside the autoclave was not to be allowed to saturate the temperature of the chamber would have to be accurately controlled. Two types of autoclave test developed. The saturated atmosphere test (RH=100%) which became known as the "Pressure Pot" test, and the unsaturated atmosphere test, which became known as the "Highly Accelerated Stress Test" (HAST). From this three sets of test conditions have become established as standard tests:

1. 85°C/85%RH, the well established and accepted test for THB testing.
2. 121°C/100%RH, a saturated unbiased test sometimes called 'the pressure pot' test, used as a storage test.
3. 130°C/85%RH, a biased test now accepted as a faster alternative to (1), also known as Highly Accelerated Stress Test (HAST).

3.8.2 The 85°C/85%RH Test

The test known as 85°C/85%RH has long been established as an accepted test for accelerated life testing and lot to lot comparisons. It is universally believed to be consistent in inducing failures mechanisms typical of those observed in field failure returns. With the increasing reliability of modern encapsulants test times can now exceed thousands of hours.

3.8.3 Saturated Autoclave or "Pressure Pot" Test

This test is carried out in an autoclave where the water vapour atmosphere is allowed to saturate. The use of a saturated atmosphere precludes the use of bias as condensation is likely to occur on the boards and devices under test causing electrical short circuits. The test was developed to produce faster testing than is possible at 85°C/85%RH (Clinical autoclaves for sterilising medical apparatus were probably first used for this purpose). It is simpler and cheaper than non-saturated autoclave testing.
as it does not require the use of sophisticated controllers. The temperature of 121°C has been adopted as standard temperature for this test. It should be noted however that results from 100% RH tests showed a poor fit to data obtained from non-saturated testing. This suggests that the use of saturated testing should be avoided if optimized extrapolation to low stress levels is to be achieved. Saturation tests can however be used for comparisons between production runs to assess changes in manufacturing processes etc. where the increase in relative humidity and temperature can provide a reduction in test time over 85°C/85%RH testing.

3.8.4 Autoclave H.A.S.T. Tests

Tests by Sinnadurai in the early 1970's showed that there was a correlation between the time to fail of devices under standard 85°C/85%RH tests and the unsaturated autoclave test. It was reported [118] that this test accelerated the degradation of plastic encapsulated components and that there was a well ordered relationship between the vapour pressure of the moisture in the atmosphere and the time to failure. This has since been shown to be incorrect [119], and the time to failure is in fact related to the relative humidity of the unsaturated water vapour. This test has since been further investigated by many other researchers [120][121] for use as an accelerated test. Before unsaturated autoclave testing could be accepted as a faster alternative to 85°C/85%RH testing it had to be shown that the failure mechanisms promoted by the two tests are consistent, and that there was a clear acceleration factor for the unsaturated autoclave test. Peck [122] confirmed this by reviewing all the available published data (before 1986) on humidity testing over the entire stress range, both above and below 85°C/85%RH to test the correlation between autoclave testing and standard humidity cabinet tests. All the data (except one source) was for a single failure mechanism (electrolytic corrosion of aluminium metallization) in epoxy packages. He plotted the observed median life under stress testing against calculated median life from the results of 61 researchers. He was able to show a good correlation from this data. The relationship used was:

\[
\text{time-of-failure} = (RH)^\alpha \exp \left( \frac{E_o}{kT} \right)
\]  

(21)
where $T$ is temperature in Kelvin, $RH$ is the relative humidity in percent, $k$ is Boltzmann's constant, $n = -2.66$ and $E_a = 0.79eV$.

As data from more test has become available these figures have been revised to $n = -3.0$ and $E_a = 0.87eV$. Hence this single relationship may be used to relate stresses both above and below $85^\circ C/85\%RH$ making extrapolation of unsaturated autoclave results to low-stress conditions possible. From these results it is possible to deduce that $130^\circ C/85\%RH$ has a 20:1 acceleration effect over $85^\circ C/85\%RH$ for the

![Figure 1](image)

**Figure 1** Correlation between test conditions and acceleration factors. According to Peck [36].

stated activation energy of 0.79eV. Figure 1 shows Peck's graph of the correlation between observed and calculated Mean Times to Failure (MTF). He was also able to show the non-correlation of the saturated autoclave test ($121^\circ,100\%RH$) with $85^\circ C/85\%RH$ test data. This non-correlation was also reported by Mc.Garvey [123] who has observed it experimentally.

However there are certain limitations to unsaturated autoclave testing or HAST. The testing temperature must always be carried out at a temperature below the glass
transition temperature $T_g$ of the encapsulating plastic. Care must be taken in the choice of test temperature so as to provide a safe margin between test temperature and $T_g$. This is because $T_g$ is lowered slightly in the presence of high relative humidity. Vanderkooi and Riddell [124] have shown that the permeability of epoxies to water vapour, while it increases slowly as temperature approaches $T_g$, takes a 30% jump at $T_g$, and then proceeds faster than before as a function of temperature. This would lead one to expect a more rapid access of moisture to the aluminium on the chip at and above $T_g$, resulting in faster corrosion and shorter device life.

3.8.5 Autoclave Equipment

Autoclave testing has been used for assessing both device reliability and that of the constituent materials [125] used in microelectronic device packages. Autoclave accelerated life testing equipment exists in two basic forms the one chamber and the two chamber autoclave.

3.8.5.1 Two Chamber Equipment

The two chamber system built by Gunn & Malik [126] used a steam generator vessel plumbed directly to a larger test chamber vessel. Heater A in the steam generator produces a constant temperature steam supply which expands into the larger test chamber. In the test chamber, Heater B reheats the steam vapour to a higher temperature creating an unsaturated steam vapour in the test vessel. By increasing the test chamber temperature, the RH of the steam vapour from the steam generator is reduced since warmer air is capable of holding more moisture. Natural convection occurs within the test chamber as the warmer steam vapour rises to the top of the chamber where it displaces cooler vapour from the steam generator. External heaters C & D are used in conjunction with the main test chamber Heater B to provide uniform heating and humidity control throughout the vessel working area. The external heaters are activated to preheat test samples before steam is produced and eliminate condensation when the steam enters the test chamber. A diagram of the equipment is shown in Figure 3. Examples of the two chamber design are the Hirayama PC-422RII and Express Test Corp. HAST-1000 and HAST-6000 autoclaves from their Series III HAST systems range.
3.8.5.2 One Chamber Equipment

Single-Vessel HAST systems exist in two forms, those that use fans to circulate the water vapour and those which rely on convection. A diagram of a single chamber autoclave that uses convection, like the one employed in this study, is shown in Figure 3. In a single chamber system water in the bottom of the test chamber is heated by an immersed electrical element to produce steam. This rises to the top of the chamber where heaters in the walls heat it further thereby raising its temperature and reducing relative humidity. To prevent condensation occurring the lid is often heated and a baffle is inserted above the devices under test to prevent dew falling on them. This could be a problem especially when cooling during
ramp-down. The dry and wet bulb temperatures are sensed by two thermometers and from this the relative humidity and pressure in the vessel are calculated. Examples of single-vessel equipment include the Hirayama PC-364R, PC-242, & PC-305.

Both types should provide the facility for electrical feed-through to the chamber so that electrical bias may be applied to the devices under test. Safety features such as electrically activated pressure release safety valves backed up by mechanical pressure release valves should be incorporated. Other refinements should include low water sensors and over heating warning. To provide a record of the history of the stress environment a paper chart recorder is often included. This records the Dry-Bulb temperature, relative humidity and pressure.

3.8.5.3 Advantages of Two Chamber System

Dual Chamber designs have advantages over single chamber ones:

1. The dual-chamber design uses natural convection for vapour circulation and control. A separate isolated steam generator heater produces a constant-temperature, saturated steam vapour unaffected by the temperature of the test chamber. The higher-temperature (dry bulb) unsaturated steam vapour will not
mix with the lower-temperature (wet bulb) saturated steam vapour.

2. The use of a two-vessel system combined with multiple heaters eliminates the need for circulating fans which would create variable pressures within the test chamber. A simplified humidity formula applies, since no differences exist in the pressures between the steam generator and the test vessel.

3. By the use of an external inert gas supply (purified air or nitrogen) plumbed to the steam generator of a dual-vessel system it is possible to create a test environment below 100°C so that 85°C/85%RH and other lower temperature humidity tests are possible. As the gas percolates through the water in the steam generator, the gas is saturated and rises into the test chamber where it is reheated by the heating systems of the test chamber. A constant minimum pressure is maintained by the pressure of the incoming gas usually 5 to 10 pounds per square inch (69,000 to 104,000 N/m²), which is continually exhausted through a needle valve in the exhaust line of the test chamber.

Both types are capable of saturated vapour pressurized testing. In the two vessel equipment this is accomplished by equalising the temperatures between the steam generator and the test chamber. A history of this technique is outlined in Sinnadurai's paper [127].

3.8.6 Cleanliness Considerations

Murtuza et al [128] have shown that it is possible for ionic contamination, such as flux residues, from outside the package to be transported to the die along the moisture front that permeates the package during humidity testing. Danielson et al [129] have investigated this affect by comparing results from contaminated and "clean" test systems and have concluded that contamination in the test chamber can effect the observed distribution of failures, which has direct consequences for any calculated acceleration factors. So that repeatable results can be obtained it is necessary that the highest standards of cleanliness be maintained. For this reason strict rules were placed on the construction of boards and mounting hardware placed in the autoclave and also
the handling procedures for devices undergoing HAST. They specified that HAST test boards use bodiless sockets and use stitch weld interconnect technology. No soldering is permitted due to the flux contamination problem. Materials for the boards and racks consist of only stainless steel, nickel, PTFE and polyimide. A strict cleaning procedure was followed for the test boards where each one was carefully manually washed with deionised water and laboratory grade detergent followed by multiple rinses and forced air drying to remove any water droplets which would leave ionic residues on the boards after drying. Antistatic rubber gloves were required for all manual handling of boards and devices to eliminate contamination by sweat and skin secretions, a potential source of sodium chloride. Similarly constructed boards and hardware was suggested by Gunn & Malik [130] as a more robust alternative to conventional tracked boards which soon degraded under HAST conditions. Danielson's recommendations have been universally adopted and are now part of JEDEC standard JESD22-A110 [131].
3.9 Acceleration Formulae

The Arrhenius equation can be used to model the rates of chemical reactions. When such a reaction is a degradation process in an electronic device then it may be used to model the time to failure at different temperatures. If the degradation process involves exposure to a humid environment then it is possible to produce an equation to model changes in both temperature and humidity. Many such models have been suggested. All have been derived from the fitting of equations to experimental data. The median time to failure of a component is observed for a range of temperatures and humidity. This time to failure is then plotted against temperature (at constant humidity) or plotted against humidity (at constant temperature). The activation and humidity constant terms, for a given failure mechanism, may then be deduced. These formulae exploit the correlation between test times at elevated temperatures and humidity to extrapolate median time to failure back to ambient conditions. The accuracy of this technique however is affected by the sample size employed and the sampling interval which effects the accuracy with which the time to failure can be determined. The failure mechanism is identified by failure analysis of the failed devices. Problems arise when more than one failure mechanism is observed.

Many models have been suggested and most have been reviewed by Charles [132].

The models can be divided into three categories:

1. Vapour Pressure models
2. An Arrhenius temperature relationship and separate humidity relationship
3. As 2 but with a variable activation energy

Vapour pressure models showed good correlation for temperatures below 100°C, but were less satisfactory for more accelerated tests. Gunn et al [133] conducted tests at a constant vapour pressure but varied temperature and humidity and concluded that device life was not a simple function of vapour pressure or vapour pressure and temperature. Reich and Hakim also proposed an vapour pressure model [134] but this model is not now considered valid as acceleration factor is believed to be a
function of relative humidity.

The relationship between temperature and lifetime shows a clear Arrhenius relationship and all the models show this. The models for the humidity relationship are based on observing a number of different physical effects. Peck [135] presented a model where the humidity dependence term is based on the surface resistivity of moisture films. Eyring proposed a humidity relationship based on the rate of chemical reactions. Lawson [136] proposed that the humidity relationship depended on the amount of adsorbed water on the encapsulant surface. A relationship where the surface resistivity of moisture on the die was proposed by Sim [137]. Sbar and Kozakiewicz [138] measured the surface conductivity of unencapsulated and silicone rubber encapsulated dies, and found, as did Koelmans [139] and Weick [140] who used silicon dioxide test chips, that the activation energy in the Arrhenius relationship was humidity dependant. The many acceleration formulae that have been suggested to model the effects of temperature and humidity stress are given in Table III.
# Table III Acceleration Formulae

<table>
<thead>
<tr>
<th>Author</th>
<th>Acceleration Formulae</th>
<th>Activation Energies</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eyring (H)</td>
<td>$t = A \exp \left( \frac{\Phi}{kT} \exp BH \right)$</td>
<td>$\Phi = 0.6eV \quad B = -0.06$</td>
</tr>
<tr>
<td>Eyring (1/H)</td>
<td>$t = A \exp \left( \frac{\Phi}{kT} \exp B \frac{H}{H} \right)$</td>
<td>$\Phi = 0.65eV \quad B = 304 \quad l$</td>
</tr>
<tr>
<td>Peck &amp; Zierdt</td>
<td>$t = A \exp \left( \frac{\Phi}{kT} + B(\ln H) \right)$</td>
<td>$\Phi = 0.54 \ eV \quad B = -4.55$</td>
</tr>
<tr>
<td>Reich &amp; Hakim</td>
<td>$t = A \exp \left( B(T+H) \right)$</td>
<td>$B = -0.073$</td>
</tr>
<tr>
<td></td>
<td>$T$ in °Celsius</td>
<td></td>
</tr>
<tr>
<td>Peck</td>
<td>$t = (RH)^n \exp \left( \frac{E_a}{kT} \right)$</td>
<td>$E_a = 0.79 \ eV \quad n = -2.66$</td>
</tr>
<tr>
<td>Lawson</td>
<td>$t = A \exp \left( \frac{\Phi}{kT} \exp (-\eta RH^2) \right)$</td>
<td>$\Phi = 0.7eV \quad \eta = 4.4 \times 10$</td>
</tr>
<tr>
<td>Sbar &amp; Kozakiewicz</td>
<td>$t = A 10^{VT} 10^{BH} 10^{CH}$</td>
<td>$\Phi = 0.41eV \quad B = -18.69$</td>
</tr>
<tr>
<td>Stroehle</td>
<td>$t = A \exp \left( \frac{B\Phi H}{T} \right) \exp(CH)$</td>
<td>$\Phi = 0.65eV \text{ at } 0% \text{ RH}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\Phi = 0.4eV \text{ at } 100% \text{RH}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$B = 0.0065$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C = -0.2513$</td>
</tr>
<tr>
<td>Hallek</td>
<td>$t = A \frac{B}{10^{TP - k}}$</td>
<td>$B = 595 \quad K = 131 \text{ mmHg}$</td>
</tr>
</tbody>
</table>

3-42
Variations on these tests, include the work of Iwamori & Matsumura [141] who experimented with mixed 121°C/100%RH and 85°C/85%RH tests where devices were alternated between the two test conditions. Ajiki et al. [142] described a cyclic biased THB test for power dissipating ICs where the bias is cycled ON/OFF. This is intended for devices where dissipation under bias would lower the temperature at the chip. Yet another modification to standard THB testing is the pretreatment of plastic encapsulated devices with salt water. This is intended to reduce test times by speeding up the corrosion rate. Yoshida & Takahashi [143] claim an acceleration factor of six over standard THB by this method. They state in their conclusion that the ranking of moisture resistance among four sample lots using this method is the same as in the 'basic test' (standard THB). It is difficult to see the value of this test other than for lot-to-lot comparisons as it is not possible to relate to life in the field, although it may prove of some use in understanding corrosion in applications for the marine environment. Another ON/OFF bias test was reported by Terasaka et al. [144] in this study plastic encapsulated devices were stored (unbiased) in the autoclave at 121°C (presumably in a saturated steam environment) for 48 hours before autoclave testing with cycled bias. This would appear to be an odd test for anyone to conduct, as has been previously stated saturated autoclave testing has no correlation with field conditions. Its inclusion with an unsaturated test would only serve to prevent data from this part of the test being related back to field conditions. It may however be of use as a means of comparing lot to lot variations in package quality.

3.10 The Development of Improved Plastic Package

Reliability

Normally high reliability semiconductor devices are encapsulated in hermetic packages. These are fabricated either as metal cans with welded seams and lead through wires passing through glass seals, or as ceramic packages with the semiconductor die entombed in a cavity been two ceramic covers with the electrical connections made through glass/ceramic seals. Both packages in essence use a
packaging material which was impervious to moisture and had extremely low rates of
gaseous diffusion. The packaging technique is still in widespread use today in high
reliability electronic systems such as those in aerospace and military applications.

Back in the late nineteen sixties, and accompanying the introduction of
integrated circuits (ICs), a new package type began to appear. This was the transfer
moulded plastic package. Initially intended as a cheap alternative to hermetic
packaging it soon found widespread acceptance in consumer electronics where the
operating environment was largely benign and reliability of little concern to the
manufacturer. Indeed, of more importance to the manufacturer were the cost
advantages these devices offered, often as little as half the cost of their hermetic
counterparts. Unfortunately the performance of the packages in humid environments
was poor.

The reliability of these devices in humid conditions was assessed under
Temperature, Humidity and Bias conditions known as THB tests. In particular one set
of conditions 85°C/85%RH was soon adopted as an industry standard.

3.10.1 Reported Reliability under 85°C/85%RH Bias Tests

It is useful to compile data from previously published sources on the results
of accelerated life testing to see how reliability has improved over the last two
decades. This improvement can be attributed to changes in package design, materials
and production practices, and has changed the proportions in which the failure
mechanisms observed.

Several researchers have paid particular attention to the reliability of
CMOS devices encapsulated in plastic. In 1971 a report by Edorf of RADC [145]
stated the use of plastic packages accounted for 50% of the monolithic IC packages
in use at the time. This report comprehensively catalogues the time to fail of different
devices in various packaging materials subjected to a range of stress tests. It was
reported that devices encapsulated using a particular epoxy compound produces 96.5%
failures under 85°C/85%RH under forward bias in 4368 hours and an MTBF of 385
hours. The predominant failure mechanism was corrosion of the chip metallization.
Gallace and Rosenfield [146] reported on the improvement in moisture resistance of plastic packaged CMOS devices as observed under 85°C/85%RH biased testing. In 1974 about 30% of devices subjected to this test were defective after 1000 hours. By 1984 this had decreased to less than 0.1% of devices. The main reasons for this improvement was said to be the optimisation of the phosphorus content of the Chemical Vapour Deposition Polysilicate Glass (CVD PSG) protective passivation layer. An even greater improvement was reported in 1984 with the claimed elimination of chloride ions from the plastic packaging resins.

Nachbauer [147] reported failure rates of 7% for 4000B series CMOS devices and of about 1% for their 4000 series HCMOS devices. These were packaged using P410B plastic, which had been superseded by 1988 by Nitto HC10-2, and Sumitomo 1100HS plastics, both believed to be more hermetic grades. It was reported that both corrosion and parametric failures were observed in these devices. Peterson [148] reported on the reliability of several manufactures of CMOS ICs under 85°C/85%RH testing during the mid 1970's and reported failures levels between 6 to 76% for 1000 hours test duration. Taylor [149] reported a fifty percent failure rate in biased CMOS devices after approximately 250 hours. In this series of tests the devices were biased and the reported failures were all parameter changes.

Bipolar logic (TTL, Schottky and Fast logic) have been studied by a number of researchers alongside CMOS devices. Brambilla et al [150] conducted 85°C/85%RH Bias tests on CMOS circuits from four manufacturers. The percentage failure rates after 1000 hours were 0, 1, 8, and 9%. Fast TTL were also tested, under the same conditions, with no failures reported before 1000 hours.

Gustafsson [151] reported in 1984 on the reliability of ICs encapsulated in a range of different plastics. They were stressed at 85°C/85%RH and after 1000 hours showed failure rates ranging from 0-100%. The very wide spread in the range of failure rates was attributed to the different level of chloride ions present. This was detected in those plastics where a high proportion of failures occurred. Comparison between two vendors of TTL logic circuits showed failures of 0% and 12% after 1000
There is less published data on the reliability of comparatively more complex devices. McGarvey [152] reported in 1979 of plastic encapsulated MOS-LSI devices producing 29% failures after 1000 hours of 85°C/85%RH. George [153]
Figure 4 Improvements in Plastic Package Reliability under 85°C/85%RH Testing of BAe. reported on the results of their Reliability Monitoring Programme on two complex Intel ICs which they procured (1988). During the period 1981-1983 they reported a decrease in failure rates from 13% to approximately 1%, when these devices were subjected to 1000 hours of 85°C/85%RH testing. The same report mentions briefly the results of 85°C/85%RH testing on plastic EPROMs where sample sizes of about 500 devices showed zero percent failures after 1000 hours whether biased or unbiased. The results from these 85°C/85%RH tests are summarised in Table III, and shown graphically in Figure 4. The lines about points 2 and 3 show the wide range of observed reliability between manufactures prevalent in the 1970's.

The reliability of more specialist coatings has also been investigated using THB methods. Alexander et al. [154] reported the development of a low cost protective coating for EPROMs that was both transparent to ultra-violet light and could achieve failure rates of less than 0.5% under 1000 hours of 85°C/85%RH testing. Fujita et al [155] described a very thin, chip-sized, ultra pure filler-free epoxy encapsulation for tape automated bonding which it was claimed could withstand 3000 hours of THB testing at 85°C/85%RH.
3.10.2 Reported Reliability of ICs under HAST with Bias

By the late 1980s the reported number of failures under 85°C/85%RH had fallen to below 1% in 1000 hours. Plastic encapsulated devices were now displaying such long times to failure under this test that a new, more severe, test was needed if the demands for evermore reliable ICs could be met and low failure rates documented. It was this requirement that led to the development HAST. This test is between 20-30 times faster than 85°C/85%RH testing (depending on test conditions) and therefore offers considerable savings in test time. The background to HAST has been covered earlier (3.8.4.).

Despite the existence of several papers on the results of HAST testing a comparison between them is difficult because it is only recently, with the introduction of JEDEC Standard JESD-A110 [131] that 130°C/85%RH has been adopted as a "standard" test condition. Previously autoclave tests had been conducted over a wide temperature and humidity range (105-140°C and 75-100%RH) with no standard measurement interval times.

Olsson [156] (1989) whilst investigating the reliability of plastic encapsulated devices for the telecommunications industry reported the results of HAST with bias at 135°C/85%RH on a range of products from seven different manufacturers. These were digital ICs device from a range of device families encapsulated in both DIP and SOIC packages. After 750 hours of exposure to this stress test the ICs from some manufactures displayed no failures whilst others had as many as 100% defective devices. This highlighted the very wide range in the reliability of devices available. To illustrate the wide variation in reliability Olsson's data is summarised in Table III, Table IV.
Table IV Summary of Olsson's Findings on the Reliability of Logic Devices.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Package Style</th>
<th>Device Family</th>
<th>Cumulative Failures %</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>PDIP</td>
<td>LS</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HC 100% @ 500 HOURS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SOIC</td>
<td>HC</td>
<td>100% @ 500 HOURS</td>
</tr>
<tr>
<td>B</td>
<td>SOIC</td>
<td>LS</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F 14</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PDIP</td>
<td>LS</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F 2.7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SOIC</td>
<td>LS</td>
<td>4.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HC 2.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>S 5.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>S 2.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SOIC</td>
<td>HC</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>SOIC</td>
<td>LS</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>PDIP</td>
<td>LS</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HC 6.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HC 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PDIP</td>
<td>LS</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HC 5.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>S 11</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HC 2.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>F 2.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SOIC</td>
<td>HC</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>SOIC</td>
<td>LS</td>
<td>0</td>
</tr>
<tr>
<td>F</td>
<td>PDIP</td>
<td>HC</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>SOIC</td>
<td>HC 8.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LS 2.7</td>
<td></td>
</tr>
</tbody>
</table>

3-49
Nachbauer [146, 147] also reported on the results of HAST testing on two different types of CMOS device manufactured during 1986. Wada et al.[157] (1988) have reported on the percentage of cumulative failures of CMOS and Bipolar ICs subjected to a HAST over a range of test temperatures (120-140°C). Wada reported 25% of devices failing after 100 hours for CMOS devices and 35% of failures were reported in Bipolar devices after 150 hours, (the test temperature was 130°C). The results from these HAST programmes is summarised in Table V and shows that, even when subjected to the very severe test conditions of HAST, plastic package reliability has shown continuing improvements over the past decade. This is illustrated graphically in Figure 5.

Table V Reliability of Plastic Encapsulated Devices under HAST

<table>
<thead>
<tr>
<th>Author</th>
<th>Date</th>
<th>Test Condition (°C/%RH)</th>
<th>Percentage of Cumulative Failures and test duration (hours)</th>
<th>Device Family</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gustaffson</td>
<td>1984</td>
<td>130/85</td>
<td>1-40%, 110</td>
<td>LS-TTL</td>
</tr>
<tr>
<td>Nauchbauer</td>
<td>1986</td>
<td>132/85</td>
<td>34%, 150</td>
<td>CMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>151/85</td>
<td>98%, 114</td>
<td></td>
</tr>
<tr>
<td>Wada</td>
<td>1988</td>
<td>130/85</td>
<td>25%, 100</td>
<td>CMOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>35%, 130</td>
<td>BIPOLAR</td>
</tr>
<tr>
<td>Olsson</td>
<td>1989</td>
<td>135/85</td>
<td>0-3%, 96</td>
<td>LS,HC,S,F,</td>
</tr>
</tbody>
</table>

3.10.3 Reported Improvements in Temperature Cycling Performance of Plastic Encapsulated ICs.

Temperature cycling is another accelerated life test designed to test the reliability of packaging. It is used to simulate many temperature excursions in rapid succession and is often used to cycle a device over its entire operating or storage
Reported Reliability of Plastic ICs

<table>
<thead>
<tr>
<th>Test Method</th>
<th>Cumulative Failures (%)</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. 130°C/85% 110 Hours LS-TTL, Gustaffson</td>
<td>100</td>
<td>83</td>
</tr>
<tr>
<td>2. 132°C/85% 150 Hours CMOS, Neuchbener</td>
<td>80</td>
<td>84</td>
</tr>
<tr>
<td>3. 130°C/85% 100 Hours CMOS, Wada</td>
<td>60</td>
<td>85</td>
</tr>
<tr>
<td>4. 135°C/85% 96 Hours LS-TTL, Olson</td>
<td>20</td>
<td>86</td>
</tr>
</tbody>
</table>

Figure 5 The Improvement in Plastic Encapsulated Device Reliability under HAST temperature range. Many thousands of cycles may be used, a number which may only be reached after many years in normal operation. Four types of thermal testing have been proposed to assess the reliability of electronic components as shown in Table V. The first two test methods are widely used to assess device reliability.

A survey of the available literature shows that the reliability of plastic encapsulated semiconductor devices subjected to temperature cycling tests has improved markedly over the past twenty years.

Edorf in 1971 reported 90% failures amongst test batches of epoxy encapsulated devices subjected to 240 cycles over the range -65 to 150°C. Gallace & Rosenfeld conducted air-to-air temperature cycling tests on plastic dual in-line packages (P-DIPs) over the temperature range -65 to 150°C. They reported only two failures in 17,000 samples in a series of tests with cycle durations ranging up to 3000 cycles. They also conducted thermal liquid to liquid shock tests over a temperature range of -65 to 150°C. Only one failure in over 18,000 samples, in tests ranging up to 9,000 cycles, was reported. Kramer & Adolphsen [158] conducted air to air temperature cycling tests on both plastic and ceramic packaged devices from a range
Table VI Thermal Stress Tests

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Nature of Test</th>
<th>Standard Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Cycling</td>
<td>Air to Air cycling</td>
<td>MIL-STD 883 Method 1011</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JEDEC-STD A104, A105-A</td>
</tr>
<tr>
<td>Thermal Shock</td>
<td>Emersion in two liquids at temperature extremes</td>
<td>MIL-STD 883 Method 1010</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JEDEC-STD A106</td>
</tr>
<tr>
<td>Stabilisation Bake</td>
<td>Exposure to constant elevated temperature</td>
<td>JEDEC-STD A103</td>
</tr>
<tr>
<td>Monitored Temperature</td>
<td>Continuity of electrical performance is monitored</td>
<td></td>
</tr>
<tr>
<td>Cycling</td>
<td>as device is temperature cycled</td>
<td></td>
</tr>
</tbody>
</table>

of manufacturers. They observed significant manufacturer to manufacturer variation and a tendency for the ceramic encapsulated devices to perform more reliably under temperature cycling. Olsson reported failures of between 0.03-1.00% and 0.08-1.35% for PEDs from a range of manufactures subjected to temperature cycling. The results from these reported temperature cycling tests are presented below in Table VII. This shows a marked improvement in the reliability of plastic encapsulated ICs under temperature cycling stress during the past twenty years as can be from Figure 6. This improvement in temperature cycling and thermal shock performance is attributed to the development of low stress moulding compounds with c.t.e. more closely matched to those of silicon and lead frame materials.

3.10.4 Combined Temperature Cycling and HAST programmes.

To investigate whether temperature excursions affected plastic packages ability to resist moisture ingress Gustafsson [160] conducted temperature cycling as an additional pre-conditioning stress before HAST and reported that this seems to have no effect on device reliability. Folkens & Lous [159] used temperature cycling and solder bath dipping as preconditioning before subjecting CMOS devices to HAST to investigate whether temperatures experienced in assembly effected moisture resistance. Temperature cycling consisted of 100 cycles between 55°C and 125°C before HAST
Table VII Reliability of Plastic Encapsulated Devices subjected to Temperature Cycling.

<table>
<thead>
<tr>
<th>Author</th>
<th>Date</th>
<th>Package</th>
<th>Temperature Range (Celsius)</th>
<th>Number of Cycles</th>
<th>Cumulative Failures (Percent)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Edorf</td>
<td>1971</td>
<td>Plastic</td>
<td>-65 - 150</td>
<td>240</td>
<td>90</td>
</tr>
<tr>
<td>Kramer &amp; Adolphsen</td>
<td>1980</td>
<td>Ceramic</td>
<td>-65 - 150</td>
<td>2500</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Plastic</td>
<td>-65 - 150</td>
<td>2500</td>
<td>0 - 100</td>
</tr>
<tr>
<td>Gallace &amp; Rosenfeld</td>
<td>1984</td>
<td>Plastic</td>
<td>-65 - 150</td>
<td>3000</td>
<td>2 in 17,000</td>
</tr>
<tr>
<td>Olsson</td>
<td>1989</td>
<td>Plastic</td>
<td>-40 - 150</td>
<td>2000</td>
<td>0.03 - 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-65 - 150</td>
<td>1000</td>
<td>0.08 - 1.35</td>
</tr>
</tbody>
</table>

Reported Reliability of Plastic ICs Subjected to Temperature Cycling (-65 to 150°C)

Figure 6 Improvements in the Reliability of PDIPs subjected to Temperature Cycling testing at 130°C/85%RH with bias. They concluded that appreciable acceleration of the electrical degradation by pretreatment with solder dipping and/or temperature cycling was not observed.
3.10.5 Reported Failure Mechanisms in the above Programmes.

The failures reported in the above test programmes were attributed to two failure modes, catastrophic failure and parametric drift. Catastrophic failures were reported by Edorf [145], Nachbauer [146, 147], Gustaffson [150], and Kramer [158]. Gustaffson reported the formation of gold-aluminium intermetallics at the bond pad interface which caused them to fracture. Nachbauer reported the presence of bond pad corrosion as being responsible for some of the catastrophic failures. Edorf, Kramer and Olsson [151, 156] all reported some device failures due to parametric drift.

Of the failures which occurred during temperature cycling only Kramer identified a failure mechanism. He identified the failures as being due to the fracturing of the bonding wires 75µm above the bond pad, and illustrated this with an electron micrograph. Wada [157] reported failure modes/mechanisms of parameter shift, electrolytic leakage current and aluminium corrosion. Comparisons between the percentage cumulative failure figures under both THB and HAST tests can only ever be approximate because of the differences in bias conditions, some researchers choosing to bias the devices under test at their maximum operating voltages, others choose any voltage across the operating range. As the rate of electrolytic corrosion is dependant on applied voltage as well as temperature and humidity some care should be exercised in comparing this data.
3.10.6 Explanation of the Improved Performance of Plastic Packaged ICs subjected to Accelerated Life Testing.

As has been shown the reliability of plastic encapsulated ICs has improved dramatically over the past twenty years. This improvement is due to improved materials, greater production cleanliness and quality control. It is even more remarkable, as at the same time as reliability was improving, device complexity and pin counts were increasing whilst the track widths and the size of surface features on the dies were decreasing, trends which could have caused ICs to become less reliable. All areas of package design have been studied by the manufacturers to produce these improvements.

Gustaffsson & Lindborg [160] have established a direct correlation between device life and the chlorine content of its encapsulating resin under accelerated life testing of plastic encapsulated microcircuits. As a result the plastic moulding compounds used in electronic packaging have greatly improved in purity. The levels of ionic impurities have been greatly reduced in particular those of chlorine and sodium. Chloride ions are responsible for the corrosion of device metallisation as they react with the aluminium of the die metallisation. Sodium has been shown to play an important role in secondary ion slow trapping in CMOS devices. Plastic moulding compounds also contain bromine as a fire retardant, and although of less importance in initiating corrosion, its concentration in the plastic has been optimised. Matching of the plastics c.t.e. to that of the lead frame has reduced the thermally induced stresses in plastic packages. This has produced better temperature cycling performance by reducing the stresses on the bonding wires and bond pads, and has also improved the humidity testing performance of these packages by reducing the thermally induced stresses on the die passivation layer. Thus reducing the risk of cracking.

The die surface of an IC is coated with a glass passivation layer. This is deposited by chemical vapour deposition (CVD) and is of polysilicate glass (PSG). To relieve stresses in this material, and so reduce cracking, it is doped with phosphorus. In moist environments the phosphorous becomes hydrolysed to phosphoric acid which reacts with the aluminium metallisation. The optimum level for this doping was established in 1974 to be 2%. Controlling phosphorus doping to this level has significantly improved device reliability in accelerated life tests. Silicon nitride
passivation techniques are now being used as an alternative to phosphorous doped glass.

The adhesion of the plastic moulding compound to the lead frame is important if this interface is not to provide a ready path for moisture from the operating environment to the die. Gallace & Rosenfeld [146] reported on a design for a lead frame where adhesion was improved by the addition of holes in the lead frame's legs inside the package. This was claimed to provide a key for the plastic and thus reduce plastic/lead frame separation. The elimination of cleaning solvents and fluxes containing chlorine from the manufacturing process has also helped reduce corrosion-related failure mechanisms.

3.11 Thick Film Resistors

Another type of component that has been assessed using THB and HAST techniques are thick film resistors. Sinnadurai & Wilson [161] [162] conducted accelerated life tests on SIL and DIL packaged thick film resistors under conditions of elevated temperature and humidity stress. Kasukabe and Tanaka [163] have shown a relationship between the stability of thick film resistors and their initial Third Harmonic Index (THI) under high temperature and THB stress. Sinnadurai et al. [164] also reported on the behaviour of thick film resistors subjected to accelerated life stresses induced when subjected to high temperature biased tests and THB testing stresses when encapsulated in different encapsulations and overglazes. Pranchov [165] & DeGroot [166] have both attempted to model the long-term drift of these devices. Troop et al [167] have applied HAST techniques to the assessment the reliability of a number of resistor types. With the exception of a certain type of wirewound device, that utilised crimped terminations, all the types tested were found to be very stable under conditions of 135°C/85%RH for up to 1,000 hours.

3.12 Summary

This chapter reviewed the available results from several large scale investigations into the reliability of plastic encapsulated ICs, as well as some smaller investigations. It shows that there has been a considerable improvement in the
reliability of plastic encapsulated semiconductors over the past twenty five years as observed under accelerated life testing.

There appears to be certain areas where little or no investigation has been conducted;

1. Temperature cycling has been conducted as a pre-stress for HAST, but not after moisture has breached the package. This would more closely reproduce the conditions seen in harsh operating environments. It would reproduce the freeze/boil action of moisture held within the package.

2. Parametric drift has been reported in a number of studies, however the basic process of parameter degradation in Bipolar and CMOS devices encapsulated in moulded plastic packages has not been studied. Identification of the electrical parameters that are susceptible to moisture may provide a reliability indicator able to detect components at risk.

3. No investigations have been conducted into the effects of the physical sizes of the device and package, such as the surface area of the encapsulated die and the thickness of the encapsulated plastic have on the performance of the devices life under accelerated life testing.

4. Full electrical characterisation of the degradation of a device is expensive and time consuming, especially of complex devices, and may be unnecessary if it is desired to know only if moisture has breached the package. To assess the ability of a package to prevent the ingress of moisture it may be possible simply to measure a leakage current between two or more electrical connections, say the supply pins.

5. Both moisture ingress and thermally induced package stresses present in plastic encapsulated ICs may be observed and quantified for a range of package styles by employing package performance test chips.
3.13 References


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CHAPTER 4

ACCELERATED LIFE TESTING OF PLASTIC PACKAGES

4.1 Introduction

It has been established from the literature survey that much attention has been paid to the reliability of integrated circuits under accelerated life testing employing temperature, humidity and bias to simulate many years of field conditions. Further inspection reveals that this data is almost exclusively from tests on digital circuits where the failure criteria was either catastrophic failure or an inability to obtain the correct output voltages across the 0/1 voltage decision threshold. Such circuits depend for their operation on the devices switching correctly at predefined voltage levels. Digital I.C.s account for the largest proportion of IC production but linear circuits also form a large and important category of semiconductor devices. These devices have to maintain a linear relationship in both voltage and phase between their input and output ports, therefore they may be expected to display greater susceptibility to parametric drift. In comparison to the many references available on work conducted on digital devices the number that are available into investigations of parameter drift as a failure mode in analogue devices is small. Therefore it was decided to explore this avenue of research. It was considered desirable for such an investigation to study the basic "building blocks" of such circuits, the Bipolar Junction Transistor (BJT) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET). To have attempted to study both device types would have been too ambitious and so the bipolar transistor was selected as it is less susceptible to ESD and is therefore more easy to characterise.

To investigate the effects of moisture ingress into plastic encapsulated devices the degradation of several parameters were monitored to discover which are the most
susceptible to the combined effects of moisture and humidity. Experiments into the effects of exposure to temperature, humidity with bias (THB) on both plastic and ceramic packaged devices were undertaken and a comparison of their relative susceptibilities to parameter degradation was performed. The tests were continued until a sufficient number of devices had failed to permit failure analysis.

Data was available on the rate of moisture absorption by Cresol Epoxy Novolac resin, which is a component of the moulding compounds used to encapsulate ICs, however no information could be found on absorption into the cured loaded moulding compound. It was therefore necessary to establish the rate of moisture absorption into the moulded plastic of actual packages. An investigation into this process was conducted over a range of temperatures and relative humidity. An investigation into the amount of moisture absorption as a function of temperature, relative humidity and time was performed. From this information it was possible to derive a model showing the temperature and humidity dependence of moisture absorption.

In addition to the combined effects of exposure to high temperatures and humidity, an experiment into the effects of absorption followed by cycling between extremes of temperature was performed. Temperature cycling of packages that contain absorbed moisture may cause them to experience mechanical stresses as the moisture condenses and freezes inside the package. Such an experiment would simulate prolonged exposure to operating conditions under the most severe conditions, such as exposure to tropical environments followed by rapid temperature excursions. Conditions such as these may be experienced by avionic equipment that could be expected to undergo rapid temperature changes as the components moves from ground level to the sub-zero temperatures experienced in flight at tens of thousands of feet.
From these considerations an experimental work programme was formulated which addressed the following areas of interest:

a) The determination of the rate of moisture ingress into moulded plastic packages, as opposed to samples of polymer, and the dependence of this process on temperature and humidity.

b) The determination of the nature, rate and dependence of the drift in the d.c. parameters of plastic encapsulated bipolar transistors under extremes of temperature and humidity such as those used in accelerated life testing.

c) To subject bipolar junction transistors, in both plastic and ceramic packages, to accelerated life testing and assess both package and device degradation whilst identifying the failure mechanisms.

d) Assessment of the combined effects of moisture ingress and subsequent temperature excursions on plastic packages.

e) Investigation of the effect on device reliability of employing a tungsten-titanium alloy (Ti/W) overcoat over the bond pad area, a technique that has recently been introduced by some manufacturers for high temperature operation.

f) To examine the effectiveness of very thin, high pin count surface mount packages in preventing moisture ingress and determine the suitability of package performance test chips for this purpose. Measure moisture ingress into such packages as a function of temperature and humidity using test chips.

g) To employ on-chip stress transducers to investigate the package induced stresses experienced by a semiconductor die encapsulated in a moulded plastic package.
The areas a) to e) are covered in this chapter and f) and g) are covered in chapter 5.

4.2 Equipment

Much of the equipment used in this investigation is common to all the sections of the project as outlined in section 4.1. A brief description of each of the major components is given below.

4.2.1 HAST Test Equipment

To accelerate the absorption of atmospheric moisture into plastic packages the packages were exposed to a range of high relative humidity and high temperatures using an autoclave operating under unsaturated conditions. The apparatus used was a PC-364RII single chamber autoclave manufactured by Hirayama. A photograph of the equipment is shown in Figure 1.

To ensure compatibility of results and ease of comparison with other studies all HAST experimental work was conducted in accordance with JEDEC standard 22-A110. This specifies a set of procedures and materials for use in HAST environments. It is particularly important that attention has to be paid to the cleanliness of all items placed in the test chamber. Polyimide boards wired with stitch welded nickel wire, to avoid solder and flux contamination, and covered with polytetrafluoroethylene (p.t.f.e.) insulation were used throughout the HAST tests. The boards are effectively inert under HAST conditions and do not degrade, even at high temperatures, since such degradation could release chemicals that may be reactive at the extreme conditions experienced in the autoclave. This could cause unrepresentative failure mechanisms to occur. The boards used were supplied by the Express Test Corporation of California, an example is shown in Figure 2. All mounting hardware such as board mounting racks were constructed from stainless steel and p.t.f.e.

The water used in the autoclave to create the high levels of humidity had to be of a very high purity. It had to be free of ionic species that were potentially reactive under the extreme conditions used for HAST. Therefore the deionised water supply for the test chamber was obtained from a Permutit 250 water de-ioniser which was further purified by a Permutit CD-PLUS water polisher which provided deionised
Figure 1 Hirayama PC 864RII Single Chamber Non-Saturating Autoclave

water with a resistivity far in excess of the recommended purity levels of $1 \text{M}\Omega$. When fitted with new filter packs resistivity levels of $18 \text{M}\Omega$ were possible with this equipment. Before accelerated HAST testing was begun a series of tests were conducted on the residual contamination present in the autoclave test chamber. This was done by sampling the residual water present in the bottom of the test chamber after testing.

The purity of the deionized water supply was checked prior to the beginning of the experimental study. The concentration of chloride ions ($\text{Cl}^-$), known to be potentially troublesome, was measured by ion chromatography and the concentrations of three cations ($\text{Na}^+,$ $\text{K}^+,$ $\text{Li}^+$) by atomic absorption. In addition a number of tests were
conducted to verify that the procedures used to clean the chamber were adequate to remove any build-up of residual contamination, thereby maintaining ionic contamination below acceptable levels. At all test intervals the levels recorded were found to be satisfactory. The levels of these contaminants are shown in Table I and all are far less than the maximum permissible levels recommended [1][2].

Table I Levels of Contamination Measured in the Autoclave

<table>
<thead>
<tr>
<th>Ionic Species</th>
<th>Specified Level (p.p.m.)</th>
<th>Measured Level (p.p.m.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cl⁻</td>
<td>10</td>
<td>0.9</td>
</tr>
<tr>
<td>Na⁺</td>
<td>10</td>
<td>1.1</td>
</tr>
<tr>
<td>K⁺</td>
<td>20</td>
<td>0.4</td>
</tr>
<tr>
<td>Li⁺</td>
<td>20</td>
<td>0.0</td>
</tr>
</tbody>
</table>
Every item that was placed in the autoclave was cleaned in deionized water containing a small quantity of liquid surfactant, followed by wiping with isopropyl alcohol to remove any organic residues, and multiple rinses with deionised water. The remaining water droplets clinging to the boards were removed by blowing with a filtered compressed air line, since such droplets may contain dissolved ionic compounds. At all times every item placed into the chamber was handled with conducting disposable latex gloves or finger cots to avoid direct contact with the skin, which is a source of sodium chloride and other contaminants. When it was necessary to move the devices under test between equipment in the laboratory they were left on the HAST test cards which were covered in new antistatic seal-easy bags to avoid ESD damage and contamination.

Electric bias was supplied to the devices under test with regulated power supplies which provided pre-set bias voltage levels with pre-set current limiting. The use of current limited supplies prevented the failed devices from producing excess dissipation should they fail by going short circuit whilst in the autoclave test chamber. It may not have been possible for the autoclave control system to correct for the excess dissipation which could have caused the equipment to deviate from the set test conditions.

4.2.2 Temperature Cycling Equipment

A temperature cycling cabinet (modified for computer control) was used in the temperature cycling tests. This was capable of providing chamber temperatures in the range -55 to 140°C and it was used to cycle the packages under test across the full military temperature range with dwell times at the extremes to allow thermal equilibrium to be attained.

4.2.3 High Temperature Equipment

To provide comparison of the results in the HAST test studies with an environment of the same temperature but without a high level of atmospheric moisture a thermostatically controlled oven was used. This was used in tests designed to help ascertain if any degradation observed in the HAST tests were due to humidity or solely high temperature. The duration of the tests were controlled by connecting the
oven and device bias supplies through a programmable time switch to the mains supply.

<table>
<thead>
<tr>
<th>Range</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td></td>
</tr>
<tr>
<td>0 - 18°C</td>
<td>0.2%</td>
</tr>
<tr>
<td>18 - 20°C</td>
<td>0.25%</td>
</tr>
<tr>
<td>20 - 50°C</td>
<td>0.4%</td>
</tr>
<tr>
<td>&lt; 200MΩ</td>
<td>1.5%</td>
</tr>
<tr>
<td>200MΩ - 20GΩ</td>
<td>1.5%</td>
</tr>
<tr>
<td>20GΩ - 200GΩ</td>
<td>1.5%</td>
</tr>
</tbody>
</table>

Table II  Electrometer accuracy

4.2.4 Electrical Characterisation

The characteristics of the devices in the test study were measured at regular intervals using a HP4145B Semiconductor Parameter Analyzer manufactured by Hewlett Packard. This equipment is capable of being controlled over the General Purpose Instrument Bus (G.P.I.B.) allowing the instrument to be brought under the control of a personal computer (PC) equipped with a suitable controller card and software. With such an arrangement data may be transferred to the PC for storage and subsequent data analysis.

4.2.5 Consideration of Possible Errors and Uncertainties

The uncertainties associated with the HAST experiments can be considered as uncertainties in attaining the test conditions and uncertainties in measurement.

The autoclave test conditions are specified for a distance of 30mm from the chamber walls, lid and base. Inside this testing area the temperature is specified as being to within one degree of the desired value. The calibration of the autoclave was checked every six months as part of a regular service schedule. Test duration could be specified to a resolution of one minute but in practice its accuracy is probably better than this as it set by an electronic timer. Electrical bias to the devices under test was switched on and off by a separate time switch so that the stress test time with bias
was the same as the time at HAST conditions. Overall the uncertainty in test conditions was considered to be acceptable.

The uncertainties in the measurement of electrical parameters is very small. The parameter analyzer has a current source accuracy of 0.5% and a current measurement accuracy of 0.5% and is regularly auto-calibrated against an internal standard. Errors associated with measurements taken with this equipment are therefore 1%. The Solartron D.M.M. has an accuracy of 0.1%. The errors associated with the electrical measurements was therefore around 1.1%.

In chapter 5 an electrometer was used to measure the leakage resistance between adjacent tracks of silicon test structure. The measurement uncertainties associated with this instrument are given in Table II. This suggests that errors in the averaged measurement of leakage resistance could be expected to be initially 1.5% on the highest range decreasing to 0.4% as the leakage resistance of the lines fall below 200MΩ. In general the observed leakage resistance fell from several hundred giga-Ohms to several hundred Ohms over 500 hours of HAST.

The major limitation with this type of test is that the electrical measurements, and so the detection of a failure, can only be accomplished at set test intervals in this case 25 or 100 hours. The resolution in the detection of when a failure occurred is the major source of uncertainty with this type of test.

4.3 Moisture Absorption Studies

In chapter three all the reported failure mechanisms associated with plastic packaged devices, that could be found, were described. The majority of these are due to the effects of moisture ingress resulting in corrosion of either the bond pad area or of the device metallisation, there may be an observable affect on device parameters when moisture is absorbed into a device package. If a conducting moisture film was to form over, or in the region of, the die or between bond pads then a change in electrical characteristics may occur. It was therefore necessary to investigate the rate at which moisture is absorbed and its dependence on temperature and humidity.

The investigation of the dependence of the rate of moisture absorption on temperature and humidity used samples of 10 P-DIP packages subjected to a range of conditions. Weight gain was measured using a Sartorius Research R200D precision
balance. This was capable of measuring the weight of devices to an accuracy of $10^{-5}$ g. The samples were removed from the test environment at intervals and allowed to cool so that the package had reached room temperature (approximately 25°C), they were then left for a further hour to ensure the internal and external temperatures were in equilibrium before weighing.

It would have been desirable to have continued these tests until the packages displayed no further increase in weight, however only the packages from the test conditions 130°C/85%RH showed any signs of moisture saturation. The time allocated to studying moisture ingress was limited, and as the initial tests at the highest temperature (130°C) had shown, saturation would take many hundreds (possibly thousands) of hours so the time to saturation at the lower temperatures had to be extrapolated. This is justified by the assumption that the weight of absorbed moisture at saturation is dependent on the number and length of open paths in the plastic material and the time to saturation depends on the energy of the water molecules which in turn is dependent on temperature.

Saturation was observed to occur at 0.3% of package weight. The effect of temperature on weight gain, as a percentage of initial weight against exposure time, is shown in Figure 3. Weight gain was observed to approach the saturation level asymptotically therefore it is difficult to judge when saturation occurs. Therefore the time to 90% of the saturated weight was measured. The time to reach this value was averaged across the group of sample packages and the time to 90% of saturation ($T_{sat}$) was plotted against the reciprocal of absolute temperature, with humidity constant as shown in Figure 5. The times to saturation for 130°C and 120°C tests were obtained directly from the data, however the time to saturation for the 110°C tests had to be obtained by extrapolation as it appeared that saturation would not occur before 1000 hours.
Table III Test Conditions for Weight Gain Tests

<table>
<thead>
<tr>
<th>Test Conditions (Celsius/%RH)</th>
<th>Sample Size</th>
<th>Time to Saturation (Hours)</th>
<th>Saturated Weight Gain (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>130°/85%</td>
<td>10</td>
<td>50</td>
<td>0.3</td>
</tr>
<tr>
<td>120°/85%</td>
<td>10</td>
<td>150</td>
<td>-</td>
</tr>
<tr>
<td>110°/85%</td>
<td>10</td>
<td>~1,000</td>
<td>-</td>
</tr>
<tr>
<td>130°/75%</td>
<td>10</td>
<td>100</td>
<td>0.25</td>
</tr>
<tr>
<td>130°/65%</td>
<td>10</td>
<td>&gt;100</td>
<td>0.13</td>
</tr>
</tbody>
</table>

Figure 3 Weight Gain of Plastic Packaged I.C.s Exposed to High Relative Humidity.

A similar approach may be followed to obtain an expression for dependence of moisture absorption on relative humidity. The percentage increase in weight due to moisture absorption at different values of relative humidity was plotted against time, as shown in Figure 5. From this data it was found that the 90% saturated weight gain
increased by approximately 0.008% for every one percent increase in relative humidity (over the range 65-85%RH). The kinks in figure 3 could be due to experimental error in the readings taken after 75 hours of HAST testing. Alternatively they could be due to effusion of moisture vapour back out of the packages after stress testing but prior to weighing. The packages were allowed to cool for four hours to attain thermal equilibrium before handling. The rate of effusion from the package back to ambient would have depended on the room ambient temperature and humidity. The later of these there was no control over thereby introducing a degree of uncertainty into the measurements. The measurements after 75 hours at 130°C and 120°C and 50 hours 110°C could have been taken on particularly dry days. A laboratory hygrometer would have helped confirm this conjecture.

**Figure 4** Time to Saturation for Plastic Moulded Packages against Temperature
Figure 5 Weight Gain of PDIP Package as a Function of Relative Humidity
4.4 Parameter Drift in Bipolar Transistors

Having observed the behaviour of the moulding compound to moisture ingress the effects of moisture upon the electrical parameters of semiconductor devices was investigated. The devices chosen for this part of the study were bipolar transistors. They were chosen because; they would provide an understanding of the effects of moisture on the basic active devices in I.C.s, they could be readily and accurately characterised using existing test equipment, they were available in the standard D.I.L. package (a common I.C. package), were available in plastic and ceramic versions of the same package (allowing comparisons to be made), and were cheap and easily obtainable.

4.4.1 The Test Vehicles

The majority of work reported in the open literature has concentrated on catastrophic failures on logic devices (both bipolar and MOS). In contrast little has been reported concerning the effects on device parameters of humidity at high
temperatures. To assess the effects of moisture absorption on the behaviour of bipolar transistors the CA3086 IC was chosen. This is a simple integrated circuit consisting of five npn bipolar junction planar transistors fabricated on silicon by the epitaxy process. Each transistor is fabricated on the same substrate although they are independently terminated at the package pins.

It was decided to study the change in d.c. parameters that accompany moisture absorption as equipment for a.c. and noise measurement was not available. A series of initial measurements were undertaken to observe which d.c. parameters were the most susceptible to degradation and the dependence of this degradation has, if any, on temperature and relative humidity. Four parameters were chosen; reverse collector saturation current $I_{CBO}$, reverse collector-emitter saturation current $I_{CEO}$, the base-emitter $I/V$ characteristic, and D.C. current gain. The parameters $I_{CBO}$ and $I_{CEO}$ were chosen to assess the changes in leakage currents either resulting from package degradation or as leakage paths over the die. The diode characteristic of the forward biased base-emitter junction was observed as this shows the condition of the forward bias depletion region between base and emitter which is fundamental to transistor action. This was measured for various values of collector to emitter voltage $V_{CE}$ so that base width modulation effects could be observed. This showed that increasing $V_{CE}$ for constant $V_{BE}$ causes a decrease in base width due to the Early effect [3], and results in a decrease of recombination base current. The d.c. current gain $\beta$, was also chosen as a fundamental parameter of device operation which is susceptible to the formation of recombination centres within the device.

4.4.2 Initial Parameter Drift Studies

Initially samples of ten packages (50 transistors) were stressed at 130°C/85%RH with bias for 100 hours with measurements made at 20 hour intervals. The parameters are sensitive to temperature, so the temperatures at which the measurements were made was recorded to allow for temperature corrections. The bias voltages were chosen so as to be typical of device operation, the base-emitter voltage was held very slightly negative to prevent the device from conducting yet low enough to avoid avalanche breakdown of the base-emitter junction.

The measurements of $I_{CBO}$, $I_{CEO}$, base-emitter characteristic and $\beta$ were then
repeated for a range of test temperatures (130, 120, 110°C) at constant humidity (85%RH) and also over a range of humidity (85, 75, 65%RH) at constant temperature (130°C). This was done to determine the dependence of the observed degradation on environmental conditions.

<table>
<thead>
<tr>
<th>Test Conditions</th>
<th>Sample Size</th>
<th>Duration (Hours)</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>130°C85%</td>
<td>50</td>
<td>100</td>
<td>ICBO, ICEO, IB vs VCE, β</td>
</tr>
<tr>
<td>120°C85%</td>
<td>50</td>
<td>100</td>
<td>ICBO, ICEO, IB vs VCE, β</td>
</tr>
<tr>
<td>110°C85%</td>
<td>50</td>
<td>100</td>
<td>ICBO, ICEO, IB vs VCE, β</td>
</tr>
<tr>
<td>130°C75%</td>
<td>50</td>
<td>100</td>
<td>ICBO, ICEO, IB vs VCE, β</td>
</tr>
<tr>
<td>130°C65%</td>
<td>50</td>
<td>100</td>
<td>ICBO, ICEO, IB vs VCE, β</td>
</tr>
</tbody>
</table>

Table IV Test Conditions & Parameters for Initial Investigation

ICBO and ICEO Degradation - The temperature dependence of ICBO for a silicon transistor is the same as that of the reverse saturation current and doubles for every 10°C rise in temperature. During these tests measurement temperatures were logged to allow for corrections to be made for this effect. ICBO was measured at 20 hour intervals over a 100 hour period over the range of temperatures and humidity stated above. The drift in ICBO and ICEO during this period is shown in Figure 7. Measurement of these parameters showed no clear increase in leakage current during the test. The measured currents were very small, in the region of 1 to 100 pA, and the fluctuations that were observed were attributed to electrical noise and temperature effects, and are typical of the errors associated with the measurement of very small currents. Both these currents flow not through the bulk of the transistor but across the surface, thus indicating that either moisture had not yet reached the die (unlikely as the packages were already saturated, as can be seen from the graphs of weight increase) or the plastic moulding compound was still strongly bonded to the die surface preventing the formation of a moisture film.
Figure 7 $I_{CBO}$ and $I_{CEO}$ for PDIP BJT's against Test Duration

**Base-Emitter Characteristic and Early Effect** - The base-emitter current was measured as a function of base-emitter voltage for several values of collector-emitter voltage, thus allowing the base-width modulation or Early effect to be observed. This indicated that there was no increase in the base current, even at low values, so that the formation of a moisture induced conductive channel between base and emitter can be discounted. The lack of any change over time in the base-emitter characteristic for different values of applied $V_{CE}$ would suggest that little change has taken place in the depletion region of the reverse biased base-collector junction for stress durations up to 100 hours.

**Degradation of d.c. Current Gain** - Measurements of collector current over five decades of base current (0.1μA to 1mA) at predetermined values of $I_B$ were made and from this data the values of d.c. current gain ($\beta$) were calculated. The relative degradation in $\beta$ from the initial unstressed values were calculated and from these values the average degradation at each measurement interval was obtained. This average value that was plotted against time and shows the degradation in $\beta$ as a
function of base current over 100 hours under HAST (130°C/85%RH with bias), Figure 8. This process was then repeated to investigate the dependence of $\beta$ degradation against temperature, Figure 9, and humidity, Figure 10, over a 100 hour period. It was observed that there was a strong dependence of $\beta$ degradation on temperature and relative humidity whilst there was little change in the size of the leakage current measurements, $I_{CBO}$ and $I_{CEO}$. The effect of a collector base leakage path on gain degradation is shown by equation (1).

$$\beta = \frac{I_C - I_{(CBO)}}{I_B - (-I_{CBO})}$$

(1)

This describes the ratio of the collector-current increment to the base-current change from cut-off to $I_B$. For example to effect a reduction of 10% in $\beta$ at a collector current of 1mA would require a leakage current between base and collector of approximately 2.2 micro-amps. However the increase in $I_{CBO}$ induced by HAST testing was in comparison negligible, being at worst several orders of magnitude smaller. Clearly an alternative explanation of gain degradation from that of current flow through surface leakage paths is required. Similarly the small nature of the collector-emitter current $I_{CEO}$ is insufficient to account for the gain degradation by a leakage path shunting the collector-emitter current.
Figure 8 Gain Degradation in PDIP BJTs under H.A.S.T. against Base Current

Figure 9 Gain Degradation in PDIP BJTs as a function of Temperature

4-19
Figure 10 Gain Degradation in PDIP BJTs as a function of Relative Humidity
4.4.3 Long Term Parameter Degradation Studies

The results of the initial parameter drift study showed that d.c. current gain was the most sensitive parameter of those measured. Not only is it an important parameter in circuit design, but it is dependent on surface recombination effects as will be shown later. Observing the long term degradation of $\beta$ should give an idea of the state of the surface of the transistor, one of the possible causes of surface degradation can be a build up of impurities due to poor package integrity.

A long term test was conducted to observe the degradation of $\beta$ with time and the occurrence, and nature, of the final failure mechanisms. It was considered useful to compare the long term reliability of plastic packaged bipolar transistors against their ceramic (hermetic) packaged counterparts. A sample of 20 PDIP packaged transistor arrays were subjected to 1,500 hours of HAST at 130°C/85%RH along with the same number of identical arrays in CERDIP packages. Devices were removed from the test for measurement at 25 hour intervals up to 100 hours and at 100 hour intervals thereafter. The group of 20 PDIP devices was further sub-divided into two groups, the first (packages 1 to 10) underwent testing as described above and the second group (packages 11 to 20) were subjected to an additional temperature cycling after HAST testing but before measurement. This additional stress consisted of two cycles from -55 to 125°C intended to freeze and then vapourise any trapped moisture thereby simulating the effects outlined in 4.1. In addition to the HAST studies two samples of 10 transistor arrays (50 transistors), one PDIP one CERDIP, were subjected to elevated temperature stress also at 130°C with identical bias to those under HAST. This test was conducted to see the effects of high temperature in isolation from the effects of moisture. The value of relative gain degradation was calculated by the same method as used for the initial tests. Once a transistor had failed catastrophically its time to failure was noted and it was removed from the running average so that the number of transistors contributing to the average degradation data decreased with time.

The effects of HAST on the relative gain of plastic encapsulated devices is shown in Figure 11. This shows that the onset of degradation occurs within the first 25 hours of stress testing as moisture begins to permeate the package which is accompanied by in a 0.2% increase in weight. The data from the measurement at
### Test Conditions for Long Duration Beta Degradation Tests

<table>
<thead>
<tr>
<th>Test Type</th>
<th>Package Type</th>
<th>Number of Transistors</th>
<th>Duration (Hours)</th>
<th>Test Conditions (Celsius/RH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HAST</td>
<td>Plastic</td>
<td>80</td>
<td>1,500</td>
<td>130°C/85%*</td>
</tr>
<tr>
<td>HAST</td>
<td>Ceramic</td>
<td>80</td>
<td>1,500</td>
<td>130°C/85%</td>
</tr>
<tr>
<td>High Temperature</td>
<td>Plastic</td>
<td>40</td>
<td>1,200</td>
<td>130°C</td>
</tr>
<tr>
<td>High Temperature</td>
<td>Ceramic</td>
<td>40</td>
<td>1,200</td>
<td>130°C</td>
</tr>
</tbody>
</table>

*First 10 packages were subjected to additional temperature cycling from -55 to +125°C before measurements conducted.

Table V Test Conditions for Long Duration Beta Degradation Tests

1,000 hours was observed to be subject to experimental error and has been omitted. The data from the two sub-groups employed to investigate the effects of temperature cycling showed no significant difference between the degradation observed in the temperature cycled and non cycled packages. Therefore they are treated as one group for the purposes of the β degradation studies. The degradation in the ceramic packaged devices is shown in Figure 12. The graph of β degradation follows much the same shape as that exhibited by the plastic encapsulated devices but its on-set was delayed by on average 500 hours. It was unlikely that the package degradation process in this case was one of permeation and failure of the package seal was suspected. Investigation of the ceramic packages integrity was undertaken using the procedures for gross and fine leak testing as specified in MIL-STD-883 method 1014.5. This technique exposes the packages to a helium atmosphere at high pressure and then measures subsequent leakage of helium from the package with a mass spectrometer. The leakage rates were small, compared to the reject criteria for military service of $1 \times 10^{-7}$ c.c./sec air at one atmosphere. These devices would not have been disqualified for use owing to poor sealing. The results of this test are shown as equivalent leakage rates at atmospheric pressure Table II.

The effects of high temperature operation on device gain are shown in
<table>
<thead>
<tr>
<th>Package Number</th>
<th>Leak Rate (c.c./sec of air at atmospheric pressure)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6x10^-9</td>
</tr>
<tr>
<td>2</td>
<td>1x10^-8</td>
</tr>
<tr>
<td>3</td>
<td>6.5x10^-9</td>
</tr>
<tr>
<td>11</td>
<td>1.5x10^-9</td>
</tr>
<tr>
<td>12</td>
<td>1x10^-9</td>
</tr>
<tr>
<td>13</td>
<td>9x10^-10</td>
</tr>
</tbody>
</table>

Table VI Helium Leak Rates for CERDIP Packages Subjected to HAST

Figure 13 for the plastic encapsulated devices and in Figure 14 for the ceramic packaged devices. In both cases degradation is small when compared to that observed under HAST and is really only significant (>5%) in the plastic encapsulated components for times in excess of 1,000 hours.
Figure 11 Average Gain Degradation of Plastic Encapsulated BJT s under HAST

Figure 12 Average Gain Degradation of CERDIP Packaged BJT s under HAST
4.4.4 Explanation of Observed Gain Degradation

An explanation for the observed gain degradation was sought. The importance of surface effects on the gain of transistors has long been known [4]. It is well known that the presence of an electrical charge on the oxide, either applied as a voltage to a gate electrode above the oxide layer, or due to the accumulation of surface charge, can effect transistor gain. Reddi [5] investigated the affects of surface charge on the current gain of silicon bipolar transistors with specially fabricated transistors that incorporated a gate electrode over the depletion region. By applying a voltage to this electrode he simulated the presence of surface charge on the oxide. The presence of charge was shown to extend the depletion region under the oxide and eventually cause inversion. If the gate electrode is considered as a capacitor with the oxide as the dielectric, then an equivalent surface charge density can be calculated for a given applied voltage. The reduction in gain is due to an increase in the density of charge on the oxide layer. The presence of this excess charge attracts free carriers of opposite polarity towards the surface from the bulk. As a result the carrier concentration at the
GAIN DEGRADATION IN BJTs UNDER HIGH TEMPERATURE STRESS AS A FUNCTION OF STRESS TIME OVER FIVE DECADES OF BASIC CURRENT

Figure 14 Average Gain Degradation of CERDIP BJTs at High Temperature

surface is different from that of the bulk [6]. Electrons and holes recombine at the traps forming a current that flows from the base as excess current. The phenomena of recombination in semiconductors was first reported by Shockley, Hall and Read [7] [8] hence they are sometimes referred to as Shockley-Hall-Read or SHR traps.

Recombination centres also exist in the bulk of the material as a result of impurities and crystal defects, and at the surface as a result of the inevitable mismatch in the crystallographic structures of the oxide and semiconductor. Bulk traps are fixed in the body of the semiconductor but their density can increase due to migration into the silicon of impurities such as gold [9]. Surface trap density will increase according to the condition of the oxide surface.

Comparison of the results from the HAST test, Figure 11, and elevated temperature stress test, Figure 13, shows that the gain degradation process is strongly influenced by the presence of moisture. This suggests that the moisture front penetrating the plastic may be hydrating mobile ions and transporting them through the plastic and eventually onto the silicon oxide passivation layer. This accumulation of charge on the oxide may then be responsible for the formation of recombination centres.
This explanation is further supported by the absence of any significant increase in the leakage currents $I_{cBO}$ and $I_{cEO}$ suggesting that the charges are effectively isolated from one another thereby denying a conduction path across the passivation layer. This would manifest itself as surface leakage current which could be measured between device terminals. It also suggests that there was no conduction path between package pins due to a build up of ionic compounds on the package surface. The absence of an appreciable surface leakage current in turn suggests that de-bonding between the moulding compound and the die surface has not occurred, a fact that is supported by the C-SAM images (Figure 17 and Figure 18) that are discussed later. Gain reduction has been reported for devices aged at high temperature (200°C) with bias applied for durations of up to 1,500 hours [10]. In this study gain reduction is observed in the presence of moisture at lower temperatures (110-130°C) and shorter duration (25 hours).

The gain reduction observed during the HAST tests was dependent on the value of base current and hence the level of emitter injection. This suggests the trapping of significant numbers of carriers was taking place at low injection levels, an effect that becomes swamped as emitter injection increases. The degradation was observed to increase with the duration of exposure to HAST suggesting the build up of traps with time. The greatest rate of degradation occurred within the first fifty hours of exposure, over this same period the package was observed to saturate with moisture, Figure 5.
4.5 Failure Analysis of Catastrophic Failures

To investigate the ultimate failure mechanisms in plastic packaged devices, samples were removed from the long duration HAST test (130°C/85%RH) after failure. During the test the β of the devices was monitored as this parameter was previously found to be sensitive to moisture ingress, it also provided a method of detecting catastrophic failure. Catastrophic failure in this case was considered to have occurred if an open or short circuit was detected at one or more of the device terminals. The first catastrophic failures was observed after 200 hours and failures continued to occur throughout the test until it was stopped at 1500 hours. The data was analyzed as two groups, those devices which had undergone temperature cycling (2 cycles -50 to 125°C following each HAST test) and those that had not been temperature cycled. The time to catastrophic failure is shown for the non-temperature cycled devices in Table VI and the temperature cycled ones in Table VII. The times to failure for both the temperature cycled and non-temperature cycled devices were plotted on Weibull paper, are shown in Figure 15.

Analysis of the Weibull plots showed there to be no significant difference in the shapes of the two distributions. Both have β values of 1.6 which are consistent with an increasing failure rate which would be expected for a "wear-out" type of failure mechanism.
<table>
<thead>
<tr>
<th>Time Hours</th>
<th>Number of Failures</th>
<th>Cumulative Failures</th>
<th>Gamma Corrected</th>
<th>Cumulative % Failed</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-100</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>100-200</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>200-300</td>
<td>1</td>
<td>1</td>
<td>50</td>
<td>2</td>
</tr>
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<td>300-400</td>
<td>2</td>
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<td>700-800</td>
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<tr>
<td>800-900</td>
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<td>650</td>
<td>56</td>
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<td>900-1000</td>
<td>9</td>
<td>37</td>
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<td>74</td>
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<tr>
<td>1000-1100</td>
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<td>37</td>
<td>850</td>
<td>74</td>
</tr>
<tr>
<td>1100-1200</td>
<td>0</td>
<td>37</td>
<td>950</td>
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<td>1200-1300</td>
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<td>1050</td>
<td>74</td>
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<td>37</td>
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</tr>
<tr>
<td>1400-1500</td>
<td>0</td>
<td>37</td>
<td>1250</td>
<td>74</td>
</tr>
</tbody>
</table>

Table VII Occurrence of Catastrophic Failures BJT Arrays - Not Temperature Cycled
<table>
<thead>
<tr>
<th>Time Hours</th>
<th>Number of Failures</th>
<th>Cumulative Failures</th>
<th>Gamma Corrected</th>
<th>Cumulative % Failures</th>
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<td>1350</td>
<td>80</td>
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</table>

Table VIII Cumulative Failure Data of BJTs - Temperature Cycled
Figure 15 Weibull plot of Catastrophic Failures in PDIP BJTs
4.5.1 Non Destructive Failure Analysis

The failed devices were subjected to a number of failure analysis techniques to determine their failure mechanisms, non destructive methods were employed initially. To investigate whether de-bonding of the moulding compound to the die/leadframe had occurred scanning acoustic microscopy (C-SAM) was employed. This technique can detect the presence of delamination and cracking in packages by measuring the return delay of an ultra sound pulse fired into the package. The velocity of propagation of ultrasound in air is slower than its velocity through a solid therefore voids can be detected by scanning the package with ultra sound pulses and measuring the time taken for the return pulse to arrive back at the transducer. The duration of the return delay is colour coded and displayed graphically with blue for the shortest return time and red for the longest. A well bonded area returns a blue/green signal and a poorly bonded area a yellow/red indicating the longer delay associated with the introduction of an air gap between components of the package. This technique is employed in the semiconductor packaging industry to assess the quality of moulded packages. It was used here to investigate whether de-bonding of the moulding compound to the die/leadframe had occurred during accelerated life testing. Two packages from the long duration HAST test, along with one sample which had been subjected to extensive temperature cycling (-55 to 125°C, 100 cycles) were investigated. The packages were scanned from above and below. The two samples from the HAST test showed no signs of delamination between die and plastic, as shown in Figure 17 and Figure 18. It was concluded that even after such a severe stress test the epoxy novolac moulding compound had remained well bonded to the die/leadframe interface, as no evidence of de-bonding was observed. Unfortunately only two packages from HAST and one from temperature cycling could be examined by this method on the grounds of cost.

The sample from the temperature cycling test showed signs of the onset of de-bonding, as illustrated by the yellow region in Figure 16. Owing to scheduling difficulties with the external consultancy (Towcester Technical Services) it had not been feasible to scan this package prior to the stress test (as was the case with the specimens subjected to HAST) therefore it was not possible to say conclusively that delamination had occurred as a result of the test or during manufacture.

4-32
Figure 16 Acoustic Micrograph of PDIP Subjected to Temperature Cycling

Figure 17 Acoustic Micrograph of P-DIP after HAST - Top Image.
4.5.2 Decapsulation

Once non destructive failure analysis was completed the plastic packaged devices were de-encapsulated by the hot acid technique using a "Jet-Etch" machine. This removes a small area of moulding compound above the die with a stream of hot (200°C) concentrated sulphuric acid. The stream is produced by the Venturi action of a stream of tap water at high pressure across a vessel containing the acid. The acid is drawn on to the package's surface where it dissolves the organic resin and both resin and the freed silica filler particles are washed away. An electrical connection between the package's bonding wires and the acid is made as soon as the acid has etched through to the wires. This connection may be used to stop the etch immediately or allow the experienced operator to continue the etch for several seconds longer until the die has become fully exposed. With care such a technique can reliably remove the plastic from above the die whilst leaving all the gold bonding wires intact. The aluminium metallisation is protected by the passivation layer (silicon dioxide) and its naturally occurring passivating oxide layer so that it is not attacked by the acid.
4.5.3 Microscopy

After the packages had been de-capsulated their exposed dies were examined by optical microscopy. Using this technique the integrity of the bond wires, bonding pads and metallization could be examined. This revealed several occurrences of corrosion of the metallization which were associated with cracks in the passivation layer. Several dies showed broken bonds where the ball-bond of the bonding wire had separated from the bond pad. Once the sites of interest had been identified by optical microscopy they were examined in greater detail by Scanning Electron Microscopy (S.E.M.). With this technique it was possible to obtain a more detailed picture of the failure sites with greater contrast and depth of field. The extent of corrosion in the packages and the frequency of occurrence of lifted bond pads is shown in Table V. The failure mechanisms observed were, metallisation corrosion and voiding between bond pad and bond wire examples of which as shown in Figure 20, and Figure 19 respectively. Three samples were removed prior to decapsulation for metallurgical cross-sectioning.
Figure 19 Electron Micrograph of Voiding Formation at the Bond Pad.

Figure 20 Optical Micrograph of Metallisation Corrosion
<table>
<thead>
<tr>
<th>Package Number</th>
<th>Occurrence of Damaged Passivation</th>
<th>Occurrence of Metallisation Corrosion</th>
<th>Number of Damaged Bond Pads</th>
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</thead>
<tbody>
<tr>
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<td>4</td>
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<td></td>
</tr>
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<td>Removed for Cross-Sectioning</td>
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<tr>
<td>20</td>
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</tbody>
</table>

Table IX Occurrence of Failure Mechanisms in PDIPs Subjected to HAST.
4.5.4 Bulk Analysis

Once all the information that could be gained by electrical measurements, C-SAM, and microscopy, had been gathered then areas of interest on the die surface were subjected to bulk analysis techniques. Surface analysis techniques would have been more appropriate if a non-etching process such as "plasma-ashing" could have been employed. This process was not available and as acid had unavoidably come into contact with the die surface as part of the decapsulation process it was felt inappropriate to use surface analysis techniques to discover the chemistry of the corrosion sites. Instead bulk analysis techniques were chosen where the chemistry just below the surface could be investigated.

![EDX Spectra at site of Metallisation Corrosion](image)

**Figure 22 EDX Spectra at site of Metallisation Corrosion**

*Energy Dispersive X-Ray (E.D.X.)* - The corrosion sites were investigated by EDX whilst undergoing electron microscopy. The presence of the chlorine was detected on corroded metallisation which had been exposed due to a cracked passivation layer, Figure 22. Owing to the nature of the EDX sensor only elements with atomic masses greater than sodium can be detected.
Figure 22 EDX Map for Aluminium at the Bond Pad / Bond Wire Interface

Figure 23 EDX. Map of Gold at a Bond Pad / Bond Wire Interface
The EDX detector may be tuned to detect the presence of a particular element and a map of its concentration can be produced. The samples that had been prepared by metallurgical sectioning were examined by this technique for the occurrence of gold and aluminium in the bond pad interface region. This showed the migration of gold into the aluminium and aluminium into the gold in some of the failed bondpad regions and showed regions of voids at the aluminium/gold interface. An example of this is illustrated in Figure 23 and Figure 24. Examination of the electron micrograph of the same region showed regions of voids in the aluminium/gold interface, Figure 25. Bond pad lifting was observed by microscopy in 14 of the 17 packages and chlorine was detected by EDX at these sites. Owing to the high rate of occurrence of corrosion in the bondpad region, especially those which were positively biased, it was conclude that this exposed region of the die was vulnerable to damage in the presences of moisture. The existence of a positive potential was particularly important in attracting hydrated cations such as the chloride ion.

![Figure 24 EDX Spectra of Contamination at a Positively Biased Bond Pad.](image)
Laser Ionisation Mass Analysis (L.I.M.A.) - Further investigation of the chemistry of corrosion sites was possible using L.I.M.A. This technique uses a burst of laser radiation to ionize a region of die producing a small crater of about 1 μm diameter and up to 5 μm deep. The resulting ionised matter is accelerated by an electrical field into a "time of flight" mass spectrometer where its composition may be analyzed according to atomic mass. According to the polarity of the accelerating electric field either positive or negative ions are analyzed. Since the laser beam is located by optical microscopy it cannot be aimed onto the site of interest as accurately as EDX, where aiming is accomplished by S.E.M., it does however have the advantage of being able to detect the ions of all chemical elements and can provide depth profiling.

The ions detected at the failed bond pads and metallisation sites using this technique are shown in Table IX. They are tabulated according to the polarity of the applied electrical bias during the accelerated life test and the polarity of the accelerating voltage applied to the mass spectrometer.

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<th>Spectra</th>
<th>Ions Detected</th>
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<td>Positive</td>
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</tr>
<tr>
<td></td>
<td>Negative</td>
<td></td>
<td>Cl, Br, Au</td>
</tr>
<tr>
<td></td>
<td>Negative</td>
<td>Positive</td>
<td>Al, A, Au</td>
</tr>
<tr>
<td></td>
<td>Negative</td>
<td></td>
<td>Cl, Br, PO₂, PO₃, Au</td>
</tr>
<tr>
<td>Metallisation</td>
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<td>Positive</td>
<td>Al</td>
</tr>
<tr>
<td></td>
<td>Negative</td>
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<td>Cl, O, OH, S, AlO, AlO₂, PO₂, PO₃</td>
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<tr>
<td></td>
<td>Negative</td>
<td>Positive</td>
<td>CN, S, O, OH, AlO, AlO₂</td>
</tr>
</tbody>
</table>

Table X Ions Detected at Failure Sites by L.I.M.A.
4.6 Comparison of Bondpad Reliability

The HAST test data on PDIP bipolar transistors showed that the bondpad area of the die in plastic encapsulated devices is vulnerable to corrosion due to the fact that it is left exposed so that wire bonding can be conducted. The aluminium gold interface is prone to corrosion and voiding as a result of the formation of intermetallic compounds. It also leaves an area of metallisation exposed so that corrosion can under-cut the passivation layer.

In 1992 a well known semiconductor manufacturer released a range of operational amplifiers which are encapsulated in a plastic package and employs a Titanium/Tungsten alloy overcoat over the bondpad area. It was claimed that this barrier effectively seals the die from moisture permeation via this route, and provides a buffer layer between the aluminium bondpad and the gold bonding wire. These devices are intended for high temperature operation (150°C maximum), this exceeds the standard commercial plastic device operating temperature range of 0 to 70°C by 80°C, and exceeds the ceramic package device specification of -55 to 125°C by 25°C. These devices are intended for use in automotive applications where they would be used as transducer amplifiers located close to sensors in areas of high temperature such as engine blocks or braking systems.

This technology appears to present an opportunity to increase the reliability of plastic packaged devices by reducing the occurrence of the most prolific failure mechanism that was observed during the experimental work on bipolar transistors. To prevent possible problems with intermetallic migration and voiding, the bond pad is coated with a layer of Ti/W alloy which completely covers the bond pad and extends out over the silicon nitride passivation layer and, it is claimed, seals it effectively making the package hermetic. Packages fabricated by this technique ought to have the potential to protect the die more effectively from the corrosive effects of moisture and the formation of inter-metallic compounds at high temperature which are responsible for weakening the bondpad interface. This new bonding technique is compared to the conventional bondpad structure in Figure 26.

To gauge the reliability performance of devices using this over-coat technique
samples were subjected to a brief accelerated life test using HAST with bias. Its purpose was to investigate whether this new process offered greater protection against bondpad failure as no data on the reliability of this process could be found in the open literature. As it had been necessary to expose conventionally packaged plastic devices to stresses in excess of 400 hours to induce moisture related catastrophic failures so it was decided to employ the highest stress temperature possible that was consistent with the acceleration of field failures. Conditions of 130°C and 85%RH and bias were employed. To ensure bias consistent with operating condition the devices were configured as unity gain voltage followers with the non-inverting input clocked with a 1kHz sinewave. This ensured that the output transistors did not remain in only one state and therefore promote corrosion of one polarity.

The devices were removed from test initially at 25 hour intervals for the first 100 hours and at 100 hourly intervals thereafter up to 600 hours. The parameters monitored were input offset current, input offset voltage and open-loop gain. Parametric drift being monitored as well as the occurrence of catastrophic failures. Catastrophic failure was judged as complete failure to operate due to the presence of an open or short circuit.
The occurrence and nature of the parameter drift in the measured parameters was small and cannot be directly compared to that observed in the study using bipolar transistors. Only data on catastrophic failures is compared as it is only a comparative reliability of the two bondpad types that was of interest to the sponsoring organisation. Of the twenty packages subjected to HAST six out of eighty operational amplifiers were found to be defective (catastrophic failures) after 600 hours of testing. This compares with thirty four defective bipolar transistors out of a sample of one hundred (twenty packages) using the conventional bondpad construction.

Although these are only the most preliminary of results, and more work needs to be done, it is concluded that the titanium/tungsten over coat provides an improved degree of protection over the conventional structure.
4.7 Summary

It has been shown that plastic packages absorb moisture from the atmosphere. The rate of absorption is dependent on the energy (temperature) of the moisture molecules on the package surface. The quantity of moisture absorbed depends on the quantity of moisture present in the atmosphere, the relative humidity. The plastic will absorb moisture at a rate dependent on temperature up to an amount governed by the ambient humidity.

Moisture absorption has been observed to cause two types of failures, parameter drift and catastrophic failure. Gain degradation was the most prevalent form of degradation in the d.c. characteristics of bipolar transistors. It was shown that the degradation was not due to simple ohmic leakage paths but to a more subtle form of degradation in transistor action. This was attributed to the build up of recombination centres in the oxide due to the migration of ionic contamination within the package. Such a process has been observed under high temperature stress tests (200°C) by other researchers. It has been shown that this process is further accelerated by the presence of moisture which hydrates the impurity ions and transports them through the moulding compound. Owing to the very sensitive nature of minority charge carriers in the emitter-base depletion region to the presence of recombination centres only very low concentrations are needed to produce gain degradation. The degradation manifests itself as an increase in base current due to the increase in recombination of electron hole pairs in the emitter-base depletion region. The increase in base current for a given value of collector current is observed as a decrease in d.c. current gain.

Catastrophic failures were observed to occur several hundred hours after parameter degradation. These failures were almost certainly due to the loss of electrical continuity across the bond pad. This area is left exposed in the conventional wire bonding method making it vulnerable to attack by mobile ions especially when bias is applied. Corrosive ions (Cl⁻ & Br⁻) were detected in this region after several hundred hours exposure to high temperature and humidity in the presence of an electric field. Comparison of the occurrence of catastrophic failures in conventionally bonded dies with those using this technique shows those using a Ti/W layer to be superior.
4.8 References


CHAPTER 5

INVESTIGATION OF PLASTIC PACKAGING BY ENCAPSULATED SENSORS

5.1 Introduction

Chapter four showed that it was possible to assess the effects of packaging on device reliability by exploiting bipolar transistor structures as test vehicles in P-DIP packages. To assess the performance of the more complex high lead-count surface mount packages a different approach was required. The previous method was not applicable owing to the non-availability of bipolar transistor arrays in these packages. The use of VLSI devices, usually encapsulated using this type of package, to monitor package performance was discounted owing to problems with characterising degradation in such complex components, hence an alternative test structure was sought. It was felt that the use of a special test chip with sensors specifically designed to measure those parameters that are of particular interest in assessing this kind of package should be used. A search of the literature was undertaken and this produced a number of possibilities, each of these was explored and finally the PMOS3 test chip from the National Microelectronics Research Centre (N.M.R.C.) at Cork in Ireland was selected.

5.2 Review of Package Performance Test Chips

Several alternative test structures were examined. Firstly the possibility of designing a test chip "in-house" was considered, and approaching an academic or industrial fabrication facility to have a number built. This would have been a very
expensive and time consuming alternative as no experience in this field was available at I.E.R.I. so this approach was discounted once it was clear that commercially available devices existed. All the known sources of test chips are shown in Table I.

Of the devices summarised the Analogue Devices test chips were discounted after negotiations with the manufacturer, as they were not prepared to release any for use by other organisations. The Electrical Research Association (E.R.A.) devices contain only those sensors relevant to the measurement of die stress. These devices could not be used to gather information on moisture ingress. The S.G.S. device, code number SD1/2, looked like a possible contender but did not offer as comprehensive a range of sensors as were available in the N.M.R.C. range. Hence it was decided to examine the possibilities afforded by these devices.

The literature search had shown that the major causes of package related device failures are caused by either moisture ingress or stress on the die and bonding wires. It was obvious that, for comprehensive assessment, a test chip containing both moisture and strain sensors would be necessary. This meant that a choice between the PMOS2, PMOS3, or PMOS4 test chips would have to be made. The choice of which PMOS test chip to use would be largely governed by which styles of package were available for its encapsulation. There were two possible package styles available, P.L.C.C. and Q.F.P. The P.L.C.C package style was only available in designs with up to 88 leads. This would have meant that if the PMOS3 chip were used then some of its sensors would have had to remain unused. Therefore a Q.F.P. style package was employed as all of its sensors could be then be connected. As the Q.F.P. style of package is generally thinner and smaller than the P.L.C.C. package it could be expected to be potentially more susceptible to environmental effects. It would have been preferable to have assessed the performance of P.L.C.C packages as well as Q.F.P.s, but this would not have been possible within budget and time constraints. The Q.F.P. is the only plastic package capable of supporting 100 or more lead devices, and it is in such packages that many new ICs are appearing.

The plastic QFP has become a well established package for VLSI devices, it offers small size and a low profile (1.4mm thick) and is available in styles from 84 to 288 leads. The main force behind the rapid adoption of QFPs has come from the personal computer and mobile communication markets and is expected to take an ever
larger share of the IC package market [1].

As with all package styles the cost and difficulty in obtaining suitable HAST test boards and sockets for QFP packaged devices increases with lead count. The number of sub-contract packaging facilities that can process the newer high lead count packages appears to decrease with increasing pin count. Therefore the PMOS3 test chip was selected as it provided all the desired sensors at the minimum of cost and could be encapsulated into a 100 lead Q.F.P. package (a widely used industry standard package). An example of a PMOS3 die is shown in Figure 1. The sensors available on the PMOS3 test chip are listed in Table II.

Enquiries were made of I.C. manufacturers and sub-contract encapsulation companies to find one prepared to carry out the packaging of the test chips. Unfortunately there were virtually no European based plastic I.C encapsulation facilities in operation at the time. Almost all of the companies approached have switched to Far Eastern production facilities on the grounds of cost. The only European based organisation was Euratec in the Netherlands, the largest package they could offer was a 88 lead P.L.C.C. Fortunately the D.R.A. were able to exercise their contacts at Mintech Semiconductors a U.K. based packaging house specialising in hermetic packaging for high reliability applications. This organisation has had some contacts with a reputable sub-contract packaging house in Malaysia. It was confirmed that the Malaysians were able to offer the 100 lead Q.F.P. package as part of their range. Contact with this facility was established via Mintech and despite the very small quantity of devices to be packaged (1 wafer) negotiations were successful and they were chosen to undertake the test chip packaging.

The unscribed PMOS3 wafer was despatched to Mintech Semiconductors who marked the non-functional dies with ink dots according to the wafer map supplied by the N.M.R.C. It was then despatched to Malaysia for scribing and encapsulation. Both the dice that had tested as functioning within specification and those that did not were encapsulated. The packages containing non-functional dice were coded with an "I" suffix to denote an inked die. The purpose of this was that although non-functional dice could not be used to gather data it was thought that they would prove useful in "dry runs" to test experimental procedure without the costly expedient of using fully functioning packaged test chips. The packaged I.C.s were identified by the printed
codes I.E.R.I. PMOS3, which was suffixed /I for those containing non-functional dice. The packaged PMOS3 test chip used in the following experimental work is shown in figure 2. A table of the lead connections is given in Appendix A, a wafer map, showing the bond wire connections in Appendix B, and a wafer specification in Appendix C.
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<th>Commercially Available</th>
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<td>PMOS 2</td>
<td>Resistance Heater, Temperature Sensor, Corrosion Monitor, Strain Gauges</td>
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<td></td>
<td></td>
<td>PMOS 4</td>
<td>Resistance Heater, Temperature Sensor, Corrosion Monitor, Strain Gauges, Daisy Chain Interconnections</td>
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<td></td>
<td>CMOS 2</td>
<td>Polysilicon Resistor Heater, Diode Temperature Sensors, Daisy Chain Interconnect, Test Structure Test Pads</td>
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<td>Diffused Resistor Heat Source, Diode Temperature Sensors</td>
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<td>Large area diffused resistor</td>
<td>Simulates dissipation</td>
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<td></td>
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<tr>
<td>Triple track aluminium meanders</td>
<td>1/ Corrosion Monitors</td>
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<tr>
<td></td>
<td>2/ Moisture sensor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3/ Metallisation shift monitors</td>
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<tr>
<td>Piezo-resistive diffused</td>
<td>Measures the strain on the die at several</td>
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<td></td>
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</tr>
<tr>
<td>p-n junction diodes</td>
<td>Sensing temperature at die surface</td>
<td>2</td>
<td></td>
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<td>Wire bond resistance structure</td>
<td>Monitors variation in wire bond resistance</td>
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<td>Substrate contact</td>
<td>Surface Ohmic contact to substrate bulk</td>
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</table>
5.3 PMOS3 Test Chip Sensors

The test chip sensors can be divided into devices for two specific tasks, those associated with the effects and rate of moisture ingress and those associated with the measurement of on stress on the die.

5.3.1 Moisture Ingress Monitors

The moisture detectors consist of three parallel aluminium tracks laid parallel on the die surface. There are four of these, two are covered by the passivation layer and two are unpassivated thus leaving them in contact with the moulding compound. The track width is ten microns as is the separation between tracks. The lines are 1 micron thick, and have a typical resistance of nominally 220 Ohms. Each of these tracks are terminated at a bond pad and are connected to the package pins by gold bonding wires in the normal
5.3 PMOS3 Test Chip Sensors

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5.3.1 Moisture Ingress Monitors

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able to hold off the advance of moisture.

2/ The occurrence of aluminium metallisation corrosion can be assessed by measuring the resistance of the tracks when they are exposed to a series of temperature and humidity stresses. During biased testing the central conductor can be grounded and the two outer conductors can be biased one positively and one negatively so that the occurrence of both anodic and cathodic corrosion can be studied.

5.3.2 Stress Gauges and Associated Structures

In addition to the triple track meanders the test chip has five stress gauges, arranged as shown in Figure 3. Each gauge is comprised of four elements spaced radially at 45° intervals. The elements are diffused resistors whose resistance changes with the piezo resistive stress it experiences. Each element is terminated with two electrical connections at one end to facilitate four terminal measurement so that resistance measurements can be accurately determined.

In addition to the stress gauges the test chip is provided with two diffused resistors which are fabricated underneath the corrosion monitors. These occupy a large area of the chip and can provide uniform heating of the die thereby simulating dissipation. Such dissipation raises the temperature of the die and produces internal stresses in the package owing to the different coefficients of thermal expansion (cte) between epoxy, silicon and leadframe.

In addition to their role in moisture detection the unpassivated corrosion monitors can be used to measure the extent of stress-induced shift in the aluminium metallisation, as a change in resistance with temperature.
Figure 3 Configuration of Stress Gauges on PMOS3 Test Chip

5.3.3 Test Chip Monitoring Equipment

To be able to conduct the large number of electrical measurements required using the many on chip sensors of the PMOS3 die it was necessary to devise a method of interconnection capable of switching a number of instruments between the 100 leads of the device. This switch must be capable of control over the GPIB so that its operation could be synchronised with the operation of the instruments. To achieve this a Keithley model 707 switching matrix was used. This versatile piece of equipment was employed throughout all the measurements conducted upon the test chips, it provided a convenient method of connecting up to eight instruments to the 100 leads of the device under test.

The switching matrix consists of a "mainframe" unit into which could be plugged up to six matrix cards. A range of matrix cards are available from the manufacturer for different purposes. A general purpose card was used for this study. This card provided a matrix of twelve columns by eight rows of cross points. At each cross point a relay makes
or breaks the connection between row and column. Multiple row/column connections are possible simultaneously, and all connections between rows and columns are allowed. Each electrical connection consists of a Hi, Lo, and a guard channel. In addition the complete matrix/mainframe assembly is completely screened to minimise interference, the incorporation of guard channels and compressive screening makes low level measurements, such as leakage current, possible.

In order to perform a measurement the test chip was placed into a zero insertion force (ZIF) socket. This mated with a small printed circuit board (PCB) assembly which brought out the 100 leads to standard Insulation Displacement Connectors (IDC). The minimum length of colour coded ribbon cable was used to connect the IDCs to the switching matrix, the colour coding was essential to identify the large number of electrical connections that were involved.

Several instruments were connected to the switching matrix. The measurement of the resistance of the leakage paths, onset of corrosion, the resistance of the piezo-resistive strain gauges, and the measurement of die temperature was accomplished with a precision resistance meter, the Solartron 7061. A platinum resistance surface temperature probe was used to measure external package temperature, with an identical probe used to measure ambient air temperature above the test socket. A GPIB programmable power supply, the Hewlett Packard HP6632A, was incorporated into the test station. The programmable supply was used to power the on-chip heaters during the measurements of package stresses. The test chip measurement system is shown in Figure 4.
Figure 4 Test Chip Thermal Stress and Moisture Ingress Measurement System
5.4 Investigation into Moisture Ingress

Moisture ingress into the package could be detected with the four triple track aluminium conductor structures known as meanders. These consisted of three parallel conductor tracks that twisted across the majority of the chips surface area. When moisture ingress into the package occurs it permeates the plastic moulding compound until it reaches the die where a moisture film builds up on the die surface. This film often has an appreciable conductance as it hydrates ionic residues from the epoxy moulding compound. The measurement of a leakage current between the closely spaced conductors would indicate the presence of a moisture film.

To investigate the dependence of moisture ingress on environmental conditions, such as temperature and relative humidity, the test chips were subjected to HAST over a range of temperatures and relative humidity. Measurements of leakage resistance between the tracks were made, both for the passivated and unpassivated structures.

Minimising errors in the measurement of leakage resistance

Discussion of effects of complicated switching system on Electrometer measurements.

The electrometer was used to measure the very HIGH values of electrical resistance between adjacent tracks in the triple track meanders initially $10^9$ to $10^{11}$ Ohms. Of concern here was the leakage resistance of the cables and possible tracking across PCBs etc. At the start of the test the initial value of resistance was measured to be in the order of $10^{11}$ Ohms, (page 5-15 figs 6 and 7) suggesting that the leads/board resistances were at least this good.

By the end of the experiment the measured resistance had fallen to the order of $10^3$ Ohms, a degradation of 8 orders of magnitude. Only the test chips went into the autoclave and none of the test set up. No leads or boards, the only part of the system that under went HAST were solely the packages themselves. Before each measurement was performed the open circuit resistance of the test set up was measured as a "system confidence check". No appreciable leakage was ever observed.
Consideration of the relative magnitudes of the resistances involved shows that if, for example, the insulation resistance of the equipment was to degrade by one thousand times whilst standing on the bench over a period of say 3 weeks (about as long as it took to run the test) it would have fallen to $10^8$ Ohms, or 100 Meg Ohms, this would still only be $100M / 1K$ or 0.001% of the final value. Insignificant when compared to the 0.25 to 1.5% error due to the electrometer. Therefore it seems fair to ascribe all of the observed degradation in resistance to the test chips. Variation in contact and line resistances (approx. 1 Ohm) had no measurable effect.

Of concern in when measuring very high resistances is the effect of interference due to the radio frequency fields (RFI) and power line fields. The input of the electrometer can not respond to signals of greater than a few Hz. However problems can occur in the presence of strong RF fields which saturate the input amplifiers causing rectification to occur with subsequent errors in the dc value indicated. To avoid this special consideration had to be given to this element of experiement design with respect to shielding. The connections from the the electrometer to the screened enclosure of the switching matrix was by double screened Triaxial cable and connectors. These effectively eliminates any earth loops by screening the signal return path with screen grounded at only one end. The cabling from the switch box to the device under test had to be by ribbon cable, no other connection was physically possible. This was kept as short as possible right up to the package legs. This type of cable consists of many closely spaced parallel conductors. Thus providing a balance cable that effectively reduces the effects of the common mode current that would be produced by interference. All unused conductors were earthed at the switch and all power leads were run at right anlges and as far from measurement leads as was possible. A diagram of the apparatus is shown in Figure 5.

Given that screening precautions effectively served to eliminate measurement errors due to interference. The remaining source of errors were those associated with the instrument. In the range 200 to 20GΩ the accuracy is ±1.5% + 1count where the resolution is 10MΩ. Therefore the error in the measurement at the begining of the test, when the leakage resistance was 100GΩ, was ±1.51GΩ. By the end of the test the
leakage resistance had fallen to the region of 1KΩ with an associated error of 0.20% + 4 counts where the resolution was 100mΩ. Therefore the error in the measurement at the end of the test was ±0.2Ω. The instruments accuracy is given in Table II of chapter 4.

To monitor the effects of moisture ingress leakage resistance measurements between tracks were made for both the passivated and un-passivated meanders. The test conditions were 130°C and 85%RH with a bias of +10 0 -10 Volts applied between the tracks. Three PMOS3 test chips were used in the tests and the decrease in leakage resistance with time is shown in Figures 6 to 8 for the unpassivated tracks and 9 to 11 for the passivated ones.

For the unpassivated tracks resistance breakdown was observed to occur between 300 and 400 hours however device number 1 began showing degradation after 50 hours and appeared to undergo two separate degradation processes. All devices underwent complete breakdown displaying resistances of several hundred Ohms after 500 hours testing regardless of their initial degradation.

The passivated moisture sensors also displayed breakdown effects between 400-500 hours resulting in leakage resistances of several hundred Ohms, although in this case the onset of degradation was more sudden. It had been expected that the passivated structures would display a greater degree of moisture resistance than the unpassivated ones. A possible explanation of their apparent similar behaviour could be found in the fact that the passivation layer is undoped silicon dioxide of only 0.3μm thickness and was deposited by chemical vapour deposition. The encapsulating plastic is approximately five thousand times thicker than the passivation layer and has permeation rate $10^3$ to $10^4$ times greater so that moisture would breach both of them at much the same rate.
Figure 5 Wiring Schematic for Measurement of Leakage Resistance

Corrosion Monitor Leakage Resistance
Un-Passivated Sensor

Figure 6 Leakage Resistance Unpassivated Tracks - Device 1
Corrosion Monitor Leakage Resistance
Un-Passivated Sensor

Figure 7 Leakage Resistance Unpassivated Tracks - Device 2

Corrosion Monitor Leakage Resistance
Un-Passivated Sensor

Figure 8 Leakage Resistance Unpassivated Tracks - Device 3
Corrosion Monitor Leakage Resistance
Passivated Sensor

Figure 9 Leakage Resistance Passivated Tracks - Device 1

Corrosion Monitor Leakage Resistance
Passivated Sensor

Figure 10 Leakage Resistance Passivated Tracks - Device 2
5.5 Investigation into the Onset of Corrosion

The triple track meander structures may be employed in a different manner to determine the rate at which the absorbed moisture attacks the aluminium metallisation and causes corrosion by the action of ionic contamination and electrical bias. The measurement equipment employed was identical to that used to measure leakage resistance, except that instead of measuring the resistance between the meander lines, the resistance of the lines were measured. Owing to the versatility of the test equipment this required only a change in the software to reconfigure the switch matrix and instruments.

The onset of corrosion of the aluminium metallisation causes its resistance to increase as the metal reacts to form metal salts whilst the cross section of the remaining unreacted metal decreases. The increase in line resistance for the un-passivated corrosion monitors is shown in Figures 12, 13 and 14. In the instances where line resistance increased the increase was associated with the positively biased tracks of corrosion monitor CM2 indicating anodic corrosion. The lines displaying an
increase in resistance along their length were also associated with a decrease in leakage resistance between tracks.

The passivated corrosion monitors showed little or no increase in line resistance therefore only the worst case example is shown Figure 15. When line resistance is considered the passivated corrosion monitors performed better than their unpassivated counterparts.

Of the unpassivated corrosion monitors number 4 consistently fared far better than number 2. It was initially thought that this may have been due to its position on the die. The test chip comprised a square die in a rectangular package the leads on the perpendicular faces having a longer length of leadframe to the outside. However corrosion monitors 2 and 4 are diagonally opposite each other on the die with their electrical connections brought out on pins 7-12 and 64-69 respectively. Both these sets of leads are on opposite long sides of the 100 lead QFP package and therefore have short leadframe lengths to the outside. If the die was centred correctly on the paddle of the leadframe then both monitors would be expected to exhibit equal degradation.

*Measurement errors associated with meander line resistance*

In this experiment the presence of the relay contact resistance, connectors and cables that made up the test rig could be expected to contribute a source of error.

However the test chip provides for four terminal measurement. The terminals being joined on the semiconductor die. Hence as four terminal measurement was employed throughout this test all the contact and line resistances associated with; bondpads, bondwires, leadframe, IC socket, connectors, cabling, relay contacts, etc. are effectively eliminated from the measurement system. The sole source of error is therefore that quoted for the instrument itself when operating in four terminal mode. Even if the experiment had been conducted with a two terminal instrument the ±Ω or so contact/cabling resistance would have been small compared to the 200 Ω nominal resistance of the track before degradation (approx. 0.5%) decreasing as the line resistance increases to 500 Ω (0.1%) as the track corroded.
The Solartron D.M.M. has an accuracy of 0.1% when operating in standard four terminal measurement mode of resistance. Therefore the errors associated with the electrical measurements was therefore around $200 \pm 0.2\Omega$. 
Figure 12 Device 1 Corrosion Monitors 2 & 4 Un-Passivated Sensors

Figure 13 Device 2 Corrosion Monitors 2 & 4 Un-Passivated Sensors
Figure 14 Leakage Resistance Passivated Tracks - Device 3

Figure 15 Line Resistance Passivated Tracks - Device 1
5.6 Investigation into Package Related Stress

Moulded plastic packages are produced by encapsulating the leadframe and die in a polymer coating of cresol epoxy novolac resin which is loaded with silica particles. The packages are moulded at high temperature (175°C), as the moulding compound sets a compressive force is exerted on the die/leadframe due the formation of cross-linked bonds between polymer molecules. This polymerisation process is further enhanced by a curing phase (150-170°C) during which the polymerisation process is completed. As the package cools the compressive force on the die increases as the c.t.e of the moulding compound is greater than the leadframe.

Whenever two or more materials with different coefficients of thermal expansion (cte) are bonded together and subjected to a temperature change their dissimilar cte will cause a stress to occur as they each try to expand at different rates. The resulting stress produces a strain in the material equal to the product of the stress and its elastic modulus. If either of these materials is brittle then damage can occur. Despite manufactures attempts to produce IC packages made from materials with as closely matched c.t.e.s as possible thermally induced stresses still exist. Whether these stresses will be serious enough to cause concern depends on a number of factors such as; die size, metallisation track width, bond pad/wire geometries, as well as the temperature change and its gradient. Over small temperature ranges these stresses are acceptable but over the larger temperature excursions demanded of high reliability equipment there exists the possibility of damage to the die, bonding wires or metallisation. The cte of the materials commonly used for plastic IC packages are shown in Table III.

5.6.1 Principle of Piezo Resistive Stress Measurement

The principle of using piezo-resistive stress as a method of determining applied force has been known for over thirty years [2]. During the 1980s developments in the fabrication of small piezo-resistive strain gauges on silicon [3][4][5] made possible the development of monitoring chips for the measurement of package stress in electronic components. The early 1990s saw the integration of such stress transducers into package performance monitoring chips such as those from the NMRC. This has made
possible the measurement of actual package related stresses in prototype and commercially available package configurations, over a range of operating temperatures, where previously this information could only be derived by computer simulation. These devices are so new that up until now no reference to their use in assessing the performance of plastic packages could be found. The package induced stress is measured by stress gauges which are located at the corners of the die, as well as at the centre.

Semiconductor stress gauges exploit the piezo-electric properties of silicon to provide an electrical means of measuring applied force. Bittle et al [6] presented an explanation of the mathematical theory of piezo-resistivity and its application to semiconductor stress gauges. When an external stress is applied to silicon its resistivity becomes anisotropic. The observed change in resistivity depends on the direction of the flow of applied current with respect to the orientation of the crystal lattice. The change in piezo-resistivity in three dimensions is described by six fractional resistivity changes which are related to the applied stress by a matrix of coupling coefficients.

$$\frac{\Delta \rho_i}{\rho_i} = \sum_{j=1}^{6} \rho \sigma_j$$  \hspace{1cm} (5-1)
where $\pi_i$ are the components of resistivity, $\sigma_j$ is the component of the stress tensor in six-component vector notation, and $\pi_j$ are the material's piezo-resistive components in tensor notation.

Due to the symmetry of the silicon lattice only three of the thirty six matrix coefficients are independent and these are denoted as; $\pi_{11}, \pi_{12}$ and $\pi_{44}$. These three coefficients are sometimes refereed to as the fundamental coefficients and all the other coefficients may be derived from them, hence the piezo-resistive tensor may be simplified to equation (5-2).

$$
\begin{bmatrix}
\pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\
\pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\
\pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\
0 & 0 & 0 & \pi_{44} & 0 & 0 \\
0 & 0 & 0 & 0 & \pi_{44} & 0 \\
0 & 0 & 0 & 0 & 0 & \pi_{44}
\end{bmatrix}
$$

The values of the fundamental coefficients depend on temperature, doping density and carrier type.

The matrix of coupling coefficients is dependent on the choice and orientation of the coordinate system with respect to the crystal lattice. The basic coupling matrix is applicable when the $x,y,$ and $z$ coordinates are parallel the cubic planes of the crystal lattice. This situation is shown in Figure 16. Here the $x$ and $y$ axes are parallel to the [010] and the [001] directions in the plane of the [100] silicon surface.

$$
\begin{bmatrix}
\Delta_{xx} & \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\
\Delta_{yy} & \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\
\Delta_{zz} & \pi_{12} & \pi_{11} & \pi_{11} & 0 & 0 & 0 \\
\Delta_{yz} & 0 & 0 & 0 & \pi_{44} & 0 & 0 \\
\Delta_{zx} & 0 & 0 & 0 & \pi_{44} & 0 & 0 \\
\Delta_{xy} & 0 & 0 & 0 & 0 & \pi_{44} & 0
\end{bmatrix}
\begin{bmatrix}
\sigma_x \\
\sigma_y \\
\sigma_z \\
\tau_{xy} \\
\tau_{zx} \\
\tau_{yx}
\end{bmatrix}
$$

Under these conditions the fractional resistivity changes produced by the normal stress...
(\sigma) and shear stresses (\tau) are linked to \Delta by a series of piezo-resistive coefficients. The Subscripts of \Delta refer to directions of resistivity changes and current, for example, \Delta_{xy} is the stress induced resistivity change in the y direction due to current flow in the x direction. Therefore \Delta_{xy} is a result of a stress induced change in the y component of electric field due to the x component of current density. Symmetry of the silicon lattice results in the converse conditions, \Delta_{yx} = \Delta_{xy}, \Delta_{xx} = \Delta_{yy} and \Delta_{yx} = \Delta_{xy}. In IC resistors the current has to flow along the direction of the resistor and the electric field that determines the voltage drop across the resistor is parallel to the current flow. Therefore it is the fractional resistance changes \Delta_{xx} and \Delta_{yy} which affect the resistors parallel to the x and y directions. Resistivity changes can be related to resistance change if the resistor is sufficiently small so that the stress experienced is constant along its length.

In the PMOS3 test chip four resistors are combined to form a unit that allows the calculation of the components \sigma_x, \sigma_y and \tau_{xy} on the silicon plane at the point where the unit is located (\sigma_x, \sigma_y are the x-component and the y-component of shear stress and \tau_{xy} is the component of the stress normal to the plane of the die). Five of these sensor units are fabricated on the die and arranged as in Figure 3.

The package provided sufficient leads to implement four terminal measurement of strain gauge resistance. This eliminated measurement errors due to the resistance of the switch box contacts, leads and ZIF socket. The sense current had to be limited to < 1 mA as the resistors have very small dimensions and even a small current will cause heating. During the experiments 100 micro amp sense current was used throughout the course of the study.
As each of the five sensor units have their measurement arms R1, R2, R3, R4 aligned in the same direction with respect to the crystal lattice. The equations for the resistance of each of these four strain gauge sensor units are described by equations (5-4), (5-5), (5-6) and (5-7).

$$\frac{\Delta R_1}{R_1} = \frac{1}{2} \sigma_x (\Pi_{11} + \Pi_{12}) + \frac{1}{2} \sigma_y (\Pi_{11} + \Pi_{12}) + \Pi_{12} \sigma_z - \tau_{xy} (\Pi_{12} - \Pi_{11})$$ (5-4)

$$\frac{\Delta R_2}{R_2} = \frac{1}{2} \sigma_x (\Pi_{11} + \Pi_{12} - \Pi_{44}) + \frac{1}{2} \sigma_y (\Pi_{11} + \Pi_{12} + \Pi_{44}) + \Pi_{12} \sigma_z$$ (5-5)

$$\frac{\Delta R_3}{R_3} = \frac{1}{2} \sigma_x (\Pi_{11} + \Pi_{12}) + \frac{1}{2} \sigma_y (\Pi_{11} + \Pi_{12}) + \Pi_{12} \sigma_z + \tau_{xy} (\Pi_{12} - \Pi_{11})$$ (5-6)

$$\frac{\Delta R_4}{R_4} = \frac{1}{2} \sigma_x (\Pi_{11} + \Pi_{12} + \Pi_{44}) + \frac{1}{2} \sigma_y (\Pi_{11} + \Pi_{12} + \Pi_{44}) - \Pi_{12} \sigma_z$$ (5-7)
Where \( z \) is the stress component along the \( z \)-direction (perpendicular to the silicon plane). The Cramer determinant of a four equation system is zero so that it is impossible to solve in a closed form. If the approximation that \( \sigma_z \) is small in comparison to the other quantities \( \sigma_x, \sigma_y, \tau_{xy} \) is used then a solution is possible.

By subtracting equation (5-6) from (5-4) we obtain (5-8)

\[
\tau_{xy} = \frac{\Delta R_3 - \Delta R_1}{R_3} \frac{\Delta R_1}{R_1} \frac{2}{2(\Pi_{12} - \Pi_{11})}
\]

If \( \sigma_z = 0 \) then (5-5) combined with (5-7) gives (5-9) and (5-10).

\[
\sigma_x = \frac{1}{\Pi_{44}(\Pi_{11} + \Pi_{12})} \frac{\Delta R_4}{R_4} + \frac{1}{2(\Pi_{11} + \Pi_{12} - \Pi_{44})} \frac{\Delta R_2}{R_2}
\]

\[
\sigma_y = \frac{1}{\Pi_{44}(\Pi_{11} + \Pi_{12})} \frac{\Delta R_2}{R_2} + \frac{1}{2(\Pi_{11} + \Pi_{12} - \Pi_{44})} \frac{\Delta R_4}{R_4}
\]

The values of the piezo-resistive coefficients at 25° Celsius for p-type resistors with a dopant concentration of \( 10^{19}/\text{cm}^3 \) are;

\[
\pi_{11} = 4.62 \times 10^{-12} \text{ cm}^2/\text{dyne}
\]
\[
\pi_{12} = 0.77 \times 10^{-12} \text{ cm}^2/\text{dyne}
\]
\[
\pi_{44} = 96.67 \times 10^{-12} \text{ cm}^2/\text{dyne}
\]

as stated in the N.M.R.C. literature [7]. It would appear from the literature that piezo resistive measurements are quoted in the c.g.s units of dynes/cm probably as they are convenient and consistent with the size of stress gauges whose dimensions are typically a fraction of a centimetre. Therefore this convention has been adopted in

5-29
favour of S.I. units to facilitate comparison with other sources. The dependence of the piezo-resistive coefficients on temperature and on surface dopant concentration are known [8] and were reported as varying by approximately -5% at -50°C to +10% at 90°C when normalised to 0°C (for a doping concentration of $5 \times 10^{19}$/cm$^2$). Using the data in [7] a correction was made to allow for the thermal coefficient of resistivity when calculating thermally induced stress.

Substituting these values into the derived equations gives the following equations for the normal and shear stresses measured in dyne/cm$^2$.

$$\tau_{xy} = \frac{\Delta R_3 - \Delta R_1}{R_3 \cdot R_1 / -7.7} \times 10^6$$  \hspace{1cm} (5-11)

$$\sigma_x = \frac{51.03 \Delta R_4 - 45.64 \Delta R_2}{R_4 / R_2} \times \frac{521 \times 10^{-12}}{521 \times 10^{-12}}$$  \hspace{1cm} (5-12)

$$\sigma_y = \frac{51.03 \Delta R_3 - 45.64 \Delta R_1}{R_3 / R_1} \times \frac{521 \times 10^{-12}}{521 \times 10^{-12}}$$  \hspace{1cm} (5-13)

### 5.6.2 Measurement of Package Stress due to Ambient Temperature

The stress caused by the differential thermal expansion of the package materials comprising the test packages were measured for a sample of five packages. Initially two gauges were used, gauge 4 (centre of die) and gauge 5 (corner of die). The number of connections that could be made at the same time through the switching matrix with a single card was limited to twelve columns and eight rows, so that only two stress sensors could be used at any one time. The central sensor was chosen as one of these as it was located at or close to the centre of the die (neutral axis) and so would experience the minimum of stress. The corner sensor would experience the maximum stress (furthest from the neutral axis) and was chosen as the second sensor. The measured stresses (after temperature correction) for each package are shown in figures 17 to 21. All stress measurements were taken with respect to room
temperature, it is around this temperature that the compressive forces were observed to peak, demonstrating that the moulding compound had been carefully designed to exert maximum compression (and hence sealing) on the die at temperatures around storage and operating conditions (low dissipation). As can be seen the normal force is less than either component of the shear force and both the components of shear force are very similar in magnitude. The shear forces are as a result of the compressive force that the cured moulding compound exerts on the die and leadframe as it cools. At temperatures above room temperature the shear force at the die corner exceeds that at the centre of the die, whereas at temperatures below the peak compressive stress the shear stress at the die centre is greater than that at the die corner.

Figure 17 Package Related Stress - Package 1
Figure 18 Package Related Stress - Package 2

Figure 19 Package Related Stress - Package 3
Figure 20 Package Related Stress - Package 4

Figure 21 Package Related Stress - Package 5
These results show that the normal stress on the die is significantly less than the shear stress confirming the assumption made in solving the linear equations. The normal stress is on average approximately an order of magnitude less than the shear stress. The stresses in the x and y directions are in the majority of cases approximately equal. The magnitude of the shear stresses observed by the die stress gauges over the test range are shown in context against both commercial and military temperature ranges. Figure 22. The range of the compressive stress experienced by the die over the operating temperature ranges are tabulated in Table IV. In general the internal package stresses were on average 2.5 to 4.8 higher over the military temperature range than the commercial range.

Besides catastrophic failures due to thermally induced stress it is possible for such stresses to cause electrical changes in device parameters. It has already been shown that differential thermal stresses can cause variations in piezo-resistivity,
Table IV Average Shear Stress Measured over Commercial and Military Operating Temperature Ranges

<table>
<thead>
<tr>
<th>Operating Temperature Range</th>
<th>Maximum Shear Force (dynes/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial (0 - 70°C)</td>
<td>≈1.0</td>
</tr>
<tr>
<td>Military (-55 - 125°C)</td>
<td>≈10</td>
</tr>
</tbody>
</table>

5.7 Summary

A review of commercially available package test chips has shown that it was possible to obtain package performance monitoring chips that could be used to address the two main areas of concern over the suitability of plastic packaged devices in high reliability systems, moisture ingress and package stress. The device chosen for this study, the PMOS3 from N.M.R.C., was shown to be suitable to monitor these processes in high I/O count packages such as the QFP. It is believed that such in situ monitoring chips will prove to be an important tool in assessing the performance of new package styles especially when the effects of; increasing I/O count, thinner plastic, larger die areas and higher dissipation are being investigated.

It has been shown that package test chips equipped with suitable sensors can measure the package induced thermal stresses experienced by a semiconductor die encapsulated in plastic packages. This may prove to be a useful technique in determining the potential hazards of using certain package material combinations with different sizes of die. This could aid the assessment of the suitability of different package styles for different operating environments. It was shown that the thermally induced package stress was not sufficiently great so as to cause concern when the particular package investigated here was cycled over the military temperature range.

The monitor chips proved effective in determining the rate and effects of moisture ingress into plastic packages and showed that the onset of corrosion could be determined. Further investigation will be necessary to determine the activation...
energies for temperature and humidity dependence of the observed failure mechanisms by repeating these experiments over a range of temperature and humidity. This would then permit an acceleration formula to be chosen so that package performance could be assessed for a required operating environment.

5.8 References


CHAPTER 6

Mathematical Modelling

6.1 Introduction

In this chapter the physical processes involved in the degradation of plastic packages and of encapsulated devices are examined. From this a mathematical model is developed which it is suggested could describe the action of these mechanisms. The moisture absorption process observed in plastic packages is described as are some of the possible effects this has on the action of the transistor. A gain degradation mechanism is suggested to explain the degradation observed in planar transistors which have been exposed to HAST testing. The mechanism describes how the accumulation of surface charge can cause depletion in the region below the oxide surface and the effect this has on the Fermi level and the subsequent effectiveness of the traps in the surface depletion region as recombination centres.

A model is presented which it is suggested can explain the weight gain behaviour observed in Chapter 4 for packages exposed to high temperatures and humidity. The model is based on Fickian diffusion modified to allow for the possibility of path blocking.

A discussion on the internal package stresses measured in Chapter 5 is presented together with a simple 1 dimensional stress analysis model.

6.1.1 Analysis of the Gain Degradation in Bipolar Transistors

It has been observed that moisture ingress through plastic packages containing bipolar
transistors is accompanied by degradation of D.C. gain when the devices are biased at low levels of emitter current. It has been shown [2] that surface effects play an important part in the behaviour of transistor gain through the effect on surface and bulk recombination. Recombination of minority charge carriers in the emitter-base region gives rise to an excess base current which is observed as a decrease in gain. Surface and bulk analysis of the die has shown that penetrating moisture transports hydrated ionic species from the plastic to the die. When the concentration of these ions on the oxide layer increases it represents a build up of surface charge. This surface charge increases the effective area of the depletion region by causing depletion of the base region below the oxide providing an increased area in which surface recombination can occur. In addition the presence of the surface charge can raise the potential of the surface with respect to the Fermi level of the junction. Movement of the Fermi level with respect to the trap level affects the effectiveness of traps as recombination centres. It is this increase in depletion region area at the surface together with changes in Fermi level position that is believed to be responsible for gain degradation.

**Figure 1** Cross Section of Typical Integrated Circuit Transistor
The performance of a planar npn transistor is dependant on, amongst other things, the condition of its surface which can be considered as being in one of four states; flatband, base surface depletion, base inversion or emitter depletion and inversion.

**Flat band condition**

With no charge present on the oxide the potential of the Si-SiO₂ interface is the same as the adjacent bulk silicon. For a forward biased npn transistor the majority of the electrons injected into the junction from the emitter pass through the base to the collector. The remainder combine with holes in the depletion region either in the bulk or the surface where they contribute to the base current and lower the observed gain. In addition electron/hole recombination in the base region gives rise to excess base current. It is this condition that is assumed to have existed in the pre stress tested devices before HAST.

**Base Surface Depletion**

Considering the case of an npn transistor with net positive charge on or over the oxide layer. The presence of net positive charge over the surface can cause depletion of holes at the base surface by repelling them further into the base region. The same effect can be produced by the addition of a controlling gate electrode over the depletion region which is biased positive with respect to the base. Base surface depletion does not alter the level of injection of carriers into the base region so that collector current is not affected. As the positive surface potential repels holes away from the surface the carrier densities are altered with the effect that the Fermi level is brought closer to the trap energy level increasing the prospect of recombination. The most efficient traps are those with energies in the middle of the bandgap. The magnitude of the increase in base current for a given base emitter voltage will depend on the density of surface recombination centres. It is this increase in base current, without a corresponding change in collector current, that results in decreasing current gain.
**Base Surface Inversion**

The width of the surface depletion region increases with net positive surface charge up to a maximum value. Beyond this value additional charge causes the surface to invert and an n-type inversion layer is formed at the surface. The region between this n-type region and the underlying p-type bulk is known as the Field Induced Junction F.I.J. to distinguish it from the intended base-emitter junction. The inversion layer may be considered as an extension of the emitter as it is connected by an Ohmic junction to the diffused inversion layer. Therefore electron injection into the base can occur from the diffused emitter and from the inversion layer. As a consequence there will be a base current component associated with the recombination of carriers in the field induced junction. The diffusion current density underneath the field induced junction, for a given forward bias, is determined by the doping concentration, the base width, and the carrier lifetime in this region. The total excess current as a result of surface inversion depends on the inversion area and the density of the diffusion current and recombination centres.

**Emitter Surface Depletion and Inversion**

When net negative charge accumulates on the oxide holes are attracted towards it narrowing the depletion region width and effectively increasing the p-type doping density. Depletion region width continues to decreases with increasing net negative surface charge (and effectively increased base doping) until its width becomes small enough so that the electric field is high enough (10^6 V/cm), and the transition region narrow enough (10um), to allow tunnelling. Tunnelling of electrons can occur either across the field induced junction from the conduction band in the emitter to the valence band of the base or via traps situated around the middle of the bandgap with subsequent recombination and gain degradation. It could be expected that emitter depletion, through the accumulation of negative surface charge would, be far less likely than depletion of the base region due to accumulation of positive charge owing to the far higher doping density in the emitter (≈10^{20} atoms cm^{-1}).

The oxide charge that accumulates as a result of moisture ingress could be comprised of either net positive or net negative charge depending on the ionic species present in
the plastic moulding compound and the polarity of the bias applied during HAST testing. The presence of both negative and positive ions were observed by surface analysis of the oxide surface of transistors removed from HAST. The base region however was biased very slightly negative during these tests promoting the accumulation of positive charge in this region. In addition it is believed that the relative doping densities of the base and emitter regions would favour base depletion and inversion in the presence of positive surface charge (rather than emitter depletion due to negative oxide charge). Therefore it is believed that the observed gain degradation was most likely a result of the accumulation of positive surface charge. The basic structure of an integrated transistor of the type used in this study is shown in Figure 1.

The relationship between gain and surface charge accumulation may be derived. D.C gain $\beta$ may be expressed in terms of emitter efficiency $\gamma$ and the base transport factor $\alpha_T$ as in equation (6-1). The base transport factor is dependant on the bulk properties of the base and losses which occur as a result of the recombination of minority charge carriers in the bulk. An effect which, it is assumed, is not greatly influenced by surface conditions. The degradation of $\beta$, due to increases in base current, is usually dominated by changes in emitter efficiency $\gamma$ and in particular the increase in the density of recombination centres. For these reasons a typical value for base transport factor of 0.995 was used which was assumed to remain constant throughout the duration of the HAST experiment. The presence of recombination centres gives rise to a recombination current that effects the emitter efficiency as in equation (6-2).

\[ \beta = \frac{\gamma \alpha_T}{1 - \gamma \alpha_T} \]  

(6-1)

\[ \gamma = \frac{I_E}{I_E + I_R + I_{rec}} \]  

(6-2)
Here $I_B$ is the diffusion current in the base, $I_E$ is the diffusion current in the emitter and $I_{rec}$ is the sum of both bulk and surface recombination currents. The emitter diffusion current (6-3) and the base diffusion current (6-4) are derived by manipulating the expressions in [1].

$$I_E = A_j \frac{qD_n n i^2}{N_{AB} W_B} \exp\left(\frac{qV_{EB}}{kT}\right)$$

(6-3)

$$I_B = A_j \frac{qD_p p i^2}{N_{DE} W_E} \exp\left(\frac{qV_{EB}}{kT}\right)$$

(6-4)

Typical values for this type of epitaxial transistor are believed to be: $D_{ab} = 35 \text{cm}^2 \text{sec}^{-1}$, $D_{pb} = 12 \text{cm}^2 \text{sec}^{-1}$, $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$, $N_p = 5 \times 10^{18} \text{ cm}^{-3}$, $N_A = 5 \times 10^{15} \text{ cm}^{-3}$, $W_B = 2 \times 10^{-4}$ cm, $W_E = 4 \times 10^{-4}$ cm, and $A_j = 2.5 \times 10^{-6} \text{cm}^2$. Typical emitter and base diffusion currents were plotted below as a function of $V_{BE}$.

![Figure 2 Emitter Diffusion Current as a function of Base Emitter voltage](image)

Figure 2 Emitter Diffusion Current as a function of Base Emitter voltage
When forward biased the base-emitter junction of a bipolar transistor is subject to recombination currents in its depletion and base regions. This can be observed as having a measurable effect on current gain particularly at low levels of $I_e$. For indirect bandgap semiconductors, such as silicon, the recombination process is via localised energy states between the conduction and valence bands. Recombination can occur in the bulk of the material due to the presence of impurities such as gold or at the surface of the semiconductor due the presence of recombination centres resulting from discontinuities in the crystal structure such as dangling bonds as well as the presence of surface contamination.

Expressions for the recombination currents, in terms of recombination centre (trap) density, can be derived from [1] by substituting an expression that links carrier life time to recombination centre density in the particular region of interest, as has been shown in [2]. The bulk recombination current $I_{\text{rec bulk}}$ is given by equation (6-5), where $\tau_0$ is the recombination time in the emitter-base depletion region.

$$I_{\text{rec bulk}} = \frac{1}{2} q \frac{\eta}{\tau_0} W_{EB} \exp\left(\frac{qV_{BE}}{2kT}\right) A_j$$  \hspace{1cm} (6-5)

The width of the base emitter $W_{EB}$ region is a function of applied bias voltage $V_{BE}$ and the built in potential of the junction, equation (6-6) from [2].
Where the built in voltage is given by equation (6-7) from [2].

\[ V_{bi} = B \ln\left(\frac{N_A N_D}{n_i^2}\right) \quad (6-7) \]

From this the bulk recombination current can be obtained as a function of \( V_{BE} \) as shown in Figure 4.

In addition to the bulk recombination current an expression for the net surface recombination current density \( U_s \) can be derived from the expression for surface recombination (6-8) as has been shown in [2].

\[ U_s = \frac{-N_{st} \sigma_p \nu_{th}(p_x p_s - n_i^2)}{\sigma_p[p_n + n_i \exp\left(\frac{E_i - E_F}{kT}\right)] + \sigma_n[n_n + n_i \exp\left(\frac{E_i - E_F}{kT}\right)]} \quad (6-8) \]

Where \( n_i \) and \( p_s \) are the surface electron and hole densities which can be obtained from the equilibrium densities \( n \) and \( p \) in the bulk material (6-8). Where \( \phi_s \) is the surface potential, \( E_F \) is the Fermi level and \( E_i \) is the intrinsic Fermi level. Which are related to the equilibrium densities \( n_0 \) and \( p_0 \) by equations (6-11) and (6-12).
It is therefore possible to derive an expression for surface recombination current density that is a function of the changing Fermi level which occurs due to the presence of a surface potential. From equations (6-6), (6-8) and (6-15) it is possible to obtain an expression for $I_{\text{rec surf}}$. Where $A_s$ is the area of the depletion region exposed to the surface, The relationship between surface recombination current density and the difference in trap and Fermi levels is shown in Figure 5.

$$I_{\text{rec surf}} = -qU_s A_s$$  \hspace{1cm} (6-15)
The effects of the surface recombination current can now be included. Figure 5 shows the effect on gain degradation of the Fermi level moving towards the recombination centres at the centre of the bandgap. If the Fermi level was pulled from 0.21eV towards the centre of the bandgap at 0.56eV, where the most efficient traps lie, and the area of the depletion region exposed to the surface was assumed to double with charge accumulation then the gain degradation that would be produced would approximately model that observed in the HAST experiments. Figure 7 shows the modelled gain degradation with the y axis displaying relative gain degradation for five decades of base current against the difference in Fermi and trap levels on the x axis (j is a index value used to generate a range of increasing Is values with time). If degradation is then plotted against $\exp(j)$ the modelled gain degradation curves closely resemble the observed degradation. Suggesting an exponential relationship between changing Fermi level position due to surface charge accumulation and time. The results can be seen to model the observed gain degradation during the HAST studies Figure 8.

![Graph showing degradation of relative gain as a function of the difference between the induced Fermi energy level $EF$ and the recombination centre energy level $Et$ (eV)](image)

**Figure 6** Degradation of relative gain as a function of the difference between the induced Fermi energy level $EF$ and the recombination centre energy level $Et$ (eV)
Figure 7 Modelled gain degradation including the effects of bulk and surface recombination currents

Figure 8 Observed Gain Degradation against HAST exposure time
The value of the Fermi level in the unstressed pn junction is dependant on the doping concentration of the base region as is given in equation (6-16) and is calculated to be 0.23eV.

\[
\Phi_i = E_i - kT \ln(N_A / n_i)
\]  

(6-16)

The amount of surface charge required to induce a given change in Fermi level can be calculated. The voltage required is known and the system is considered to be analogous to a capacitor with the silicon dioxide passivation layer as the dielectric of thickness \( y_{ox} \) with a surface potential \( E_s \) across the plates. Where the potential \( E_s \) is produced by charge \( Q_{ox} \). The capacitance per unit area is given by (6-18) and the charge by (6-18);

\[
C = \frac{\varepsilon_0 \varepsilon_{ox}}{y_{ox}}
\]

(6-18)

\[
V_G = \frac{Q_{ox} y_{ox}}{\varepsilon_0 \varepsilon_{ox}}
\]

(6-17)

For an oxide thickness of 1 micron and an oxide voltage due to surface charge accumulation of 0.5 Volts which produces a change in the Fermi level of 0.17eV from its intrinsic value to a recombination centre level of 0.56eV at the centre of the bandgap would require a charge concentration of 1.7x10^{-9} Coulombs per square cm. This would be equivalent to 1.1x10^{10} impurity atoms per square cm. If the number of atoms in one square cm of silicon dioxide is approximately 1.4x10^{15} then this represents a surface contamination level of approximately 8 p.p.m.

If it is assumed that this level of contamination is transported by the ingresson of moisture as a solvent front then it could be expected to obey the relation suggested by Fickian diffusion between the mass of diffused matter and time. (6-19). Dividing through by mass provides an expression for the number of ionised atoms (assumed monovalent) that have diffused through to the die in a given time \( t \). This represents
the charge present on the die after time $t$.

$$M(t) = AmC_0 2\sqrt{\frac{Dt}{\pi}}$$ (6-19)

This charge then induces a voltage on the oxide surface with respect to the semiconductor given by (6-18). This surface charge together with the applied base emitter voltage $V_{BE}$ changes the position of the Fermi level. The resulting change in surface recombination current can be inferred from (6-8) and (6-15). A relationship between the square root of diffusion time and gain degradation maybe postulated. Inferring the diffusion constant from the available data allowed a graph of gain degradation against time to be plotted, Figure 8. Comparison with the observed degradation showed similar behaviour despite the assumptions necessary in its derivation.
The maximum gain degradation that could occur due to this mechanism is limited by the maximum surface current that can flow before the onset of inversion. The maximum value of surface current can be derived by substituting expressions for the potential levels in the bandgap and using \( C_n \) and \( C_p \) the electron and hole capture rates defined as:

\[
C_n = v_{th} \sigma_n \tag{6-20}
\]

\[
C_p = v_{th} \sigma_p \tag{6-21}
\]

Where \( v_{th} \) is the surface recombination velocity (the effective mean velocity for recombination of charge carriers in a direction normal to the surface) and \( \sigma_n, \sigma_p \) are the capture cross sections for electrons and holes respectively.

\[
I_{recsurf} = \frac{0.5 qn_iN_F \sqrt{C_n C_p}}{\cosh(\beta(\phi_s - \phi_F - \phi_0)) + \exp(\beta(V_{BE}/2)) \cosh(\beta(\phi_s - \phi_F - \phi_0 + V_{BE}/2))} \exp((\beta V_{BE} - 1))
\]

(6-22)

Examination of (6-15) shows that the value of surface current reaches a maximum when:

\[
\phi_s - \phi_F - \phi_0 + \frac{V_{BE}}{2} = 0 \tag{6-23}
\]

So that the maximum value of surface recombination current that can occur due to an accumulation of surface charge for a given extended depletion region area \( A_s \) is given by (6-22).

\[
C_n = v_{th} \sigma_n \tag{6-24}
\]
\[ I_{\text{max}} = \frac{0.5 q n N_{\text{ox}} A_x \sqrt{C_x C_p} \exp(\beta (V_{BE} - 1))}{\cosh(\beta (\phi_x - \phi_y - \phi_0)) + \exp(\beta V_{BE}/2)} \]  \hspace{1cm} (6-25)

It has been shown in [2] that the width of the extended depletion region exposed to the surface \( x_d \), can be derived by solving the Poisson equations which describe the potential that exists between the silicon and oxide. Where \( \delta y \) is an incremental distance into the oxide layer. Insertion of the boundary conditions (potential in the silicon is zero at \( x=0 \phi=0 \)), the potentials that exist at the interface \( (x=x_d) \) are equal \( \phi(x=x_d)=\psi_0 \), the electric displacement is equal to the charge densities per unit area \( Q_{ox} \), and the potential is equal to the applied oxide voltage) and integration yields an expression for the surface potential, due to charge accumulation, in terms of the width of the extended depletion region \( x_d \) [2].

\[ C_p = n_m \sigma_p \]  \hspace{1cm} (6-26)

\[ \frac{d^2 \phi}{dy^2} = \frac{Q_{ox}}{\epsilon_{ox} \delta y} \]  \hspace{1cm} (6-27)

\[ \frac{d^2 \phi}{dx^2} = \frac{q N_A}{\epsilon_s} \]  \hspace{1cm} (6-28)

\[ \phi = V_G - \phi_{MS} \]  \hspace{1cm} (6-29)

\[ V_G - \phi_{MS} = -\left( \frac{Q_{ox}}{\epsilon_{ox}} - \frac{q N_A x_d}{\epsilon_{ox}} \right) y_{ox} + \left( \frac{q N_A}{2 \epsilon_s} x_d^2 \right) \]  \hspace{1cm} (6-30)
If the potential on the oxide is considered to be analogous to a gate electrode with potential \( V_G \) applied then rearranging equation (6-29) produces an expression for \( \phi \) in terms of \( x_{ds} \). If the oxide is considered as a capacitor with the distance between its plates equal to the oxide thickness \( Y_{ox} \) the charge \( Q_{ox} \) produces a voltage \( V_G \) where the capacitance per unit area is:

\[
\phi = \frac{qN_A x_{ds}^2}{2 \varepsilon_s} \tag{6-31}
\]

\[
C = \frac{\varepsilon_0 \varepsilon_{ox}}{d} \tag{6-32}
\]

\[
V_G = \frac{Q_{ox} Y_{ox}}{\varepsilon_0 \varepsilon_{ox}} \tag{6-33}
\]

Where \( \phi_{MS} \) is the difference in work function between the metal and semiconductor if the charge were present on a gate electrode rather than over the oxide, hence in this system \( \phi_{MS} = 0 \). Substituting for \( V_G \) into (6-29), the expression for extended depletion region at the surface, yields an expression in terms of surface charge density \( Q_{ox} \). A fuller derivation may be found in Appendix 1 of [1].

\[
x_{ds} = -\frac{\varepsilon_s Y_{ox}}{\varepsilon_{ox}} + \frac{1}{\varepsilon_{ox}} \left( \frac{\varepsilon_{ox} Y_{ox}^2}{qN_A} \right)^2 + 2 \frac{\varepsilon_s}{qN_A} (V_G - \phi_{MS}) + \frac{\varepsilon_{ox} Y_{ox} Q_{ox}}{qN_A} \tag{6-34}
\]

\[
x_{ds} = -\frac{\varepsilon_s Y_{ox}}{\varepsilon_{ox}} + \frac{1}{\varepsilon_{ox}} \left( \frac{\varepsilon_{ox} Y_{ox}^2}{qN_A} \right)^2 + Q_{ox} \frac{2 \varepsilon_s Y_{ox}}{qN_A \varepsilon_{ox}} \left( \frac{1}{\varepsilon_0} + \frac{\varepsilon_s}{qN_A \varepsilon_{ox}} \right) \tag{6-35}
\]

This shows how the depletion region width below the oxide surface increases with increasing surface charge density \( Q_{ox} \) (6-34). If, as assumed, this surface charge is due to mono-valent ions (which were observed by surface analysis to predominate) then the dependence of \( x_{ds} \) on \( Q_{ox} \) is as shown in Figure 9.
Figure 9 Extended Surface Depletion Region Width against Surface Charge Concentration.

It has been shown [2] that the extended depletion layer width $x_{ds}$ depends on the amount of surface charge present up to a maximum value, which occurs just prior to inversion of the surface. Inversion occurs when the accumulation of carriers at the surface is equal in concentration and opposite in polarity to the net doping density of the semiconductor (6-35).

$$\phi_s = 2\phi_F \frac{2kT}{q} \ln(N_A/n_i) \quad (6-36)$$

Substitution into (6-29) produces an expression for the maximum value of depletion layer width that can exist before inversion takes place (6-36).
\[ x_{dr\ max} = \sqrt{\frac{4\epsilon \kappa T}{q^2 N_A} \ln \left( \frac{N_A}{n_i} \right)} \]  

(6-37)

Substituting this expression for maximum depletion layer width into (6-34) and solving for Q yields an expression for the corresponding surface density that would cause depletion to occur (6-36).
6.1.2 Consideration of Experimental Results

The observed average gain degradation in the devices subjected to accelerated life testing under HAST is shown in Figure 9. The average value of DC gain at low bias levels (0.1\textmu{}A) was observed to have degraded from an initial value of approximately 50 to approximately 40 after 500 hours of accelerated life testing.

Considering the un-degraded case where gain =50 and substituting the calculated values for $I_E$ and $I_B$ into the expression for emitter efficiency yields a value for the total recombination current (bulk and surface) of 1.244nA. Inserting typical values into the parameters for the bulk recombination current expression gives 1.235nA which suggests that the surface recombination current in the transistors prior to accelerated life testing is 8.8pA. Substituting this value into the expression for surface recombination current yields a value for the area of the depletion region exposed to the surface prior to HAST of $62\times10^{-6}$ cm$^2$.

The average value of DC current gain after a period of 500 hours of accelerated life testing is 40 which suggests that the corresponding value of surface recombination current had increased to 0.443nA. Taking a value for surface potential that is at or close to the value that corresponds to the level where trap capturing efficiency is at a maximum (around the middle of the band gap) and substituting it into (6-15) provides a value for the smallest effective area of surface charge that could produce this level of gain degradation.

The structure of a planar transistor showing the extended depletion region at the surface and the accumulation of surface charge due to the build up of ionic contamination is shown in Figure 10. In the case of gate electrode over the base surface the depletion region at the surface extends the length of the electrode. It is assumed that in the presence of surface charge the extended region exists over the base surface. If the surface depletion region
extends for a length greater than the diffusion length then non uniform recombination will occur along its length. In this case the extended surface depletion region is described in terms of effective area $A'$. This complicates the analysis and makes the calculation of the actual charge at the surface difficult. It may be inferred that $Q_{ox}$ has not reached a level where the surface potential it would set up is great enough to cause inversion as no clear increase in gain was observed that could be attributed to the formation of a field induced junction extending the effective emitter area.

In order to confirm and quantify the presence of low levels of contamination surface analysis techniques such as laser ionisation mass analysis (L.I.M.A) and secondary ionisation mass spectroscopy (S.I.M.S.) could have been employed. This would have required a means of removing the plastic encapsulation without further contaminating the oxide surface. The jet etch technique available was unsuitable for this purpose as it brings hot acid into contact with the oxide surface. The standard technique employed for encapsulant removal prior to chemical analysis is plasma ashing. Unfortunately no plasma ashing facility was available within the university and no external facility could be found. Hence it was not possible to directly confirm the actual level of impurity ions on the oxide surface that was predicted by the gain degradation model.
The measurement of gain reduction is a sensitive method of determining the presence of moisture at the die. It is probably also a more meaningful parameter than observing catastrophic device failures (e.g. corrosion) in determining operational life times. It can provide an indication that very small quantities of moisture have breached the package and have reached the die surface. This process can proceed the onset of corrosion by several hundreds of hours under HAST conditions. It has been shown to be a more sensitive method in detecting moisture penetration of the package through to the die than measuring the leakage currents between triple track meander patterns. It is therefore believed possible that it could provide a much quicker and more sensitive method of assessing package reliability offering reduced accelerated life testing times.

6.1.3 Model Constraints

The simple model suggested here for gain degradation models the effects of the Sah-Noyce-Shockley recombination current. It is only intended to model gain degradation at low levels of collector current and does not operate in the high injection condition. The model can be further extended to take into account the effects of bandgap narrowing. In heavily doped regions, such as the emitter, band gap narrowing occurs due to the stored electrostatic energy of majority-minority pairs [3]. This paper states that at room temperature bandgap narrowing follows the relationship shown in equation (6-37). Where the emitter doping density \( N_E \) is in \( \text{cm}^{-3} \).

\[
\Delta E_G = 22.5 \sqrt{\frac{N_E}{10^{18}}} \text{ meV} \tag{6-38}
\]

The intrinsic carrier density in the emitter then becomes;

\[
n_{ie}^2 = n_i^2 \exp\left(\frac{\Delta E_g}{kT}\right) \tag{6-39}
\]

The effect of this narrowing of the band gap is to further reduce gain.

The only other reference to a gain reduction mechanism for bipolar transistors that could be found in a literature survey conducted on recent publications (1990-95) was attributed to hot carriers processes such as hot-electron and hole trapping, [4][5].
degradation process results from the interaction of hot carriers generated from band to band tunnelling at the base emitter junction which are subsequently "heated" (accelerated) by the junction electric field. This causes base oxide damage due to the generation of interface traps. This cause of degradation was discounted as an explanation of the gain degradation observed in these experiments as it requires high base-emitter reverse bias potentials, that are below but near the Zener voltage, and far higher stress temperatures (150-200°C) than were employed. If this gain degradation process had been present in this series of experiments then it would have been observed in the results of the high temperature and biased stress tests. Significant gain degradation was only observed in those tests where high levels of humidity were employed regardless of whether the packaging was plastic or ceramic.

6.2 Moisture Ingress Models
To assess the extent to which moisture absorption occurs in plastic packages a series of experiments were conducted where weight gain against exposure time was observed during HAST testing. There are believed to be two possible moisture ingress mechanisms for plastic packages; bulk absorption and ingress along the leadframe/package interface.

6.2.1 Fickian Bulk Absorption Model
To investigate the bulk absorption behaviour a Fickian model was first assumed. If the package is at thermal equilibrium at ambient temperature $T$, where $k$ is Boltzmann's constant, then the moisture diffusion constant $D(T)$ is given by (6-39).

$$D(T) = D_0 \exp\left(-\frac{E_A}{kT}\right) \quad (6-40)$$

Where $E_A$ is the activation energy for moisture diffusion and $D_0$ is a characteristic constant. Provided that the vapour pressure/humidity at the surface is constant and the moisture does not diffuse through to the leadframe (so that the sample is effectively infinite) the situation can be described by the mathematics of "constant source" diffusion.
Figure 11 Average Percentage Weight Gain for Plastic Packages versus the Square Root of Exposure Time.
The moisture concentration $C(x,t)$ is described by the governing diffusion equation (6-40),

$$\frac{\partial C}{\partial t} = D(T) \frac{\partial^2 C}{\partial x^2}$$

with boundary and initial conditions;

$$C(x=0, t) = C_0 \quad C(X-\infty, t) = 0 \quad C(x, t=0) = 0 \quad (6-42)$$

In this case the moisture distribution at time $t$ is given by (6-42)

$$C(x, t) = C_0 \text{erfc} \left( \frac{x}{2\sqrt{Dt}} \right) \quad (6-43)$$

where erfc is the complementary error function. This will lead to a weight gain at time $t$ of;

$$M(t) = Am \int_{0}^{\infty} C(x, t) \, dx \quad (6-44)$$

Where $m$ is the weight of a single molecule, and $A$ is the area of the plastic surface. Substituting for $C$ yields (6-44);

$$M(t) = Am C_0^2 \frac{\sqrt{Dt}}{\pi} \quad (6-45)$$

Thus the weight gain could be expected to increase with time as $t^{3/2}$, with temperature $T$ as $D^{1/2}$ or $\exp(-E_A/2kT)$ and with vapour pressure as $C_0$. If the initial weight is $M_0$, the relative weight gain is $M(t)/M_0$. To examine the dependence of weight gain on exposure time all the samples were normalised to $t=0$ and the percentage mean weight gain was plotted against the square root of time, Figure 11. Table I shows the results of linear regression analysis for both logarithmic and square root of time models.

The weight gain behaviour shown in Figure 11 displays an initial linear relationship between weight gain and root time. The graphs are believed to depart from this.
behaviour as time increases and the package begins to saturate. This is believed to be due to the decreasing available volume into which moisture may diffuse as the diffusion channels become blocked. This behaviour can be modelled as; a reduction

<table>
<thead>
<tr>
<th>Relationship</th>
<th>Parameter</th>
<th>130°C</th>
<th>120°C</th>
<th>110°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>f(\sqrt{t})</td>
<td>c</td>
<td>0.06</td>
<td>0.06</td>
<td>0.05</td>
</tr>
<tr>
<td></td>
<td>(R^2)</td>
<td>0.86</td>
<td>0.92</td>
<td>0.76</td>
</tr>
<tr>
<td></td>
<td>m</td>
<td>0.03</td>
<td>0.02</td>
<td>0.01</td>
</tr>
<tr>
<td>f(log t)</td>
<td>c</td>
<td>0.09</td>
<td>0.08</td>
<td>0.06</td>
</tr>
<tr>
<td></td>
<td>(R^2)</td>
<td>0.57</td>
<td>0.73</td>
<td>0.37</td>
</tr>
<tr>
<td></td>
<td>m</td>
<td>0.10</td>
<td>0.09</td>
<td>0.02</td>
</tr>
</tbody>
</table>

in the surface area \(A(t)\) through which diffusion can occur, or as a time decreasing available volume per unit surface area \(V(t)\), or a time decreasing diffusion constant \(D(t)\) encompassing both surface and bulk effects. For the purposes of this study it is convenient to consider the process as a surface effect with an available surface area decreasing with time.

Rearranging the diffusion equation (6-44) in terms of \(M(t)/\sqrt{t}\) provides an expression for the available area for diffusion. Plotting relative weight gain over the square root of exposure time against time shows the decrease in area available for diffusion (6-45).

\[
A(t) = \frac{M}{\sqrt{t}} \frac{1}{2mC_0} \sqrt{\frac{\pi}{D}} \quad (6-46)
\]

Therefore it is suggested that the mechanism by which the plastic moulding compound absorbs moisture can be described by Fickian diffusion if allowance is made for path blocking. Figure 12 shows the behaviour of relative weight gain against the square
Figure 12 Weight Gain against the square root of Exposure Time

root of exposure time. Linear regression was used to produce the best straight line fit (dashed lines) which shows good agreement with the model. All three regression fitted lines have very similar gradients suggesting that the rate at which available diffusion paths are blocked is largely independent of temperature for the temperatures used in this study. The regression data is shown in Table II.

Table II Linear Regression data for Weight Gain versus root time

<table>
<thead>
<tr>
<th>Parameter</th>
<th>110°C</th>
<th>120°C</th>
<th>130°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>c</td>
<td>0.029</td>
<td>0.049</td>
<td>0.051</td>
</tr>
<tr>
<td>R²</td>
<td>0.90</td>
<td>0.92</td>
<td>0.95</td>
</tr>
<tr>
<td>m</td>
<td>-0.002</td>
<td>-0.002</td>
<td>-0.0017</td>
</tr>
</tbody>
</table>

6.2.2 Percolation Model

The weight gain studies suggest that moisture absorption cannot be described by a
simple Fickian diffusion process without allowance being made for path blocking effects. Considering the structure of the material an interesting alternative to Fickian diffusion would be to consider the problem in terms of a percolation model. This could prove to be an interesting alternative method of analysis.

Percolation differs from the simple diffusion transport mechanism in that a stochastic scattering or relaxation mechanism exists. In percolation processes, such as the mechanism considered here, there is a distinction between the fluid or gas particles and the scattering medium. The properties of the medium, although varying in some form from point to point are constant with time so that the random scattering of particles must be treated as a property of the medium.

If the filler-loaded epoxy moulding compound is considered to be a simple lattice of sites in two dimensions interconnected by potential transport paths (bonds) then this two dimensional structure may be considered to be one of four models; hexagon, triangular, square and Kagome and the percolation process can be described in one of two ways; a bond percolation model or a site percolation model. The bond percolation model is more appropriate to the modelling of the flow of a fluid through a porous material and is assumed here.

Movement of fluid molecules through the medium is by a series of n-step walks along the bond between sites to one of its nearest neighbours. A walk is said to be self-avoiding if it visits no atoms more than once. A set of unblocked atoms linked to one another through unblocked bonds is called a "cluster".

The fluid can become contained in clusters where no connecting bonds are present so that no further onward walks are possible. The probability that a single fluid molecule will wet infinitely many sites is called the percolation probability.

\[ P(p) = \lim_{N \to \infty} P_N(p) \]  

If this percolation probability is less than the critical percolation then the fluid spreads
only locally. If all clusters of "wet" atoms are of finite size the fluid is contained in localized regions. Under these conditions some weight gain would be observed but would be limited to a certain value once all available sites are filled and further onward transport is no longer possible. If however the percolation probability is greater than critical percolation probability then a cluster of infinite size is formed and a percolation channel exists with the fluid spreading through the medium. The critical probability depends on the topology of the lattice and on the type of percolation, bond or site percolation process. The values of critical probabilities can be obtained by Monte Carlo simulation or by series expansions [6].

Observing the loaded epoxy moulding compound under the electron microscope it has the structure shown in Chapter 4 Figure 24. The moulding compound is heavily loaded with filler particles (~70%) under the compressive moulding force (approximately one ton). These particles are forced to arrange themselves into a close packed roughly tessellating structure to minimise the volume they occupy. Of the four possible models the two dimensional hexagon lattice seems to be the closest approximation to the structure observed under the electron microscope and was therefore assumed to be the most appropriate model for this problem. This is valid as N is large because the filler particle size (10μm) is very much less than the moulding compound thickness (1.5mm).

The percolation process proceeds as the atoms try to pass along N individual bonds through the material. For an atom to be able to pass along the bond and "wet" the site at the other end depends on the energy of the atom and the "impedance" of the bond path.

The energies of the fluid atoms depends on their temperature and are given by the Maxwell-Boltzmann distribution (6-47).
The energy required to pass along the bond is also expected to have a distribution of energies which may, for example, be described by the normal distribution shown in (6-48). Where \( P(B) \) represents the probability of a given bond energy. Unfortunately it has not been possible, so far, to infer the parameters of this distribution from experiment so that this approach, although promising, could not be employed in this case. It is believed this could form part of a future study. The probability that a given molecule has sufficient energy to percolate onwards would depend on the area of overlap between the distribution of energies of the moisture molecules \( P(E) \) and the distribution of bond energies \( P(B) \) being greater than the percolation probability.

\[
P(E) = \int_0^{E_1} \frac{2}{\sqrt{\pi}} \left( \frac{1}{kT} \right)^{\frac{3}{2}} E^\frac{1}{2} \exp\left(-\frac{E}{kT}\right) dE
\]

(6-48)

The effect of increasing saturated vapour pressure/relative humidity has the effect of increasing the number of pores that are accessible to moisture and so increase the saturated weight gain. Increasing the temperature increases the kinetic energy of the water molecules in the atmosphere and so increases the likelihood of them attaining a given percolation probability and travelling further into the plastic.

\[
P(B) = \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{1}{2B^2}\right)
\]

(6-49)

6.2.3 Relationship of Weight Gain with Humidity

In section 6.2.1 the moisture absorption properties of the material were considered over time with temperature for constant relative humidity. It has long been believed that in THB accelerated life testing the effects of moisture are dependent on the relative humidity of the test atmosphere. This model is a result of work conducted in the late 1960's on the changes in electrical resistance of adsorbed moisture films on
un-encapsulated test patterns and from catastrophic corrosion failures of encapsulated aluminium interdigitated test structures. In these tests the time taken for moisture to breach the package was very small compared to the time for the corrosion process to produce catastrophic failure. When the failure mechanism is one of parameter degradation the degradation could occur at a similar rate to, and accompany, moisture ingress. The idea that the failure mechanism is dependent on the relative humidity of the atmosphere does not take into account the behaviour of the atmospheric moisture as a function of temperature. Two cases are considered.

**Constant Temperature, Different Relative Humidities**

When conducting a series of accelerated life tests over a range of relative humidities at constant temperature the acceleration observed between tests could be expected to have a linear relationship with relative humidity. Relative humidity is the percentage of the vapour pressure of water $\rho$ in the atmosphere relative to the saturated vapour pressure of water $\rho_o$ at a given temperature (6-49). It was used in this study, in common with most others, as a measure of humidity so as to be consistent with the majority of research.

$$RH\% = 100 \frac{\rho}{\rho_o} \quad (6-50)$$

The absolute humidity $d$, or mass of water vapour per unit volume of air, is a function of the vapour pressure of water at a given temperature as given by equation (6-50).

$$d = 0.00217 \frac{\rho}{T} \quad (6-51)$$

Where absolute humidity is in Kg/m$^3$, $\rho$ is the vapour pressure of water, and $T$ is absolute temperature. This is satisfactory provided temperature remains constant. If however the temperature is changed while relative humidity is kept constant, the absolute humidity, and hence the amount of water vapour available for absorption, alters as the saturated vapour pressure of air $\rho_o$. This behaviour was observed in the linear relationship displayed by the graph of the weight gain versus relative humidity
in Figure 13 and Figure 10 of chapter 4. Applying linear regression to these data confirmed a linear relationship with $R^2 = 0.972$, a gradient of 0.0193 and an intercept of 0.0075.

When the number of water molecules impinging on the package is in equilibrium with the number escaping from its surface by evaporation the weight the package will have reached its saturated weight. The number of water molecules impinging on the package surface is dependent on the quantity present in the atmosphere which is described by the absolute humidity. If the temperature remains constant then there exists a linear relationship between relative humidity and saturated weight. This was observed in the experimental data and is shown in chapter 4. However the time to saturation increases with decreasing humidity and lower saturation times had to be obtained by extrapolation. Consequently the results were subject to a degree of experimental error with an inherently worse linear regression statistics $R^2$ of 0.964 for gradient of 0.075 and an intercept of 0.083.
Behaviour at Non-Constant Temperature and Constant RH

If the temperature is not constant then different behaviour exists. The absorption of a gas, such as water vapour, into a porous solid such as a plastic moulding compound might be expected to depend on the energy of the incident gas molecules and the number of collisions per unit area per unit time.

The energy of the incident gas molecules is dependant on their temperature and is described by the Maxwell-Boltzmann distribution. The r.m.s. velocity is given in equation (6-51) from [6].

\[ \bar{u} = \sqrt{\frac{8kT}{\pi m}} \]  

(6-52)

The number of molecules impinging on unit area in unit time is given by equation (6-52) from [6],

\[ I_n = \frac{1}{4} n \bar{u} \]  

(6-53)

where \( n \) is the total number of atoms per unit volume of the gas, \( m \) is the mass of a water vapour molecule and \( d \) is the mass of vapour per unit volume, i.e.

\[ n = \frac{d}{m} \]  

(6-54)

\[ d = 0.00217 \left( \frac{RH}{100} \right) \rho_o \frac{T}{T} \]  

(6-55)

Combining equations (6-51) and (6-52) yields equation (6-54) for absolute humidity.

The weight gain could be expected to depend on the number of water vapour molecules incident on unit surface area in unit time, and their energy (6-55).
Therefore the weight gain would be proportional to both the relative humidity and the square of temperature. It will also depend on the saturated vapour pressure of water vapour $P_o$ which exhibits only a slight dependence on temperature over this range (6-55) Hence an expression for weight gain in terms of temperature at constant relative humidity would be of the form (6-56) where $k$ is a constant of proportionality found by experiment.

\[
\text{Weight Gain} = k \cdot \left(\frac{\text{RH}}{100}\right) \cdot \sqrt{T}
\]  

(6-57)

When conducting tests at different temperatures with the same relative humidity the conventional acceleration formulae would take the change in temperature into account by means of the Arrhenius equation. This describes the rate of progress of chemical reactions such as corrosion and is valid when considering the failure process as solely one catastrophic failure due to corrosion (a chemical reaction) of an unpackaged device or where the time taken for moisture to breach the package is negligible in comparison to the time required for corrosion to cause failure.

If the observed failure process is one of parameter degradation then significant degradation could occur before moisture saturation of the plastic has occurred. The duration of the moisture absorption process is then a significant proportion of the time required for parameter degradation to be observed.

6.2.4 Leadframe Interface Absorption

A possible second method of absorption is along the leadframe plastic interface. This method would be more likely following the degradation of adhesion of the epoxy to the metal or in packages where the leadframe has been contaminated before moulding,
thereby impairing adhesion. Absorption by this process would be more likely to be observed in packages with a large number of leads or where the leadframe is physically short.

In general the results of the C-SAM tests would suggest that debonding between plastic and leadframe is unlikely even under the most severe of conditions such as HAST. Evidence of debonding could only be found after temperature cycling (100 cycles -55 to 125°C) as observed in section 4.5.1. Unfortunately there were no other alternative tests available, such as dye-penetration, with which to confirm these results. Although no evidence could be found for this effect, with the resources available, this mechanism cannot be discounted. Indeed several factors exist that support the view that in the packages studied moisture ingress along the leadframe could have been the dominant process. They were that despite the considerably different thicknesses of plastic moulding compound over the dies the initial detection of moisture ingress occurred at approximately the same time in both DIL and QFP packages. In addition corrosion was observed at the bondpads in those DIL packages subjected to failure analysis suggesting a creeping moisture front along the leadframe and bondwires.

It is speculated that this process may be more apparent in packages that have been exposed to a soldering process, such as IR reflow or wave soldering, which may promote depolymerisation and debonding. The effects of assembly methods on moisture absorption and subsequent reliability, particularly of surface mount components, could perhaps form the basis of further study.
6.3 Package Internal Stress Model

In addition to the effects of moisture absorption on the reliability of plastic packages there can also exist thermal stress considerations such as those investigated in chapter 5. The internal package stress imparted to the die by the shrinkage of the plastic moulding compound in a 100 quad flat pack package has been measured using on chip stress gauges chapter 5. To verify the results of this study a mathematical model of the behaviour of materials with dissimilar coefficients of thermal expansion (c.t.e) as in the structure a semiconductor has been derived. The behaviour of the model is tested against measured data.

6.3.1 Stress model for QFP Package

In general if the change in length of a material with temperature is given by its cte \(k\). This change in length of an element of such a material \(\Delta l\) is proportional to the change in temperature \(\Delta T\) and the elements original length \(l_0\), equation (6-57).

\[
\Delta l = k(T_1 - T_0)l_0 - l_0
\]  

(6-58)

When two materials A and B with dissimilar c.t.e.s are subjected to the same temperature change their expansion in length will be different.

\[
\Delta l_A = \Delta T.k_A l_0
\]  

(6-59)

\[
\Delta l_B = \Delta T.k_B l_0
\]  

(6-60)

Where

\[
\Delta T = T_1 - T_0
\]  

(6-61)

and

\[
\Delta l = l_1 - l_0
\]  

(6-62)

From Young's modulus;

6-35
If the two materials are bonded together all the way along their length such that a relative change in length is not possible the constrained expansion will produce an internal stress. The difference in force between the two materials is given by (6-64).

\[ F_A = \Delta T k_A l_o E_A \quad (6-63) \]
\[ F_B = \Delta T k_B l_o E_B \quad (6-64) \]

If one of the materials has a Young's modulus that varies with temperature then the model is further complicated. It has been shown in [7] that the Young's modulus of a typical cured epoxy novolac moulding compound varies with temperature. An expression for the thermal behaviour of the moulding compound with respect to its Young’s modulus was derived from this data by linear regression (6-66).

\[ E_B(T) = -4.7T + 1500 \quad (6-67) \]

Combining this expression with (6-64) gives an expression for internal stress that is a quadratic function of temperature which describes the general shape of the observed results in chapter 5. The expression for stress in a 1 dimensional model is given in equation (6-67) where \( T \) is the measurement temperature in degrees Celsius.

\[ F(T) = (T - T_0) l_o (k_A E_A - k_B E_B) \quad (6-68) \]

Substituting typical values for the copper leadframe of; \( E_A = 11.7 \times 10^3 \) dynes/cm\(^2\) and \( K_A = 17 \times 10^{-6} \) p.p.m/°C and for the loaded epoxy moulding compound of; \( K_B = 15 \times 10^{-6} \) p.p.m/°C the predicted behaviour of the package stress model was calculated over the test temperature range. The results of this simulation are shown in Figure 13 and are in units of \( 10^3 \) dynes/cm\(^2\) and temperature is in Celsius.

The model predicts a linear relationship between observed stress and distance from the
neutral axis $l_o$. The stress displays a quadratic relationship versus temperature with zero stress occurring at the moulding temperature (170°C) which increases as the package cools.

![Graph](image)

**Figure 14** Thermal Behaviour of Package Stress as Predicted by simple 1-D model.

When compared with the measured package stress data obtained by on chip sensors, chapter 5, the predicted stress from the simple 1-D model was found to be an order of magnitude too small. The model predicted stresses of the order of $10^8$ dynes/cm² whereas the on-chip sensors measured stresses of the order $10^9$ dynes/cm². The peak stress in the observed data is around 0 to 25°C, depending on device, whereas the model predicted a peak at -25°C. This could be due to the differences between the actual formulation of the moulding compound used and the values quoted in [7], as well as assumptions made in employing linear interpolation to obtain data on the thermal behaviour of Young's modulus. In addition the behaviour of the c.t.e of the moulding compound with temperature could not be taken into account owing to insufficient data. This limitation would also effect the accuracy of the model.

Other limitations of the simple 1 dimensional model that would affect its accuracy are;
That the model only considers the stress between two materials, the leadframe and the moulding compound. In fact the real case is somewhat more complex as it consisted of a sandwich of moulding compound, copper leadframe, silicon die and moulding compound.

The model considered the package material to extend only as far as the stress gauge (0.25 cm from the neutral axis). In practice the package extends beyond the sensor by a further 1 cm and this material also contributes to compressive stress on the die.

The 1-dimensional model, does not take into account the effect of stress into or out of the material above and below, or from material to the sides, of the line through the modelled package.

The position of stress gauge from neutral axis was taken as 0.25 cm from die centre. This was based on measurements taken from the die drawing supplied by the N.M.R.C. If the die were not centred over the neutral axis of the package during the moulding process then errors in stress measurement would occur.

The physical properties of materials were taken as typical values from other studies and can not be guaranteed as being correct for the package employed in this study. Neither was it possible to verify these data experimentally.

6.3.2 Consequences for the Moisture Ingress Model

The reduction in compressive force of the package on to the die and leadframe, with increasing temperature, could increase the rate of permeation of moisture into the package. It has been observed from the data obtained with encapsulated strain gauges that the compressive stress of the plastic on the die decreases from a given level towards zero as the plastic is heated up towards its original moulding temperature. The effect of this is expected to be two fold; first the compressive force exerted on the leadframe by the plastic is reduced so decreasing its sealing properties, and second the percolation threshold of the plastic would decrease as the compressive force between
the resin and filler particles reduces, opening up the existing micro-pores in the moulding compound. This would leave diffusion along the leadframe/plastic interface as a possible moisture absorption mechanism that allows moisture access to the die. However this mechanism would require a loss of adhesion between the epoxy resin to the metal surface.

6.4 Conclusions

**Gain Degradation** - The gain degradation process was modelled theoretically by considering the effects of oxide surface charge on the gain of the transistor owing to the formation of an extended depletion region below the base surface. It was hoped that the model could have been extended to predict the amount of surface charge on the oxide necessary to cause the observed degradation. In practice a relationship to the effective area of charge was derived which links it to terminal currents taking typical values for the physical parameters of the device. An expression for the maximum width of the extended depletion region prior to inversion had already been derived by Reddi.

It was shown that the accumulation of surface charge, which was believed to be due to the transport of ionic contamination by the penetrating moisture front, could effect gain degradation by increasing depletion below the surface widening the depletion region area. In addition a secondary effect was to further reduce gain by enhancing the likelihood of mid-band trapping by recombination centres in the surface region. This occurs as a result of the change in carrier levels bending the Fermi level closer to the trap level thereby increasing the possibility of recombination.

**Moisture Ingress** - The moisture absorption properties of loaded epoxy novolac resins used as moulding compounds for plastic encapsulation of integrated circuits was studied as a function of temperature and humidity. It was found that the moisture absorption process was initially approximately Fickian in nature. With increasing time the moisture front penetrated further into the plastic and the absorption process displayed weight gain characteristic of path blocking behaviour. A model was
suggested that describes weight gain in terms of a reducing effective surface area available for absorption. This behaviour was suggested to explain the path blocking effects of the penetrating moisture front.

As temperature was increased the absorption process tended towards a more Fickian type of behaviour. This was observed as the weight gain with time behaviour tended more towards a root time relationship. The total weight gain observed was very small as no percolation channel existed for the mass transport of moisture through the plastic moulding compound. It was shown however, that despite the lack of a percolation channel, degradation of the electrical behaviour was still possible owing to the extremely low levels of oxide contamination that are required for gain degradation. Comparison with identical samples of transistors, aged under the same physical and electrical conditions, but under conditions of extremely low relative humidity, proved that the degradation process was due to the presence of moisture in the test atmosphere which must have been reaching the die.

*Package Stress Model* - A test die containing, amongst other sensors, piezo-resistive strain gauges was used to measure the package related stresses operating within a 100 lead plastic QFP package over a wide temperature range. An interesting feature of the observations was the peak stress around room temperature which was attributed to the variation in Young's modulus of the moulding compound with temperature. A simple 1 dimensional theoretical mathematical model was derived that showed reasonable qualitative agreement with the experimental results but poor quantitative performance. This lack of accuracy can reasonably be attributed to the simplifications and assumptions made in its derivation in addition to the use of typical values for the properties of its component materials.

**6.5 References**


CHAPTER 7

CONCLUSIONS AND FURTHER STUDY

7.1 Introduction

The study reported in this thesis reported on areas of concern in the exposure of electronic semiconductor components encapsulated in moulded plastic packages to extreme environmental conditions of high temperature and high humidity. It was shown why such doubts had existed in the past along with the reported improvements in reliability that had taken place in the past twenty years. The reasons for these improvements and the process and material changes responsible were reviewed along with failure data from the results of accelerated life testing.

The research reported in this thesis identified the importance of moisture ingress into plastic encapsulated ICs as a potential cause of parameter degradation. Previously the majority of work in this field had considered catastrophic failure mechanisms due to moisture ingress. As the majority of the reported work had focused on catastrophic failures, failures which today require many hundreds of hours under the most severe accelerated life test conditions to occur, it was decided to study parameter changes in addition to catastrophic failures as these occurred earlier and could be a precursor to complete failure. The changes in D.C. parameters of Bipolar Transistors were studied, one parameter which was found to be particularly sensitive to the effects of heat, moisture and bias was d.c gain (or beta). The degradation of beta in Bipolar Transistors encapsulated in P-DIP packages was studied as well as the wear-out mechanisms leading to catastrophic failure.

The study of other package styles required another approach and for this part of the study package performance monitoring chips were employed. These were encapsulated in 100 lead Plastic QFP packages and subjected to H.A.S.T. and temperature cycling tests. The use of these devices made possible the in-situ measurement of moisture and package related stress at the die.

This thesis represents the distillation of the results from many thousands of
hours of H.A.S.T. tests over a range of test conditions (110-130°C & 65-85%RH), and many hundreds of hours of tests at elevated temperature it is not suggested that this study was exhaustive and suggestions for further investigations are made.

7.2 Moisture Absorption

The initial phase of the study was to investigate the moisture absorption behaviour of moulded plastic packages. This was accomplished by monitoring the weight gain of the packages when exposed to a range of temperature and humidity. It was found that although in the first few hours of exposure the moisture absorption appeared to have a square root dependency on exposure time, typical of Fickian diffusion, however as time increased the behaviour tended more towards the path blocking behaviour of a percolation process operating below its percolation threshold. Such behaviour prevented mass transport of moisture to the die and hence allowed excellent moisture sealing properties. The parameter degradation study showed that exceedingly small levels of moisture were in fact needed for gain degradation to be observed at low current levels so that it could occur even when a percolation channel for bulk transport did not exist.
7.3 Performance of Plastic Packages

Two different package styles were employed in this study, the Dual In Line Package (through hole) in which were encapsulated bipolar transistors, and the Quad Flat Pack package (Surface Mount) which was used to encapsulate the package monitoring test dice.

7.3.1 Plastic Dual In Line Package

The results of H.A.S.T. testing on the P-DIP Bipolar transistors revealed that the D.C. current gain (beta) was particularly sensitive to the ingress of moisture. (Tests under identical elevated temperature and bias conditions showed virtually no early signs of beta degradation). This degradation was observed to begin after only 25 hours in the autoclave at 130°C and 85%RH. Catastrophic failures began to occur after 200 hours and continued throughout the test to 1500 hours. Plotting the occurrence of these failures on Weibull paper for both the temperature cycled and non-temperature cycled devices showed them to have identical shape parameters and to have increasing failure rates associated with the presence of a wear-out mechanism.

*Parameter Failures* - The Bipolar Transistors were observed to suffer dramatic gain degradation under H.A.S.T. testing (up to 15%). In the case of the plastic encapsulated devices this was observed to begin as early as the first measurement interval of 25 hours. The gain degradation process produced fairly even degradation over the first 600 hours of accelerated life testing. The test base current was increased over five decades (0.1 to 1,000 μA) the collector current was measured and the D.C. current gain was calculated. The degree of degradation was observed to be strongly related to the level of base current. The flow of base current controls the flow of emitter-collector current, when this is small the transistor is operating under low injection conditions. This refers to the level of minority charge carriers that are injected from the highly doped emitter region into the emitter-base depletion region. While the minority charge carriers cross the depletion region they are susceptible to recombination, either at the surface or in the bulk. On recombining they contribute to the base current. Under low injection conditions the level of minority charge carriers
was small and a comparatively large proportion of them under go recombination, hence for a small emitter currents the greatest reduction in gain is measured. As the level of injection (emitter current) was increased gain increased as the fixed number of recombination centres were swamped by the high level of minority charge carriers injected into the region. At very high injection levels the number of recombination centres were so small in comparison to the level of minority carriers that they had little effect on gain.

The gain degradation process observed during the H.A.S.T. tests resembled closely the gain degradation observed in epitaxial Bipolar transistors exposed to far higher temperatures (200°C) and bias, but for very much longer durations (>1000 hours). In this process thermally mobile impurity ions in the moulding compound were responsible for a time and temperature dependent build up of surface charge on the oxide passivation layer which was responsible for an increase in the number of recombination sites in the depletion region with a subsequent increase in base current and decrease in observed gain. The surface charge build up was attributed to the mobility of contaminants in the silicon dioxide passivation. In the H.A.S.T. test gain degradation was observed to occur far more rapidly than that reported in the elevated temperature tests. No appreciable degradation was observed in the high temperature biased tests which were run as a control. An explanation for this effect is that the build up of charge is due to the much more rapid transport of impurity ions from the plastic to the passivation layer in the presence of the ingress of moisture.

The dependence of the rate of gain degradation, and hence surface charge build up on the oxide, has been shown to be dependent on the energy (temperature) of the water molecules and also dependent on the number available (relative humidity) to form the solvent front.

**Catastrophic Failures** - Failure analysis of the de-capsulated devices revealed two competing failure mechanisms, bond pad fracture and metallisation corrosion. Of these the bond pad failure was the most prevalent and resulted in a complete loss of electrical continuity as revealed by SEM. Metallisation corrosion was most frequently observed to have occurred when associated with a cracked passivation layer, although it is not possible to say which occurred first. It seems most likely that metallisation
corrosion occurred as a result of moisture breaching the passivation layer through the most minimal of defects and the resulting formation of aluminium salts from the corrosion process caused further damage to the passivation layer, and hence even greater corrosion with further passivation layer damage. Had the damage to the passivation layer occurred as a result of thermal gradients then a much higher occurrence of this failure mechanism might have been expected in the batch subjected to temperature cycling (-55 to 125°C) but this was not the case.

When the data from the thermal cycled and non-cycled test were examined as Weibull plots no difference was observed between the two groups of data and it was concluded that the effects of temperature cycling was minimal despite the packages having absorbed on average 0.3% of their body weight of water from the atmosphere.

Bulk analysis at the sites of both types of failure mechanisms showed the presence of chlorine and bromine ions. Both of these elements are associated with corrosion and the corrosion processes have been explained in chapter 3 (3.4.5.3.4). The presence of chlorine can be traced back to residues from the reaction that is used to produce the Epoxy-Novolac Resin, in this reaction Novolac resin is reacted with epichlorohydrin to form Epoxy Novolac Resin. Despite the manufacturers attempts to reduce the concentration of chloride ions in the resin (<10 p.p.m.) some residual ions remain which are hydrated in the presence of moisture and will migrate towards positively biased areas of the die.

Bromide ions are present as a result of the reaction of tetra-bromo-phenol-A with epichlorohydrin to produce a brominated epoxy compound that is mixed with the resin to act as a fire retardant. In the presence of moisture and an applied potential bromide ions are also detected at anodic regions.

Bond pad failure was observed to be the most common cause of failure in these packages. The bond pads are left exposed in the conventional method of wire bonding making them prone to corrosion. In addition the junction between the gold bond-wire and aluminium bond pad is liable to embrittlement by the formation of intermetallic compounds. The formation of such compounds requires the migration of one metal into the other which can result in voids appearing in the bulk of the metal. This process is accelerated by the presence of bromide ions from the halogenated fire retardants as reported in chapter 3 (3.4.5.4.).
The development of a new bond pad structure where the aluminium metallisation is completely covered by a titanium-tungsten alloy which extends out over the passivation layer may help to prevent this failure mechanism. Firstly the sealing of the bond pad should help prevent corrosion of the aluminum metallisation and secondly the gold bond wire is separated from the aluminium bond pad by the alloy layer thereby reducing the occurrence of voiding. A test between the comparative reliability of the two bonding methods under H.A.S.T. would suggest that the alloy coated bond pads may have better high temperature and humidity reliability.
7.3.2 Plastic Quad Flat Pack

The study of more complex packages such as the QFP with its much increased lead count made another approach to the assessment of plastic package reliability possible. In this case it was possible to employ the latest generation of package performance test chips. These are sophisticated devices with a number of sensors designed to address the major failure mechanisms associated with plastic packaging. It was found that by employing these devices it was possible to monitor build up of moisture at the die over a range of temperatures and humidity, and also measure the package induced stresses on the die.

**Moisture Ingression** - The PMOS3 test chips proved useful in the investigation into the rate of moisture ingress into QFPs. The unpassivated leakage path detectors showed that moisture was breaching the moulding compound and having an effect on surface resistance for test times between 50 to 300 hours. The passivated sensors, with one exception, showed no significant increase in leakage current for test times up 400 hours. Considering the test conditions were 130°C/85%RH with bias of +/- 10 Volts these figures are very impressive for a package whose thickness is only 1mm from the die surface to the external environment.

**Corrosion Onset** - The unpassivated corrosion monitors showed signs of corrosion after 300 hours and the passivated ones showed no change within the duration of the test (400 hours). From this data it was concluded that the 100 lead QFP package has very impressive moisture resisting properties despite it thin size.

**Package Induced Die Stress** - The package related internal stresses exerted on the die were measured at two different sites and their variation with temperature was measured. The magnitude of these stresses were compared to the stresses required to cause failure by shear or compression of the component parts of the die and package.

7.4 Achievements

It is considered that in the course of this study the following necessary processes were
successfully accomplished;

An extensive literature survey was conducted that brought to light an extensive number of reported failure mechanisms. The extensive treatment of the improvements that have taken place in package technology over the past 25 years was presented. The actual reported improvements in device reliability due to package performance was presented by reporting the results of accelerated tests conducted by other workers in this field. The resulting improvements were shown graphically. The results of this survey were used to plan the study.

An autoclave was commissioned for the accelerated life testing of electronic components by HAST techniques. The correct operation of which required the tracing and purchasing of specialist test boards and the construction of test jigs from approved materials to comply with JEDEC standard A110. A test regime was established which ensured the required levels of ionic contamination were maintained by thorough and regular cleaning. This was checked by chemical analysis (ion chromatography and atomic absorption) of the water samples taken from the equipment. The equipment was inspected and serviced at six monthly intervals.

Accelerated life tests were conducted on plastic and ceramic encapsulated devices employing; HAST, temperature cycling and high temperature aging in ovens.

The presence of parameter degradation was observed in bipolar transistors. The most sensitive parameter was gain. This was observed to occur long before catastrophic failure. It was therefore suggested that monitoring of degradation may provide an initial early warning of later catastrophic failure due to moisture ingress.

If this could be shown to be true then the monitoring of parameter degradation (in particular gain degradation for Bipolar transistors) could be used as a method of shortening accelerated life test times. This could have cost saving implications for the semiconductor industry as it would allow poorly encapsulated batches to be detected earlier thereby increasing testing throughput and so provide a greater return on
accelerated life testing equipment, or alternatively reduce the number of autoclaves required. It is particularly important to find a method of detecting the possible onset of failure earlier as the HAST testing that is presently conducted is under the most highly accelerated conditions consistent with accelerating representative failures. Increasing temperature further would have the potential risk of degrading the plastic by stressing it at temperature too close its glass transition temperature. Humidity cannot realistically be taken above 85% as there are problems with maintaining the temperature profile accurately across the chamber with the risk that condensation could form in locally cool regions.

A mechanism has been suggested that relates moisture ingress to the build up of charge on the oxide layer and its subsequent effects on observed gain degradation. A mathematical model has been derived that described the action of surface charge accumulation by considering its effective surface area and the effect it has on gain through the formation of an extended depletion region and Fermi Level changes.

Catastrophic failure mechanisms were observed and failure analysis was performed which attributed the failures to corrosion of the metallisation and bond pad areas. The effected areas were subjected to surface and bulk analysis which showed halogen induced corrosion. The presence of these ions on the positive biased areas suggested that the ions were mobile and migrated with the applied electric field. The tests required metallurgical cross sectioning and sample preparation techniques.

Silicon test dies incorporating strain gauges were encapsulated in plastic surface mount packages and the package induced stresses observed over an extensive range of operating temperatures. A model was proposed that described this behaviour.

The same test dies incorporated triple track aluminium meanders which were used to detect the ingress moisture reaching the die by the formation of leakage paths. The onset of corrosion was detected by observing the increase in line resistance. This was accomplished for both passivated and un-passivated structures which allowed conclusions to be drawn about the effectiveness of the passivation layer in preventing
moisture reaching the silicon surface.

As result of this study two papers have been published into the applicability of HAST testing in assessing package related reliability, [1] [2].

In the course of this investigation a test station was constructed for the logging of results. The test station comprised of a number of GPIB controlled instruments under the control of a PC. The PC was connected to the departmental computer network via Ethernet which allowed rapid collection, logging and transfer of data to a more powerful machine which was employed for data analysis. The test station software was written in C programming language.
7.5 Future Study

Investigate further the effects of moisture and temperature on Bipolar transistors:

a/. Use a.c measurements from l.f to r.f. and also investigate noise performance as it has been suggested that this is a potential indicator of the condition of surface state.

b/. Look for a possible correlation between early parameter degradation, later degradation and even catastrophic failure.

c/. Could such a correlation, if it exits, be used to shorten test times and identify weak packages.

d/. Is the weight gain process reversible by baking to remove absorbed moisture and if so are any of the observed parameter changes even partly reversible? An investigation of such effects could lead to a better understanding of the "no fault found condition" that has been frequently reported in the field failure data returned to I.E.R.I. for collation into the field failure database.

e/. The study could be repeated with MOS devices - using both d.c and a.c. measurements.

Further study employing the PMOS3 package test chip;

f/. Use PMOS3 test chips to investigate moisture ingress using interdigitated test structures but repeat with capacitive measurement techniques instead of resistance measurements.

g/. The strain gauges could be employed to see if there is any build up of or relief of stress in the package following temperature cycling.

h/. Does the decrease in compressive stress of the moulding compound on the die
with increasing temperature, as observed by stress gauge measurement, result in an easier path for moisture ingress? If so what effect does this have the expected life time (from accelerated life test data) for plastic packaged devices in humid environments? Is there a danger of predicting too short an expected life due to the increased ease of moisture ingress at the temperatures used. In which case is there an argument for using a humidity term that is a function of temperature in the acceleration equations? Would such a non-linear system prove be too difficult to model?

h/. The QFP package displayed excellent moisture resistance properties however as the method of moisture detection was different to that employed for the DIP package comparison between them was not possible. It would be useful to observe the effects on gain degradation for identical transistor arrays encapsulated in identical QFP packages.
7.6 Summary

Plastic encapsulation of semiconductors has improved remarkably over the past twenty five years its ability to resist the ingress of moisture resulting in much longer test times before failures occur. With increasingly complex devices coming onto the market more attention should be payed to parameter degradation as a means of detecting package integrity. Corrosion failures are much reduced by the better moisture resistance but also by the reduction of ionic species in the packaging materials (especially chlorine, bromine and phosphorus). The bond pads remain a weak point however, but there is reason to believe that in this area too reliability can be improved by the sealing the pad from the moulding compound with an alloy buffer layer such as Titanium/Tungsten.

Plastic packages with thicknesses as thin as 1mm can provide impressive moisture resistance. The spread of plastic packaged devices into applications were traditionally hermetic packaged devices have been used looks increasing likely. Ceramic packaged devices will still remain pre-eminent for some time to come in areas where high dissipation (>4 Watts) is required.

References

APPENDIX A

PMOS3 TEST CHIP PIN-OUTS OF TEST PACKAGE

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APPENDIX B

IERI TEST PACKAGE BOND WIRE DIAGRAM
APPENDIX C

PMOS3 WAFER SPECIFICATION
PACKAGE PERFORMANCE MONITORING TEST CHIP

PMOS3 - NMRC

WAFER SPECIFICATIONS

Diameter: 100mm
Thickness: 500 micron
Fabrication Process: PMOS with extra n+ diffusion.
Silicon crystal orientation: <100>.
Substrate Doping: N-type; 2-4 ohm-cm
P+ Diffusion Doping: 108 ohms per square.
Gate Oxide Thickness: 1150 angstroms.
Metallisation: Aluminium/1% silicon.
Passivation:
   Bottom layer: 6k angstroms doped (3-5% Phosphorous) CVD silicon dioxide.
   Top layer: 3k anstroms undoped CVD silicon dioxide.
Number of complete die per wafer: 170 approx.
Wafer back metallisation: None.

DIE SPECIFICATIONS:

Die size: 5800 microns by 5800 microns.
Die pitch: 5900 microns by 5900 microns.
Scribe channel width: 100 microns.
Number of I/O pads: Top - 25
               Bottom - 19
               Left - 25
               Right - 25

Total I/O Pads: 94
I/O Pad Size: 100 microns square.
I/O Pad Pitch: 200 microns.
Passivation window opening over I/O pads: 90 microns.
The IC contains a number of structures which can be used to evaluate the performance of IC packaging materials and structures. The following is a list of the various structures and their areas of application.

- 2 off large area diffused resistors
  - heat source/temperature sensor

- 4 off triple track aluminium meanders (2 monitors are unpassivated)
  - corrosion monitors
  - surface conductivity moisture sensors (with temperature sensor)
  - stress-induced metal shift (unpassivated structure only)

- 5 off, four resistor, diffused resistor strain gauges
  - piezo-resistive strain

- 2 off p-n junction diodes
  - temperature sensing

- Wire Bond Resistance Structure: Monitor variation in wire bond resistance.

- Substrate Contact: Surface ohmic contact to substrate bulk.
PACKAGE PERFORMANCE MONITORING TEST CHIP

PMOS3 · NMRC

TEST STRUCTURE DETAILS

CORROSION MONITOR:

Type: Triple track aluminium meander.
Schematic: See accompanying document.
Number of Monitors: 4.
Line width: 10 microns.
Line pitch: 10 microns.
Line thickness: 1 micron.
Typical line resistance: 220 +/- 10 ohms.
Number of I/O pads: 2 per individual conductor/6 per monitor.

Pasivation:
  Monitors C1 and C3 are passivated
  Monitors C2 and C4 are unpassivated.

Gate Oxide Runners:
  Gate oxide "runners" are incorporated into the structure at right angles to the metal tracks to simulate the topography of an actual integrated circuit. Three sets of runners are used with the following widths/pitches: 10/20 microns; 20/40 microns and 50/100 microns.

Accelerated Testing:
  The structure can be used in accelerated temperature/humidity stress tests. The line resistance or the leakage current between lines can be monitored. In biased stress testing, the central conductor can be grounded and the two outer conductors biased positively and negatively as required. In this manner, the occurrence of both anodic and cathodic corrosion can be studied in one structure.

Unpassivated Corrosion Monitors:
  These devices may also be used to measure the extent of stress induced shift of aluminium metal. A further application is as surface conductivity monitors (in conjunction with on-chip temperature sensors) in the investigation of the moisture content of hermetic IC packages.

Four Point Resistance Measurements:
  If very accurate measurements of conductor resistance are required, four point resistance measurements can be made at the package level only.
PACKAGE PERFORMANCE MONITORING TEST CHIP

PMOS3 - NMRC

TEST STRUCTURE DETAILS

Heat Source: - 2 off.

Material: P+ diffusion in N- substrate.

Typical resistance: 300 ohms

Current Limit:
  200-250 milli-amp approx. per resistor.
  - (limited by current carrying capability of metallisation/wire bond).

Voltage Limit:
  Device tested to 25 volts only, approx. 1.5W per heater. Further tests required to check operation at higher voltages.

Number of I/O Pads:
  Four per heater/two per electrode.
  - allows four point resistance measurement for accurate measurement of temperature coefficient of resistance.
  - allows accurate calculation of resistance during thermal characterisation tests.

Temperature Coefficient of Resistance (TCR)
  - +800ppm/°C @ 20°C
  - +1400ppm/°C @ 100°C

Ref. TCR Plot
APPENDIX D

PUBLICATIONS RESULTING FROM THIS STUDY

"The Comparative Reliability of Resistor Types Under HAST"
N.M. Troop, J.A. Jones & J.A. Hayes,
6th European Capacitor and Resistor Symposium
CARTS - Europe '92
5th-8th October 1992
Novotel Brugge Centrum, Belgium

"HAST an Accelerated Life Test for Packaging"
N.M. Troop
I.E.E Electronics Division Colloquium on "Characteristics of Device Packaging"
Institution of Electrical Engineers Savoy Place London WC2 0BL
23rd November 1992 Digest Number 1992/213