

## A review of thin-film transistors/circuits fabrication with 3D self-aligned imprint lithography

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## Flexible and Printed Electronics



### TOPICAL REVIEW

# A review of thin-film transistors/circuits fabrication with 3D self-aligned imprint lithography

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### Abstract

Nanoimprint lithography (NIL) is a promising method for the fabrication of micro/nanostructures through a simple, low-cost, and high throughput process. Imprinted 2D structure with high resolution has been demonstrated successfully for certain applications including magnetic hard disks and optical gratings. Manufacturing low-cost electronic devices that require patterned multi-layers with NIL is very challenging, particularly for those requiring different patterns. In recent years, considerable effort has been made using the self-aligned imprinting technique, opening an alternative way to develop and fabricate complementary flexible electronics. In this paper we review thin film transistor (TFT) fabrication with 3D self-aligned imprint lithography (SAIL), which enables the patterning and alignment of submicron features on meter-scale flexible substrates in the roll-to-roll configuration. The 3D SAIL solves the problem of precision interlayer registry of devices on a moving web by encoding all geometric information required for all device patterning steps into a monolithic imprinted 3D structure.

## 1. Introduction

Recent developments in semiconductor materials and flexible electronics applications have motivated a rapid increase in demands for low-cost, high-throughput, and high-resolution fabrication techniques [1–5]. Low-cost electronics require roll-to-roll production with flexible substrates [6–8], which undergo non-uniform deformation during device fabrication so that the usual photolithographic processes that require precise layer-to-layer alignment are difficult and costly to implement. Conventional 2D nanoimprint lithography (NIL) is capable of producing structures with high resolution, and is compatible with roll-to-roll manufacturing processes [9–11]. However, it is only suitable to produce single-layered structures, and it is challenging to build up subsequent layers aligned with existing structures. The problem of layer-to-layer alignment on flexible substrates can be solved using a 3D self-aligned imprint lithography (SAIL) by encoding all geometric information required for all patterning steps into a monolithic 3D mask that is imprinted on a thin film stack deposited on a flexible substrate [12–14]. Since the monolithic mask (normally made of polymers) itself also distorts with the substrate,

alignment is preserved throughout subsequent processing. The 3D SAIL enables the patterning and alignment of submicron-sized features on meter-scaled flexible substrates in a roll-to-roll environment, using a sequence of steps to alternately etch functional materials and thinning the mask with multi-levels to define the dimension of each device component. This technique can be used for manufacturing various electronics, for instance, arrays of thin film transistors (TFT) that serve as an active matrix backplane for flexible display. Although 3D SAIL can be used for making many different devices, here we will focus on several processes for transistor fabrication that play key roles in flexible electronics. We will start with a brief description on conventional NIL techniques, followed by an introduction of silicon-based TFT fabrication with 3D SAIL, and then discuss the combination of 3D SAIL with other fabrication techniques for organic transistor development.

## 2. NIL

Fabrication of small structures by imprinting or molding was introduced in the 1970s when thermal

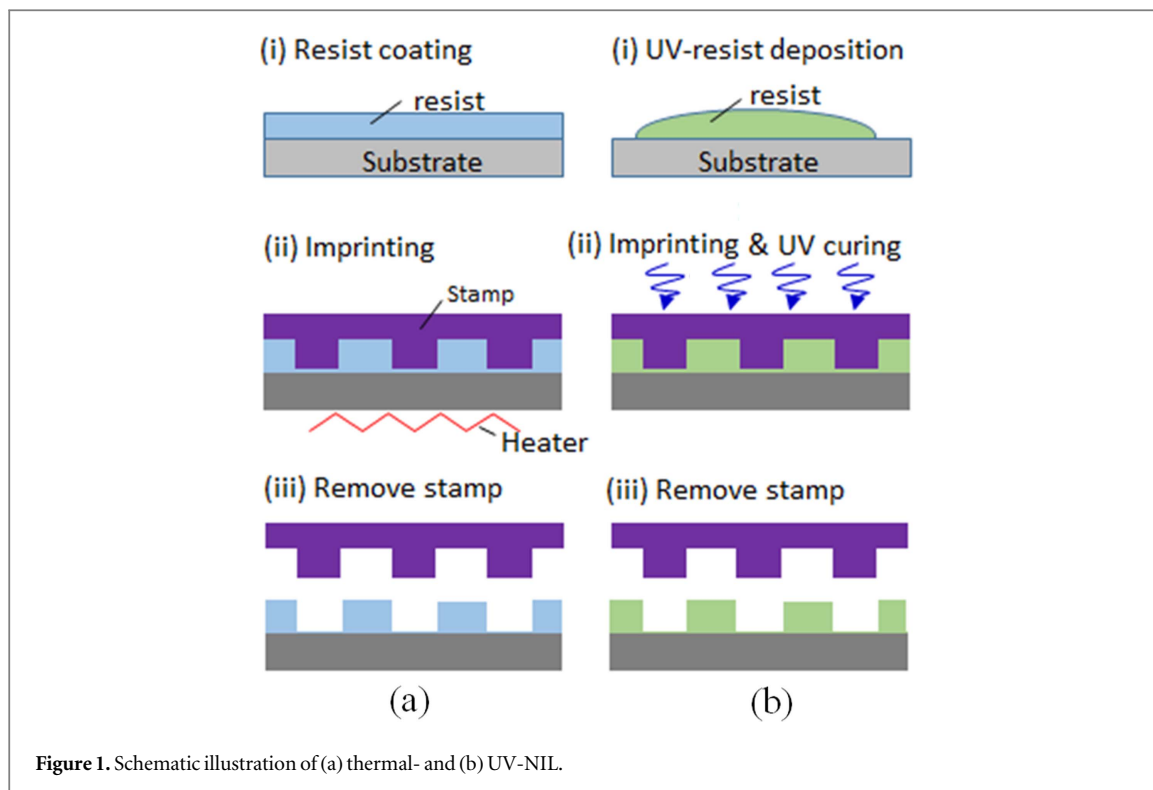


Figure 1. Schematic illustration of (a) thermal- and (b) UV-NIL.

embossing was published from RCA laboratories at Princeton, NJ, USA [15]. Meanwhile, researchers at NTT laboratories in Japan had studied imprint technology and named it the ‘molded mask method’ [16]. Remarkable progress was made in 1995 when Chou *et al* demonstrated a nanostructure with 25 nm resolution obtained by nanoimprinting and subsequent pattern transfer [17, 18]. Since then, nanoimprinting has attracted great attention for fabricating micro/nanostructures for various applications including magnetic [19, 20], electronic [21, 22], optical [23, 24], and biological devices [25, 26]. Based on thermal-NIL, alternative methods have also been demonstrated. For instance, Colburn *et al* developed step-and-flash imprint lithography (S-FIL), which is considered as UV-NIL [27]. Figure 1 shows a schematic illustration of thermal- and UV-NIL, respectively. For the thermal imprint the imprint stamp is normally fabricated by standard lithography, like an electrical beam or optical lithography using rigid materials.

The stamp, treated by a hydrophobic self-assembled monolayer (SAM) molecule for anti-adhesion, is brought against a pre-coated polymer layer with low glass-transition temperature at proper temperature, and the structured sample is released after cooling the sample to room temperature (figure 1(a)). Plasma etching is required to remove the residual thin resist layer for further transfer of the imprinted pattern into other materials (by lift-off, electroplating, and mask-etching). For the UV-NIL as shown in figure 1(b), a UV-curable resist is used, making it more convenient than thermal-NIL because the UV curing can be done in a time scale much

shorter than that used for heating and cooling. A transparent stamp, like polydimethylsiloxane (PDMS) or quartz, is normally used for UV-NIL to ensure UV light access. The UV resist can be applied by spin coating or dispensing with a controlled volume. The UV-curable resist with very low viscosity is able to spread out on the substrate and fill the space with the capillary effect during imprinting. If a flexible stamp is used, the NIL is called soft thermal-NIL or soft UV-NIL [28, 29]. Deformation of the soft stamp leads to distortion of the imprinted structure and limits the resolution of soft UV-NIL.

The most commonly used stamp materials are silicon, silicon oxide, silicon nitride, metals, and polymers, because these materials are compatible with conventional semiconductor technology for high-resolution fabrication or duplication. Rigid stamps that are directly fabricated use standard lithography technologies, like e-beam, optical interference, focus ion beam, and photolithography, while soft-stamps are duplicated from rigid templates [30–32]. Some rigid stamps are also made by duplication from master templates, for instance, nickel stamps can be created by electroplating from a lithographically patterned master [33]. Anti-adhesion treatment is required for most stamps except those made of materials that are intrinsically hydrophobic/oleophobic, like PDMS, and Teflon [34, 35]. A commonly used anti-sticking agent is SAM terminated with hydrophobic/oleophobic groups ( $-\text{CF}_3$ ,  $-\text{CH}_3$ , etc) applied on the stamp surface. Imprint stamps are commercially available, e.g. Nanonex, Obducat, and NIL Technology offer customized stamps with different standards.

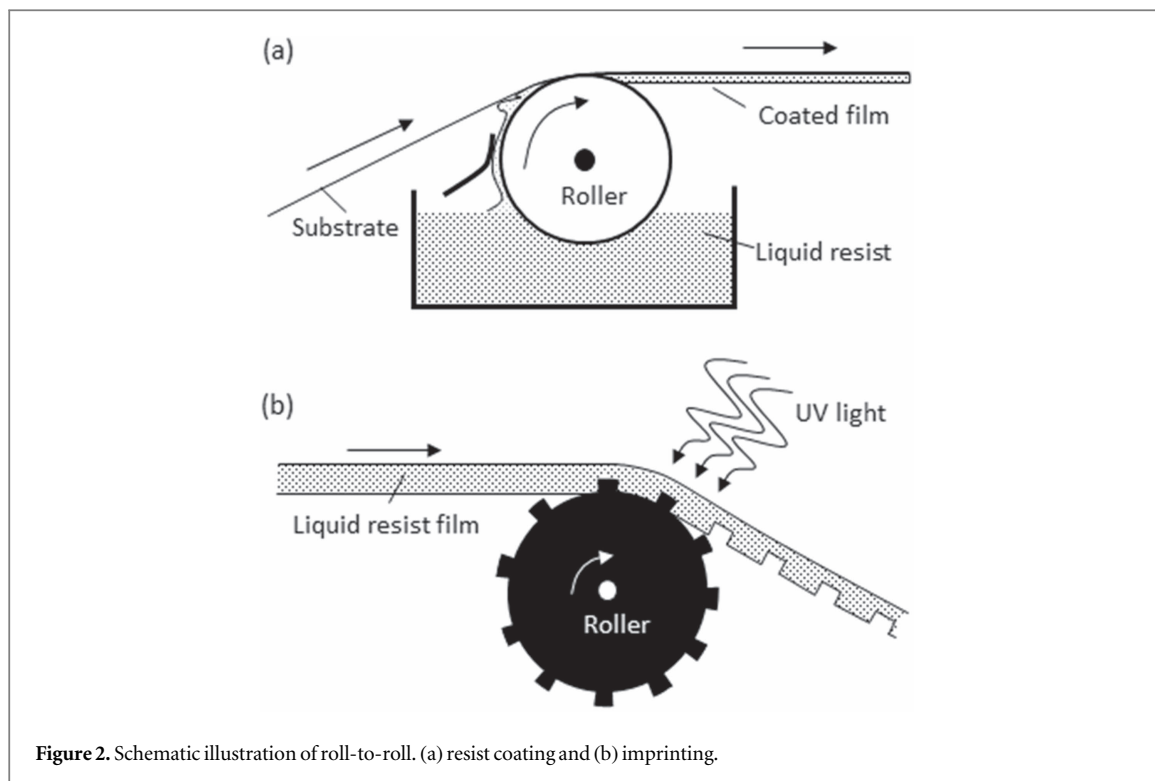


Figure 2. Schematic illustration of roll-to-roll. (a) resist coating and (b) imprinting.

Imprint resists with different properties are required according to the nanoimprint method adapted and final structures fabricated. Some properties of imprinting resists are the same across all methods: sufficiently low viscosity to fill up all features, sufficient mechanical strength, and a dry etching property of the finished structure for later pattern transfer. Commercially available UV-resists are offered by some companies such as Micro Resist Technology, AMO, Obducat, and Molecular Imprint. Commercial NIL tools allow automatic substrate loading, alignment, and imprinting with integrated thermal or UV sources. The world-leading suppliers include Molecular Imprint, Nanonex, SUSS MicroTec, EV Group, and Obducat.

The high resolution and throughput of NIL offer great potential for industrial applications. Presently, the most popular imprinting techniques are (i) large area single-step imprint, (ii) step-and-repeat imprint, and (iii) roll-to-roll imprint. The challenge of imprinting a structure over a large area is maintaining firm contact between the stamp and substrate, and this is achieved by using soft UV-NIL. Current commercial UV-NIL tools enable imprinting nanostructures over an area up to 30 cm by 30 cm. Another commercially available imprinting device is the step-and-repeat nanoimprint technique, where the imprint is performed repeatedly over a large substrate using a relatively smaller rigid stamp (for instance 2.5 cm by 2.5 cm), which avoids the deformation of the soft stamp in the case of soft UV-NIL, and also achieves higher resolution. Roll-to-roll imprint is a technology for high-throughput fabrication. Roller stamps and flexible substrates are used to realize high speed and resolution

(figure 2). A similar technique is roll-to-plate NIL, which uses a structured roller imprint on a rigid substrate [10].

### 3. TFT

Transistors are a type of device where electrical current between two electrodes is controlled by a third electrode. Such three-terminal devices can perform many useful functions, such as signal amplification and logical processing. The solid state transistor was invented by John Bardeen, Walter Brattain, and William Shockley, who received the Nobel Prize in physics in 1956. Transistors can generally be categorized into two types: the bipolar junction transistor (BJT) and field effect transistor (FET). The BJT was the first kind of commercially mass-produced transistor [36, 37]. It consists of two p-n junctions: the base-collector and base-emitter junctions. Collector and emitter currents are effectively controlled by the small current at the base. The FET uses either holes (p-channel) or electrons (n-channel) for conduction between source and drain electrodes. A gate electrode, which is separated from the semiconductor by a dielectrics layer, is used to control the source-drain current through varying the applied gate voltage [38]. The most commonly used FET design is the metal-oxide-semiconductor field effect transistor (MOSFET), where heavily doped regions are used to form source/drain electrodes [39]. Figure 3(a) shows a schematic illustration of an n-channel MOSFET structure.

BJTs are characterized by linear current transfer between the collector and base currents, and they have

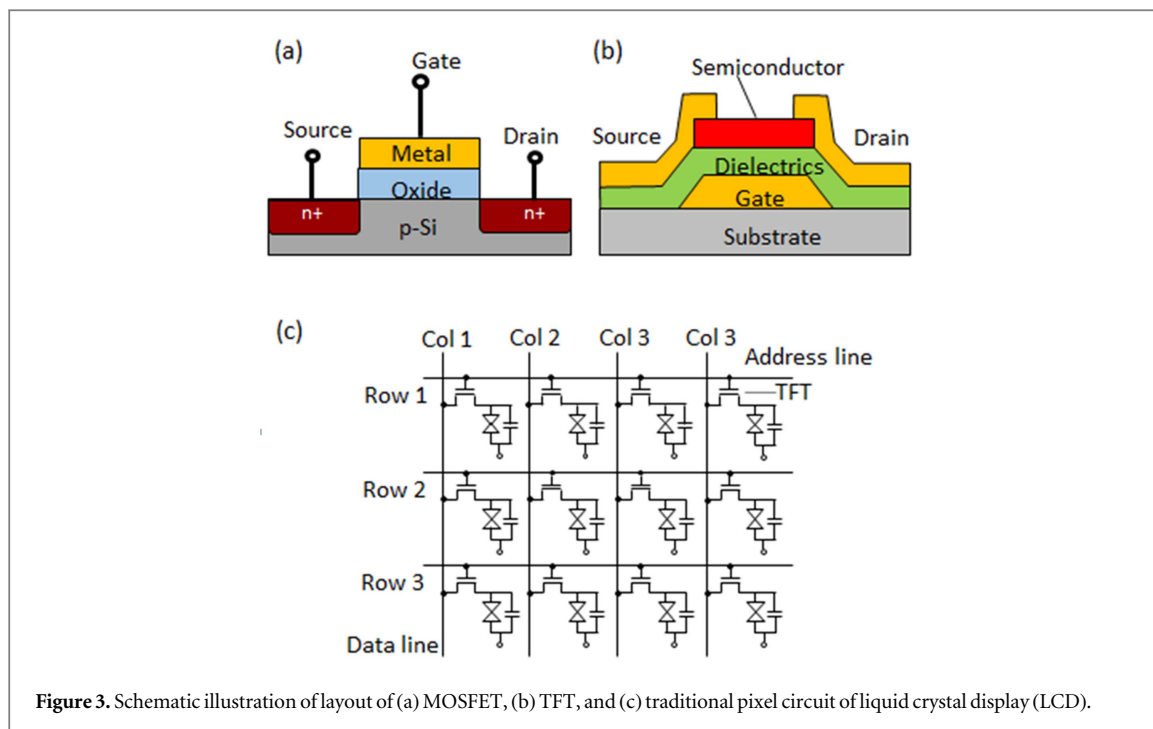


Figure 3. Schematic illustration of layout of (a) MOSFET, (b) TFT, and (c) traditional pixel circuit of liquid crystal display (LCD).

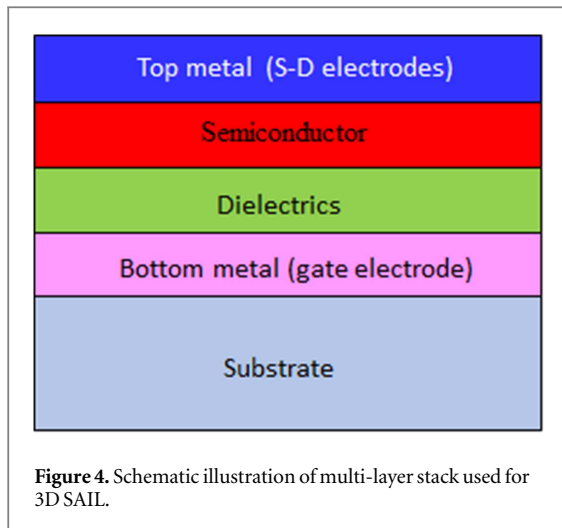
much larger transconductance and higher input signal gain than FETs. In addition, they have higher speeds and higher maximum operating frequency, and consequently are preferred in amplifier circuits and linear integrated circuits, as well as in high-frequency and high-power applications. When operated as switches the BJTs consume appreciable power and therefore are less suitable for very large-scale integration circuits. However, they are used in very high-speed logic circuits. The FETs are characterized by high input impedance, and certain types of FETs operate as a relay, making them superior as switches. Therefore, the dominating logic family for implementing memories, central processing units (CPUs) and digital signal processors (DSPs) are made of MOS transistors, especially in circuits with complementary metal–oxide–semiconductor (CMOS) design, which has good logic performance parameters and low energy consumption. The MOSFET made from a single crystalline semiconductor requires ion-implantation, high-temperature diffusion etc. Processes that are not suitable for low-cost production on a plastic substrate. A low-cost version of the FET is the TFT, which can be fabricated at low temperature through depositing thin films of functional materials (polycrystalline silicon (p-Si), amorphous silicon ( $\alpha$ -Si), oxide, organic semiconductors) on substrates by cheap deposition methods including sputtering, thermal evaporation, and printing [40, 41]. The TFTs are widely used in active matrix flat-panel displays where an integrated switching device is used at each cross point of data and address lines. Integrated switching devices mostly use TFTs made of micro-structured thin-films [42]. The number of TFTs used in a single pixel of display depends on the particular design. Figure 3(c) is a schematic illustration of a pixel

circuit of an active matrix liquid crystal display (LCD), showing that TFT fabrication determines the process of the backplane manufacturing.

#### 4. 3D SAIL

As a conventional microfabrication technique, optical lithography is difficult to be used for manufacturing flexible electronics with high throughput, such as in roll-to-roll. When optical lithography is used to pattern microelectronic devices on plastic substrates the dimensional change associated with the fabrication process can be as large as 0.1 percent. This change translates into 100  $\mu\text{m}$  of overlay misalignment if a 10 cm wide web is used, which is larger than the pixel size of display, and makes the interlayer alignment with optical lithography very challenging. To address this problem a roll-to-roll based on 3D SAIL technology has been developed [43]. In the 3D SAIL process, all geometric information is coded in a monolithic, multi-level 3D polymer mask that is imprinted on a stack of device materials pre-deposited on a substrate. The mask contains information about the dimensions and azimuth relations of all components of devices, including source–drain electrodes, the semiconductor layer, and the gate electrode.

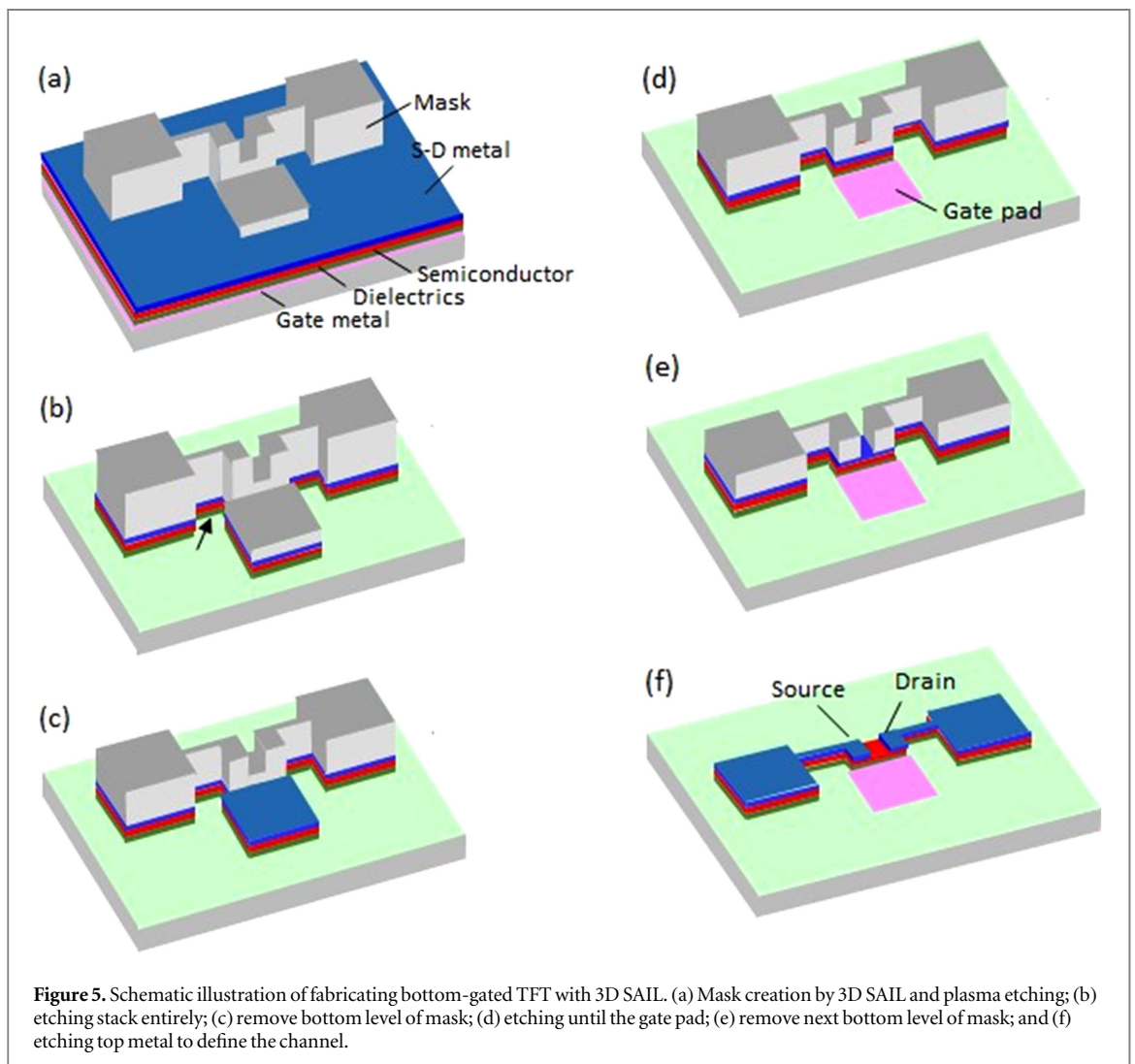
A stack of multi-layered films was pre-deposited on a substrate and then a 3D polymer mask was generated by SAIL. Figures 4 and 5 are schematic illustrations of the thin-film stack and pattern transfer process for fabrication of a bottom-gated transistor [43]. After creation of a 3D polymer mask (figure 5(a)) etching (both wet and dry) was used to entirely etch through the film stack (figure 5(b)). Plasma etching

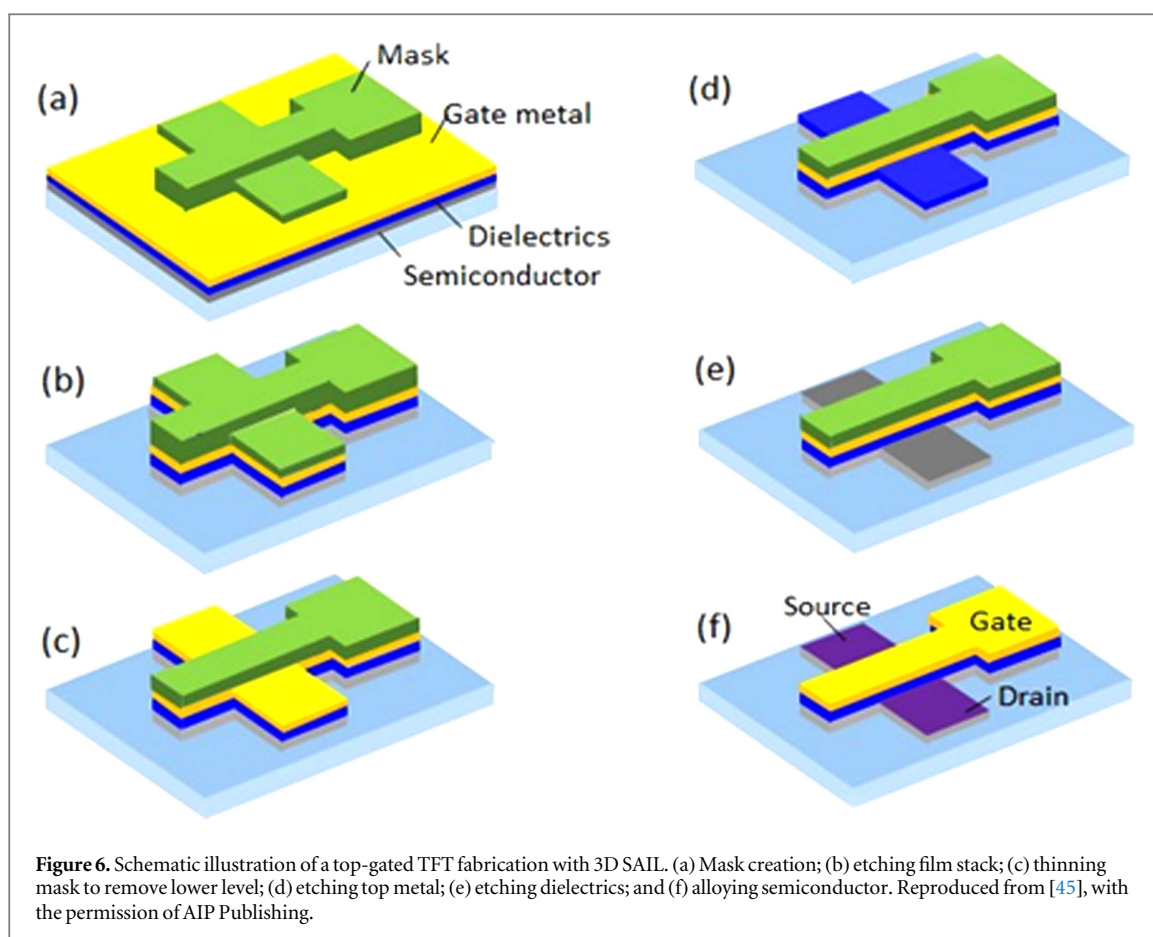


was used to etch the sample until the lowest level of the mask was removed to expose the top metal layer (figure 5(c)), and then sequential etching was applied to expose the gate pad (figure 5(d)).

Dry etching was further used to remove the second lowest level of the mask to expose the top metal layer in the channel (figure 5(e)), and one additional etching

was used to define the transistor channel (figure 5(e)). Finally, the remaining mask was removed using solvent (figure 5(f)). The thin-film stack was modified depending on the type of transistor. For  $\alpha$ -Si TFT a highly doped microcrystalline silicon ( $\mu$ c-Si) layer can be introduced between the top metal layer and the active layer for charge injection. An example of this kind of film stack was developed by Hewlett-Packard (HP) Laboratories: Cr(S-D)/ $\mu$ c-Si/ $\alpha$ -Si/SiN<sub>x</sub>/Al(G)/substrate [43]. Etching selectivity of the top and bottom metal layers is important because it ensures that one metal layer is less affected while another metal is etched. Gate isolation is required to improve device performance speed and reduce gate leakage current. This is achieved through a wet etching-induced undercut that completely removes the bottom metal with the narrowest dimension of the device (indicated by an arrow in figure 5(b)). It is desirable to have different etching properties between neighbor layers, i.e. a layer can be etched well in one process by the adjacent layers that are not. Other systems for 3D SAIL used by HP Labs are metal-oxide-semiconductor TFTs, for instance Cu(S-D)/IGZO/SiO<sub>x</sub>/Al(G)/polyimide [44]. The indium gallium zinc oxide (IGZO) semiconductor-based TFT is superior to  $\alpha$ -Si for SAIL manufacturing. It does not



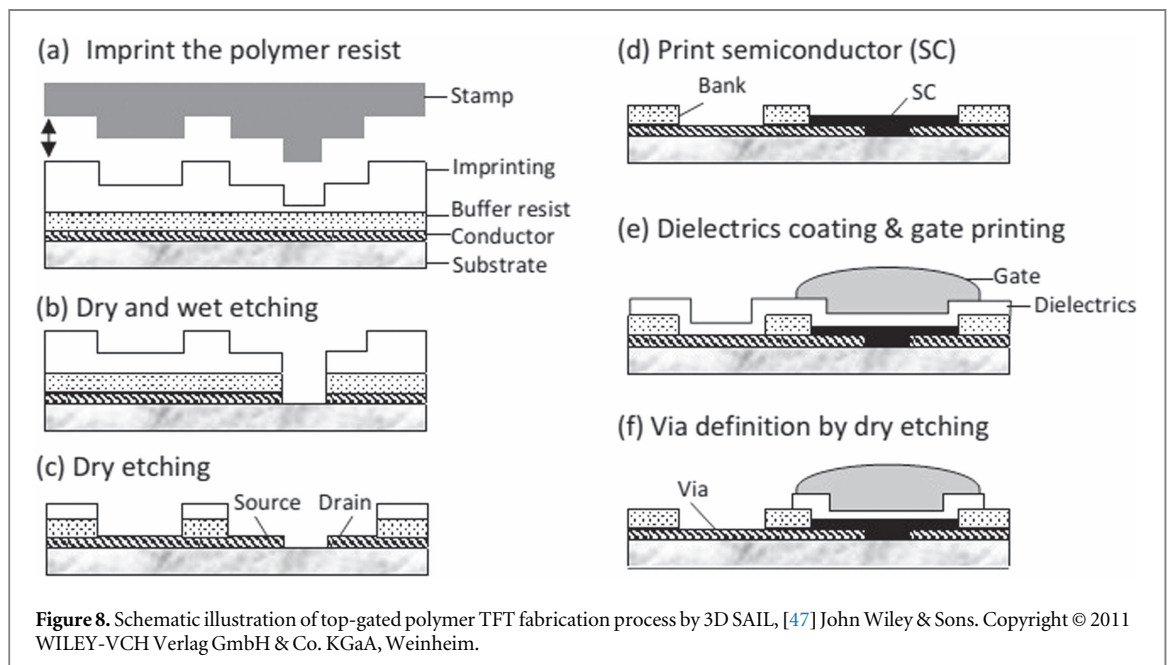
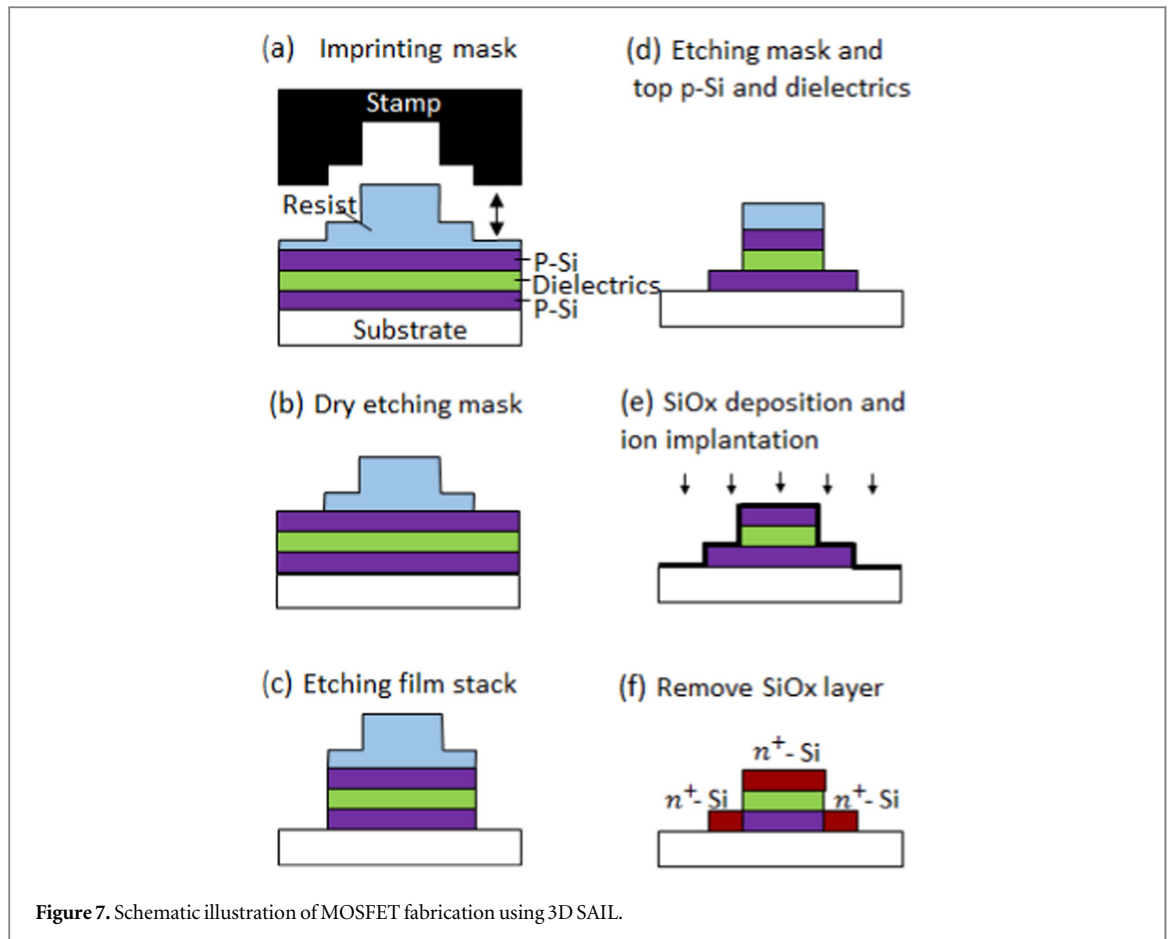


require an additional layer between the top metal and semiconductor layers, and it has better etching control because the oxide semiconductor is an excellent etching stop for the top metal.

Alternatively, top-gated transistors have been fabricated using the 3D SAIL proposed by Lausecker *et al* as schematically illustrated in figure 6 [45]. After a 3D polymer mask was created on a pre-deposited multi-layer film (semiconductor, dielectrics, and gate metal layer) (figure 6(a)) the layered stack was etched entirely using the imprinted 3D polymer as a mask (figure 6(b)). Then the mask was thinned by plasma etching to remove its lower level and partially expose the stack (figure 6(c)). Sequential etching was applied to etch the unprotected top metal and dielectrics to expose the bottom semiconductor layer (figures 6(d) and (e)). The source–drain electrodes were defined by selective alloying of the semiconducting layer (figure 6(f)). When  $\alpha$ -Si acts as the active layer, selective alloying was conducted by a blanket deposition of Ni followed by thermal treatment and dissolving the unreacted Ni [45]. The Ni reacts with Si to form Ni silicide at around 280 °C, which is compatible with many organic flexible substrates (Kapton & AryLite). The top-gated TFT has a simpler process than that used for bottom-gated TFTs with 3D SAIL. One embodiment of the thin-film stack for such top-gated TFT fabrication is Cr/SiNx/ $\alpha$ -Si/substrate.

Koo *et al* developed a polycrystalline silicon MOSFET fabrication process with 3D SAIL [46], which is illustrated in figure 7. Si/SiO<sub>2</sub>/p-Si was realized by thermal growth of SiO<sub>2</sub> on a silicon on insulator wafer and subsequent deposition of p-Si with low-pressure chemical vapor deposition. A 3D polymer mask was fabricated by UV-NIL (figure 7(a)). After removal of the residual polymer layer with O<sub>2</sub> plasma (figure 7(b)) the stack was entirely etched with HBr plasma (figure 7(c)). The top p-Si and SiO<sub>2</sub> layers were dry etched after the lower level layer of the mask was removed by O<sub>2</sub> plasma (figure 7(d)). A thin scattering SiO<sub>2</sub> layer was thermally evaporated (figure 7(e)) after dissolving the remaining polymer mask. Finally, source/drain/gate electrodes were defined by ion-implantation, thermal activation, and removing the scattering SiO<sub>2</sub> layer using diluted hydrofluoric acid (figures 7(e), (f)).

The repeated etching of the thin-film stack described above is not suitable for many materials, such as certain organic semiconductors highly sensitive to ion contamination. To address this problem there have been attempts to combine the merits of the 3D imprint and other patterning technology. For instance, 3D SAIL combined with inkjet printing offers high resolution patterning for both metal electrodes and organic semiconductors. Figure 8 illustrates a process developed by Li *et al* [47]. Buffer resist and imprinting resist layers were spin coated on a substrate with a pre-



deposited conducting layer. Then a 3D silicon stamp with a two-level structure fabricated by photolithography and dry etching was used to emboss the top polymer layer (figure 8(a)), and a plasma etching is followed to etch through the imprinted deeper trench. Next, wet etching was conducted to define the TFT channel in the conducting layer using the resist as a

mask (figure 8(b)). Plasma etching was further applied to etch through the shallow trench in the mask to expose the source–drain electrodes with predesigned dimensions (figure 8(c)), while banks for inkjet printing of semiconductor material were defined after removing the remaining imprinting resist with solvent. A philic/phobic contrast between banks and the



electrode/substrate was created by surface treatment, and then a semiconductor material was deposited by inkjet printing (figure 8(d)). A dielectric layer was then spin coated and a gate electrode was printed to complete the TFT fabrication (figure 8(e)). For circuit fabrication an additional plasma etching can be applied to open inter-device connection, while the semiconductor and a portion of dielectric layers are protected by the gate electrode (figure 8(f)). It is possible to define banks by the imprinting resist without using the buffer layer. In this case, the selection of the imprinting resist is crucial because it must be easy to imprint and robust enough to endure subsequent processing. The insertion of a buffer layer is a simple way to avoid the difficulty of bank material selection. Polystyrene (PS) and polymethylglutarimide (PMGI) were used as the imprinting and buffer resists. The PS top layer has a relatively low glass-transition temperature, which is favorable for imprinting. The PMGI film, with a high glass-transition point is thermally stable when imprinting the PS layer. The PMGI layer was spin coated on an indium tin oxide-coated substrate and subsequently baked. Then, a PS layer was spun from a toluene solution on the PMGI film and baked. The PS layer was imprinted to form a 3D mask (figure 8(a)). After entirely etching through the deep trenches by  $O_2 + CF_4$  gas mixture plasma, the ITO was etched using commercial ITO etchant to define the TFT channel using the PMGI resist as an etching mask (figure 8(b)). The imprinted shallow trenches were transferred onto the ITO by plasma etching to define source and drain electrodes (figure 8(c)), and the remaining PS was removed in toluene.  $CF_4$  plasma treatment was used to create a philic/phobic contrast between the PMGI banks and ITO, and a 50 nm thick poly (9,9-dioctylfluorene-co-bithiophene) (2008P) semiconductor material was inkjet-printed between the PMGI banks (figure 8(d)). Finally, the TFTs were completed by spin coating the poly(methyl methacrylate) (PMMA) dielectric layer and inkjet printing the gate electrode using a poly (3,4-ethylenedioxythiophene): poly (styrenesulfonate) (PEDOT:PSS) water suspension (figure 8(e)). To increase the gate printing resolution several-nanometer-thick polyvinylphenol was spin coated on the surface of the PMMA before PEDOT:PSS printing. Figure 9(a) shows ITO electrodes with PMGI banks aligned on them, which confines the inkjet-printed semiconductor. Figure 9(b) shows the performance of a TFT fabricated by this method.

3D SAIL has also been used to fabricate transistors with source-drain electrodes with different work functions for integrating both p- and n-type transistors to form CMOS-like circuits. The fabrication process [48] is illustrated in figure 10. Two conductive layers with high and low work function were pre-deposited on a substrate. A polymer resist layer was spin coated on the conductive films. Then, a stamp was brought to imprint the resist to form a 3D polymer

mask (figure 10(a)). Subsequently, plasma etching was applied to etch through the bottom of the imprinted trench entirely, followed by wet (or dry) etching to define the TFT channels in the conductive layers by using the resist as the etching mask (figure 10(b)). Plasma and wet etching were applied again to expose one pair of source-drain electrodes and to remove the top conductive layer of this pair of electrodes (on the right side of figure 10(c)).

Plasma etching was applied once again to expose another pair of electrodes (left side of figure 10(d)). Thus, two pairs of electrodes with high and low work functions were defined, which is essential for the hole and electron injection into p- and n-channels, respectively. Both p- and n-type semiconductors were deposited by inkjet printing (figure 10(e)). Finally, fabrication was completed by spin coating a dielectric layer, followed by inkjet printing the gate electrodes (figure 10(f)). As an example, titanium (30 nm) and gold (100 nm) layers were deposited on a glass substrate by sputtering. They were chosen to be the conductive layers because the values of their work functions (Au: 5.2 eV, Ti: 4.3 eV) favor hole and electron injection into the p- and n-type semiconductors, respectively. Furthermore, the Ti layer acts as an adhesion layer for the Au film. PMMA was used as the resist for imprinting while PMGI was chosen as a buffer polymer layer (same reason as in figure 8). The PMGI layer is thermally stable ( $T_g \sim 205^\circ$ ) during imprinting, and is robust enough to resist the solvent attack during the subsequent solution processing. A PMGI and PMMA layer were spin coated in turn on top of the Au/Ti films, and baked. The PMMA was imprinted using a silicon stamp at  $160^\circ C$ . After entirely etching through the deep trenches by plasma ( $O_2 + CF_4$  gas mixture) the Au/Ti were etched sequentially in gold etchant ( $KI:I_2:H_2O = 4:1:200$ ) and 1%HF aqueous solution to define the TFT channel with the polymer resist as the etching mask. Plasma etching was further applied to expose the Au and a wet etching was followed to remove the top Au layer in order to define the Ti electrodes for n-channel TFTs. Plasma etching was applied again to expose the Au electrodes for definition of p-channel TFTs. The remaining PMMA was then removed by acetone and PMGI was left as the banks to confine the printed semiconductor. Both p- and n-type semiconductor polymers, poly(3,3'-dialkylquaterthiophene) (PQT-12) and {poly {[N,N0-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,50-(2,20-bithiophene)}} (P(NDI2ODT2)), were inkjet-printed from 1,2-dichlorobenzene solutions. After baking the printed semiconductors at  $110^\circ C$  for 4 h and  $140^\circ C$  for 20 min, a PMMA dielectric layer was spin coated and dried at  $90^\circ C$  for 30 min. Finally, PEDOT:PSS aqueous suspension was inkjet-deposited for the gate electrodes. Figure 11 shows an image of a 3D silicon stamp (figure 11(a)) and two pairs of electrodes made with Au and Ti (figure 11(b)), while figure 12 displays

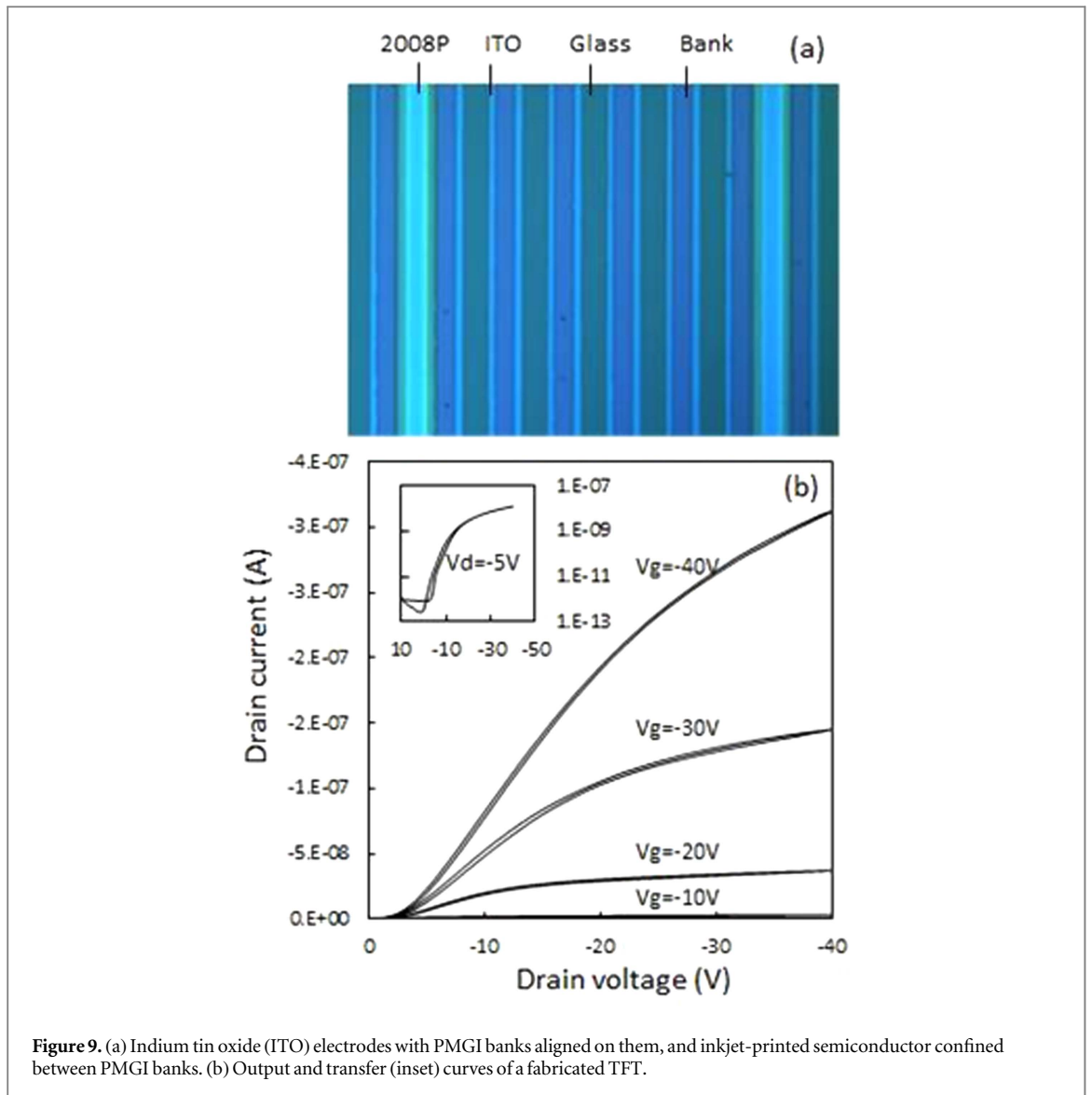


Figure 9. (a) Indium tin oxide (ITO) electrodes with PMGI banks aligned on them, and inkjet-printed semiconductor confined between PMGI banks. (b) Output and transfer (inset) curves of a fabricated TFT.

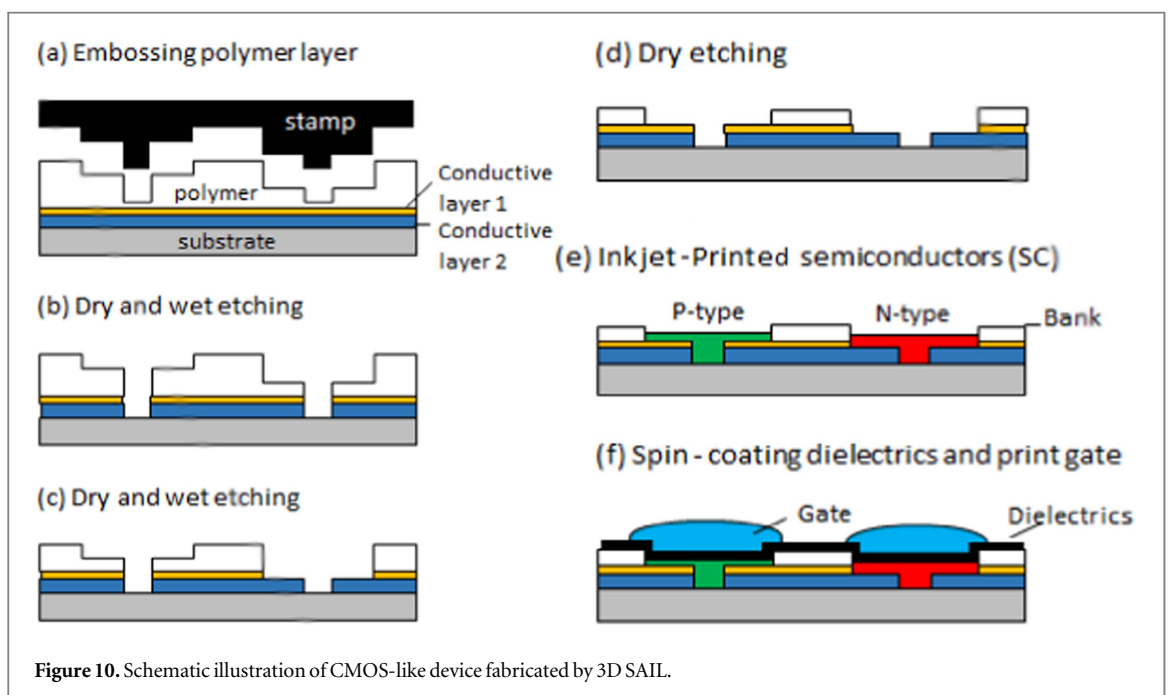
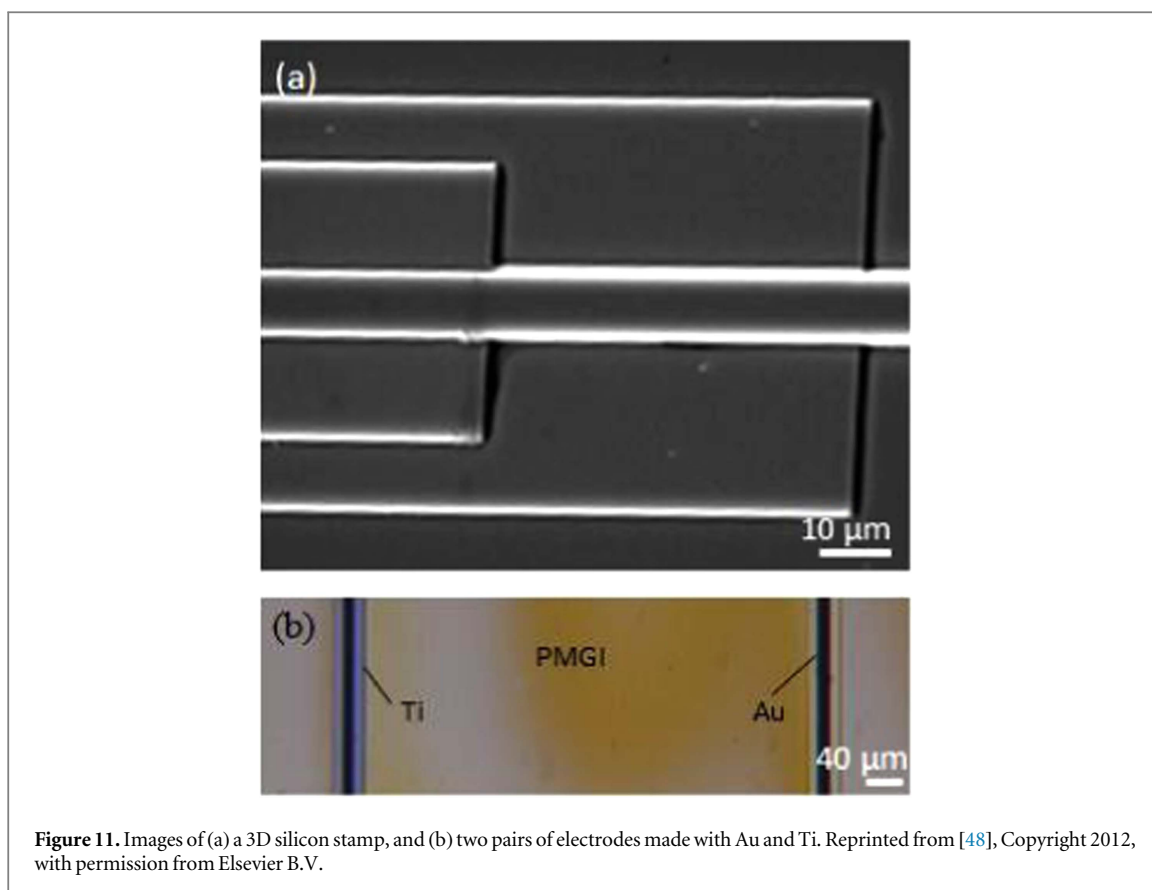
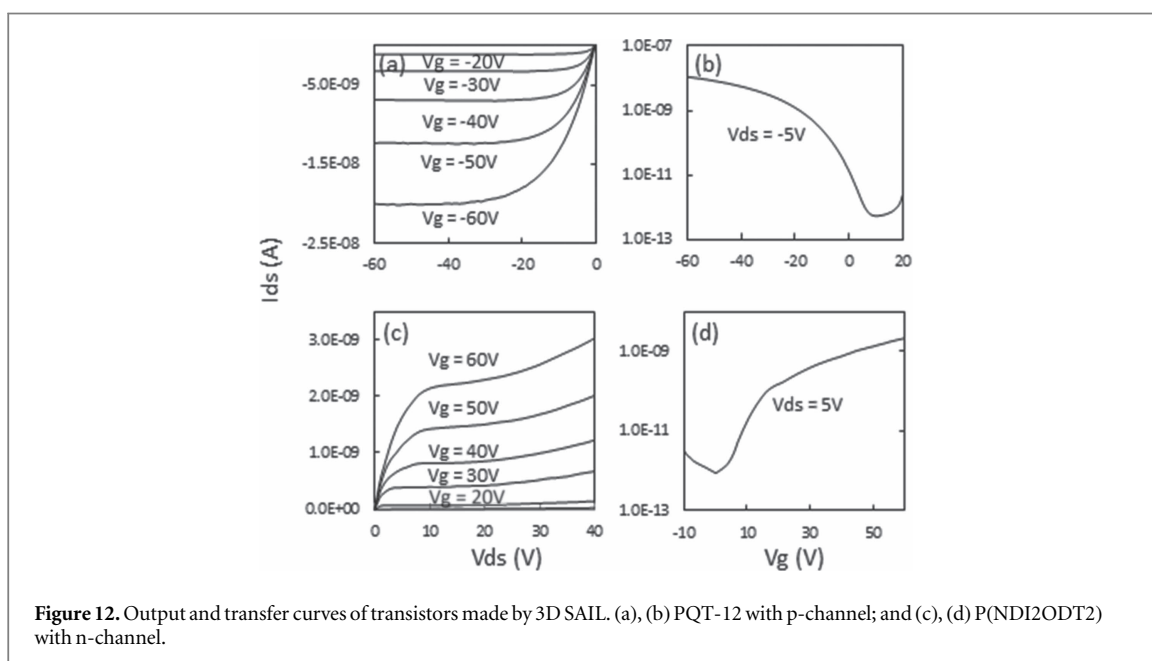


Figure 10. Schematic illustration of CMOS-like device fabricated by 3D SAIL.



**Figure 11.** Images of (a) a 3D silicon stamp, and (b) two pairs of electrodes made with Au and Ti. Reprinted from [48], Copyright 2012, with permission from Elsevier B.V.

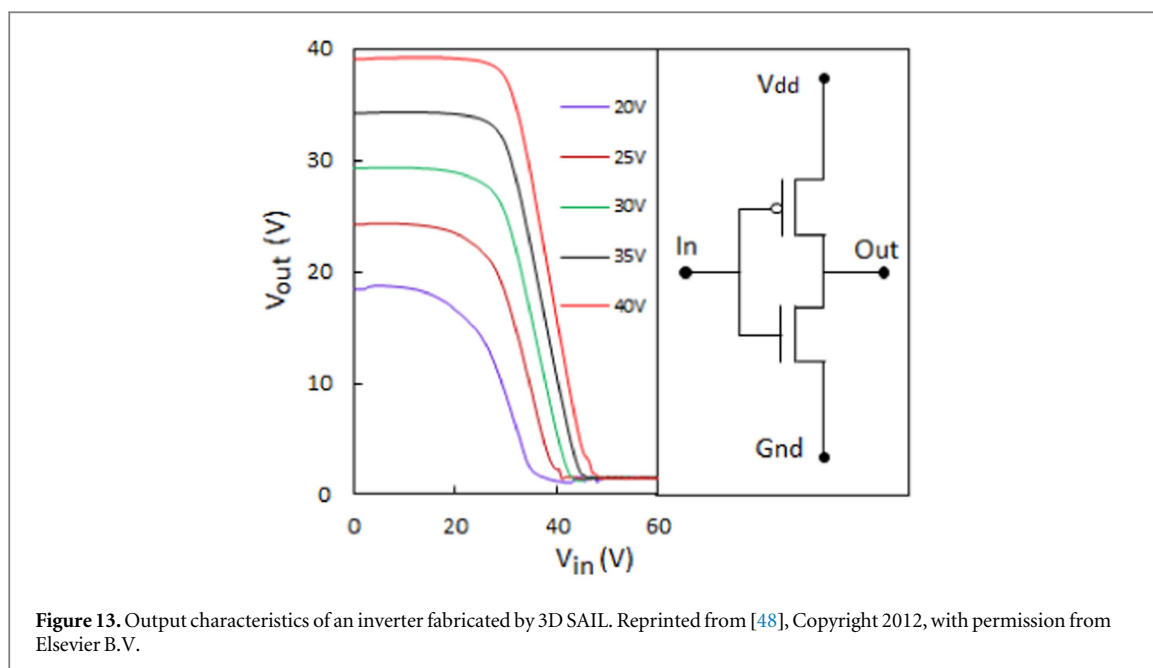


**Figure 12.** Output and transfer curves of transistors made by 3D SAIL. (a), (b) PQT-12 with p-channel; and (c), (d) P(NDI2ODT2) with n-channel.

output and transfer curves of both PQT-12 (figures 12(a), (b)) and P(NDI2ODT2) (figures 12(c), (d)) transistors. Output characteristics of an inverter fabricated by this process are shown in figure 13.

Qin *et al* developed a process to fabricate bottom-gated organic transistors using 3D SAIL combined with inkjet printing (figure 14) [49]. Polyethylene naphthalate (PEN) foil is temporarily bonded to a rigid substrate. A thin SU8 resist was spin coated to reduce

the PEN surface roughness. The bottom gate conductor, dielectrics, and top conductor layers were sequentially defined by sputtering Al, anodization, and sputtering Au/Cr. Then a layer of mr-I7030R imprinting resist was spin coated (figure 14(a)) and a 3D resist mask was imprinted using a Ni 3D stamp (figure 14(b)). The mask was thinned by  $O_2$  plasma and both metal layers and dielectrics were etched (figure 14(c)). The resist mask underwent plasma



etching until the bottom level was removed, and subsequent wet etching was applied to define interdigital source–drain electrodes (figure 14(d)). After removing the remaining resist mask by solvent 6,13-bis(triisopropylsilylethynyl) pentacene, the semiconductor, was printed over the source–drain electrodes to finish TFT fabrication (figure 14(e)).

Fabrication of electronics with bottom-up 3D SAIL was developed at Holst Center in the Netherlands. Here, a primary 3D structure with a secondary patterned micron structure were embossed, and materials were deposited selectively from solution onto a micro-structured area by the capillary effect [50, 51]. 3D SAIL technology development has also been conducted by several other research teams with various end-goals, such as establishing interconnections in printed circuit boards [52], and metallizing fine metal structures [53].

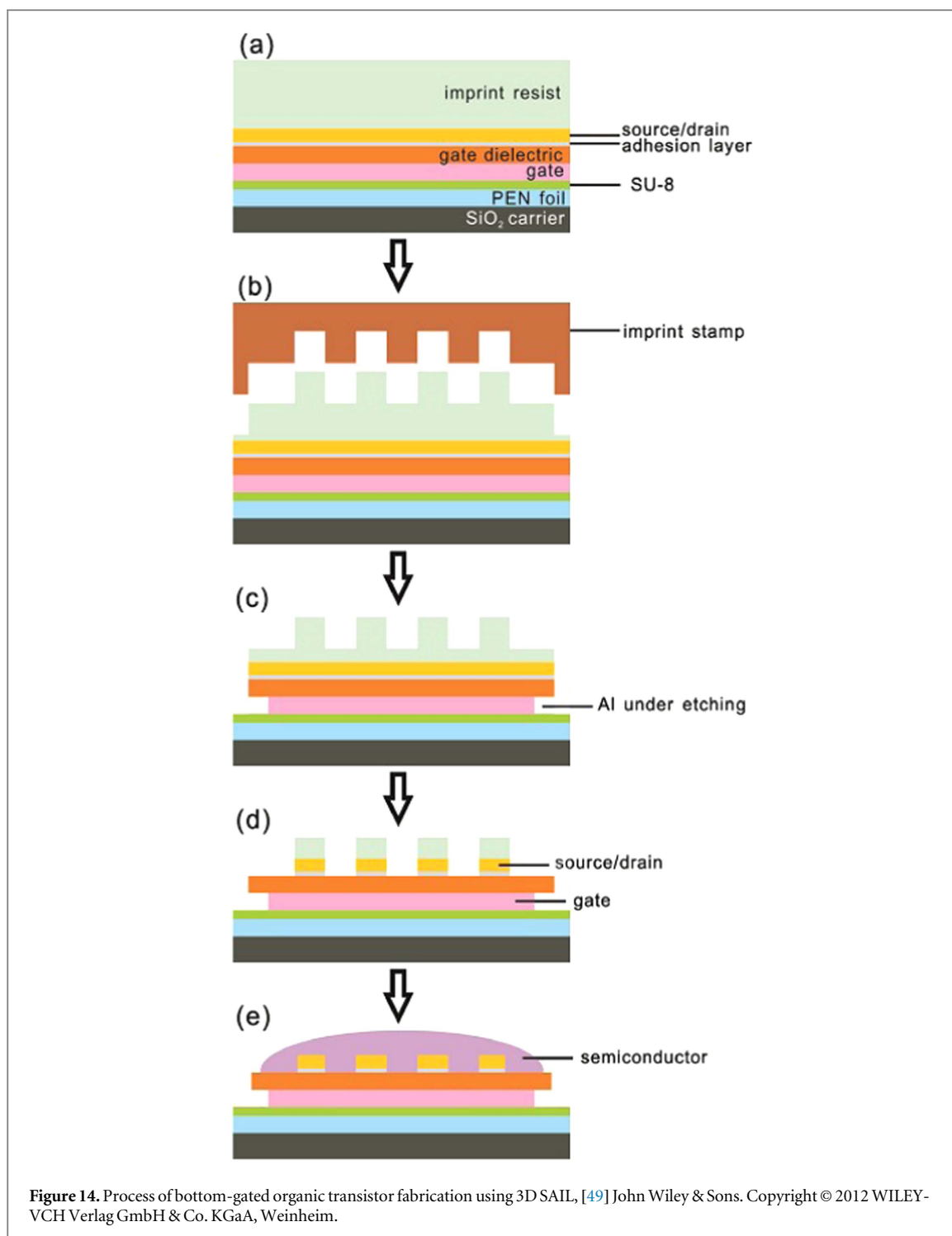
2D imprinting has also been used to achieve self-alignment in the fabrication of organic TFTs. Stadlober *et al* developed self-aligned fabrication of organic TFTs by combining NIL with a backside light exposure technique to achieve minimal electrode overlap [54–56]. A narrow metal gate electrode was defined by NIL and subsequent pattern transfer. Then dielectrics and photoresist layers were spin coated and exposed with backside light. Source–drain electrodes were defined by subsequent photoresist development and lift-off. Finally, a semiconductor was deposited over the source–drain electrodes. Li *et al* combined 2D imprinting with inkjet printing to define gate and source–drain electrodes to achieve self-alignment [57]. Gate electrodes capped on the ridges of polymer insulator stripes were defined by thermal imprinting, subsequent lift-off of metal, and dry etching.

After spin coating PMMA dielectrics, PEDOT:PSS was inkjet-printed into grooves next to the gate. A

polymer semiconductor was spin coated over the source–drain electrodes to complete TFT fabrication. Although the 2D imprint is relatively easy to implement it is difficult to pattern all TFT components, and additional low-resolution patterning is required for circuit fabrication. Table 1 summarizes the several representative 3D imprint processes reviewed in this paper. One can see that the main factor to limiting patterning resolution is wet etching, due to the metal layers involved. Dry etching-compatible conductors, like highly doped Si and conductive polymers, is a better choice for very high resolution patterning.

## 5. Conclusions

Imprinting lithography has attracted wide attention for the fabrication of various types of materials and devices. Depending on the type of imprinting contact, NIL techniques can be classified into three types: plate-to-plate, roll-to-plate, and roll-to-roll NIL. The roller-based processes, particularly roll-to-roll NIL, is highly promising for large-scale manufacturing of flexible electronics. To address the challenge of inter-layer alignment for the fabrication of devices/circuits with structured multi-layers, a 3D SAIL technique has been developed where all the information of device dimensions is coded in a 3D imprint-defined mask. The information coded on the mask is subsequently transferred into functional layers of devices by sequential etching. The imprinted 3D mask that deforms together with the flexible substrate ensures that all layers of devices are perfectly aligned and patterned with high resolution during manufacturing, which permits the fabrication of complementary TFTs with a single-step self-aligned patterning. Recent development and availability of necessary relevant roll-to-roll techniques including roll-to-roll film coating, roll-to-



**Table 1.** Summary of the potential resolution of the main 3D imprint processes reviewed.

Developers	Potential channel resolution	Edge definition	Process that limits resolution
HP	0.5 $\mu\text{m}$	0.2 $\mu\text{m}$	Wet etching
Princeton Linz	0.5 $\mu\text{m}$	0.2 $\mu\text{m}$	Wet etching
AMO GmbH	0.1 $\mu\text{m}$	50 nm	Imprinting
Cambridge Tyndall	0.5 $\mu\text{m}$	0.2 $\mu\text{m}$	Wet etching
NTO/IMEC/CUT	0.5 $\mu\text{m}$	0.2 $\mu\text{m}$	Wet etching

roll plasma/wet etching, etc, have laid a strong foundation for the success of the 3D SAIL technique.

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