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Single Event Effect Testing of the Micron MT46V128M8

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Introduction

The Micron MT46V128M8 was tested for single event effects (SEE) at the Texas A&M University Cyclotron Facility (TAMU) in June of 2017. Testing revealed a sensitivity to device hang-ups classified as single event functional interrupts (SEFI) and possible soft data errors classified as single event upsets (SEU). SEFIs occurred so frequently as to make identification of SEUs difficult.

To mitigate some of the risk posed by single event latch-ups, circuitry was added to the electrical test setup design to detect a high current event and manually cycle the power and reboot the device. This was ultimately not needed as no single event latchups (SEL) were seen.

Devices Tested

MT46V128M8 (DDR) Background

The MT46V128M8 is a single-chip, 1 Gb DDR SDRAM memory. The devices tested are packaged in a 66-pin plastic thin-shrink small outline package (TSSOP) with gold bond wires bonded to a lead frame overlaying the majority of the die (see Figure 1). Further details on the device function, organization, and possible applications can be found in the full datasheet[1].

Device Under Test (DUT) Preparation

A number of devices were prepared from two pre-selected Lot Date Codes (LDC). Table 1 lists the pertinent DUT information.

Table 1. MT46V128M8 Test Information

Part Number:	MT46V128M8
Manufacturer:	Micron
Lot Date Code:	0830 and 1012
Quantity Tested:	2
Part Function:	DDR SDRAM
Part Technology:	CMOS
Package Style:	66 TSSOP
REAG Identification	16-019, 16-020

A Nisene JetEtch machine[2] was used to de-encapsulate the plastic package and expose the silicon die for irradiation. This was a difficult process due to the fragility of the wirebond connection to the pad frame. A mixture of Nitric and Sulfuric acid was used at approximately 90˚C until a portion of die was exposed. Devices were tested for functionality after de-encapsulating and due to the aforementioned fragility, yield was low. Wire bonds at the pad frame were broken during the de-encapsulation and can be seen in Figure 1. The conclusion drawn was that the acid was eroding the pad frame beneath the bond wires and breaking the bonds.

After multiple part failures in pre-testing and adapting the process, a process where a minimum of encapsulant removal reduced wire bond failure and produced functioning parts. One of the test

parts, DUT #1, can be seen in Figure 2. It should be noted that, due to intervening plastic and to some extent the pad frame, a large portion of the die is not able to be upset by the ion beam. After post-prep testing, four devices were deemed acceptable for evaluation.

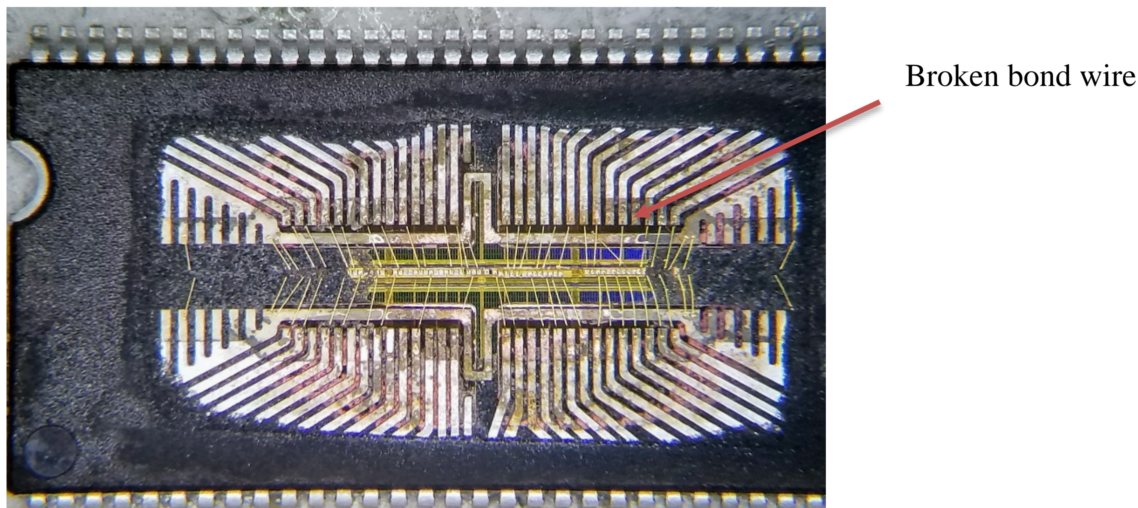


Figure 1: DUT showing pad frame and broken bond wire

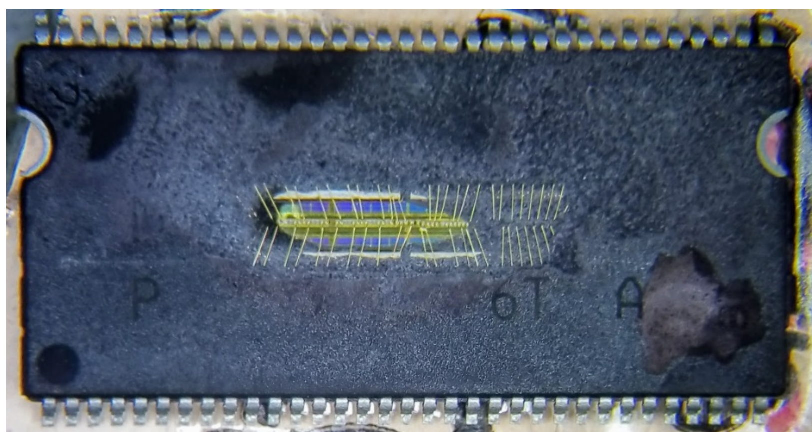


Figure 2: Limited, functional, de-encapsulated (DUT #1) part as tested

Test Method

Test Description

Temperature: Room temperature
Monitored Test Voltages: 5.0V (Spartan 3A board voltage), 2.5V (DDR 2.5 and 1.25V supplies)

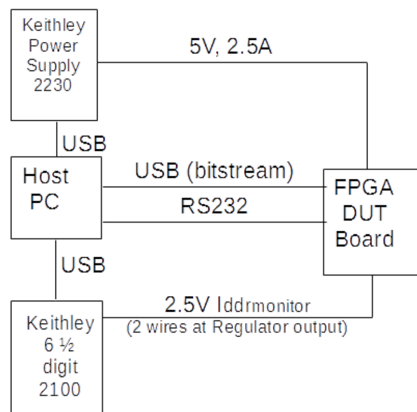
Two types of tests were used during the test run, dynamic and static. The dynamic test run consisted of writing and reading the DDR memory in 100, 32-bit word block increments during irradiation by the heavy ion beam. Dynamic runs 61 and after are write once with the ion beam off and read continuously with the beam on. The Spartan 3e firmware limited the reporting of

errors to the first 100 erroneous 32-bit words for both types of test. Bit errors were accumulated and reported for these 100 words. Later runs, after run 49, had this limit removed for Static testing.

Static test runs consisted of writing the DDR memory, irradiating with the heavy ion beam, and then reading. Power was cycled between runs to resolve SEFIs and ensure a good memory initialization. The test setup and a picture of the DUT in the beamline are shown in Figure 3. The DUT is mounted in a socket mounted to the Spartan-3e FPGA board via an interposer board required to match pins between the board and the DUT. The Spartan-3e board firmware implements a Microblaze processor and a MT46V64M16 memory controller. For this reason, only the odd order bytes in a 32 bit access are valid.

Error Detection

Three types of errors were detected by the test hardware: errors at single addresses, sequential errors, and sequential errors with a 4k address spacing. With the exception of single address errors that resolved without an intervening power cycle, most of the errors are categorized as single-event functional interrupt (SEFI). No high-current single event latch-ups (SEL) were seen during the test runs.



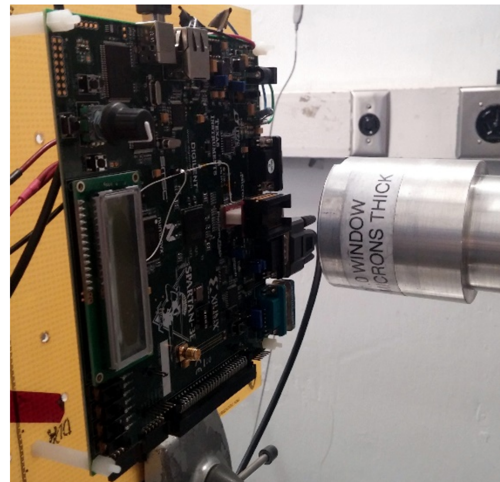


Figure 3: Test setup

Error Recovery

Both Static and Dynamic test runs show error recovery was at least possible when single address errors occurred, but due to the firmware ending the collection of errors after the first 100 word errors, this is difficult to confirm. Sequential address and 4k spaced errors were determined to be SEFIs and required power cycling to correct.

Test Facility

Heavy-ion testing was performed at the Texas A&M University Cyclotron Facility (TAMU), using their K500 cyclotron at the 15 MeV/amu tune. The following ions were used for this test:

Table 1: Ions used

Ion	Effective LET ($MeV*cm^2/mg$) After 1mil Aramica and40mm air
N	1.3-1.4
Ne	2.7-3.1
Ar	8.4-10
Cu	19.9
Kr	28.3-34.9

Flux: Testing was conducted with the fluxes between $5x10^3$ particles/cm^2/s and $5x10^4$ particles/cm^2/s, with the majority of tests at the lower end of the range.

Fluence: Fluences ranged from $3x10^3$ particles/cm^2 up to $1x10^7$ particles/cm^2. The highest fluence occurred at the end of testing of DUT #1 to rule out single event latchup (SEL).

Results

Single Event Latch-up

Single event latch-ups (high current events requiring a power cycle and device reset) were not observed.

Other single event effects

Single event upsets were reported via serial interface at 115200 baud for memory mismatches from the pre-programmed 32-bit pattern 0xAA00AA00. SEFIs requiring a power cycle to resolve were observed at each LET and generally masked any underlying single bit errors that occurred during testing. Post processing of the logs showed some limited reporting of single address upsets, but it is difficult to draw conclusions due to the large amount of SEFIs and the small window of beam exposure. Therefore, only SEFI cross sections were analyzed. The data from the processed run log is shown in Table 2 below. Figure 4 plots the cross section of SEFI onset vs. LET for the two parts tested and shows a Weibull fit (red line) of the estimated SEFI cross section with parameters A = 3.069, B = 1.28×10^{-4}, C = 0.89, and D = 200.

Table 2: SEFI cross section data (from TAMU_RESTORE_DDR_JUNE_2017_Runlog_Final_Corrected.xlsx)

Run #	DUT #	Eff. LET	SEFI CS	LET Avg	SEFI CS Avg	CS StdDev	CS - StdDev	CS + StdDev	CS min	CS max
38	1	3.1	2.6E-07	3.1	4.7E-07	4.7E-07	-4.0E-09	9.4E-07	1.3E-07	1.0E-06
39	1	3.1	1.0E-06							
40	1	3.1	1.3E-07							
34	1	3.6	1.0E-06	3.7	7.3E-07	4.2E-07	3.1E-07	1.1E-06	1.5E-07	1.3E-06
35	1	3.6	1.5E-07							
36	1	3.6	1.3E-06							
37	1	3.6	9.8E-07							
25	1	3.8	4.0E-07							
27	1	3.8	5.8E-07							
9	1	8.4	5.0E-06	8.4	7.4E-06	2.5E-06	4.9E-06	9.9E-06	5.0E-06	1.0E-05
12	1	8.4	7.1E-06							
13	1	8.4	1.0E-05							
14	1	11.5	6.9E-06	11.5	6.4E-06	7.8E-07	5.6E-06	7.2E-06	5.8E-06	6.9E-06
15	1	11.5	5.8E-06							
22	1	14.1	9.1E-06	14.1	7.5E-06	3.3E-06	4.2E-06	1.1E-05	3.7E-06	9.7E-06
23	1	14.1	9.7E-06							
24	1	14.1	3.7E-06							
63	2	19.9	1.2E-04	19.9	6.4E-05	4.9E-05	1.4E-05	1.1E-04	3.3E-06	1.2E-04
64	2	19.9	5.8E-05							
65	2	19.9	6.9E-05							
67	2	19.9	3.3E-06							
57	2	34.9	2.4E-05	34.9	8.6E-05	1.2E-04	-3.3E-05	2.1E-04	1.1E-05	2.2E-04
58	2	34.9	1.1E-05							
62	2	34.9	2.2E-04							
54	2	40.0	3.9E-06	40.1	1.3E-04	1.6E-04	-3.3E-05	2.9E-04	3.9E-06	3.5E-04
55	2	40.0	2.5E-05							
56	2	40.0	1.5E-05							
60	2	40.3	2.4E-04							
61	2	40.3	3.5E-04							

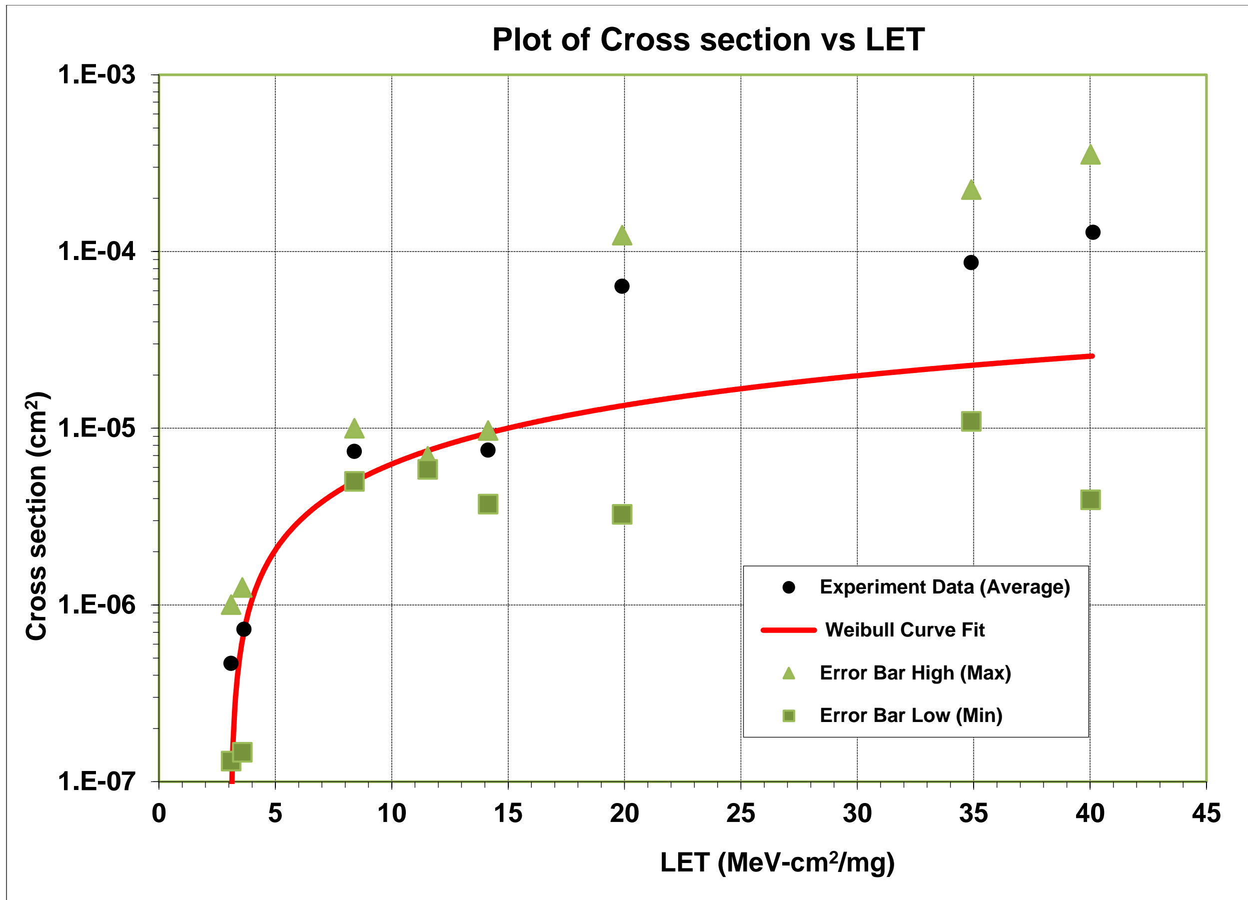


Figure 4: SEFI Cross section vs. LET (*Weibull fit parameters A = 3.069, B = 1.28 x 10^{-4}, C = 0.89, and D = 200*)

Conclusions

This part proved challenging to evaluate. A memory controller to match the part was not commercially available and had to be adapted from a similar, but mismatched part. Due to pin mismatches, a hardware interposer was also required for the test to match pins to the memory controller adaptation. The memory controller and hardware limited the memory array available for testing to 25% of the actual array. The part die was overlaid by a bond pad frame that further limited incident radiation to a fraction of the die. Finally, difficulties with de-encapsulating the die limited that actual affected area further.

Regardless of the above, upsets were seen in the two parts tested and a bounding of the SEFI sensitivity of the part can be estimated. From the plot above, SEFI cross section can be estimated to be less than ~$5x10^{-4}$ cm^2.

References

(1) https://www.micron.com/~/media/documents/products/data-sheet/dram/ddr1/1gb_ddr.pdf
(2) http://www.nisene.com/jetetch-pro

Run Log

See TAMU_RESTORE_DDR_JUNE_2017_Runlog_Final_Corrected.xlsx