# Two Timing Samplers

Edward H. Frank
Robert F. Sproull

Department of Computer Science
Carnegie-Mellon University
Pittsburgh, PA 15213

## Abstract

Testing VLSI chips presents a variety of problems, some of which can be solved by building *on-chip* testing structures. On-chip testing structures can allow a designer to test aspects of a circuit which might be difficult to test even with expensive test equipment and moreover can provide reasonable testing hardware to designers who do not have access to sophisticated off-chip testing equipment.

In this paper we describe a type of on-chip test structure called a *timing sampler* which enables the designer to accurately measure when on-chip signal transitions occur. The timing samplers we present are simple. They have been fabricated as part of a multi-project chip and experimental results show that they are reasonably accurate as well.



This research was sponsored by the Defense Advanced Research Projects Agency (DOD), ARPA Order No. 3597, monitored by the Air Force Avionics Laboratory Under Contract F33615-78-C-1551.

The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the US Government.

## 1 Introduction

As VLSI chips become increasingly complex designers are discovering that testing and debugging must be considered in the overall chip design. As a result, testing mechanisms such as scan-in/scan-out (often called shift-register latch (SRL) or level-sensitive scan design (LSSD) [Eichelberger 78]) for accessing internal state and on-chip signature analysis [Frohwerk 77] such as BILBO [Koenemann 79] are becoming more common. In this paper we describe another type of on-chip testing mechanism which is useful for measuring some aspects of circuit performance.

When assessing the performance of a circuit, it is often important to measure the time of occurence of an on-chip signal. For example, to measure the performance of an adder design, the designer wants to know when the carry signal arrives at the end of the carry chain. The simple expedient of connecting the signal to an output pad driver and measuring the arrival time off-chip is inadequate because a long unknown delay is introduced by the pad driver.

An accurate measurement of the time behavior of a signal could be obtained if we could build an on-chip digital oscilloscope, capable of measuring the signal value at all points in time. We present two circuits for making such measurements in a limited way. The first is a simple latch, which records the value of the signal when a timing signal arrives from off-chip. The second, a C-element, can determine the time at which a single transition appears on the signal to be tested. An additional advantage of the second scheme is that it requires exactly one pad to accomplish the test. Note that the time required to drive the input pad used by the timing signal does not significantly effect the results.

## 2 Latch sampler

A latch can be used to sample the value of a signal under the control of an externally-generated timing signal. We fabricate a latch near the place where the signal to be tested is generated (Figure 1). Signal **T** is the one being tested; **L** is a timing signal generated off-chip; and **R** communicates the result of the test for off-chip analysis. This circuit samples the signal **T**, using the latching signal **L** to determine the time at which the sample is to be taken. **L** is normally high; it is lowered at the instant we want to take a sample (Figure 2). The latch is thereafter closed, with a feedback path ensuring static stability. A complete trace of the behavior of **T** is obtained by repeating the experiment many times, varying the time at which **L** is lowered.

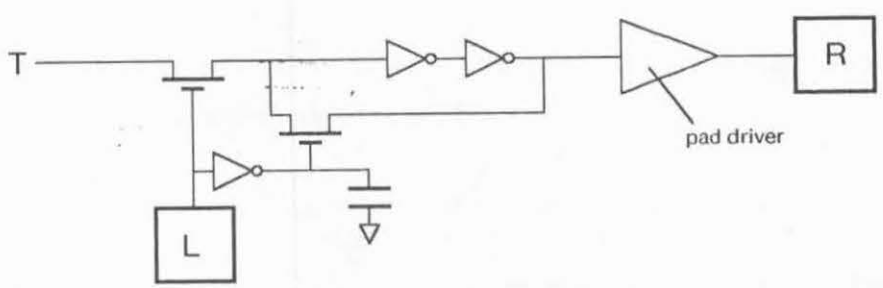


**Figure 1:** Latch Sampler.

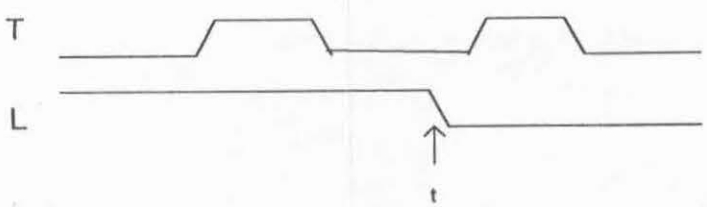


**Figure 2:** Operating the latch sampler. *t* represents the approximate time of the sample of **T**.

Proper operation of this circuit requires some attention to its design. When **L** is lowered, the pass transistor opens, preventing further change of the charge on the gate of the first inverter of the latch. Note that the gate may be neither fully charged to Vdd nor fully discharged to ground. We now allow the signal to propagate through the latch inverters, and then close the feedback pass transistor. (For this reason, the pullup time of the inverter that inverts **L** to drive the feedback pass transistor gate is arranged to be quite long, substantially longer than the propagation delay through the latch. The pullup time is slowed with a large diffusion-to-substrate capacitor.) After the feedback pass transistor closes, the latch may remain in a metastable state for some time. After allowing sufficient time for metastable exit and delay through the pad driver, we measure the result of the test by sensing pad **R**.

## 3 C-element sampler

The second scheme for measuring timing uses a C-element[1] as shown in the circuit Figure 3. The use of this scheme is illustrated in Figure 4, which shows a test to determine the time at which the signal **T** rises. **L** is initially low, to insure that the C-element is set to zero. **L** is then raised for a while, and lowered at a known time *t*. If *t* precedes the rise of **T**, the C-element will remain zero; if *t* follows the rise of **T**, the C-element will be set to one. The results of the experiment are observed on the output pad **R**. The experiment to detect a falling transition on **T** is the symmetric opposite of the one described above (i.e., **L** is simply the complement of the signal shown in Figure 4.)

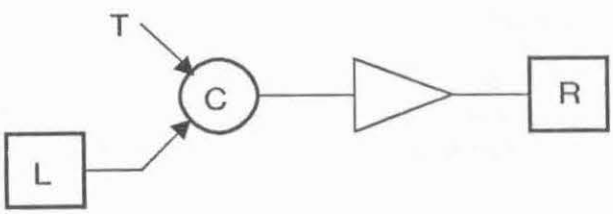


**Figure 3:** C-element timing sampler.

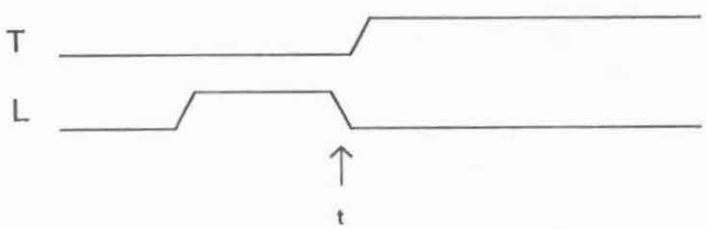


**Figure 4:** Operating the C-element sampler.

A trick allows us to economize on pads, using a single pad **LR** to communicate both the **L** signal and the results of the test (Figure 5). During the first phase of a test, **LR** is driven from off-chip with the signal shown for **L** in Figure 4. Then the external drive is removed (e.g., by driving **LR** with a tristate driver), and we now detect the results of the experiment by observing whether pad **LR** is high or low. The trick is that although **LR** may change state when the drive is removed, the C-element will not change state. For example, if **LR** is low,

[1] A C-element "... is a bistable device that provides an action similar to hysteresis, in that its output becomes 1 only after *all* of its inputs are 1, and becomes zero only after *all* of its inputs are zero." [Seitz 80]

and the C-element output is high, removing the drive will cause the pad to become high by charging through the resistor, which leaves the C-element high.

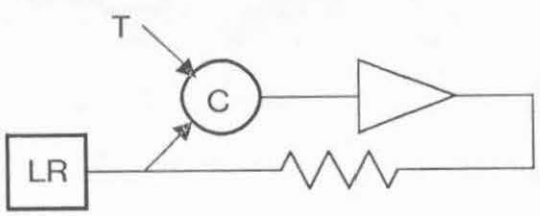


**Figure 5:** Using a single pad **LR** for both **L** and **R**.

## 4 Experiments

We have designed and had fabricated a project (as part of two different multi-project chips, MPC580 and M08B) to test these circuits. The circuit diagrams and layouts are shown in Figures 6 and 7. In addition to testing the ideas mentioned in this paper, the project also provides a conventional C-element for various uses (inputs on **T** and **LR**; output on **C**). The circuit diagram of the jig for testing these projects is shown in Figure 8. Basically, we use the variable width pulse generator running at one-half the frequency of the free-running oscillator to vary where the edge of **T** occurs relative to the edge of **L** or **LR**. The **R** and **C** outputs are used to measure the results for the latch and C-element respectively.

As previously mentioned the circuits were fabricated two separate times. Due to a minor mistake[2] the MPC580 version of the chip had a non-functional latch sampler. This error was fixed in the M08B version. The C-element sampler worked in both versions of the chip. We statically tested that the **LR** pin worked as both **L** and **R**. To simplfy the test jig, however we, used the **C** output in the dynamic tests.

Figure 9 and Table 1 summarize our results. Although we tested both versions of the C-element, the results were almost identical and so only one set of figures is shown. As can be seen, the latch sampler performed extremely well, with a jitter of at most two nanoseconds. The C-element was not nearly as satisfactory. While the jitter was about the same as the latch, the internal switching delay of the flip-flop caused two problems. First, because of an asymmetry in the C-element, the delay was much greater for the high-to-low C-element transition than for the low-to-high transition. Second, because this delay was much greater than the precision with which we would like to be able to measure signals and moreover because it will vary from fab run to fab run, it makes the C-element as designed here not particularly useful to make accurate timing measurements.

While not shown here, experiments such as measuring the effects of supply voltage and temperature on the timing sampler should also be performed. In addition, Puri [Puri 77] has used a similar form of timing sampler for measuring the minimum pulse width required to disturb a latch.

## 5 Pad Considerations

One objective of any on-chip testing scheme is to minimize the number of pads devoted exclusively to this purpose. The latch scheme seems at first glance to require two pads for each signal, one for **L** and one for R. However, a single latching signal **L** could be used to control several latches; this allows us to sample *n*

[2]Forgetting to wire the **R** pad to ground.

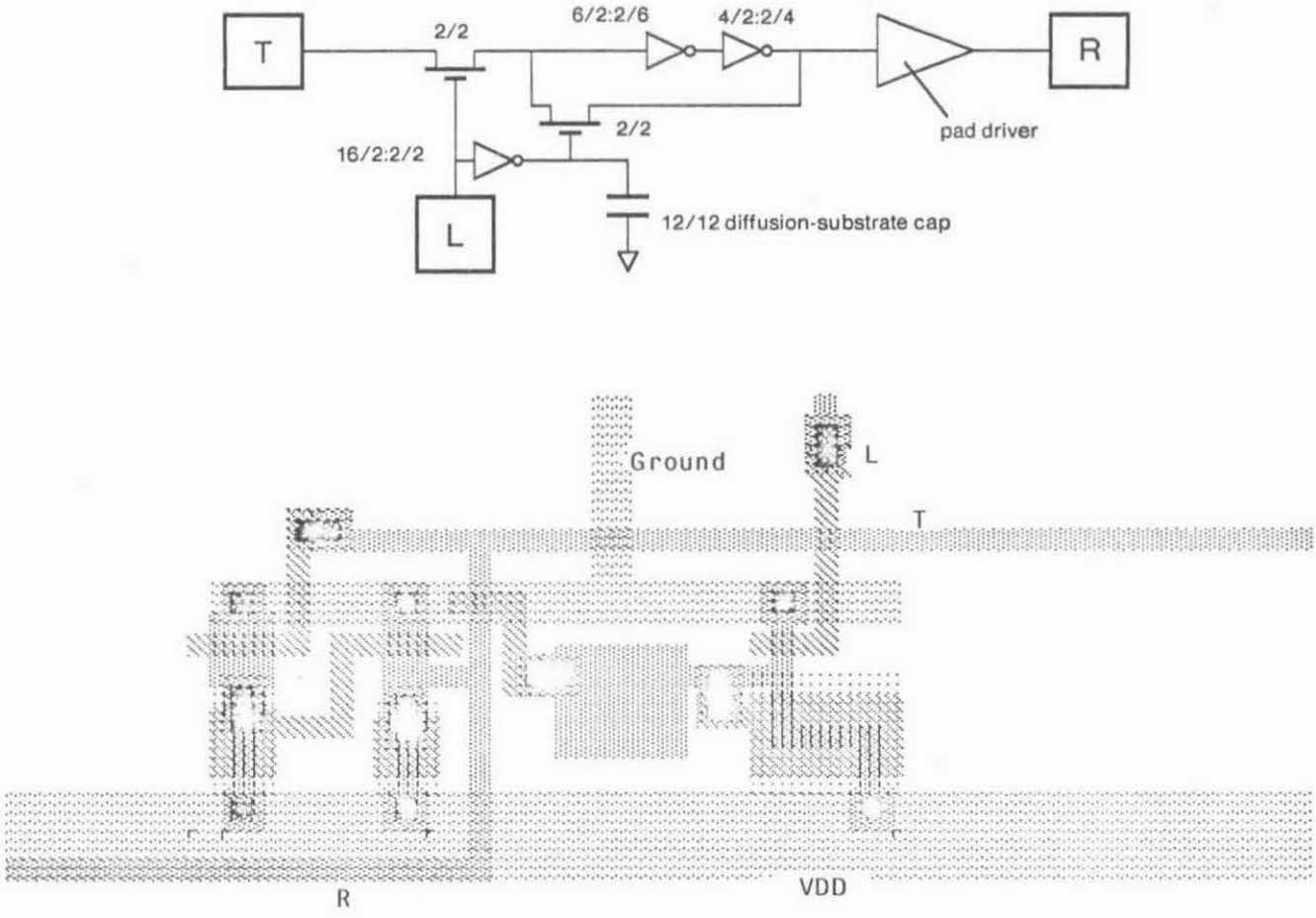


**Figure 6:** Circuit diagram and layout of the latch sampler. Transistor geometries are given as L/W in units of lambda.

signals using $n$+1 pads: $n$ pads for the results R and a single pad for **L**. This number can be reduced still further if the chip being tested has incorporated some general provision for scanning out internal state (e.g. shift-register latch). In this case, only a single pad for **L** is required, because the contents of the various static latches controlled by **L** can be determined by the scanning mechanism. Moreover, if properly designed, the clock of the scan-out path itself can be used as the **L** signal.

The C-element scheme seems to require a single pad for each signal being tested. However, it too can take advantage of provisions for scanning out internal state: each C-element output can be transmitted off-chip by the scanning mechanism.

## 6 Conclusions

On-chip timing samplers can provide the designer with an effective tool for measuring performance without using sophisticated test equipment. By incorporating these samplers into a scan-out path it is possible for the designer to provide both access to internal state and precise on-chip timing measurements without using many additional pads.

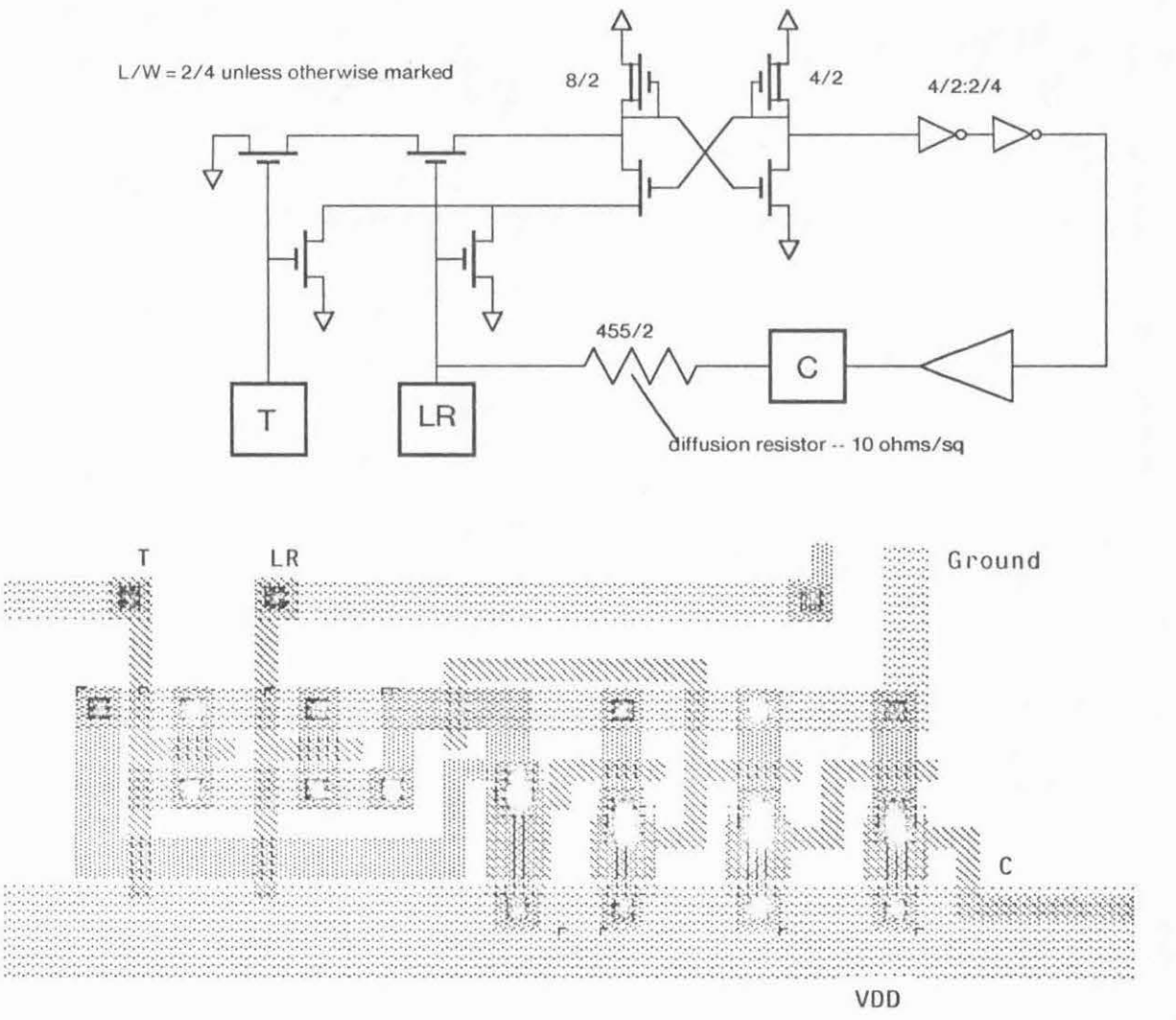


**Figure 7:** Circuit diagram and layout of the C-element sampler. The diffusion resistor is not shown in the layout.

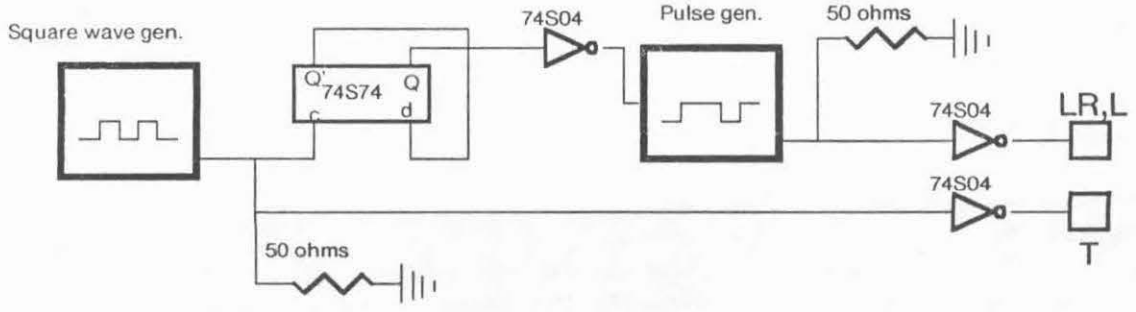


**Figure 8:** Jig used to test latch and C-element samplers.

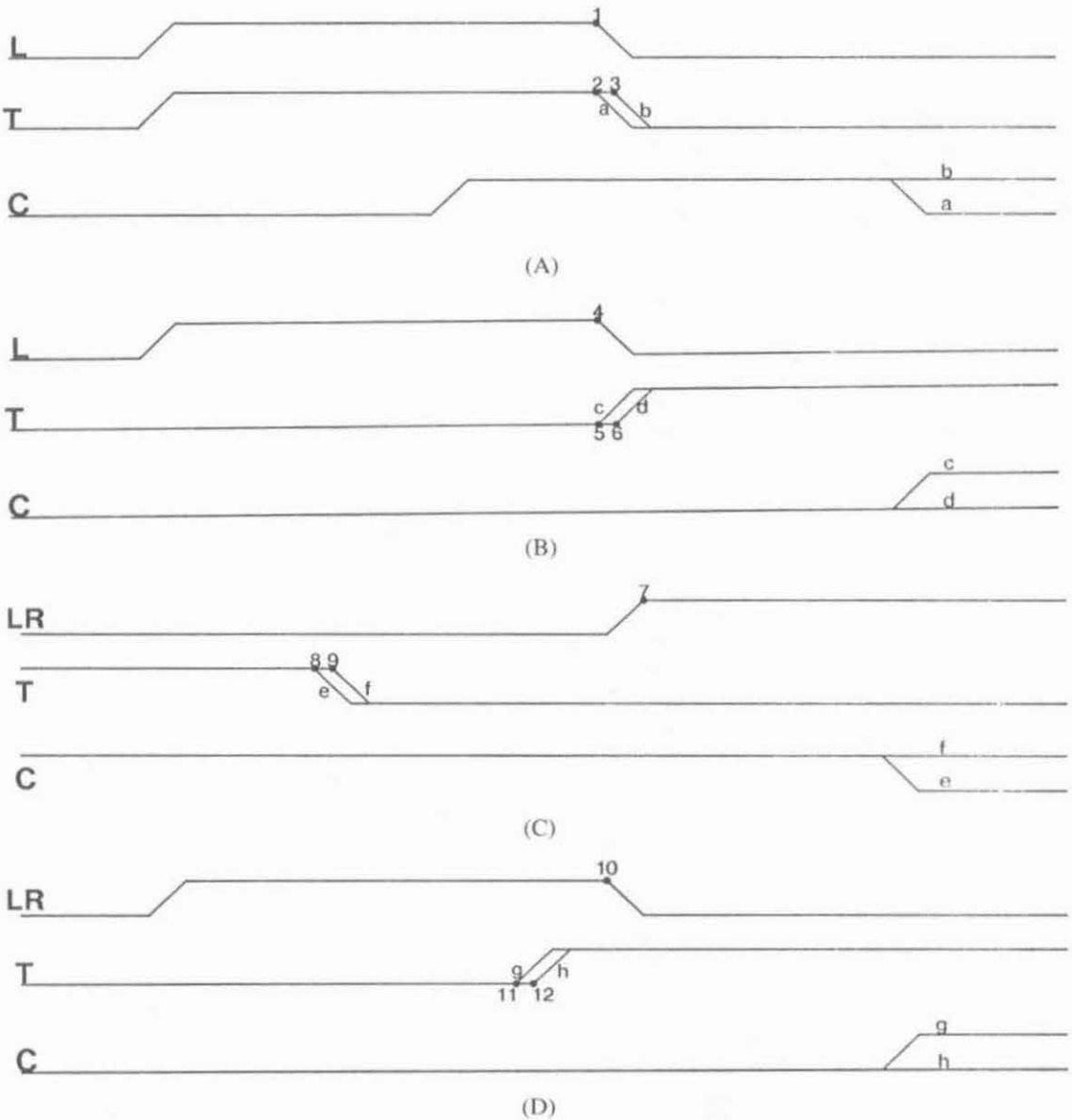


**Figure 9:** Results of timing experiments. Lower case letters indicate the edge of **T** that generates the corresponding output on **C** or **R**. Numbers and dots are used as reference points for the measurements. The horizontal axis is not to scale. Rise and fall times for **T**, **L** and **LR** are 4ns. (A) Latch sampler used to detect falling edge of **T**. (B) Latch sampler used to detect rising edge of **T**. (C) C-element sampler used to detect falling edge of **T**. (D) C-element used to detect rising edge of **T**.

| | |
|---|---|
| Latch used to detect falling edge of **T** (Figure 9A): | |
| $T_{2 \text{ to } 1}$ to produce output a: | 0 ns (min) |
| $T_{1 \text{ to } 3}$ to produce output b: | 2 ns (min) |
| Latch used to detect rising edge of **T** (Figure 9B): | |
| $T_{5 \text{ to } 4}$ to produce output c: | 0 ns (min) |
| $T_{4 \text{ to } 6}$ to produce outupt d: | 2 ns (min) |
| C-element used to detect falling edge of **T** (Figure 9C): | |
| $T_{8 \text{ to } 7}$ to produce output e: | 32 ns (min) |
| $T_{9 \text{ to } 7}$ to produce output f: | 30 ns (max) |
| C-element used to detect rising edge of **T** (Figure 9D): | |
| $T_{11 \text{ to } 10}$ to produce output g: | 12ns (min) |
| $T_{12 \text{ to } 10}$ to produce output h: | 10ns (max) |

**Table 1:** Timing measurements. All times are +/- 1 ns.

## References

[Eichelberger 78] Eichelberger, E.B., and Williams, T.W.
A logic design structure for LSI testability.
"*Journal of Design Automation and Fault Tolerant Computing*" 2(2):165-178, May, 1978.

[Frohwerk 77] Frohwerk, R.A.
Signature analysis: a new digital field service method.
*Hewlett-Packard Journal* :2-8, May, 1977.

[Koenemann 79] Koenemann, B., Mucha, J., and Zwiehoff, G.
Built-in logic block observation techniques.
In *Test Conference Proceedings*, pages 37-41. October, 1979.

[Puri 77] Puri, P.
The functional tester: an aid to the designer.
In *Test Conference Proceedings*, pages 64-80. 1977.

[Seitz 80] Seitz, C.
System Timing.
In *Introduction to VLSI Systems*, chapter 7, pages 218-254. Addison-Wesley, 1980.