Characterization and Scaling of MOS Flip Flop Performance in Synchronizer Applications

Thomas J. Chaney and Fred U. Rosenberger
Washington University
St. Louis, Missouri

Abstract:

The measured and calculated values of the Flip Flop parameters needed to specify synchronizer reliability are presented for 3 different depletion-load, silicon gate, NMOS, R-S Flip Flop circuits with gate lengths ranging from 6μm to 4.2μm. Estimates of the probability of synchronizer failure to resolve within allowed or desired times can be determined from these parameters.

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I. Introduction

A fundamental problem exists in communicating between any two concurrently operating digital systems that lack a common time reference. This problem involves the inability to build a completely reliable synchronizer or arbiter that will work in a prescribed amount of time. The problem may be stated as:

> Given two independent input events, determine within a bounded time of the arrival of the first one, which of them arrives first. If the difference in arrival time is small, either decision is acceptable but must be made irrevocably within a bounded time interval. By increasing the time allowed, the probability of not being able to determine which arrives first is reduced but this probability cannot be made zero. This lack of decision, or resolution, usually manifests itself by the output of a Flip Flop or output of a Flip Flop containing circuit being either undefined (between a high and low state), oscillating a number of times between the high and low states, or changing states at an arbitrary time after the input events.

It must be noted that the fact that a Flip Flop output is not resolved does not necessarily mean that the system the Flip Flop is embedded in will fail, only that it may fail. Experience has shown that the frequency of system failures may be significantly less than the calculated frequency of Flip Flop not resolved occurrences. Thus the data presented here represents an upper bound on system failures, not a prediction of system failures.

Previously published work has dealt with both the fundamental problem and with circuit characterization, primarily for TTL circuits. (1 through 21) This paper addresses the problem of characterizing the performance of MOS synchronizer Flip Flops in a manner that allows prediction of error probabilities based on Flip Flop parameters and the application conditions. This characterization of the time response of Flip Flops for use as synchronizers or arbiters involves several parameters in addition to the usually specified propagation delay. Section II briefly describes the additional parameters required, Section III gives equations which can be used for calculating these parameters, Section IV gives the results of measurements on several Flip Flops and finally, Section V discusses the implications of scaling on the performance of synchronizers and systems using them.

II. Definition of Synchronizer Flip Flop Parameters

The Flip Flop characterization outlined here is derived from a phenomenological model based directly upon our experiemental studies of electric circuits and is taken from the development in Wann, et al. (16) The synchronizer Flip Flop circuit considered in this paper is shown in Figure 1 with both R and S inputs initially high. We wish to estimate the probability that the synchronizer will fail to achieve a logically defined and stable output by a time t' after the time the earlier of the two inputs have switched low which we shall assume occurs at time t=0. Let us further assume that the high to low transition at the Reset input takes place at a time t_d relative to the Set input transition and that t_d has a uniform probability density p(t) over an interval $t_a \leq t_d \leq t_m$, that is

$$p(t_d) = \begin{cases} 0 & t_d < t_a \\ \dfrac{1}{t_m - t_a} = \dfrac{1}{\delta} & t_a \leq t_d \leq t_m \\ 0 & t_m < t_d \end{cases} \qquad (1)$$

where t_m is sufficiently positive that the Flip Flop always Resets, and t_a is sufficiently negative that the Flip Flop always Sets, within the normally specified propagation delay time following the time the earlier of the two inputs has switched low.

For t_d uniformly distributed over this interval, we can define F(t') as the probability that the Flip Flop output has not achieved a logically defined and stable value at the time t' for a single occurrence of the Set and Reset inputs going low. Experiments have shown that for sufficiently large values of t' (t' > h) this probability can be approximated by

$$F(t') = \frac{T_o}{\delta} \exp \frac{-t'}{\tau_r} \qquad t' > h \qquad (2)$$

where $\delta = t_m - t_a$

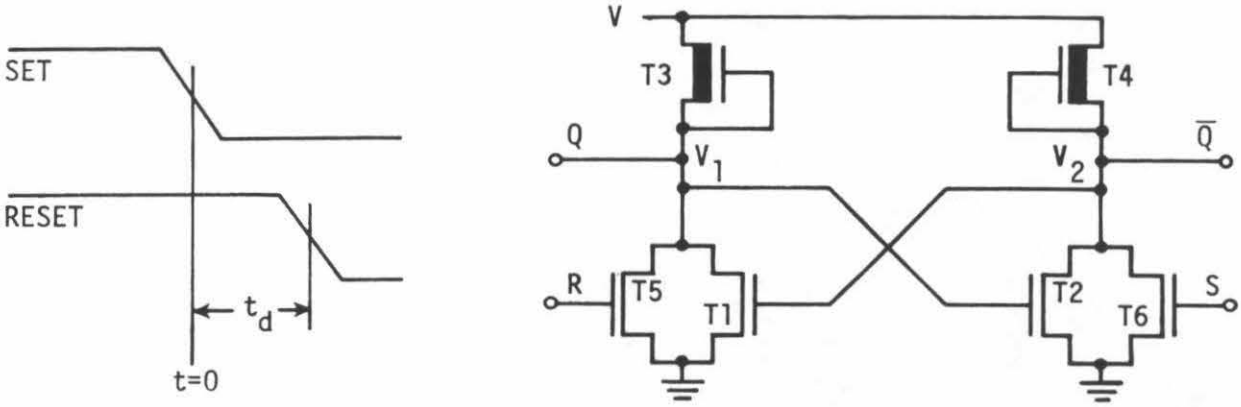
and the parameters τ_r and T_o depend upon the specific circuit. Multiplying both sides of Equation (2) by δ and taking the natural logarithm of both sides yields

$$\ln[\delta\ F(t')] = -\frac{1}{\tau_r}(t') + \ln\,[T_o] \qquad t' > h \qquad (3)$$

Hence, a semilogarithmic plot of δ F(t') versus t', as shown in Figure 2, is a straight line of slope $(-1/\tau_r)$. By setting t' equal to zero in Equation

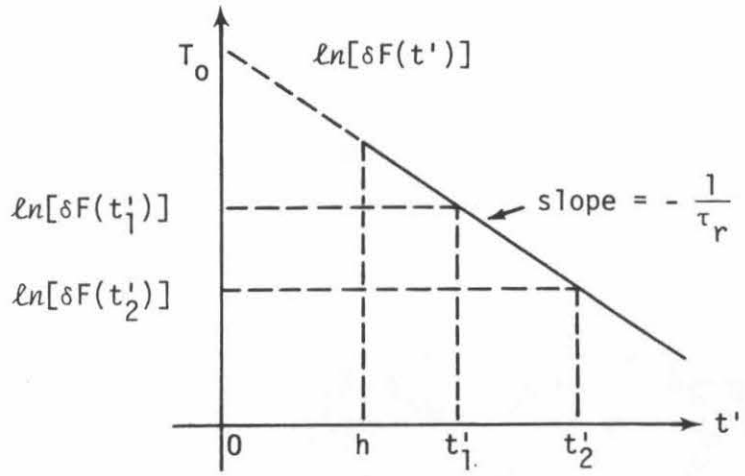
(3) it is clear that T_o is equal to $\delta\ F_e(0)$ where $F_e(t')$ is the linear extrapolation of $F(t')$ for $t' \leq h$.

The synchronizer Flip Flop thus can be characterized by three parameters, τ_r, T_o, and h. Clocked Flip Flop types such as J-K or D Flip Flops can be characterized in a similar manner where t' is the time after the clocking event. τ_r and T_o are calculated and the results compared with measurements for NMOS Flip Flops in Sections III and IV.



NMOS R-S FLIP-FLOP

FIGURE 1



GRAPHICAL REPRESENTATION OF PROBABILITY THAT SYNCHRONIZER HAS NOT ACHIEVED A LOGICALLY DEFINED AND STABLE STATUS

FIGURE 2

III. Calculation of values for T_o and τ_r

In this section equations are presented for the values T_o and τ_r as a function of the circuit parameters. The goal is to produce relatively simple equations in terms of the MOSFET threshold voltages and dimensions. More complete and precise equations can obviously be developed but simulation would probably be a more reasonable approach if greater accuracy is desired. It should be noted, however, that the simulation of Flip Flops in the metastable region with general purpose simulators should be approached with caution since such a simulation may be more a test of the numerical analysis techniques used in the simulator than of the circuit being simulated. The circuit used for the analysis is shown in Figure 1. The analysis is divided into two parts, the initialization time, t_i, starting when the Set and Reset inputs go low and lasting until the Flip Flop outputs reach the metastable state and the resolution time, t_r, starting from this point and lasting until the outputs diverge.

We are interested in the case where the Set and Reset signals go low nearly simultaneously so that a short time after they both go low the two outputs are approximately equal and at the same voltage as an inverter with its input connected to its output. We will call this voltage V_{INV}. If the circuit were balanced with perfect symmetry, the two output voltages exactly equal and the circuit noise-free, the Flip Flop would remain in this balanced condition indefinitely. Any initial imbalance will be amplified by the two inverters forming the Flip Flop and will eventually cause the outputs to reach the normal high and low voltages. The time required to reach the normal output levels is dependent on the initial imbalance in the Flip Flop outputs and on the gain and frequency characteristics of the inverters forming the Flip Flop. We will first determine the resolving time, t_r, the time to reach defined output levels based on an initial small difference in output voltages, and then determine the difference in output voltages at the beginning of the resolving time period as a function of the relative time that the Set and Reset inputs go low. Obviously t_i plus t_r equal the t' defined in Section II. Figure 3 shows a typical set of waveforms and the definition of the initialization time and resolving time for a Flip Flop.

For the resolving time calculation we will use a simple linear model since the major part of the operation occurs with V_1 and V_2 confined to a narrow voltage range close to V_{INV}. Toward the end of the resolving time, as V_1 and V_2 approach the normal high and low levels, this linear approximation becomes less and less valid but the error introduced by using the linear approximation is small.

In addition to errors introduced by the linear model at the end of the resolving time, the definition of when the outputs are resolved affects the calculations. As will be seen, the definition of the voltage at which the output is resolved and the use of linear approximations for the circuits will affect the calculated values for T_o but not the value of τ_r.

The pulldown transistors are obviously operating in the saturation region when their inputs and outputs are equal to V_{INV} since they have a positive threshold voltage, V_T, but the pullup transistor may be operating in either the saturation or resistive region. We will assume here that the pullup threshold voltage is sufficiently negative that it is in the resistive operating region when its drain voltage is at V_{INV}. Somewhat simpler equations are obtained if the pullup is assumed to be operating in the saturation region instead.

Figure 4 shows an equivalent circuit for the Flip Flop in the linear operating region when both the Set and Reset inputs are low, the pulldown transistor is saturated, and the pullup transistor is in the resistive region. For this case:

$$I_{T1} = \frac{\mu C_G}{2 \cdot L^2} (V_2 - V_{TPD})^2 \tag{4}$$

$$I_{T2} = \frac{\mu C_G}{2 \cdot L^2} (V_1 - V_{TPD})^2 \tag{5}$$

C_{TOT} = Total capacitance of node 1 including the gate capacitance of T2

$$R_1 = \left.\frac{dV_{DS}}{dI_{DS}}\right|_{V_{DS}=V_{DD}-V_{INV}} = \frac{L^2 \cdot k}{C_G \cdot \mu} \cdot \frac{1}{(V_{INV} - V_{DD} - V_{TPU})} \tag{6}$$

$$V_{INV} = \frac{k \cdot V_{TPD} + V_{DD} + V_{TPU}}{1+k} + \frac{\sqrt{V_{TPU}^2 + 2k \cdot V_{TPU} V_{TPD} - k \cdot V_{TPD}^2 + 2k \cdot V_{DD}(V_{TPD} - V_{TPU}) - k \cdot V_{DD}^2}}{1+k} \tag{7}$$

where: μ = Mobility of electrons

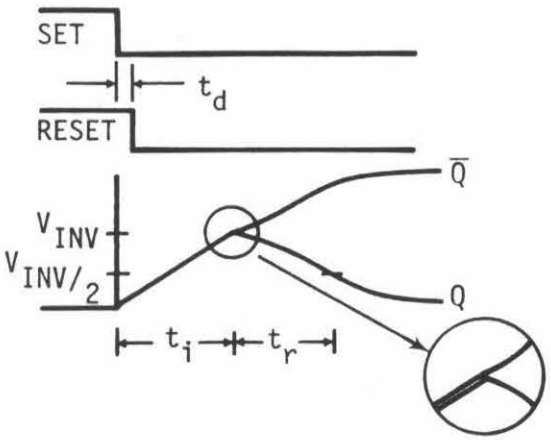
C_G = Gate capacitance of pulldown transistor

L = Gate length of pulldown transistor

$k = \frac{L_{PU}}{W_{PU}} \cdot \frac{W_{PD}}{L_{PD}}$ where L and W are the length and width of the PU (pullup) and PD (pulldown) transistors

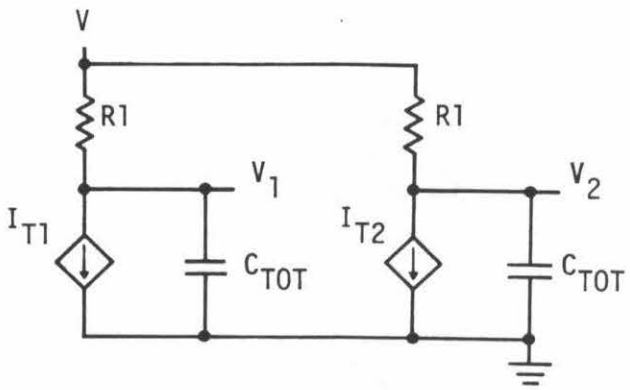
V_{TPD} = threshold voltage of pulldown transistor

V_{TPU} = threshold voltage of pullup transistor



TYPICAL WAVEFORMS FOR t_d SMALL AND POSITIVE

FIGURE 3



EQUIVALENT CIRCUIT FOR FLIP FLOP IN THE METASTABLE REGION

FIGURE 4

If the circuit has voltages $V_1 = V_{INV} - \Delta V$ and $V_2 = V_{INV} + \Delta V$ at time t_i, then the voltage V_1 as a function of time is given by

$$V_1 = V_{INV} - \Delta V \cdot \exp[p(A-1)(t-t_i)] \qquad t \geq t_i \tag{8}$$

where $p = \dfrac{C_G \cdot \mu(V_{INV} - V_{DD} - V_{TPU})}{C_{TOT} \cdot L^2 \cdot k}$ = the bandwidth of one inverter stage of the Flip Flop

$$A = k \cdot \frac{V_{INV} - V_{TPD}}{V_{INV} - V_{DD} - V_{TPU}} = \text{magnitude of the low frequency gain of one inverter stage}$$

thus the τ_r defined in Section II is given by

$$\tau_r = \frac{1}{p(A-1)} = \frac{C_{TOT} L^2}{C_G \mu} \cdot \frac{k}{k(V_{INV} - V_{TPD}) - (V_{INV} - V_{DD} - V_{TPU})} \tag{9}$$

and $$V_1 = V_{INV} - \Delta V \cdot \exp \frac{t-t_i}{\tau_r} \tag{10}$$

$$V_2 = V_{INV} + \Delta V \cdot \exp \frac{t-t_i}{\tau_r} \tag{11}$$

If the magnitude of the gain in the metastable region is large, τ_r is approximately equal to the inverse of the gain-bandwidth product. If the

magnitude of the gain is close to 1, τ_r becomes very large, but logic inverters with a gain of one are not very desirable for other reasons.

Next we wish to find the initial offset voltage ΔV as a function of the time difference between the Set and Reset signals, t_d. We will assume that both V_1 and V_2 are initially at 0 volts and start to increase linearly when the Set and Reset inputs, respectively, go low, and continue going positive until the average voltage of V_1 and V_2 is equal to V_{INV}. The difference between V_1 and V_2 at this time will be equal to $2 \cdot \Delta V$. Obviously in the real circuit the voltages V_1 and V_2 do not increase linearly once they are greater than V_{TPD} or when the pullup transistor is no longer saturated. Also the values of the two outputs, V_1 and V_2, start to diverge before their average reaches V_{INV}, but for ease of analysis we will consider the two regions of operation to be distinct, one in which the initial difference between the two outputs is established, and second the resolving time during which this small initial difference is amplified until the outputs reach the levels we establish as resolved. If we assume that the pullup transistors remain saturated, the pullup current is

$$I_{PU} = \frac{C_{GPU} \cdot \mu}{2 \cdot L_{PU}^2} (V_{TPU})^2 = \frac{C_G \cdot \mu}{2 \cdot L^2 \cdot k} (V_{TPU})^2 \tag{12}$$

$$\text{let} \quad w = \frac{dV_1}{dt} = \frac{dV_2}{dt} = \frac{I_{PU}}{C_{TOT}} = \frac{C_G \cdot \mu}{C_{TOT} \cdot 2 \cdot k \cdot L^2} (V_{TPU})^2 \tag{13}$$

$$\text{then} \quad 2 \cdot \Delta V = t_d \cdot w$$

$$\text{or} \quad \Delta V = \frac{t_d \cdot w}{2}$$

$$\text{and} \quad t_i = \frac{|t_d|}{2} + V_{INV} \cdot \frac{1}{w} \tag{14}$$

If we define the Flip Flop to be resolved when one of the outputs reaches $V_{INV}/2$ or halfway between 0 volts and V_{INV} we find the probability that the Flip Flop output is <u>not</u> resolved at t' is:

$$F(t') = \Pr[\text{Flip Flop output not resolved at } t']$$

$$F(t') = \begin{cases} \Pr[1/2\ V_{INV} < V_1(t')] & t_d > 0 \\ \Pr[1/2\ V_{INV} < V_2(t')] & t_d < 0 \end{cases} \tag{15}$$

Substituting equations (10) and (11) for V_1 and V_2:

$$F(t') = \begin{cases} \Pr[1/2\ V_{INV} < V_{INV} - \frac{t_d \cdot w}{2} \exp \frac{t' - t_i}{\tau_r}] & t_d > 0 \\ \Pr[1/2\ V_{INV} < V_{INV} + \frac{t_d \cdot w}{2} \exp \frac{t' - t_i}{\tau_r}] & t_d < 0 \end{cases} \quad (16)$$

$$F(t') = \begin{cases} \Pr[t_d < \frac{V_{INV}}{w} \exp \frac{|t_d|}{2\tau_r} \cdot \exp (\frac{V_{INV}}{w \cdot \tau_r} - \frac{t'}{\tau_r})] & t_d < 0 \\ \Pr[t_d > \frac{V_{INV}}{w} \exp \frac{|t_d|}{2\tau_r} \cdot \exp (\frac{V_{INV}}{w \cdot \tau_r} - \frac{t'}{\tau_r})] & t_d > 0 \end{cases} \quad (17)$$

$$F(t') = \Pr[|t_d| < \frac{V_{INV}}{w} \exp \frac{|t_d|}{2\tau_r} \cdot \exp (\frac{V_{INV}}{w \cdot \tau_r} - \frac{t'}{\tau_r})] \quad (18)$$

Equation (18) is valid only for t'>h. For h large enough $t_d \ll \tau_r$ so that

$$\exp \frac{|t_d|}{2\tau_r} \cong 1$$

$$F(t') = \Pr[|t_d| < \frac{V_{INV}}{w} \cdot \exp (\frac{V_{INV}}{w \cdot \tau_r} - \frac{t'}{\tau_r})] \quad (19)$$

If t_d is uniformly distributed over δ, δ includes the range of t_d, and t' is large enough that

$$\delta > \frac{V_{INV}}{w} \exp (\frac{V_{INV}}{w \cdot \tau_r} - \frac{t'}{\tau_r}) \quad (20)$$

then from (19); F(t') is the portion of the interval, δ, for which $|t_d|$ is less than $\frac{V_{INV}}{w} \exp (\frac{V_{INV}}{w \cdot \tau_r} - \frac{t'}{\tau_r})$, or is twice $\frac{V_{INV}}{w} \exp (\frac{V_{INV}}{w \cdot \tau_r} - \frac{t'}{\tau_r})$ divided by δ.

Thus
$$F(t') = \frac{2V_{INV}}{\delta \cdot w} \exp (\frac{V_{INV}}{w \cdot \tau_r} - \frac{t'}{\tau_r}) \quad (21)$$

or $$\delta F(t') = \frac{2V_{INV}}{w} \exp\left(\frac{V_{INV}}{w \cdot \tau_r} - \frac{t'}{\tau_r}\right) \tag{22}$$

and $$\boxed{T_o = \frac{2 \cdot V_{INV}}{w} \exp \frac{V_{INV}}{w \cdot \tau_r}.} \tag{23}$$

IV. Measurement of Synchronizer Flip Flop Parameters

A. Test method

The method used to determine experimentally a plot of the type shown in Figure 2 involves observing $\delta F(t')$ for at least two distinct times t_1', $t_2', \ldots, t_n'$ that are greater than h. The requirement that the input event time t_d is uniformly distributed over the interval $[t_a, t_m]$ is achieved experimentally by obtaining both input signals from the same timing source, and slowly adjusting the delay of one input signal so that in the course of an experiment a large set of values of t_d, uniformly distributed over the interval $[t_a, t_m]$, are generated.

A simplified drawing of the test setup used to measure $\delta F(t_n')$ is shown in Figure 5. Note that the sampling clock signal is derived only from the Set input to the F-F under test, not the "earlier to the two inputs" defined in Part II. The change in differential delay, t_d, between the two inputs required to change the output, Q, from always remaining low to always switching high is less than 0.1 nsec for the circuits tested. The values of D4, D5, D6 are approximately 5nsec. Thus the error introduced in t_n' by measuring from the Set input transition is very small. The "unstable state detector" shown in Figure 5 provides an output during the period the F-F under test is unresolved. This circuit is implemented with comparator circuits that measure when the Flip Flop outputs are not high or low. (7, 11, 21) The change in differential delay, t_d, is implemented with a 50 ohm adjustable coaxial airline (G.R. type 874-LAL) that is extended and contracted at a constant rate by a leadscrew and motor with a change of t_d of about 10^{-12} seconds per second.

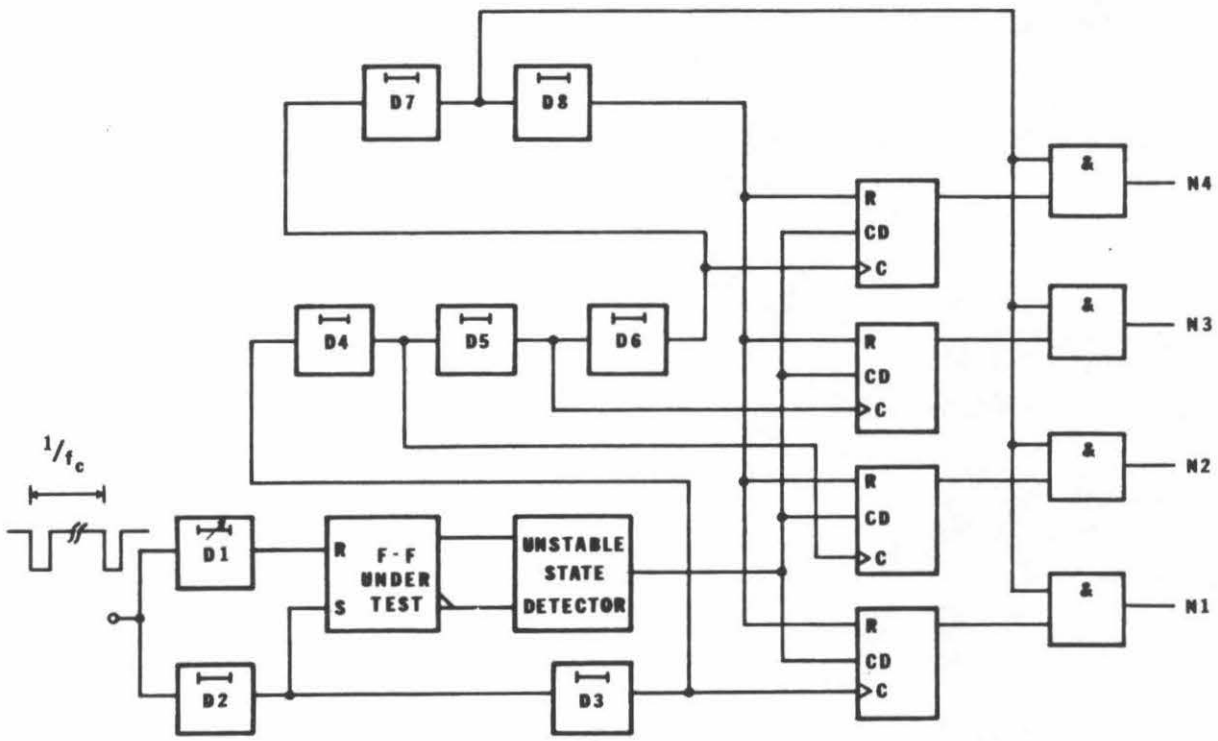
The equation required to calculate values of $\delta F(t_n')$ for each t_n' from the values collected using the test setup of Figure 5 is based on $F(t_n') = N_n/N_o$. N_o is the total number of uniformly distributed events ($t_a \leq t_d \leq t_m$) and N_n is the number of times the Flip Flop under test is still unresolved at t_n'. Let f_c be the frequency of the timing source and t_x be the time an experiment runs. Then $N_o = f_c \cdot t_x$ and

$$\delta F(t_n') = \frac{N_n \cdot \delta}{f_c \cdot t_x}.$$

δ is the total change in differential delay during the experimental run and can be expressed as $\delta = A_{coax} \cdot t_x$ where A_{coax} is the change in the amount of delay of the adjustable airline per second of experimental run. So:

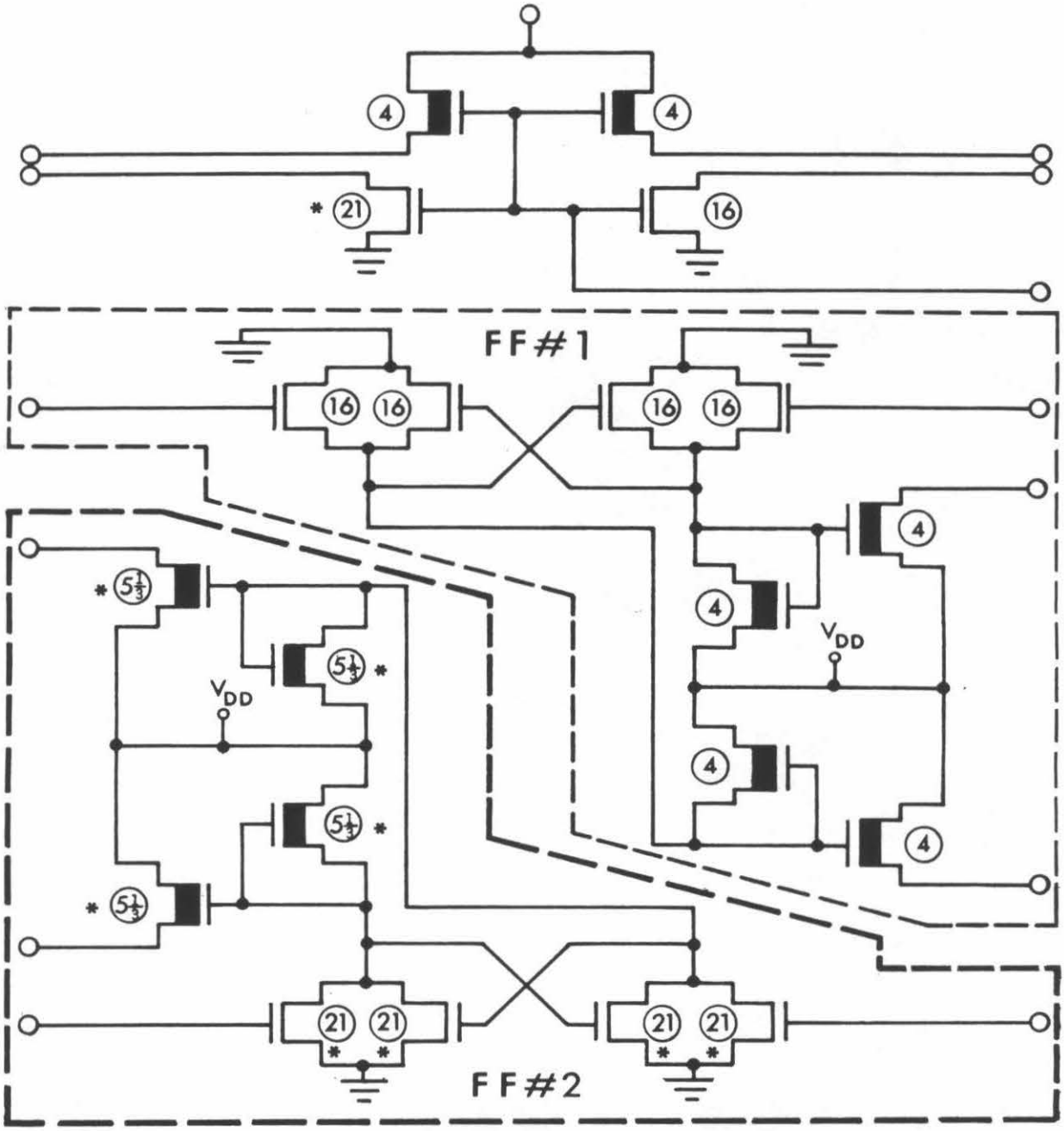
$$\delta F(t_n') = \frac{A_{coax}}{f_c} N_n.$$

Thus before an experiment, the event input frequency, the value of A_{coax}, and the values of t_1', t_2', t_3', and t_4' (indicated in Figure 2) are measured and recorded. Then after several test runs, half with the adjustable delay line extending and half with the delay line contracting, the average values of N_1 through N_4 are used to calculate the values of $\delta F(t_n')$. The value of h is then determined based on the linearity of the resulting plot or set at smallest value of t_1', used during the tests, whichever is larger.



SIMPLIFIED PROBABILITY UNRESOLVED TEST CIRCUIT

FIGURE 5



NOTES: (NO.) IS W/L

* TRANSISTORS HAVE L = 4 1/6 μM
OTHER TRANSISTORS HAVE L = 5 μM

FLIP FLOP CIRCUIT TESTED
FIGURE 6

B. Circuits tested

Two or three circuits from each of 3 different layouts have been tested. All 3 layouts are depletion-load, silicon gate, NMOS, R-S type Flip Flop circuits. Two of the Flip Flop circuits (three of each circuit were tested) are shown in Figure 6. FF #1 and FF #2 are identical, including layout pattern, except for the transistor gate lengths which are 5μm and 4 1/6 μm (mask dimension). The width to length ratio of the Flip Flop transistors is large to minimize the effect of stray capacitance. Four test transistors were included to allow measuring transistor parameters. Note that the outputs of each Flip Flop are buffered with source-follower transistors. During the tests, the source-follower transistor outputs were biased with a 300 ohm load resistor to ground. The source-follower signals, which were approximately 0.4V in amplitude and delayed approximately 5 ns, allowed monitoring the Flip Flop output waveforms with minimum loading.

The third Flip Flop (two circuits were tested) is the arbitration Flip Flop in an arbiter circuit designed by Dr. Ivan Sutherland and was fabricated with 6μm gate lengths (mask dimensions). (21) Table 1 gives a comparison of the basic circuit parameters for the 3 circuits tested. The tolerances noted are an indication of the consistency of the measurements and the fitting of the transconductance curves to the simplified equations used to calculate some of the table values.

The measured and calculated values for T_o and τ_r using the nominal values given in Table 1 and equations (9) and (23) are reasonably close as Table 2 shows, especially considering the model used and inability to measure some of the circuit parameters of the Flip Flops tested. It should be noted that the experimental results were not all measured on circuits from the same wafer. Figure 7 shows a graph of mean time between unresolved events for one of the Flip Flops (FF #1) as a function of allowed settling time, event rate, and logic delay. The curve labeled D=1, E=0 depicts the synchronizer Flip Flop performance if the input interrupt event rate is equal to the clock rate and the synchronizer Flip Flop output is tested at the next clock time with no logic gates or delay in series with the Flip Flop output. The curve labeled $D=10^{-3}$, E=0.5 depicts the synchronizer Flip Flop performance if the event rate is one thousandth the clock rate and the synchronizer Flip Flop output, after passing through logic gates or delay equal to one half the clock period, is tested at the next clock time.

CIRCUIT	L μM (2)	k (2)	V_{DD} = 5.0V			C_G (pfd.) (4)	C_{TOT} (pfd.) (4)	μ (5,6)
			V_{TPD} (6)	V_{TPU} (6)	V_{INV}			
ARBITER -1	6	5	-	-	-	0.087	0.34	-
ARBITER -2	"	"	-	-	-	"	"	-
FF #1-1	5	4	.5V (3)	-3V (3)	2V (3)	0.16	0.40	550 (3)
FF #1-3,4 (1)	"	"	.5V±.2V	-3V±.6V	2V±.1V	"	"	550±150
FF #2-2	4 1/6	4	.5V (3)	-3V (3)	2V (3)	0.13	0.36	550 (3)
FF #2-3,4 (1)	"	"	.5V±.2V	-3V±.6V	2V±.1V	"	"	550±150

(1) Chips 3 and 4 were near neighbors. The test results were all essentially identical.
(2) Mask dimensions.
(3) Estimated as average of chip 3 and 4.
(4) Estimated using layout masks and: [from Ref. (20)]
Gate - Channel cap. = 4×10^{-4} pfd/μm^2
Diffusion cap. = 0.8×10^{-4} pfd/μm^2
Polysilicon cap. = 0.4×10^{-4} pfd/μm^2
Metal cap. = 0.3×10^{-4} pfd/μm^2
(5) Cm^2/Volt Sec.
(6) Calculated from test transistor transconductance curves.

BASIC CIRCUIT PARAMETERS

TABLE 1

CIRCUIT	MEASURED (NSEC.)				CALCULATED (NSEC.)		$\frac{\tau_r \text{ calc.}}{\tau_r \text{ meas.}}$
	τ_r	T_o	t_{pd} L-H	$\overline{<h}$	τ_r	T_o	
ARBITER -1	2.4	-	-	-	-	-	-
ARBITER -2	2.1	-	-	-	-	-	-
FF #1-1	1.67	20	4	11	.76	58	46%
FF #1-3,4	1.45	13	4	9	"	"	52%
FF #2-2	1.44	8	-	11	.58	46	40%
FF #2-3,4	1.20	15	5	9	"	"	48%

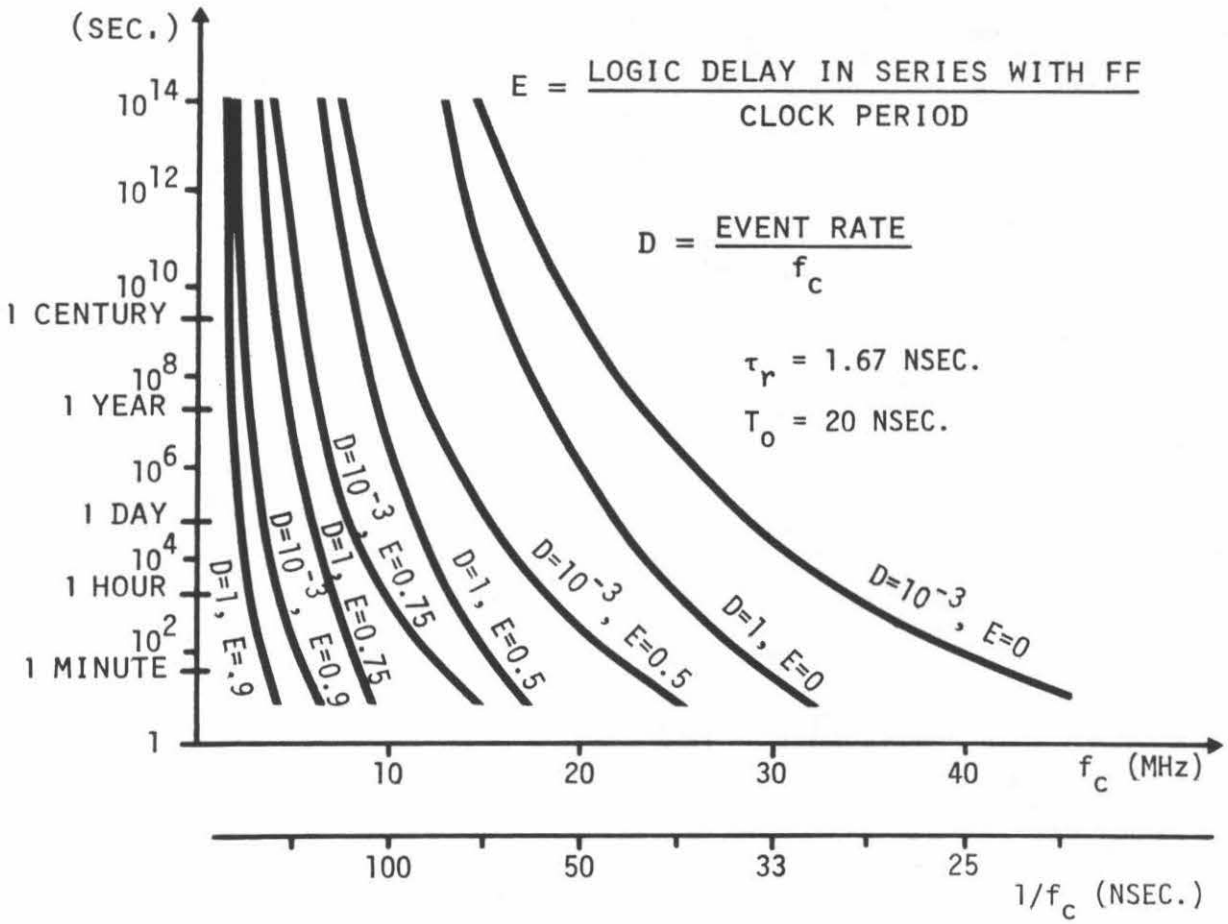
EXPERIMENTAL AND CALCULATED VALUES OF SYNCHRONIZER PARAMETERS

TABLE 2

$$MTBSU = \frac{\exp\left(\frac{1-E}{f_c \cdot \tau_r}\right)}{(T_o)(f_c)^2 D}$$

MEAN TIME BETWEEN
SYNCHRONIZER UNRESOLVED
AT CLOCK TIME (MTBSU)

FOR EVENT OCCURRENCES
UNIFORMLY DISTRIBUTED
WITH RESPECT TO CLOCK



PROBABILITY OUTPUT OF SYNCHRONIZER FLIP FLOP
AND LOGIC IS STILL UNRESOLVED AT NEXT CLOCK TIME

FIGURE 7

V. Conclusions

As feature sizes and voltages are scaled down by α it can be shown using equations (9) and (23) that both T_o and τ_r are reduced proportionally to the scaling. Since normal propagation delays also scale proportionally to dimensions and voltages (20, 22), the ratio of T_o and τ_r to propagation delay remains constant. Thus, if system dimensions and operation times are scaled, the probability of a synchronizing Flip Flop failing to resolve within the allowed time remains the same for each occurrence. However, since the operation times are reduced by scaling, a higher rate of unresolved outputs is produced if we take advantage of the ability to perform more operations per second. Also, if we take advantage of the scaling to build systems with α^2 times as many elements and build them with the same proportion of synchronizers, then scaled systems will have α^3 as many synchronizing events per second, all with the same probability of failure as the unscaled system. Thus, if the unscaled system had a mean time between synchronizer unresolved (MTBSU) of one per year, a system scaled by 10 would have a MTBSU of about 9 hours, a significant reduction. Obviously the scaling of MTBSU is not very desirable. The moral here is that the same design techniques for interconnecting subsystems that are used with today's designs and feature sizes may not be directly applicable with scaled circuits.

Considerable refinement in measurements, techniques and sample size, and calculations is possible and some additional effort seems worthwhile. In particular measurements on circuits whose fabrication parameters are better characterized would be worthwhile. In addition, better characterizations of Flip Flop performance with input switching and conditions that cause resolving times between t_{pd} and h is warranted, both to provide better understanding of the circuit operation and for use in asynchronous arbiter circuits where operations are delayed only until the Flip Flop resolves instead of providing a long fixed waiting time. In these arbiter circuits the parameter of interest is expected settling time, not the time required to reduce F(t') to less than some particular value.

VI. References

1. Krevden, N.L., "The Dynamics of the Toggle Action," Proceedings of the Western Joint Computer Conference, Los Angles, CA.: 46-50, May 6-8, 1958.

2. Gray, H., Digital Computer Engineering, Prentice-Hall, Inc., Englewood Cliffs, NJ: 198-201, 1963.

3. Catt, I., "Time Loss Through Gating of Asynchronous Logic Signal Pulses," IEEE Trans. on Electronic Computers, EC-15:108-111, Feb. 1966.

4. Littlefield, W.M., and Chaney, T.J., "The Glitch Phenomenon," Computer Systems Laboratory, Washington University, St. Louis, MO, Technical Memorandum #10, Dec. 1966.

5. Mars, P., "Study of the Probabilitic Behavior of Regenerative Switching Circuits," Proc. IEE, (England), 115:642-668, May 1968.

6. Couranz, G.R., An Analysis of Binary Circuits Under Marginal Triggering Conditions, Computer Systems Laboratory, Washington University, St. Louis, MO, Technical Report #15, Nov. 1969.

7. Adams, R.L., Castaldo, D.R., and Kurz, G.W., "Real-time Detection of Latch Resolution Using Threshold Means," U.S. Patent 3,515,998, June 1970.

8. Wheeler, D.J., "System Design for Non-Engineering Students and the Synchronization Problem," Proc. of the Conf. on Teaching of Computer Design, Univ. of Newcastle-upon-Tyne, England, 88-94, Sept. 1971.

9. Plummer, W.W., "Asynchronous Arbiters," IEEE Trans. on Computers, C21:37-42, Jan. 1972.

10. Workshop on Synchronizer Failures, Washington University, St. Louis, MO, April 27-28, 1972.

11. Chaney, T.J., Ornstein, S.M., and Littlefield, W.M., "Beware the Synchronizer," in Digest of Papers - COMPCON '72, IEEE Computer Society Conference: 317-319, Sept. 1972.

12. Chaney, T.J., and Molnar, C.E., "Anomalous Behavior of Synchronizer and Arbiter Circuits," IEEE Trans. on Computers, C-22:421-422, April 1973.

13. Kinnement, D.J., and Edwards, D.B.G., "Circuit Technology in a Large Computer System," The Radio and Electronic Engineer, 43:435-441, July 1973.

14. Chaney, T.J., The Synchronizer 'Glitch' Problem, Computer Systems Laboratory, Washington University, St. Louis, MO, Technical Report #47, Feb. 1974.

15. Hurtado, M., Dynamic Structure and Performance of Asymptotically Bistable Systems, D.Sc. Dissertation, Dept. of Electrical Engineering, Washington University, St. Louis, MO, 1975.

16. Wann, D.F., Molnar, C.E., Chaney, T.J., and Hurtado, M., "A Fundamental Problem Associated with the Physical Realization of Certain Classes of Petri-Nets," Conf. on Petri-Nets and Related Methods, MIT, Cambridge, MA, S.S. Patil-Editor, July 1975, to be published. Copies available as Technical Memorandum #215, Computer Systems Laboratory, Washington University, 724 S. Euclid Ave., St. Louis, MO 63110.

17. Pechoucek, M., "Anomalous Response Times of Input Synchronizers," IEEE Trans. on Computers, C-25, No. 2:133-139, Feb. 1976.

18. Kinniment, D.J., Woods, J.V., "Synchronization and Arbitration Circuits in Digital Systems," Proc. of the IEE, (England), Vol. 123, No. 10:961-66, Oct. 1976.

19. Marino, L.R., "The Effect of Asynchronous Inputs on Sequential Network Reliability," IEEE Trans. on Computers, C-26, No. 11:1082-90, Nov. 1977.

20. Mead, C.A., and Conway, L.A., Introduction to VLSI Circuits, to be published.

21. Sutherland, I.E., "A Specific Arbiter Design, ARBIT2," Computer Science Department, California Institute of Technology, Pasadena, CA, Display File No. 226, Sept. 22, 1976.

22. Dennard, R.H., Gaensslen, F.H., Yu, H.N., Rideout, V.L., Bassous, E., and LeBlanc, A.R., "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," IEEE Journal of Solid-State Circuits, SC-9, No. 5, Oct. 1974.