Moore's Law, Competition and Intel's Productivity in the Mid-1990s*

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In the mid-1990s, a pickup in measured productivity growth for the semiconductor industry coincided with an economy-wide acceleration in labor productivity growth. The pickup in semiconductor markets reflected an increase in the growth of real output that was generated by what Dale Jorgenson (2001) called an "inflection point" in the price indexes for the semiconductor industry. Jorgenson hypothesized that the inflection point reflected increases in the rate of product innovation made possible by an increase in Moore's Law, a stylized description of technology that currently states that the number of electrical components on a chip will double every eighteen months. Within semiconductors, microprocessors (MPUs) produced by Intel—the world's largest producer of the chips that serve as a computer's central processing unit—were the primary contributor to the inflection point in the semiconductor index.

The inflection point in the price index coincided with two changes in the price contours for Intel's chips. As shown in the top panel of figure 1, price contours for Intel's chips became steeper around 1995. Because most price index formulae boil down to functions of weighted averages of price change, steeper price contours translate directly into more rapidly declining price indexes. At the same time, the product lifecycle for MPUs—the length of time chips are sold in the market—shortened and Intel began to introduce chips more frequently. This is seen in the lower panel, where lifespans for Intel's chips are depicted as horizontal lines plotted against the speed of the chip.

What caused these changes in pricing and product cycles? This paper provides a simple framework to help gain some intuition on these issues. The model provides a set of conditions under which an increase in Moore's Law is consistent with both of these stylized facts. In the model, an increase in Moore's Law raises the quality of future chips relative to today's chips. If consumers view these chips as substitutes, then increases in the quality of tomorrow's chips push down the prices for today's chips and can, under certain conditions, generate an inflection point in the price index. With regard to product lifecycles, the model suggests that increases in the rate of product introductions and reductions in chips' market lives could simply be the monopolist's profit-maximizing response to an exogenous increase in Moore's Law.

Thus, the model provides support for the Moore's Law hypothesis. However, the framework also suggests that changes in the attributes of *contemporaneous* substitutes can have the same effects. Thus, the model suggests that increases in the quality of competitor's chips can generate an inflection point through the same channel. This is an important possibility to consider because Intel faced increasing competition from AMD beginning in the mid-1990s, about when the inflection point occurred.

I. Price Contours and Inflection Points

Suppose the quality of chips evolves at an exogenous rate q that is determined by Moore's Law. There are fixed costs incurred when a chip is introduced (I^c) so that chips are introduced only occasionally. For simplicity, assume that the firm produces one chip at a time and that all chips live for *A* periods, so that over some period of length *M*, C=M/A chips are introduced.

The price that consumers are willing to pay for chip *c*, *a* periods old is given by:

$$P_{c,a} = P_o e^{-sa}$$

where P_o is the introduction price and $0<s<1$ is the slope of the (logged) price contour.

Introduction prices depend on the attributes of available substitutes. If consumers view today and future chips as substitutes, then introduction prices depend on the quality of future chips relative to today's chips and the price contours may be stated as:

(1) $$P_{c,a} = P_o(q)e^{-sa}$$

where increases in Moore's Law lower introduction prices: $dP_o/dq<0$.

Prices of all chips decline at the rate *s* so that price indexes decline at that rate as well and inflection points in the index are generated by changes in the slope of the price contours. Therefore, a simple way to ensure that changes in Moore's Law cause inflection points is to specify the slope as a function of *q* (s=s(q), with s'>0). This assumption may be justified in two ways. First, suppose that MPU markets are populated by heterogeneous buyers and that Intel engages in inter-temporal price discrimination—it sells first to those with a high willingness-to-pay, then sequentially lowers prices. As explained by Joel Dean (1969):

> "Launching a new product with a high price is an efficient device for breaking the market up into segments that differ in price elasticity of demand. The initial high price serves to skim the cream of the market that is relatively insensitive to price. Subsequent price reductions tap successively more elastic sectors of the market.

> This pricing strategy is exemplified by the systematic succession of editions of a book, sometimes starting with a $50 limited personal edition and ending up with a 25-cent pocket book." (P. 174)

In this view, an increase in *q* causes price contours to pivot because buyers change as the chip ages: early buyers are willing to pay more for the chip than later buyers.

The alternative argument—that does not require consumer heterogeneity—is that the relative quality of a chip changes as it ages: the quality of an older chip gets "closer" to that of available substitutes it ages. If the inter-temporal substitution between today and tomorrow's chips intensifies as the new chip's arrival nears, then prices for older chips—those closer in time to the arrival of the new chip—will be both lower and more price-sensitive than prices for newer chips.

II. A Simple Model

Given the assumption that increases in *q* generate inflection points, how does an increase in *q* affect product lifecycles? To model the firm's choices regarding product lifecycles, assume that the rapidly declining prices discussed above force the firm to produce at capacity. This is consistent with anecdotal evidence for this industry and has been used in previous models of the semiconductor industry (e.g., Ken Flamm (1989)). Further assume that that capacity and, hence, output ($\tilde{y}$) is fixed over time. This assumption is admittedly problematic because there are thought to be important learning economies for semiconductors, especially for devices sold in highly competitive markets (notably, memory chips). However, industry data suggests that learning effects are less important for MPUs (Aizcorbe(2002)).

The firm's objective is to choose the number of chips it will introduce over the M periods (and thus the length of chips' lifespans) so as to maximize profits. The price contours above imply that the revenues collected over the life of each chip c are:

$$R_c = P_o(q)\tilde{y} \int e^{-s(q)a}\, da$$

$$= P_o(q)\tilde{y}\, (1-e^{-s(q)A})/s$$

Profits over the M periods may then be written as the profits obtained from each chip times the number of chips introduced:

$$(2) \qquad \Pi_M = [\, R_c - I_c\,]C\ .$$

The optimal number of chips maximizes this expression (an appendix detailing the equilibrium conditions is available upon request). The first-order condition says that profits are maximized when the marginal revenue from introducing an additional chip equals the marginal cost of doing so:

$$(3) \qquad R_c\, [\ 1 + d\ln R_c/d\ln C] = I_c$$

The term on the left-hand side is marginal revenue. It says that introducing an additional chip brings R_c in revenues but reduces the amount of revenue obtained from each chip by $d\ln R_c/d\ln C$. This occurs because more introductions implies shorter lifespans thus reducing per-chip revenue. The first order condition states that this marginal revenue of adding a chip introduction equals the introduction cost.

The second order condition is satisfied if this marginal revenue decreases with the number of chip introductions. It can be shown that this condition will hold so long as price contours slope downward. In the expression for marginal revenue, increased introductions lower per-chip revenue so the first term is negative. The effect on the elasticity—the second term in marginal revenue—is less obvious. Intuitively, the elasticity captures the losses in per-chip revenues when lifespans are reduced in response to increased introductions. These lost revenues come from the end of chips' lifespans, where per-period revenue is the lowest. So, with a large number of introductions, chips are relatively young at exit and the lost revenues—as the tail end of their lifespan is truncated—are relatively high. In contrast, with fewer introductions, the lost revenues are from older (less profitable) chips. Thus, the losses in per-chip revenue increase (become more negative) with the number of chip introductions. That is, $d(dlnR_c/dlnC)/dC<0$ and the second-order condition holds.

III. Effects of an Increase in Moore's Law

The shape of price contours also plays an important role in determining the effect of changes in Moore's Law on the number of chip introductions. As noted above, downward-sloping price contours imply that an increase in *q* lowers the prices of older chips more than those of other chips. If these relative differences reduce the marginal benefit of selling older chips, then the firm will have an incentive to shift sales towards younger chips, which it does by introducing more chips.

Formally, the effect of an increase in *q* on chip introductions is found by taking the total derivative of the first-order condition (3) and solving for dC/dq:

(4) $$dC/dq = - [dR_c/dq + C\, dR_c'(C)/dq] \;/\; [2dR_c/dC + C\, dR_c'(C)/dC] ,$$

where $R_c'(C)$ is the derivative of per-chip revenues with respect to chip introductions. Evaluating this expression, the second-order condition ensures that the denominator is negative. Therefore, increases in *q* generate higher chip introductions ($dC/dq >0$) if the bracketed term in the numerator is positive. That numerator represents what happens to the responsiveness of per-chip revenue to changes in C when *q* rises. The first term is negative: increases in *q* push down prices of all chips and, hence, per-chip revenue. The second term represents how changes in *q* affect the losses in per-chip revenue associated with increases in C. The value of these lost sales declines (becomes less negative) when the rise in *q* pushes down prices of all chips. Therefore, the second term is positive. If that effect is high enough to offset the declines in per-chip revenues captured in the first term, increases in *q* will generate more chip introductions. The end result is a new equilibrium where more chips are introduced over the M periods and where each chip has a shorter market life.

Thus, if price contours are sufficiently steep, increases in Moore's Law can generate the changes to product lifecycles seen beginning in 1995.

IV. Increased Competition from AMD

In this simple framework, factors that change the slope of price contours can generate an inflection point. The lever that generates this result is the presence of the *inter-temporal* substitute: tomorrow's chip. One might ask, then, whether changes in the attributes of *contemporaneous* substitutes can generate similar effects. If consumers view chips produced by competitors—like AMD—as substitutes for Intel's chips, then the quality of the AMD chip would affect prices for Intel's chips. For example, let introduction prices be a function of the quality of the AMD chip: $P_o(q,Q^{AMD})$ with $dP_o/dQ^{AMD}<0$. If, as argued above, prices for older chips are more price-sensitive than those of newer chips, then the quality of AMD chips also determines the slope of the price contours: $s=s(q,Q^{AMD})$, with $ds/dQ^{AMD}>0$.

Given the parallel treatment of Intel's future chips and AMD's current chip in these expressions, an increase in the quality of the AMD chip will have effects similar to an increase in Moore's Law. Tracing through the effects, increases in the quality of the AMD chip makes it a more attractive substitute and directly steepens Intel's price contours: older chips are viewed as closer substitutes to the (lower quality) AMD chips so those prices fall further than prices for newer chips. As was the case with an increase in Moore's Law, this can create an inflection point if price contours respond sufficiently to the change in AMD's chips. With respect to product cycles, the the cost associated with introducing chips falls when contours become steeper and Intel responds by adding chip introductions until equilibrium is restored. This increase in the number of chips introduced over *M*, implies shorter market lives for each chip. The end result is the same as with an increase in Moore's Law: a new equilibrium where price contours are steeper, the price index has an inflection point, product introduction rates are higher and each chip's market life is shorter.

V Conclusions

This paper provides a stylized framework that outlines conditions under which an increase in Moore's Law can (i) generates an inflection point in the MPU price index and (ii) could have prompted Intel to increase the rate of product introduction and shorter each chips' product cycle. The assumptions required to generate this result also suggest that increases in competition can generate the same results. Because these competing explanations have different implications for the sustainability of the increase in productivity growth, future work is needed to study these possibilities in a more rigorous fashion.

References

Aizcorbe, Ana. "Product Innovation, Product Introductions and Productivity at Intel in the 1990s," Paper presented at NBER Productivity Workshop, March, 2004.

Aizcorbe, Ana. "Why Are Semiconductor Prices Falling So Fast? Industry Estimates and Implications for Productivity Measurement," Federal Reserve Board (Washington, D.C.) Working Paper No. 2002-20, February 2002.

Aizcorbe, Ana and Kortum, Sam. "Moore's Law and Microprocessors: A Textbook Model." Mimeo, August, 2004.

Flamm, Ken. Mismanaged Trade: Strategic Policy and the Semiconductor Industry. Washington, DC: Brookings Institution, 1989.

Jorgenson, Dale W. "Information Technology and the U.S. Economy," American Economic Review, March 2001, 91(2), pp.1-32.

Footnotes

[*] This is a shortened and revised version of Aizcorbe (2004). I thank Sam Kortum for his comments as discussant at the NBER Productivity Workshop and for all that I have learned from our subsequent collaboration on these issues (Aizcorbe and Kortum (2004)). I also thank Shane Greenstein, Marshall Reinsdorf and seminar participants at the Bureau of Economic Analysis, the Brookings Institution and the New York Federal Reserve Bank for helpful comments.

Figure 1. Price Contours and Product Cycles

Intel's Desktop Microprocessor Chips, 1993-2002