

DSP for Embedded and Real-Time Systems

Expert Guide

Robert Oshana

CHAPTER 8

High-level Design Tools for Complex DSP Applications

Yang Sun¹, Guohui Wang¹, Bei Yin¹, Joseph R. Cavallaro¹, Tai Ly²

¹Rice University, ECE Department, Houston, TX ²National Instruments Corporation, Austin, TX

High-level synthesis design methodology

High level synthesis (HLS) [1], also known as behavioral synthesis and algorithmic synthesis, is a design process in which a high level, functional description of a design is automatically compiled into a RTL implementation that meets certain user specified design constraints. The HLS design description is 'high level' compared to RTL in two aspects: design abstraction, and specification language.