Testing of DC/DC Converters for 48 V Electric Vehicles

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Abstract. DC/DC applications in automotive market are expected to require new system specifications in next years. Because of the spreading of electrical cars, the power line at 48 V will be very common. Moreover, the converter chips and external passives are required to occupy less area. A DC/DC solution, meeting such requirements, is presented in this work. The switched capacitors architecture is intended to reduce external passive devices space occupation, whereas sustained electrical power is kept high. This paper discusses a preliminary version of the converter, with experimental results from measurements, and presents the final chip architecture, with some simulation result data.

1 Introduction

In electric vehicles the DC supply system is moving towards 48 V to manage increased electric power levels, but avoiding to increase too much the current level and hence the cable losses. Due to the presence on-board of low-voltage electronics, 48 V DC/DC converters are key components of next vehicle generation to supply sensors, microcontrollers and memories directly from the 48 V. In the framework of the ATHENIS_3D EU project [1], with VALEO and ams AG industrial partners, we designed two DC/DC converters. A first version has been designed to interface the 48 V with already existing 12 V DC power bus on board vehicles. This version has off-chip control thus allowing to implement the desired control strategy on an external microcontroller.

The final DC/DC version integrates multiplestages to directly supply from the 48 V low-voltage loads (5 V and 1.65 V). Due to cranking and overvoltage phenomena, the 48 V nominal battery voltage can vary from 6 V to 60 V. Since linear regulators would be to inefficient for applications with a big difference between the input and the output voltage levels, a switching DC/DC converter approach has been followed. Hereafter the new DC/DC converter architecture in its two configurations is briefly presented (Section 2). Section 3 presents the testing plan for the DC/DC converter characterization phase. Section 4 presents the design of the testing board and the achieved experimental results due to electrical and thermal characterization. Conclusions are drawn in Section 5.

2 48 V DC/DC Converter Architectures

The first proposed version of the converter allows to make compatible the classics 12 V automotive devices with the new 48 V standard. A switching technique is used to keep the power efficiency higher than a linear converter. The converter is an inductorless DC/DC, designed to improve the integration in a single die. It is a step-up/step-down

switched capacitor converter. This architecture, see circuit schematic in Figure 1, is called serial-parallel converter for the typical operating modes. It allows to make three voltage conversion ratios (VCRs) 2, 1, 1/2. Thus with two cascade converters is possible convert the wide range voltage in a voltage around 12 V.

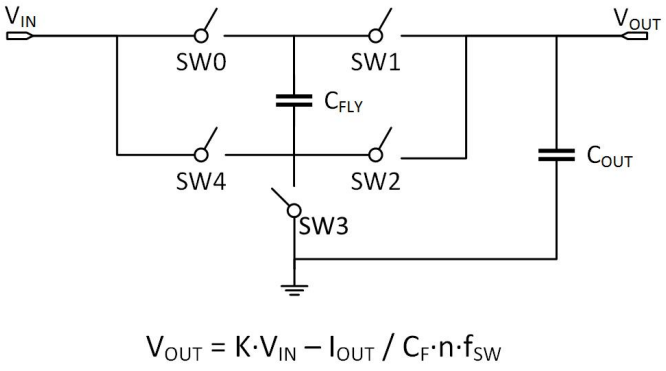

Fig. 1: Circuit schematic.

For this first 48 V converter, it has been decided to implement a single stage in each chip and use two separate chips to convert the 48 V power line to 12 V (see Figure 4 in Section 3). This allows to make more deep test than other configurations. The switch topologies have been specifically designed for this application. HV-MOSFETs in ams AG 0.35 μm technology have been used, that can operate up to 70 V. The used switching frequency is 90 kHz, which has been derived after EMI/EMC analysis in the automotive field. In order to test some control techniques as PWM (Pulse Width Modulation), SKIP, PFM (Pulse Frequency Modulation) and analyze the best control solution, an external digital block has been implemented for the test chip. The skip and the PFM modes allow for a spreading of the generated electromagnetic noise and hence they improve the EMI performance vs. classic PWM. The skip mode is simpler to implement since it does not require voltage controlled oscillators but it can create substrate injection problems when skipping for a long time period in case of low current values. The test version of the DC/DC converter has been bonded in a DIL24 ceramic package. The test board in Figure 2 has been designed with SMD capacitors, however the project concept aims at stacking capacitors on top of the converter IC, thus minimizing PCB area.

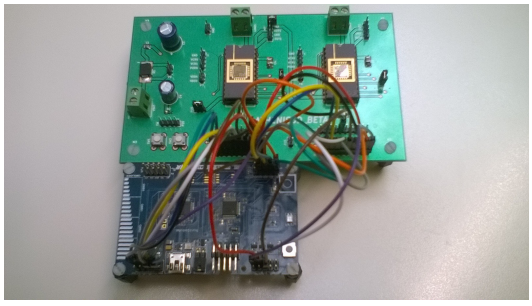

Fig. 2: Test board of the first system version.

The second converter version is an upgrade of the first one. It converts the wide input voltage (6 V up to 60 V) in two regulated voltages 5 V and 1.65 V with a

target load current from few tens of mA up to 300 mA. This converter is a multi-stage system composed from the preview converter, an insulator block (we patented in [2]), another DC/DC converter stage and two LDOs (Figure 3). The entire system is integrated in a single die of 36 mm^2 (including the area of the big PADs) in 0.35 μm HV-CMOS technology.

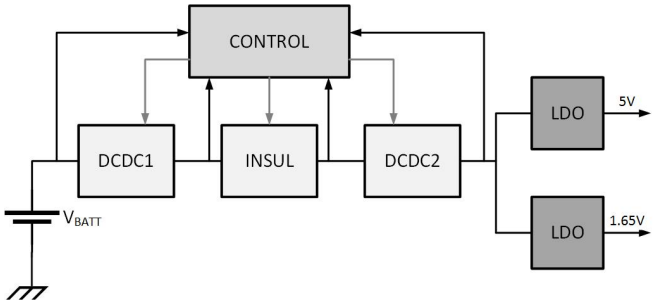

Fig. 3: Multistage architecture of the complete ATHENIS_3D 48 V DC/DC converter.

The principle of operation of the insulator block is to insert one or several serial capacitors voltage to guarantee the insulation. A switched capacitor technique has been used in order to avoid bulky inductors and transformers. If at least one switch (or more) fails, there is no possibility to have overvoltage at the output. The aim of the second converter stage is to decrease the voltage around 6 V and to keep a high efficiency level. This stage allows to obtain the VCRs 1/2 and 1/3 by using two flying capacitors and more switches. A flash ADC converter is used to choose the operating mode of both converter stages. It compares the input voltage with reference voltages and generates a digital signal for the control block. About the LDOs blocks, integrated architectures we already proposed in literature [3] have been adopted. Operating with an input voltage much lower than 48 V, the LDO regulators have acceptable efficiency.

Both the converters have been designed and simulated in all PVT (Process-Voltage-Temperature) corner cases at layout level with Cadence-Virtuoso tools and the results are compared with those obtained from the measurements. The regulation capability of each switching-capacitor DC/DC converter stage depends on the switching frequency f_{SW}, on the size of the capacitor C_{FLY} plus a terms n depending on the conversion ratio: $V_{OUT} = KVinIout/(n \cdot C_{FLY} \cdot f_{SW})$. The power supply rejection ratio (PSRR) of the whole converter in Figure 3 is at least 40 dB at low frequencies and -90 dB at the switching frequency. As result, without using inductors but just capacitors (with values from 100 nF to 10 μF) the design allows to regulate high input voltages (one order of magnitude of variation from 6 V to 60 V).

With respect to 48 V DC/DC converters using inductors, our converter has a comparable efficiency when supplying low-voltage loads with output currents limited to hundreds of mA, and reduces size and weight avoiding inductors and transformers.

3 Testing Plan

The architecture for a preliminary testing of the system is shown in Figure 4. Since the test chip version only implements the first DC/DC stage of the complete ATHENIS_3D system, its testing has been designed in order to measure the performances of a series of two stages.

The switching phases control is implemented on the microcontroller unit: no digital part has been included in the test chip version of ATHENIS_3D. The goal of such

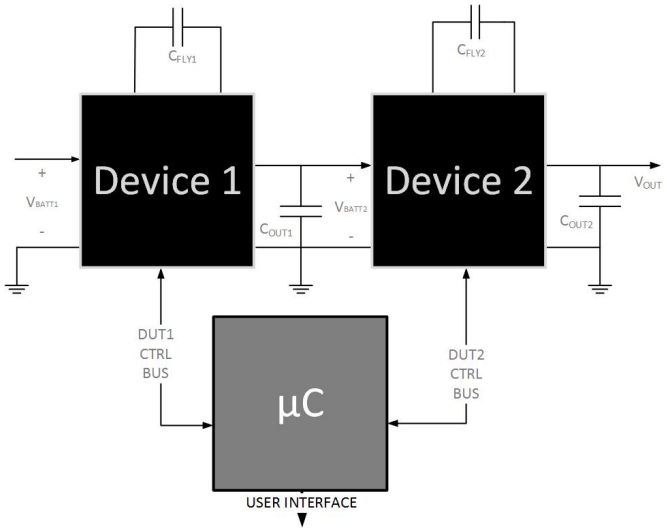

Fig. 4: Test concept scheme.

architecture is to measure some of the performance parameters of the DC/DC, both for a single stage and for a series configuration, and to check the reliability of the ASIC simulations in real application. The devices under test (hereafter, DUTs) must be mounted in the same functional configuration (i.e. flying and load capacitance included). An anti-EMI filter to block the electromagnetic conductive interference to V_{BATT} source has been designed for this application, too.

3.1 Microcontroller block

The microcontroller block is responsible for generating the phases for driving the power MOSFETs acting as switch (of the architecture shown in Figure 1) of both DUTs. It performs the skip control in case of too large output voltage; it also initializes the devices with a proper startup signal. The chosen microcontroller for this application was an ATMEL®AT32UC3L064. It has been adopted in a ready-to-use evaluation board, UC3-L0 XPLAINED, for its good availability of I/O PINs to be connected to DUTs.

For each DUT, seven phase signals had to be generated, whose behavior depended on the current DUT input voltage state. Some of the phases for the second stage can be kept in fixed (logic 1 or logic 0) state, since the testing architecture allows the second DUT to be driven only in unitary and half modes (as shown in previous section). Phases are conventionally called 'positive' when the positive edge is happening in the first half of the period, 'negative' when the positive edge is in the second half of the period. Some phases are always on or off, depending on the current driving mode. An important condition on the phases driving is that two in-phase signals must be fully overlapped: the first signal set must be reset after the reset event of the other signal. The period of the phases lasts 11.125 μs, corresponding to about 90 kHz. The phase generation has been implemented by the configuration of a microcontroller timer counter resource.

The skip control is only enabled once a switching event has been fully completed (i.e. after all the rising and falling edges at the beginning and in the middle of a period). If the skip request is received, all phases are frozen in their current state. The startup procedure simply keeps in set (i.e. '1') state a signal for a period of 1.79 ms.

3.2 Parameters under test

The device parameters to be measured are summarized in Table 1.

Test name	**Procedure**	**Notes**
Line Regulation test	Sweep V_{BATT} input and measure DUT1 and DUT2 output voltage	*Test performed in nominal load conditions*
Load Regulation test	Sweep load with nominal V_{BATT} applied to input	
Efficiency test	Measure the ratio between output and input electrical power	*Wait the transients to be finished*
No load test	Measure output voltage in case of zero-current sinking	
Ripple test	Measure min, mean and max output voltages to find out ripple factor	*Ripple factor γ is the ratio between ripple voltage and mean voltage*

Table 1: DC/DC parameters under test

4 Test setup and results

The testing board (Figure 2) developed for beta version of ATHENIS_3D implements the testing scheme proposed in previous section (Figure 4). It has the input filter onboard and configurable connectors to measure the output voltage of both stages. Other connectors are used to link the microcontroller I/O signals (switching phases, skip and startup signals) and to monitor them, and to configure the phase generation mode for both the DUTs. The SMD capacitors used for test purposes were 3.3 μF for the C_{fly} and 10 μF for the C_{out}, for both DUTs.

Some preliminary test have been performed, following the test protocol summarized in Table 1. Input voltage range has been swept from 6 V to 60 V and output current has been set to a wide range of values, from 0 A up to 1 A, in order to simulate different load conditions. Preliminary results show correct operations for nominal input voltage (48 V) and load currents up to 240 mA. In the same input nominal condition and for 150 mA sunk at the output, we measured an efficiency of 80.5%. An important parameter for such a switching architecture is the output ripple voltage. The ripple factor was measured to be 0.13% in nominal conditions ($V_{BATT} = 48\ V$, $I_{LOAD} = 150mA$): the output voltage was 10.33 V, while the peak-to-peak ripple voltage excursion was 13 mV.

Some more detailed data have been acquired in order to characterize the architecture by ranging the load current (Load Regulation Test). In Figure 5 are shown output voltages (of both devices) for a $V_{BATT} = 48\ V$ test. The load current has been swept from 0 A up to 400 mA.

As an innovation with respect to the state of the art, the proposed 48 V DC/DC converter avoids cumbersome transformers vs. inductor based converters [3] [4], and increases the working voltage and current levels vs. known switched-cap converters [5] [6], typically limited to low-power applications.

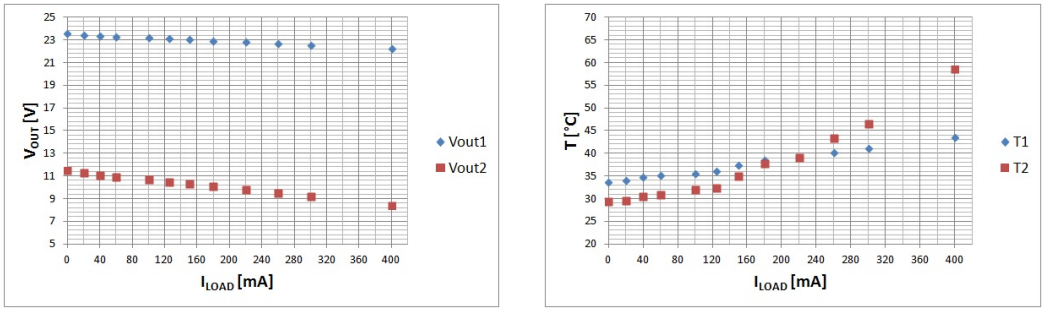

Fig. 5: Load Regulation test results. Output voltages profiles and temperature profiles for both devices by sweeping load current.

5 Conclusions

This work aims at presenting a novel architecture for implementing next-generation DC/DC converters in harsh automotive application [7] [8], where the power line at 48 V is expected to spread in electric car applications. The architecture is based on switching capacitors, in order to reduce die size by avoiding the usage of inductors.

This work has been carried out within the EU project ATHENIS_3D. The test chip architecture has been presented and evaluated through experimental measurements. At 48 V its ripple factor is 0.13%, whereas the measured efficiency is 80.5% Experimental results of the test chip and deeper simulations suggest the final architecture of ATHENIS_3D to meet the efficiency and stability requirements.

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