Technical Report No. 32-670

Field-Effect Transistors as DC Amplifiers

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The characteristics and the operation of field-effect transistors as dc amplifiers are reviewed, followed by a discussion of circuit techniques for providing low drift performance. Some considerations to questions of temporal stability and to methods of measuring field-effect transistor characteristics are given, and a short discussion of future trends is also included.

Author

I. INTRODUCTION

The field-effect transistor (FET) was investigated for application as a dc amplifier. The investigation was predicated on the fact that, where signal-source resistance is high or where amplifier input resistance must necessarily be large, the low input current of the FET would be an important advantage over the conventional bipolar transistor. It also was suspected that a lower drift might be achieved, even for low impedance applications.

In this Report, following the short review of FET characteristics, subjects covered are drift mechanisms and bias, device selection, circuits, stability, measurements, FETs as modulators and choppers, and future predictions.

II. FET CHARACTERISTICS

The external characteristics of the FET have been described in many publications (Ref. 1–5): the input impedance is very large; the drain characteristics have a large variational resistance resembling a vacuum tube pentode; and the input (gate) current is very low, being the leakage current of a reverse-biased p-n junction.

Figure 1 shows a sketch of a typical, diffused, planar FET; a geometry of such form appears to be popular with most manufacturers at the present time. A p-channel device is shown, but n-channel devices are similar.

Geometrical factors important in the FET are length L, width W, and thickness $2a$ of the channel. These dimensions, plus the type of junction (e.g., abrupt, graded, etc.) and the amount of doping, determine the three most important operating characteristics of the device:

1. Pinch-off voltage V_P.
2. Drain current I_{DSS} in pinch-off region at zero-gate bias ($V_{gs} = 0$; $V_{ds} > V_P$).
3. Transconductance g_{m0} for same conditions as 2 above.

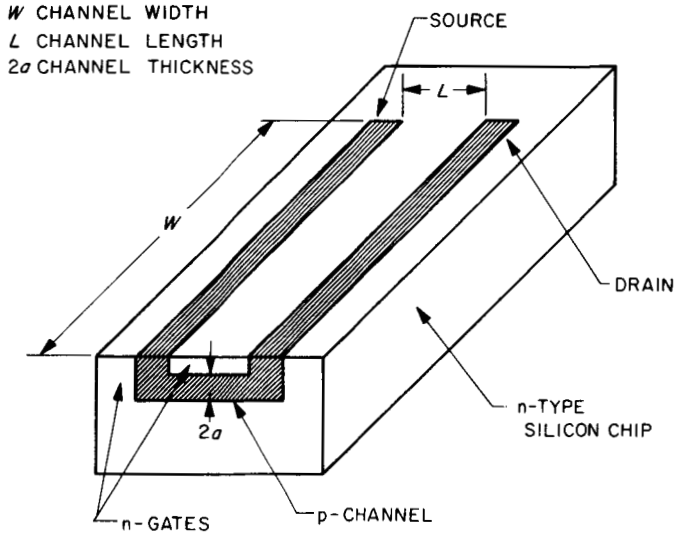

Fig. 1. Typical geometry of FET

According to Shockley (Ref. 4), the operating characteristics are related to the geometry in the following manner:

$$g_{m0} = \frac{2\sigma a W}{L} \tag{1}$$

$$V_P = \frac{\sigma a^2}{2\mu K} \tag{2}$$

$$I_{DSS} = \frac{\sigma^2 a^3 W}{nL\mu K} \tag{3}$$

where

σ = conductivity of the channel (determined by doping)

μ = mobility of majority carriers in the channel

K = dielectric constant of the material ($K = 1.06 \times 10^{-12}$ farads/cm for silicon)

n = a number between 2 and 3 that is determined by the type of junction

From the above, the useful relation

$$\frac{nI_{DSS}}{g_{m0}V_P} = 1 \tag{4}$$

may be derived.

Several transfer characteristics using various simplifying approximations have been derived (Ref. 2, 4, 6–8). The most useful may be adapted from Richer and Middlebrook (Ref. 8), who state that in the drain pinch-off region

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{gs}}{V_P}\right)^n \tag{5}$$

For many present-day devices, n is very close to 2. Moreover, Middlebrook and Richer (Ref. 6–8, and 10) explain on very general grounds that n must be quite close to 2 for a wide variety of device types.

The proper signs to use within the parenthesis are a matter of some concern; if care is not taken with the sign, incorrect results can easily be obtained in any manipulations of Eq. (5).[1] For the form chosen here, V_P is always regarded as a positive number and the normal operating polarity of V_{gs} (that is, the polarity for reverse gate bias) is assigned a positive sign. For this choice of conventions, drain current decreases with larger gate bias.

Transconductance is given by

$$g_m = \frac{dI_{DS}}{dV_{gs}} = -\frac{nI_{DSS}}{V_P}\left(1 - \frac{V_{gs}}{V_P}\right)^{n-1}$$

$$= -g_{m0}\left(1 - \frac{V_{gs}}{V_P}\right)^{n-1} \tag{6}$$

Observe that for the chosen convention, transconductance is a negative number.

It will be noted that if $n = 2$, transconductance is a linear function of input voltage, and the FET has the potentiality of being a highly linear multiplier (Ref. 11 and 12).

[1]Three different sign conventions have been found in the literature.

III. DRIFT CRITERIA

A. Drift Mechanisms

In a stable FET, there are three temperature-sensitive mechanisms which contribute to drift:

1. Leakage current from gate to channel. This is the leakage current of a reverse biased p-n junction and shows an exponential temperature dependence.
2. "Built-in" voltage (contact potential) between gate and channel. This is exactly analogous to the V_{be} of a transistor and shows the same linear dependence upon temperature.
3. Channel conductance. The semiconductor in the channel has conductance that varies with temperature due to changes in mobility.

An approximate drift equivalent circuit is shown in Fig. 2. Leakage current i_L is the familiar diode reverse current that approximately doubles for every 10°C increase in temperature. It is also somewhat dependent upon the voltages applied to the device (apparently more dependent than simple diode reverse current). The effective amplifier drift caused by variation of i_L depends upon the internal resistance of the signal generator. If the internal resistance is sufficiently small, the drift due to i_L may be negligible.

The contact potential V_c is 0.5 to 0.7 v in silicon at room temperature and has a temperature coefficient of -1.8 to -2.5 mv/°C. The exact numbers are determined by the channel doping; the magnitude of temperature coefficient is typically in excess of 2 mv/°C, because channel resistivity is typically quite high. The exact value of the contact potential is of little concern to the circuit designer in that it cannot be measured externally by any practical means.

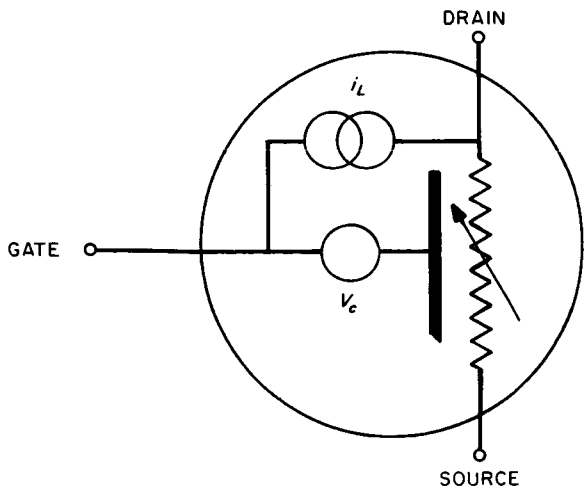

Fig. 2. Drift equivalent circuit of FET

The contact potential is a measure of the built-in depletion region in the channel at zero bias. A negative temperature coefficient of V_c means that the depletion region narrows (i.e., conducting portion of channel widens) and the channel can carry more current as the temperature rises.

The conductivity of silicon, within the range of normal operating temperatures, decreases with increasing temperature. For a given applied voltage between drain and source, decreased conductance due to an increased temperature results in a smaller channel current. Silicon has a temperature coefficient of conductance between -0.5 to -0.8%/°C at room temperature. A value of -0.7% appears to be typical.

B. Bias for Zero Drift

Contact potential and conductivity have opposite effects upon channel current. It has been shown (Ref. 13–15) that it is possible to bias an FET in such a manner that the two effects exactly cancel, leaving a device having very low drift over a very wide temperature range.

In Appendix A, equations presented earlier are used to derive several related bias conditions which provide zero drift. The results are summarized in this section.

Under very general conditions, involving no approximations or assumptions regarding the form of the transfer function (Ref. 14), it can be shown that drain current will be independent of temperature provided that the FET is biased so that

$$\frac{I_{DS}}{g_m} = \frac{\dfrac{\partial V_c}{\partial T}}{\dfrac{1}{\sigma}\dfrac{\partial \sigma}{\partial T}} \tag{7}$$

where σ is channel conductivity. If values of

$$\frac{\partial V_c}{\partial T} = -2.2\,\text{mv/°C}$$

and

$$\frac{1}{\sigma}\frac{\partial\sigma}{\partial T} = -0.007/°\text{C}$$

are taken as typical, then, for zero drift,

$$\frac{I_{DS}}{g_m} = 0.31\,\text{v} \tag{8}$$

If a power-law transfer function (Eq. 5) is assumed to be correct, it may be shown that another description of the zero drift condition is provided by

$$V_{gs} = \frac{\frac{1}{\sigma}\frac{\partial\sigma}{\partial T}V_P - n\frac{\partial V_c}{\partial T}}{\frac{1}{\sigma}\frac{\partial\sigma}{\partial T}} \tag{9}$$

Taking $n = 2$ and the above values for the derivatives yields

$$V_{gs} = V_P - 0.63\,\text{v} \tag{10}$$

for zero drift. It may be seen that zero drift at zero bias will occur for $V_P = 0.63$ v for the type of FET that has the assumed properties. Experiments with low pinch-off, diffused FETs have verified Eq. (10).

One more condition may be derived; under the same restrictions and numerical values that apply to Eq. (10), it can be shown that the drain current for zero drift is

$$I_{DS} = I_{DSS}\left(\frac{0.63}{V_P}\right)^2 \tag{11}$$

These three equations are actually different methods of stating the same condition; if any one is fulfilled, the other two must also hold.

Almost any FET can be biased to the zero drift condition. (The exception would be for very low V_P units where forward bias on the gate would be required.)

The numerical values (Eq. 8, 10, and 11) are a result of specific assumptions regarding values of n, $(1/\sigma)(\partial\sigma/\partial T)$, and $\partial V_c/\partial T$. These numbers are all a function of the FET construction and doping, so the formulae should not be applied directly without first verifying the assumed values.

IV. DEVICE SELECTION

It is assumed in this section that the geometry of Fig. 1 is applicable. Some of the conclusions to be drawn on the basis of this assumption may have to be altered if a different geometry is employed. The device of Fig. 1 is fabricated by masking and diffusion techniques. The three dimensions of interest are width, length, and thickness of the channel. Of these dimensions, width is ordinarily by far the largest (5–500 mils) and is very accurately determined by masking. Length is appreciably smaller (0.5–5 mils); it is determined primarily by the masking but diffusion will have some effect. Accuracy of length cannot be as good as accuracy of width. Thickness is very small (less than 1 μ for low pinch-off units) and is much more difficult to control than the masked dimensions. (For additional information on typical devices see Ref. 3, and 16–19).

It may be seen (Eq. 1–3) that electrical characteristics are linearly proportional to length and width but that pinch-off voltage varies with the square of thickness and drain current varies with the cube. Assuming that all devices with the same type number from one manufacturer are made from the same mask, it may be seen that variations in thickness should be most responsible for the variations of electrical properties between different units; this assumption will be used later.

It was previously shown that almost any FET can be biased to the zero-drift condition and that this bias may be determined once pinch-off voltage is known. Consider criteria now for selection of units, subject to the constraint that the unit will be biased for zero drift.

Several quantities of interest are the gate leakage, the input capacity, and the gain. Leakage and capacity are primarily dependent upon junction area (and surface treatment for the leakage) and are relatively fixed for any device type. To minimize these factors, a small-area device is needed, but once the device type is chosen these factors can be further reduced only by a culling process among many units of the type.

Gain is proportional to transconductance which, in turn, is proportional to channel width. A large width is needed for large transconductance, and this requirement is in conflict with the small area requirements for small leakage and capacity. Some compromise is needed; this compromise is made in the choice of device type.

After a type has been chosen, it is desirable to select among units to obtain the maximum gain. It is assumed that the only difference between units of the same type is in the channel thickness and that this difference accounts for the spread of electrical characteristics.

With this assumption, and imposing the zero-drift constraints of the preceding section, it is relatively simple (Appendix B) to combine Eq. (1), (2), and (6) to obtain the result that operating transconductance is proportional to $(V_P)^{-\frac{1}{2}}$ (provided $n = 2$). A graph of normalized transconductance vs. pinch-off voltage is plotted in Fig. 3.

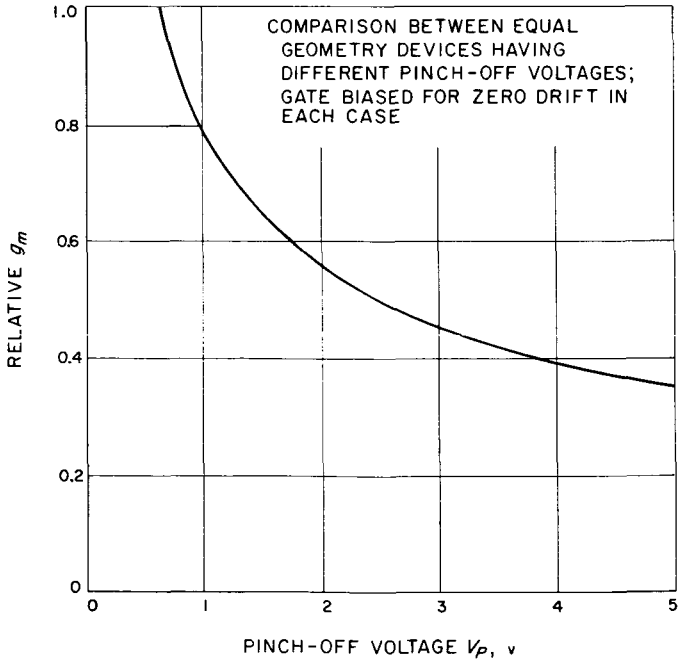

Fig. 3. Relative operating transconductance

It is evident that V_P should be small in order to obtain the largest gain. Note that this conclusion is arrived at despite the fact that the combination of Eq. (1) and (2) shows that zero bias transconductance (g_{m0}) increases for increasing V_P.

By means of a similar analysis, it is easily shown that operating drain current (for the zero-drift condition) is also proportional to $(V_P)^{-\frac{1}{2}}$. Evans (Ref. 13) makes use of empirical statistics of one manufacturer's product and concludes that transconductance and current actually vary as $(V_P)^{-0.4}$, which is reasonably close to $(V_P)^{-\frac{1}{2}}$.

From experience with tubes and with regular transistors, it appears likely that a differential circuit using a long-tailed pair would have many desirable features. For best results, the two units of the pair should be closely matched. Selection of transistors for such a pair might proceed somewhat as follows:

1. Choose device type from data sheet information. Such factors as transconductance, leakage, range of pinch-off voltages, and capacitance would influence the choice.
2. From a batch of the chosen type, select units having sufficiently low pinch-off voltage.
3. If necessary, make drift tests to verify that the zero-drift bias conditions as outlined here are applicable to the chosen device type.
4. Select pairs of units on the basis of matching pinch-off voltages as closely as possible.
5. Check pairs to be certain that drain currents are closely matched. The currents will be well matched if pinch-off voltages match, provided that the theory in this Report is correct. However, if some parasitic effect has been ignored (ohmic resistance in the source lead is one possibility) the current match might be poor. Strictly speaking, currents should be compared at the actual intended operating point. As a practical matter, it is probably allowable to measure the zero bias current, I_{DSS}.
6. Check units for acceptable leakage levels at the highest operating temperature.

This process may seem somewhat complicated, but it is actually simpler than the process for selecting a pair of bipolar transistors, where it is necessary to match current gain at all temperatures and, also, to match base to emitter voltages.

V. CIRCUITS

Because of the inherent drift balancing nature of an FET, it is feasible to operate the FET in a single-ended circuit and still obtain useful low-drift performance. However, the adjustment for very low drift may prove to be somewhat touchy. Evans (Ref. 13) derives an expression for the drift that results from a misadjustment of drain current from the optimum value; if the current is 1% high or low, the equivalent input drift will be 11 μv/°C. For a precision amplifier, evidently it is necessary to maintain very close control over the power supplies and bias network.

Moreover, to establish a current with any degree of accuracy, it is necessary to use a relatively large resistance in the source lead (analogous to the large resistance in the cathode lead for tubes or to the emitter lead for bipolar transistors). In a dc amplifier, this resistance unavoidably causes degeneration and reduction of gain, an occurrence which might cause the drift of the second stage to become significant.

The basic circuit for a balanced amplifier is shown in Fig. 4. It is essentially the same as the familiar long-tailed pair that has been used with tubes and bipolar transistors. Analysis of the circuit follows the same lines as that for the earlier devices and the same benefits of common mode rejection and drift cancellation are obtained. Here only the features peculiar to FETs will be considered.

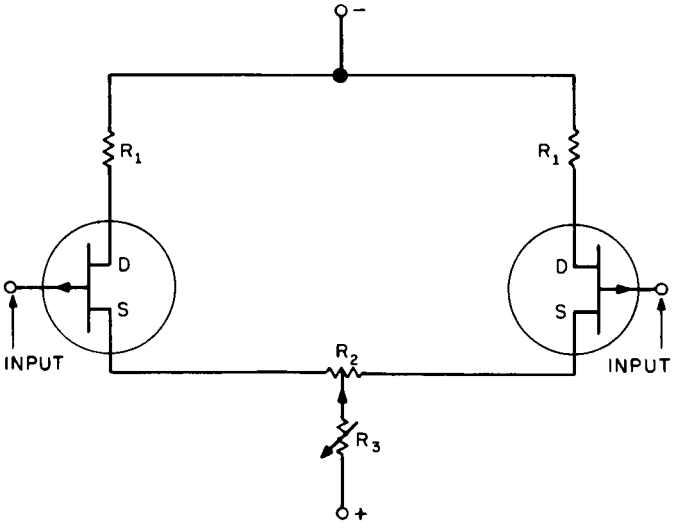

Fig. 4. Balanced amplifier

In the circuit resistors R1 represent the total load resistance, including the effects of the following stage. For best rejection of common mode effects, these resistors should be closely matched.

It is worth noting that the load resistors might have to be quite large in order to obtain useful gain from the first stage. In a small geometry device the transconductance might typically be as small as 100 μmhos; so that to obtain a gain of 10, resistors R1 must be 100 kΩ.

Because of this requirement for a large load resistance, it is essential that the following stage have a large input resistance; another pair of FETs would appear to be ideal in this respect. If bipolar transistors are used, they must be biased and bootstrapped for high input resistance in a manner that would not be optimum for either gain or bandwidth. Furthermore, the base current of bipolar transistors must be well balanced so as not to cause appreciable drift due to the drop in the resistors R1.

Resistor R3 is the conventional "long tail" of the pair and is used to establish the operating currents of the FETs. It may be replaced by an active constant-current source if desired. This is a variable resistor to permit adjustment of the current so that the FETs can be set at their zero-drift operating currents. When this is done, temperature unbalances and temperature transients do not cause drifts and offsets as they do in the case of bipolar transistors where drift cancellation occurs solely because of matching between the two transistors. Where each device is individually set for zero drift, the temperature equalizing problem is not nearly so critical. (As a corollary, if temperatures of the pair are well equalized —e.g., by expedients such as placing both devices in the same case—the residual temperature differential will have a much smaller effect than it will have for two bipolar transistors similarly encapsulated.)

The two FETs cannot be matched exactly in the selection process; there is certain to be some small difference in their optimum bias points. It is the purpose of R2 to compensate for these differences by actually biasing each FET to its proper bias for zero drift. Observe that R2 is not a zero-offset adjustment; instead, it is a drift compensation and must be set by a process of varying the temperature and determining drift with R2 held at various settings.

In the device-selection process, it should be very easy to match low pinch-off FETs within 0.25 v, and quite reasonable to match them within 0.1 v. For this reason, R2 should not be required to have much range of adjustment and, therefore, need not have a particularly large resistance. As a result, degeneration and loss of gain should be small and unimportant.

As a consequence of this adjustment method, the individual currents, and, therefore, the drain voltages of the two units will not be equal and there will be an offset at the output. However, this is a fixed offset if R2 and R3 have been adjusted properly, and it can be corrected by a conventional offset adjustment control.

Next, consider methods of compensating for gate leakage current. Devices are available with rated leakage of less than 50 picoamps at room temperature and less than 150 nanoamps (na) at 150°C. At 100°C the leakage would be 5 na. For a differential pair, it is often possible to equalize the resistances seen by each input terminal. In that case, the net drift is caused by the difference in leakage between the two inputs.

Other situations arise for which it is desirable to minimize the currents in each individual input. A cancellation scheme in which the leakage of a silicon diode is balanced against the gate leakage is shown in Fig. 5. In this circuit the FET leakage current i_L (Fig. 2) is counteracted by the leakage current of a reverse biased diode. The diode is selected to have the same leakage current as the FET at the highest operating temperature.

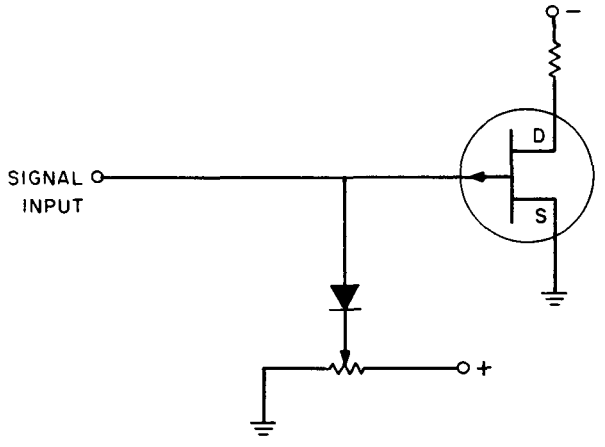

Fig. 5. Leakage current cancellation

VI. STABILITY

Up to this point, an assumption has been implied that temperature is the only cause of drift in device characteristics and that an FET is stable over time. Theoretically, the device is indeed time-stable since there is no fundamental mode of deterioration or consumption of substance. In this respect, the FET is the same as regular transistors and diodes.

However, the possibility is very real that the detailed manufacturing technology can result in less than ideal behavior and in deterioration in an actual device. In common with conventional transistors, an FET can suffer from worsening leakage due to surface contamination and from catastrophic failure due to metallurgical bonding difficulties (purple plague). These are avoided by various techniques known to the manufacturers.

Apparently there is another difficulty that is peculiar to diffused FETs; that is, the diffusion process sometimes does not stop completely in the diffusion oven but continues indefinitely at a slow rate. Eventually, the two gate layers diffuse together; the channel is permanently pinched off, and the device is rendered useless. To guard against such failure occurring in an operating circuit, it is advisable to burn in devices at some elevated temperature. Any change in pinch-off voltage during the course of burn-in is cause for alarm.

Other devices are diffused; the question might be asked why do FETs get into difficulty from continuing diffusion whereas other devices seem unaffected. In a simple diode, for example, continuing diffusion would result in a migration of the exact location of the junction within the

semiconductor and some change in the impurity gradient. Very careful measurements might show a change in diode characteristics, but it would be expected to be very small.

In an FET on the other hand, migration of junctions brings the two junctions closer to each other, thereby narrowing the channel thickness. Since FET characteristics are critically dependent upon channel thickness, the characteristics would change substantially. Any difficulty would be particularly severe in a low pinch-off voltage unit where the channel thickness is 1 μ or less.

It is not to be inferred from this discussion that diffused FETs are necessarily unreliable and unstable—in fact, exactly the opposite is true. Most FETs being built today are of the diffused type and most are thought to be stable.

It is possible to build an FET in such manner that it exhibits a negative-resistance gate characteristic (Ref. 1 and 2). A device of this type could have unstable behavior in a high resistance circuit; whereas, it would be perfectly acceptable in a low resistance circuit. The causes of negative resistance are well known, and the phenomenon should not appear in an FET except by design.

VII. FET MODULATORS AND CHOPPERS

The very nearly square-law FET characteristic permits the construction of quite good multipliers (Ref. 11 and 12). Several authors describe high-level, balanced, four-quadrant multipliers using a matched pair of FETs.

For low-level (microvolt) applications, FETs have the great advantage of exhibiting precisely zero-offset voltage in the ON (zero bias) condition. Offset current arises in the OFF condition; this current is the gate to channel reverse leakage and can be very small.

It must be recognized that an FET is a voltage-variable resistance and not a good switch. The FET OFF-resistance can be extremely large, but the ON-resistance is also large: 200–10,000 Ω, typically. Thus, the efficiency of an FET chopper will not be as high as the efficiency of a bipolar-transistor chopper. However, low efficiency is equivalent only to signal attenuation which may be compensated by additional ac amplification. A much more serious problem is the transfer of the carrier drive voltage into the signal circuits by way of gate-to-channel capacitance. Because the chopper operates at a relatively high impedance level, even small capacitances can transfer excessive amounts of drive. Such carrier leakage is indistinguishable from signal offset.

In order to obtain good results, it is necessary to use a low capacitance FET (this choice will not only tend to minimize dc leakage current but also will increase the FET ON-resistance) and to employ some scheme of neutralization. The latter expedient is complicated by the fact that the FET capacitance is nonlinear; it varies substantially between the OFF and ON conditions (Ref. 9 and 20). Neutralization by means of a simple, passive capacitor can have only limited effectiveness. Despite these difficulties, a simple FET chopper has been demonstrated (Ref. 21) which exhibited a drift in offset of only 105 μv between 25 and 100°C.

Better performance should be possible in a circuit originally devised for bipolar-transistor choppers (Ref. 22). The circuit is shown in Fig. 6. Two FETs are used; each feeds one input of an ac differential amplifier, and the drifts and leakages of one FET compensate for the like deficiencies of the other. If the two FETs are matched for pinch-off voltage, capacitance, and leakage current, their drift performance should be extremely good.

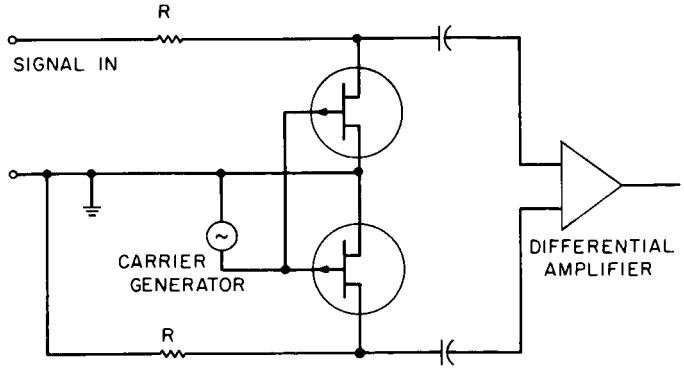

Fig. 6. Balanced chopper

VIII. MEASUREMENTS OF FET CHARACTERISTICS

FET currents can be very small; this is particularly true of gate currents. In order to obtain correct measurements, it is necessary to avoid any extraneous leakage currents or power line pickup. Otherwise, current measurements are straightforward.

Transconductance may be determined by a bridge technique (Fig. 7). At null, the resistance between drain and gate is the reciprocal of transconductance. It is necessary that the reactance of the blocking capacitor at the frequency of measurement be negligible compared to R_F and that the reactance of the internal capacitor C_{gd} be very large compared to R_F. Capacities to ground do not affect the measurement.

It is somewhat more difficult to measure pinch-off voltage V_P. For a rough approximation, the knee of the zero-bias drain-current vs. drain-voltage curve may be taken as V_P. This knee can be obtained on a curve tracer, but the accuracy of the method is poor.

Another approach is to determine the bias needed to reduce drain current to zero. Unfortunately, current never does reduce to zero (because of leakage), so this method is usually unsatisfactory.

A better method is somewhat indirect. Richer and Middlebrook (Ref. 8) have pointed out that if the FET transfer characteristic follows a power-law (Eq. 5), then the plot of the ratio of drain current to transconductance I_{DS}/g_m vs. gate voltage is a straight line with the magnitude of the slope equal to the reciprocal of the exponent n and the intercept on the abscissa equal to V_P. Generating such a plot can be quite tedious, but it should yield good results for V_P.

Measurements of I_{DS}/g_m were performed on a number of FETs, and some of the results are shown in Fig. 8. Slopes may be seen to be very close to 1/2 which means $n \approx 2$. Most data closely fit good straight lines, but some curves deviate markedly at very low current levels. Simple extrapolation of the linear portion of the curves will yield an intercept and a value for V_P.

Where the exponent $n = 2$, the plot of g_m vs. V_{gs} should be a straight line, and the intercept should be at $V_{gs} = V_P$. These curves have been plotted in Fig. 9 for several of the FETs shown in Fig. 8. The data provide quite a good fit to straight lines, and close examination shows that the intercepts are very nearly the same as in Fig. 8.

Thus, where $n \approx 2$ and g_m is a linear function of V_{gs} (the usual case for most FETs), it is feasible to determine V_P from a plot of g_m. This procedure entails much less effort than utilizing a plot of I_{DS}/g_m.

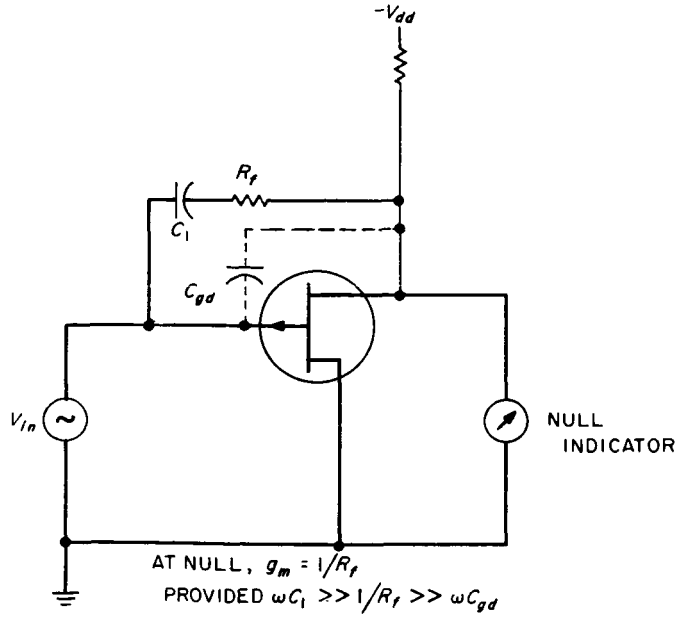

Fig. 7. Transconductance measurement

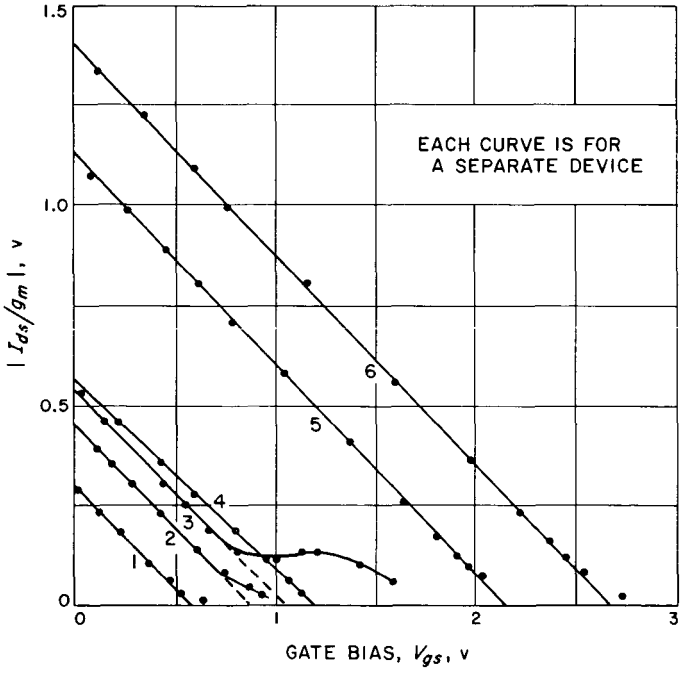

Fig. 8. Measured FET characteristics

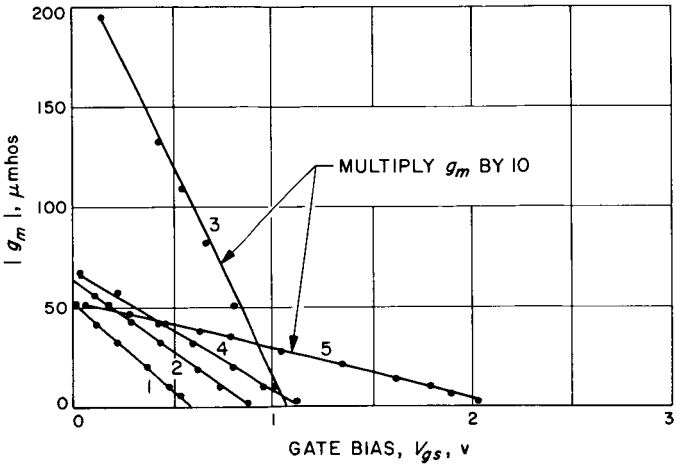

Fig. 9. Measured transconductance

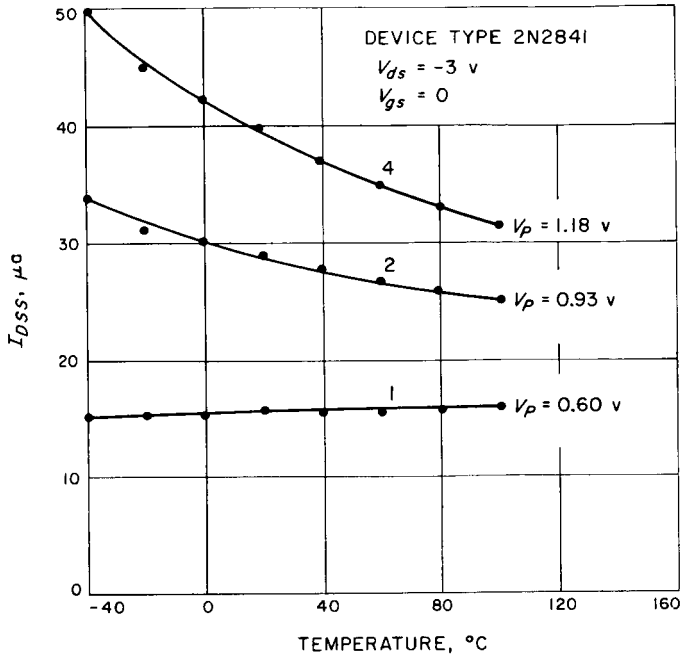

Fig. 10. Drain current vs. temperature

Measurements of I_{DSS} vs. temperature were performed for several units; the results are shown in Fig. 10. The behavior of unit number 1 is of particular interest; it exhibits a very small, almost zero, positive temperature coefficient. Pinch-off voltage at room temperature was determined to be 0.60 v which is slightly less than the 0.63 v predicted by Eq. (10) for zero drift. The ratio I_{DSS}/g_{m0} was determined to be 0.30 v which may be compared to the 0.31 v required by Eq. (8) for zero drift. These measurements may be regarded as good experimental verification of the analytic expressions.

IX. PREDICTIONS FOR THE FUTURE

Present day, good quality FETs are quite expensive. One safe prediction is that prices will fall as demand rises and as more manufacturers enter the field.

The major attraction of FETs is their high input impedance, a fact the manufacturers are well aware of. It is reasonable to expect continuing improvements in leakage current, input resistance, and reduction of capacitance.

The advantages of low pinch-off FETs have been widely recognized (Ref. 23). Several devices specifically designed (or selected) for low V_P are available now; the number of such types will undoubtedly increase.

This Report has shown the desirability of matched FET pairs, preferably in a single case. It is hoped that manufacturers will provide such devices.

All of the material of this Report has been concerned with p-n junction FETs. This is the only type of FET commercially available today, and the situation is unlikely to change significantly for the next several years at least. However, work is being performed on insulated-gate

FETs (Ref. 24–26) where the gate is separated from the channel by a very thin insulator (e.g., silicon oxide). The only gate leakage is that due to nonideal behavior of the insulator so that input resistances of 10^{15} Ω are feasible. These devices potentially are easier to fabricate than p-n junctions and, therefore, may be expected to appear in great quantities when research and development are completed.

NOMENCLATURE

a	one-half channel thickness
C_{gd}	capacitance between gate and drain
g_m	transconductance
g_{mo}	zero bias transconductance
i_L	FET leakage current
I_{DS}	drain current
I_{DSS}	drain current at zero bias
K	dielectric constant of the material
L	channel length
n	number between 2 and 3, determined by junction
T	temperature
V_{be}	voltage between base and emitter of bipolar transistor
V_c	contact potential between gate and channel
V_{gs}	voltage applied between gate and source
V_P	pinch-off voltage
W	channel width
σ	conductivity of channel
μ	mobility of majority carriers in the channel

APPENDIX A

Derivation of Zero-Drift Conditions

Start with Eq. (5)

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{gs}}{V_P}\right)^n$$

and substitute the expression

$$I_{DSS} = \frac{\sigma^2 a^3 W}{nL\mu K}$$

for I_{DSS} to obtain

$$I_{DS} = \frac{\sigma^2 a^3 W}{nL\mu K}\left(1 - \frac{V_{gs}}{V_P}\right)^n \tag{A1}$$

However, conductivity is the product of mobile charge density by charge mobility, i.e., $\sigma = \rho\mu$. Eliminating μ from Eq. (A1) yields

$$I_{DS} = \frac{\sigma\rho a^3 W}{nLK}\left(1 - \frac{V_{gs}}{V_P}\right)^n \tag{A2}$$

At normal temperatures the donors or acceptors are all fully ionized so ρ is independent of temperature. Likewise, a, W, n, L, and K are also temperature independent. The only temperature sensitive terms are conductivity and contact potential.

Conductivity appears explicitly in Eq. (A2) but an artifice must be used to account for the contact potential. To this end, redefine V_{gs} to consist of two parts: $V_{gs} = V_X + V_N$ where V_X is the actual external voltage applied between gate and source terminals, and V_N is an internal voltage that represents the variable portion of the contact potential. At temperature T contact potential is thereby defined as

$$V_c(T) = V_c(T_0) + V_N(T) \tag{A3}$$

where T_0 is a reference temperature and $V_N(T_0) = 0$.

Regard V_X as constant; $V_c(T_0)$ is also constant. As a result,

$$\frac{\partial V_{gs}}{\partial T} = \frac{\partial V_N}{\partial T} = \frac{\partial V_c}{\partial T} \tag{A4}$$

at $T = T_0$. That is to say, the change of contact potential is treated exactly as if it were an externally applied signal. This is a somewhat inelegant expedient, but it provides the necessary grasp upon V_c.

With this definition, differentiate drain current with respect to temperature; set the derivative equal to zero; and solve for the various appropriate quantities.

$$\frac{\partial I_{DS}}{\partial T} = 0 \tag{A5}$$

$$= \frac{\rho\sigma a^3 W}{nLK}\left[\left(1 - \frac{V_{gs}}{V_P}\right)^n \frac{1}{\sigma}\frac{\partial\sigma}{\partial T} - \frac{n}{V_P}\left(1 - \frac{V_{gs}}{V_P}\right)^{n-1}\frac{\partial V_c}{\partial T}\right]$$

If Eq. (5), (6), and (A2) are applied, the result is

$$I_{ds}\frac{1}{\sigma}\frac{\partial\sigma}{\partial T} - |g_m|\frac{\partial V_c}{\partial T} = 0 \tag{A6}$$

which is readily manipulated to obtain Eq. (7) for one statement of the zero-drift condition.

It should be noted that the assumption of power-law behavior (Eq. 5) is not necessary to derive Eq. (7); Hoerni and Weir (Ref. 14) obtain the same result making no assumption regarding the form of the transfer characteristic.

It is clear, returning to Eq. (A5), that the bracketed term must be equal to zero if the whole equation is to be true.

Factoring out the common term gives

$$\left(1 - \frac{V_{gs}}{V_P}\right)\frac{1}{\sigma}\frac{\partial\sigma}{\partial T} - \frac{n}{V_P}\frac{\partial V_c}{\partial T} = 0 \tag{A7}$$

When this equation is solved for V_{gs}, the result is

$$V_{gs} = \frac{\left(\frac{1}{\sigma}\frac{\partial\sigma}{\partial T}V_P - n\frac{\partial V_c}{\partial T}\right)}{\frac{1}{\sigma}\frac{\partial\sigma}{\partial T}} \tag{A8}$$

which is the same as Eq. (9).

An expression for the drain-current condition for zero drift is obtained by taking the value of V_{gs} determined from Eq. (9) and substituting it into Eq. (5). The result, for the numerical values assumed, is given in Eq. (11).

It has been demonstrated that an FET may be biased in such manner that drain current is independent of temperature. Further, similar analysis shows that the temperature coefficient of transconductance at the bias for zero drift will always be negative and is given by

$$\frac{1}{g_{m0}}\frac{\partial|g_m|}{\partial T} = -\frac{0.0022}{V_P} \tag{A9}$$

This expression very roughly matches published curves on some manufacturer's data sheets.

Additional analysis has shown that g_m will be temperature independent if $V_{gs} = V_P - 0.315$ v. This is equivalent to stating

$$I_{DS} = I_{DSS}\left(\frac{0.315}{V_P}\right)^2$$

This expression can be manipulated further to show that zero change of gain occurs at a drain bias current that is ¼ of the current required for zero drift (Ref. 15).

There has been no opportunity for experimental verification of these transconductance conditions, and there should not be too much confidence placed upon them. However, it is certain that there is no bias condition that can provide zero drift and constant gain simultaneously.

APPENDIX B

Derivation of Operating Transconductance

From Eq. (6), transconductance is given by

$$|g_m| = g_{m0}\left(1 - \frac{V_{gs}}{V_P}\right)^{n-1}$$

Assume $n = 2$ and impose the zero-drift bias condition (Eq. 10)

$$V_{gs} = V_P - 0.63\,\text{v}$$

Substituting Eq. (10) into Eq. (6) yields

$$|g_m| = \frac{0.63 g_{m0}}{V_P} \tag{B1}$$

From Eq. (1)

$$g_{m0} = \frac{2\sigma a W}{L}$$

and Eq. (2)

$$V_P = \frac{\sigma a^2}{2\mu K}$$

produces

$$a = \left(\frac{2\mu K V_P}{\sigma}\right)^{1/2} \tag{B2}$$

so that

$$g_{m0} = \left(\frac{2\mu K V_P}{\sigma}\right)^{1/2}\left(\frac{2\sigma W}{L}\right)$$

$$= (V_P)^{1/2}(2\mu\sigma K)^{1/2}\left(\frac{2W}{L}\right) \tag{B3}$$

Assume that μ, σ, K, W, and L are all constant for all devices of a single type number. (See "Device Selection" section for justification of this assumption.)

Substituting Eq. (B3) into Eq. (B1) results in

$$|g_m| = \frac{0.63}{V_P}(V_P)^{1/2}\left[\frac{2W}{L}(2\mu\sigma K)^{1/2}\right]$$

$$= \frac{0.63}{(V_P)^{1/2}}\left[\frac{2W}{L}(2\mu\sigma K)^{1/2}\right] \tag{B4}$$

In other words, the transconductance at zero-drift bias is inversely proportional to the square root of V_P. For largest gain, V_P should be small.

REFERENCES

1. Dacey, G. C., and Ross, I. M., "Unipolar Field-Effect Transistors," *Proceedings, IRE,* Vol. 41, pp. 970–979, August 1953.
2. Dacey, G. C., and Ross, I. M., "The Field-Effect Transistor," *Bell System Technical Journal,* Vol. 34, pp. 1149–1189, November 1955.
3. Evans, Arthur D., "Characteristics of Unipolar Field-Effect Transistors," *Electronic Industries,* March 1963.
4. Shockley, W., "A Unipolar Field-Effect Transistor," *Proceedings, IRE,* Vol. 40, pp. 1365–1377, November 1952.
5. Shockley, W., "Transistor Electronics: Imperfections, Unipolar, and Analog Transistors," *Proceedings, IRE,* Vol. 40, pp. 1289–1313, November 1952.

REFERENCES (Cont'd)

6. Middlebrook, R. D., "Limits on the Power-Law Exponent for Field-Effect Transistor Transfer Characteristics," *Solid State Electronics*, Vol. 6, pp. 542–544, September 1963.

7. Middlebrook, R. D., "A Simple Derivation of Field-Effect Transistor Characteristics," *Proceedings, IEEE*, Vol. 51, p. 1146, August 1963.

8. Richer, I., and Middlebrook, R. D., "Power Law Nature of Field-Effect Transistor Experimental Characteristics," *Proceedings, IEEE*, Vol. 51, pp. 1145–1146, August 1963.

9. Richer, I., "Input Capacitance of Field-Effect Transistors," *Proceedings, IRE*, Vol. 51, p. 1249, September 1963.

10. Richer, I., "Basic Limits on the Properties of Field-Effect Transistors," *Solid State Electronics*, Vol. 6, pp. 539–542, September 1963.

11. Highleymen, W. H., and Jacob, E. S., "An Analog Multiplier Using Two Field-Effect Transistors," *Transactions, Communications Systems, IRE*, CS-10, pp. 311–317, September 1962.

12. Martin, T. B., "Circuit Applications of the Field-Effect Transistor," *Semiconductor Products*, Vol. 5, Part I, pp. 33–39, February 1942; and Part II, pp. 30–38, March 1962.

13. Evans, L., *Biasing UNIFETs to Give Zero DC Drift*, Application Note No. 100C, Siliconix Inc., Sunnyvale, California, July 1963.

14. Hoerni, J. A., and Weir, B., "Conditions for a Temperature Compensated Silicon Field-Effect Transistor," *Proceedings, IRE*, Vol. 51, pp. 1058–1059, July 1963.

15. Sevin, L. J., "Behavior of Field-Effect Transistor Characteristics With Temperature," *Seminar Notes*, Texas Instruments, Inc., Dallas, July 1, 1963.

16. Onodera, G. C., Corrigan, W. J., and Warner, R. M., "Silicon Field-Effect Transistor With Internal Epitaxial Channel," *Proceedings, IRE*, Vol. 50, p. 1824, August 1962.

17. Roosild, S. A., Dolan, R. P., and Neil, D. O., "A Unipolar Structure Applying Lateral Diffusion," *Proceedings, IEEE*, Vol. 51, pp. 1059–1060, July 1963.

18. Warner, R. M., Jackson, W. H., Doucette, E. I., and Stone, H. A., "A Semiconductor Current Limiter," *Proceedings, IRE*, Vol. 47, pp. 44–56, January 1959.

19. Weglen, H. A. Richard, "The Cylindrical Field-Effect Transistor," *Transactions, Electron Devices, IRE*, ED6, pp. 442–449, October 1959.

20. Lindholm, F. A., and Latham, D. C., "Junction Capacitance of Field-Effect Transistors," *Proceedings, IEEE*, Vol. 51, pp. 404–405, February 1963.

21. *Field-Effect Low-Level Choppers*, Application Note, Siliconix, Inc., Sunnyvale, California, November 1963.

22. Holcomb, S. W., Opp, F., and Walston, J. A., "Choppers: Their Applications and Characteristics," *Seminar Notes*, Texas Instruments, Inc., Dallas, July 15, 1963.

23. Evans, L., "The Case for Low Pinch-Off Voltages in FETs," *Electronic Design*, pp. 46–51, October 11, 1963.

REFERENCES (Cont'd)

24. Borkan, H., and Weimer, P. K., "An Analysis of the Characteristics of Insulated-Gate Thin-Film Transistors," *RCA Review*, Vol. 24, pp. 153–165, June 1963.

25. Hofstein, S. R., and Heiman, F. P., "The Silicon Insulated Gate Field-Effect Transistor," *Proceedings, IEEE*, Vol. 51, pp. 1190–1201, September 1963.

26. Weimer, P. K., "The TFT—A New Thin-Film Transistor," *Proceedings, IRE*, Vol. 50, pp. 1462–1469, June 1962.

BIBLIOGRAPHY[2]

Bechtel, N. G., "A Circuit and Noise Model of the Field-Effect Transistor," *Technical Papers Digest*, Solid State Circuits Conference, pp. 92–93, 1963.

Boeckemuehl, R. R., "Analysis of Field-Effect Transistors With Arbitrary Charge Distribution," *Transactions, IEEE*, ED-10, January 1963.

Bruncke, W. C., "Noise Measurements in Field-Effect Transistors," *Proceedings, IEEE*, Vol. 51, pp. 378–379, February 1963.

Halladay, H. E., and Bruncke, W. C., "Excess Noise in Field-Effect Transistors," *Proceedings, IEEE*, Vol. 51, p. 1071, November 1963.

Hilbiber, D., and Leistiko, O., "A High Performance Universal Operational Amplifier," *Digest of Technical Papers*, International Solid State Circuits Conference, pp. 40–41, 1963.

Latham, D. C., et al, "New Modes of Operation for Field-Effect Devices," *Proceedings, IEEE*, Vol. 51, p. 226, January 1943.

Lauritzen, P. O., "Field-Effect Transistors as Low-Noise Amplifiers," *Digest of Technical Papers*, International Solid State Circuits Conference, pp. 62–63, 1962.

Olsen, D. R., "Equivalent Circuit for a Field-Effect Transistor," *Proceedings, IEEE*, Vol. 51, p. 254, January 1963.

Pearson, G. S., "High Impedance Field-Effect Silicon Transistors," *Physics Review*, Vol. 90, p. 336, April 15, 1953.

Prior, R. C., and Shockley, W., "Joining Solutions at the Pinch-Off Point in Field-Effect Transistor," *Transactions, IRE*, ED-4, pp. 1–14, December 1953.

Van der Ziel, A., "Carrier Density Fluctuation Noise in Field-Effect Transistors," *Proceedings, IEEE*, Vol. 51, p. 1670, November 1963.

Van der Ziel, A., "Shot Noise in Thin Film Transistors," *Proceedings, IRE*, Vol. 50, pp. 1985–1986, September 1962.

[2]Listed for information only: papers relate to noise- and specific-type circuits but are not directly applicable to subject of dc amplifiers.

BIBLIOGRAPHY (Cont'd)

Van der Ziel, A., "Thermal Noise in Field-Effect Transistors," *Proceedings, IEEE,* Vol. 50, pp. 1808–1812, August 1962.

Van der Ziel, A., "Gate Noise in Field-Effect Transistors at Moderately High Frequencies," *Proceedings, IEEE,* Vol. 51, pp. 461–467, March 1963.

Warner, R. M., "Epitaxial FET Cutoff Voltage," *Proceedings, IEEE,* Vol. 51, pp. 939–940, June 1963.

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