FINAL REPORT
JPL CONTRACT NO. 950492

Integrated Electronic Gating System for Multiplexing Applications

IBM Components Division

FINAL REPORT
JPL CONTRACT NO. 950492

December 15, 1964

Integrated Electronic Gating System for Multiplexing Applications

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

Final report under contract to the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration, under Contract NAS 7-100.

Prepared by
International Business Machines Corporation
Components Division
East Fishkill Facility, Route 52
Hopewell Junction, N.Y. 12533

CONTENTS

ABSTRACT

19926

A Light Actuated Switch (LAS) has been developed for low level electronic commutating (multiplexing) and chopper applications. This device is ideally suited for such applications because of the extremely low offset voltage, low leakage currents, low switch ON impedance, complete electrical isolation, and moderately high speed switching characteristics.

The Light Actuated Switch consists of a GaAs p-n junction infrared source and an electrically isolated silicon photo detector. The silicon detector has the characteristics of a symmetrical, bilateral switch which changes into a low impedance state upon application of a forward bias (drive) current to the GaAs p-n junction light source, and remains in the conductive state until drive current is removed.

A general design theory, based on the Ebers & Moll low level transistor model, is given, with special emphasis on breakdown voltage, ON impedance, offset voltage, and switching speed. It is shown how the design considerations lead to a specific geometry for the detector. Results of extensive testing are reported.

Author

FOREWARD

This report is a final report on JPL Contract No. 950492. The work covered a period from April 17, 1963 to November 15, 1964.

The program, entitled, "Integrated Electronic Gating Systems For Multiplexing Applications," was for a best-of-efforts results. Although the study was a group effort, the program technical supervision was passed from Mr. R. M. Folsom to Dr. W. Pieczonka and subsequently to Dr. E. S. Wajda.

This report was prepared by the Components Division of International Business Machines Corp., Poughkeepsie, New York.

This report is unclassified.

SECTION 1 - PURPOSE OF PROGRAM

1.1 INTRODUCTION

In data acquisition systems, many inputs are sampled in a programmed manner by means of a multiplexor. The principle of multiplexing is not new, and before the introduction of the transistor in 1948, electro-mechanical devices, such as relays, performed this operation. Even the best of these devices were large, heavy, costly, and very slow compared to today's solid state switches. By the proper combination of solid-state active devices and passive components, electronic multiplexing systems used today represent a great improvement over the older electro-mechanical devices. However, further improvements would be highly desirable, especially a reduction in weight, size, and power consumption.

Low level signal switching, requires devices that possess the following properties:

1. High open and low closed impedance.
2. As low a contact potential as possible, to minimize error at low signal levels.
3. Good isolation between control element and device contact.
4. High switching speed.
5. Ability to handle signals of both polarities.
6. Ability to withstand high common-mode voltages.

The mechanical relay fulfills all of the above requirements but is limited in switching speed. Solid-state devices, in general, overcome the speed limitation but may have other undesireable features, such as:[1] polarity problem, where a single bi-polar device cannot accept both polarities;[2] offset voltage problem, where a non-zero contact potential exists; and[3] isolation problem, which, however, could be overcome through transformer coupling.

1.2 PROGRAM OBJECTIVES

The program had as its objective the development of a solid-state switch to be used in an electronic gating system for space-craft multiplexing applications. The switches had to be capable of being switched by some separate logic at rates from DC to 10,000 times a second, per switch, in any sequence. A light actuated switch, consisting of an electroluminescent diode source, and a photon detector formed the basis for this development program.

1.3 LIGHT ACTUATED SWITCH (LAS)

If two transistors are connected back to back, as shown in Figure 1, the effective resistance between the input and output terminals of the switch is the sum of the two ON resistances. The effective offset voltage between the input and output terminals is the

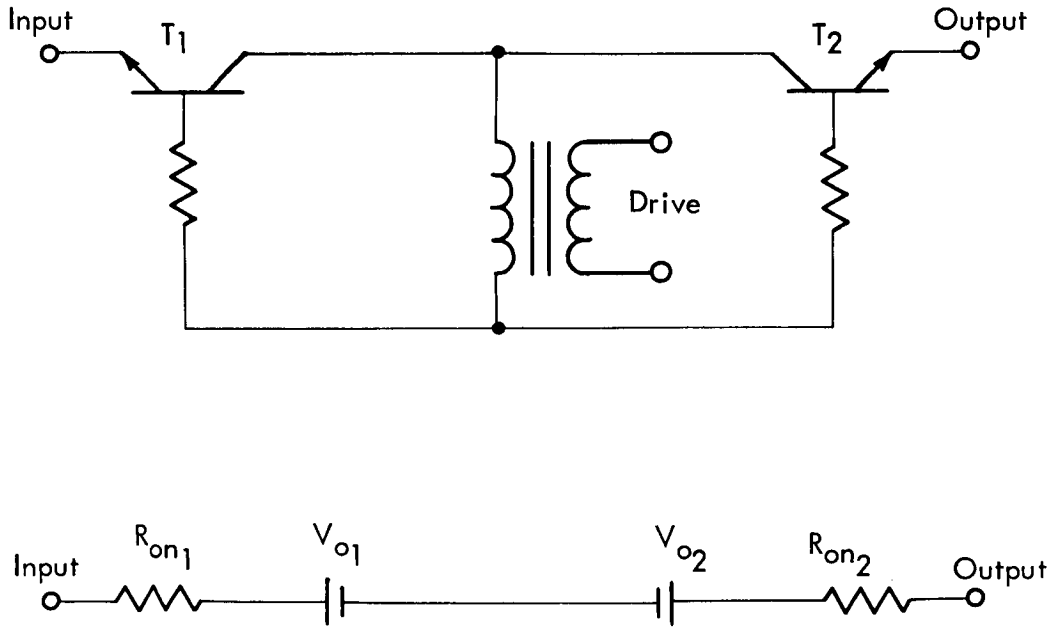


FIGURE 1 - MATCHED PAIR "CHOPPER/MULTIPLEX SWITCH" CIRCUIT
(R. L. Bright -- U.S. Patent #2,962,603 dated 29 November 1960)

difference between the offset voltages of the two transistors. A very small net offset voltage may be obtained by matching the two transistors and operating them in an inverted mode. This circuit, either in discrete form[1] or in integrated form[2], is capable of high-speed operation and nearly satisfies all the desirable features of the mechanical relay. The recent discovery[3] of electroluminescence in III-V compound semiconductor p-n junctions has made possible a switching device which improves upon its electrically driven counterpart. This improved device is basically identical to the electrically driven one, except that it is actuated by the light emitted from the p-n junction. The photon-actuated switch is more like the mechanical relay because it has perfect isolation between control element and device contact. It is this feature that is so important in the development of a solid-state multiplexor switch, requiring complete isolation from ground.

The light actuated switch (LAS), developed in this program, consists of a gallium-arsenide p-n junction, an infrared source and an electrically isolated silicon photo-detector. The silicon detector has the characteristics of a symmetrical, bilateral switch which changes into a low impedance state upon application of a forward bias (drive) current to the gallium arsenide electroluminescent diode, and remains in the conductive state until the drive current is removed.

1.4 SWITCH PERFORMANCE GOALS

The prime requirement of the switch design was reliability of operation. The Jet Propulsion Laboratories' specification, No. 31140, set the basic guide lines and objectives.

The DC equivalent circuit for the switch is shown in Figure 2,and the numeric values for the parameters are given in Table 1, along with other desired performance characteristics.

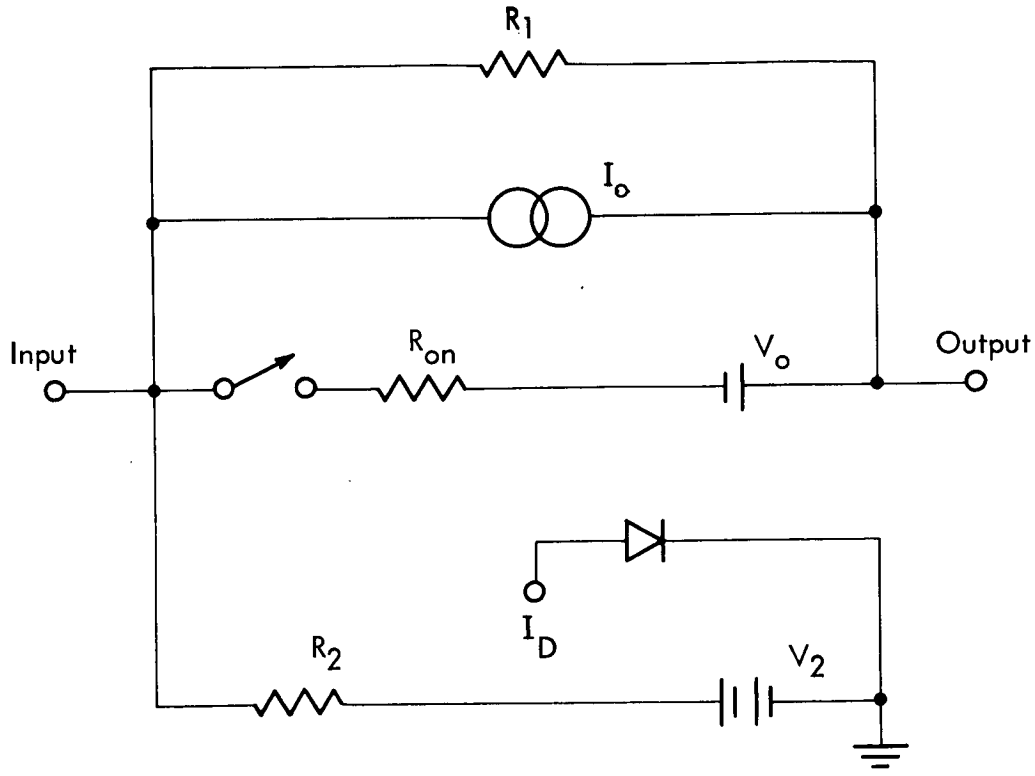


FIGURE 2 - DC EQUIVALENT CIRCUIT

The packaging objective was to achieve a 100-times improvement (reduction) in size over JPL's existing system. Where presently one switch occupies 0.3 cubic inch, the LAS packaged in a TO-18 header would occupy approximately .003 cubic inch. In consonance with the size reduction of the switch, the weight reduction objective was a 10-times improvement from the existing 6.8 grams to less than 0.5 grams.

TABLE 1

SWITCH DESIGN OBJECTIVES

R_1	-	Switch open dc impedance	≥ 100 megohms
R_{ee} or R_{on}	-	Switch closed dc impedance	≤ 20 ohms
R_2	-	Switch input to ground dc impedance	≥ 100 megohms
V_o	-	Switch closed contact potential	≤ ± 50 microvolts
I_o	-	Switch open leakage current	To meet all specs
R_s	-	Source impedance	20 ohms to 10 K ohms
R_L	-	Load impedance	10 K ohms to 1 M ohms
V_i	-	Input signal	± 5 volts
I_s	-	Switch closed current	≤ ± 500 μ amps
BV_{ee} or V_m	-	Voltage overload without switch damage, open or closed	≥ ± 35 volts
I_m	-	Current overload without switch damage, open or closed	≥ ± 10 millamperes
$(t_r + t_f)$	-	Switch rise and fall times	< 20 microseconds
P	-	Total power to close switch	50-100 milliwatts

(Resolution, Linearity, Cross-talk, Error Band, as indicated in JPL Specification No. 31140.)

SECTION 2 - GaAs DIODE DEVELOPMENT

2.1 DIODE REQUIREMENTS

To be an efficient control element for the LAS, the GaAs diode must have the following properties:

a. High external efficiency, which is defined here as the ratio of the light output to the diode input current.

b. Low forward voltage for a given current level to minimize input power.

2.2 ELECTROLUMINESCENCE IN GaAs

Radiative recombination is a process by which excess electrons and holes can recombine in semiconductors[4]. The rate of recombination of the minority carrier can be represented as the sum of two terms: (1) the recombination through impurity centers with the emission of either phonons or photons, and (2) band-to-band transitions with the emission of photons with energy equal to that of the semiconductor gap.

During the past few years, GaAs recombination processes (spontaneous as well as stimulated) have been studied, but the exact nature of the recombination mechanism responsible for GaAs electroluminescence is still uncertain.

Black et al[4] have found that the recombination radiation emitted from forward biased GaAs diodes was proportional to the diode current and that the band edge radiation, at 1.47 ev, is by far the dominant recombination process for injected carriers. Nathan and Burns[4] have compared fluorescence measurements on homogeneously-doped samples of GaAs with the emission from a forward-biased p-n diode and concluded that the recombination radiation involved an acceptor center.

Independent experiments reported by Gleener et al[4] show that the observed shift of emission energy with magnetic field can be approximately explained by a transition which proceeds through the ground states of donors.

Lucovsky and Repper[4] have studied the characteristics of the spontaneous radiation as a function of doping density. They concluded that for doping densities below 1.5×10^{17} cm^{-3} the recombination radiation is due to the electronic transitions between states in the conduction band and the Zn acceptor level. For doping densities in excess of 2×10^{18} cm^{-3}, the recombination radiation is generated by transitions, originating at the bottom of the donor impurity band and terminating at the bottom of the acceptor impurity band or at the edge of the valence band.

2.3 DESIGN CONSIDERATIONS

The GaAs diode design was based on the results of many experiments correlating light output of the GaAs electroluminescent diodes with process parameters and inherent material properties. These experiments are briefly described.

a. Effect of Diffusant Species

To determine the effect of doping impurity species on the light output, zinc and sulphur - doped diodes were compared.

Using n-type GaAs wafers, doped with Te to a carrier concentration of $7.7 \times 10^{16} \sim 2.6 \times 10^{17}$ cm^{-3} as starting material, diodes were made by diffusing Zn at a surface concentration between $5 \times 10^{19} \sim 2 \times 10^{20}$ cm^{-3}. Junction depths of 0.15 and 0.5 mils were obtained from 2 and 23 hour diffusions at 720°C, respectively.

Using p-type GaAs wafers, doped with Zn to a carrier concentration of 4×10^{17} cm^{-3} as starting material, diodes were made by diffusing sulphur at a surface con-

centration of $4x10^{18}cm^{-3}$. Junction depth of 0.25 mils was obtained from 120 hour diffusions at 1020°C.

An analysis of these diodes showed that the zinc-diffused units had a much higher external efficiency than the sulphur-diffused ones.

b. Starting Material

Diodes, made by diffusing Zn into n-type "undoped" GaAs wafers having a carrier concentration approximately $5x10^{17}$ cm^{-3}, had much higher light outputs at a given forward-bias than diodes made by diffusing Zn into n-type GaAs that was "doped with Te" to the same $5x10^{17}$ cm^{-3} carrier concentration.

c. Comparison Between Light Output from the p-Side and from the n-Side

Figure 3 shows that the light output obtained from the n-side of the diode is about twice that of the p-side, even though the n-side is three times thicker than the p-side.

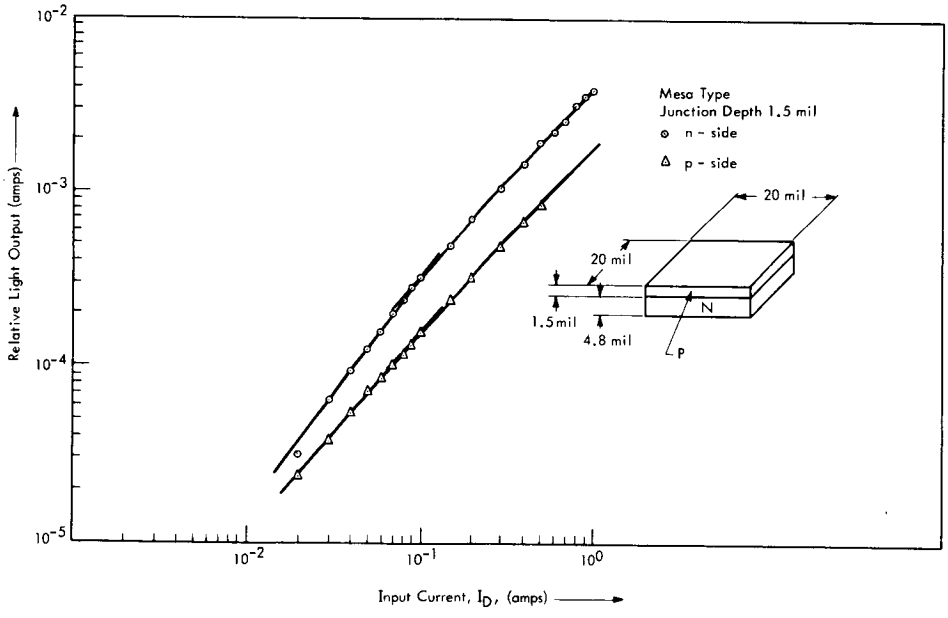


FIGURE 3 - LIGHT OUTPUT FROM MESA DIODE CONFIGURATION

It is believed that the decrease in output from the p-side is caused by higher absorption in the heavily doped p-layer. This result confirms the findings of several authors[5], namely that the absorption coefficient of p-type GaAs (with a doping level of $10^{19} \sim 10^{20}$ cm^{-3}) is much higher than that of n-type GaAs (with a doping level of $10^{16} \sim 10^{18}$ cm^{-3}) in the 1.0 - 1.5 ev photon energy range.

d. Mesa vs,planar diode configuration

Planar diodes were made by using SiO masking techniques. Arrays of 5 mil openings were obtained by evaporating SiO through a metal-wire mask. Diodes with the same junction depths as the mesa-type diodes were fabricated. Due to the nature of the planar configuration, the p-n junctions penetrate to the surface of the p-layer, and the additional light emitted from the junction edge adds to the normal light coming through the bulk p-layer. Thus, the total light output from the p-side is about the same as that from the opposite n-side. (See Figure 4.)

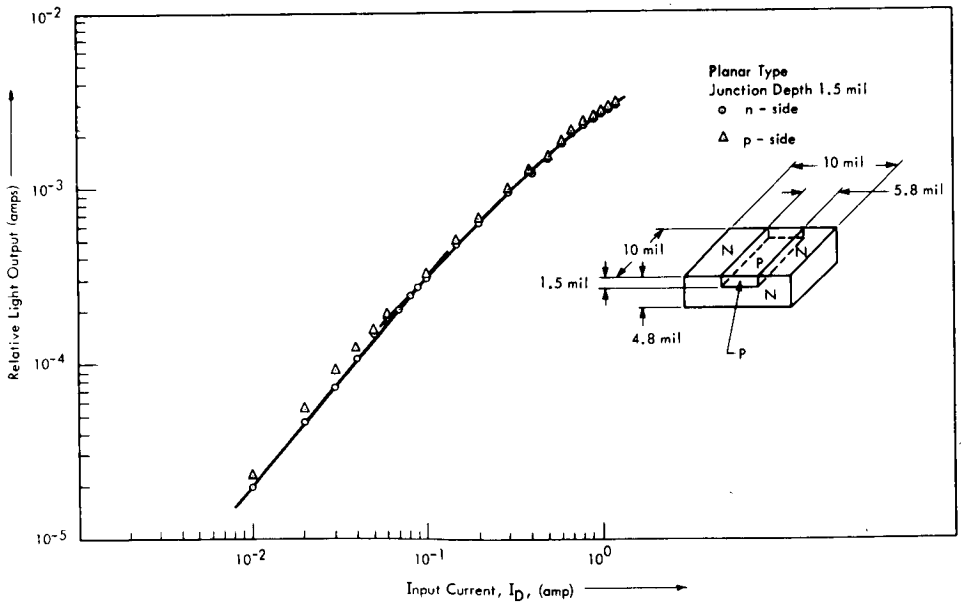


FIGURE 4 - LIGHT OUTPUT FROM PLANAR DIODE CONFIGURATION

Although the planar-type diode can be made as efficient as the mesa-type diode, severe process limitations exist in the SiO masking technique. Zinc can be partially masked by thick SiO layers at low diffusion temperatures. Above 750°C, effective masking is very difficult.

e. Size Dependence

Figure 5 shows the variation of light output with input current for three sizes of mesa-type diodes. As is expected, the light output varies with the current density. Thus, small size diodes are preferred, with proper heat dissipation.

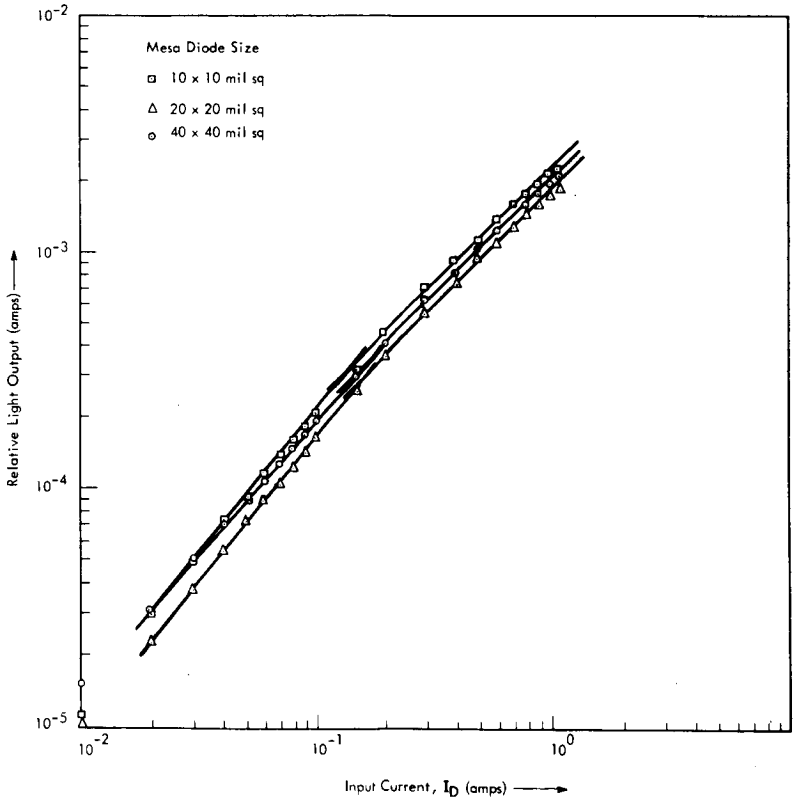


FIGURE 5 - EFFECT OF DIODE SIZE ON LIGHT OUTPUT

f. Optical Coatings

Because GaAs has a high index of refraction (n=3.6), the critical angle of reflection at the GaAs - air interface is about 16 degrees. Internal reflection losses can be reduced by a material whose index of refraction is between GaAs and air. An epoxy (Maraglas*) whose index of refraction is about 1.5 increased the relative light output by a factor of two, as shown in Figure 6. A higher temperature epoxy (220^{o}C), Randac*, with comparable optical properties was subsequently used.

*Trademark, Mitchell Rand Corp. Hillburn, New York

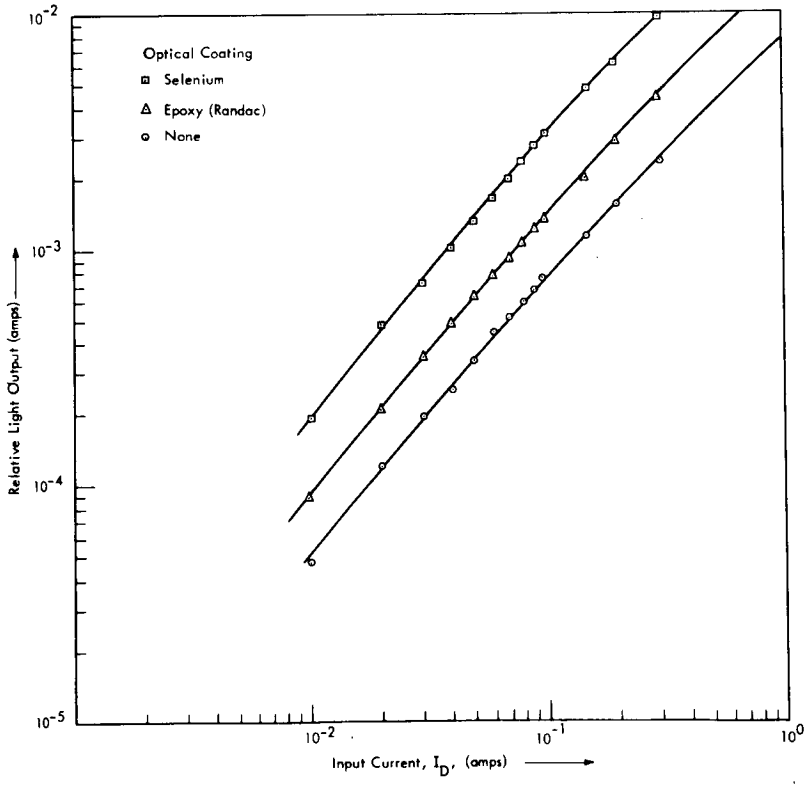


FIGURE 6 - EFFECT OF OPTICAL COATING ON RELATIVE LIGHT OUTPUT

g. Contact Resistance

For electroluminescence, the GaAs diodes must be forward-biased. A low forward-voltage is necessary to minimize the input power. Ohmic contacts, made to the p-type and n-type GaAs, should have minimum contact resistance.

Pure indium makes good ohmic contacts to p-type GaAs, and 98% In - 2% Te makes good ohmic contacts to n-type GaAs. The disadvantage of such ohmic ontacts manifests in low alloying temperature ($\leq 156^{o}C$). Evaporated mixtures of 98% Ag - 2% Te or 99% Ag - 1% As, alloyed at 575~600^{o}C, make good ohmic contacts to n-type GaAs, whereas evaporated mixtures of 98% Ag - 2% Zn, alloyed at 575~600^{o}C, make good ohmic contacts to p-type GaAs. For $I_D \sim 100$ ma, typical forward voltage drops are about 1.2 ~1.3 volts.

2.4 DIODE FABRICATION PROCESS

The following schedule summarizes the diode fabrication steps. Figure 7 shows schematically the diode assembly.

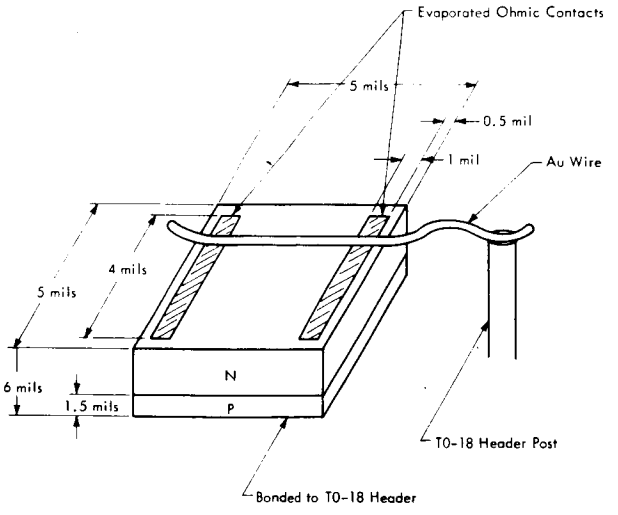


FIGURE 7 - SCHEMATIC OF DIODE ASSEMBLY

a. The starting material was n-type undoped GaAs with a resistivity of 0.005 ohm-cm.

b. Wafers were polished to a mirror finish with a final thickness of 8-9 mils.

c. Zinc was diffused in a capsule (18 cc) diffusion process at 850°C for 4 hours. The source was 1.5mg metallic zinc, and 0.4 mg/cc arsenic was added to suppress the dissociation of GaAs. A junction depth of 1.5 mils resulted with a surface concentration of 10^{20} cm^{-3}.

d. The n-side of the wafers was polished, and the overall wafer thickness was reduced to 6 mils.

e. Contacts were evaporated at a substrate temperature of 400°C (98% Ag - 2% Te for n-type and 98% Ag - 2% Zn for p-type).

f. The contacts were alloyed at 600°C for 2 minutes.

g. The wafers were cut into 5x5 mil squares.

h. Diodes were bonded to Au-Ga plated TO-18 headers with the p-side down.

i. One mil Au wires were thermocompression bonded (TCB) to the diode contacts.

j. The entire diode assembly was electrolytically cleaned in a KOH solution.

2.5 TEST PROCEDURE

The forward characteristics of each diode were checked with a Tektronix 505 curve tracer.

Diode light outputs were measured with the apparatus shown in Figure 8 under pulsed input conditions. A Hoffman 110C silicon solar cell was used for the light sensor, and the output was displayed on an oscilloscope. The light intensity was measured at a fixed distance between the solar cell and the GaAs diodes. The drive current consisted of 50μ-sec wide pulses at all current levels, with a repetition rate of 10^3 cps.

(A solar cell detecting efficiency of 62% at 0.9 microns[6] was assumed for all external efficiency calculations.)

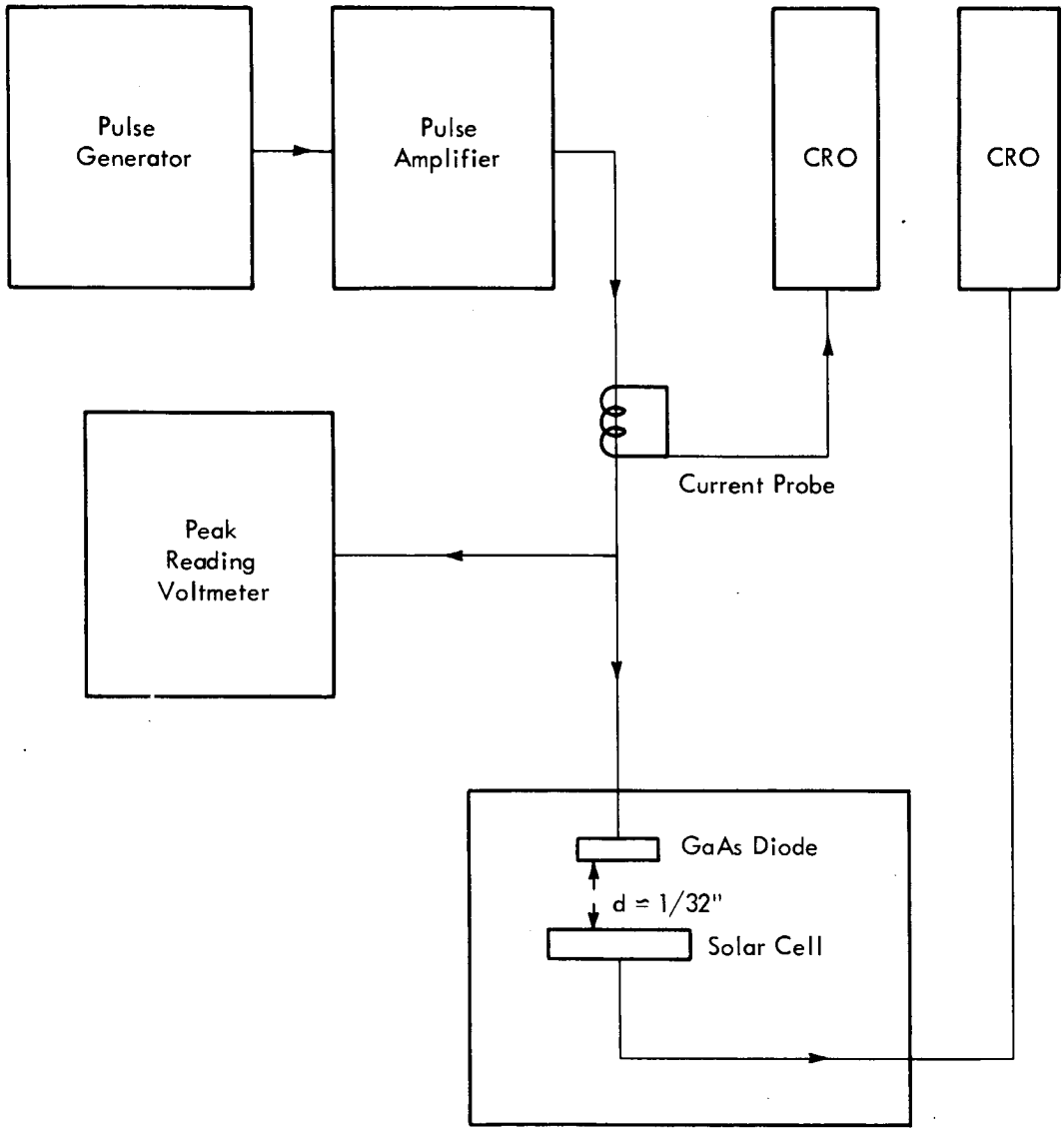


FIGURE 8 - APPARATUS FOR MEASURING LIGHT OUTPUTS FROM DIODE

2.6 TEST RESULTS

2.6.1 Current-Voltage Characteristics

Figure 9 shows a typical forward and reverse V-I characteristic. At I_D = 100 ma, the forward voltage drop is 1.3 volts. The reverse breakdown occurs at 11 to 12 volts and is rather sharp. A plot of the V-I characteristics at 300^{o}K over several decades of input current is also shown in the figure. Slope change from 2.1 to 1.6 was observed.

2.6.2 Relative Light Output

A theoretical analysis of the efficiency of a dome shaped vs. a flat GaAs diode is given in Appendix C. Figure 6 shows the variation of the relative light output with diode current for epoxy and selenium coated units and for uncoated units. At I_D of 100 ma. the relative light output increased by a factor of 1.8 and 4.2 through the use of epoxy and selenium coats, respectively. The nonlinearity at high input currents is probably due to excessive heating.

External efficiencies, ranging from 1.4% to 3.1%, were achieved through the use of such optical coatings on the diodes. The variation of external efficiency with temperature is shown in Figure 10.

2.6.3 Emitted Light Distribution

A photograph taken through an image converter showing the light emitted from the top surface of a diode at I_D of 100 ma is shown in Figure 11.

The light emitted from the edge of the junction at various input current levels

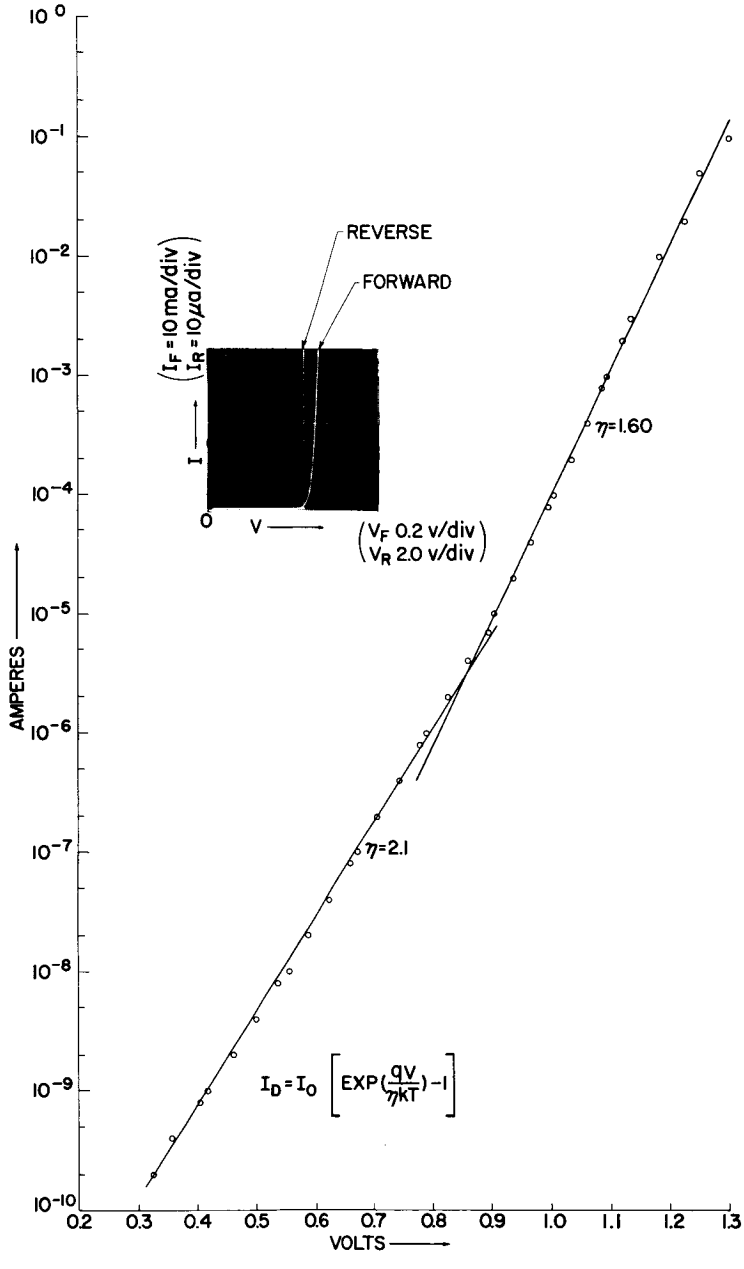


FIGURE 9 - DIODE CURRENT-VOLTAGE CHARACTERISTIC

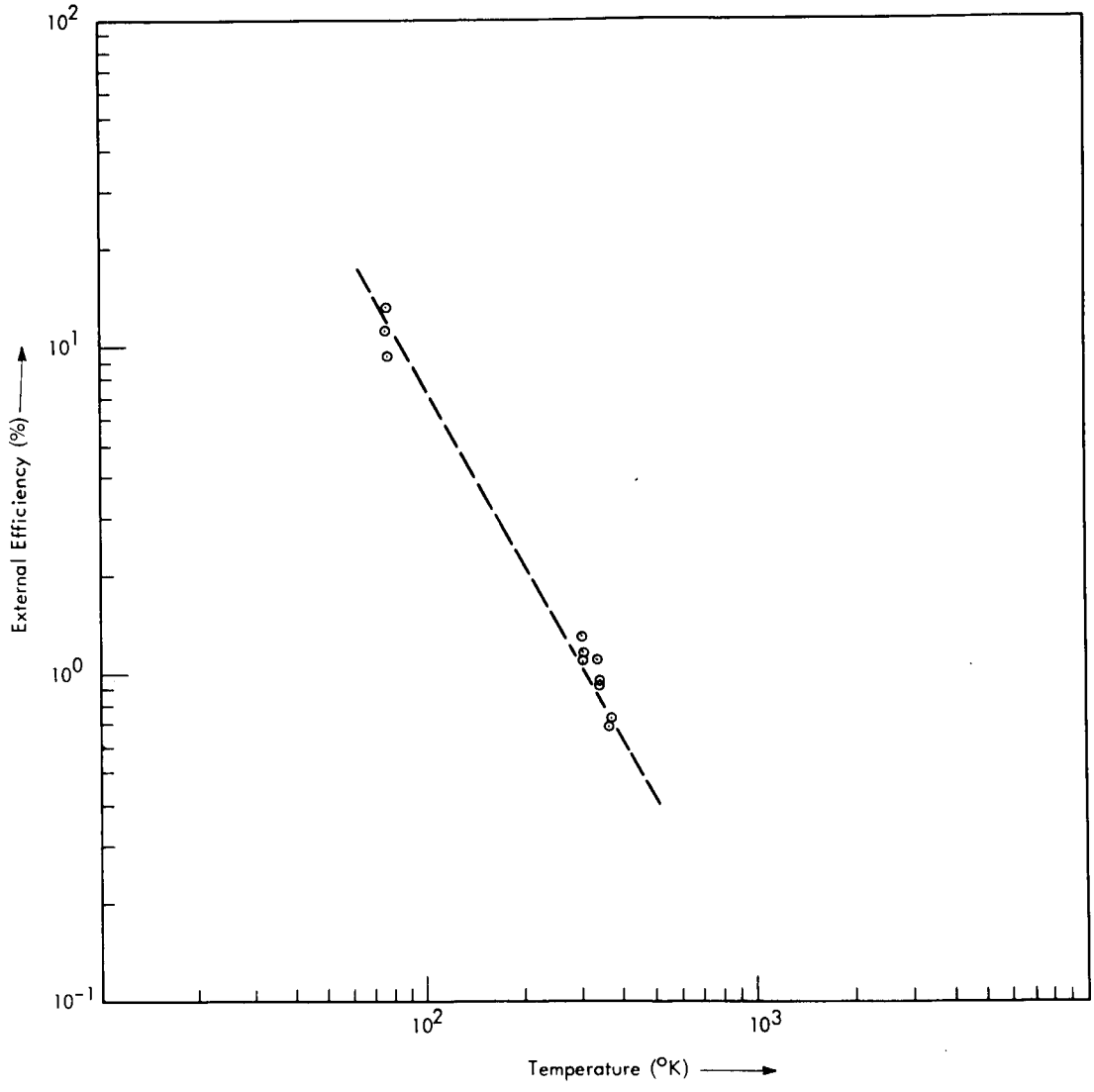


FIGURE 10 - EXTERNAL EFFICIENCY vs. TEMPERATURE

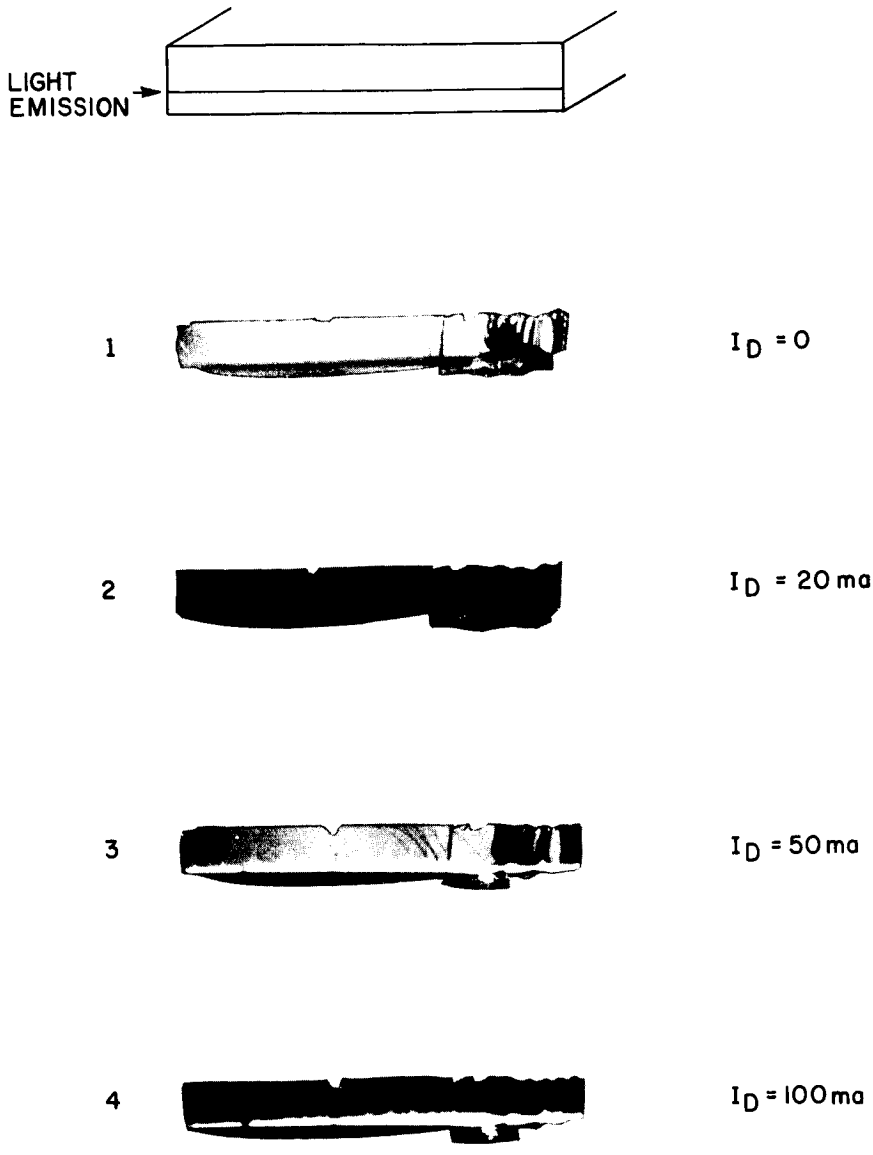
Diode Size 10 x 10 mils
I_D = 100 ma

FIGURE 11 - LIGHT PATTERN THROUGH IMAGE CONVERTOR

is shown in Figure 12. It appears that the light comes from the n-side of the junction which is contradictory to previous observation[7].

2.6.4 Rise and Fall Times of the Emitted Light

The response times of the emitted light were measured with the circuit shown in Figure 13a. A photomultiplier (Dumont K 2397) with a rise time of 10^{-8} seconds was used to sense the diode light output. Rise and fall times of the emitted light were less than 20 nano-seconds, as shown in Figure 13b, and are not the limiting factor in the integrated switch response.



MAGNIFICATION 72X

FIGURE 12 - LIGHT EMISSION FROM A DIODE EDGE

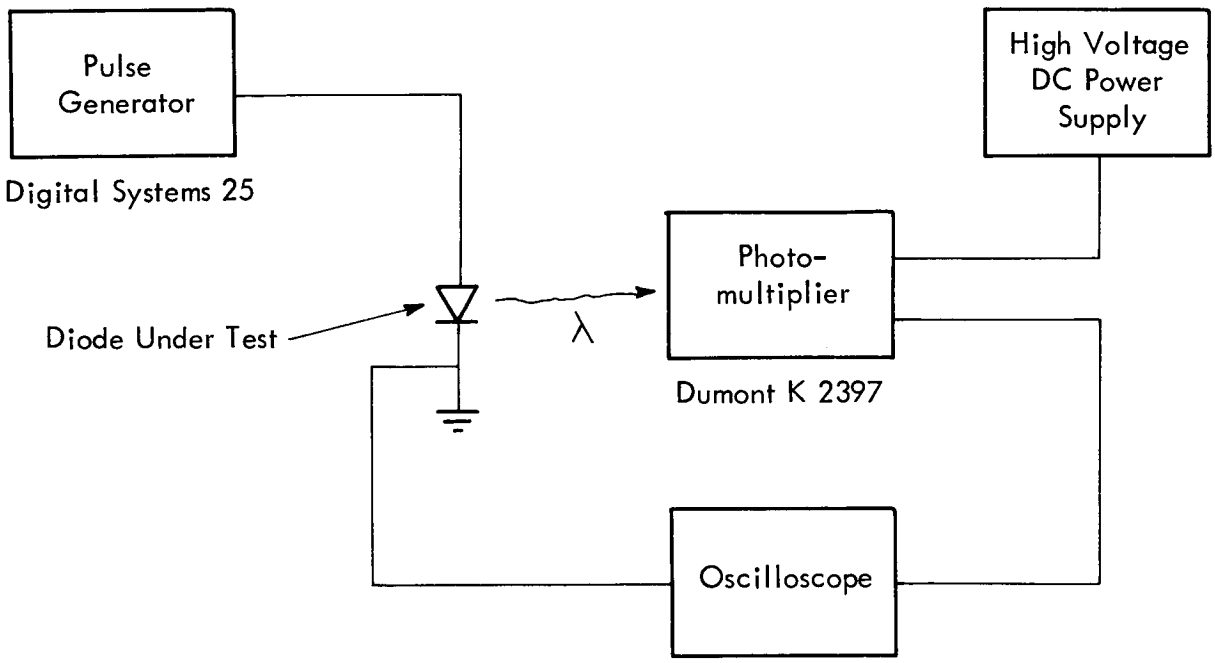


FIGURE 13a RESPONSE TIME CIRCUIT

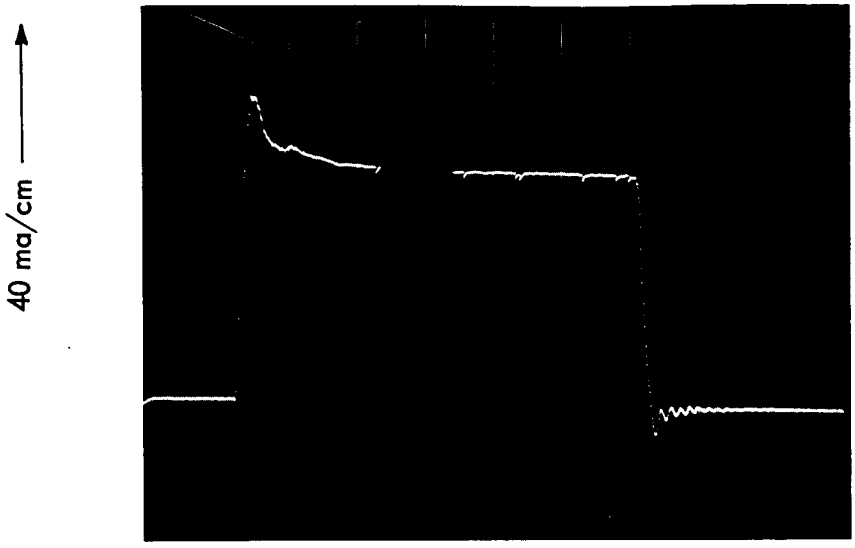


FIGURE 13b RESPONSE TIME MEASUREMENT

structure. Diffusion and drift mechanisms cause an accumulation of majority carriers (holes) in the base region thereby making it positive and causing J_2 to inject. When these injected carriers reach J_3, it saturates and becomes forward biased and injects throughout. That portion of the carriers (electrons) injected by J_3 within a diffusion length of J_1 is collected by J_1 and constitutes the current flowing through the switch. It is clear that for efficient operation and light sensitivity, all junctions should be good emitters.

3.2 DET REQUIREMENTS

For the DET to function as an efficient switch, the two transistors must have the following properties:

a. High gain and frequency response. This necessitates a narrow base width. The high gain is required so that the transistor is driven as deeply as possible into saturation.

b. Junction J_3 (collector) must be an efficient photo junction to provide as much base drive as possible. To accomplish this, most of the incident light must be absorbed near J_3.

c. The impedance between the two emitters and the effective offset voltage should be as small as possible during the ON period of the switch.

d. High emitter junction breakdown voltages are necessary in common mode operation where large overload voltages can be encountered.

e. For fast data transmittal through the switch, short rise and fall times are needed.

3.3 DET DESIGN CONSIDERATIONS

The DET in Figure 15 is turned on by an effective base current generated through the absorption of photons in the bulk of the device. This consideration dictates a certain

SECTION 3 - DOUBLE EMITTER TRANSISTOR (DET)

3.1 DET MODE OF OPERATION

The DET is a double-emitter transistor which combines the advantages of (a) using a matched pair of transistors in a Bright circuit[1] configuration to achieve low offset voltages, (b) integrating the two matched transistors to minimize thermal potentials in the signal path, and (c) using optical excitation instead of electrical drive for complete input-output isolation.

The phenomenological operation of the optically driven switch can be inferred from Figure 14, which is drawn for an NPN DET and for a particular polarity. For the opposite polarity, the junctions reverse their roles.

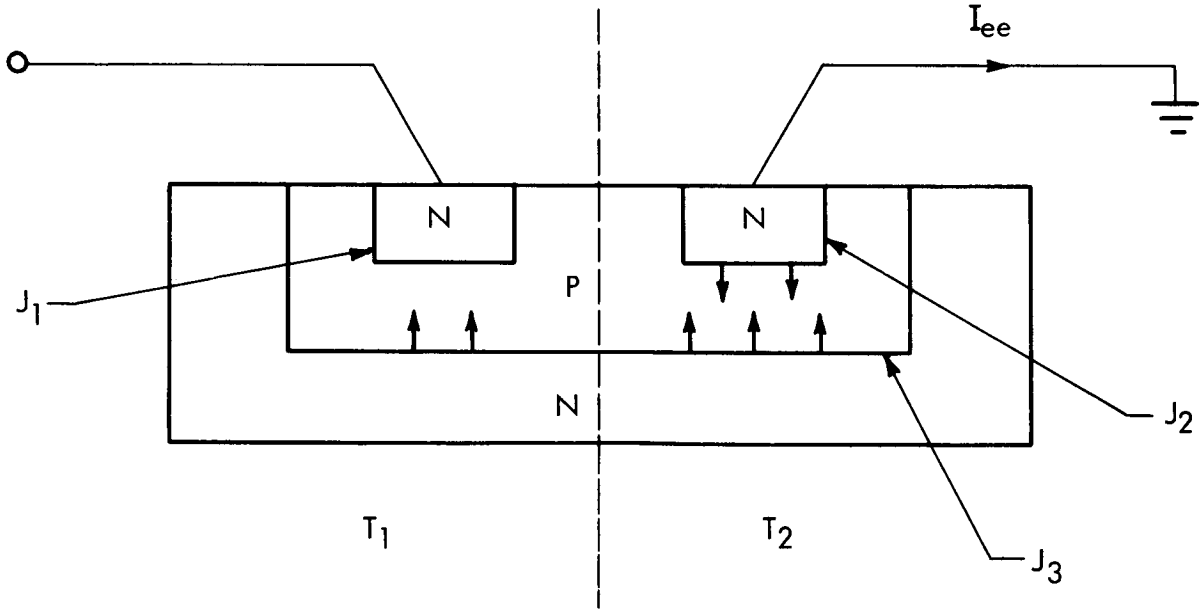


FIGURE 14 - DET MODE OF OPERATION

In the dark condition, J_1 is reverse biased, while J_2 and J_3 are nearly neutral (slightly forward biased). In the light condition, electron hole pairs are created throughout the

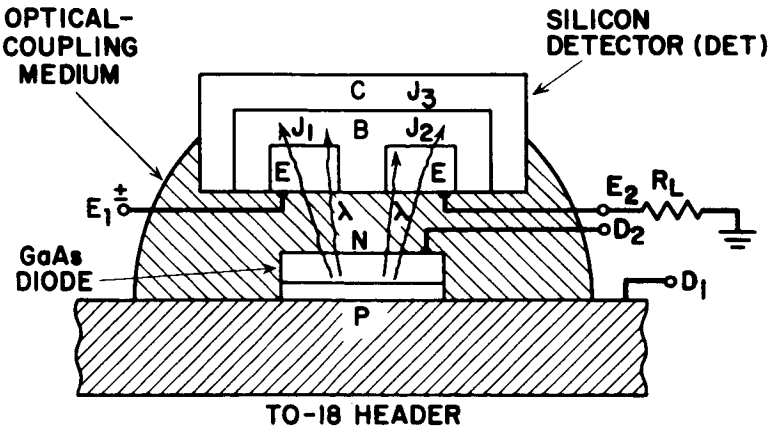


FIGURE 15 - LAS SCHEMATIC

geometry for the device. For J_1 (or J_2) to be an effective emitter, it should be as large in area as possible. The best that can be done is that the area of J_1 (or J_2) equals one-half of the area of J_3. The surface area of the emitters must also be left unmetallized to allow light to penetrate.

The DET breakdown voltage, BV_{ee}, is given by equation (B-18) of Appendix B.

$$BV_{ee} \simeq BV_{eb}\left(\frac{1}{\beta_i}\right)^{1/n} \qquad \text{(B-18)}$$

BV_{eb} is the avalanche breakdown voltage of the emitter junction and is an inverse function of the impurity doping level, N_b, of the base region as shown in Figure 16. To raise BV_{ee}, the base doping must be chosen as low as possible.

During the course of planar processing, the lightly doped base tends to invert (NPN) or accumulate (PNP). The former induces a conductance channel between the emitters with soft, lower breakdowns, whereas the latter lowers breakdown by lowering effective resistivity. Coupled with this there is usually a degradation in low level β values. Thus, placing a lower limit on N_b of about 10^{16} cm^{-3} will give an emitter-base breakdown of approximately 70 volts.

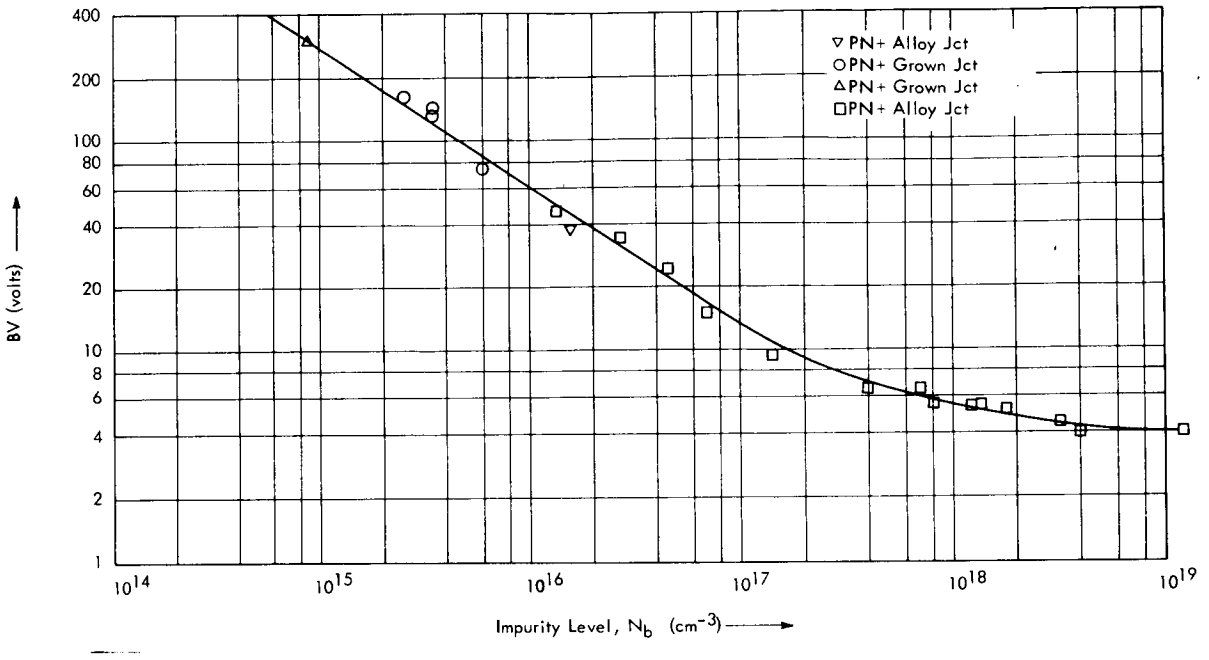


FIGURE 16 - BREAKDOWN VOLTAGE vs. IMPURITY LEVEL
(S. L. Miller, Phys. Rev., 105, 1246 (1957)

The breakdown voltage BV_{ee} is also inversely dependent on the inverse gain, β_i, but as will be shown later, high β_i values are desireable for low switch ON impedance and low offset potentials.

The ON impedance, R_{ee}, between emitters in the light condition must be kept low. On the basis of Ebers and Moll's small-signal analysis (Appendix B), the ON impedance is approximated by:

$$R_{ee} \simeq \frac{2nS}{I_b} \left(\frac{1}{\beta_i}\right) + R_i \qquad \text{(B-14)}$$

where β_i is the inverse common-emitter current transfer ratio, I_b is the effective base current and R_i is the intrinsic resistance. The base current (I_b) will depend on the useful area of the detector, viz., on the area through which photons enter the devices. Thus, I_b can be expressed in terms of the detector area, which is approximately equal to the collector area, A_c.

$$I_b = K_1 A_c$$

The constant, K_1, includes the efficiency of electron-hole pair creation.

Since n and s in equation (B-14) are constants, the ON impedance becomes:

$$R_{ee} \simeq \frac{K_2}{A_c \beta_i}$$

To lower the value of R_{ee}, one must increase β_i or increase the area, A_c. The latter choice is undesirable from the point of view of speed and packaging. Hence, the increasing of β_i remains as the prime factor in lowering R_{ee}. In terms of physical constants, β_i can be written as:

$$\beta_i = \frac{A_e}{A_c} \frac{D_{nb}}{D_{pc}} \frac{N_d}{N_a} \frac{L_{pc}}{W_b} \simeq K_3 \frac{A_e}{A_c}$$

where: A_e and A_c are the emitter and collector areas, respectively

D_{nb} = the electron diffusion constant in the base
D_{pc} = the hole diffusion constant in the collector
N_d = donor concentration in collector
N_a = acceptor concentration in base region
L_{pc} = diffusion length of holes in collector
W_b = base width

This makes R_{ee} inversely dependent on the emitter area.

$$R_{ee} \simeq K_4\left(\frac{1}{A_e}\right)$$

A circular geometry with closely spaced, "D" shaped emitters was chosen in the DET design.

For switching applications, one of the greatest advantages of the double-emitter transistor is its low offset voltage. Defining this as V_0 (the voltage between emitters when no current is flowing), we have from equation (B-10),

$$V_0 = nS \ln\left[\frac{(1 + \beta_{n1})\ \beta_{n2}}{\beta_{n1}\ (1 + \beta_{n2})}\right]$$

If $\beta_{n1} = \beta_{n2}$, V_0 automatically becomes zero for any value of n and any value of temperature. A difference between β_{n1} and β_{n2} will not greatly influence V_0 unless the forward β's are small. A measure of how closely the two β_n's have to be matched is $\frac{\Delta\beta n}{(\beta n)^2}$, as shown:

If $\beta_{n1} = \beta_n + \Delta\beta_n$, and $\beta_{n2} = \beta_n$, then the argument of the natural logarithm of Eq. (B-10) is

$$\frac{1 + \left(\frac{\Delta\beta_n}{\beta_n}\right) + \left(\frac{1}{\beta_n}\right)}{1 + \left(\frac{\Delta\beta_n}{\beta_n}\right) + \left(\frac{1}{\beta_n}\right) + \left[\frac{\Delta\beta_n}{(\beta_n)^2}\right]}$$

3.4 HISTORY OF DET DEVELOPMENT

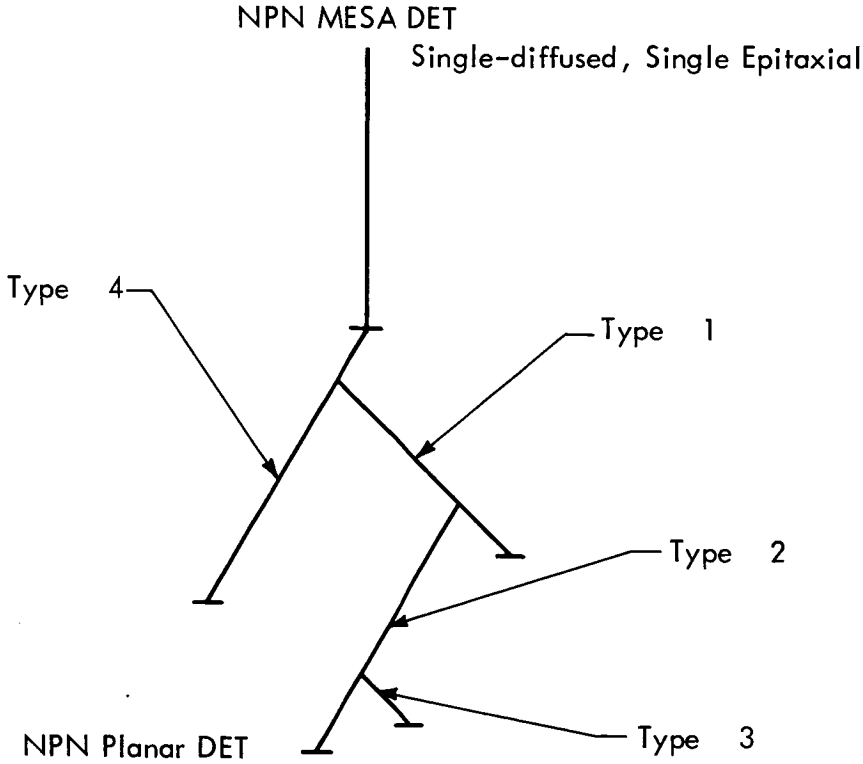
The geneology of the development of the photon detector is shown in Figure 17a. Several approaches were attempted that can be classified in the following manner (Figure 17b):

TYPE 1: Double-diffused, planar, NPN DET

TYPE 2: Single-diffused, single epitaxial, planar, NPN DET

TYPE 3: Single-diffused, double epitaxial, planar, NPN DET

TYPE 4: Single-diffused, single epitaxial, planar, PNP DET



Type 1: NPN Planar DET
Double-diffused

Type 2: NPN Planar DET
Single-diffused, Single Epitaxial

Type 3: NPN Planar DET
Single-diffused, Double Epitaxial

Type 4: PNP Planar DET
Single-diffused, Single Epitaxial

FIGURE 17a - GENEOLOGY OF PHOTON DETECTOR DEVELOPMENT

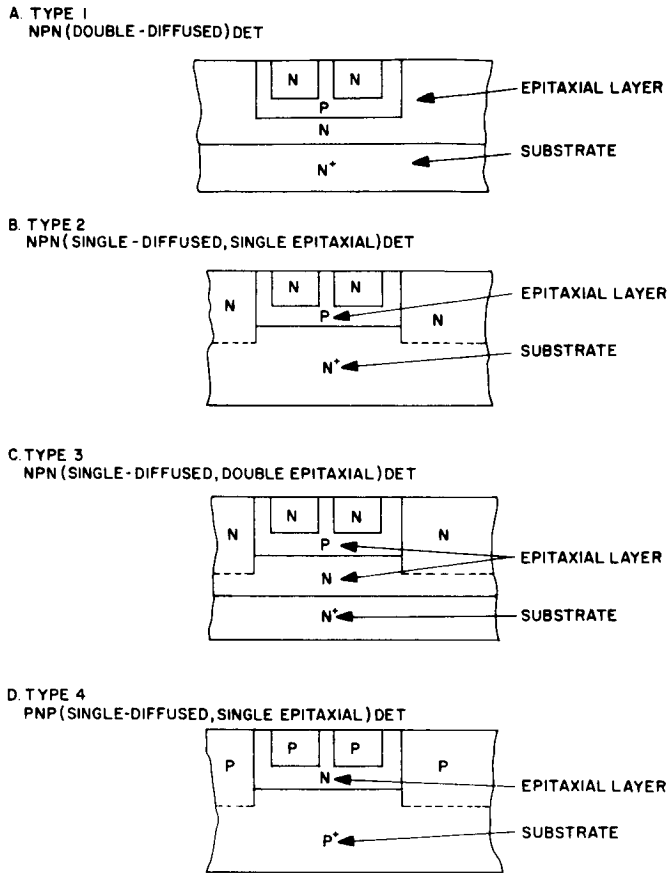


FIGURE 17b - DET APPROACHES

The evolution of the final geometry is shown in Figure 18, where several of the different geometries attempted are displayed.

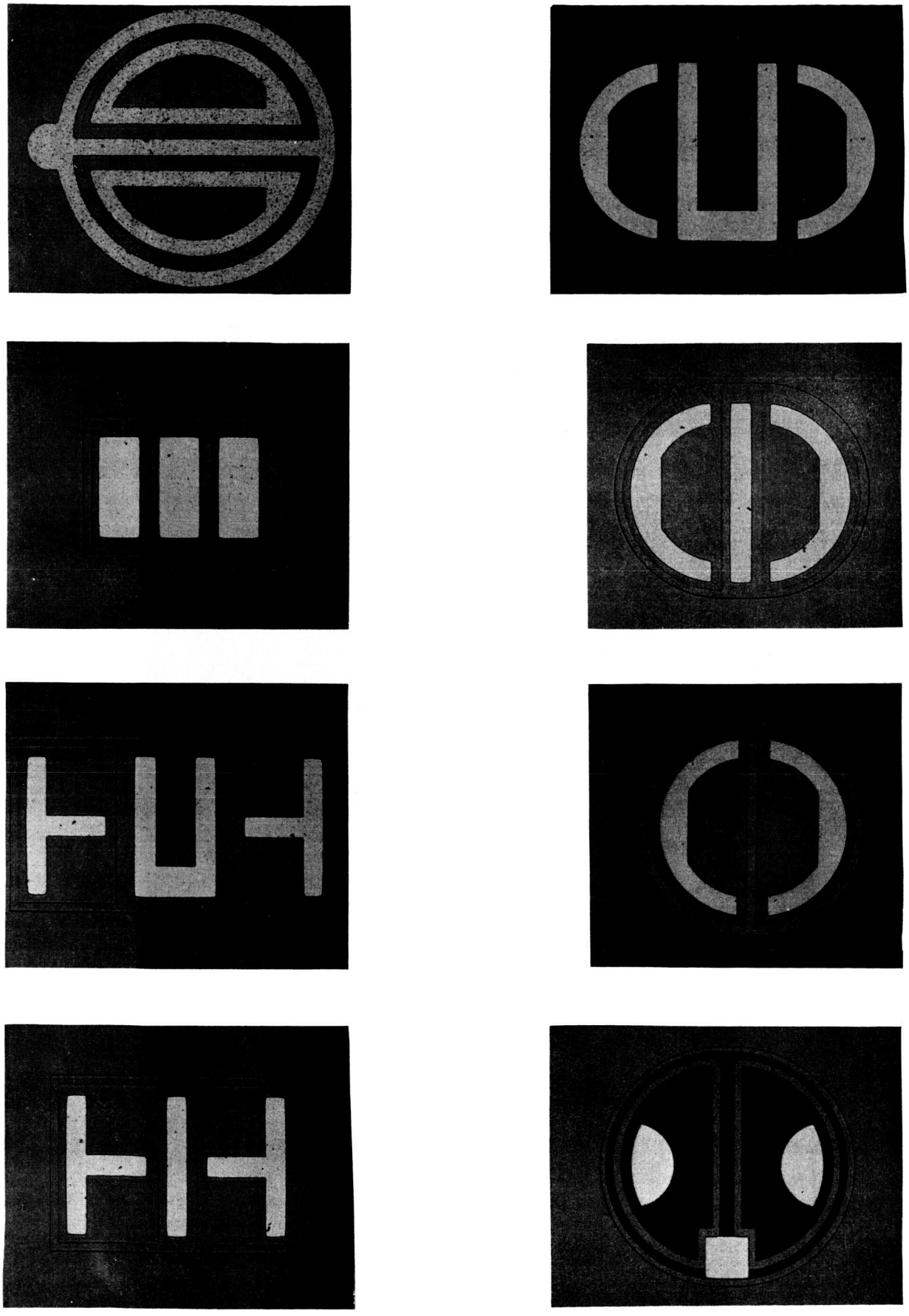


FIGURE 18 - EVOLUTION OF DET GEOMETRY

The development started with a single-diffused NPN mesa configuration. The problems encountered were

a) Low BV_{ee} values -

Measured values were lower than expected from doping.

b) Low β_i values -

The values ranged from 0.2-2.0 and were non-uniform over the wafer.

c) High ON impedance -

This is a consequence of the low β_i and also indicates a lack of sensitivity.

The possible causes were:

a) Inversion on low-doped base surfaces. As shown in Figure 19, the N^+ inversion channels short the N doped emitters, increase leakage and degrade the BV_{ee} values.

b) Epitaxial material

The low BV_{ee} values might be attributed to an impurity gradient in the epitaxial layer.

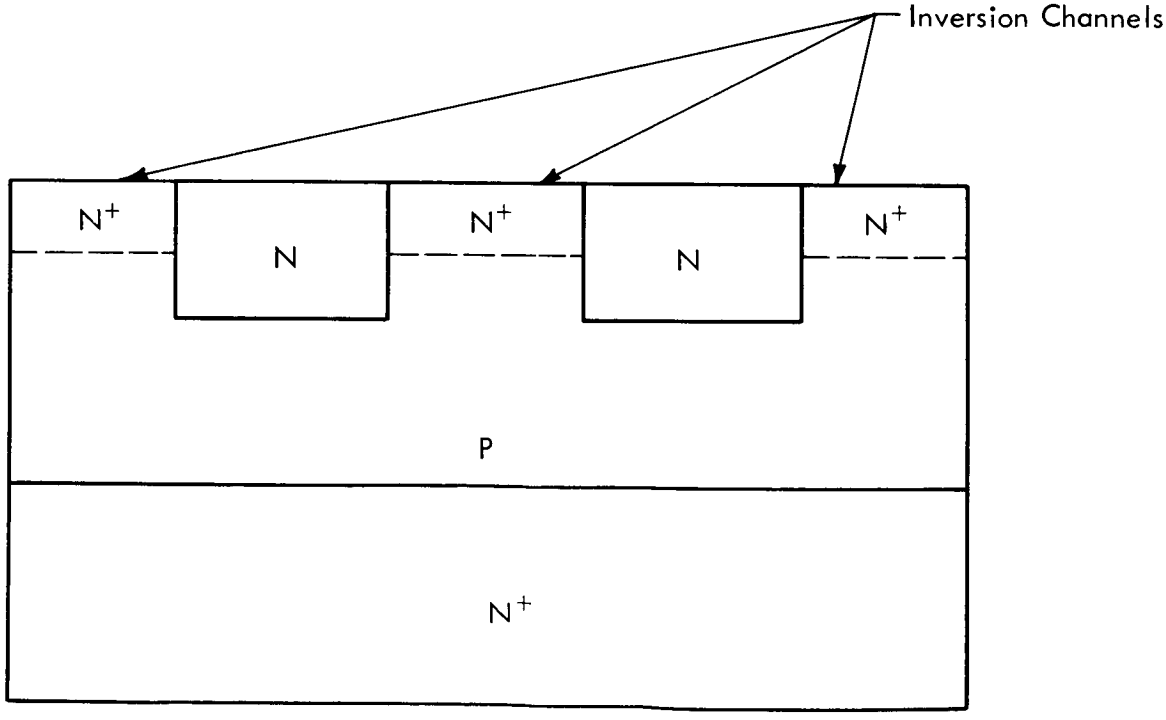


FIGURE 19 - INVERSION CHANNELS

Attempted solution to these problems took the form of:

a) P^+ channel inhibiting diffusion

This was done to break up the inversion channels by introducing heavily doped P^+ regions in the spaces between the emitters.

b) Retrograde epitaxial layer

The concentration of these layers was such that the neighborhood of the P on N^+ junction was more heavily doped than the surface.

The retrograde epitaxial approach did not succeed. The use of the channel inhibiting diffusion improved the breakdowns, which appeared to be sharper, and slightly increased the β_i values, which, in turn, caused some decrease in R_{ee}.

The possibility of an overall P^+ skin prior to initial oxidation of the grown surface was investigated, but though improvement was apparent, the method had practical limitations.

Since inversion appeared to be a serious problem affecting BV_{ee} and β_i, a new line of approach was necessary. In a PNP transistor, there is no inversion. Instead, accumulation occurs. This, in general, is not as serious a problem as inversion. Provided the PNP units possess comparable β_i values, they could be used instead of the NPN units.

TYPE 4

The problems encountered in the PNP units were:

a) Uniform, but low β_i.

Even though the devices had good sharp BV_{ee}'s, their β_i values were still low. They seemed to be the same over the entire wafer in the neighborhood of two.

b) High ON impedance.

From calculations, the R_{ee} values based on the measured β_i were lower than the measured ON impedance values.

c) High forward breakdowns.

Another factor contributing to a high ON impedance was the high forward breakdowns. This could be traced to the contact metallurgy of the devices.

Two solutions were attempted:

a) Ambient heat treatment

Devices were treated in forming gas for 2 minutes at 500°C.

b) Contact metallurgy

Several materials were tried: Al, Pd, Pt, Pd-Al.

The ambient treatment proved successful in raising β's, especially β_i's. This improvement was repeatedly observed with no degradation during further processing of the devices. The ON impedance values also decreased.

Of the several contact materials used, the Pd-Al combination gave the best results. The forwards improved, but they were still high, thus contributing to the high R_{ee} values. To determine whether a tradeoff existed between gaining in β and R_{ee} at the expense of lower BV_{ee} values, double-diffused planar NPN units were fabricated.

TYPE 1

The major problem with this type of DET was the low BV_{ee} value. There exists an inherent limitation in the double-diffused device which puts an upper limit on the practically attainable BV_{ee} value ($\sim$15 volts).

Using PH_3 instead of P_2O_5 diffusion techniques, surface imperfections and degradation due to high phosphorus surface concentration were minimized. This permitted fabrication of sensitive, high gain, low R_{ee}, and low BV_{ee} units. The success of the PH_3 diffusion revived the efforts on the single-diffused NPN DET, but now a planar configuration was attempted.

TYPE 2 & 3

The problem areas during this investigation centered on:

a) Starting material

The quality of the starting material varied considerably. Variation of initial processing seemed to affect the qualities of the finished device.

b) Contact metallurgy

Aluminum in contact with SiO_2 increased the leakage problems. Other metals, like Pt, were difficult to evaporate economically. Pd was hard to TCB.

Attempted solutions:

a) Several experiments were conducted to determine whether chemically polished or mechanically polished wafers were better and whether in-situ deposited silicon oxide was better than thermally grown oxide.

b) To improve the uniformity of the grown junction, in addition to single epitaxial wafers, double epitaxial wafers were grown.

c) Pd (about 600 Å) with Al (about 1000 Å) on top was tried for contacts.

The results of these experiments showed that:

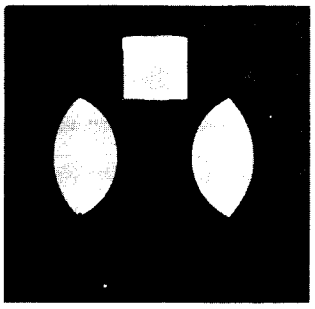
a) Chemically polished wafers proved to be superior.

b) Grown silicon oxide decreased leakage currents.

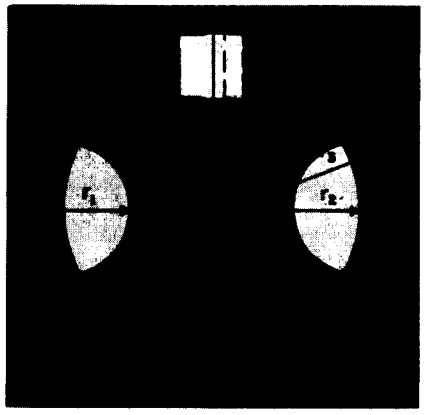
c) Double epitaxial wafers did not show marked improvement in uniformity.

d) The combination of Pd and Al yielded good contacts.

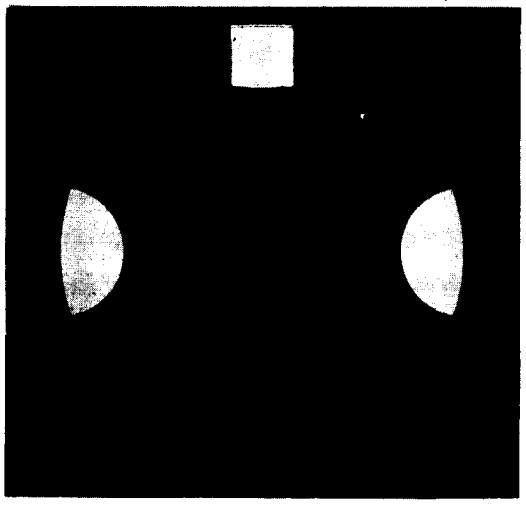
Of the different approaches, Type 2 & Type 3 turned out to have characteristics that were closest to the design objectives. The final choice is a Type 2 or a Type 3 device with the geometry shown in Figure 20.



	(mils)	
r_1	2.75	COLLECTOR AREA
r_2	3.75	~125 sq. mils
r_3	4.50	
r_4	5.00	EMITTER AREA
r_5	5.50	~56 sq. mils
r_6	6.00	



r_1	3.00	COLLECTOR AREA
r_2	6.25	~243 sq. mils
r_3	7.00	
r_4	7.50	EMITTER AREA
r_5	8.00	~145 sq. mils
r_6	8.50	



r_1	3.00	COLLECTOR AREA
r_2	8.75	~402 sq. mils
r_3	9.50	
r_4	10.00	EMITTER AREA
r_5	10.25	~270 sq. mils
r_6	11.00	

FIGURE 20 - FINAL VERSION OF DET (TYPE 2)

3.5 COMPARISON OF DET THEORY AND EXPERIMENT

In analyzing a detector made up of discrete devices (two transistors), it is relatively easy to determine the normal and inverse β values and the two base currents involved; but it is quite difficult to do so in the case of the integrated DET. In the latter case, only the total base current can be measured. For the DET (a symmetrical device), one must assume that I_b (in equations B-7 through B-14) is one-half the total base current. The values of β_i in these expressions cannot be measured separately for the two halves of the device. The value that should be used in the calculation is the one obtained when the two emitters are connected in common, with I_b as the total base current. The forward beta, β_n, can be measured separately for the two halves at one-half the total base current.

DET units of Types 1, 2 and 4 have been fabricated with base lead attachments in order that a comparison could be made between theory (Appendix B) and experiment. Figures 21 a - 21 c are plots of β vs I_b for such DET units. The Type 1 device has the highest β values whereas the Type 4 units, the lowest. Figure 22 shows the variation of the ON impedance, R_{ee}, as a function of the total base current. The solid curves were calculated from Eq. (B-12) using measured β values. A value of 1.5 was used for n, and values of 2 and 5 were used for R_i, respectively, for the Type 1 and Type 2 DET's. For the Type 4 DET, a value of 1.5 was used for n, and a value of 50 for R_i. The good agreement between theory and measurement over four decades of base current indicates that the Ebers and Moll model used in this study is very useful in first-order calculations.

The reason for the high R_i value for the Type 4 DET is not completely understood, though part of it could be due to the high absorption coefficient in the P region, the high forward breakdown voltage (therefore, high contact resistance), and the apparent series bulk resistance.

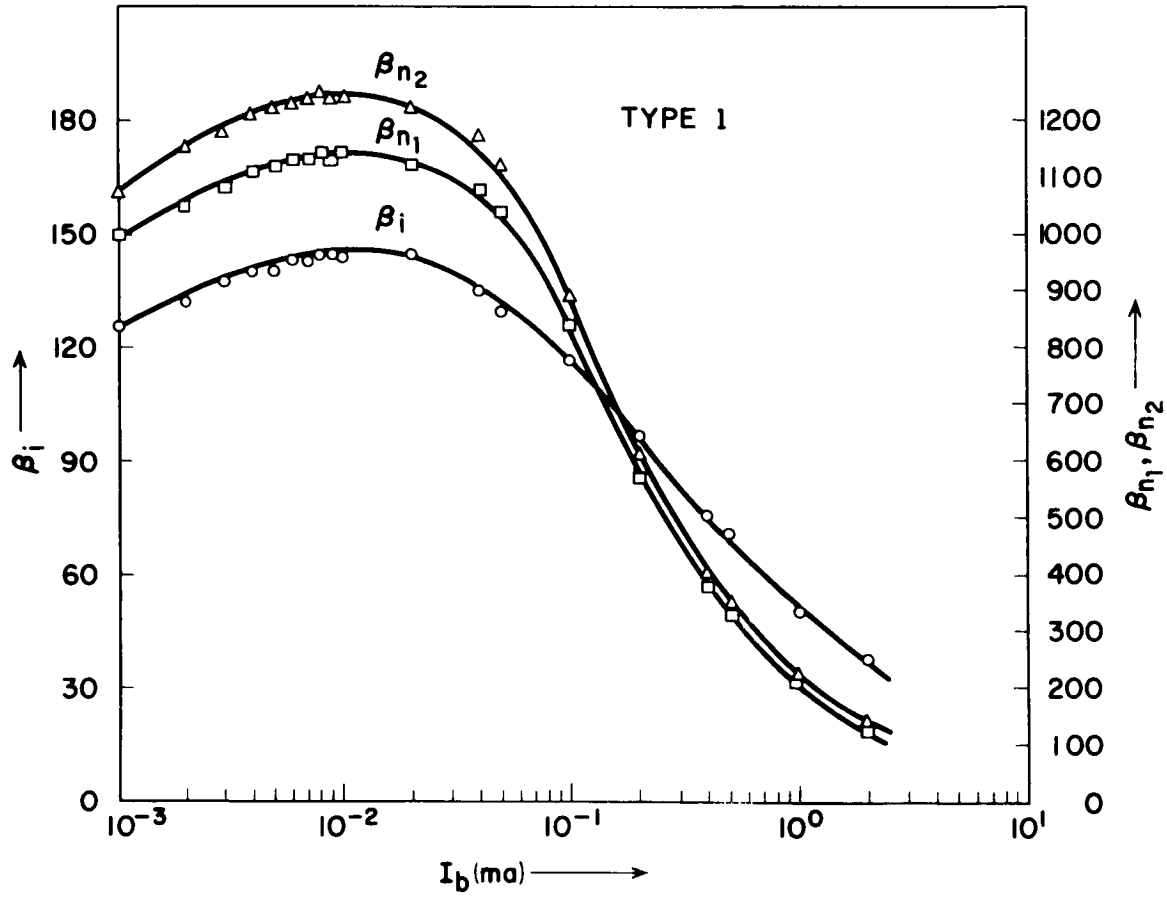


FIGURE 21 a - β vs. I_b (TYPE 1)

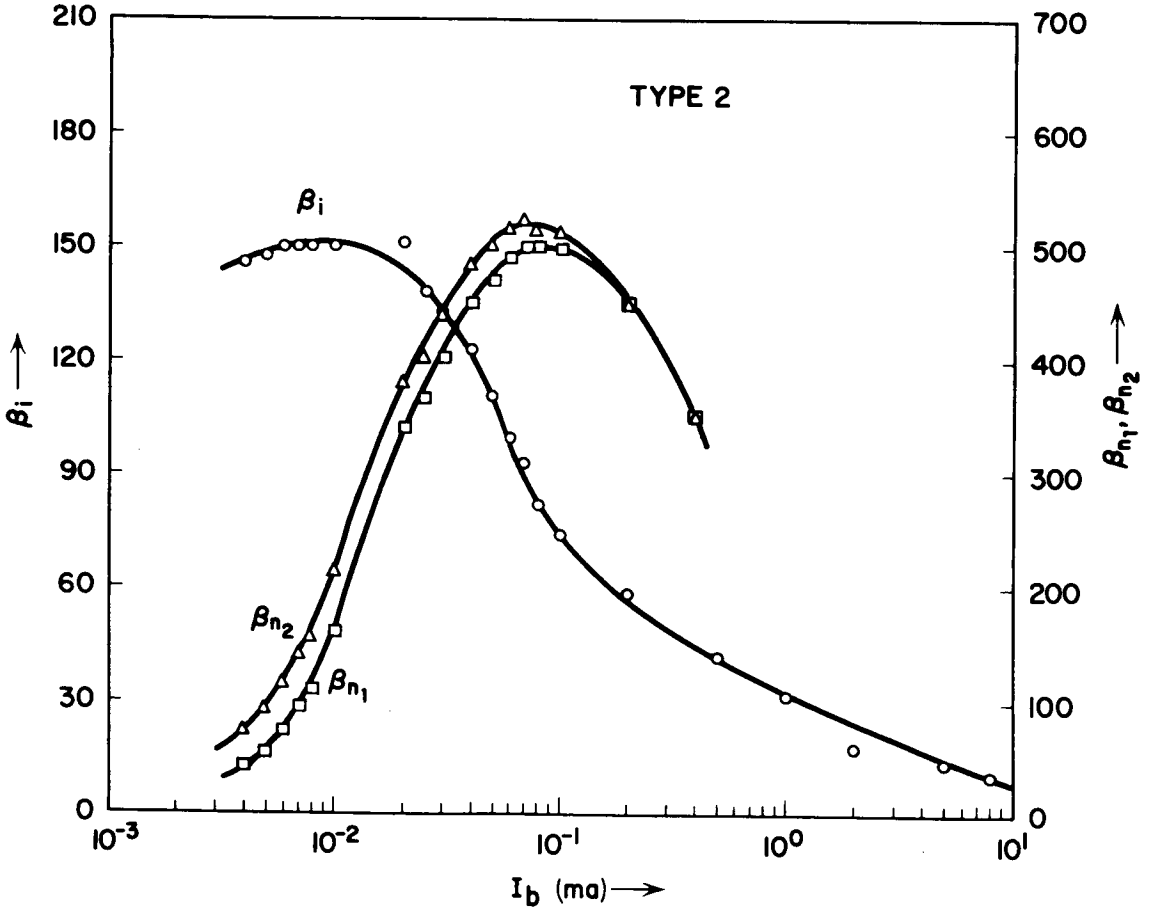


FIGURE 21 b - β vs. I_b (TYPE 2)

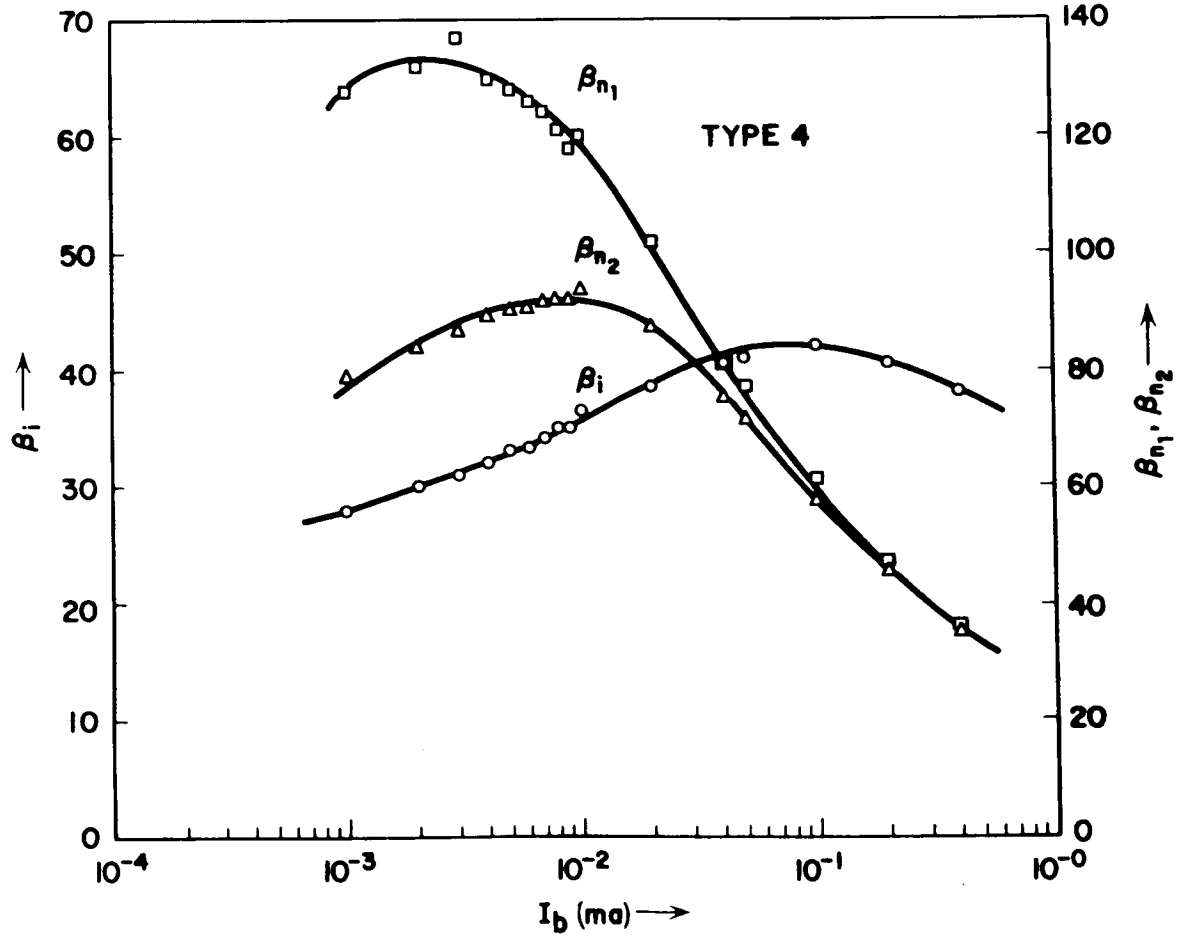


FIGURE 21 c - β vs. I_b (TYPE 3)

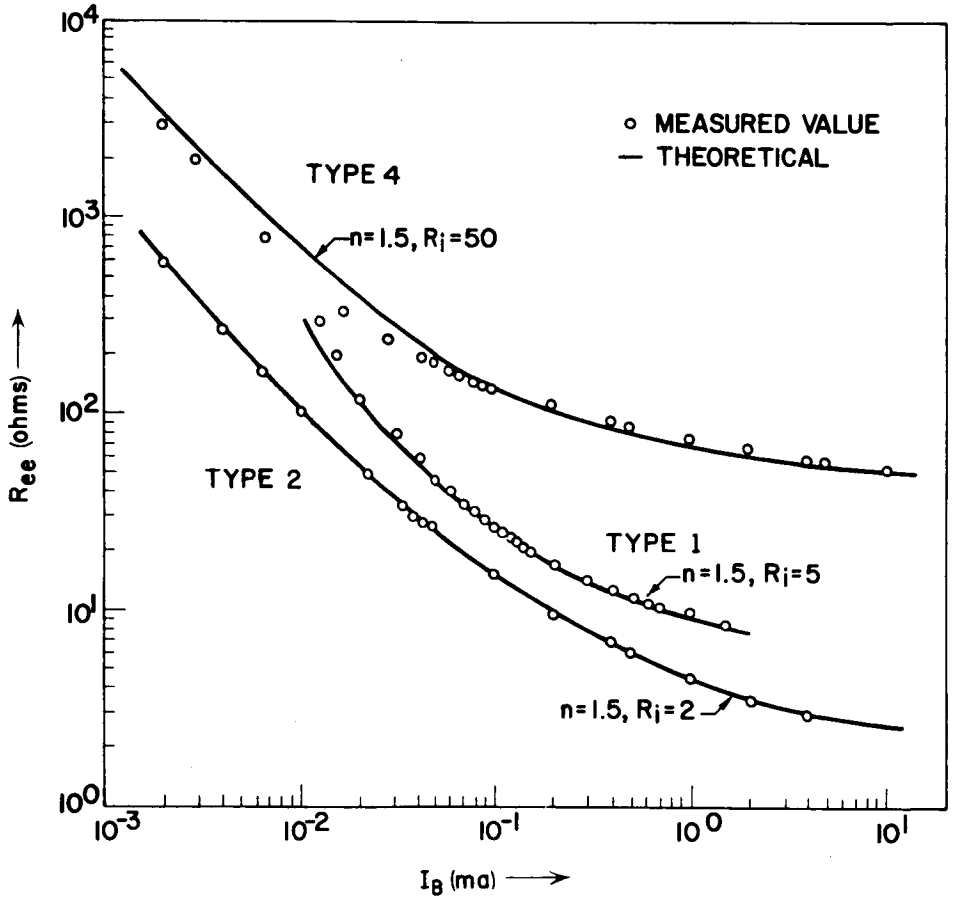


FIGURE 22 - ON IMPEDANCE vs. I_b

The optically driven DET obeys the same general theory as the electrically driven one. In this case, there is no connection to the base emitter junction, and the device is turned on by an effective base current generated through the absorption of photons in the bulk of the device. It is apparent that in principle the optically driven switch closely approximates the mechanical relay since the switch control is isolated from the switch contacts. This feature gives the optical switch a decided circuit advantage over its electrical counterpart. To study the optical switch more closely, devices were made on a wafer, such that devices in even numbered rows had base contacts and could be electrically driven, whereas devices in odd numbered rows had no base contacts. Figure 23 shows plots of the ON impedance of three optically driven DET's as a function of GaAs diode current. For 80 ma through the diode, the Type 2 units show the lowest ON impedance.

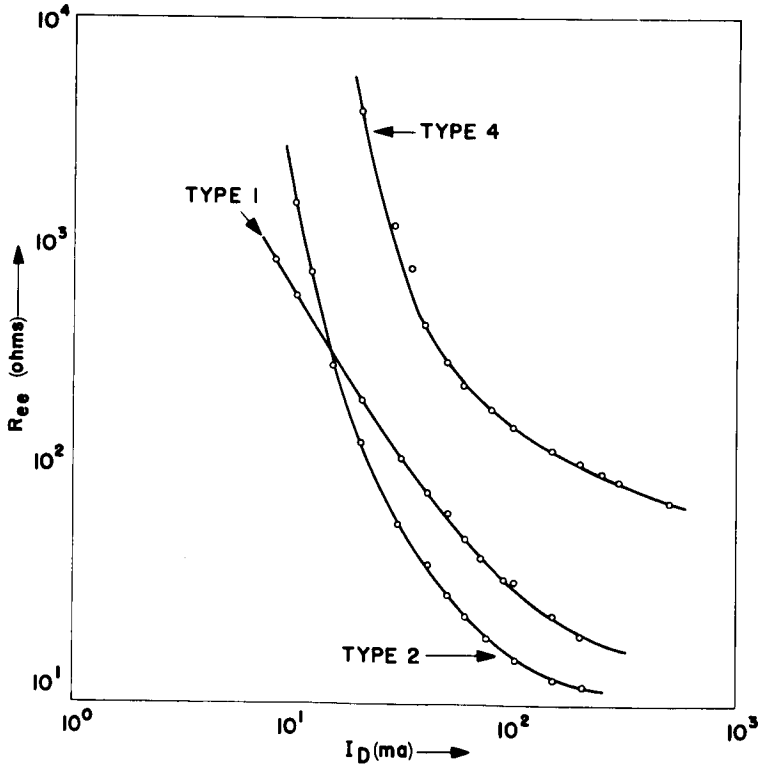


FIGURE 23 - ON IMPEDANCE vs. I_d

By comparing DET units that were driven electrically and optically and using the ON impedance as the normalizing parameter, a plot of effective base current vs. the diode drive current could be made, as shown in Figure 24. Such a plot permits an estimate of conversion efficiency. (See Section 4.)

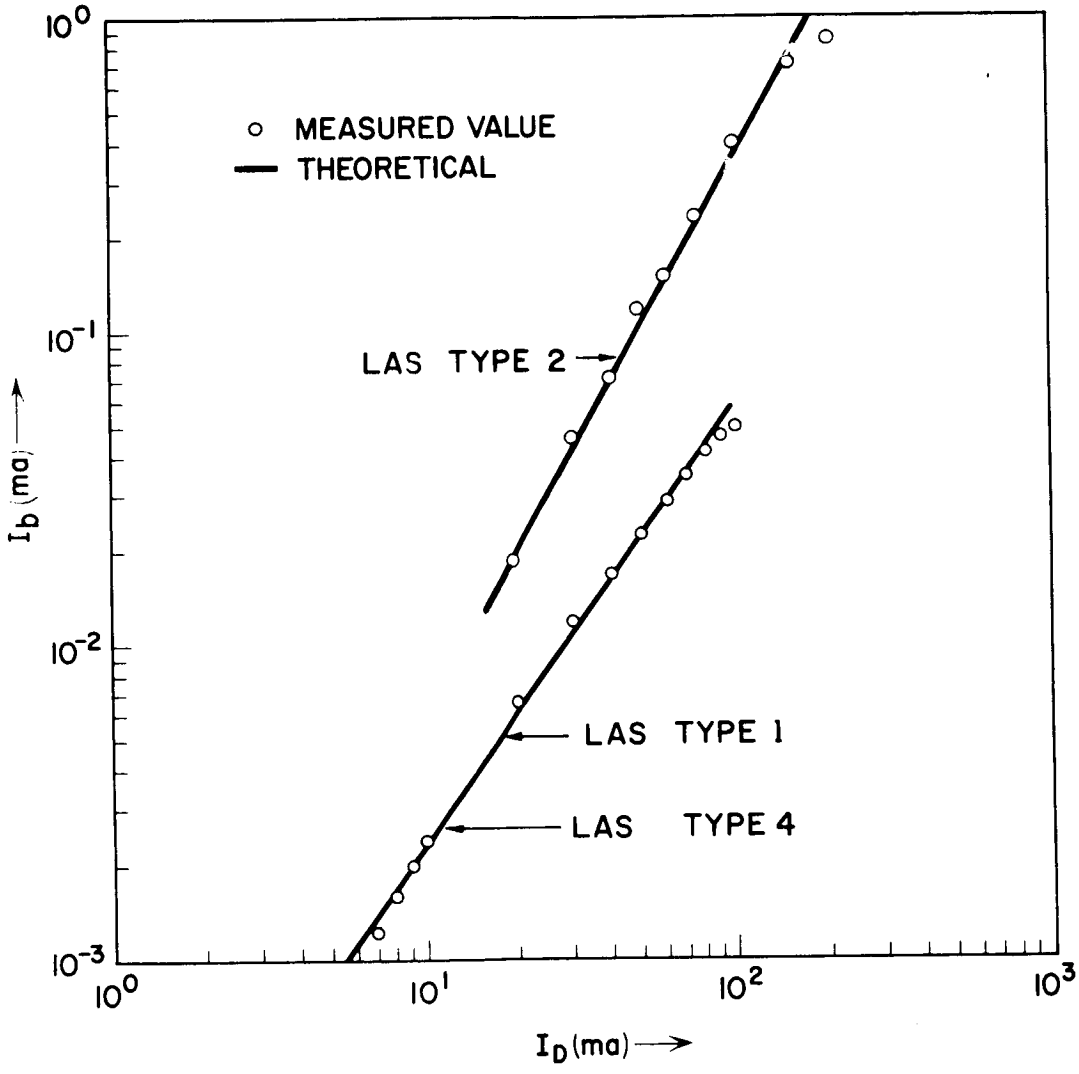


FIGURE 24 - EFFECTIVE BASE CURRENT I_b vs. I_d

Figures 25 a and 25 b shows plots of how the offset voltage varies at room temperature with the diode current for two optically driven DET's. The calculated V_0 values using equation (B-10) and the measured β values are also shown in the figures. The quantitative agreement between theory and experiment could be better; some of the errors could probably be attributed to β and V_0 measurements. With a diode drive current of 100 ma, the effective base current is approximately 5×10^{-2} ma for a Type 4 DET as shown in Figure 24). The corresponding β_i value from Figure 21c is approximately 41. According to eq. (B-18) and assuming n = 4, the value of BV_{ee} is 27.6 volts.

Experimentally, BV_{ee} values of 30 ~40 volts have been obtained. The apparent discrepancy is due to the approximate nature of eq. (B-18). BV_{ee} values for Type 1 and Type 2 DET's were in the ranges of 10 ~ 15 volts and 20 ~ 25 volts, respectively.

3.6 TRADEOFF CONSIDERATIONS

A study has been made to evaluate any possible compromise between the DET size and performance upgrading. The study has been made on Type 1, 2 and 4 DET units and the results were similar in all cases.

DET units, having collector/emitter areas of 402/270, 243/145 and 125/56 square mils, were processed on a single wafer (Type 2 units will be discussed).

The inverse gain measurements, β_i, shown in Figure 26, agreed with theoretical expectations. Since β_i is directly proportional to the ratio of the emitter to collector areas, the gain should be higher for the large size devices.

	Large	Medium	Small
Ae/A_c	0.67	0.59	0.44
β_i (I_b = 0.1 ma)	42	36	22

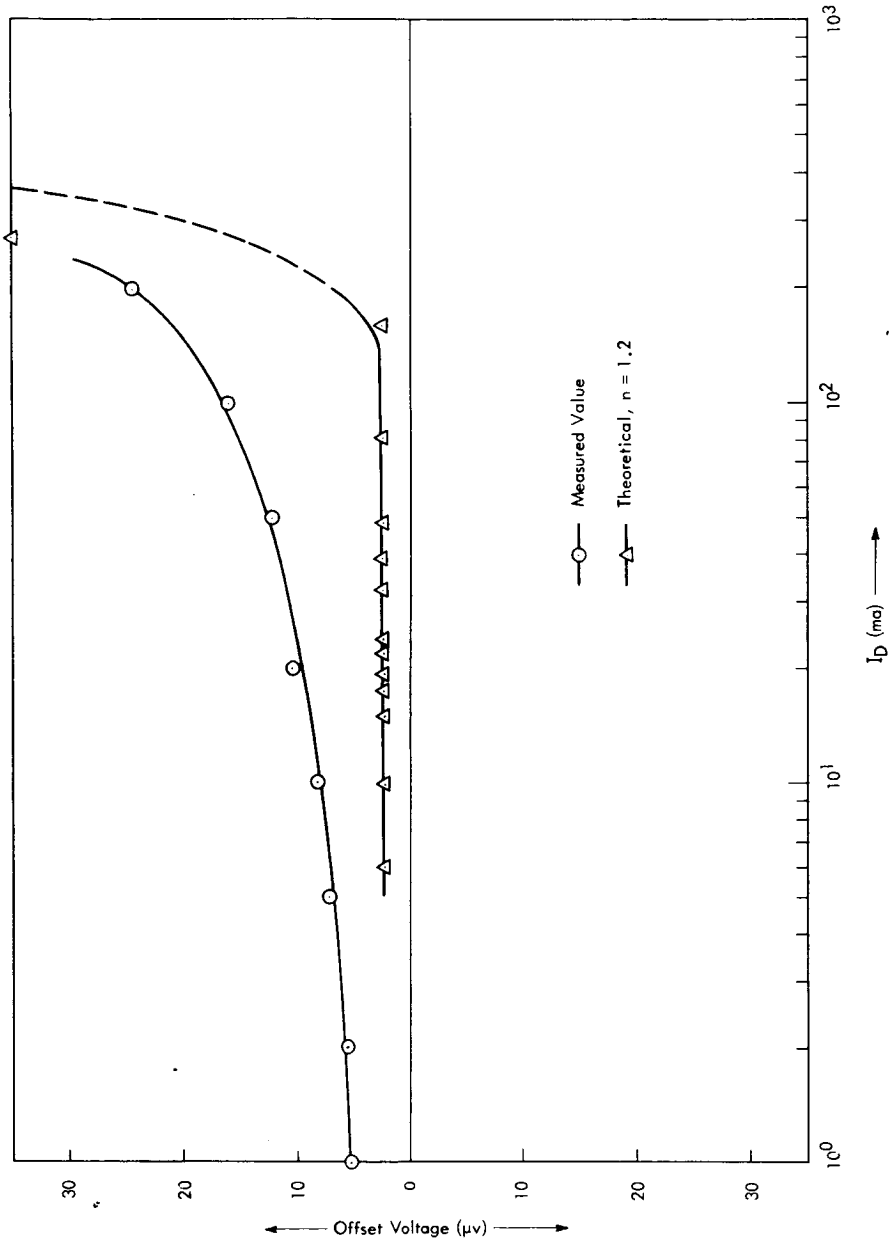


FIGURE 25 a - OFFSET VOLTAGE, V_o, vs. I_d (TYPE 1)

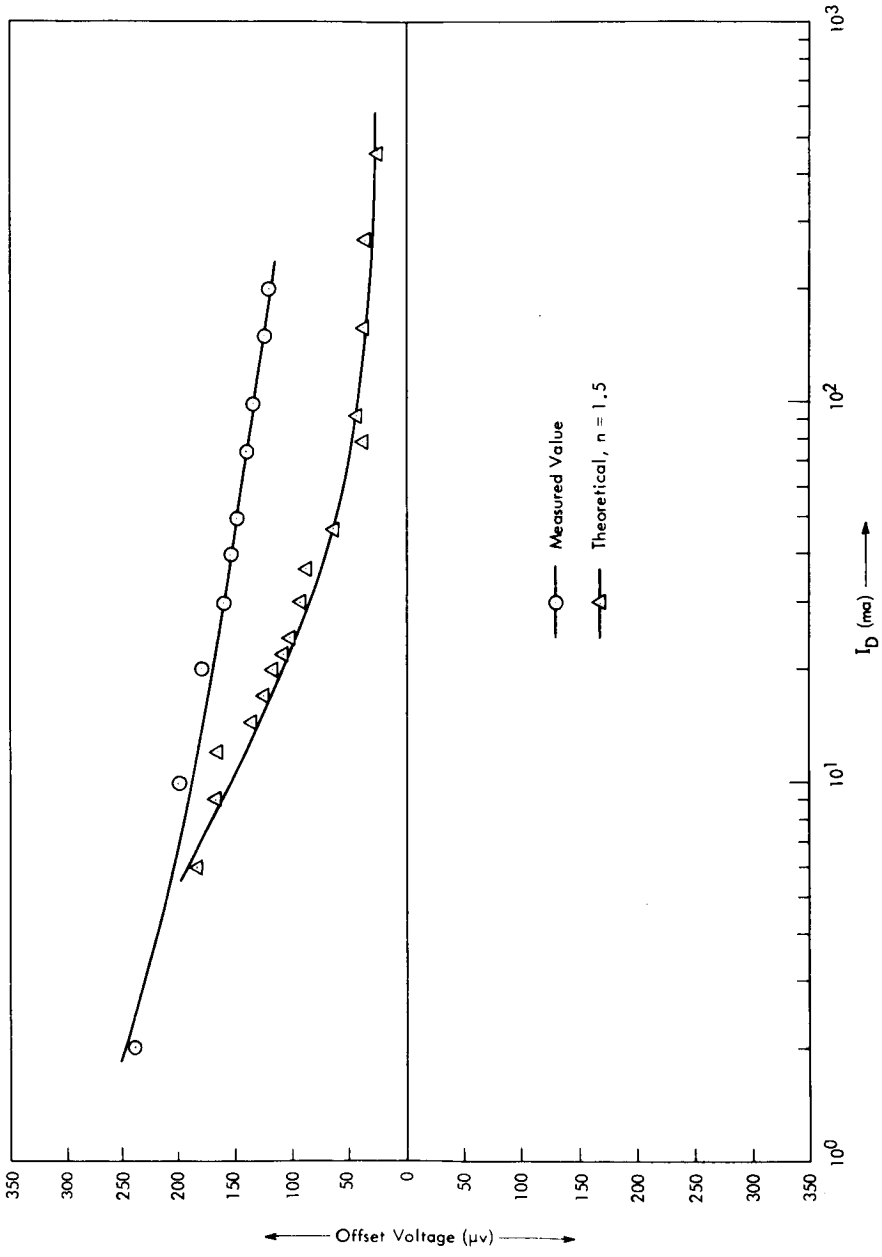


FIGURE 25 b - OFFSET VOLTAGE, V_o, vs. I_d (TYPE 4)

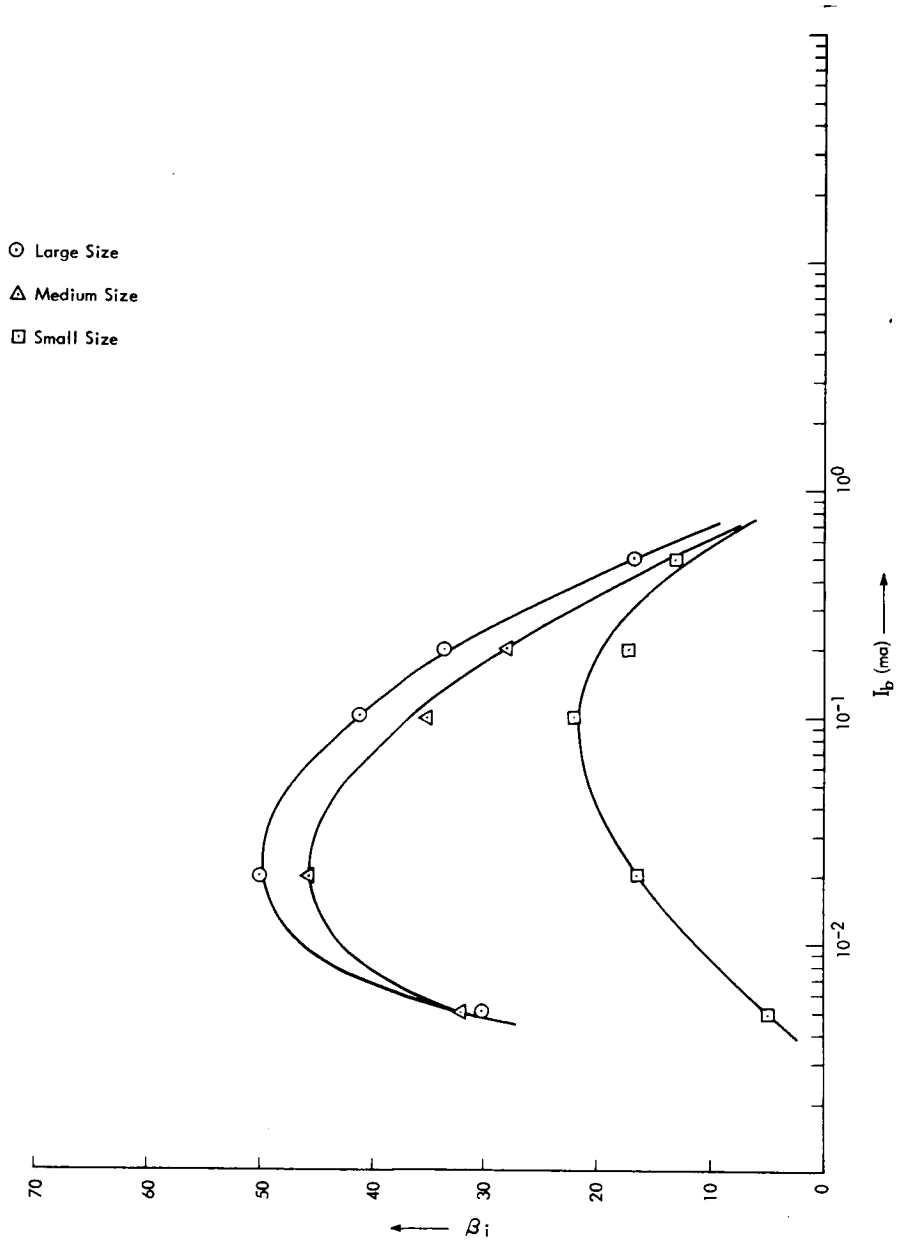


FIGURE 26 - β_i vs. I_b (TYPE 2)

The ON impedance of the switch is inversely proportional to the product of I_b and β_i. Furthermore, I_b is known to be directly proportional to the useful area of the DET, i.e., area through which photons enter the device. Therefore, switches having small size DET's should have higher ON impedance values as compared to those switches having medium or large size DET's. Figure 27 shows just such a comparison.

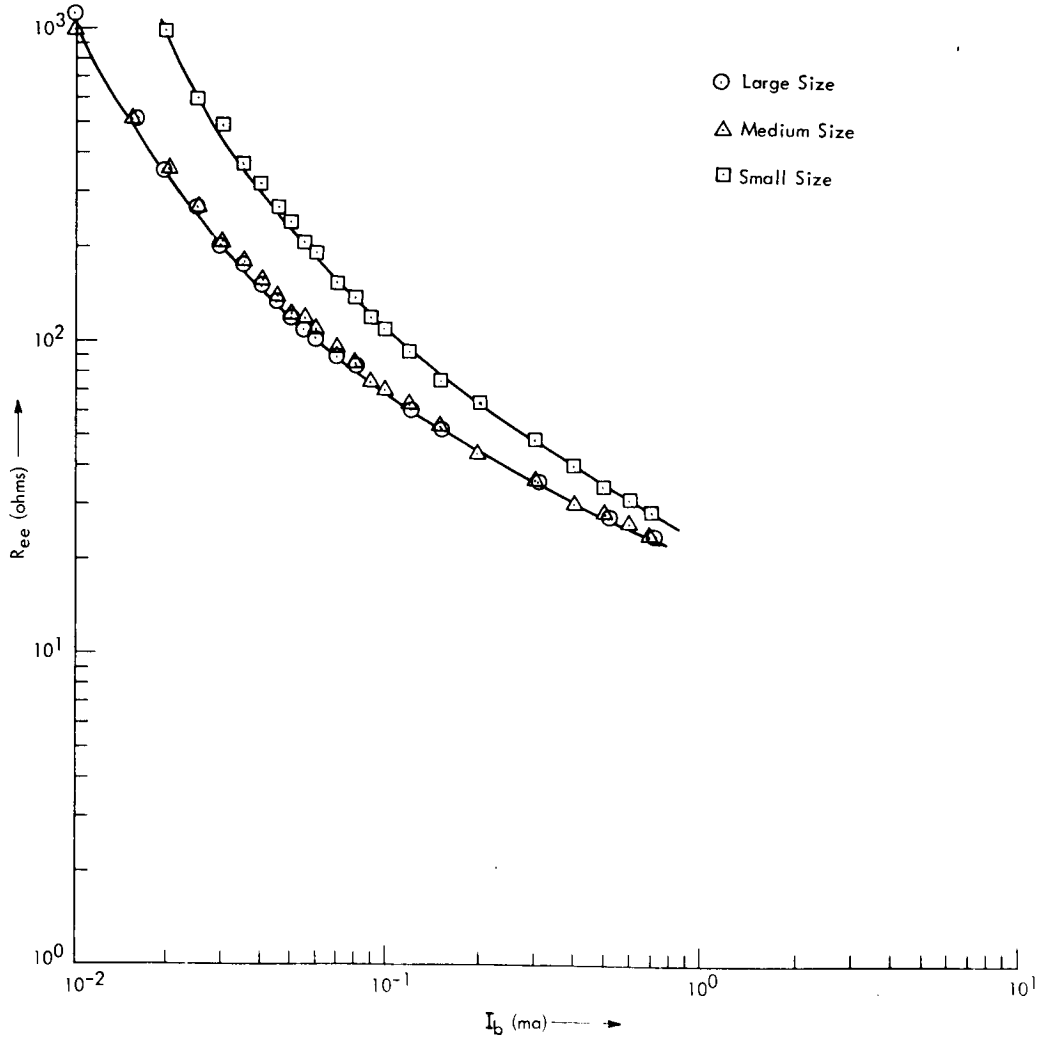


FIGURE 27 - ON IMPEDANCE vs. I_b (TYPE 2)

Since large and medium size DET units have high β_i values as compared to the small size, they should have a lower breakdown voltage, BV_{ee}, according to equation B-18. Table 2 gives typical BV_{ee} results for the three different size units.

TABLE 2

EFFECT OF DET'S SIZE ON BREAKDOWN VOLTAGE

	BV_{ee1} (@ 100 μ a)	BV_{ee2}
Large Size	26/18.5 (*)	25/17.5 (*)
	28/18.5	30/19.5
Medium Size	30/19.0	21/13.5
	31/18.5	28/17.0
Small Size	32/26.0	29/23.5

(*) The first value is the maximum value of BV_{ee} and the second is the "snap-back" value.

Devices in alternate rows on the wafer had provision for base lead attachment. This permitted fabrication of DET units that could be driven electrically instead of optically, and some comparison data between the different size detectors was obtained.

Figure 28 shows the R_{ee} dependence on I_D, and Figure 29, the conversion efficiency for the different sized units.

In this entire study, the size difference from large to medium units is not as significant as the size change from medium to small.

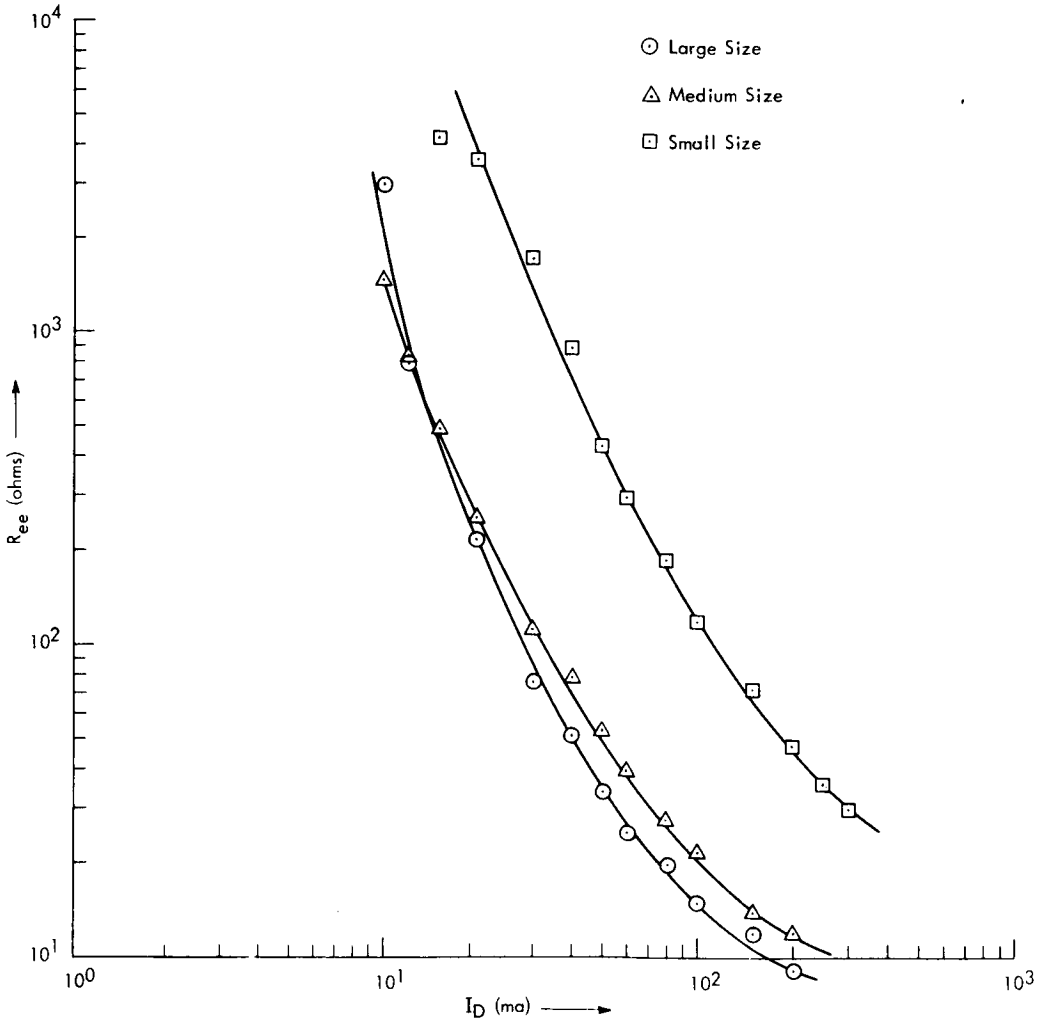


FIGURE 28 - ON IMPEDANCE vs. I_d (TYPE 2)

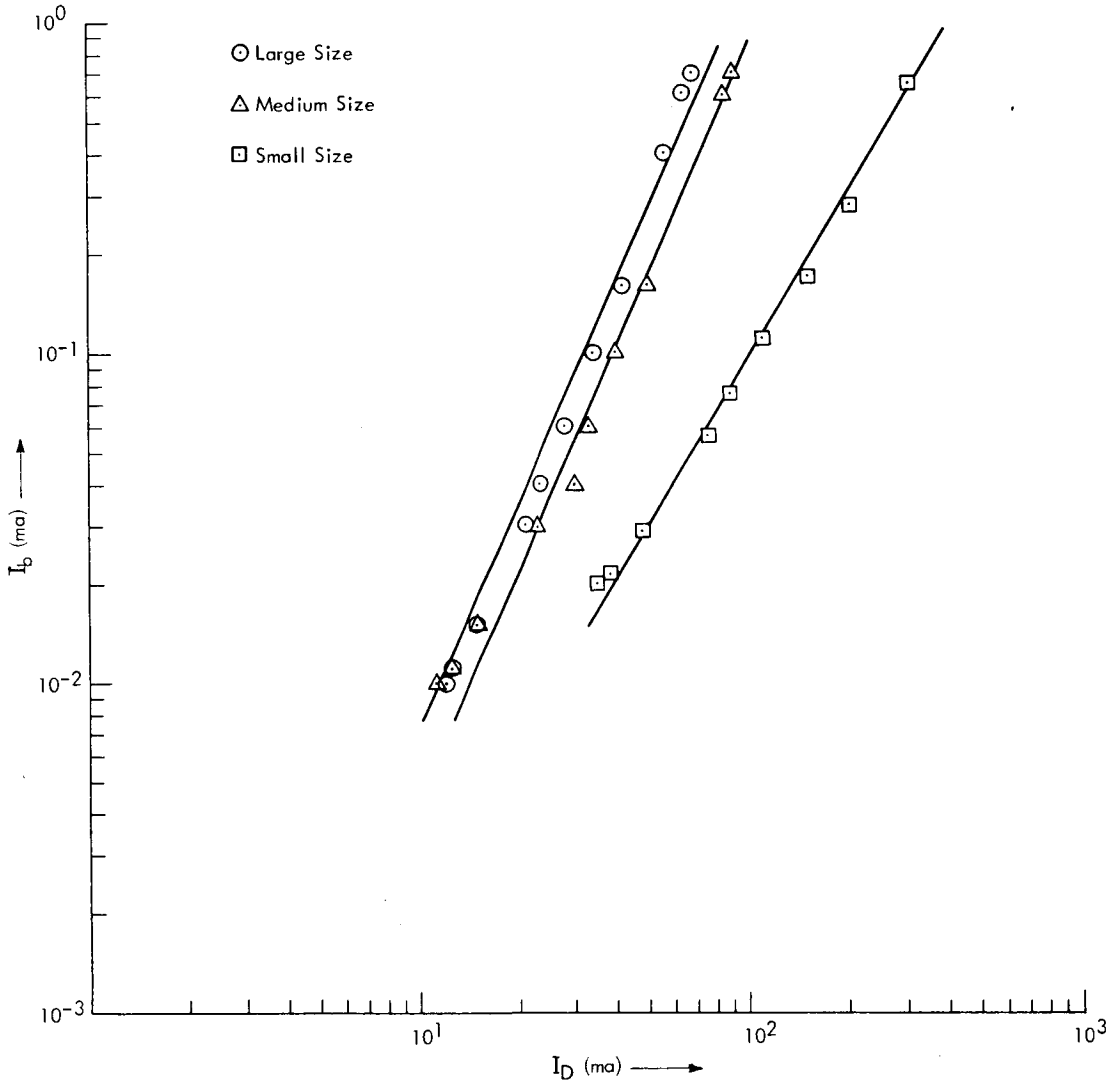


FIGURE 29 - TRANSFER EFFICIENCY vs. DET SIZE (TYPE 2)

3.7 DET FABRICATION

A detailed fabrication procedure is given for the four Types of DET units that were studied. A typical set of masks that were used in the KPR* process steps for the Type 1 and 2 DET units is shown in Figure 30.

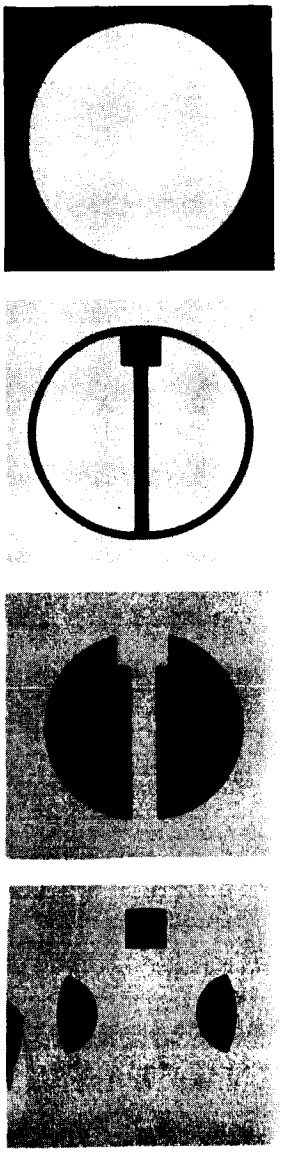


FIGURE 30 - MASK SET FOR DET FABRICATION

*Trademark - Eastman Kodak Co. (Kodak Photo Resist)

3.7.1 Type 1 - NPN, Double Diffused DET

Starting Material - Epitaxial N layer on an N+ substrate.

(N) - Phosphorus-doped, 1.0 ohm-cm, 10 microns thick

(N+) - Antimony-doped, 0.01 ohm-cm, (111) orientation

Initial Oxidation: The purpose of this step is to cover the wafer with a uniform oxide layer.

T = 980°C, time adjusted to produce approximately 5000 angstroms of oxide thickness.

Base Diffusion - (Figure 31 a)

KPR process to open base region in oxide.

Boron diffusion to achieve a junction depth of 3.0 microns and a surface concentration of 1.5×10^{18} cm^{-3}.

Emitter Diffusion - (Figure 31 b)

KPR process to open emitter holes in oxide.

Phosphorus diffusion to achieve a junction depth of 2.0 microns with a surface concentration of 5×10^{20} cm^{-3}.

Contact Metallurgy - Two processes have been used. (See Figure 31 c)

Aluminum Process:

KPR process to open contact holes in oxide.

Evaporate aluminum with substrate temperature at 200°C.

KPR process to produce pattern for subtractive etching of aluminum.

Alloy contacts in a vacuum oven at 450°C for approximately 2 minutes.

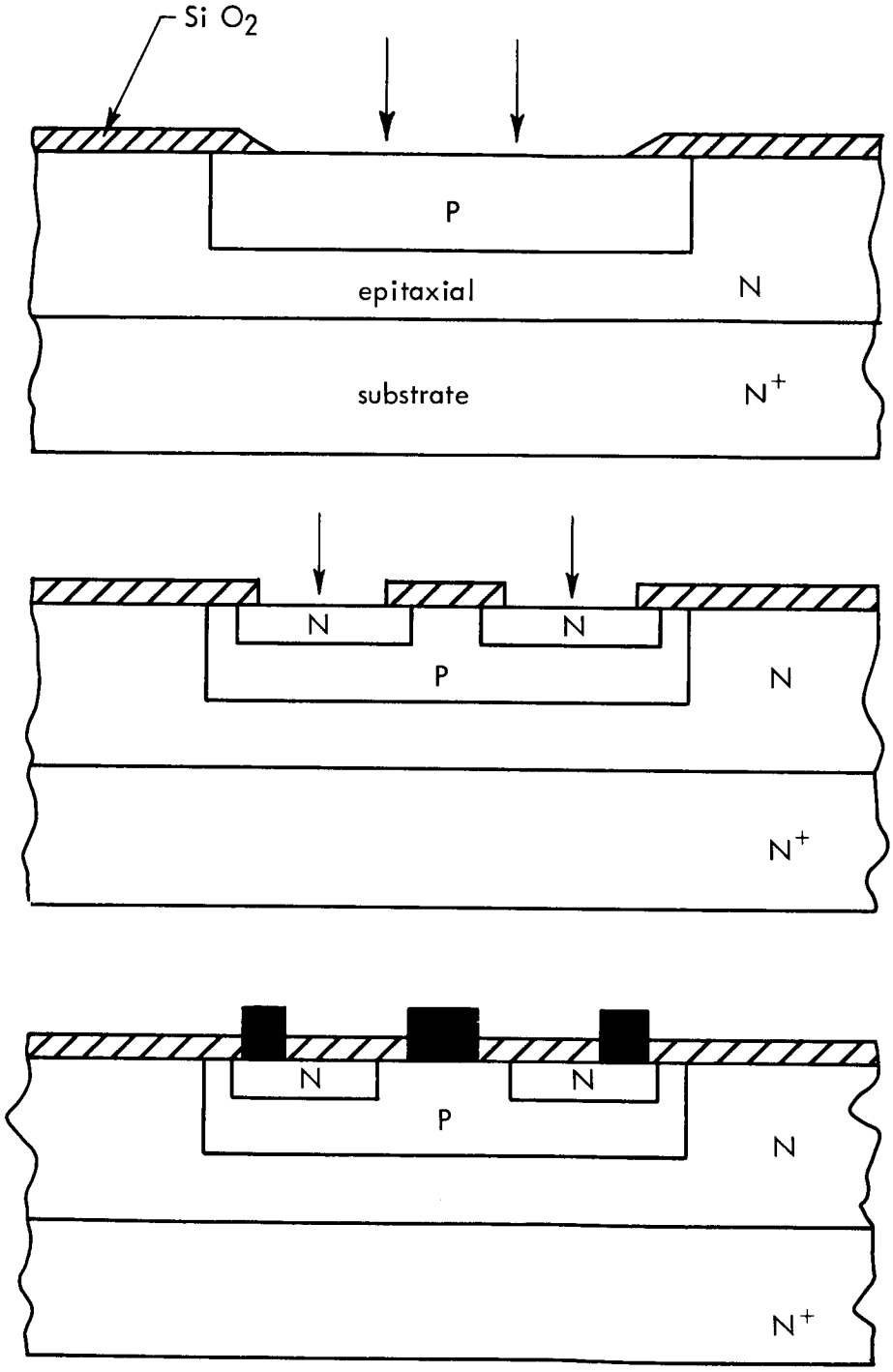
Platinum Process:

KPR process to open contact holes in oxide.

Evaporate platinum, using an electron gun, from a carbon container.

Alloy contacts in vacuum oven at 600°C for 2 minutes.

Remove Pt in unwanted regions by mechanical polishing.



a) Collector Diffusion

b) Emitter Diffusion

c) Contact Application

FIGURE 31 - FABRICATION STEPS FOR TYPE 1 DET

3.7.2 Type 2 - NPN, Single-Diffused, Single Epitaxial DET

Type 3 - NPN, Single-Diffused, Double Epitaxial DET

Starting Material

(Type 2) Epitaxial P layer on an N+ substrate

(P) - Boron doped, 2.0 ohm-cm, 3.0 microns thick

(N+) - Antimony doped, .012 ohm-cm, (111) orientation

(Type 3) Epitaxial P layer, grown onto an epitaxial N+ layer, which was grown on an N+ substrate. The epitaxial (N+) layer was Phosphorus-doped, 0.01 ohm-cm and had a thickness of 5.5 microns. The other layers were same as shown above in Type 2.

Initial Oxidation - T = 980°C, time adjusted to produce approximately 5000 angstroms of oxide thickness.

Pinch-off Diffusion (Isolation) -(Figure 32 a)

KPR process to isolate base region.

Phosphorus diffused at 1100°C. Diffusion time adjusted to achieve complete isolation of the P-Type base region.

Etch wafer in buffered HF acid to remove any P_2O_5 glass without disturbing the initial oxidation over the base region.

Re-oxidation at 980°C

Guard Ring Diffusion -(Figure 32 b)

KPR process to open ring in base region.

Boron diffused at 940°C for approximately 20 minutes.

(diffusion depth is not critical).

Emitter Diffusion -(Figure 32 c)

KPR process to open emitter areas

Phosphorus diffused at 970°C. Time adjusted to produce a junction depth of 1.5 microns with a surface concentration of approximately 5×10^{20} cm^{-3}.

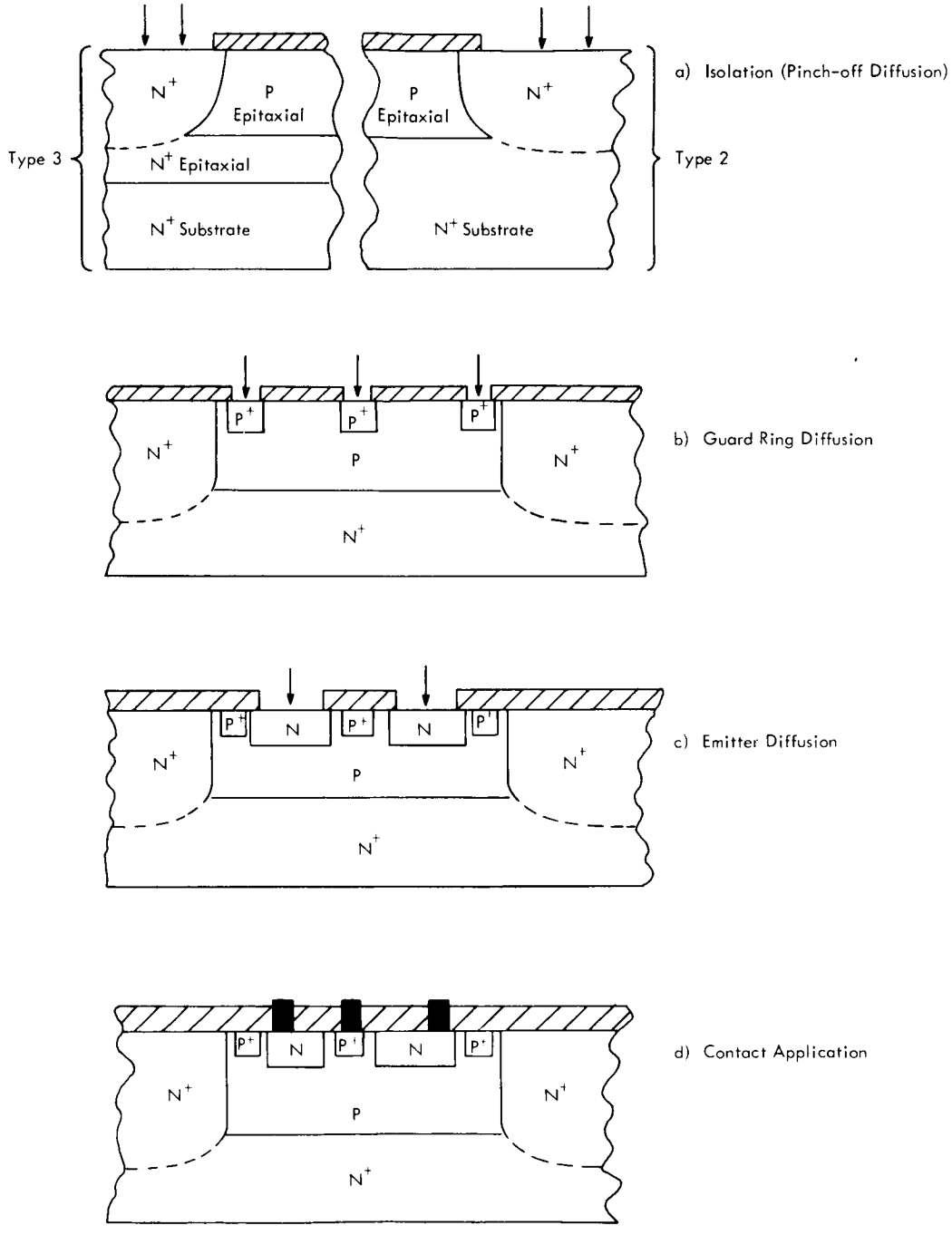


FIGURE 32 - FABRICATION STEPS FOR TYPES 2 & 3 DETS

Contact Metallurgy - (Figure 32 d)

KPR process to open contact holes in oxide.

Evaporate 400-600 angstroms of palladium at a substrate temperature of 200°C.

Alloy contacts in a vacuum oven for about 1 minute at 450°C.

Evaporate aluminum over the palladium - T = 150°C, Al thickness about 1000 angstroms.

Remove metal in unwanted regions by ultrasonic cleaning in distilled water. The palladium does not adhere to the oxide and is easily removed when agitated.

3.7.3 Type 4 - PNP, Single-Diffused, Single Epitaxial DET

Starting Material - N epitaxial layer on a P+ substrate.

(N) - Phosphorus doped, 0.25 ohm-cm, 5.5 microns thick.

(P+) - Boron doped, .015 ohm-cm, (111) oriented.

Initial Oxidation - T = 980°C, time established to produce an oxide layer of about 5000 angstroms.

Pinch-off Diffusion (Isolation) - (Figure 33 a)

KPR process to isolate base region.

Boron diffused at 1200°C and time adjusted to produce complete isolation of the N region. (The epitaxial interface junction position will change as shown, during the pinch-off diffusion.)

Emitter Diffusion - (Figure 33 b)

KPR process to open emitter holes in oxide

Boron diffused at 1200°C. Time adjusted to produce a junction depth of 2.0 microns and a surface concentration of about 10^{20} cm^{-3}.

When base contacts were required, a phosphorus diffusion was made at 1100°C, for about 3 minutes as shown in Figure 33 c. This produced a highly doped N+ region near the surface, which was necessary for making ohmic base contacts.

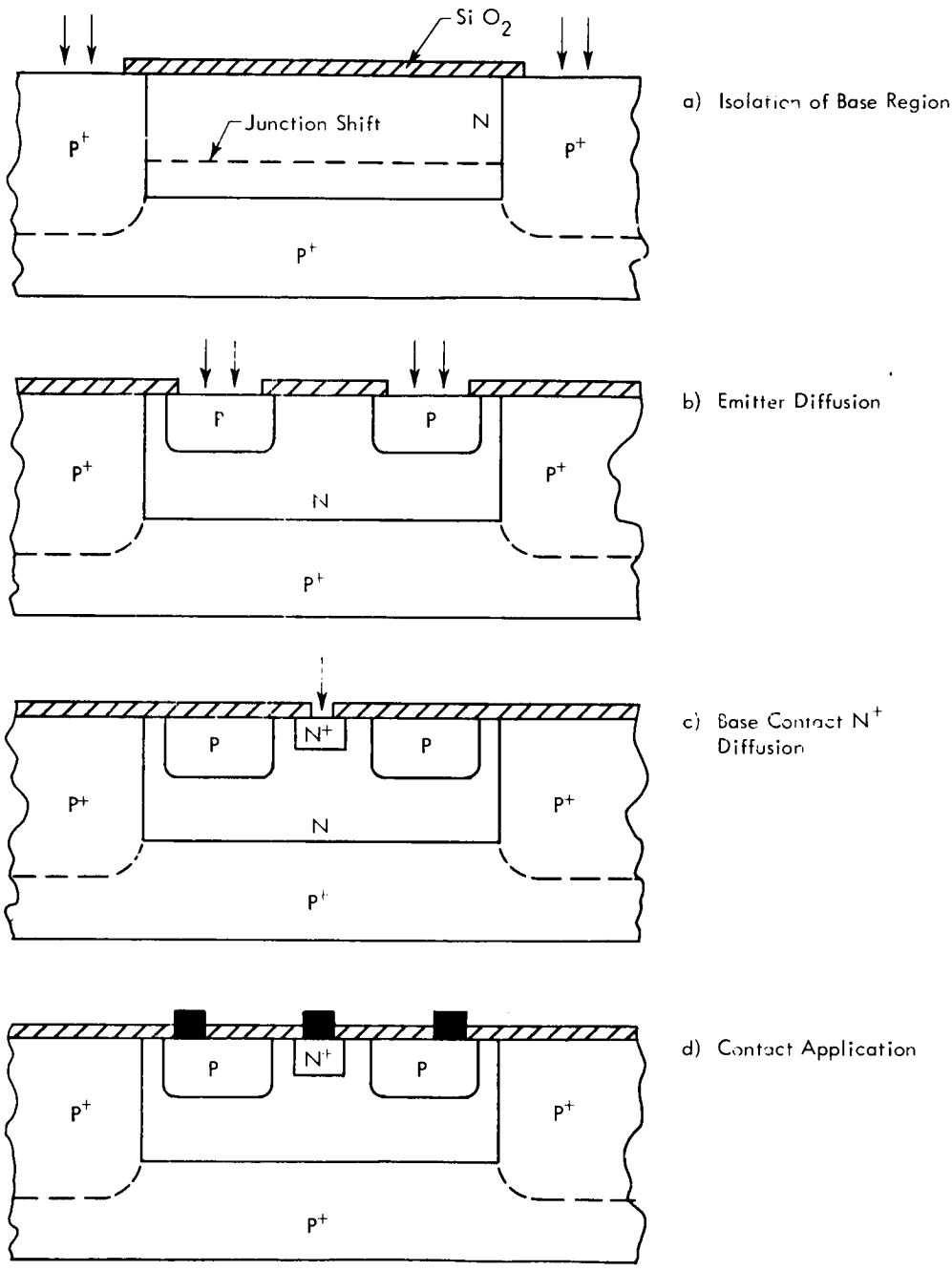


FIGURE 33 - FABRICATION STEPS FOR TYPE 4 DET

Contact Metallurgy - (Figure 33 d)

Method is identical to that described for Types 2 and 3.

After contact metallurgy, the wafer was diced into individual DET units which were mounted temporarily on TO-5 headers for TCB lead attachments. This step was common to all DET types.

3.8 DET TEST PROCEDURE AND RESULTS

During the fabrication process, wafers were tested after each of the following steps:

a. Initial epitaxial material - Several mesa diodes were made on the material, and the quality of the epitaxial junction was examined by measuring the breakdown voltages.

b. After pinch-off diffusion - Breakdown voltages were checked and compared with values obtained in step a.

c. After emitter diffusion - Values of BV_{ee}, BV_{ebo}, BV_{cbo}, β_n, β_i and light sensitivity were measured.

A comparison of these parameters on the various DET types is shown in Table 3.

TABLE 3

DET TEST RESULTS

TYPE	1	2	3	4	Notes on measurement
Measured DET Characteristics					
BV_{ee} (volts)	11.0	17-26	17-24	30-40	K & S Model 313 Three Point Probe with Tektronix Type 575 Transistor Curve tracer. I_s = 100 μ a
R_{ON} (ohms)	3-6	1.5-3	-	16-50	Tektronix Curve Tracer, with microscope light illuminating the device
β_n	500-1400	280-350	280-330	50-70	Tektronix Curve Tracer I_b = 0.2 ma V_c = 0.7 volts
β_i	20-70	18-25	17-20	5-30	Tektronix Curve Tracer I_b = 0.2 ma V_c = 0.7 volts

SECTION 4 - INTEGRATED SWITCH (LAS)

4.1 SWITCH ASSEMBLY PROCEDURE

Tested DET chips were removed from their temporary mountings and suspended over the diodes by bonding the emitter leads to the posts of the TO-18 header on which the diode was already mounted (see Figure 34a). An optical coupling medium (Randac epoxy) was applied between the diode and DET. The epoxy was cured in air at 60°C for 20 hours followed by a cure at 80°C for one hour. The integrated switches were then encapsulated.

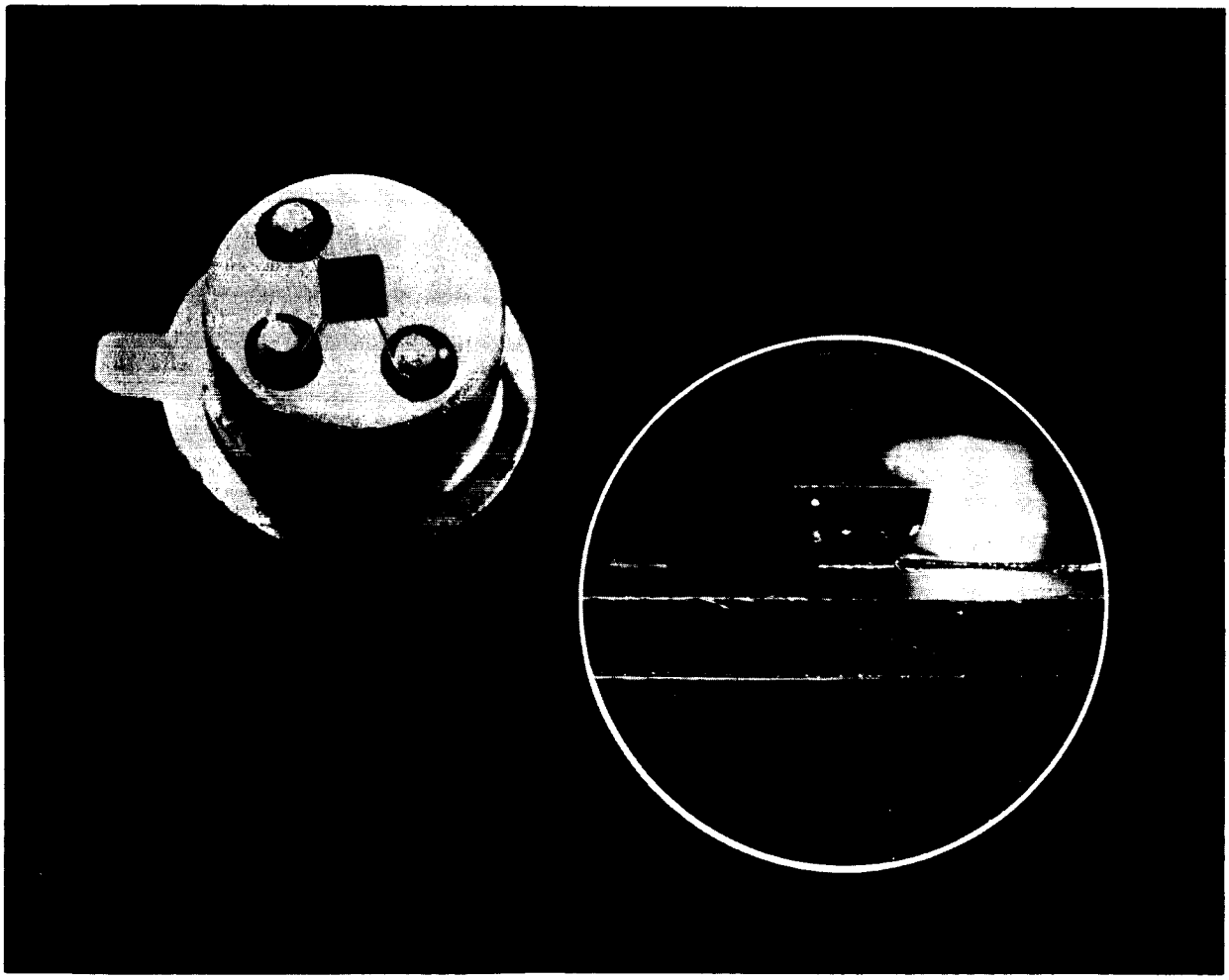


FIGURE 34a - LAS ASSEMBLY

Since the DET size is greater than the diode, alignment was facilitated by scribing guide lines on the TO-18 header as shown in Figure 34b. The infrared transmission photograph shows good alignment using this technique.

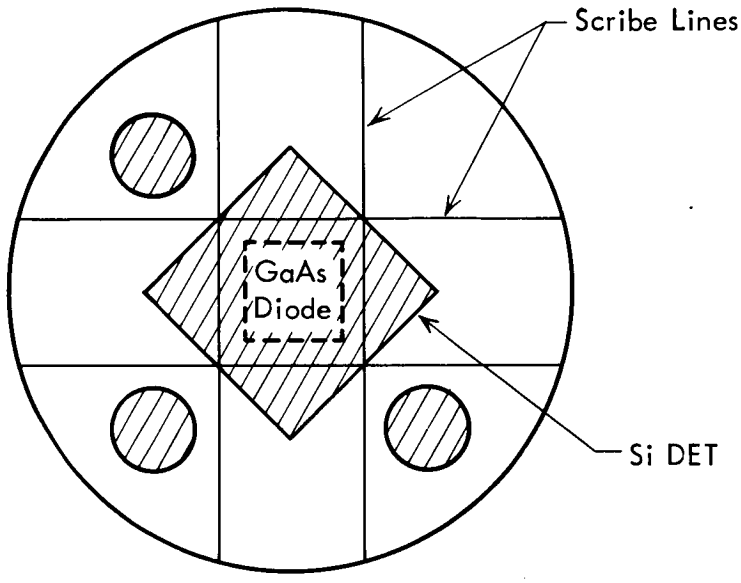


FIGURE 34b - LAS SCRIBE LINES

4.2 PACKAGING CONSIDERATIONS

The type of LAS package strongly influences the switch characteristics. Several studies have been made on the present switch package, and the results are discussed.

4.2.1 LAS Efficiency

The efficiency of the LAS was determined empirically from Figure 24.

Using I_D = 80 ma and selecting I_b from Figure 24, η_{LAS} is found to be approximately 0.06% for switches with Type 1 and 4 DET units and 0.30 - .35% for Type 2 LAS devices. This difference in efficiency is due primarily to the difference in junction quality between the single and double diffused DET's. Specific reference is made to the collector base junction which in one case is an epitaxially grown junction, whereas in the other it is a diffused junction. The low efficiency of the Type 4 switches can be explained by the movement of the collector-base junction during subsequent heat treatments. This movement is due to an impurity redistribution which changes the junction from abrupt to diffused.

4.2.2 Improved Light Coupling

A point source of light placed in the focus of a parabolic reflecting surface will generate a parallel beam whose width is equal to the opening of the parabolic reflector. From photographic evidence, a considerable portion of the light emitted by the GaAs source appears at the edge of the diode junction. A parabolic focusing scheme seemed like a desirable solution to increase the amount of light leaving the source. Figure 35 shows the light output from diodes employing different header arrangements.

In these experiments, the silicon solar cell detector was not coupled directly to the epoxy, as is the case in an actual LAS. To simulate the actual LAS, complete switches were fabricated in three configurations as shown in Figure 36, and the ON impedance was measured for each case under identical conditions. The three cases were as listed below:

1. The DET was mounted on top of a deep parabolic dent (diode inside) as shown in Figure 36a, R_{ee} = 50 Ω.
2. The DET was mounted on top of a shallow parabolic dent (diode inside) as shown in Figure 36b, R_{ee} = 19 Ω.
3. The DET was mounted on top of the diode which is mounted flat on the header as shown in Figure 36c, R_{ee} = 10 Ω.

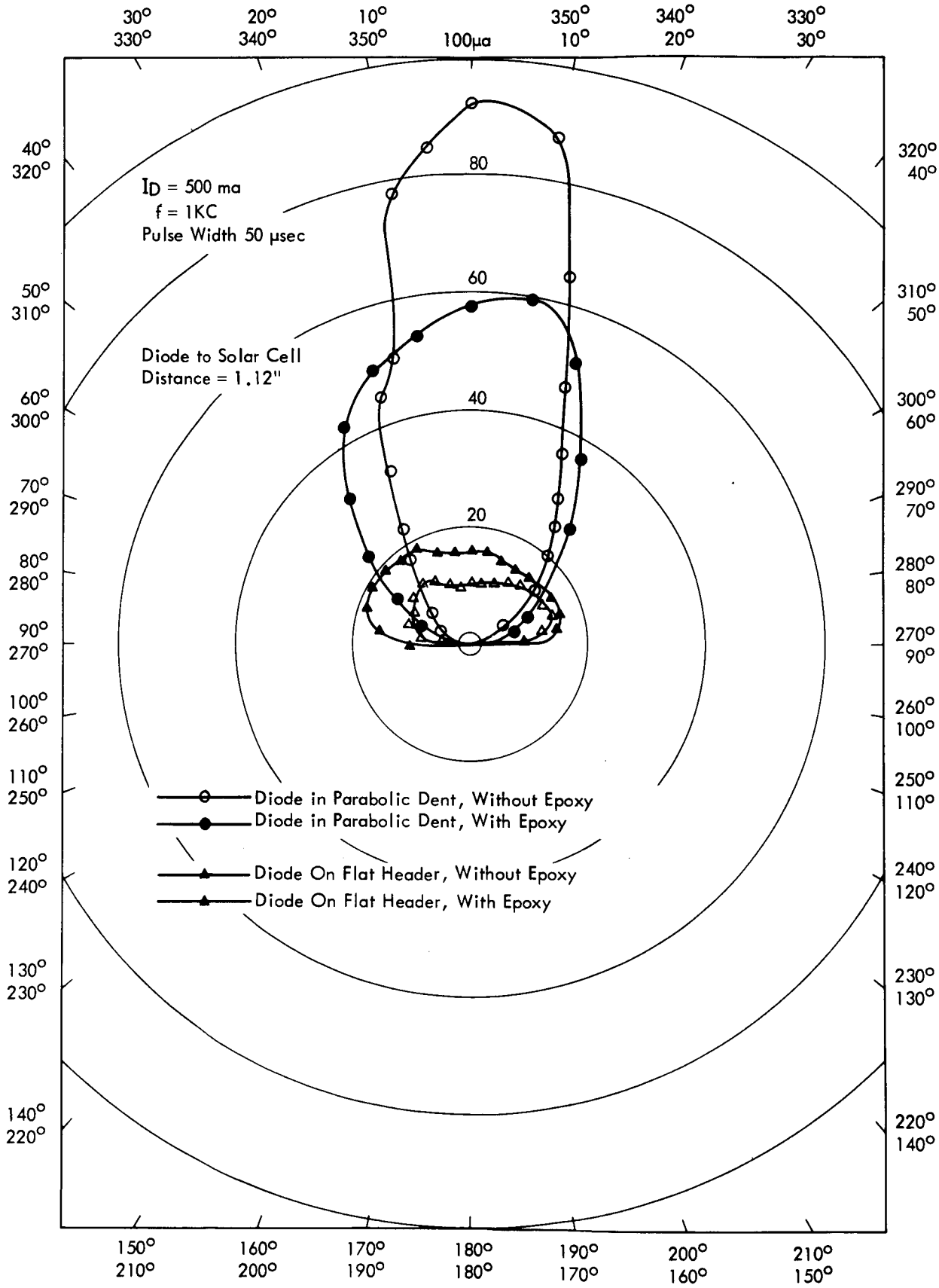


FIGURE 35 - EFFECT OF PARABOLIC FOCUSING

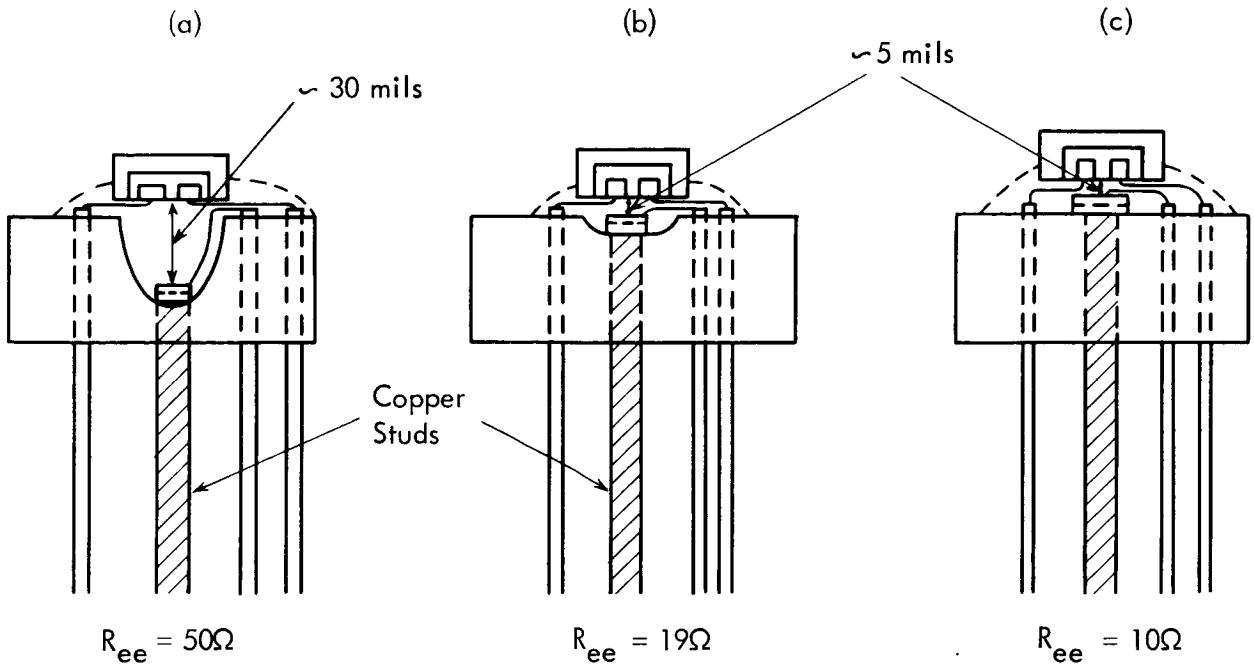


FIGURE 36 - R_{ee} VARIATION WITH LAS FOCUSING ARRANGEMENT

Epoxy was used in all cases as the coupling medium. The higher R_{ee} value in case 1 could be partially attributed to the large separation distance between diode and detector (approx. 30 mils) as compared to only 5 mils in case 3. The R_{ee} value for the second case approaches in the limit, the R_{ee} value of the third case. The conclusion one can draw from these experiments is that, for the present, the flat package gives the best results with epoxy filling the gap between source and detector.

Another approach was considered for improving the light coupling, viz., the use of some high index of refraction glass in place of the epoxy currently used. The requirements imposed on the glass are:

a. High index of refraction; i.e., the value for glass should be as close to 3.5 - 3.6 (GaAs, Si) as possible.
b. Coefficient of thermal expansion should be compatible with both GaAs and Si.
c. Melting and softening point should be low in order to be compatible to processing temperatures.
d. No undesirable impurities from the glass should enter into the GaAs or Si.
e. Low thermal resistance to insure best heat dissipation.

Though several glasses were investigated, none seemed to fulfill all of the above requirements.

4.3 SWITCH TEST PROCEDURES

The test procedures that were followed are those specified in JPL Specification # 31140. A detailed outline of these appears in Appendix A. All of the results quoted in the following sections and all of the tests performed were obtained on switches packaged in the arrangement described in section 4.2.

4.4 SWITCH TEST RESULTS

Characterization served a very important role in the development of the LAS. It was a tool with which the success of the work could be measured at every stage of the development. To minimize switch destruction and errors due to switch heating, overdriving,etc., pulse conditions were employed instead of D.C. conditions whenever possible. The results helped to understand the operation of the LAS and revealed possible new avenues of future work.

In discussing the different parameters, emphasis will be on the final version of the switch,viz., on LAS incorporating Type 2 and Type 3 DET's. Parameter values differing greatly from those of the above will also be given for the other types.

a. R_1 - Switch Open D.C. Impedance.
   This parameter is a measure of the leakage through the switch in its OFF condition. The higher R_1 is, the lower is the leakage between the emitters and the closer the LAS approaches an ideal switch. Out of twenty typical units tested at + 85°C, only one was below the specified 100 M Ωminimum. All the others were well over this value. At + 25°C, not one unit was below 3500 M Ω. Table 4 gives the R_1 values of all twenty devices at both + 25°C and + 85°C temperatures.

b. R_2 - Switch Input to Ground D. C. Impedance.

The measure of isolation between control element and device contact is the value of R_2. This quantity, according to specifications, was to be at least 100 M Ω. Measurements performed at ± 35 volts at a temperature of + 85°C yielded more than 2.0×10^5 M Ω for all units listed. Table 4 gives the measured R_2 values of all twenty devices.

TABLE 4

I_o, R_1, R_2 - TEST RESULTS

LAS	I_o na		R_1 Ω	R_1 MΩ	R_2 Ω
No. *	@ 25°C	@ 85°C	@ 25°C	@ 85°C	@ 85°C
7	0.056	4.1	8.93×10^{10}	1220	2.19×10^{11}
10	0.032	3.4	1.56×10^{11}	1470	2.33×10^{11}
11	0.058	4.4	8.6×10^{10}	1140	1.84×10^{11}
12	0.021	4.4	2.38×10^{11}	1140	2.07×10^{11}
13	0.063	5.7	7.95×10^{10}	877	2.92×10^{11}
14	0.034	3.8	1.43×10^{11}	1320	2.92×10^{11}
15	0.046	3.6	1.08×10^{11}	1390	2.33×10^{11}
16	0.079	4.6	6.33×10^{10}	1088	2.19×10^{11}
17	1.4	96	3.57×10^{9}	52	2.5×10^{11}
18	.49	33	1.02×10^{10}	152	3.89×10^{11}
19	.58	16	8.6×10^{9}	312	2.19×10^{11}
20	.011	2.6	4.55×10^{11}	1925	2.5×10^{11}
21	.0125	2.5	4×10^{11}	2000	4.27×10^{11}
24	.16	11	3.12×10^{10}	455	2.92×10^{11}
32	.018	2.0	2.78×10^{11}	2500	4.12×10^{11}
33	.085	7.5	5.88×10^{10}	677	6.37×10^{11}
36	.028	1.25	1.79×10^{11}	4000	4.12×10^{11}
38	.098	13	5.1×10^{10}	385	4.67×10^{11}
39	.023	1.5	2.17×10^{11}	3330	4.38×10^{11}
40	.053	6.8	9.45×10^{10}	735	4.12×10^{11}

* Run #173

c. I_o - Switch Open Leakage Current

The leakage current, I_o, is taken from the data of the R_1 tests. It gives a more direct means of evaluating the leakage properties of the LAS. Except for one switch out of twenty that were tested for I_o, none were above 35 na, with 16 units having values below 10 na. Table 4 shows the details of this test. I_o varied linearly with temperature as illustrated in Figure 37.

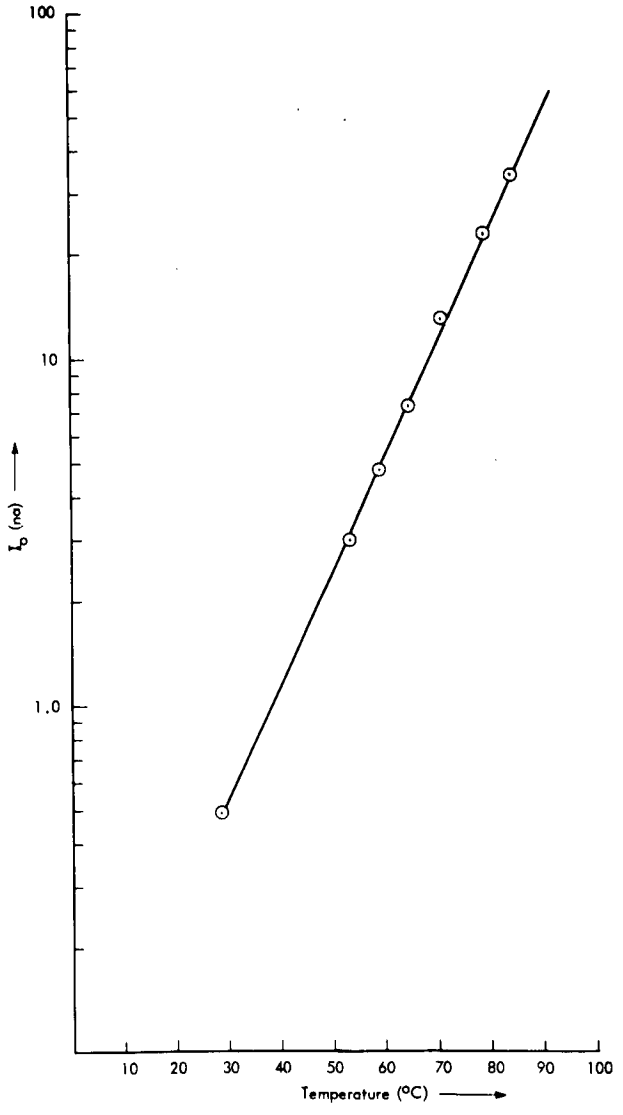


FIGURE 37 - I_o VARIATION WITH TEMPERATURE

d. V_o - Switch Closed Contact Potential (Offset Voltage)

The offset voltage is an indication of the asymmetry that exists between the two halves of the DET. It is easily expressed in terms of the forward gains, β_{n1} and β_{n2}, as shown in section 3.3. V_o was measured for Type 2 - 3 LAS as a function of the diode drive current at - 10°C, + 25°C and + 85°C. For Type 1 LAS tests were performed at + 10°C, + 30°C, + 40°C, + 50°C and + 60°C. At room temperature and + 85°C with I_D = 75 - 80 ma, V_o was found to be equal to or less than 50 μv. The V_o values for the LAS with Type 1 DET's were considerably lower, which was easily accounted for, since the β_n values were very high for these devices. At - 10°C the LAS with Type 2 and 3 units had V_o values between 50 and 150 μv for most of the units tested. The range of the V_o values for a greater number of LAS is given in Figure 38.

e. R_{ee} - Switch Closed D. C. Impedance

For the LAS to approximate the behavior of an ideal switch, the ON impedance under operating conditions should be very low. This parameter was measured for a very large number of switches, because of the amount of information that could be drawn from this measurement. The relative light output of the diode, the efficiency of the optical coupling medium, the sensitivity of the detector, the accuracy of alignment of source and detector are all factors that affect the R_{ee} value. Close to eighty LAS with Type 2 and Type 3 DET's were tested. Most of these were below 25 Ω at I_D = 50 ma and dropped to 10 - 12 Ω at I_D values of 80 - 100 ma. Typical R_{ee} vs. I_D curves are shown in Figure 23, and the variation of R_{ee} with temperature is given in Figure 39. The spread of R_{ee} for a given value of I_D is illustrated in Figure 40.

f. $V_M = BV_{ee}$ - Maximum Overload Voltage

The maximum voltage that the switch can sustain is equal to BV_{ee}, the emitter to emitter breakdown voltage. This quantity specifies the voltage handling capabil-

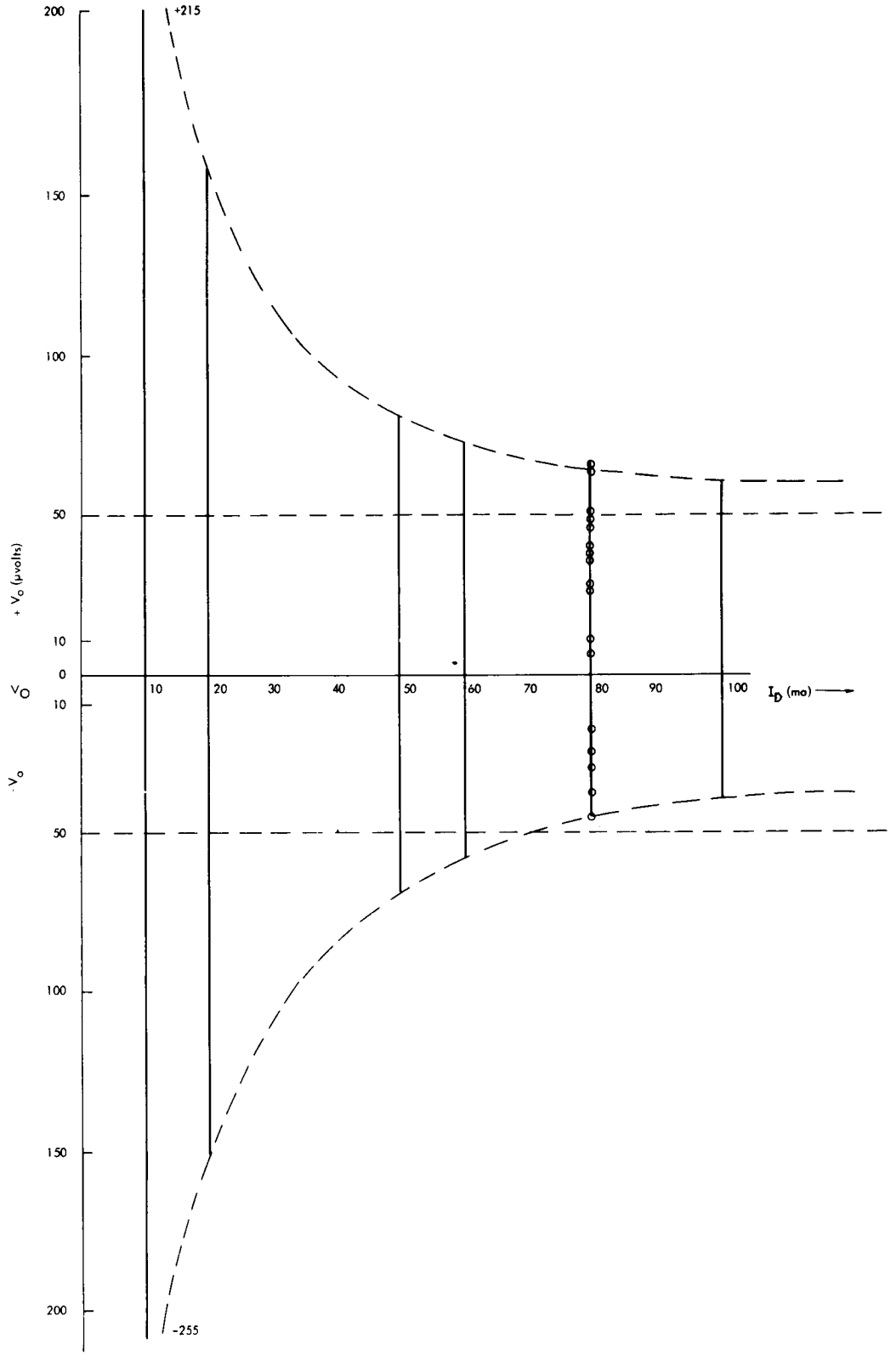


FIGURE 38 - SPREAD OF V_o WITH I_D

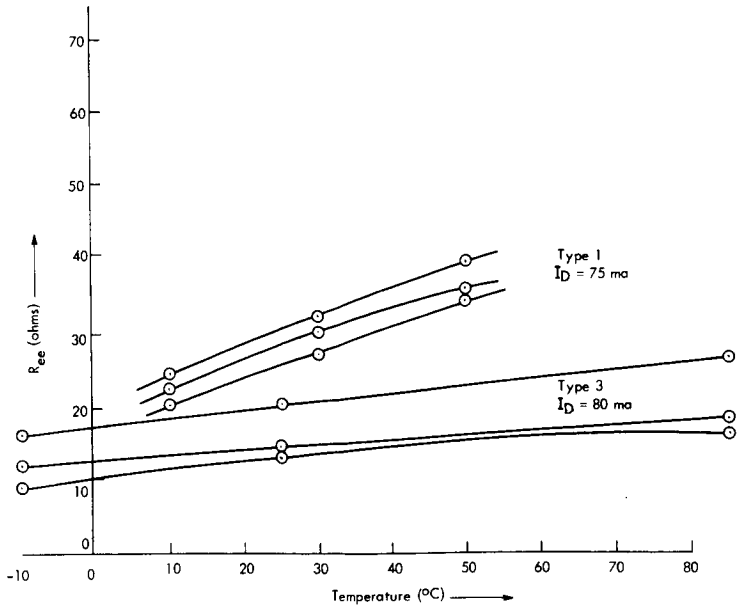


FIGURE 39 - VARIATION OF R_{ee} vs. TEMPERATURE

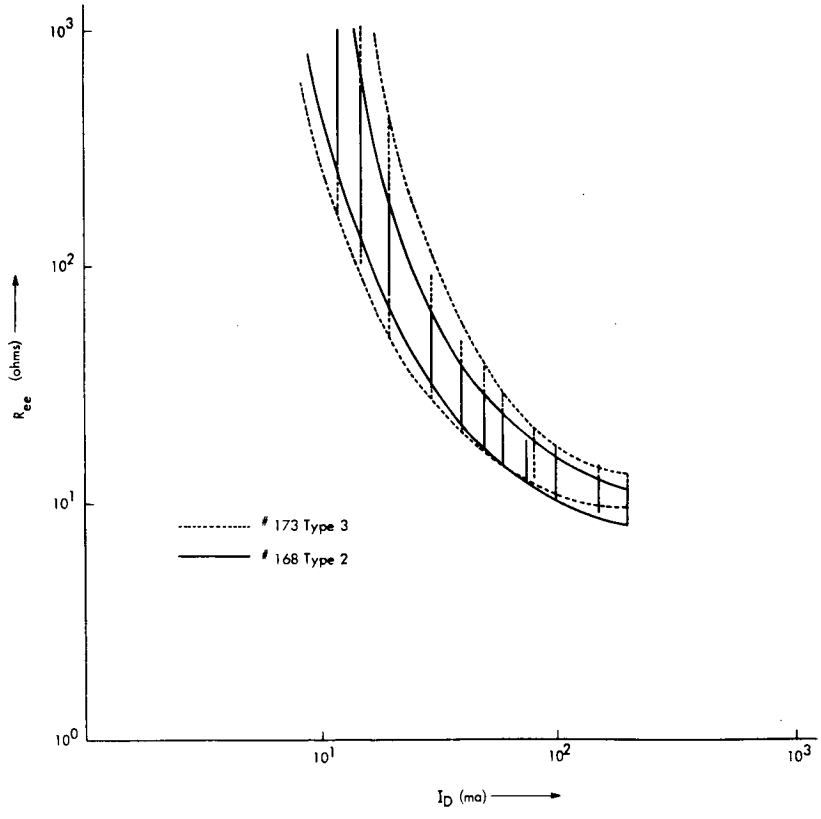


FIGURE 40 - SPREAD OF R_{ee} vs. I_d

ities of the LAS, though it is a quality of the DET itself. In every unit tested, the BV_{ee} values did not change substantially between -10°C and + 85°C (Tables 5a and 5b). In section 3.8, it was shown that BV_{ee} differed for the various DET types.

TABLE 5a

BV_{ee} - TEST RESULTS*

I_s

LAS NO.	50 μa BV ee1	50 μa BV ee2	100 μa BV ee1	100 μa BV ee2	500 μa BV ee1	500 μa BV ee2	1 ma BV ee1	1 ma BV ee2	2.5 ma BV ee1	2.5 ma BV ee2	5 ma BV ee1	5 ma BV ee2	10 ma BV ee1	10 ma BV ee2
25°C														
12		21	21.3	21	21.7	21.5	21.7	21	21	20	20	18.8	19.2	17.8
13		22.5		23		22.5		22		21	19.6	20	18.2	18.4
14	24.5	24	24.5	24	24	22.5	23	21	21.3	18.4	19.6	16.2	18	15
15	24.5	24	24.5	23.8	24.2	22	23.5	20.5	22	17.4	20.5	15.2	19	14
16		23.5		23.5	23.5	22.5	22.5	21.5	21	19.4	19.4	17.8	18	16.6
85°C														
12		20.5	21	20.5	21.5	21		21		20.5		19.6		18.8
13		22	22	22.5	22	22.5	21.5	22	20	21.5	18.8	20	17.8	18.4
14	23.5	23	23.5	23	23	22	22	21	20.5	18.6	18.8	16.8	17.2	15.4
15	23.5	23	23.5	22.7	23.5	21.5	22.5	20	21	17.8	19.6	15.8	18.2	14.8
16		22.5		22.5	22.5	22	22	21	20	19.2	18.4	18	17.8	17.2

* A very large number of BV_{ee} measurements were performed, of which the above is a typical sampling. (Run #173, Type 3)

TABLE 5b

BV_{ee} - TEST RESULTS

I_s

LAS NO.	100 μa BV ee1	100 μa BV ee2	10 ma BV ee1	10 ma BV ee2
26°C				
5*	20.5		18.5	17.5
6	22.5		18	17.5
7	22.5		17.5	17
8	22		17.5	16.5
10	22.5		18.5	
-10°C				
5	21.3		18.4	18
6	23.5		18.4	18.2
7	23.5		18.2	17.4
8	23		18	17.6
10	23.5		18.8	18

* Run #168 - Type 2

g. t_r, t_f - Rise and Fall Time

The speed of response is determined by the length of the turn-on and turn-off times of the LAS. As mentioned in section 2.6.4, the GaAs diode has response times in the nanosecond range. The observed rise and fall times of the LAS are in the microsecond range. The LAS speed limitation is therefore imposed by the DET. The t_f values increased directly with load and showed a marked increase at elevated temperatures. Table 6 shows t_r and t_f values for several LAS units. The load and temperature dependence of the fall times are shown in Figures 41a and 41b, respectively.

TABLE 6

RESPONSE TIME TEST RESULTS

LAS NO.	t_r μ sec	t_f μ sec
1*	1.0	7.0
2	1.0	7.0
3	1.0	4.4
5	1.2	6.0
6	1.1	8.0
7	1.3	8.0
8	1.3	10.0
9	1.2	6.6
10	1.6	8.0
11	1.1	7.0
12	1.1	6.4
27	1.1	6.5
28	1.2	5.0
30	1.0	8.5
35	1.2	5.4

* Run #168 Type 2

7**	1.8	9.0
10	1.8	7.0
11	2.0	7.0
12	1.8	12.0
13	2.0	9.0
14	1.8	11.0
15	2.0	11.0
16	2.0	11.0
32	1.7	7.0
40	1.9	9.0

** Run #173 Type 3

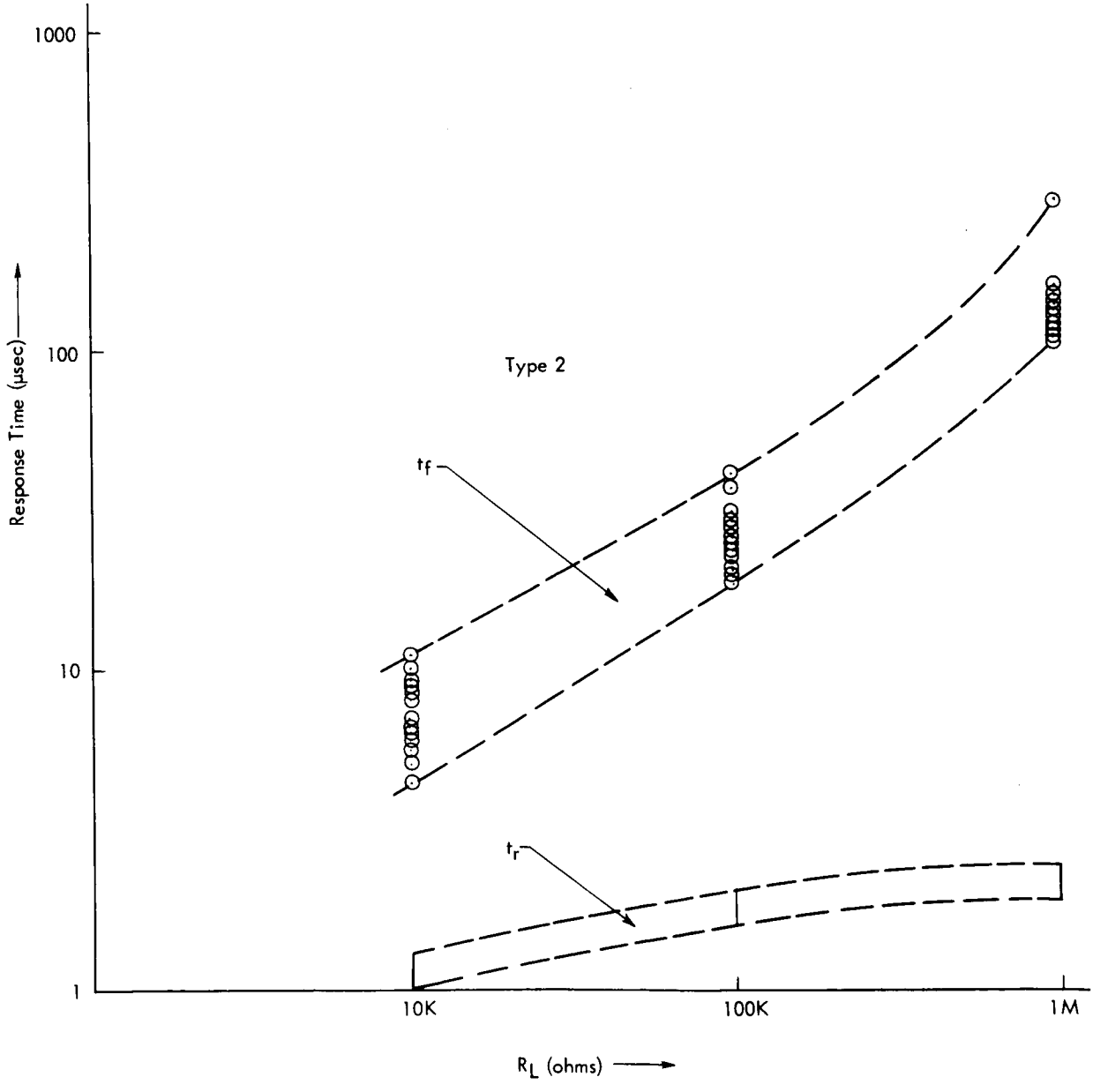


FIGURE 41 a - DEPENDENCE OF RESPONSE TIMES ON LOAD

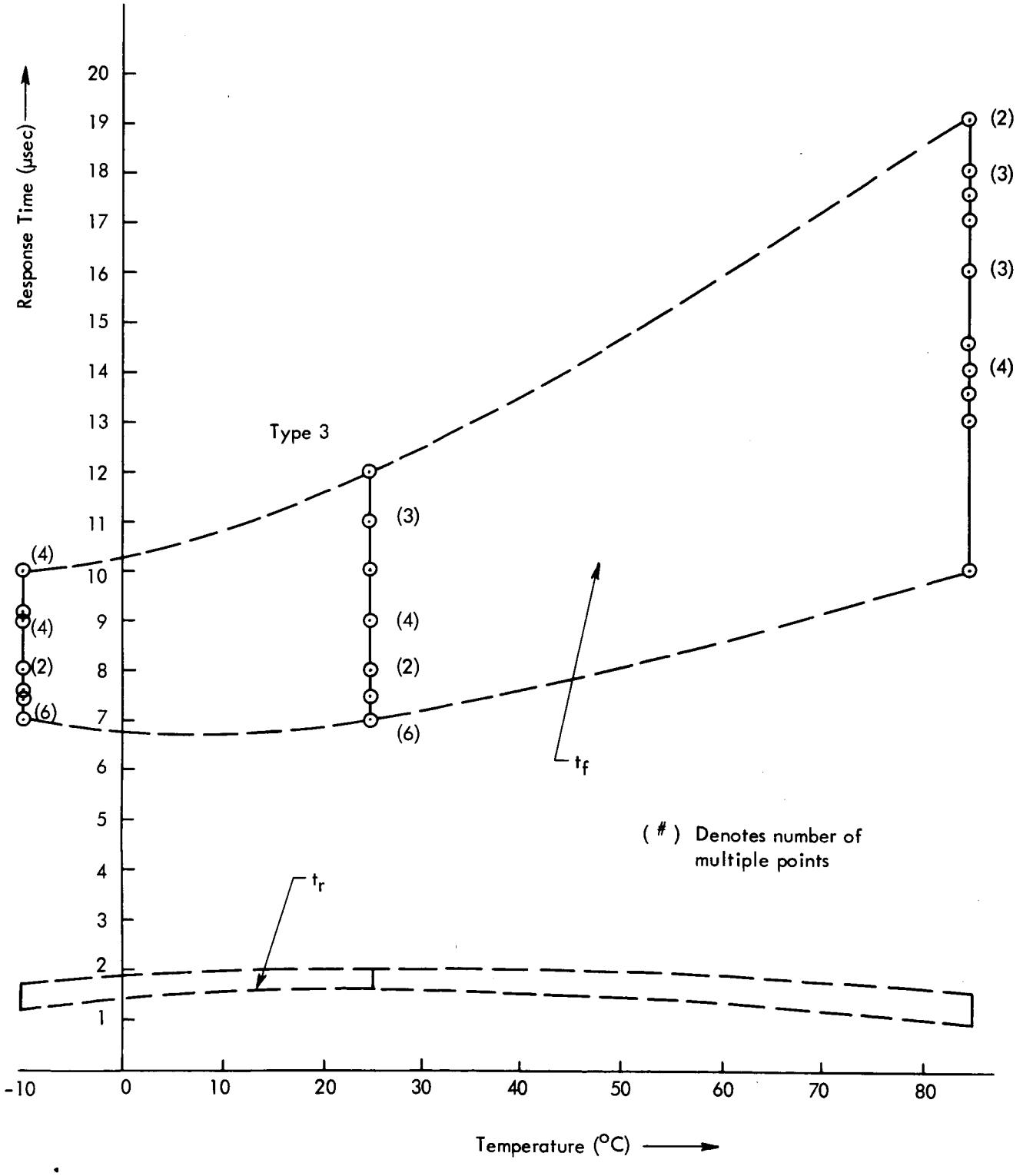


FIGURE 41 b - DEPENDENCE OF RESPONSE TIMES ON TEMPERATURE

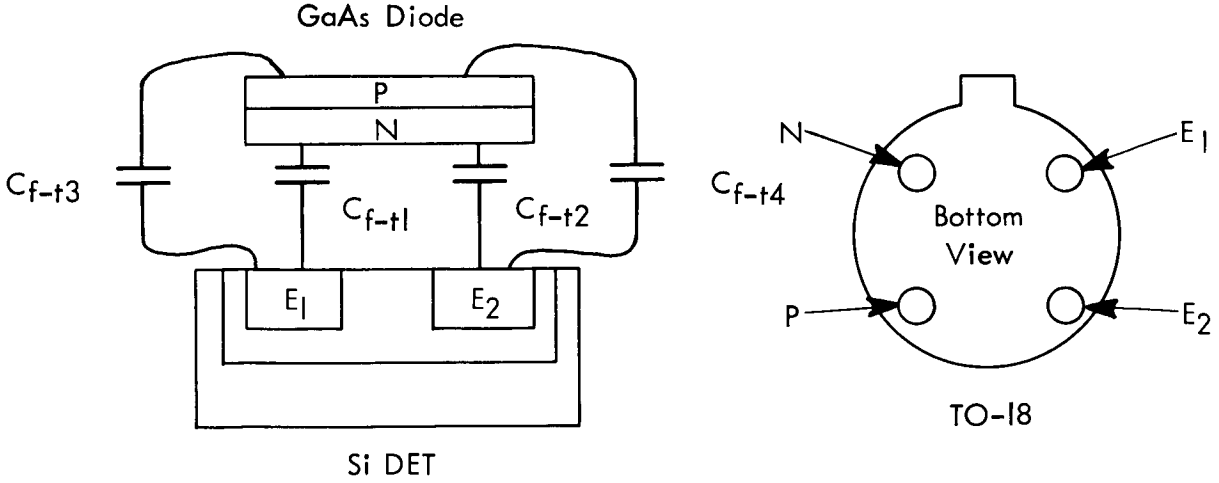
h. C_{f-t} - Feed-through Capacitance

One way to evaluate the LAS package was to measure the capacitance between either emitters and the P or the N side of the diode. The definitions and values of the different capacitances measured are shown in Table 7. The tests were done at 1 MC. The observed C_{f-t} values were below 1.8 pf for all of the measured devices.

TABLE 7

LAS* #	C_{f-t_1} pf	C_{f-t_2} pf	C_{f-t_3} pf	C_{f-t_4} pf
45	1.51	1.47	1.69	1.69
46	1.38	1.35	1.61	1.61
47	1.49	1.45	1.65	1.70
48	1.51	1.48	1.78	1.76
49	1.43	1.38	1.72	1.76

* Run #173



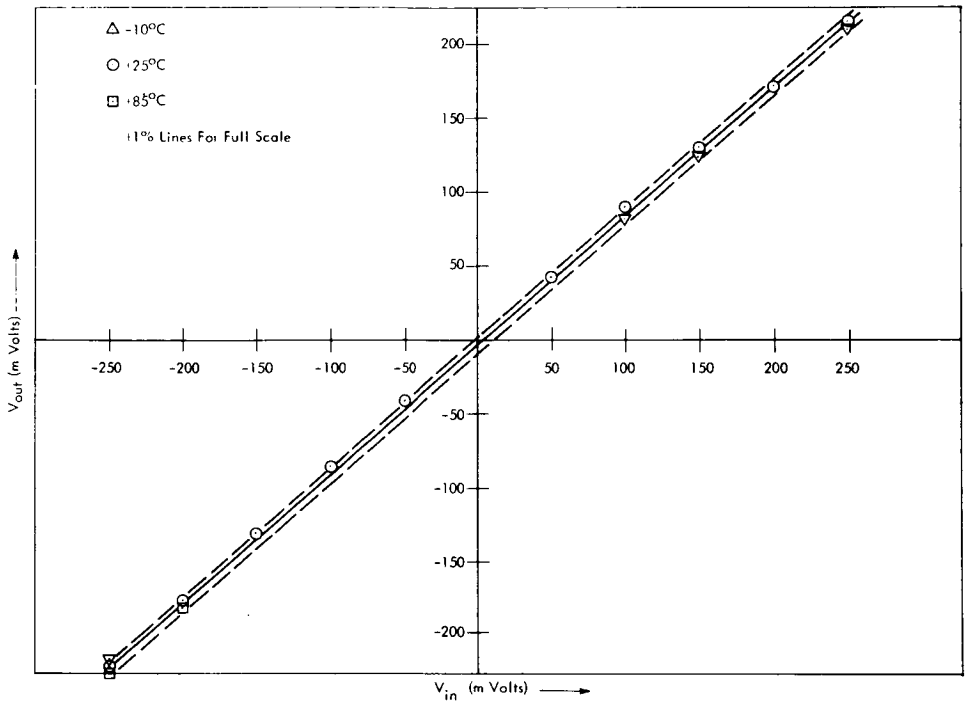


FIGURE 42b - ERROR BAND TEST RESULTS, ± 250 mv

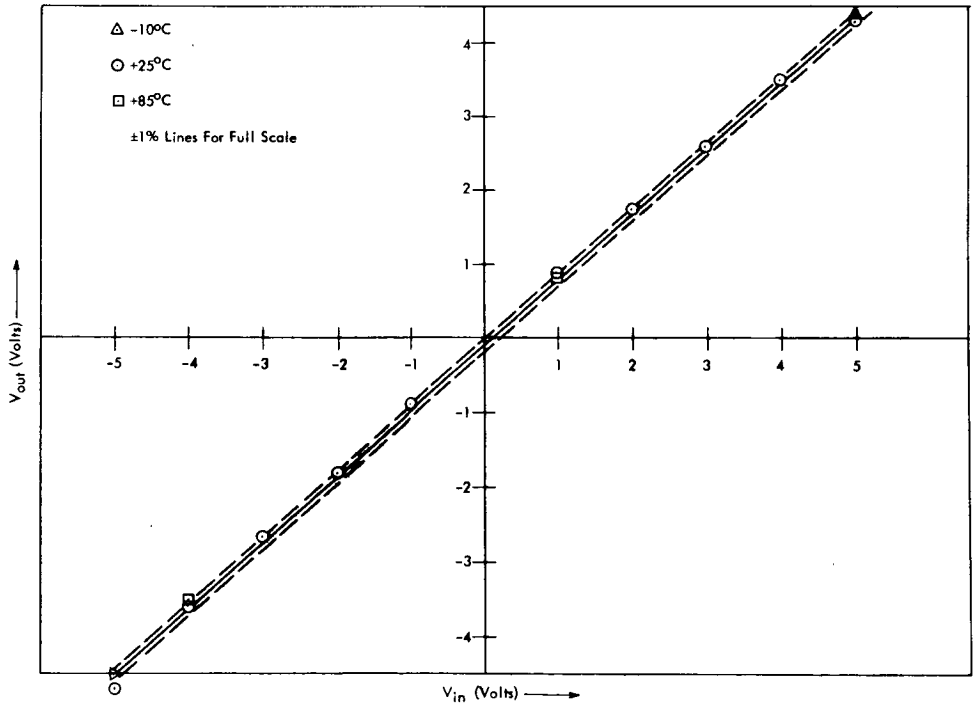


FIGURE 42c - ERROR BAND TEST RESULTS, ±5 v

i. Error Band

The purpose of this measurement was to show the combined effects of error arising from linearity, resolution, zero shift, sensitivity shift, offset, noise level, etc., between input and output of the LAS. The results of an Error Band Test are shown for a representative unit on Figure 42. For the ± 250 mv and ± 5 volt ranges, the error is within ± 1% of full scale when subjected to environmental conditions, as compared to the room temperature static condition. In the ± 5 mv range, the apparent error (seemingly greater than ± 1% but less than ± 2.5%) is due to the inaccuracy inherent in reading the trace on an oscilloscope display under severe noise conditions.

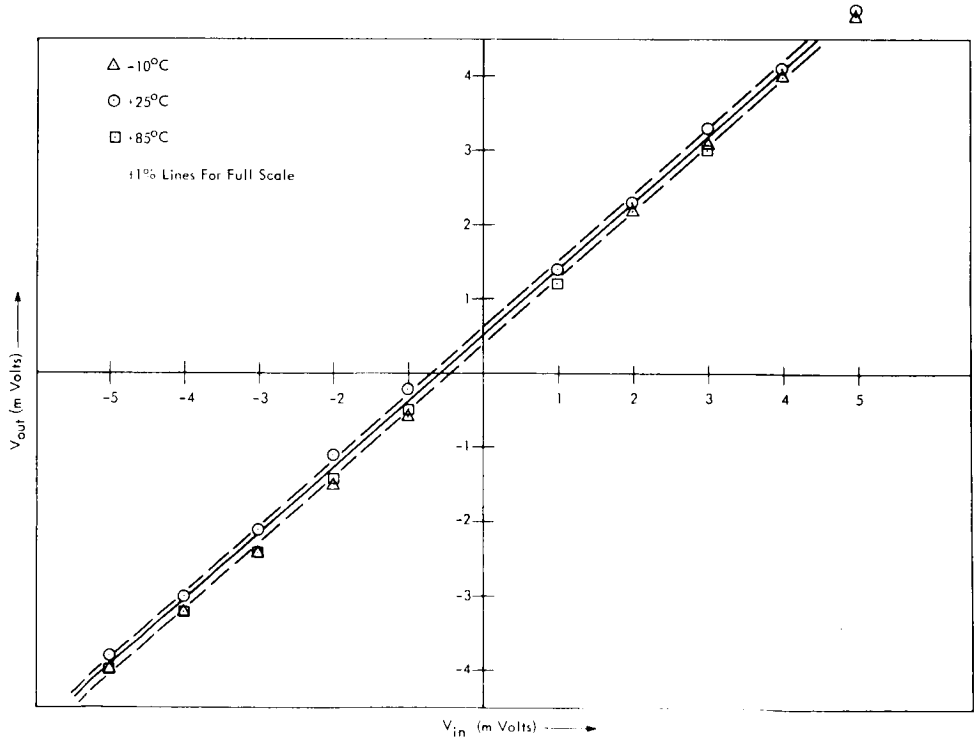


FIGURE 42a - ERROR BAND TEST RESULTS, ±5 mv

j. Mechanical Evaluation

1. Two LAS units were subjected to an Impact Shock Test. The units were rigidly mounted in a fixture which was attached to a shock table. Each unit was subjected to impact shock of 3000 G's ± 10% for a duration of 0.2 millisec ± 0.05 millisec. Six blows were applied in each of the following directions:
    a. Parallel to the leads, toward the top of the device.
    b. Parallel to the leads, toward the bottom of the device.
    c. Perpendicular to the leads.
2. Two LAS units were subjected to 20,000 G's Constant Acceleration Test for three minutes. Direction of acceleration was toward the top of the unit.
3. Two more LAS units were given a sinusoidal vibration at a 0.5 inch DA, 10 to 45 cps and 50 G's constant peak acceleration, 46 to 2000 cps. Frequency traversed 10 to 2000, back to 10 cps in four minutes, with four complete frequency sweeps in each of three mutually perpendicular axes. Total vibration time was 48 minutes.

A unit was considered to be a failure if there was any evidence of mechanical damage or if there was any change in electrical characteristics. No such failures were observed.

On the basis of the test results, the following quantities reached their "design objective" values:

R_{ee} $\leq 20\ \Omega$

R_1 $\geq 100\ M\ \Omega$

R_2 $\geq 100\ M\ \Omega$

V_o	$\leq 50\ \mu v$
I_o	to meet all specifications
I_M	$\geq \pm 10$ ma

The voltage overload without switch damage (BV_{ee}) was below the value specified as a design objective, though Type 4 units were made with greater than $\pm$35 volt values.

SECTION 5 - LIFE TESTS

To determine the reliability of the LAS, a number of life tests were performed. DET and light sources were tested extensively.

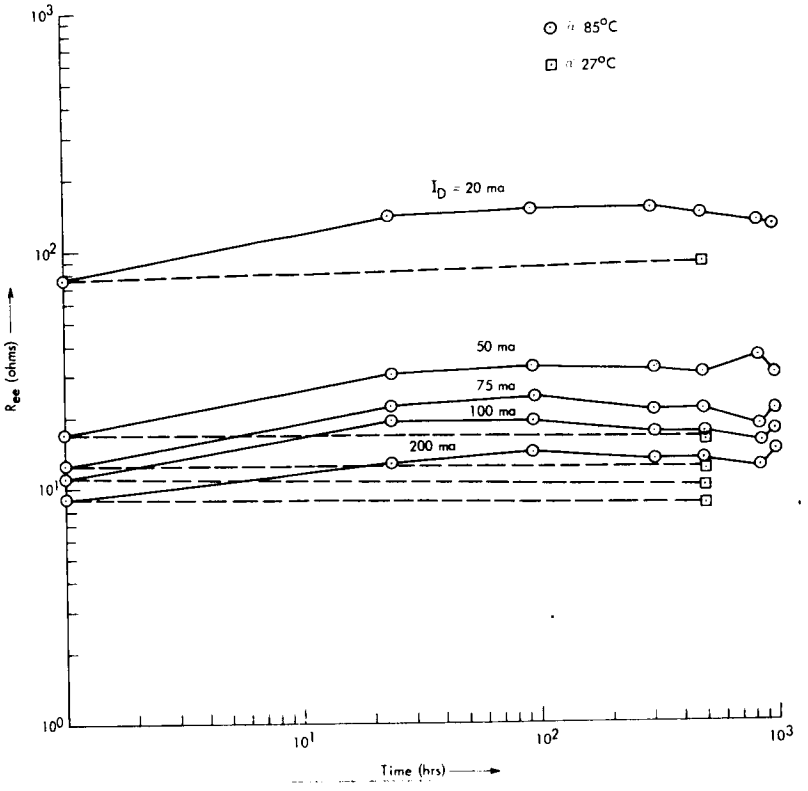
5.1 LAS SHELF LIFE TEST

Five devices were put on 85°C shelf life test. The values of R_{ee}, t_f, and BV_{ee} were measured at various times up to 1000 hours. In addition, two of the units were removed after 504 hours from the high temperature environment, cooled to room temperature, measured, and replaced into the 85°C environment. After 1008 hours at 85°C, the five devices were cooled to room temperature and remeasured. A subsequent measurement of R_{ee}, t_f, and BV_{ee} took place at - 10°C. The results indicated that the values of R_{ee} and t_f increased initially and leveled out at longer times (see Figure 43). When brought back to room temperature (26°C) after the 1008 hours 85°C shelf life test, the values of R_{ee} and t_f were very close to their initial values at 0 hour at 26°C. The emitter to emitter breakdown, shown in Table 8, exhibited very little change throughout the test.

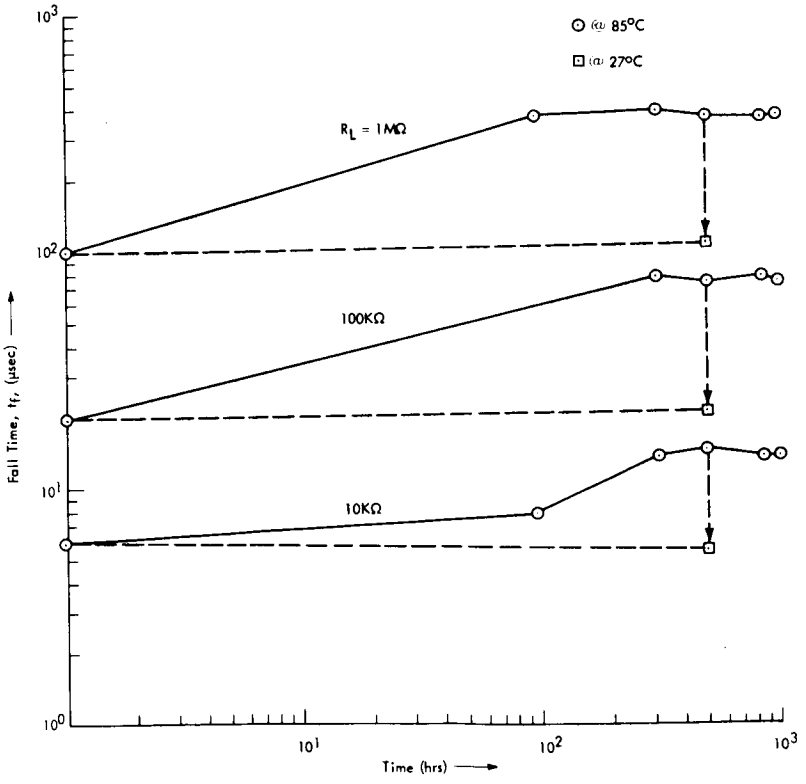
TABLE 8

BV_{ee} VARIATION WITH TIME AT 85°C

Time (hours)	#168-005				#006				#007				#008				#010			
	100 μa		10 ma		100 μa		10 ma		100 μa		10 ma		100 μa		10 ma		100 μa		10 ma	
	E_1	E_2	E_1	E_2	E_1	E_2	E_1	E_2	E_1	E_2	E_1	E_2	E_1	E_2	E_1	E_2	E_1	E_2	E_1	E_2
0	20.5	20.5	17.5	18.5	22.5	22.5	17.5	18	22.5	22.5	17	17.5	22	22	16.5	17.5	22.5	22.5	18.5	18.5
24																				
96	20	19.5	16.5	17.5	21	21	16	17	21.5	21	16	17	21	20.5	15.5	16	21	21.5	17	17.5
312	20.5	19.5	16.5	18	21	20	16	17.3	21.5	20	15.5	17.3	20.5	19	15.3	16.7	22	20.5	15.8	18
504	20	19.4	16.6	18	21.5	21	16.4	16.8	21.5	21	16.2	17.6	21	20	15.6	16.6	21	20	17	17.6
504 @27°C	21	21	17.2	18	23	23	17.4	17.8												
864	20.5	19.6	16.4	17.6	21.5	21.5	16.2	17	22	21.5	16	17	21	21	15.4	16.2	22	21	16.6	17.6
1008	20.5	19.6	17.6	16.4	21.5	21.5	17	16.2	21.5	21.5	17	16	21	21	16.2	15.6	21.5	20.5	17.4	16.6
1008 @26°C	21	21	18.2	17.6	23	23	18.2	17.8	23	23	18	17.2	22.5	22.5	17.6	17.2	23	23	18.6	17.6
@-10°C	21.3	21.3	18.4	18	23.5	23.5	18.4	18.2	23.5	23.5	18.2	17.4	23	23	18	17.6	23.5	23.5	18.8	18



a - R_{ee} vs. hours



b - t_f vs. hours

FIGURE 43 - SHELF LIFE-TEST RESULTS AT 85°C

5.2 LAS LOAD LIFE TEST A

Two switches (from Run No. 168, units 5 and 6) were tested under a load condition at room temperature, as shown in Figure 44.

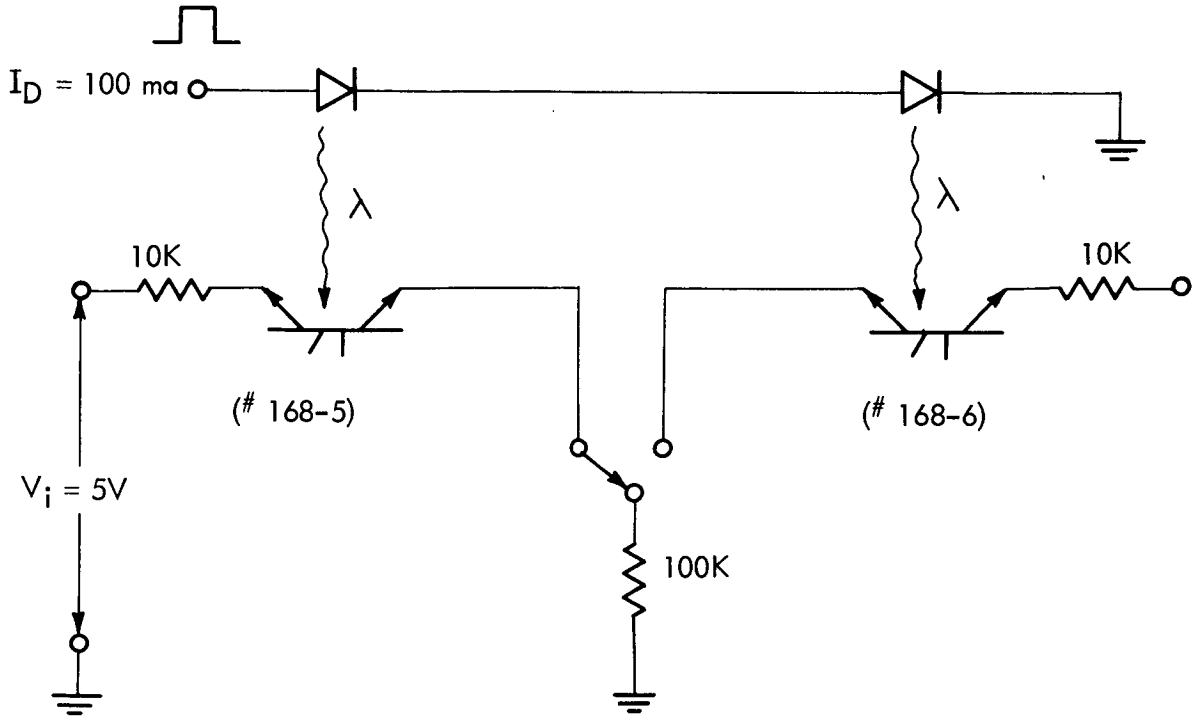


FIGURE 44 - TEST CIRCUIT FOR LOAD LIFE-TEST-A

It is apparent that LAS (No. 168-5) has current flowing through both its diode and DET, whereas LAS (No. 168-6) has current flowing only through its diode. The purpose in using this arrangement was to detect any degradation of the DET. The results, shown in Figure 45, suggest a possible degradation in both the DET and the diode. The more severe increase in ON impedance of unit (No. 168-5) is attributed to changes in both the detector and source, while the lesser change in R_{ee} of unit (No. 168-6) is attributed to degradation of the diode, since the DET was "unloaded" during the 1000 hours.

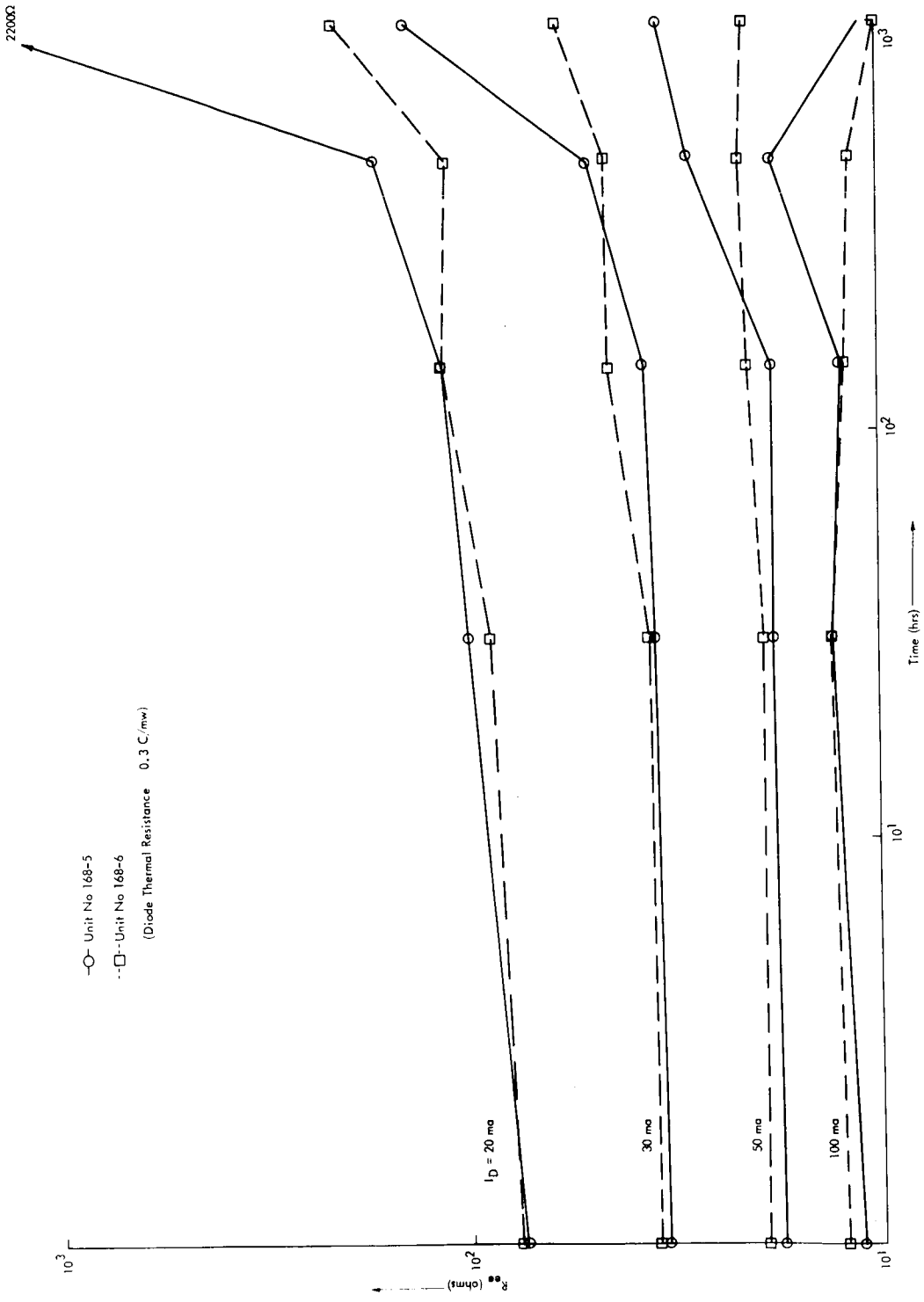


FIGURE 45 - LOAD LIFE-TEST-A RESULTS

5.3 LAS LOAD LIFE TEST B

To further study the degradation problem, thirteen devices (Run No. 173) were put on a load life test at 65°C. This test was conducted under DC conditions with 50 ma drive on the diodes and 10 volts input on the DET, with R_L = 10 K ohms. The R_{ee} values of the switches were monitored during the test. After 593 hours, two switches showed considerable increase in ON impedance. A third switch, initially very high, remained unchanged. The remaining switches increased initially but showed a tendency to level off after 330 hours, as shown in Figure 46.

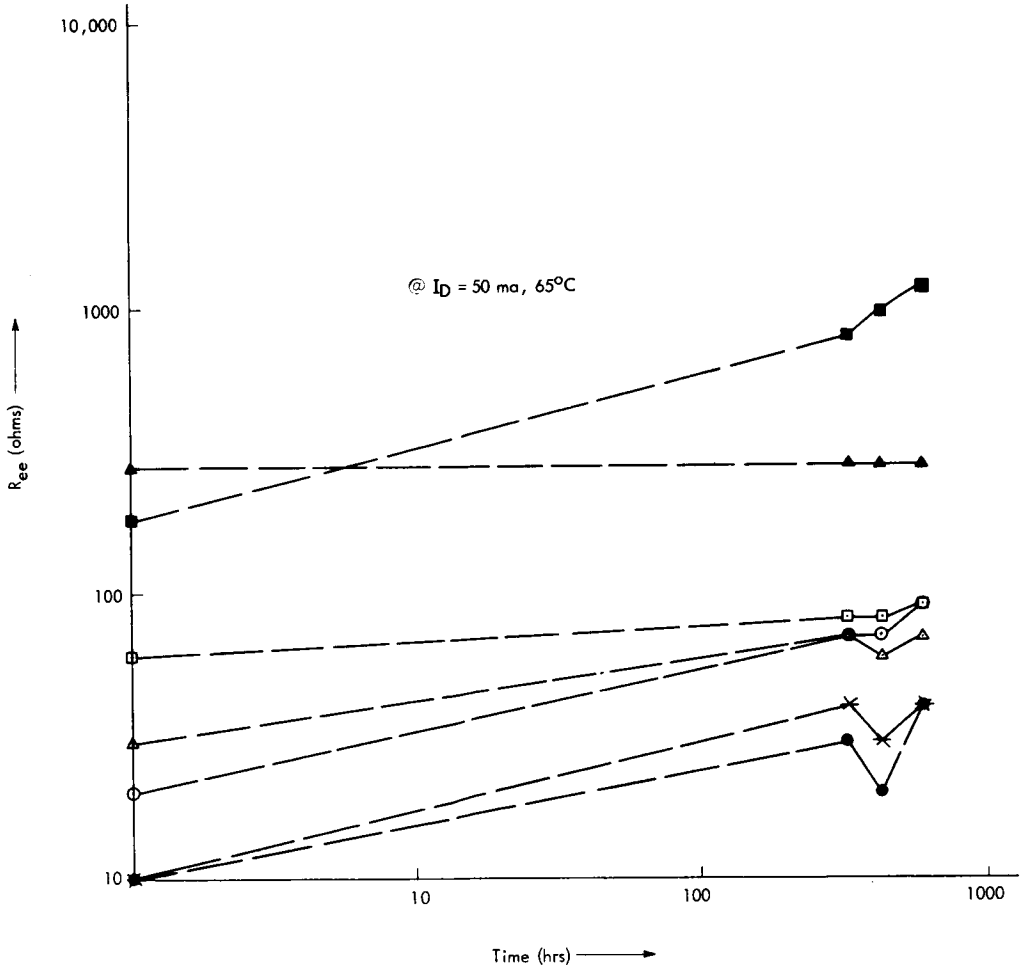


FIGURE 46 - LOAD LIFE-TEST-B RESULTS

5.4 DIODE LIFE TESTS

Several GaAs diodes were tested under different conditions. The diodes were of different sizes (5x5 mils sq., 5x10 mils sq., 10x10 units sq.), had epoxy, selenium, or no coating, and were aged at current drives ranging from 30 ma - 100 ma dc at room temperature and at 65^{o}C. The relative light output was monitored. The trends of both temperature measurements were similar and are summarized in Table 9 and below:

a. Higher aging currents resulted in higher degradation.

b. Under identical conditions, degradation was far more serious with selenium coating than with epoxy.

c. Degradation was directly proportional to current density.

d. At high aging currents, epoxy coated units showed less degradation than uncoated units.

e. Diodes, aged at currents in the vicinity of 30 ma after 1700 hours, showed less than 4% degradation.

TABLE 9

DIODE LIFE TEST RESULTS

Diode No.	Size Mils	Coat	Aging Condition DC ma	Read Condition DC ma	Test Time Hours	Degradation
41B-143A	5x5	Epoxy	30	30	1710	2.17
41B-144D	5x10	Air	30	30	1710	3.5
41B-5	10x10	Selenium	35	50	980	98
36B-11	10x10	Epoxy	35	50	1902	18.2
A	10x10	Epoxy	50	50	1000	5.0
B	10x10	Epoxy	50	50	1000	5.7
C	10x10	Epoxy	50	50	1000	9.1
D	10x10	Epoxy	50	50	1000	16.0
32B-28	10x10	Epoxy	70	70	403	6.7
36A-11	10x10	Epoxy	70	70	403	12.1
36A-12	10x10	Epoxy	70	70	403	13.5
36A-13	10x10	Epoxy	70	70	403	11.1
36A-17	10x10	Epoxy	70	70	403	14.6
36A-20	10x10	Epoxy	70	70	403	16.7
41B-3B	5x10	Selenium	70	70	403	37.8
41B-6A	5x5	Selenium	70	70	403	69.3
41B-135A	5x5	Epoxy	100	100	1710	48.6

SECTION 6 - CONCLUSIONS AND RECOMMENDATIONS

The results of this study lead to several conclusions and recommendations for further development. Feasibility for the light actuated switch has been ascertained, but the program duration has not permitted much device engineering optimization.

6.1 CONCLUSIONS

a. An electroluminescent GaAs diode, with a high external efficiency and low forward voltage, has been developed.

b. Of the four types of silicon DET detectors that have been studied, the NPN, single-diffused configuration had performance characteristics which satisfied most of the JPL specifications.

c. Agreement between a first order theory (Ebers and Moll) and experiment has been found for some parameters of the DET detectors.

d. The epoxy between the light source and DET detector provides a temporary but not necessarily optimized solution to the light coupling problem.

e. The characteristics of the LAS have shown some degradation when tested at elevated temperatures under load conditions. The degradation is due partly to the GaAs diode degradation and partly to the silicon DET degradation. The exact nature of the degradation mechanism is not understood at this time.

6.2 RECOMMENDATIONS

To optimize the performance of the LAS, a continued study program should be addressed to the following problem areas:

a. The LAS package should be redesigned for more efficient heat dissipation and light coupling.

b. Investigate glassing and high refractive ceramics as a substitute for, or in combination with, the epoxy photon coupling medium.

c. Identify the degradation mechanisms by separating the contributions from the GaAs light diode and the silicon DET detector.

d. Using the latch drive scheme, described in Section 7, fabricate a multi-gate, monolithic multiplexor. Such an approach would offer high reliability with a minimum of components.

SECTION 7 - LAS DRIVE SCHEME

To use the LAS for the gates of an electronic gating system, a compatible drives scheme was proposed. Figure 47 illustrates a "latching" circuit which can be controlled externally by clock signals or other means. The control currents involved in the turn-on and turn-off are in the order of microamps. For effective latching, the current gain of the diode-transistor combination must be equal to or greater than unity.

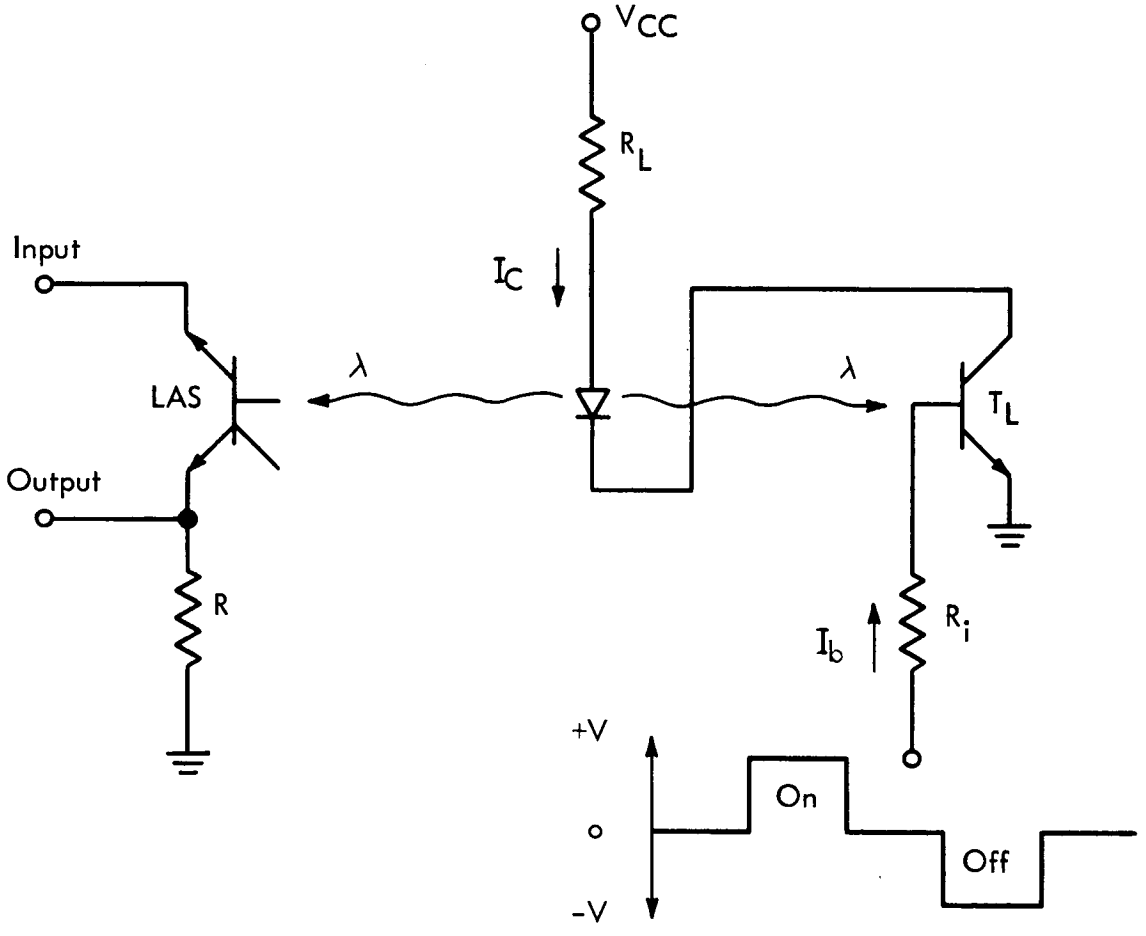


FIGURE 47 - LATCH DRIVE SCHEME

To discuss the operation of the latch, an NPN drive transistor, T_L, is assumed. With $I_b = 0$, the transistor is OFF if no current is flowing in the circuit. Application of a forward bias to the emitter-base junction and a $V_{cc} > 0$ will turn the transistor ON, allowing current I_c to flow. If I_c is large enough, such that the light emitted from the diode will create an equivalent base drive sufficient to hold the transistor ON, removal of I_b, that is, the external forward bias on the emitter base junction, will not affect the current flow, and the circuit is considered to be "latched." To "unlatch," one has to bring the base to ground level. In principle, while the current is flowing through the diode, not only the transistor T_L, but also the LAS is illuminated, thus turned ON. On the other hand, when $I_c \sim 0$, the switch is OFF.

Several latches were made from different runs, incorporating Type 1 and Type 2 transistors. These latches were carefully studied in order to uniquely determine the necessary conditions for "latching." The minimum values of V_{cc} and I_b were determined such that latching still occurred. These are summarized in Table 10. Also shown are R_{ce} values, where determined, corresponding to the proper diode currents. In addition to the above, the $I_c - V_c$ characteristics, with I_b as a parameter, were determined for the drive transistor (T_L), and with their use, I_b vs. I_c curves were plotted for a Type I and a Type 2 transistor. (See Figures 48 and 49). Superimposed on these figures are the I_{b1} (effective base current generated by light) vs. I_c (current through the diode) curves. The points of intersection establish the values of I_b, emitter-base forward bias, necessary to initate and sustain latching. The values found from these curves are near the experimentally observed values, and the analysis seems adequate in first order approximation. For Type 1, the following was found:

	Experimental Latching Point	Calculated Latching Point
I_b	13 μa	15 μa
I_c	50 ma	39 ma
V_{cc}	5.5 v	3.5 volts

Thus, an approximate manner of predicting the condition for "latching" was established, and the ability of the latch to drive a switch was demonstrated.

The advantages of this drive circuit are apparent even more in the case of an integrated package. These are:

1. Compatibility of drive transistor and switch transistor in monolithic form.
2. Minimized power requirement.
3. Minimum number of components.
4. Increased reliability through decreased number of necessary interconnections.

TABLE 10

LATCHING CONDITIONS

Device	V_{cc} volts	I_B μa	β_n @ I_B = 0.2 ma	I_c ma	R_{LE} Ω
#110-74	5.5	13	1400	50	8
(Type 1)	6.0	12	1400	60	6
	7.0	9	1400	80	6
#110-73	7.5	20	1200	70	9
(Type 1)	10.0	16	1200	115	8
#110-70	12.0	7	980	140	8
(Type 1)	14.0	6	980	170	8
#110-72	17.0	21	500	205	8
(Type 1)	19.0	19	500	230	8
#181-10	9.0	20	350	90	-
(Type 2)	10.0	20	350	102	-
	12.0	20	350	140	-
#181-18	12	26	240	120	14
(Type 2)	13	26	240	140	13.5

V_{cc} = Power supply voltage

I_B = Emitter base forward bias necessary to initiate latching

β_n = forward β of T_1

I_c = current flowing through T_1 when latched

R_{CE} = collector-emitter impedance measured as a function of I_D = (diode current)

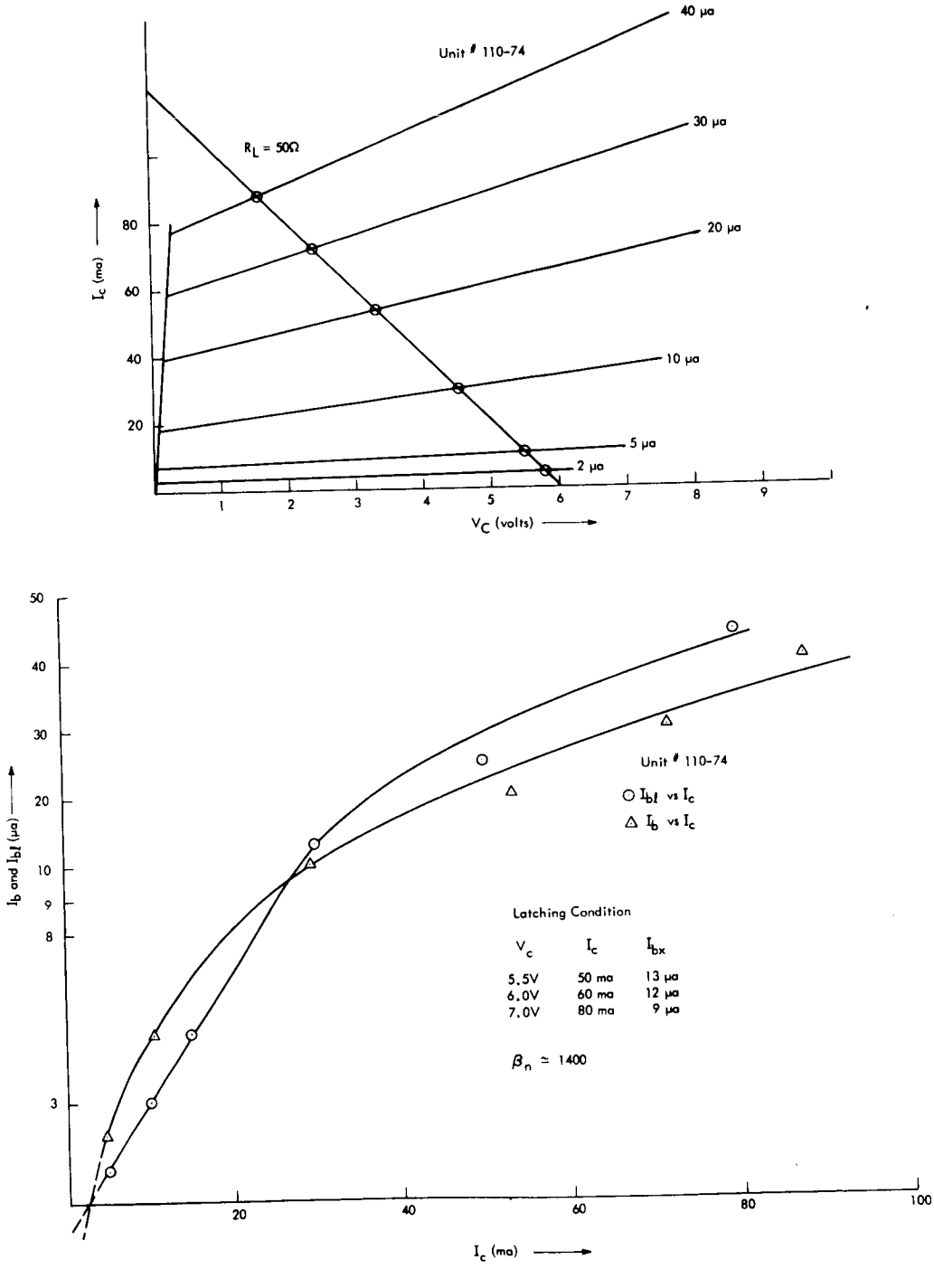
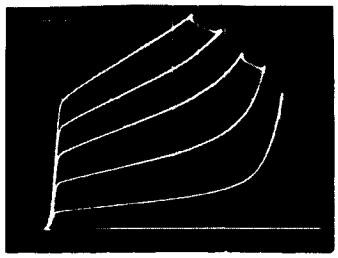
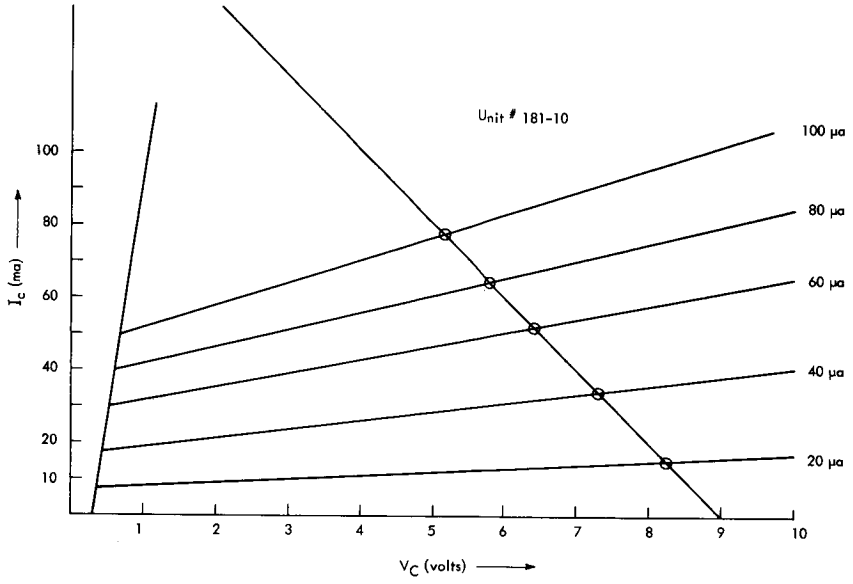


FIGURE 48 - LATCH CHARACTERISTICS (TYPE 1)





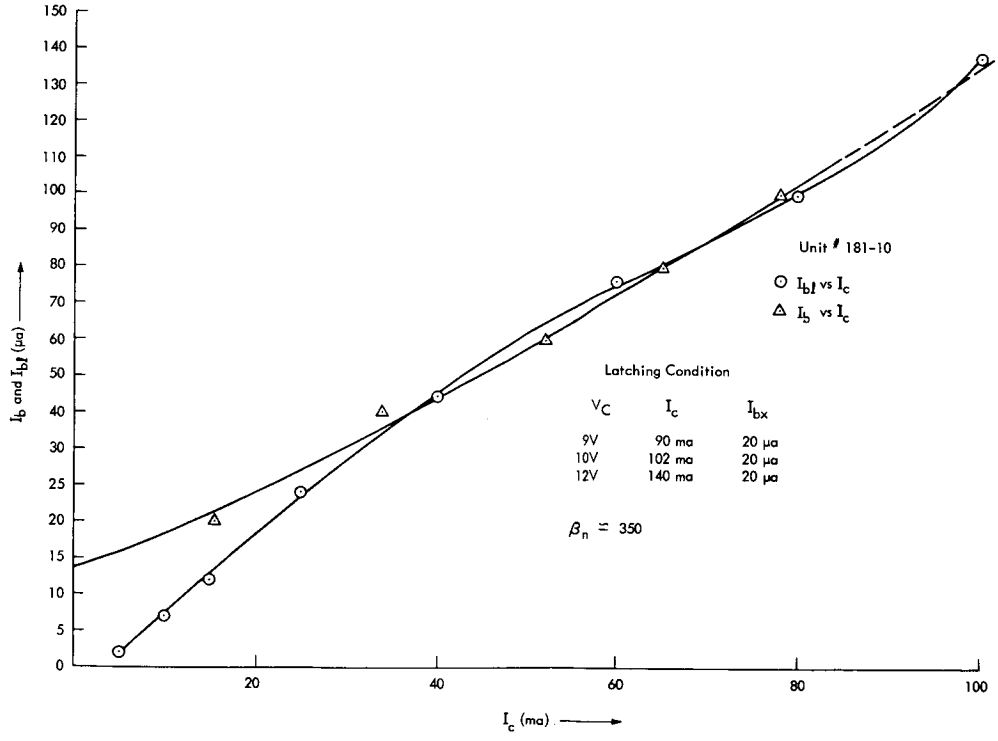


FIGURE 49 - LATCH CHARACTERISTICS (TYPE 2)

SECTION 8 - PERSONNEL

The following scientists and engineers have participated in the LAS program in various supervisory and technical capacities. The project leadership responsibility was shared by R. M. Folsom, W. A. Pieczonka and E. S. Wajda.

During the course of this development, significant contributions and technical support were obtained from the IBM Components Division, Materials and Applications groups and from Messrs. F. Kulakowski and G. H. Schmidt.

ROBERT M. FOLSOM

Academic Degrees

B. S., Engineering Physics, University of Maine 1949

Professional Interest and Experience

Mr. Folsom joined IBM in 1957 and has been engaged in the advanced development of semiconductor devices since that time. His early work included a rather extensive investigation of the effects of high-energy β radiation on germanium NPN and PNP drift transistors, with the object of utilizing these effects in transistor design. He also developed a high-speed low-storage germanium NPN mesa logic transistor that is currently in production. He is presently manager of ULD Engineering.

From 1953 to the time he joined IBM, he worked for the Diamond Ordance Fuze Laboratories on semiconductor materials processing technology and on device development. Previously, from 1950 to 1953, he worked for the National Bureau of Standards on the development of sub-miniature vacuum tubes for VT fuze applications.

Publications

"Diffusion Masking and All-Diffused Germanium NPN Mesa Transistors", 1959 IRE-PGED Electron Devices Meeting, Oct. 29-30, Washington, D. C.

"A High-Speed, Medium-Power, All-Diffused Germanium NPN Mesa Transistor", 1962 IRE International Convention, March 26-29, New York, N. Y.

"A High-Speed, Medium-Power, Triple-Diffused Germanium NPN Switching Transistor", 1962 IRE-PGED Electron Devices Meeting, Oct. 25-27, Washington, D. C.

WALDEMAR A. PIECZONKA

Academic Degrees

B. S., Mathematics and Physics,	Saskatchewan University	1953
M. S., Physics	McMaster University	1957
Ph. D., Physics,	McMaster University	1960

Professional Interests and Experience

Dr. Pieczonka joined IBM in 1960 and worked on the advanced development of medium power transistors for solid state memory applications. This included the development of a high-speed medium-power, triple-diffused germanium NPN mesa transistor and the development of a high-speed, medium-power, double diffused epitaxial silicon NPN mesa transistor that is currently in pilot-line production. He made an extensive theoretical study, backed up with experimental results, of switching transistor operation at high level injection.

Before joining IBM, he worked for three years for Canadian Westinghouse Corporation on a guided missile project. Presently, he is employed by Canadian Westinghouse Corporation.

Publications

"An Electron Spin Resonance Study of Manganese Impurity in Brucite", Can. Journal of Physics, 39, 145 (1961).

"A High-Speed, Medium-Power, All-Diffused Germanium NPN Mesa Transistor", 1962 IRE International Convention, March 26-29, New York, N. Y.

"A High-Speed, Medium-Power, Triple-Diffused Germanium NPN Switching Transistor", 1962 IRE-PGED Electron Devices Meeting, Oct. 25-27, Washington, D. C.

"Transient Response in High-Speed Transistors", N. Y. Metropolitan Area Chapter, PGED, November 15, 1962.

"GaAs-Si Photon Activated Switch" - to be published in PGED Transaction of IEEE.

PETER POLGAR

Academic Degrees

B. E. S., Electrical Engineering, Brigham Young University, 1960

M. S., Physics, Rutgers - The State University, 1963

M. S., Electrical Engineering, Completed all course requirements at Brigham Young U.

Professional Interests and Experience

Mr. Polgar joined IBM in June, 1963 and since that time participated in a development effort aimed at light emitting and detecting solid state devices. Prior to joining IBM he spent summers doing Research in Physics and Electrical Engineering at the Shell Oil Research and Development Laboratories.

He was a teaching assistant from 1959 - 1963 at Brigham Young University and Rutgers State University.

Publication

"GaAs-Si Photon Activated Switch" - to be published in PGED Transaction of IEEE.

MAURICE M. ROY

Academic Degrees

Courses in Physics and Math - Marist College

Professional Interests and Experience

Since joining IBM in 1956, Mr. Roy has been engaged in various phases of semiconductor device development. He has been instrumental in developing key fabrication processes for the Ge drift transistor, and Light Actuated Switch.

Publications

"A High-Speed Mesa Transistor," - IBM Technical Publication - (1962).

"GaAs-Si Photon Activated Switch" - to be published in PGED Transactions of IEEE.

EDWARD S. WAJDA

Academic Degrees

B. S., Physics, Union College	1945
M. S., Physics, Cornell University	1948
Ph.D., Physics, Rensselaer Polytechnic Institute	1953

Professional Interests and Experience

Dr. Wajda is manager of Exploratory Device Development in the IBM Components Division. He has done extensive research work in anisotropic diffusion phenomena in metals and thin films for microelectronic applications. For two years prior to his joining IBM in 1955, Dr. Wajda was an Assistant Professor of Physics at Union College. His work in IBM has consisted of extensive research and development of semiconductor materials and processes. Dr. Wajda has also worked on instrumentation development and analytical instrument analysis. He is a member of Sigma Xi.

Publications

"Self Diffusion in Zinc" - Acta Metallurgica - (1953).

"Grain Boundary Self Diffusion in Zinc" - Acta Metallurgica - (1954).

"An Automatic Counter" - Nucleonics - (1952).

"Cadmium Grain Boundary and Lattice Diffusion" - Acta Metallurgica - (1955).

"Calculation of Entropies of Lattice Defects" - Phys. Rev. - (1955).

"Silicon Epitaxial Growth" - IBM Journal - (1960).

"Silicon PN Layer Formation by Vapor Growth" - Vol 5 - Properties of Elemental Compound Semiconductors - (1960).

"Status of Vapor Growth of Silicon" - Vol 12 - Metallurgy of Elemental and Compound Semiconductors (1961).

"Vapor Growth of Silicon" - Art and Science of Crystals - (1963).

"Thin Film Circuits" - Microelectronics - (1963).

"Vapor Growth of Semiconductors" - AIME Conf. Proceedings (Cleveland) - (1963).

"Gallium Diffusion in Silicon" - Applied Physics Letters - (1964).

TSU-HSING YEH

Academic Degrees

B. S., Mechanical Engineering, National Taiwan University	1952
M. S., Metallurgical Engineering, Notre Dame	1955
PhD., Solid-State Science and Technology, University at Syracuse	1958

Professional Interests and Experience

Dr. Yeh joined IBM in 1958 and has since that time worked on fundamental diffusion phenomenon is silicon and in gallium-arsenide and in developing new diffusion processes and technology.

Publications

"Relations between the Notch Tensile Strength of Cylindrical and Prismatic Specimens of Titanium Alloys and Heat-Treated Steels", by G. Sachs, J. G. Sessler, R. F. Pray and T. H. Yeh, Journal of Basic Engineering (Transactions of the ASME) p. 401-410, June 1960.

"The Decomposition of Austenite in 4340 Steel during Cooling" by E. P. Klier and T. H. Yeh, presented in October 18, 1960, Philadelphia Meeting of American Society for Metals.

"Diffusion of Boron in Silicon" by T. H. Yeh and W. J. Armstrong, Journal of Electrochemical Society, V. 108, p. 63c, 1961.

"Diffusion of Phosphorus in Silicon" by T. H. Yeh, Bulletin of the American Phys. Society, Series III, Vol. 7, No. 4, p. 332, April, 1962.

"Thermal Oxidation of Silicon" by T. H. Yeh, J. Appl. Phys., V. 33, p. 2849, (1962).

"Surface Masking in GaAs during Diffusion" by T. H. Yeh, J. Electrochemical Society, V. 110, p. 341 (1963).

"Junction Delineation in GaAs" by T. H. Yeh and A. E. Blakeslee, J. of Electrochemical Society, V. 110, p. 1018 (1963).

"Diffusion of Sulfur, Selenium, and Tellurium in GaAs" by T. H. Yeh, Journal of Electrochemical Society, V. 111, p. 253 (1964).

"GaAs-Si Photon Activated Switch" - to be published in PGED Transaction of IEEE.

REFERENCES

1. R. L. Bright, AIEE Transactions, 74, Part I, March (1955).
2. B. Mitchell and B. Bell, Solid-State Design, 3, Oct. (1962).
3. M. I. Nathan, et al, Appl. Phys. Letters, 62 (1962).
   R. N. Hall, et al, Phys. Rev. Letters, 9 (1962).
4. R. N. Hall, Proc. Inst. Elect. Eng.,106B, 983 (1960).
   J. Black, H. Lockwood and S. Mayburg, J. Appl. Phys., 34, 178 (1963).
   M. I. Nathan and G. Burns, Appl. Phys. Letters 1, 89 (1962).
   F. L. Gleener,et al, Phys. Rev. Letters 10, 472 (1963).
   G. Lucovsky and C. J. Reeper, Appl. Phys. Letters 3, 71 (1963).
5. R. Braunstein, J. I. Pankov and H. Nelson, Appl. Phys. Letters 3, 31 (1963).
   I. Kudman and T. Seidel, J. of Appl. Phys., 33, 771 (1962).
   W. Spitzer and J. Whelan, Phys. Rev.,114, 59 (1959).
   W. J. Turner and W. E. Reese, J. of Appl. Phys., 35, 350 (1964).
6. G. Cheroff, C. Lanza, and S. Triebwasser (to be published).
7. A. E. Michel, E. J. Walker and M. I. Nathan, IBM Journal, 7, 70 (1963).
8. Ebers, J. J. and Moll, J. L., Proc, IRE, 42, 1761 (1954).
9. Miller, S. L., Phys., 105, 1246 (1957).

APPENDICES

APPENDIX A - LIGHT ACTUATED SWITCH TEST PROCEDURE

The integrated switches were tested to the following procedure and conditions. The LAS parameter value limits are given in Table A-1, and a listing of the specific test equipment used is given in Table A-2.

TABLE A-1

Parameter	Minimum	Maximum	Unit
R_1	100 M		Ω
R_{ON}		20	Ω
R_2	100 M		Ω
V_O		± 50 μ	v
I_o	compatible with other specs.		
R_S	20	10K	Ω
R_L	10K	1M	Ω
V_i		± 5	v
I_S		± 500μ	a
V_M	± 35		v
I_M		± 10m	a
$t_r + t_f$		20 μ (at R_L = 10K)	s
P		100m	w

Resolution: 10μv input fluctuations must be resolved

Linearity: Linearity from output to input shall be within 0.2% over full scale ranges of ± 5mv, ± 250mv, and ± 5v.

Cross Talk: For nine switches open with full inputs, the tenth switch must have output less than ± 5mv when it is closed and has zero input.

Error-Band: Linearity over the space flight temperature (-10°C to 85°C) must be within ± 1%.

TABLE A-1

(cont.)

EXPLANATION OF PARAMETERS:

R_1	Switch open dc impedance
R_{ON} or R_{ee}	Switch closed dc impedance
R_2	Switch input to ground dc impedance
V_O	Switch closed contact potential (offset voltage)
I_o	Switch open leakage current
R_S	Source impedance
R_L	Load impedance
V_i	Input signal
I_S	Switch closed current
V_M or BV_{ee}	Maximum overload voltage - same as emitter to emitter breakdown voltage
I_M	Maximum overload current
t_r	Switch rise time
t_f	Switch fall time
P	Switch closing power (dc) under pulsed condition P is average power.

TABLE A-2

TEST INSTRUMENTATION

Section	Measured or Generated Quantity	Instrument
A-1	I	Keithley 150A
A-1	V	Keithley 150A
A-2	I_D (all measurements)	E-H Research Lab. Model 132A Pulse Generator
A-2	V_i	HP233A Audio Oscillator
A-2	V	Tektronix Type 545 Oscilloscope with "O" operational amplifier plug-in unit
A-3	I	Keithley 150A
	V	e/m Regatran Semiconductor Power Supply & Tektronix Type V/Type Oscilloscope
A-4	V_o	Keithley 150A, HP425A DC Micro volt ammeter
A-7	V_I	Tektronix Type 575 Transistor Curve Tracer
A-8	V_i	e/m Regatran Semiconductor Power Supply & Tektronix Type 535 Oscilloscope with Type 53/54C dual trace plug-in unit
A-9	V_{in}	Power Designs' Model 605 Power Supply
	V_{out}	Tektronix Type 545 Oscilloscope with Type D plug-in unit

Temperature tests were performed in a Delta Series 1060-WF Temperature Chamber and in oil temperature bath.

A-1 Switch Open DC Impedance (R_1)

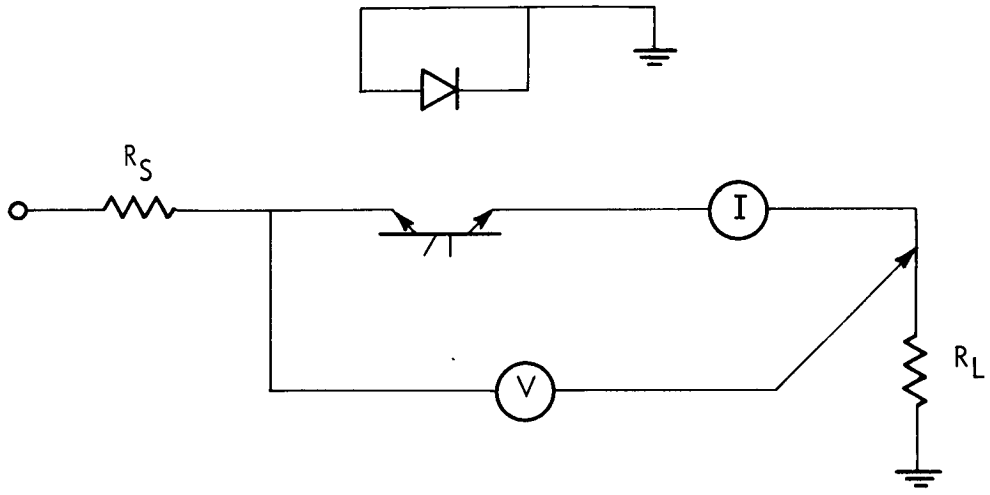
Test Conditions:

Test 1 V = $\pm$ 5 mv

Test 2 V = $\pm$ 5 v

$R_1 = \pm$ V/$\pm$ I Ω

This test was performed only at 85°C.



A-2 Switch Closed DC Impedance (R_{ee})

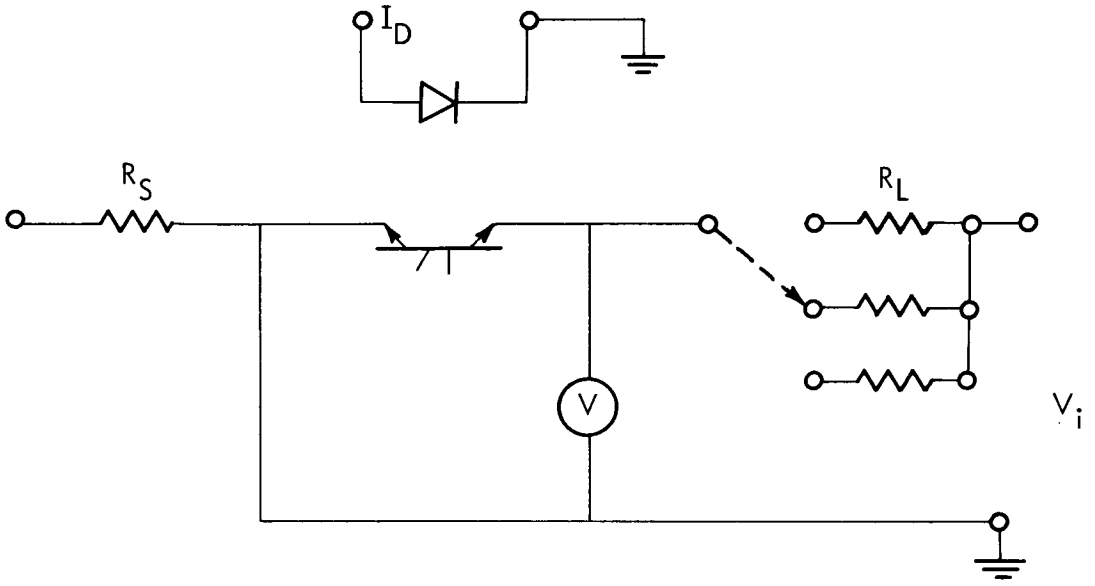
Test Condition:

$R_L = 10$ K, $V_i = 5$ v

Source power $P = V_d I_d = 50\text{-}100$ mw

$$R_{ee} = R_L \left(\frac{V}{V_i - V} \right)$$

This test was performed at -10°C, +25°C and 85°C. The input impedance of the voltmeter used in this measurement was sufficiently high so that halving it did not alter the measured contact potential. Also, care was exercised to minimize thermoelectric effects in the circuit.



A-3 Switch Input to Ground DC Impedance (R_2)

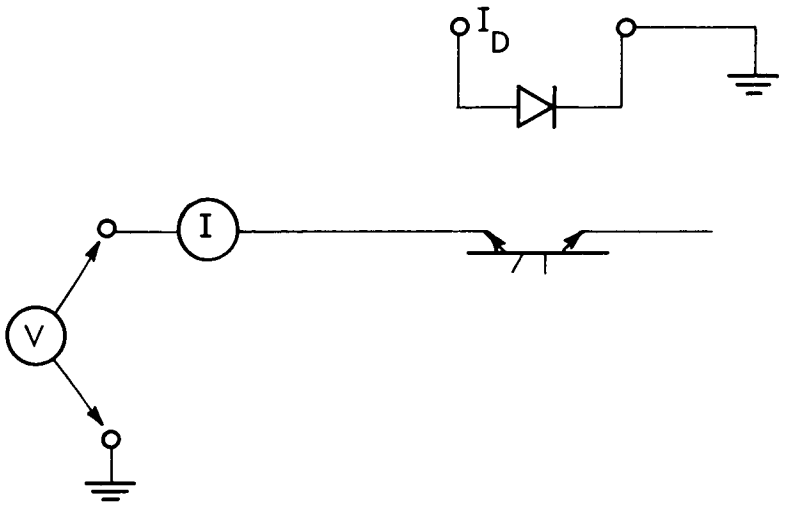
Test Condition:

Source power $P = V_d I_d = 50\text{-}100$ mw

$V = \pm 35$ v

$R_2 = \pm V/\pm I\ \Omega$

This test was performed only at 85°C.

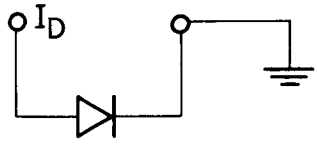


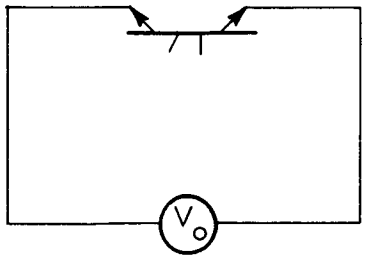
A-4 Switch Closed Contact Potential (V_o)

Test Condition:

Source power $P = V_d I_d = 50\text{-}100$ mw

This test was performed at $-10^{\circ}C$, $+25^{\circ}C$ and $+85^{\circ}C$. The input impedance of the voltmeter used in this measurement was sufficiently high so that halving it did not alter the measured contact potential. Also, care was exercised to minimize thermoelectric effects in the circuit.





A-5 Switch Open Leakage Current (I_o)

This parameter did not require separate measurement since the current measured in section A-1 was I_O.

A-6 Switch Closed Current (I_s)

This parameter did not require separate determination because it is dependent upon R_{ee}. It could be inferred from the R_{ee} test, section A-2.

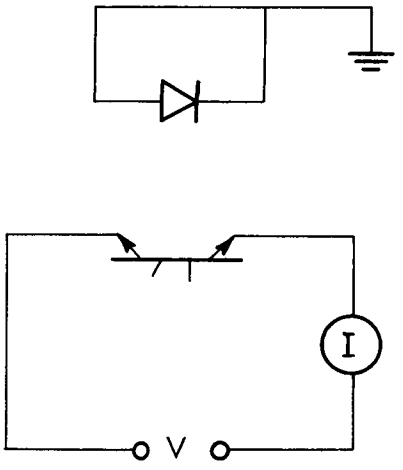
$$I_S = \pm \frac{(V_i - V)}{R_L}$$

A-7 Maximum Overload Voltage (V_m)

Test Condition:

At V = ± 35v, I must be below 350 na.

This test was performed at +25°C with representative samples checked at +85°C.



A-8 Switch Output Pulse Rise and Fall Times (t_r, t_f)

Test Conditions:

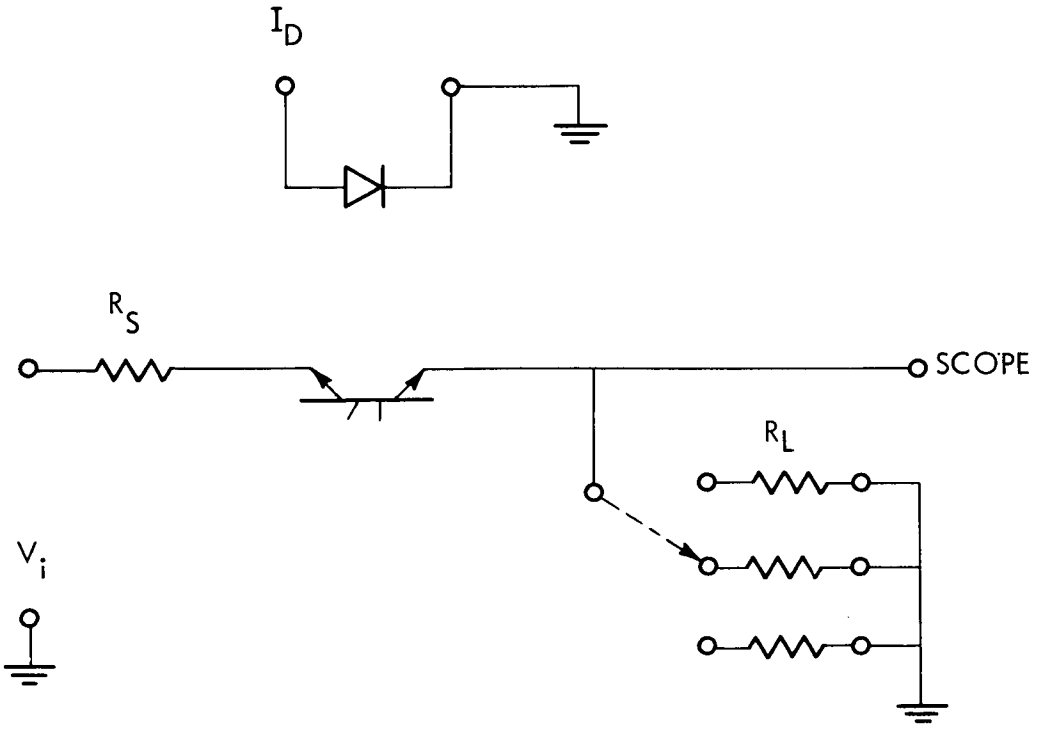
Source input pulse: rise time 100 ns

width 50 μs

average power 50-100mw

R_S = 10K R_L = 10K V_i = $\pm$ 5v

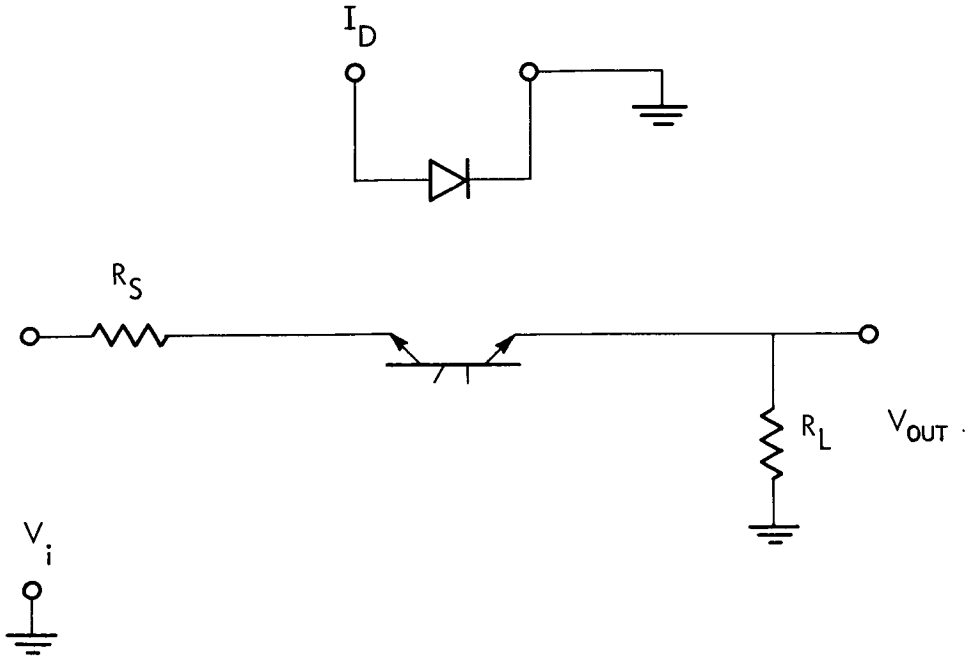
Both rise and fall times are measured from the 10 percent to the 90 percent points. Care was exercised when these measurements were taken to insure that no external capacitance (wiring, leads, etc.) contributed to the t_f time constant. The symmetry of fall times by interchanging the polarity on the silicon device was checked on representative samples. This test was performed at -10°C, +25°C, and +85°C.



A-9 Error Band

Linearity plots were made for every switch while it operated at -10°C, +25°C, and +85°C at atmospheric pressures. The linearity plots were taken at three ranges of V_{in} values.

Test 1	$R_L = 10K\ \Omega$	$V_i = \pm 5mv$
	$R_s = 20\Omega$	
Test 2	$R_L = 10K\ \Omega$	$V_i = \pm 250mv$
	$R_s = 20\Omega$	
Test 3	$R_L = 10K\ \Omega$	$V_i = \pm 5v$
	$R_s = 20\Omega$	



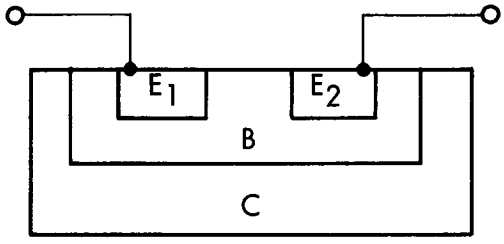
A-10 Environmental Testing

The environmental tests, listed in JPL specification No. 30257, have not been completely made on the LAS units. Some shock tests have been performed, but no thermal sterilization or space flight temperature tests have been attempted.

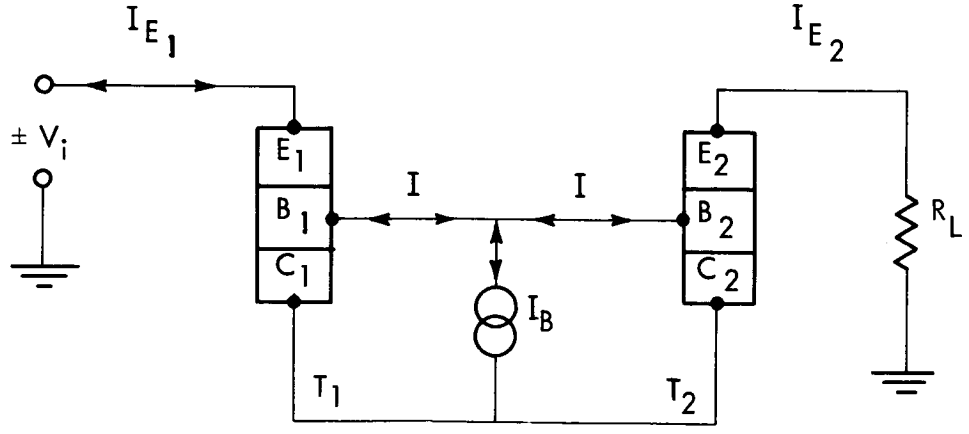
APPENDIX B - THEORETICAL ANALYSIS OF THE DETECTOR

The double emitter transistor (DET) has been shown to be an effective device for switching low level signals [2]. The effectiveness results from the symmetry in the device as well as the homogeneity that should exist between two junctions formed close together on a single semiconductor chip. An analysis of the DET on the basis of the Ebers and Moll [8] low level transistor model is presented. Relationships between the device gains and device characteristics such as offset voltage and dynamic resistance are derived.

A schematic representation of the planar DET is shown below.



The device can be NPN or PNP, and in either case it is unpolarized because of its symmetry. When driven from an external current source in a switching configuration, the above double emitter device can be represented by two separate devices as shown below.



The separate devices, T_1 and T_2 can be characterized by four α's. These are:

α_{nl} = Normal α of unit 1

α_{il} = Inverse α of unit 1

α_{n2} = Normal α of unit 2

α_{i2} = Inverse α of unit 2

From the Ebers and Moll reciprocity relations between currents in the ideal device, the following expressions for the various junction potentials can be easily derived:

$$V_{c1} = nS \ln \left[- \frac{I_{c1} + \alpha_{n1} I_{e1}}{I_{co1}} \right] \quad \text{(B-1)}$$

$$V_{e1} = nS \ln \left[- \frac{I_{e1} + \alpha_{i1} I_{c1}}{I_{eo1}} \right] \quad \text{(B-2)}$$

$$V_{c2} = nS \ln \left[- \frac{I_{c2} + \alpha_{n2} I_{e2}}{I_{co2}} \right] \quad \text{(B-3)}$$

$$V_{e2} = nS \ln \left[- \frac{I_{e2} + \alpha_{i2} I_{c2}}{I_{eo2}} \right] \quad \text{(B-4)}$$

where: $S = kt/q$

n = surface dependent parameter with value usually between unity and two (n = 1 for ideal junction).

It is assumed here that n is the same for all junctions. The remainder of the symbols are self explanatory. The expressions are valid for both NPN and PNP structures if currents flowing into the transistor are considered positive. The potential drop across the device is as follows:

$$V_{ee} = V_{e1} - V_{c1} - V_{e2} + V_{c2} \tag{B-5}$$

Upon substitution of the various potentials,

$$V_{ee} = (\pm)\, nS \quad \ln \left\{ \frac{I_{co1}\, I_{eo2}\, (I_{e1} + \alpha_{i1}\, I_{c1})\, (I_{c2} + \alpha_{n2}\, I_{e2})}{I_{eo1}\, I_{co2}\, (I_{c1} + \alpha_{n1}\, I_{e1})\, (I_{e2} + \alpha_{i2}\, I_{c2})} \right\} \tag{B-6}$$

The (+) and (-) apply to NPN and PNP configurations, respectively. Now from reciprocity and continuity considerations, we know that

$$\begin{aligned} &\frac{I_{co}}{I_{eo}} = \frac{\alpha_n}{\alpha_i} \quad ; \qquad I_e + I_c + I_b = 0 \\ &I_{e1} = -I_{e2} \equiv \left| I_e \right| \qquad I_{b1} = I_{b2} \equiv I_b \end{aligned} \tag{B-7}$$

Making use of these relationships we can write the following:

$$V_{ee} = (\pm)\ \ nS \quad \ln \left\{ \frac{\alpha_{n1}\, \alpha_{i2} \left[I_e - \alpha_{i1}\ (I_e + I_b) \right] \left[I_e - I_b - \alpha_{n2}\, I_e \right]}{\alpha_{i1}\, \alpha_{n2} \left[\alpha_{n1}\, I_e - I_e - I_b \right] \left[\alpha_{i2}\, (I_e - I_b) - I_e \right]} \right\} \tag{B-8}$$

It is convenient to rewrite the above expression in terms of β, the common-emitter current transfer ratio.

$$V_{ee} = (\pm)\ \ nS \quad \ln \left\{ \frac{\left[1 + \beta_{n1} + \beta_c \right] \left[\beta_{n2} \left(1 + \frac{\beta_c}{\beta_{i2}} \right) \right]}{\left[\beta_{n1} \left(1 - \frac{\beta_c}{\beta_{i1}} \right) \right] \left[1 + \beta_{n2} - \beta_c \right]} \right\} \tag{B-9}$$

where $\beta_c \equiv \frac{I_e}{I_b}$

Offset Voltage

The value of V_{ee} at $I_e = 0$ is usually called V_o, the offset voltage. The magnitude of this voltage sets the lower limit on the amplitude of signals that can be meaningfully sampled. Obviously, then,to minimize error,one would like V_o to be as low as possible. From expression (B-9) we have:

$$V_o = \left[V_{ee}\right]_{I_e = o} = nS \quad \ln \left\{ \frac{(1 + \beta_{n1})\ \beta_{n2}}{(1 + \beta_{n2})\ \beta_{n1}} \right\} \qquad \text{(B-10)}$$

It can be seen from (B-10) that $V_o \equiv 0$ whenever $\beta_n \equiv \beta_{n2}$ for any values of the β's and for any value of n and temperature. Usually, however, there is some mismatch in the β's,and an offset results. Figure B-1 illustrates a particular case. Here we show the dependence of V_o on β mismatch at room temperature and 85^oC. The curves represent a constant V_o of 50 μv. It can be seen that at room temperature for a β_{n1} of 10, β_{n2} is to be matched to within two per cent of β_{n1} for $V_o \leq 50\ \mu v$. For a β_{n1} of 100, the mismatch can be 26 per cent. At higher temperatures the match must be closer for the same V_o. This may be somewhat compensated by increases in $\beta$with increasing temperature.

ON Impedance

Another parameter of the DET is the impedance R_{ee} across the swtich when it is turned on. For effective circuit operation, this resistance should be as low as possible. The resistance can be readily obtained by differentiating equation (B-9) with respect to I_e.

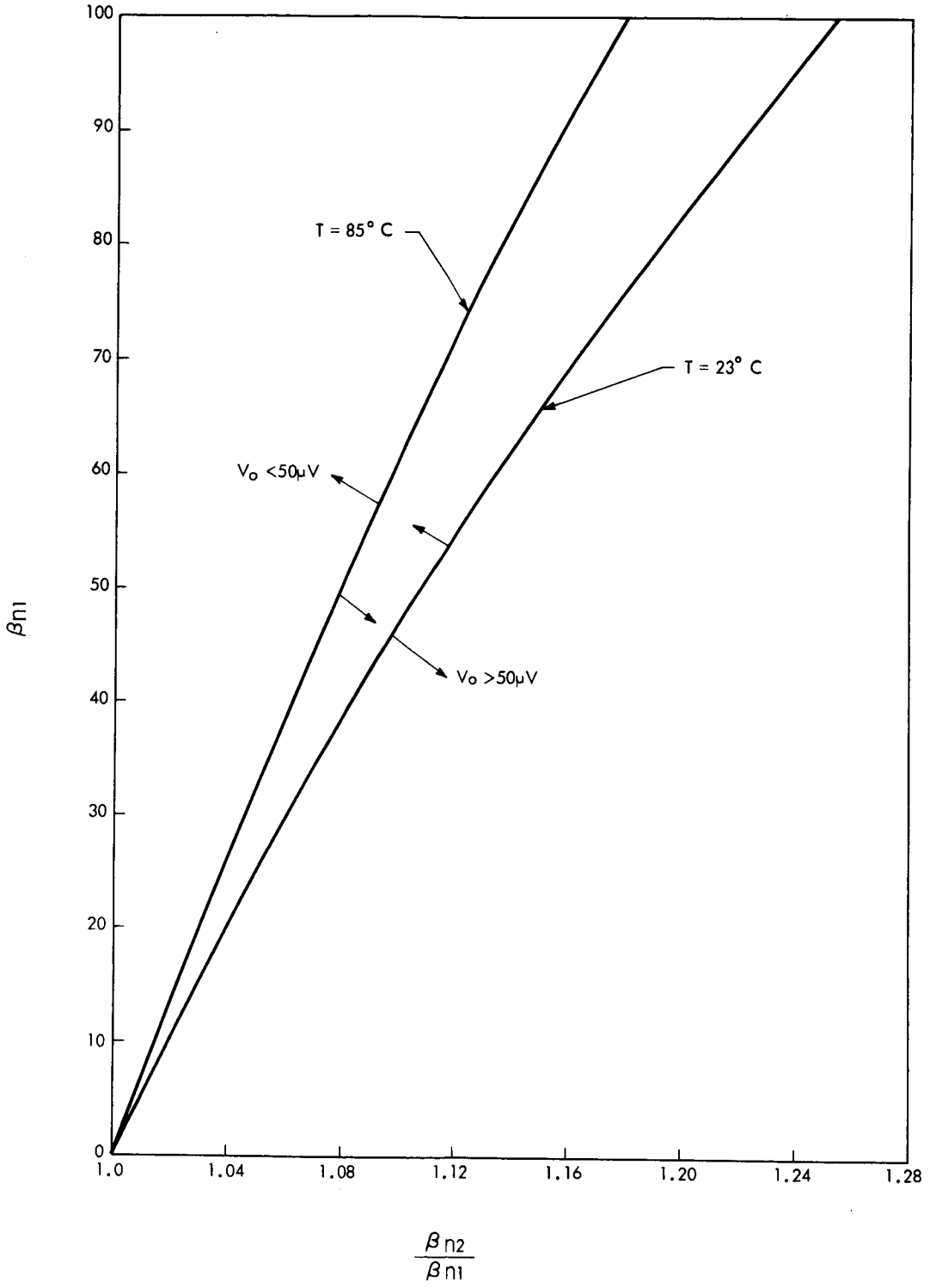


FIGURE B-1 - DEPENDENCE OF OFFSET VOLTAGE ON β_i

$$R_{ee} = \frac{dV_{ee}}{dI_e} = \frac{nS}{I_b} \left\{ \left[\frac{1}{1+\beta_{n1}+\beta_c}\right] + \left[\frac{1}{\beta_{i2}+\beta_c}\right] + \left[\frac{1}{\beta_{i1}-\beta_c}\right] + \left[\frac{1}{1+\beta_{n2}-\beta_c}\right] \right\} \quad \text{(B-11)}$$

For the case where:

$$\beta_{n1} = \beta_{n2} \equiv \beta_n$$

$$\beta_{i1} = \beta_{i2} = \beta_i$$

equation (B-11) reduces to

$$R_{ee} = \frac{2nS}{I_b} \left[\frac{\beta_i}{\beta_i^2 - \beta_c^2} + \frac{\beta_n + 1}{(\beta_n + 1)^2 - \beta_c^2} \right] \quad \text{(B-12)}$$

Usually, $\beta_n >> \beta_i$ and the quantity β_c is small compared to both β_n and β_i since $I_b > I_e$. Therefore, the ON impedance can be approximated by:

$$R_{ee} \approx \frac{2nS}{I_b} \left(\frac{1}{\beta_i}\right) \quad \text{(B-13)}$$

Besides the dynamic resistance, the switch has a finite non-zero intrinsic resistance, R_i, in the contacts and its bulk material. This should be low (1 or 2 Ω) and represents the lowest possible resistance that can be obtained at high I_b. We should write therefore a more accurate expression for the total switch resistance.

$$R_{ee} \simeq \frac{2nS}{I_b} \left(\frac{1}{\beta_i}\right) + R_i \quad \text{(B-14)}$$

Breakdown Voltage

Device breakdown, BV_{ee}, occurs when $\alpha M = 1$, where α is the current gain, and M is the multiplication factor which can be expressed in terms of the magnitude of the applied reverse bias as :

$$M = \frac{1}{1 - \left(\frac{BV_{ee}}{BV_{eb}}\right)^n} \tag{B-15}$$

where BV_{eb} is the critical value of the reverse bias at which avalanche breakdown occurs. The exponent n is of the order of $2 \sim 4$ for silicon[9].

Since αM must be equal to unity, Eq. (B-15) can be written as

$$1 - \left(\frac{BV_{ee}}{BV_{eb}}\right)^n = \alpha \tag{B-16}$$

or, in terms of β_i (where β_i = inverse β of the two halves)

$$\left(\frac{BV_{ee}}{BV_{eb}}\right)^n = \frac{1}{\beta_i + 1} \tag{B-17}$$

For $\beta_i >> 1$,

$$BV_{ee} \simeq BV_{eb} \left(\frac{1}{\beta_i}\right)^{1/n} \tag{B-18}$$

where BV_{eb} = avalanche breakdown voltage, and is a function of the impurity level, N_B, of the base region.

Response Time

From Ebers' and Moll's work, approximate expressions cannot easily written for the DET, mainly because one is dealing with a device with separate (two) emitters - with the rest of the transistor, base and collector common for the two halves. The speed of response of the DET is still of importance, because it is the silicon device which primarily restricts the LAS. The frequency-handling capability was determined empirically using the following expression:

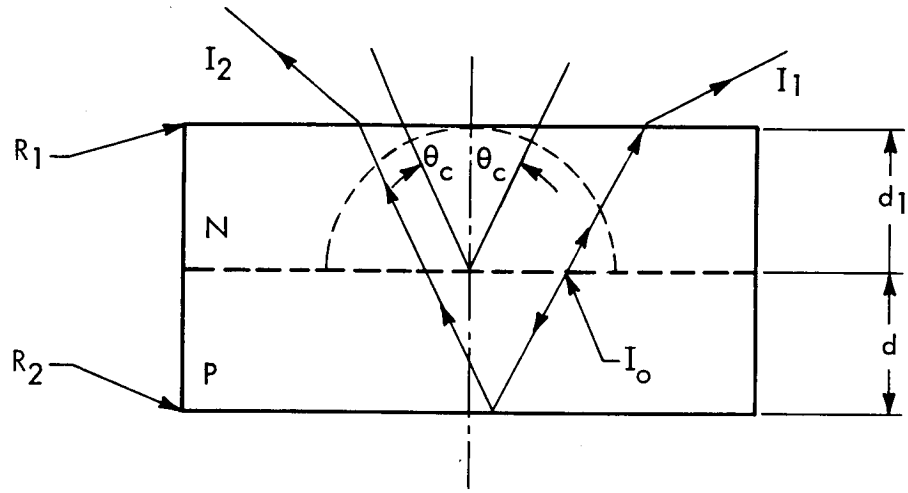
$$f_{max} = \frac{1}{t_{ON} + t_{OFF}} \tag{B-19}$$

Since $t_{OFF} >> t_{ON}$

$$f_{max} \simeq \frac{1}{t_{OFF}} \tag{B-20}$$

APPENDIX C - ANALYSIS OF THE EFFICIENCY OF DOME VS. FLAT LIGHT SOURCE

An investigation was conducted to determine whether a dome or a flat GaAs light source was better for application in the LAS. Let us consider a plane GaAs p-n junction as shown in Figure C-1.



where
- d = thickness of P region
- d_1 = thickness of N region
- α_n = absorption coefficient of N region
- α_p = absorption coefficient of P region
- R_1 = coefficient of reflection between GaAs and air
- R_2 = coefficient of reflection between GaAs and some reflective surface
- n = refractive index of GaAs
- θ_c = critical angle

FIGURE C-1 - PLANE GaAs LIGHT SOURCE

Light generated at the junction will travel in two directions, one half going through the N region, the other half through the P region. The latter will be reflected at the R_2 interface and will go through the P region once more, then leave the device

through the N region. These are represented in Figure C-1 by I_1 and I_2. If I_0 is the total light generated then $I_0/2$ will go in either direction, and one can write

$$I_1 = \frac{I_0}{2} e^{\left(-\alpha_n d_1\right)}(1 - R_1) \qquad (C\text{-}1)$$

and

$$I_2 = \frac{I_0}{2}\left[e^{-\alpha_p d}\left(R_2\right)e^{-\alpha_p d} e^{-\alpha_n d_1} (1 - R_1)\right] \qquad (C\text{-}2)$$

assuming small enough angles such that d COS $\theta \approx d$. Without considering the restriction imposed by total internal reflection, the total light leaving the device would be just

$$I_T = I_1 + I_2 \qquad (C\text{-}3)$$

The critical angle based on $n = 3.5$ is

$$\theta_c = \sin^{-1} \frac{1}{n} \simeq 16^o \qquad (C\text{-}4)$$

This means that only the light within a cone of half angle θ with apex at the source will leave the device. This introduces a reduction by a factor of

$$\frac{\text{Area of curved cone base}}{\text{Area of hemisphere}} = (1 - \text{COS } \theta_c) \qquad (C\text{-}5)$$

Thus, the total light leaving the plane device is

$$I_{T_1} = (I_1 + I_2)\ (1 - \text{COS } \theta_c)$$

$$I_{T_1} = I_o (1 - \text{COS } \theta_c)\left[\frac{(1 - R_1)}{2} e^{-\alpha_n d_1}\left(1 + R_2 e^{-2 \alpha_p d}\right)\right] \qquad (C\text{-}6)$$

If from the GaAs the light goes into air, the quantity $\frac{(1 - R_1)}{2}$ can be rewritten in terms of the refractive indices of GaAs and air:

$$\frac{1 - R_1}{2} = \frac{2n}{(n + 1)^2} \qquad (C\text{-}7)$$

and the total amount of light leaving the device becomes

$$I_{T_1} = I_o (1 - \cos \theta_c) \left[\frac{2n}{(n + 1)^2} \; e^{- \alpha_n d_1} (1 + R_2 \; e^{-2 \alpha p d}) \right] \qquad (C\text{-}8)$$

Now consider a hemispherically constructed light source as shown in Figure C-2. Proceeding as before and noting that light will reach the R_1 interface in the direction of the normal, the total light leaving the devices is:

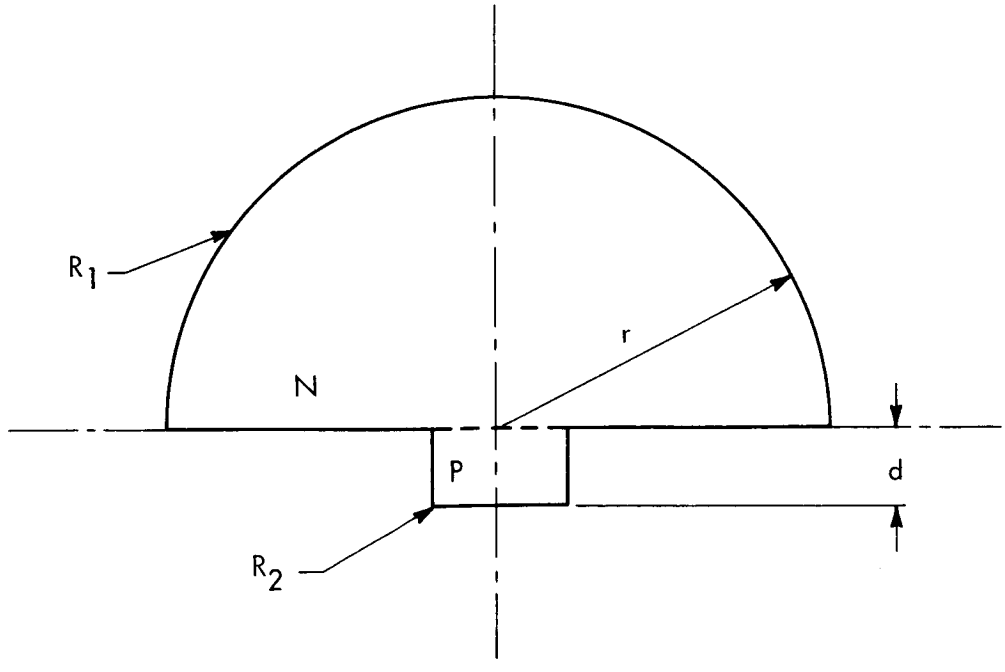


FIGURE C-2 - HEMISPHERICAL GaAs SOURCE (POINT SOURCE)

$$I_{T_2} = I_0 \left[\frac{2n}{(n+1)^2} \; e^{-\alpha_n r} \; (1 + R_2 \, e^{-2\alpha_p d}) \right] \qquad \text{(C-9)}$$

Comparing equations (C-8) and (C-9) it is apparent that the hemispherical device is better by a factor of

$$\frac{1}{(1 - \cos \theta_c)} \; e^{\left[-\alpha_n (r - d_1)\right]}$$

Reconsider the hemispherical device, but with sources extended over the base instead of one point source located at the center. Figure C-3 shows this arrangement. This model consists of eight ring sources and a circular source at the center. All the light generated at the center source and its vicinity will leave the device, but light generated outside of this area will suffer internal reflection, and only a fraction will leave. To facilitate the treatement of this arrangement, a 10 mil base diameter hemisphere was assumed with approximately 61 sources. Part of the analysis was done graphically. Taking the difference in contributions of the sources into account, by introducing the quantity A_i, one arrives at the following expression:

$$I_{T_3} = I_0 \left[\frac{2n}{(n+1)^2} \; e^{-\alpha n r} \; (1 + R_2 \; e^{-2 \alpha p d}) \right] \sum_{i=1}^{5} (A_i) \qquad \text{(C-10)}$$

A_i is the product of the following quantities,

$$a_{i1} = \frac{\text{area of } i^{th} \text{ source}}{\text{total junction area}}$$

$$a_{i2} = \frac{\text{number of like i sources}}{\text{total number of sources}} \qquad \text{(C-11)}$$

$$a_{i3} = \frac{\text{area through which light passes}}{\text{total area of hemisphere}}$$

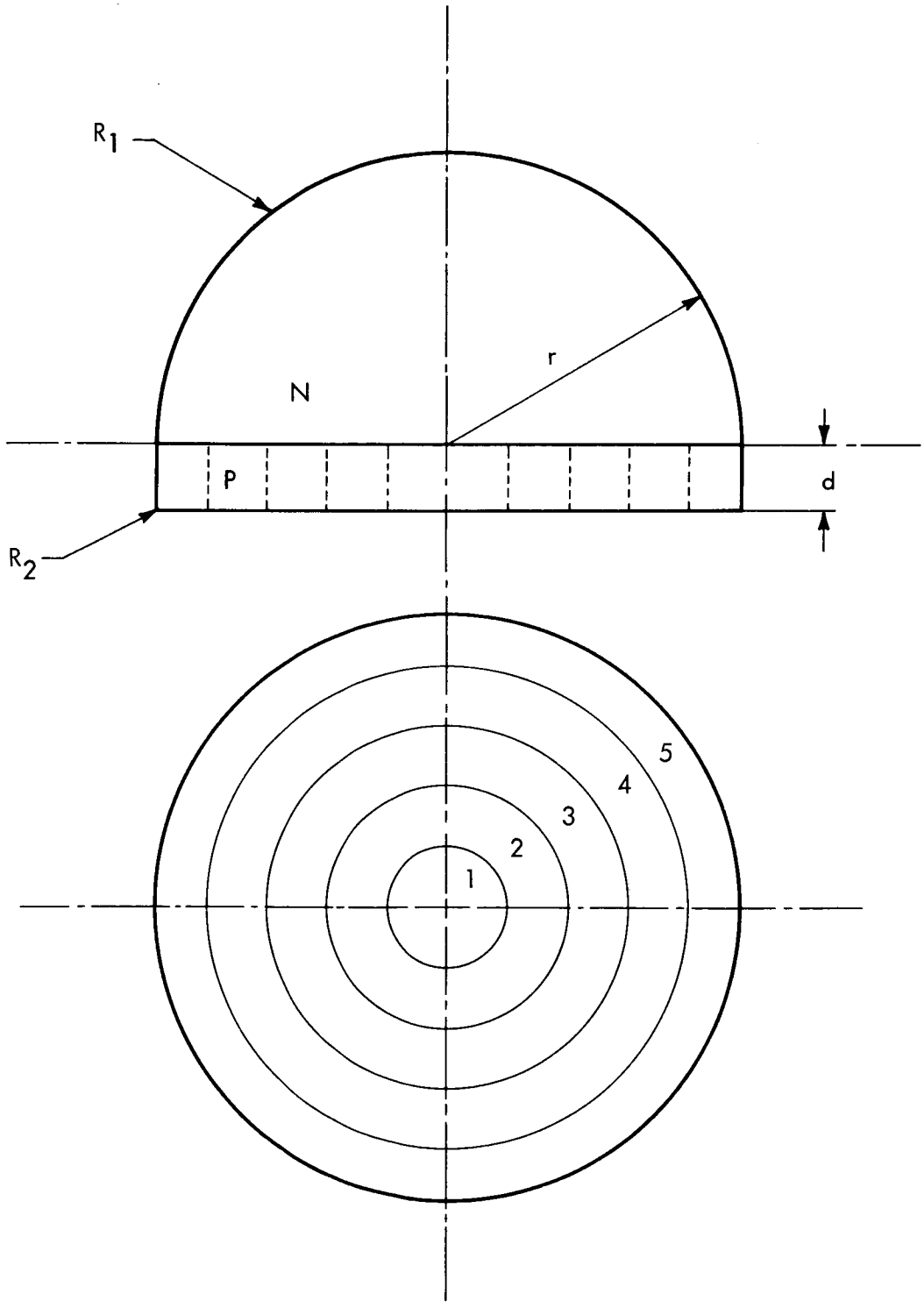


FIGURE C-3 - HEMISPHERICAL GaAs LIGHT SOURCE (EXTENDED SOURCES)

For the assumed dimensions, the total emitted light is:

$$I_{T_3} = 0.318\, I_{T_2} \qquad \text{(C-12)}$$

Equation (C-12) shows that when the number of the sources is extended the light output is only about 30% of what it was with a single point source. One can thus conclude that for a hemispherical construction a point source at the center of the base will give optimum performance insofar as total light output is concerned.

Returning to the plane structure, consider the arrangement of Figure C-4. The light now travels from GaAs into a dielectric (epoxy for example).* This will change the quantity $(1 - R_1)$ and also the critical angle θ_c:

$$R_1 = \frac{(n - n_1)^2}{(n + n_1)^2} \qquad \text{(C-13)}$$

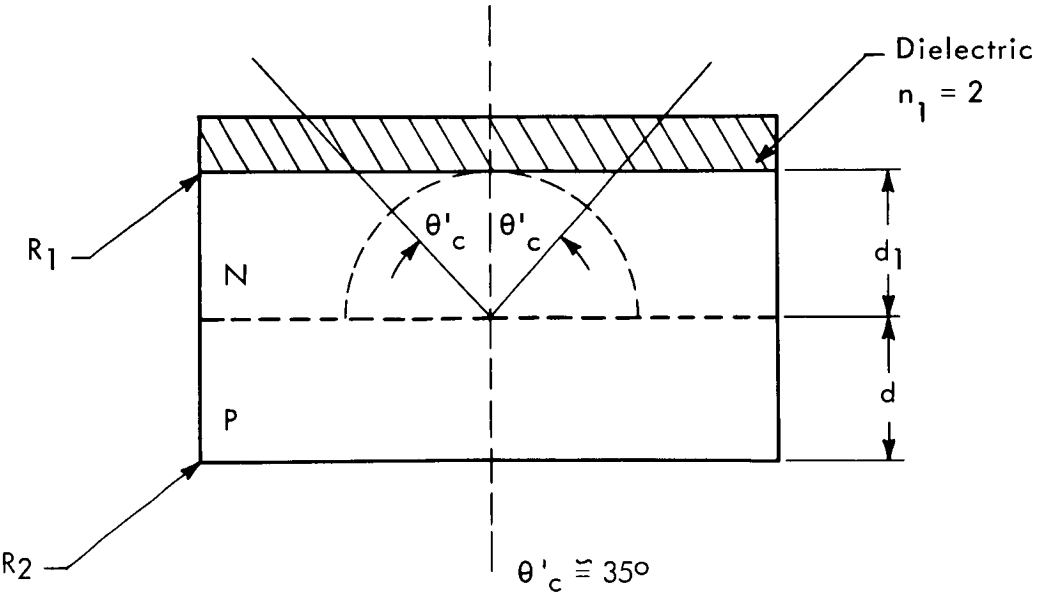


FIGURE C-4 - PLANE GaAs SOURCE WITH DIELECTRIC COATING

* The epoxy used on actual diodes had a refractive index varying between 1.4 and 1.55. To simplify matters, $n_1 = 2$ will be used for the dielectric.

$$1 - R_1 = \frac{(n + n_1)^2 - (n - n_1)^2}{(n + n_1)^2} = \frac{4nn_1}{(n + n_1)^2} \qquad \text{(C-14)}$$

The critical angle becomes

$$\theta_c' = \sin^{-1}\left(\frac{n_1}{n}\right) = \sin^{-1}\left(\frac{2}{3.5}\right) \simeq 35^o \qquad \text{(C-15)}$$

This means that only the light within a cone of half angle θ_c' with apex at the source will leave the device. This introduces a reduction by a factor of

$$\frac{\text{Area of curved cone base}}{\text{Area of hemisphere}} = (1 - \cos\theta_c') \qquad \text{(C-16)}$$

The total light leaving the device is now

$$I_{T_4} = I_0 (1 - \cos\theta_c')\left[\left(\frac{2nn_1}{(n+n_1)^2}\right) e^{-\alpha_n d_1} (1 + R_2\, e^{-2\alpha_p d})\right] \qquad \text{(C-17)}$$

Comparing the total light outputs of the different arrangements under consideration, one obtains the following ratios:

$$\frac{I_{T_2}}{I_{T_1}} = \frac{1}{(1 - \cos\theta_c)}\, e^{-\alpha_n (r - d_1)} \qquad \text{(C-18a)}$$

$$\frac{I_{T_2}}{I_{T_3}} = \frac{1}{0.318} \simeq 3.14 \qquad \text{(C-18b)}$$

$$\frac{I_{T_2}}{I_{T_4}} = \frac{1}{(1 - \cos\theta'_c)}\left[\frac{(n + n_1)^2}{n_1 (n + 1)^2}\, e^{-\alpha_n (r-d_1)}\right] \qquad \text{(C-18c)}$$

On the basis of the foregoing calculation, the hemispherical device with a single point source is still the best for overall light emission.

Let us now take into account the detector. Figures C-5a and C-5b show the light sources together with the detecting silicon devices. Even a casual observation shows that all the light emitted from the hemisphere will not reach the detector, while practically all the light emitted from the plane device will be collected.

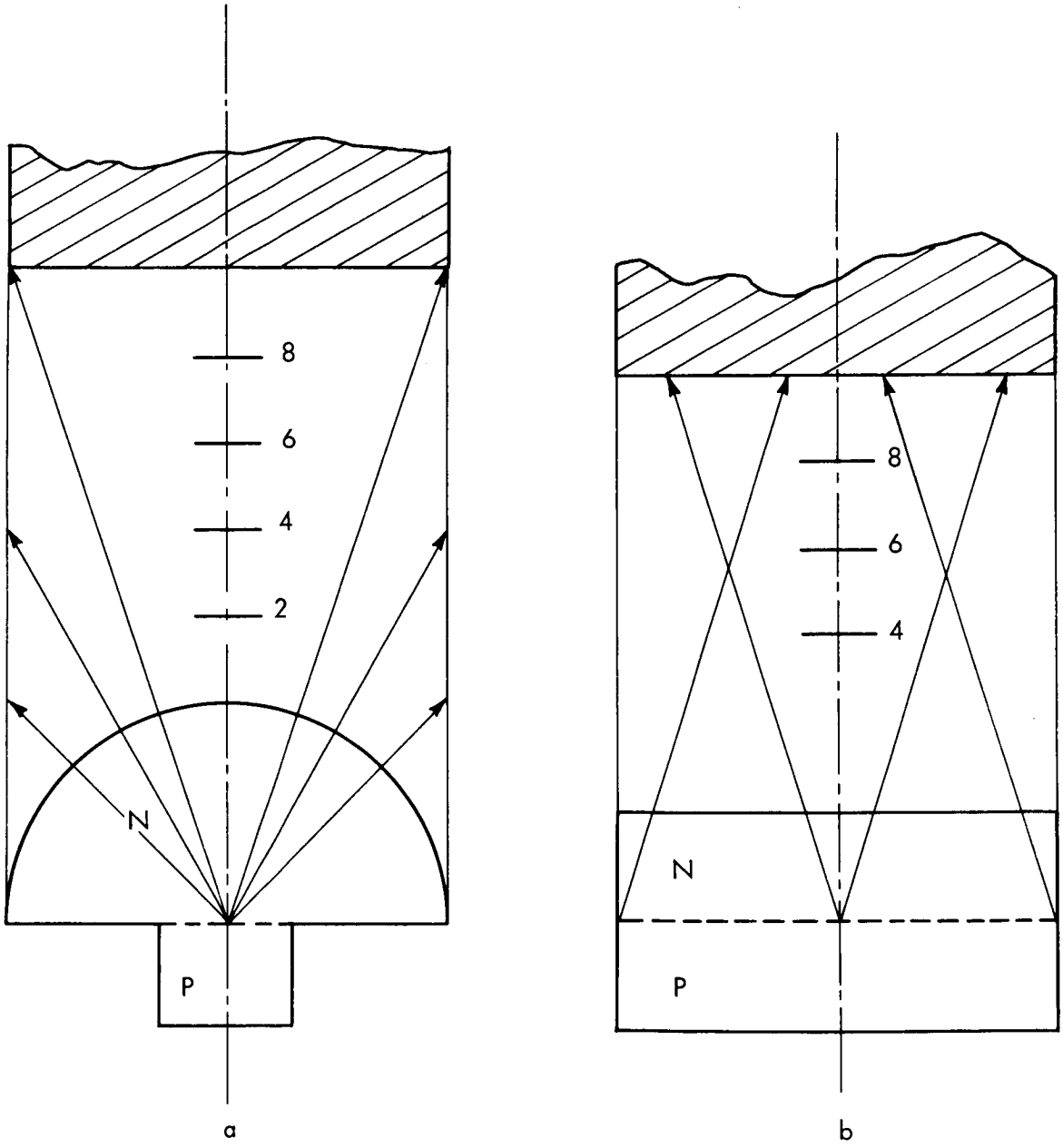


FIGURE C-5 - LIGHT SOURCE AND DETECTOR

Assume a 10 mil diameter hemisphere, a 10 x 10 mils squared plane device and a 10 x 10 mils squared detector. Table C-1 shows the percentage of the total emitted light reaching the detector for different emitter-detector distances, considering a three-dimensional model.

TABLE C-1
(Hemispherical Device)

Emitter Detector Distance (mils)	Percentage Reaching the Detector
0	29.6
1	23.6
2	19.0
3	15.6
4	13.0
5	10.6
6	9.4
7	8.0
8	7.0
9	6.2
10	5.6

From the above calculation, for best detection, one has to place the detector on the top of the hemispherical source. Even in this arrangement only about 30% of the total emitted light will reach the silicon detector. This means that the ratio given by equation(C-18c) would change to:

$$\frac{0.296}{(1-\cos\theta'_c)}\left[\frac{(n+n_1)^2}{n_1(n+1)^2}\right]e^{-\alpha n\,(r-d_1)} \qquad \text{(C-19)}$$

It is clear that although the hemispherical device with a point source is the best for maximum total light output, for the purpose of the LAS the plane device with the dielectric coat is better.

The advantage in using the dielectric coat comes from not only the increase in the critical angle, but also from a substantial increase in transmission from ~69% to ~93%. With 93% transmission the loss due to multiple reflection is negligible. In the above work light was assumed to travel from GaAs source to dielectric and from dielectric to the silicon detector. If there is an air layer between the dielectric and the detector, one finds that the presence of the dielectric does not offer any improvement in the critical angle, though slight improvement in transmission is observed. Using a curved dielectric over using a flat dielectric shows some improvement in the angle of refraction.

Summarizing the results, one finds on the basis of the above analysis that the ratio

$$\frac{I_{T_2}}{I_{T_4}} = \frac{\text{Total emitted light from hemisphere with point source}}{\text{Total emitted light from plane device with dielectric}} = \tag{C-20}$$

$$\frac{1}{(1 - \cos \theta'_c)} \left[\frac{(n + n_1)^2}{n_1 (n + 1)^2} \right] e^{-\alpha_n (r - d_1)} = 4.15\, e^{-\alpha n (r - d_1)}$$

Assuming that $(r - d_1)$ is of the order of 10 mils, then the above ratio becomes with the inclusion of the detection consideration:

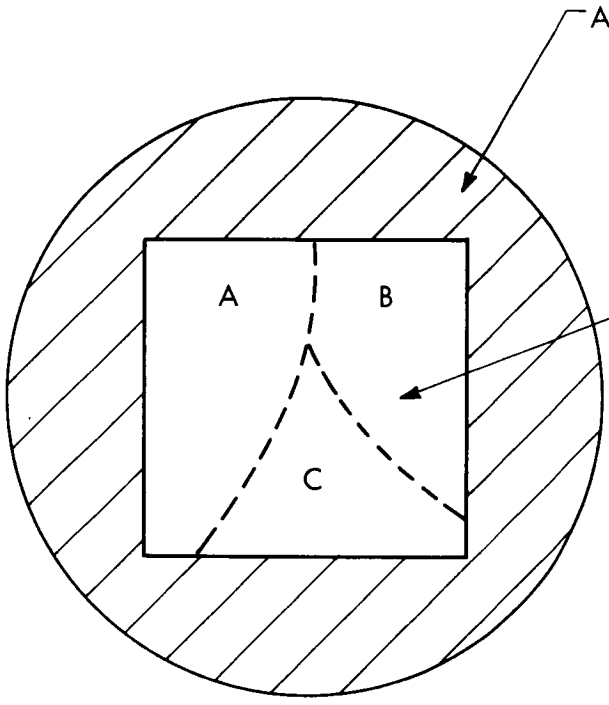
$$\left(\frac{I_{T_2}}{I_{T_4}} \right)' = 0.296 \times 4.15 \times 0.467 \tilde{=} 0.573 \tag{C-21}$$

which clearly shows the advantage of the plane light source with the dielectric over the hemisphere with a point source for the LAS.

APPENDIX D - YIELD CONSIDERATIONS

Due to the developmental nature of the contract, a detailed yield evolutation was not attempted. Three runs were selected, however, to give some indication of the spread in DET characteristics, resulting from a representative fabrication process. Types 1, 2, and 3 DET units were considered. In general, one would expect far higher yield figures from Type 1 devices since the junctions were formed by diffusion only, whereas Types 2 and 3 would have lower yield figures since the collector-base junction was formed by an epitaxial growth process. Results backed up the expectations.

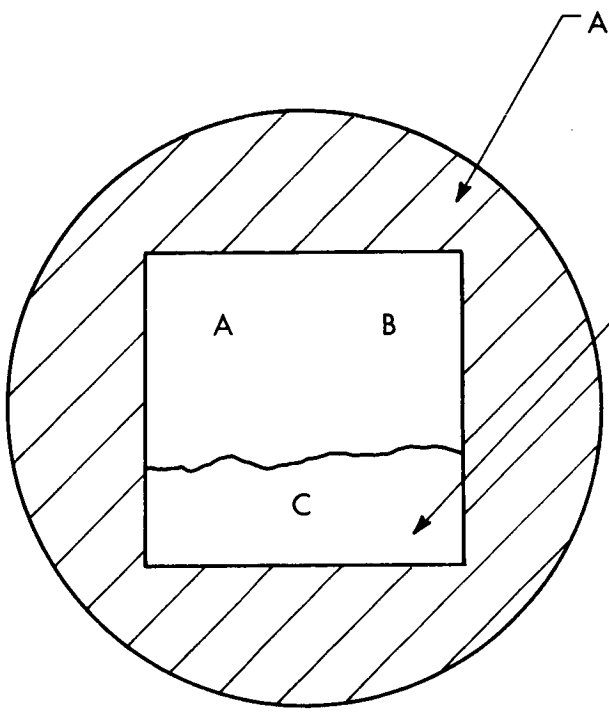
1 - Type 1. (Run #110).



	β_n	β_i	BV_{ee} (volts)
A	500	50	10-11
B	1300-1400	130	10-11
C	500-1300	50-130	10-11

Due to a fault in the mask, every 5th row was useless, leaving about 320 units with medium and small size geometries. Ninety eight units were mounted for different tests and incorporated into complete LAS devices. Approximately one hundred units were destroyed or lost during assembly and processing.

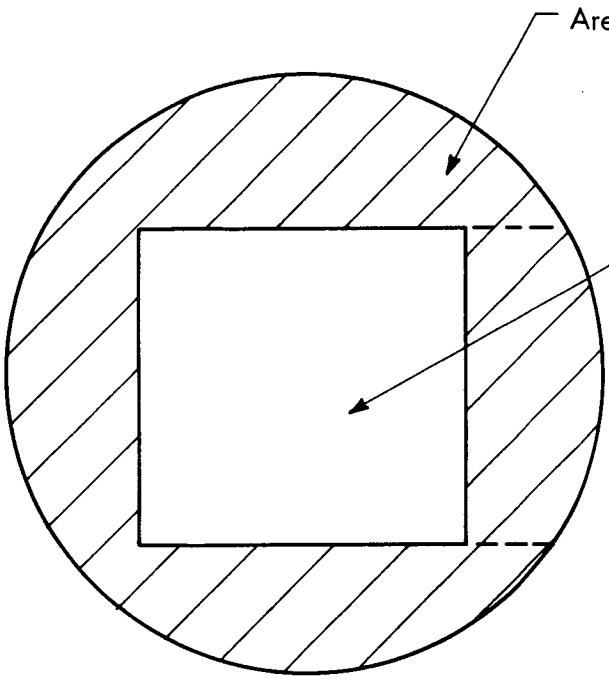
2 - Type 2. (Run #168)



	β_n	β_i	BV_{ee} (volts)
A	700-800	50	13-14
B	Punch through was observed due to a taper in the grown p layer		
C	350-600	50-85	20-25

Fifty one units were mounted (all units were of medium size geometry) for different tests and incorporated into complete LAS units. Approximately fifty units were destroyed or lost during processing and assembly.

3 - Type 3. (Run # 173)



β_n	β_i	BV_{ee} (volts)
280-330	20-50	18-24

Random checking within the "useful area" showed the presence of leaky units. Fifty three selected units were incorporated into complete LAS units. All units were of medium size geometry. About fifty units were lost or destroyed during assembly and processing.

APPENDIX E - PUBLICATIONS, PRESENTATIONS, INVENTION DISCLOSURES

During the course of this program, technical information concerning the Light Actuated Switch was disseminated through the following media:

Presentations -

1. IEEE Device Conference, Washington, D. C. - October (1964) "GaAs Photon Activated Switch" - T. H. Yeh.
2. IEEE Metropolitan Section, Nutley, New Jersey - November (1964) "GaAs Light Actuated Switch" - P. Polgar.
3. Progress Reports to JPL.

August 12, 1963	(Poughkeepsie, N. Y.)
October 29, 1963	(Poughkeepsie, N. Y.)
November 18, 1963	(Pasadena, California)
December 19, 1963	(Poughkeepsie, N. Y.)
March 31, 1964	(Poughkeepsie, N. Y.)
August 6, 1964	(Poughkeepsie, N. Y.)
November 5-6, 1964	(Poughkeepsie, N. Y.)

Publications -

1. "GaAs-Si Photon Activated Switch" - to be submitted to PGED transactions of IEEE.
2. Monthly Progress Reports to JPL.

Invention Disclosures -

1. "Fabrication of Heterojunction - Hemojunction Transistors" - T. H. Yeh, W. Pieczonka, M. Roy, E. Blakeslee.
2. "Gallium Arsenide Surface - Barrier Diodes"- W. Pieczonka, M. Roy, T. H. Yeh.
3. "GaAs Light-Emitting Diode" - M. Roy, T. H. Yeh.