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Design Study of Error-Detecting and Error-Correcting Shift Register

F. Michael Horn

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ABSTRACT

2130-2

This Report details the design study of an N-bit error-detecting and error-correcting (NEDEC) shift register, N being the number of stages in the device. Design criteria are discussed, and NEDEC philosophy, mechanization, and development are detailed. A six-stage circulating register was constructed and successfully tested over the temperature range (-20 to $+100°C$). Several representative peripheral circuits are included, together with proposed feedback-logic mechanization. Advantages and disadvantages are enumerated. Test data are given for reference.

I. INTRODUCTION

The advantages attributed to error-check coding schemes are well known. These schemes offer diminishing returns because the ratio of check bits to information bits become excessive in light of the error detection/correction capability obtained. A break point is reached beyond which increases in system complexity fail to yield commensurate increases toward achievable reliability. The NEDEC system offers two distinct advantages over coding schemes:

1. Check bits are not required. All bits are usable information.

2. A reasonable increase in hardware yields N-bit transient error-detection/correction, a result impossible with coding schemes.

Such a device is exceptionally useful in unmanned spacecraft applications for greatly reducing vulnerability to transient failures.

II. DESIGN CRITERIA

The NEDEC approach must be constrained by a set of ground rules:

1. *Physical Considerations*. Weight and volume must not be excessively compounded over a system without error detection and correction. Every con-

sideration should be given to the design to ensure simplicity of fabrication and packaging and to minimize post-fabrication electrical adjustment.

2. *Memory Constraints*. No loss of memory should result from internal malfunction or external system failure.

3. *Event Timing.* No timing error whatsoever can be tolerated. Register count may differ from actual time count in case of power failure or register internal corrective action. For a pulse rate n/t, n time-count pulses may be lost, where

$$n = [(n/t)] [(T)]$$

$T =$ duration of power failure or corrective action.

4. *Environmental Constraints.* Any practical design should ensure adequate operation over the expected environment without the use of compensating circuitry because such compensation often decreases reliability.

III. DESIGN LIMITATION

It is assumed that information is loaded into the register correctly. No provision is incorporated to verify initial register content.

IV. DESIGN PRINCIPLES

The classical core-diode shift register was the point of departure in evolving an error-correcting device. This consists of two toroids and two diodes per stage. Shifting of information from transmitter core to receiver core is accomplished by current steering. A detailed description of this operation is included in Appendix B. At each transfer, the transmitter core is reset, with the accompanying loss of information. It is the destructive readout of the transmitter core that prevents detection of shifting errors. If a nondestructive information transfer were possible, then both transmitter and receiver cores could be compared for agreement. A transfluxor or other multi-aperture device could fulfill this requirement. It would be necessary to read out the transmitter core through the minor aperture, using the output energy to adjust the state of the receiver core. Both transmitter and receiver cores could then be primed, interrogated, and compared.

The major problem posed by nondestructive transfer is a flux-gain limitation. Since the flux output during switching of the transmitter-core minor aperture is less than that required to switch the receiver core, flux gain is required. Flux gain could be achieved by using a current-steering technique similar to that of the classical core-diode register. Subsequent circuit design proceeded along these lines.

V. FUNCTIONAL DESIGN

A current-steering transfer technique leads to the NEDEC shift register. NEDEC design employs two multiaperture cores and two diodes per register stage. For logical purposes, the register may be divided into register cores and buffer cores, although both sets alternately serve as a transmitter and a receiver, respectively. NEDEC logical organization is given in Fig. 1.

Assume that the data to be shifted appears initially in the register cores. The buffer cores are set to zero by a common clear winding. Information in the register cores is now transferred to the buffer cores by nondestructive readout of the register cores. Both core sets should thus compare bit to bit. This comparison is made by priming both core sets, and by interrogating buffer and register cores. One sense wire links all register cores in the same direction, while a second sense wire links all buffer cores in a similar direction. These sense lines drive opposite ends of a transformer primary. If the transfer was perfect, the voltage induced on both sense lines should be exactly

equal, and the voltage at the transformer secondary should be zero. Any discrepancy between register and buffer cores will appear at the secondary as a positive or negative voltage, which may be used in turn to drive an error indicator. Core variations may be normalized by use of a small shuttle-noise-cancelling toroid with reverse windings.

Up to this point, the information has not been destroyed in the register cores. If no error was made during transfer, these cores may now be cleared, and a transfer may be initiated between buffer cores and register cores. The process is identical to that described above. If, after comparison, no error indication is present, the buffer cores may then be cleared, and the shift cycle is complete. Note that the shift is completed in parallel. In event of an error, the error voltage may be used to command iteration of the transfer cycle. This cycle may be repeated until the error indication disappears. Only in the event of valid transfer will the cycle continue and clear the transmitter cores.
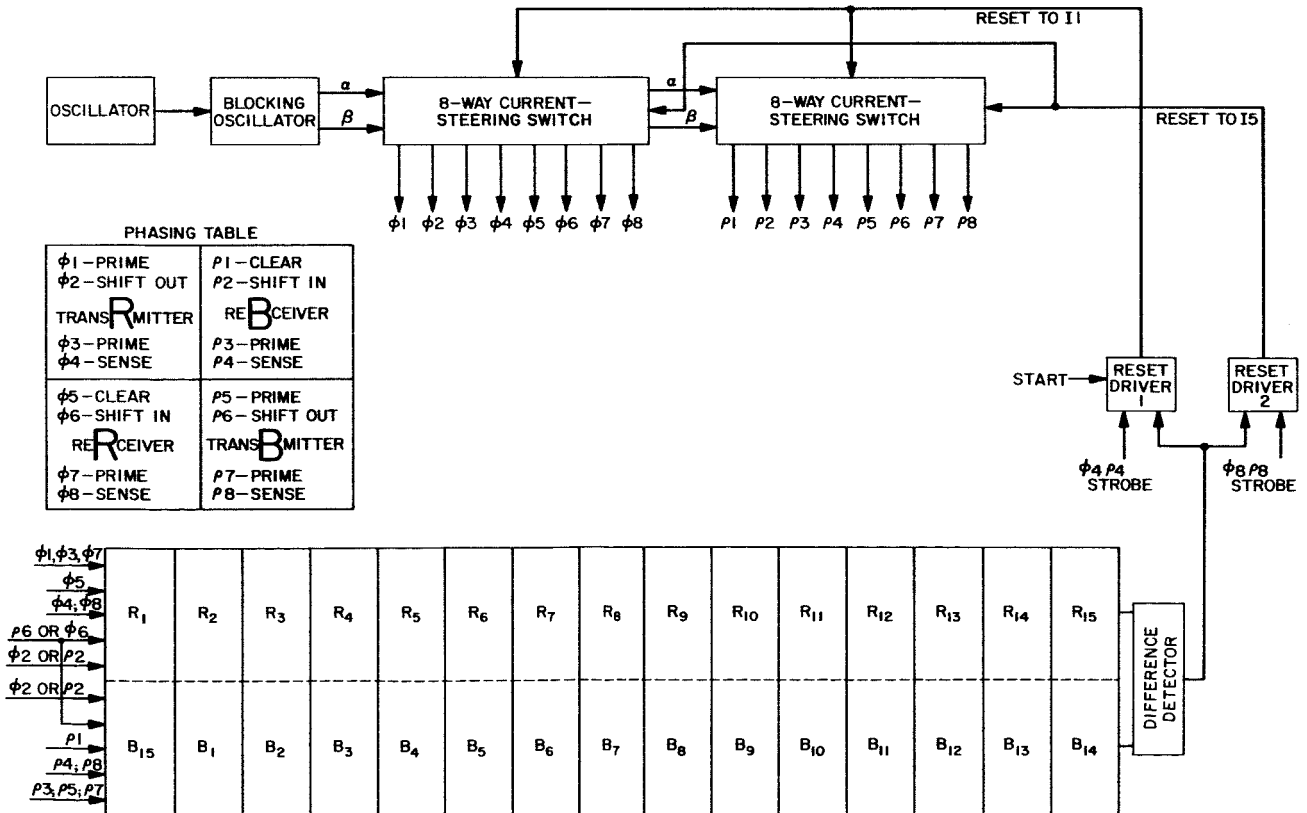

Fig. 1. NEDEC organization

VI. DETAIL DESIGN

The NEDEC system may be divided functionally into three principal sections: register proper, clock-driver circuitry, and error detection/correction circuitry. Design emphasis was placed on the register itself, although each section has been given consideration.

A. Register Proper

The heart of the NEDEC system is a multiaperture ferrite core. A shaped transfluxor, manufactured by Siemens & Halske A.G., or equivalent, is utilized. The Siemens B 64 715 R 402 (Fig. 2) has three minor apertures, two of identical size and one with a smaller diameter. An exemplary core-circuit configuration is shown in Fig. 3.

The nondestructive complete transfer is accomplished in two steps: (1) parallel transfer from the register cores to the buffer cores during Intervals 1–4, and (2) parallel transfer from the buffer cores to the register cores during Intervals 5–8.

Drive currents for the register cores are denoted ϕ. Currents for the buffer cores are denoted ρ (Table 1). A timing-reference diagram is included in Appendix A. Intervals 1–8 occur in sequence if no error is made. If an error is made during transfer from register to buffer cores, this is detected during interval I4. The error voltage triggers Reset Driver 1 (Fig. 1), which returns the clock to interval I1. Similarly, any error made during transfer from buffer cores to register cores is detected

during interval I8, which triggers Reset Driver 2, returning the clock to interval I5. For either case, Intervals 1–4 or Intervals 5–8 are iterated until the error indication disappears.

For simplicity only one-half of the complete shift operation is described; i.e., the transfer from the register cores to the buffer cores. The same process is operative for the opposite transfer. During interval I1, the receiver core is cleared through the major aperture by phase $\rho 1$. Simultaneously, the transmitter core, which has been set during a previous phase, is primed for readout by $\phi 1$. Transfer may now take place. Current $\phi 2$ or $\rho 2$ will divide between transmitter- and receiver-core paths. If the transmitter core was a "one", it will switch to "zero" (around the minor aperture only). During switching time, the transmitter-core path offers a very high impedance relative to the receiver-core path. Thus, current will be steered to the receiver core and will set it to the "one" state. Had the transmitter core previously been "zero", no switching of the transmitter-core minor aperture would have occurred. The transmitter path would then present a virtual short circuit to the drive current. No current would be steered to the receiver core, in this instance. It would therefore remain in the "clear" or "zero" state, since it was cleared during $\rho 1$. Interval I3 primes the minor apertures of both transmitter and receiver cores for subsequent interrogation during interval I4. Note that the transfer occurs between the *minor* aperture of the transmitter and the *major* aperture of the receiver.

The transfer technique just described has one major drawback, and that is an excessive steer-loop voltage drop of approximately 6 to 8 v per stage which severely affects "back transfer" and limits the number of register stages. Since this voltage drop is multiplied by the number of stages, the input voltage requirement becomes
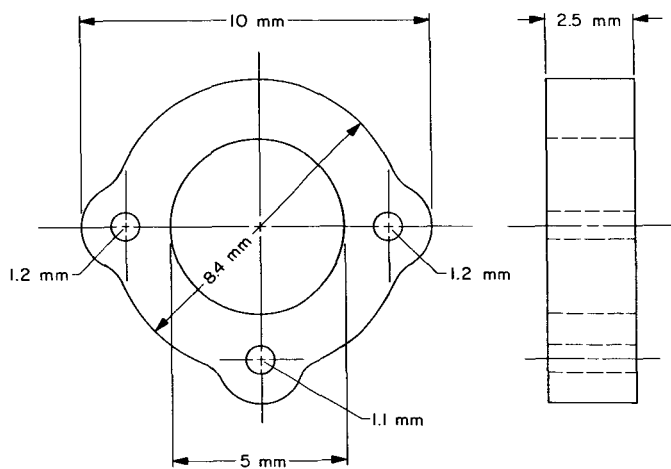
Fig. 2. SIEMENS transfluxor

Table 1. Phasing table

Interval	I1	I2	I3	I4	I5	I6	I7	I8
Register	$\phi 1$ Prime	$\phi 2$ Read	$\phi 3$ Prime	$\phi 4$ Read	$\phi 5$ Clear	$\phi 6$ Set	$\phi 7$ Prime	$\phi 8$ Read
Buffer	$\rho 1$ Clear	$\rho 2$ Set	$\rho 3$ Prime	$\rho 4$ Read	$\rho 5$ Prime	$\rho 6$ Read	$\rho 7$ Prime	$\rho 8$ Read

prohibitive for devices of greater than six stages. The transfer from *minor* aperture to *minor* aperture was thus adopted (Fig. 4), because this offered several distinct advantages: Less energy is required for the transfer, since the magnetic path is considerably shorter. Less flux gain is required, with a resultant reduction in turns ratio. Fewer net turns are required, simplifying fabrication. Finally, the steer-loop voltage drop is decreased to approximately 1.5 to 2.0 v per stage. One problem is induced however. Flux output increases monotonically with current, until saturation. When transferring from minor to minor, prime-current amplitude becomes extremely critical. Once the prime current exceeds the threshold necessary for saturation, the output flux begins to decrease. Over successive prime-read cycles, it decreases to about 60% of its maximum value. Multiple prime-read cycles are initiated in order to correct an existing system error. The integrated flux output (integrator time constant $\tau = RC = 10.99 \ \mu sec$) during repetitive prime-read cycles is shown in Fig. 5. By designing the transfer loop to function at a flux level 40% below maximum, this problem can be overcome. Nominal switching of the transmitter core is thereby faster. If the peak flux is available (as it is on the first prime-read cycle), the switching occurs more slowly. In either case, the transfer is completed properly.
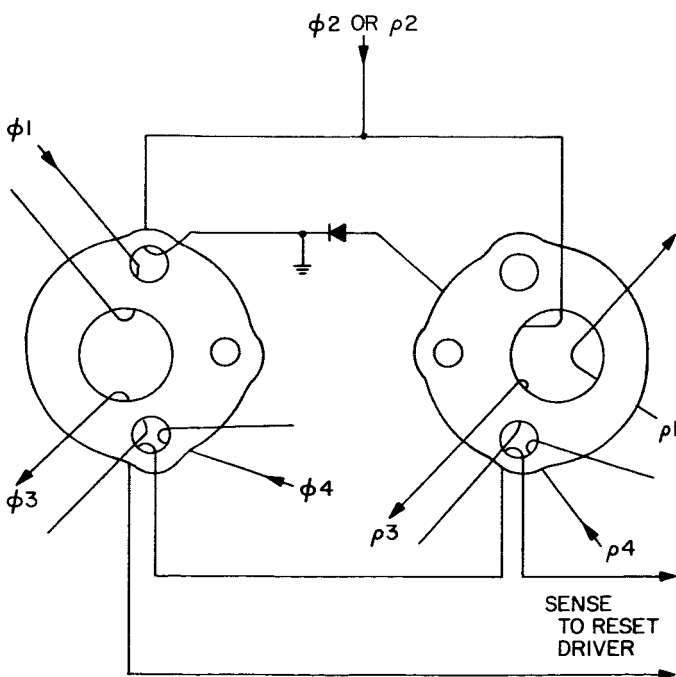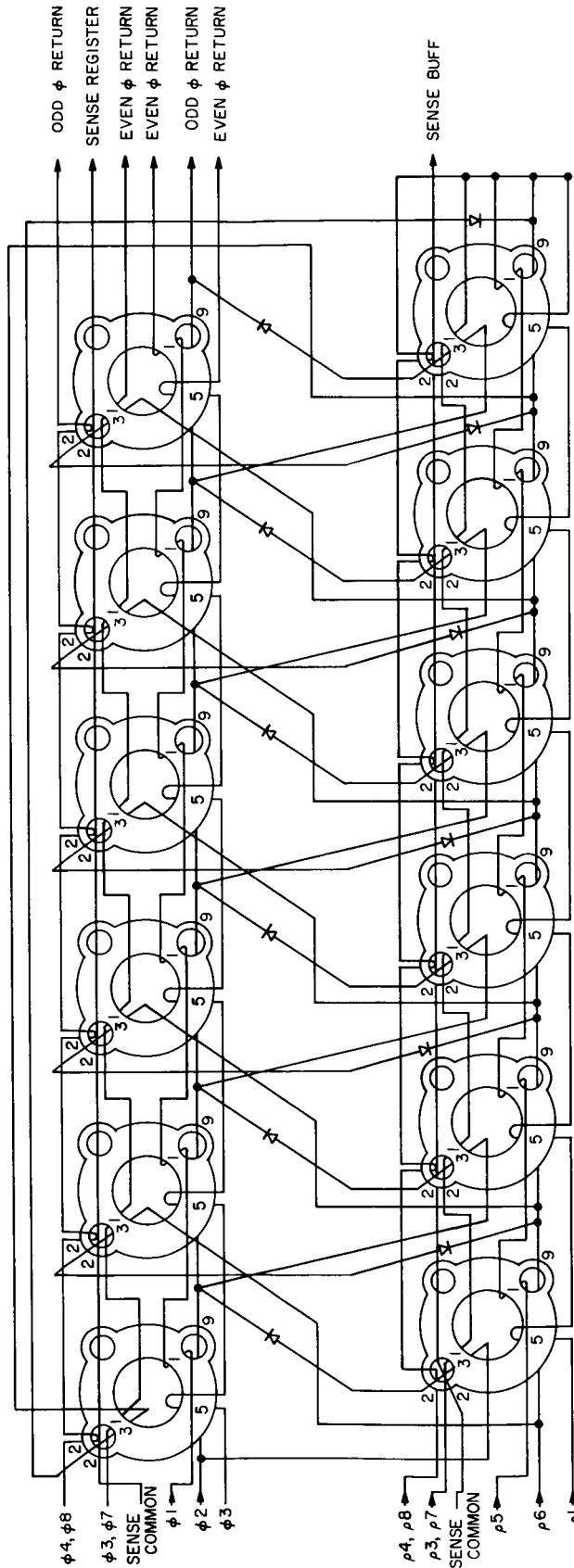
In order to avoid compensating circuitry, it is imperative that the remaining drive currents not be especially critical. Both pulse amplitude and pulse shape may be expected to vary $\pm 25\%$. The nominal drive-current amplitude should be 33% above the current required to ensure complete switching. Wave shape is somewhat more difficult to define. Excessively fast rise time will transfer erroneous "ones", while very slow rising pulses will drop existing "ones". An operative corridor is thus defined.

Project time limitations did not permit extensive investigation of all drive-current margins. Partial results are included in Section VI of this Report.

A feedback network is required for any shift register used as a timekeeping device. A two-tap linear network is most common. For application in the NEDEC scheme, the exclusive-or must be formed and transferred nondestructively. Then, comparison must be made between the receiver core and the exclusive-or logic pair. Stated differently, the exclusive-or must be formed twice: the first formation generates and stores the logical sum; the second formation generates the logical sum, simultaneously comparing it with the sum previously stored in the receiver core. Two transfluxors form the logic pair. They are cleared during I1. At I2 time, information is transferred from the selected register stages, and is stored simultaneously in the corresponding buffer stages and in the logic pair. Phases I3 and I4 prime and interrogate the logic pair to verify valid transfer. Any discrepancy is detected at the difference detector coincident with the error data from the register to buffer shift. Phase I5 primes the logic pair. At I6 time, current is steered through both cores of the logic pair. The steer windings are routed such that the modulo-2 sum is generated at the output diode (Fig. 6).

Toroids are illustrated for simplicity. A trial unit, using 180-mil toroids, has been tested successfully. In practice, the windings thread the minor aperture of the Siemens transfluxor. Although this has not been tested, no unusual difficulty is anticipated. The final prime occurs at I7. The exclusive-or interrogation at I8 is illustrated in Fig. 7. Logic notation is given in Fig. 8.

Note that the modulo-2 generator requires three diodes, and the verification circuit requires seven diodes. The two networks may be combined with a saving of

Fig. 3. Shift scheme

ODD φ RETURN
SENSE REGISTER
EVEN φ RETURN
EVEN φ RETURN
ODD φ RETURN
EVEN φ RETURN

SENSE BUFF

NOTES:

REGISTER INITIALIZE NOT SHOWN.
BREADBOARD USES STEERING SWITCH
RESET CURRENT TO INITIALIZE.
(FIVE TURNS ON CORE ONE, FOR SET
FIVE TURNS ON CORES TWO-SIX, FOR RESET)
CIRCULATION OF A SINGLE "ONE" OR A SINGLE "ZERO"
IS AFFECTED BY INTERCHANGING THE INPUT
AND OUTPUT CONNECTIONS.

DIODES IN690
WIRE 36 ga SOLDERIZE

φ4, φ8
φ3, φ7
SENSE COMMON
φ1
φ2
φ3

ρ4, ρ8
ρ3, ρ7
SENSE COMMON
ρ5
ρ6
ρI
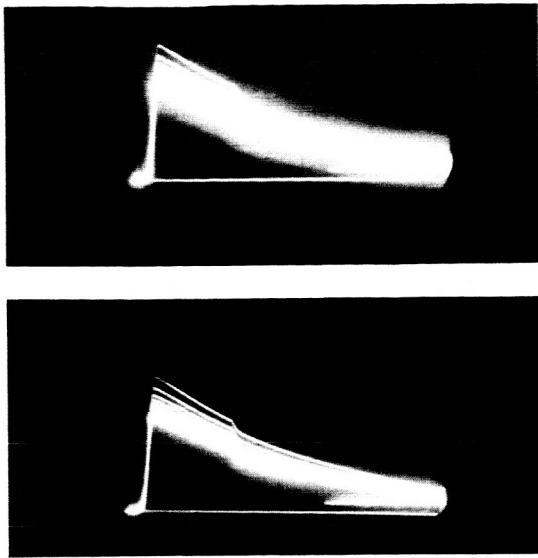
Fig. 4. NEDEC shift register

6

Fig. 5. Integrated-flux-output amplitude during repetitive prime read cycles
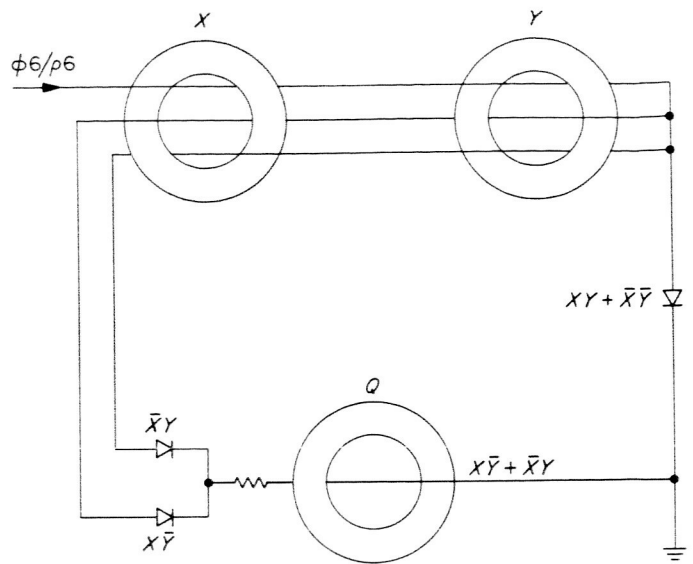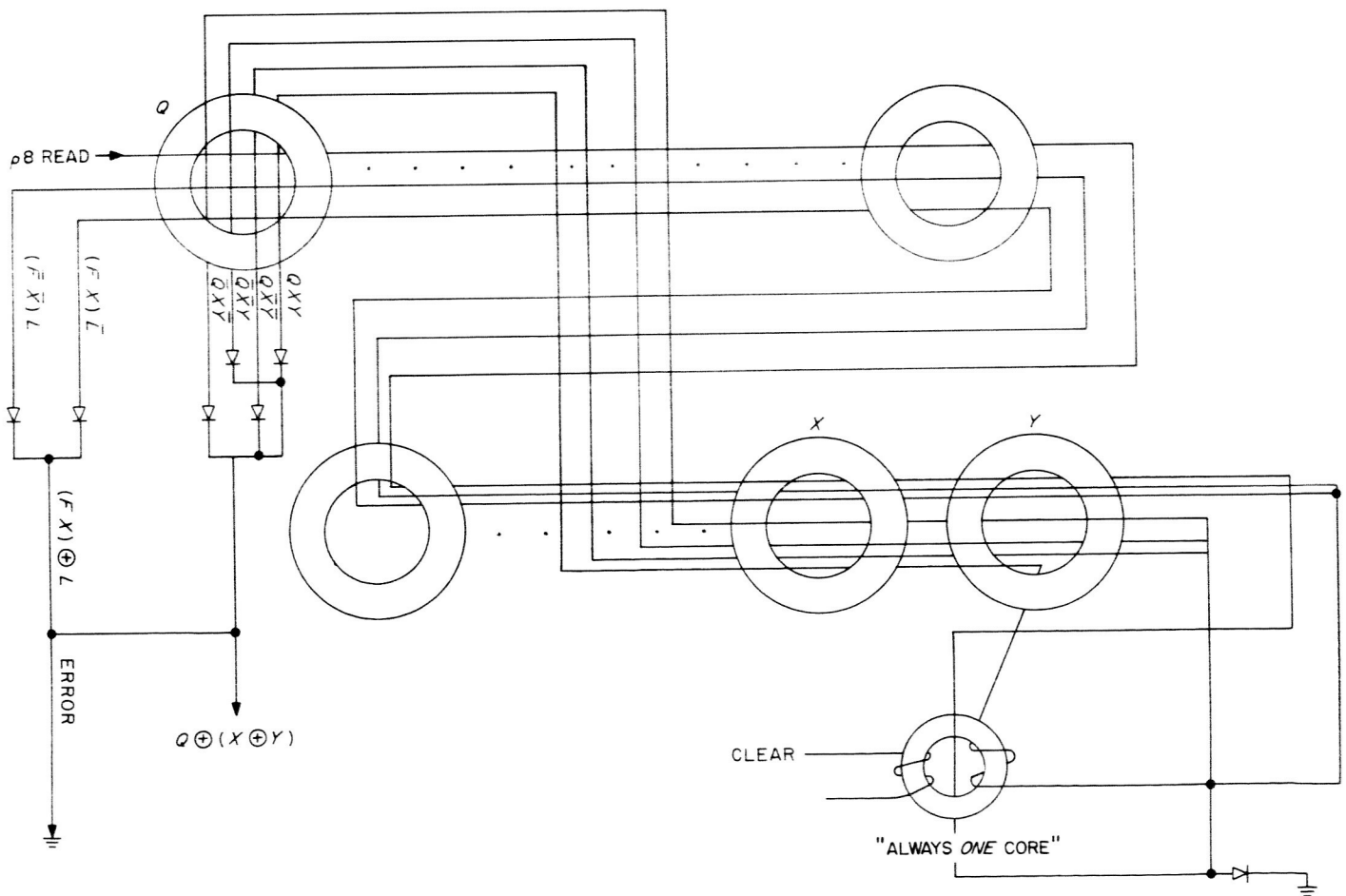

Fig. 6. Portion of feedback logic

Fig. 7. Feedback-logic comparison cycle

three diodes. The logical analysis is omitted. Operating with the minor apertures could present noise problems that could render the combined network marginal. Testing is required to verify this.

B. Clock-Driver Circuitry

The clock-driver circuitry employs conventional techniques; therefore, less detail is required to describe it.
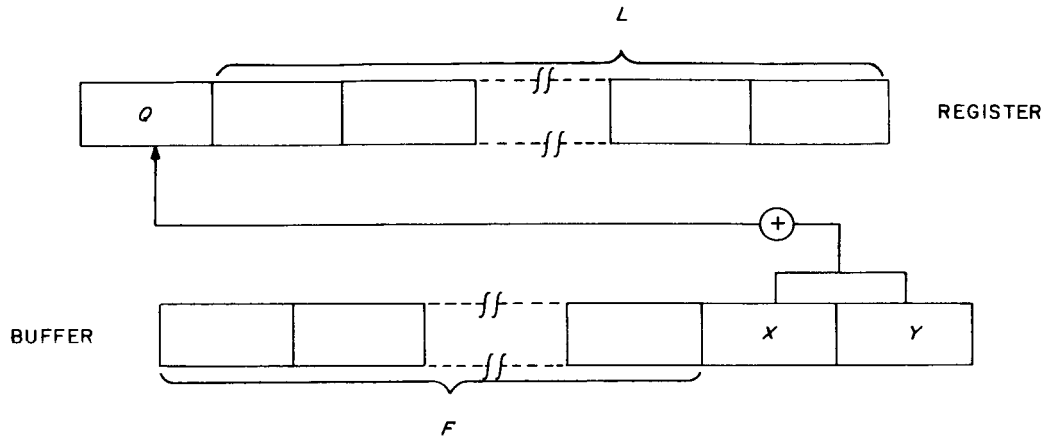
Shift Process

Shift: register ⟶ buffer

Compare: all register stages
            with all buffer stages.

Clear: register

$\text{ERROR} = (Q\,L) \oplus (F\,X\,Y)$

where $Q\,L = \sum$ of voltages of
the register, etc.

and

$\oplus$ implies a difference
voltage between register
and buffer.

⎱ register
⎰ to
⎱ buffer
⎰ shift

Shift: buffer ⟶ register

Compare: buffer with register
            $(F + X$ with $L)$.
            Q with $\oplus$ Logic Output

$\text{ERROR} =$

$[(F\,X) \oplus L] + [Q \oplus (X \oplus Y)]$

⎱ buffer to
⎰ register shift

where:

$Q =$ first register stage

$L =$ all register stages except Q

$Y =$ last buffer stage

$X =$ buffer stage used in conjunction
      with Y to form the exclusive-or

$F =$ remaining buffer stages excluding
      the exclusive-or stages

Fig. 8. NEDEC logic notation

A crystal-controlled oscillator is used as a frequency source. Two conventional blocking oscillators are connected so that even-numbered inputs are regenerated by the first blocking oscillator, and odd-numbered inputs are regenerated by the second blocking oscillator. These outputs are labeled α and β, respectively, and they drive the α and β input lines of an eight-way current-steering switch (Fig. 9). The switching cores shown furnish the select function by alternately triggering each blocking oscillator.

The two current-steering switches drive the register cores and the buffer cores, respectively. The serial arrangement was chosen for convenience in breadboarding. Alternatives and their failure modes are considered later. Outputs from the first switch thread the register cores only. Similarly, outputs from the second switch thread the buffer cores only. The loads on the first switch are returned to the inputs of the second switch rather than to ground. Both switches operate synchronously, recycling to the initial interval after four or eight pulse intervals. For a normal cycle, the eighth output pulse will automatically reset the switches to Interval 1. In event of system errors, the switch is reset to Interval 1 if the error is detected during Interval-4 time, and to Interval 5 if the error is detected during Interval-8 time. A typical switch is illustrated in Fig. 10. Actual turns ratios are dependent upon the expected load, desired pulse shape, etc.

C. Error-Detection and -Correction Circuitry

The error-detection circuit consists of a sense line to link all transfluxors in the shift register and of a pair of reset drivers to recycle the current-steering switches to
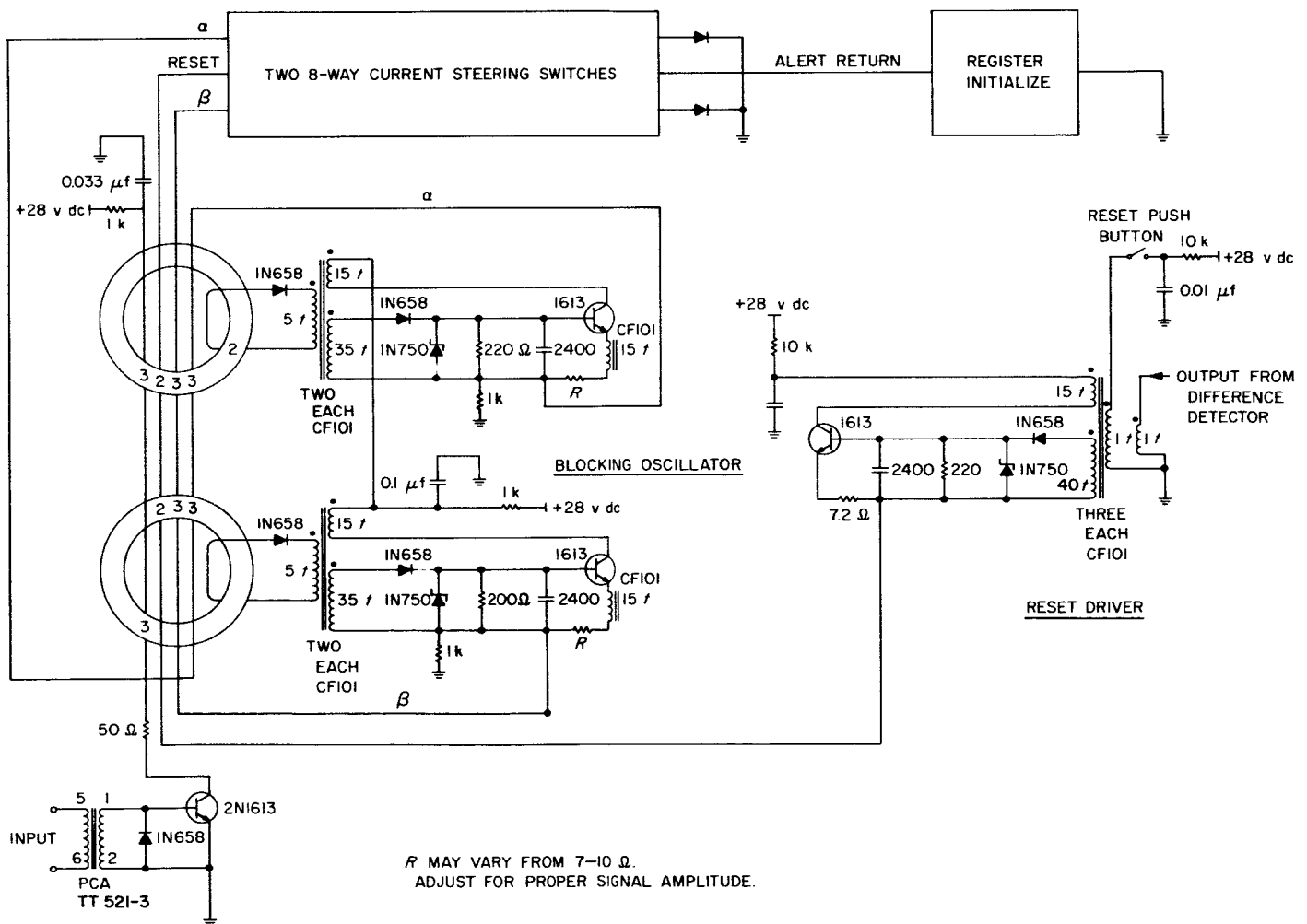

Fig. 9. Drive circuitry

180-MIL CORES

SOLENOID WIND 15 t
SECTOR WIND 13 t
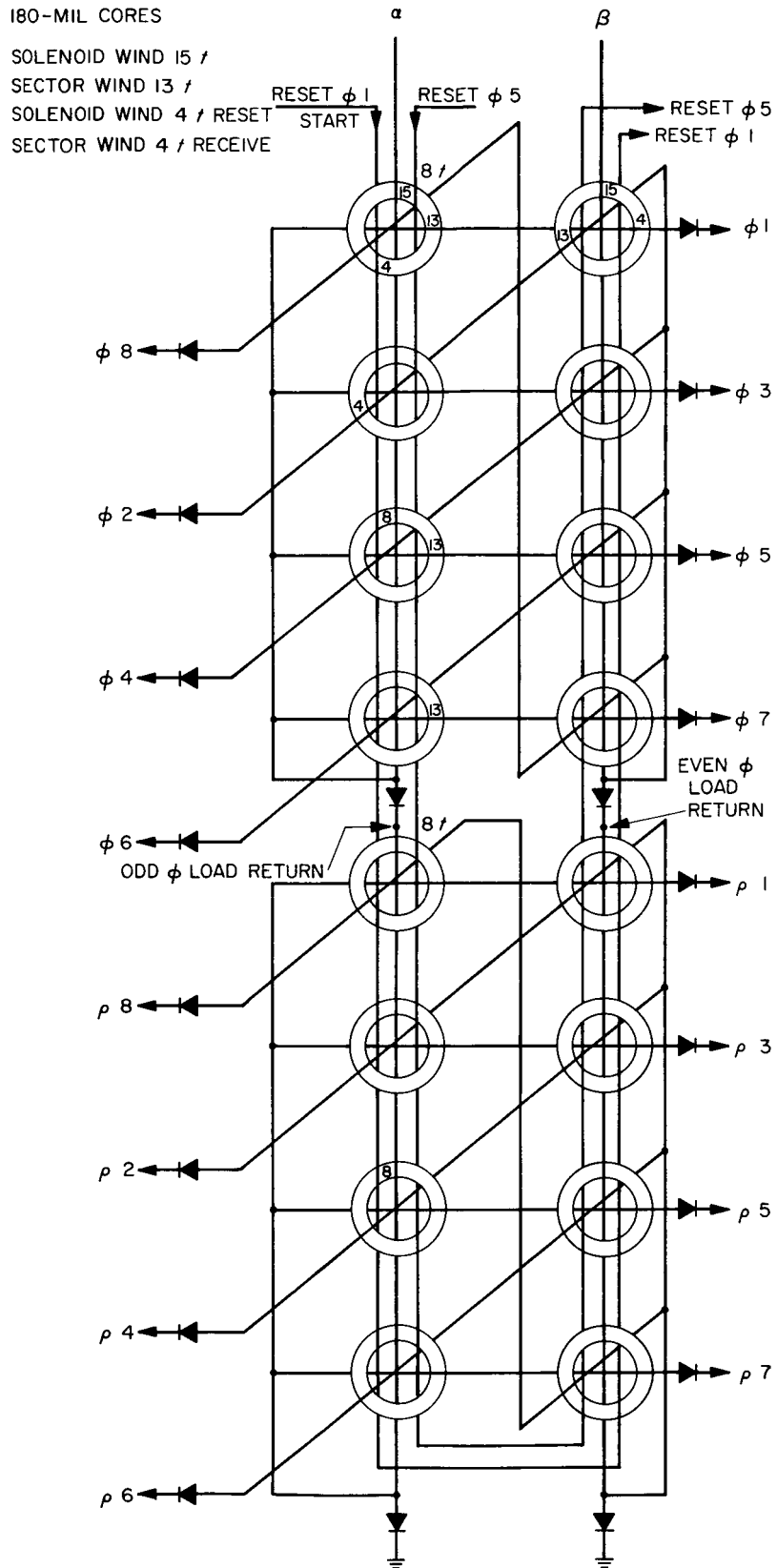SOLENOID WIND 4 t RESET
SECTOR WIND 4 t RECEIVE

Fig. 10. Two 8-way current-steering switches

the appropriate interval. A coupling circuit is required between the sense line and the reset drivers. As the sense output is bipolar, the coupling circuit must accommodate this bipolar input and trigger the reset drivers, in either case. Design of the coupling circuit must consider residual- and shuttle-noise rejection.

VII. CIRCUIT DESIGN

A six-stage circulating register was constructed. To facilitate fabrication and testing, several substitutions were made in the system already described. Two Rese Corporation Pulse Generators were connected in tandem to provide an eight-phase clock driver in lieu of the current-steering switch. The register wiring was modified so that each drive current energized the proper lines in both register cores and buffer cores, thus avoiding sixteen distinct clock current drivers. Considerable flexibility was gained because each drive current could be individually adjusted as to amplitude, rise time, and fall time. This control is essential for temperature testing. The modulo-2 summing logic was replaced with a closed-loop recirculation path. The reset drivers were disabled, and the sense line outputs were qualitatively evaluated with an oscilloscope.

Any chosen information word could be pre-wired into the register by appropriately routing a start wire, which is energized by the system start pulse. This start pulse must occur between I8 and the following I1.

Of prime interest is the evaluation of shift characteristics; i. e., the "ones" build-up or dropout, zero noise, operating frequencies, voltage drops, etc. These characteristics must be examined with respect to variations in drive-current parameters. Finally, a set of operating characteristics over a temperature band must be determined.

The full shift cycle from register cores to buffer cores, and conversely, was tested repeatedly at room temperature. After loading the register, the initial "one" shift transferred more flux than subsequent shifts. The transfer characteristics stabilized at an acceptable level (gain/stage > unity), as shown in Fig. 11. Two worst-case information words were loaded into the register and circulated. The first, a single "one" (100000), was circulated overnight without dropout; the other, a single "zero" (011111), was also circulated overnight without
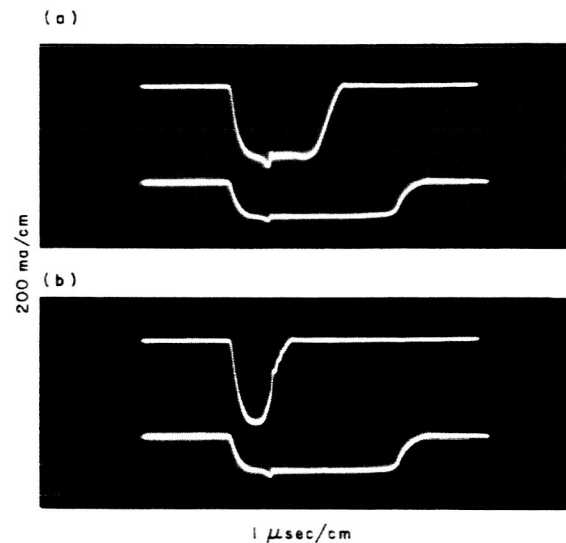

Fig. 11. Transfer wave shapes: (a) initial flux transfer; (b) subsequent flux transfers

"ones" build-up. This was done using a nominal 0.5-amp, 6-μsec current pulse on all eight drive lines. Switching was found to be complete in 2 μsec in all cases, including prime, transfer, and interrogation phases.

Typical drive-current wave shapes are shown in Fig. 12. A sharp rise, faster than 1.75 μsec was found to introduce shifting errors. A 2.0-μsec rise time should provide adequate margin. Since switching is complete at 2.0 μsec, a net current pulse of 2.5 μsec is ample. This places a 400-kc theoretical limit on the pulse rate, which is equivalent to a shift rate of 50 kc. Using the nominal 6-μsec pulse, the system operated up to 12.5 kc, or an equivalent shift rate of 156 shifts/sec before failure at room temperature, well above design requirements.

Receiver-core wave shapes are shown in Fig. 13(a). The upper trace shows the current steered into the receiver core after insertion, in turn, of a "one" and
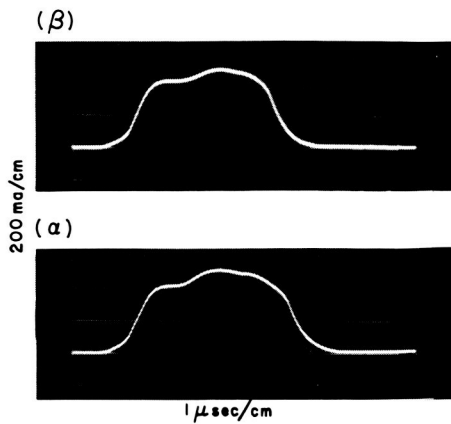
(β)

(α)

200 ma/cm

1 μsec/cm

Fig. 12. Typical drive-current wave shapes
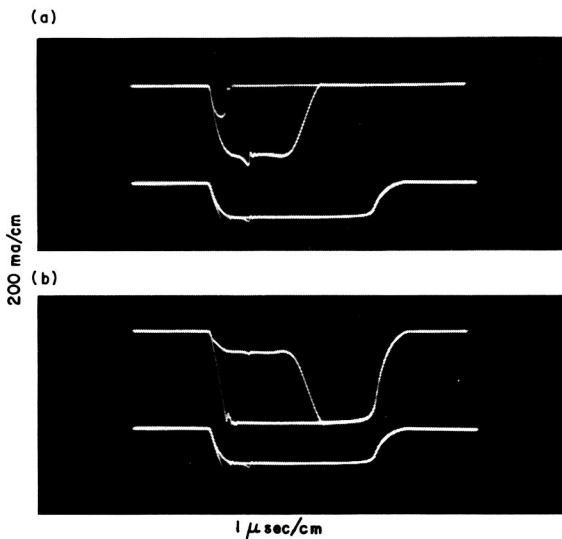
(a)

(b)

200 ma/cm

1 μsec/cm

Fig. 13. Current-steering wave shapes

a "zero". Both currents are proportional to the flux switched in the receiver and transmitter cores. The integrated area under each is indicative of the 1-to-0 transfer ratio. The results are superimposed. The full pulse is shown immediately below. Figure 13(b) shows the corresponding wave shapes for the transmitter core. The 1-to-0 ratio is dependent upon the switching time, steer-loop winding ratios, diode-voltage drop, and respective path lengths of transmitter- and receiver-core legs. A 4-to-1 differential in 1-to-0 ratio was found between the minor apertures, the larger diameter minor aperture being superior.

A two-turn solenoid winding links all the register cores. A second, similar winding links all the buffer cores. This pair serves as the system sense circuitry. With the two windings connected (Fig. 3), an oscilloscope

may be used in place of the reset driver to analyze the sense signal variations. Figure 14 shows the residual noise level with all "zeros" circulating. Figure 15 shows the nulled sense output while circulating a single "one". Similarly, Fig. 16 shows the nulled sense output, with five "ones" circulating. If the connection between the register and buffer windings is broken, the photographs shown in Figs. 17 and 18 are obtained. A signal-to-noise ratio of 13 is defined in Fig. 19, leaving an acceptable margin for noise suppression in the error-correction circuit. The sense output for the complete shift cycle is given for reference in Fig. 20.

Evaluation of register performance with respect to temperature was completed after some difficulty. Drive currents above 525 ma were unobtainable because of voltage limiting of the current drivers. An attempt was made
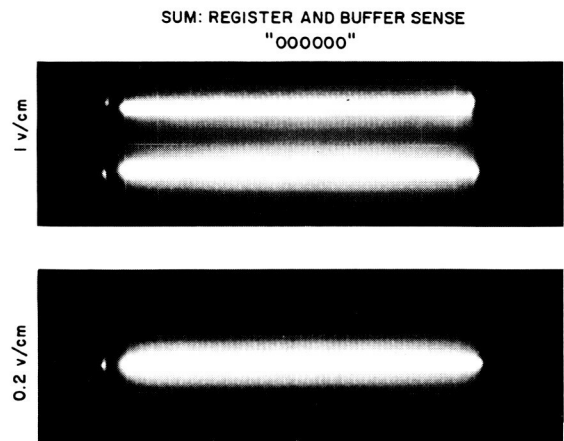
SUM: REGISTER AND BUFFER SENSE
"000000"

1 v/cm

0.2 v/cm

Fig. 14. Sense circuit: zero noise

SUM: REGISTER AND BUFFER SENSE
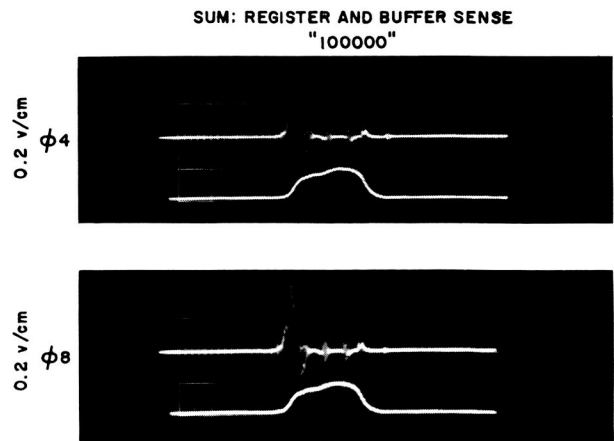"100000"

0.2 v/cm   φ4

0.2 v/cm   φ8
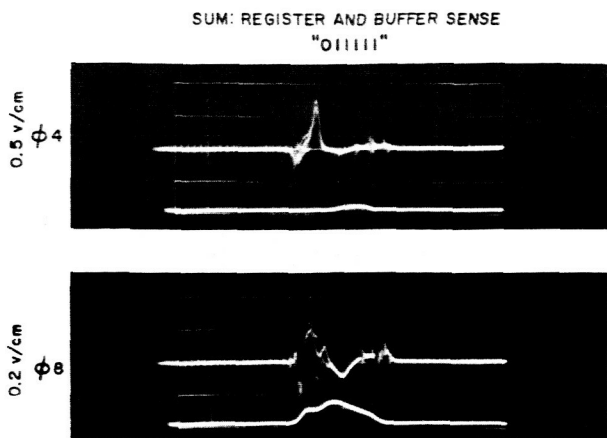
Fig. 15. Sense circuit: data cancellation

Fig. 16. Sense circuit: data cancellation
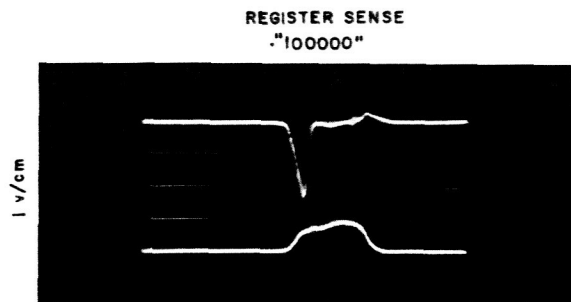
Fig. 17. Sense circuit: uncancelled output magnitude

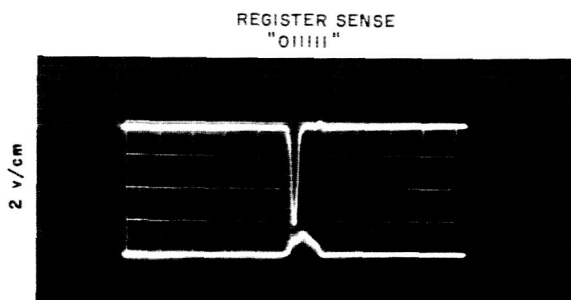Fig. 18. Sense circuit: uncancelled output magnitude

Fig. 19. Sense circuit: signal-to-noise determination
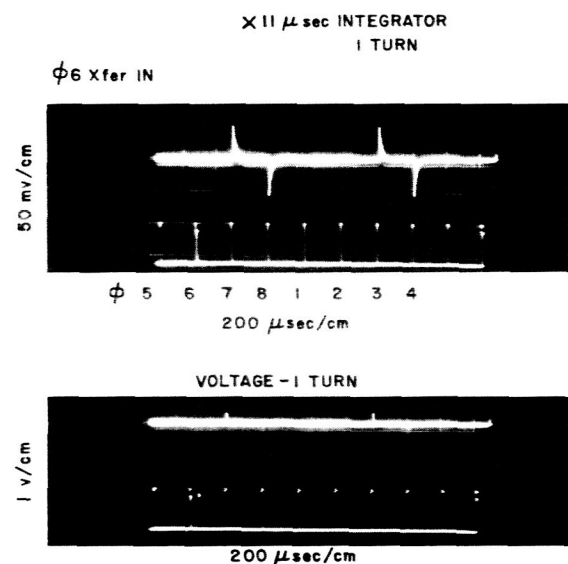
Fig. 20. Sense circuit: complete shift cycle

to increase the pulse amplitude by increasing the pulse-generator supply voltage from a nominal 28 to 40 v dc. Voltage limiting still occurred, but at a slightly increased amplitude of 650 ma. At this supply level, the clock oscillator was overstressed, and further amplitude control was impractical.

Register shifting ability, being independent of the error-detection phases, depends only on Intervals I1, I2, I5, and I6. For simplicity, only these were included

in the margin checks. Successful operation of the register was attained over a temperature excursion of −20 to +100°C without degradation of signal-to-noise ratio at nominal drive currents. The resultant temperature margins for current drivers 1, 2, 5, and 6 at 28-v dc nominal supply voltage are listed in Table A-1 included in Appendix A. The HIGH and LOW readings given represent the actual drive-current amplitude range for proper register operation. Drivers 5 and 6 were later operated at 40 v dc, and the higher results are included in Appendix A under Table A-2. Time did not permit

modification of all four drivers, but it may be assumed that similar results would be obtained. Note that the highs are *not* true maximum values of register operation, but the limiting values of the current drivers, the results of which are plotted in Figs. 21 and 22. A list of system characteristics is also included in Table A-3.

The above measurements were made with the following considerations:

1. LOW reading of Interval 5 yielded HIGH "zero" transfer (approximately 50% of "one" transfer) without errors in shifting.

2. Nominal reading of Interval 5 is based on a peak current of 500 ma.

3. All drive currents have a rise time of 2.0 μsec.

4. Error voltage is measured with all drive currents set at 500-ma peak. At varying temperatures, the

notch current (voltage limiting value of the current drivers at 40 v dc) may have varied. These readings are therefore empirical only. The integrated error signal was fairly constant over the temperature range (Table 2).

Table 2. Integrated error voltage

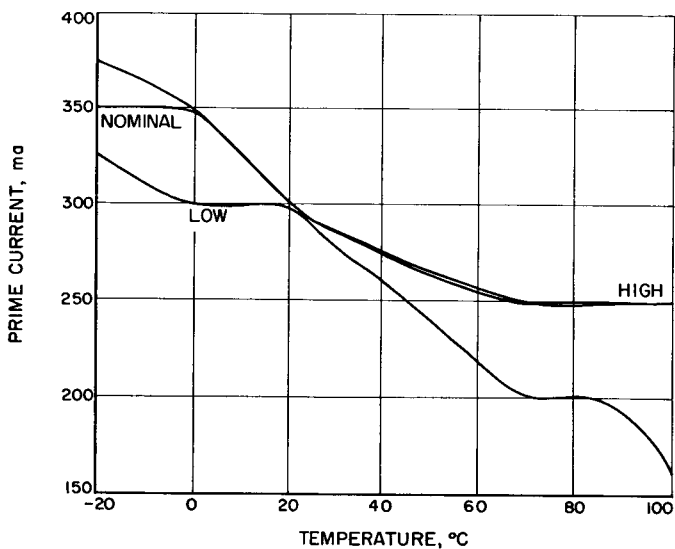| Temperature, °C	Output, v-μsec
100	0.55
85	0.44
70	0.385
40	0.275
20	0.275
0	0.240
−20	0.00

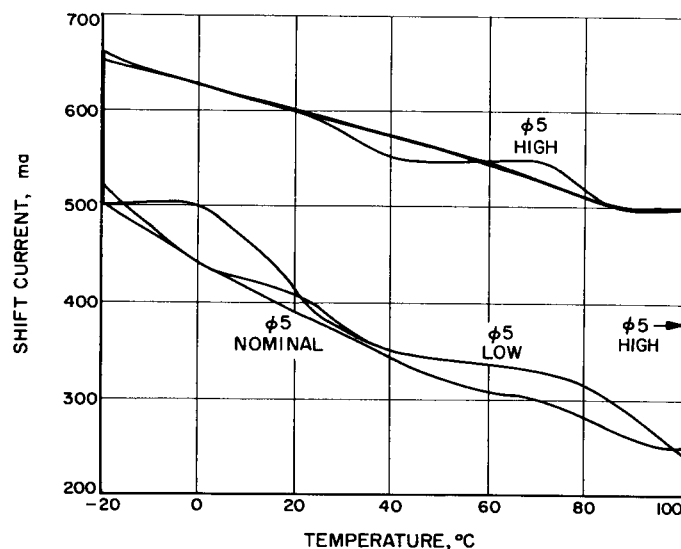**Fig. 21. Temperature characteristics**

Fig. 22. Temperature characteristics

VIII. EVALUATION AND CONCLUSIONS

The NEDEC system is a fundamentally simple design approach to an otherwise complicated logic-design problem. The inherent reliability of NEDEC is considerably higher than for conventional parity check schemes, but the design approach outlined here requires some additional clarification.

The philosophy underlying the design of NEDEC is that the system be immune to transient failures. Such failures most likely result from substandard driving functions. Errors introduced are assumed to be non-compensatory:

1. Multiple errors (that null the error signal) *cannot* be generated during the shift. "Ones" may be transferred as "zeros" and conversely, but *not* both simultaneously, since drive currents at a given time are correspondingly high *or* low but *not* both.

2. The winding configuration and the ferrite geometry preclude the possibility of dropping a "one" from the transmitter and transferring a "zero" to the receiver, regardless of the drive-current amplitude. The proof is omitted here.[1]

A set of failure modes is also inherent in the current-steering switch. Input currents to the switch are directed to the proper load. Failure of the reset to fully initialize the switch to $I1$ or $I5$ may cause an incorrect interval sequence. This will result in a detectable shift error. A weak input current may fail to step the switch. The shift operation is not affected, although a timing

[1]See Stanford Research Institute Report No. 1, Project 3696, Sec. III.

error is introduced. Note that during any correction cycle timing errors are similarly introduced. Should a low input current fail to be properly steered and thereby clear the switch to the "all-zero" state, a catastrophic failure would result, which is beyond the scope of the system to correct. Any input pulse to the current-steering switch that is adequate to step the switch will also be adequate to operate the register. Thus, any read pulse obtained will be sufficient to ensure interrogation and to detect any error present.

Serial operation of two current-steering switches has several interesting aspects. Probability of an "all-zero" catastrophic failure is reduced, since both switches must be completely cleared. Clearing only one switch will result in a detectable error and will reset both switches. A second advantage is gained. Each core set is driven by a semi-independent switch. Error-detection probability is increased by two separate lines performing the same functions in each respective core set. Thus, if an α phase is substandard, the corresponding β phase may suffice. Again, these advantages must be weighed against the increased complexity.

Finally, the NEDEC system is a power consumer. One-half ampere drive currents with 50-v drops (for 18 stages) consume upward of 25 w. The duty cycle, however, is considerably less than unity. The specific percentage depends upon the shift rate.

Feasibility of the NEDEC concepts has been sufficiently established. Much additional effort is required now to refine these concepts to yield a practical design capable of incorporation into a spacecraft system.

APPENDIX A

Supplementary Data

INPUT

PRIME ϕI
TRANSMITTER

PRIME ρ5
TRANSMITTER

STEER ϕ2

STEER ρ6

PRIME ϕ3,ϕ7;ρ3,ρ7
RECEIVER

READ ϕ4,ϕ8;ρ4,ρ8
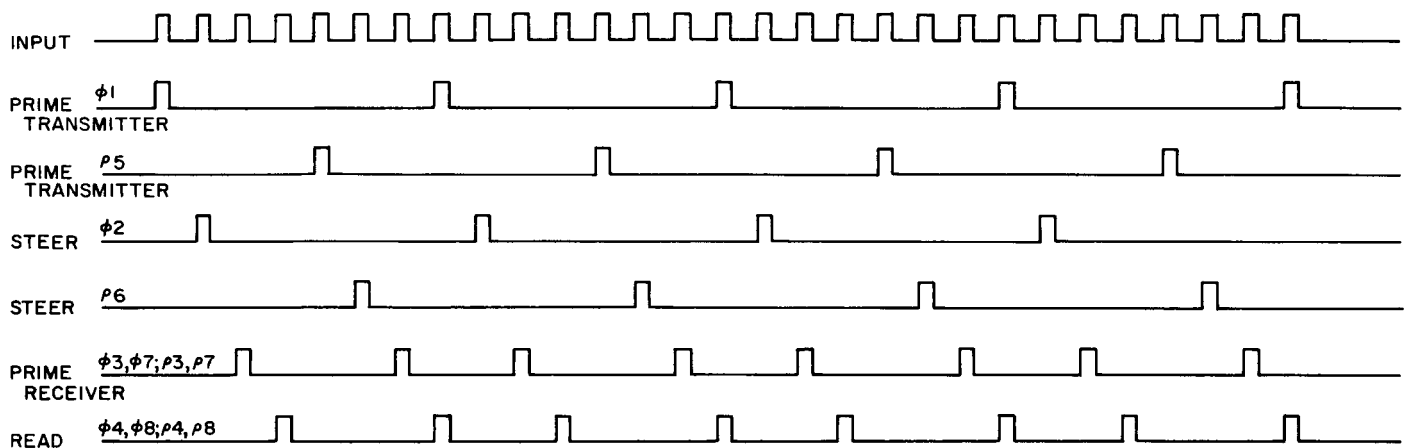
NOTE:
  ϕ WINDINGS THREAD REGISTER CORES ONLY. *
  ρ WINDINGS THREAD BUFFER CORES ONLY. *
     MULTIPLE PHASES ON A SINGLE WINDING ARE OBTAINED BY INTERCONNECTION OF RESPECTIVE STEERING-SWITCH OUTPUTS.
* STEER WINDINGS THREAD BOTH REGISTER AND BUFFER CORES.

Fig. A-1. Timing reference diagram

Table A-1. Temperature margins: Drivers 1, 2, 5, 6

Temperature, °C	Interval 1		Interval 2		Interval 5		Interval 6	
	HIGH ma	LOW ma	HIGH ma	LOW ma	HIGH ma	LOW ma	HIGH ma	LOW ma
−20	315	290	580	540	325	300	525	500
0	300	270	550	470	280	260	510	440
20	270	250	500	400	280	260	480	440
40	260	240	480	400	270	260	450	360
70	250	225	430	330	250	220	425	300
85	230	215	430	300	230	200	400	300

Table A-2. Drive margins[a]

Interval 5			Temperature, °C	Interval 6	
HIGH ma	NOMINAL ma	LOW ma		HIGH ma	LOW ma
300			20	600	410
	300			600	390
		300		600	390
275			40	550	340
	275			575	340
		260		575	350
250			70	550	300
	250			525	300
		200		525	330
250			85	500	270
	250			500	270
		200		500	300
250			100	500	250
	250			500	250
		160		500	340
350			0	625	440
	350			625	440
		300		625	500
375			−20	660	520
	350			650	500
		325		650	500

[a] Register failure occurred at −31°C at nominal drives.

Table A-3. System characteristics

Pulse Amplitude	450–500 ma
Pulse Width	5–6 μsec
Rise Time	1.50–2.0 μsec, minimum
Turns Ratio	transmitter/receiver = 9/3
Prime NI	0.5-amp turns
Read NI	1.0-amp turns
Clear NI	2.5-amp turns
Sense	2 turns/core
Transfer Order	minor aperture 2 to minor aperture 1
Interrogate Order	minor aperture 1 compared with minor aperture 1
Clear Drive	through major aperture
Voltage	+28-v dc
Total Steer Loop Drop	16 v
Total Stages	6 (breadboard only)
Cores	Siemens & Halske B64 715 R 402 Transfluxor
Diodes	2 per stage—1N690
Wire	36 gauge—Soldereze

APPENDIX B

An Elementary Magnetic-Core-Diode Circuit[1]

A magnetic core and diode combination, which functions as the basic element of a shift register, is described. Circuit diagrams of several logic mechanizations and shift registers are also described. The basic circuit uses low-drive 0.080-in.-OD ferrite memory cores at shifting rates up to a megacycle, with a power utilization of 1 mw/stage/kc.

The basic shift-register configuration is depicted in Fig. B-1. To explain the transfer operation of this shift register, the super-position of the volt-second ampere-turn curves (Fig. B-2) is used. These curves are the dc B-H loops modified by the number of turns in the transfer loop.

The transfer circuit uses parameters determined empirically. The output (transmit) winding on each core is 10 turns, and the input (receive) winding is 4 turns. The effective flux of a transmitting core is 250% that of the receiving core, while the coercive force required to switch the transmitting core is 40% of that required to switch the receiving core.

When a current is applied to the coupling loop with the a priori condition that the receiving core contains a "zero" $(-B_r)$, the action in the coupling loop is dependent upon the information state of the transmitting core. If the transmitting core contains a "zero" $(-B_r)$, the current causes a flux change in the core along the reversible portion of the B-H loop from $-B_r$ to $-B_s$,

which generates a small noise-voltage dVo (disturbed zero voltage). If dVo does not exceed the forward barrier voltage of the diode, then no current flows through the input winding of the receiving core, and no flux change occurs in the receiving core. If the transmitting core contains a "one" $(+B_r)$ when the current is applied, only that portion of the applied current necessary to switch the transmitting core back to the "zero" state flows through the output winding. The remainder of the current flows through the input winding of the receiving core and the diode. This current division continues until the transmitting core is reset to the "zero" $(-B_r)$ state, and then all of the current flows through the output windings of the transmitting core (as in the case of a zero transfer) for the remainder of the current pulse.
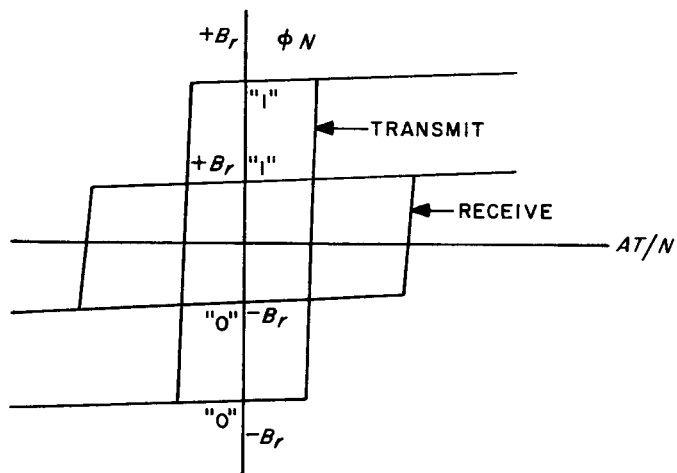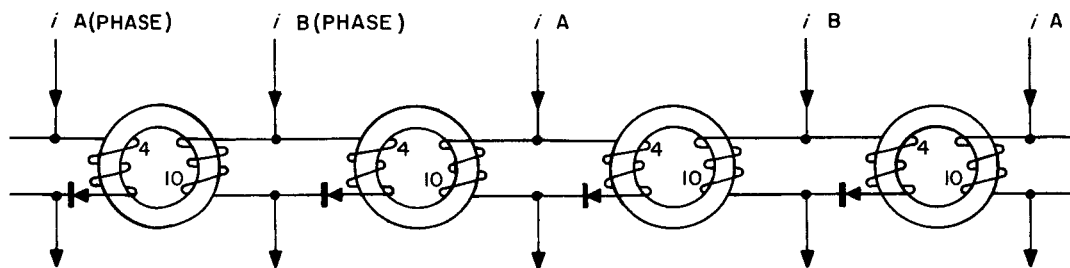

Fig. B-2. B-H diagram

Fig. B-1. Winding scheme

If the applied current pulse is above a certain minimum value (200 ma for the circuit shown), then during switching of the transmitting core, sufficient current is steered through the receiving core to set it to the "one" $(+B_r)$ state. The current division process can be considered as the superposition of almost equal currents in each leg, plus a circulating current. The voltage across the transmitting-core output winding equals the sum of the voltages across the receiving-core input winding and the diode forward drop during transfer of a "one." The two cores involved are therefore constrained to switch at the same speed. Because of the greater number of turns on the output winding, and the equivalent core resistance is a function of N^2, the maximum division of current would be in the ratio of 6 to 1. The forward drop of the diode modifies this ratio because the voltage of the output winding must overcome this counter voltage. The division ratio then becomes more nearly 4 to 1.

Waveforms of the currents and voltages during a "one" transfer are depicted in Fig. B-3.

The basic circuit, together with two-phase current-pulse sources, provides a means for mechanizing a two-core-per-bit unidirectional shift register. Referring to Fig. B-1 it can be observed that from a previous A phase, core 1 will have been set to zero. Let core 1 be set to "one" by the next A phase. Then at the following B phase, core 2 will be set to "one" as core 1 is cleared to "zero." On the succeeding A phase the "one" in core 2 will be transferred to core 3, and core 2 will be cleared.

When a "one" is being cleared from a core, the voltage developed across the input winding of that core is of such polarity that the input diode is forward biased. It would seem that a current flow could be established in the input loop which would set the preceding core to the "one" state. There is a voltage v developed across the 10-turn output winding of any core being cleared to "zero" which is identically equal to the voltage developed across the 4-turn input winding of the following core plus the forward drop of the diode. The voltage v developed across the input winding of the core being cleared is $0.4v$. This $0.4v$ is obviously insufficient to overcome the diode barrier voltage, and develop v across the output of the previous core, which would be necessary to set that core. This impedance mismatch in the reverse direction allows one core to drive more than one following core. It was found empirically that a 15-turn output winding would just drive three receiving cores, which indicates that the minimum turns ratio of 5-transmit-to-4 receive will overcome the coupling loop losses. Some overdrive in the form of more output turns should be added to give a safety factor. Fig. B-4 shows the fan-out arrangement.

To provide additional assurance that the receiving cores will not set the transmitting core when they are cleared, the transmitting output turns should be at least $7N$, where N is the number of receiving cores.
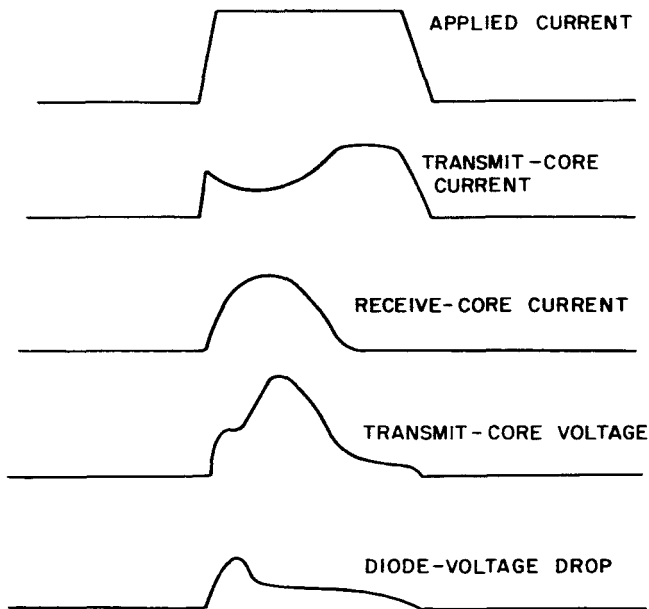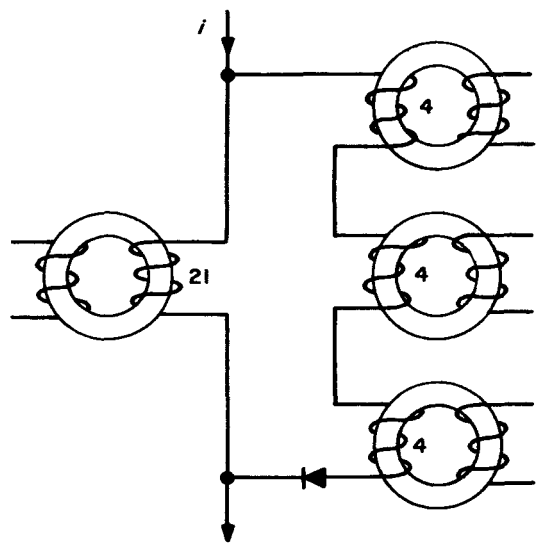

Fig. B-3. Typical wave forms

Fig. B-4. Fan-out circuit