MINIATURE SPACE-BORNE MEMORY

Contract NAS5-9518

UNIVAC Research Operations, Blue Bell, Pa.

Monthly Technical Report No. 2 February 9, 1965

Period Reported: January 4, 1965 to January 31, 1965

Summary:

The development work is on schedule as shown in the planning chart included with last month's report. High temperature tests were made on a number of adhesives which had been considered for use in the construction of the memory stack. These tests showed, contrary to manufacturer's data sheets, that the adhesive systems were not satisfactory for 48-hour storage at 150°C. New adhesive systems will be tested. Additional protective metallic platings over the magnetic thin film plated wire will be tested. In addition to the tin plating now undergoing life tests, gold, rhodium, and cadmium platings will be tested.

Task 1: Memory System and Circuit Design.

The detailed logical design of the timing and control circuits are 80% complete. Breadboard circuits have been built for this section of the memory and require 275 milliwatts of power at a 500 KC bit rate. This is within the estimate of power allocated for these circuits. Two new timing charts are included in Figures 1 and 2. These timing charts represent small changes from those published with Report No. 1. It will no longer be necessary to have a 100 microsecond delay when changing from a read to a write command. This 100 microsecond delay is still required when changing from a write to a read command.

The new sense amplifier design is nearly complete. It provides additional gain and much faster overload recovery as compared to the previous very low power sense amplifier design. These changes were necessary due to the increased speed of operation and much larger memory than was previously accommodated. Electrical tests of the complete sense line length proposed for the memory are well advanced. Electrical test unit 1 provides a means of testing a complete bit sense path which is up to 10 feet long. The revised system as detailed in the last month's report requires only a 6 foot sense line. The tests on this long sense line have confirmed our previous measurements and calculations. This test unit will be used to provide a realistic test of the signal and transient voltages to be encountered in the full size memory.

The word line drive circuits are very little changed from the previous designs. Investigations of alternate circuits such as a transistor driver per word line have shown that the diode selection matrix and system of word drive switch is the best overall system. The principle reason for keeping the diode selection matrix is that the use of one redundant diode for every four to eight word line diodes provides economical protection against failure of a large portion of the matrix in the event that a single diode should develop a short circuit. We have not been able to find a comparable protection method for the transistor matrix. Measurements with electrical test unit 3 provide a realistic load for these word drive and selection circuits. Preliminary results indicate that we will be able to use a two-turn word drive line in place of the single turn word drive line first planned. This will minimize the power consumption in the word drive circuits and make the requirements on the driver transistors much simpler by requiring about 500 ma of drive rather than 800 ma.

Task 2: Reliability and Quality Assurance

Quotations have been received from Sprague Electric Company, Corning Glass Electronics Division, Halex, Incorporated, and CTS Corporation, for the thin film hybrid circuits. CTS Corporation and Sprague Electric Company responded with the most favorable quotations, but at significantly higher costs than the estimates which were received and were used in the preparation of the proposal. We are asking for an explanation for the increased costs in these quotations. The negotiations with CTS Corporation seem to indicate that it might be desirable to proceed directly to a final design using semiconductor chips in place of the discrete transistors originally planned.

Task 3: Memory System Interconnections

Electrical test units 1 and 3 were completed during this period. These units provide for accurate simulation of the complete sense line and complete word drive line for a full memory stack. In addition, they provide electrical test of several alternate forms of honeycomb plane construction. The use of mu-metal in place of copper is being evaluated. Mu-metal memory planes may provide a further significant reduction in word drive current.

Evaluation planes have been built to permit testing various sets of word line widths to find the optimum set of conditions for signal amplitude, drive current and adjacent bit interference. In addition, a special evaluation plane has been made consisting of copper plated mu-metal word drive lines bonded to thin glass epoxy. This will be checked for

possible further drive current reduction. Approximately one dozen samples of various constructions for the memory planes and several adhesive systems were tested for 48-hour storage at 150°C. Samples using Scotch Bond AF202, Hysol 2094, and Flexrock adhesives exhibited various degrees of degradation in the bond after storage at 150°C for 48 hours. The fourth adhesive DEN 438 did not de-laminate under this storage temperature but the bond strength was judged to be inadequate. New higher temperature adhesives are being procured for test of the basic memory stack construction. All of the tested adhesives were stated to be useful beyond the temperature range to which they were subjected. The new samples which will be tested are stated to have a much higher useful range of operating temperature than the first set.

A set of small sections of memory planes are being fabricated to test four possible methods to interconnect the plated wires from plane to plane of the proposed memory stack. These interconnections need to be made on an average center-to-center spacing of 15 mils. Figure 3 is an overall sketch of the proposed half memory in a Nimbus module which is 4" x 6" x 13".

Task 4: Memory Element Fabrication and Testing

Three different groups of plated wires are undergoing extended life tests at 95°C and 90% relative humidity. Plated wire samples insulated with polyurethane as is the current practice on all of our plated wires, showed no signs of corrosion or degradation of their electrical and magnetic properties. Unprotected plated wires showed a few spots of corrosion after about 300 hours of these accelerated life tests with some loss of useful signal amplitude. The plated wires protected with a thin plating of tin about 10,000 A thick showed less corrosion and degradation than the unprotected wires but they were inferior to the polyurethane insulated wires. These life tests will continue and experiments are planned for the immediate future to test the effect of reflowing the tin after it has been electroplated. The plated wires will be passed through a tiny heated chamber to melt the tin plating in an attempt to close up any pin holes that may be present. In addition to this effort to improve the protection afforded by tin plating, other wire samples have been plated with gold, rhodium, and cadmium, and are undergoing accelerated life tests for corrosion.

Tasks 5 through 9:

No work scheduled until later in the project.

Task 10: Project Management

The tasks are on schedule as published in Report No. 1, and no revision appears to be necessary in the planning chart. Extra effort is being added to Task 4, since the results indicate that more work is going to be needed in this area to develop a corrosion protective coating. The quotations on the thin film circuits, although higher than the original estimates which we received, and form the basis for this work, do not represent a serious obstacle. The rate of expenditure for labor is still slightly below the average estimated rate and there is a reasonable possibility that the slightly lower labor cost will be able to compensate for the expected higher thin film circuit costs. Next month's report will have a more detailed summary and analysis of this problem.

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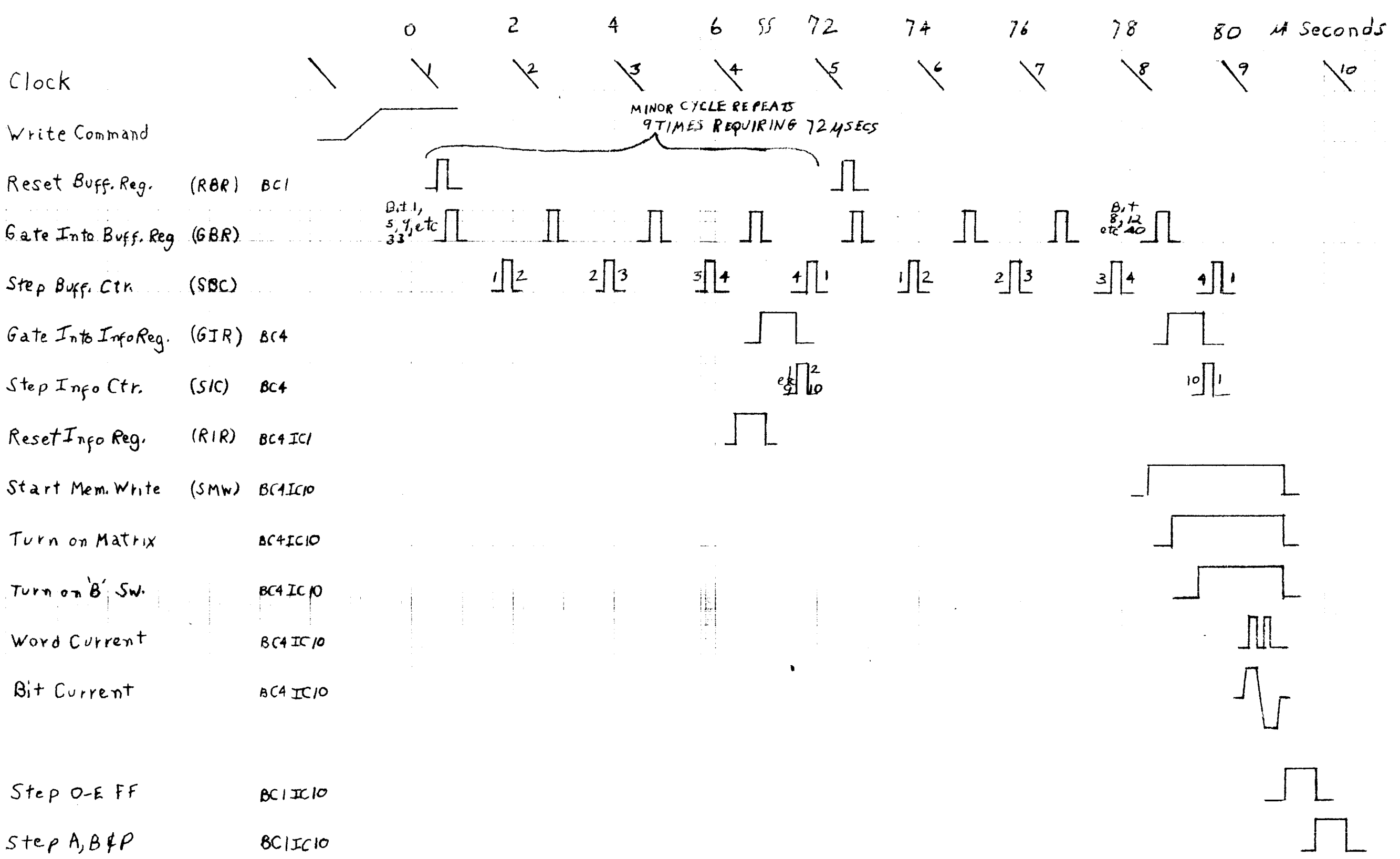
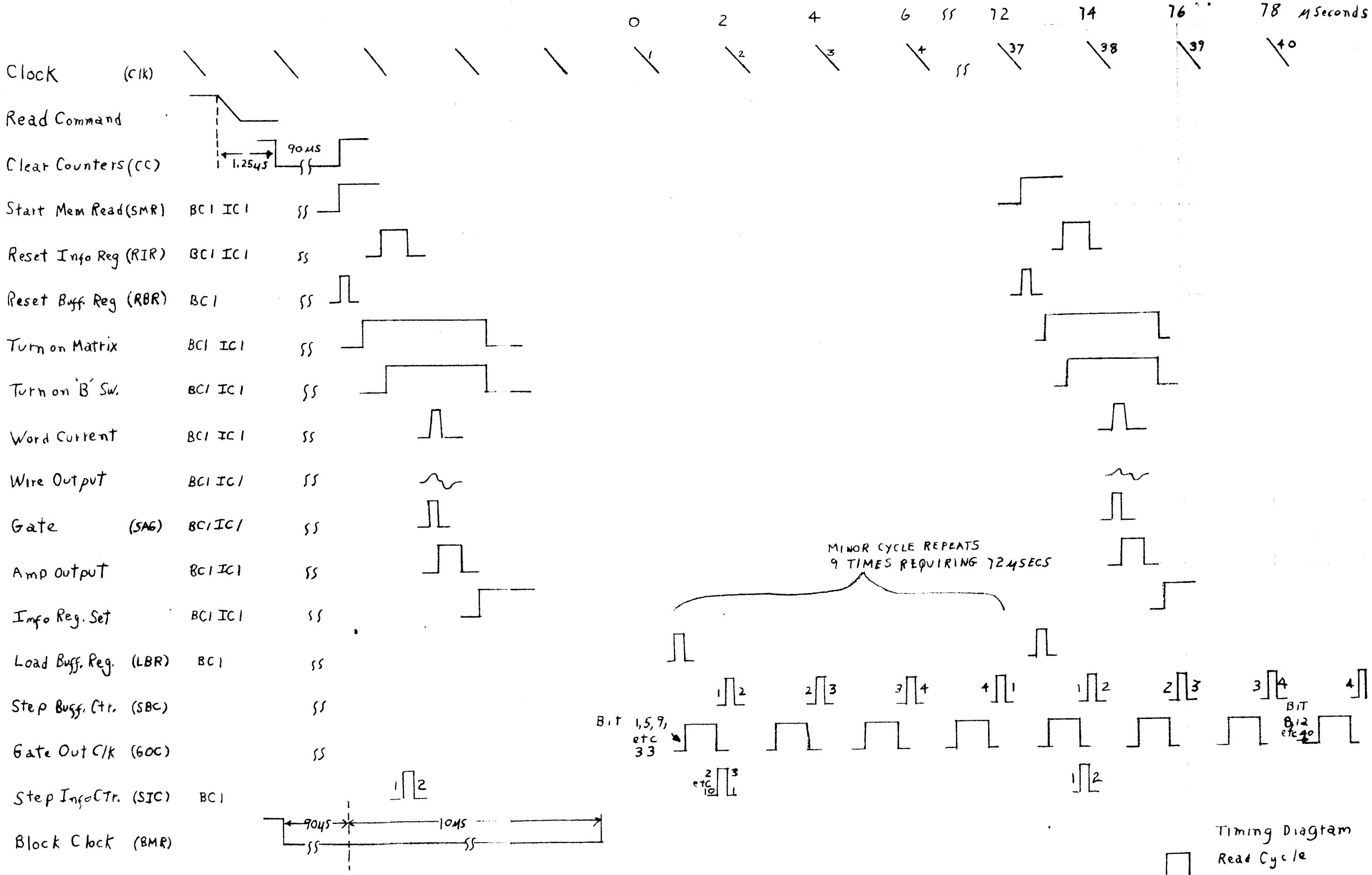


Timing Diagram
Write Cycle
Goddard Memory
2/9/65



Timing Diagram
Read Cycle
Goddard Memory
2/9/65