SYSTEMS MANAGEMENT AND ENGINEERING DEPARTMENT
Fairchild Space and Defense Systems
A Division of Fairchild Camera and Instrument Corporation
5 Aerial Way, Syosset, New York

Report No. SME-AK-8
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Job No. 1492-700

SATURN SWITCH SELECTOR
PHASE II COMPLETION REPORT

CONTRACT NO. NAS8-11683
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SECTION I

INTRODUCTION

A. PROGRAM OBJECTIVE

The object of this program is to determine through basic research and development, the extent, if any, that micro-miniaturization can be adapted to the next generation space vehicle program. The particular sub-system chosen as the basis for this study, is the Saturn Switch Selector (Mod 1). The goal of this program is a micro-miniaturized version of the Switch Selector to obtain, in the order of importance as listed, (1) higher reliability, (2) longer operating life, and (3) savings in space and weight. The reliability desired, based upon a 100 hour orbital mission is 0.999.

B. SCOPE OF WORK - PHASE II

Breadboard Evaluation and Package Design

Utilizing the Switch Selector circuit design generated in Phase I, a breadboard capable of demonstrating design practicality and operational reliability was fabricated and tested. An interconnecting technique and

package design was then prepared based upon the installation requirements of the existing Mod I Switch Selector System.

C. SUMMARY

A breadboard, containing the control logic circuitry, magnetic core input register, steady state register and three representative decode and output channels, was fabricated. Tests were conducted over the extremes of temperature and supply voltage profiles. The results of the breadboard evaluation task are discussed in Section II of this report.

A complete packaging design has been generated, containing the finalized system circuitry developed through Phase I and the Phase II breadboard analysis. The overall packaging concept and the specific techniques utilized are discussed in Section III.

The report concludes with Section IV, a comprehensive reliability analysis of the finalized system.

Authors

SECTION II

BREADBOARD EVALUATION

A. CONTROL REGISTER

The Phase I design study, selected as the key elements in the solid state redesign version of the latching relay register, multi-aperture magnetic cores. A detailed description of the operation of these devices was given in the Phase I Report together with the proposed circuit configuration of the Control Register, shown here in Figure 1.

The initial effort in the evaluation of the applicability of multi-aperture cores was devoted to an investigation of available devices capable of operating over the required temperature range of -55°C to +125°C. The following suppliers of multi-aperture core devices were considered:

(1) Indiana General Corp., Elect. Div., Keasby, New Jersey

(2) Ferroxcube Corp., Saugertees, New York

(3) RCA Semiconductor & Materials Div., Needham Heights, Mississippi

(4) Amp Inc., Harrisburgh, Pennsylvania

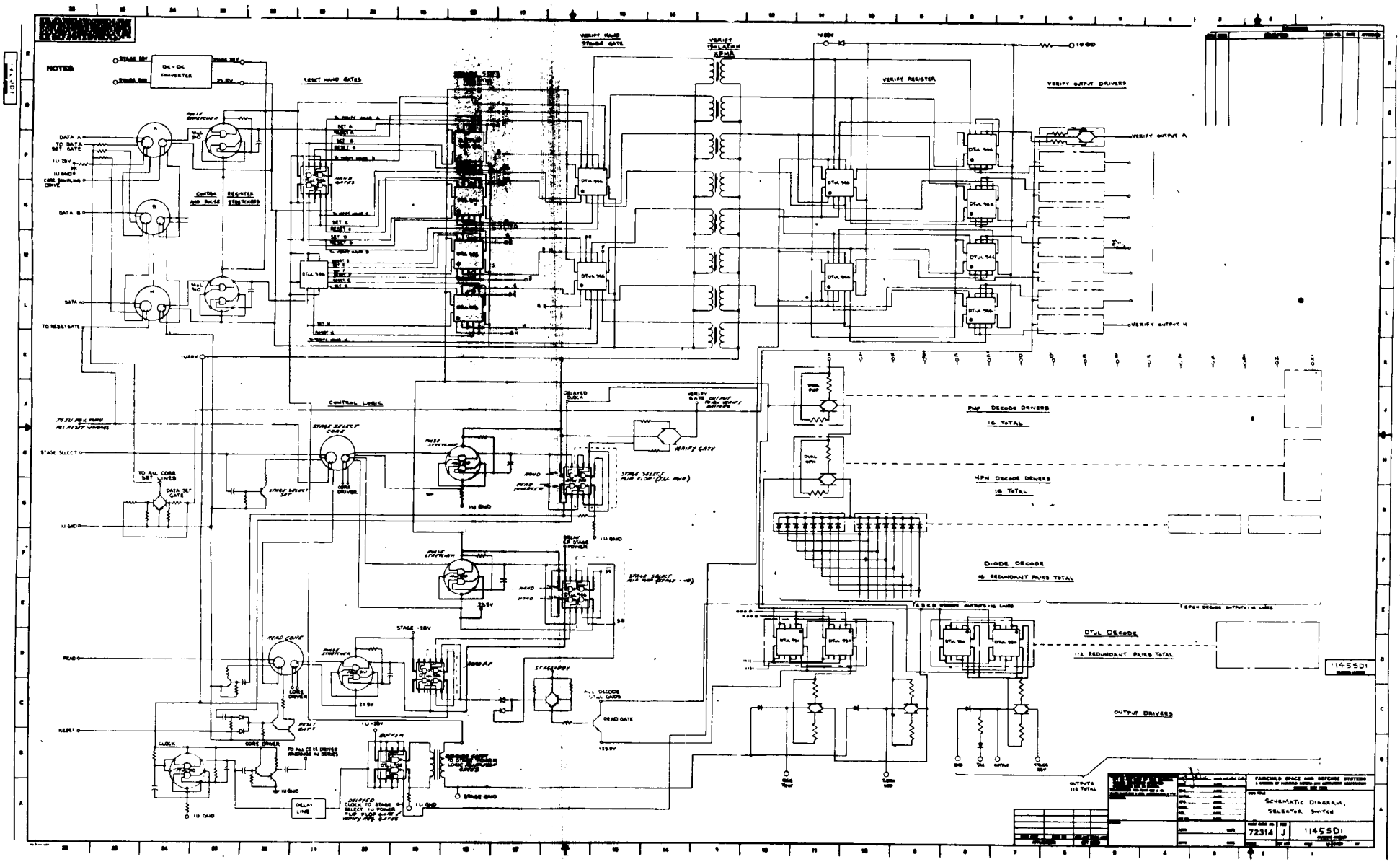

NOTES:
RESET HAND GATES
VERIFY REGISTER
VERIFY OUTPUT DRIVERS
CONTROL LOGIC
PNP DECODE DRIVERS
16 TOTAL
NPN DECODE DRIVERS
16 TOTAL
DIODE DECODE
16 REDUNDANT PAIRS TOTAL
DTUL DECODE
112 REDUNDANT PAIRS TOTAL
OUTPUT DRIVERS
SCHEMATIC DIAGRAM,
SELECTOR SWITCH
72314
J
1145501

FIGURE [illegible] DIA[illegible]

Sources (1) and (2) above manufacture a series of multi-aperture cores but have not, as yet, developed a unit capable of reliable operation above 70°C. Sources (3) and (4), have recently marketed wide temperature range core systems with an operating temperature range compatible with the environment required by the Switch Selector specifications. Further investigation revealed that Amp Inc., specializes in specific core memory packaging configurations and actually purchase the basic cores from RCA. Consequently, the effort was concentrated on utilizing the RCA Transfluxor Type No. 0154M5.

Since the Transfluxor is a relatively new device, very little technical information regarding various application techniques is available. Therefore, it was felt that an extensive breadboard and development effort was necessary to establish optimum winding data, drive current ranges, and required control circuitry.

A supply of basic cores (unwound) was obtained from RCA. These cores are extremely small, (see Figure 2), measuring .096" long by

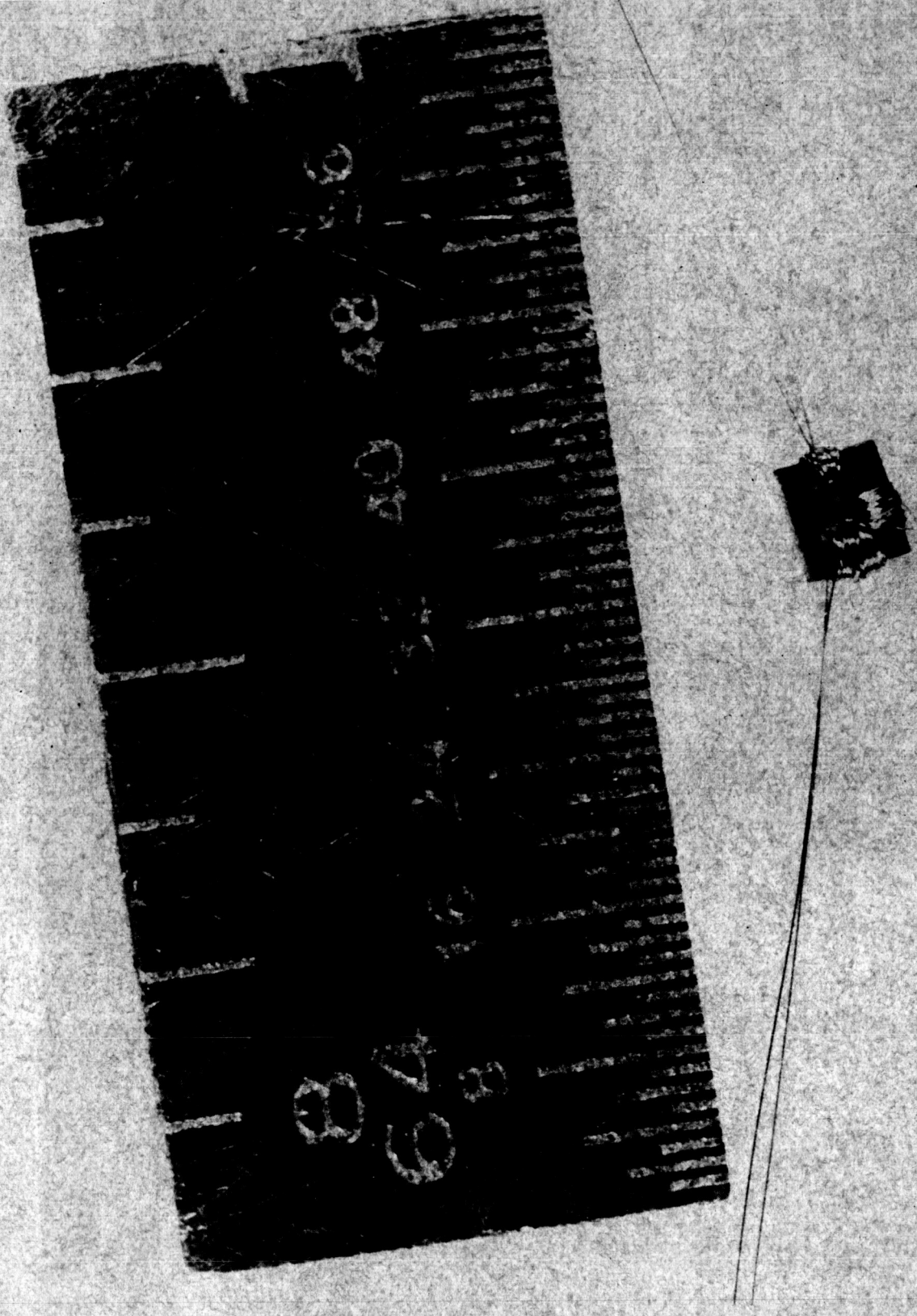


FIGURE 2. TRANSFLUXOR

.086" wide with a major aperture diameter of .040" and minor aperture diameter of .015". Obviously, the general handling of these devices was quite difficult, particularly the task of manually winding the various function windings within the apertures. The cores were wound as follows:

Major Aperture - Two Windings

Winding 1 - Block or Reset

Winding 2 - Set

Minor Aperture - Two Windings

Winding 1 - Read-Prime (Sampling)

Winding 2 - Output

The data shown in Figure 3 was used to determine the optimum current per turn in the Block or Reset winding. This is seen to be one ampere per turn. Figures 4, 5, and 6 show the data used to arrive at the optimum current per turn in the Set winding. This is seen to be approximately 575 milliamperes per turn. Since the Set current is supplied from the I.U. and is limited to

BLOCK CURRENT
AS A FUNCTION OF TEMPERATURE

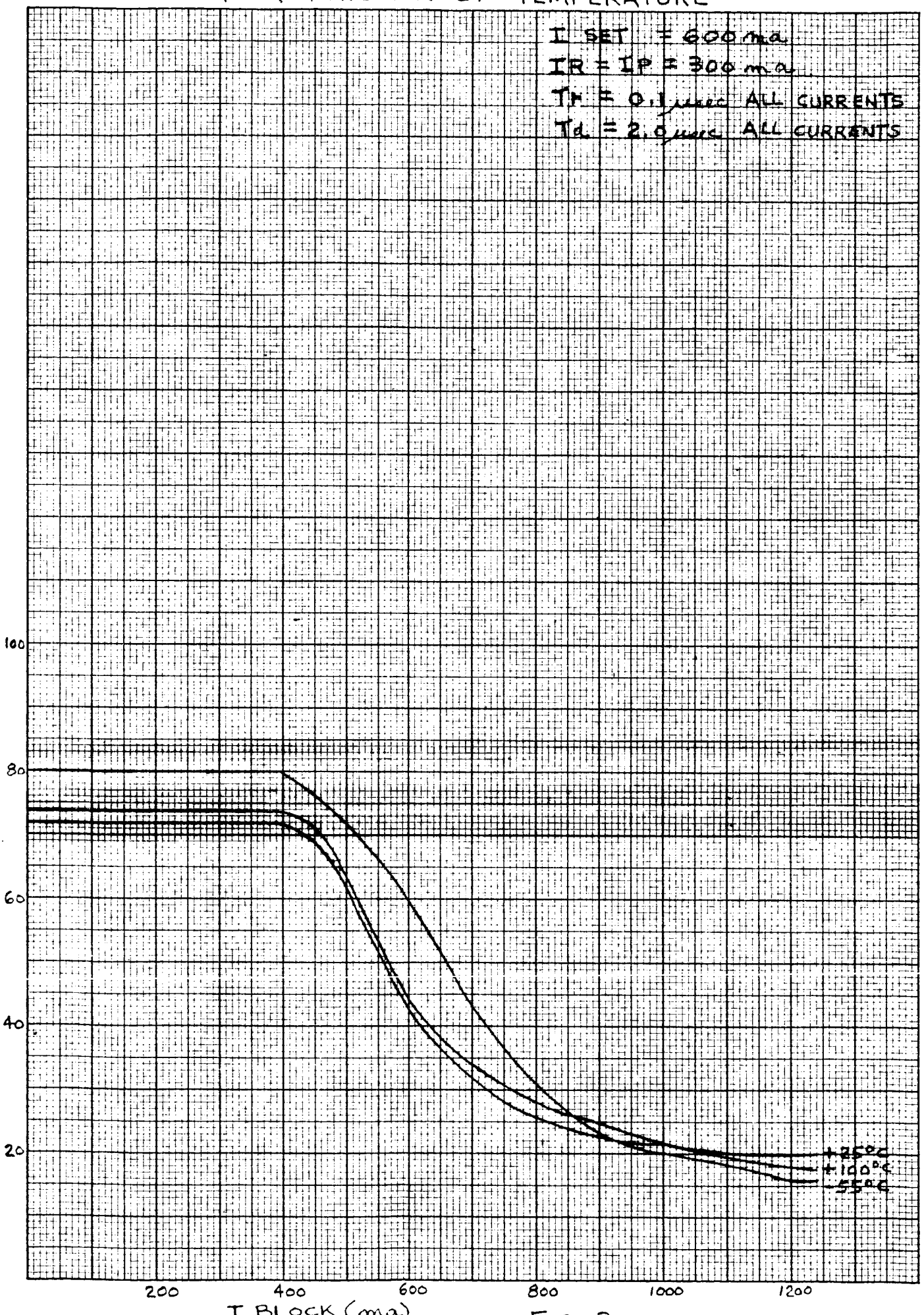


FIG. 3

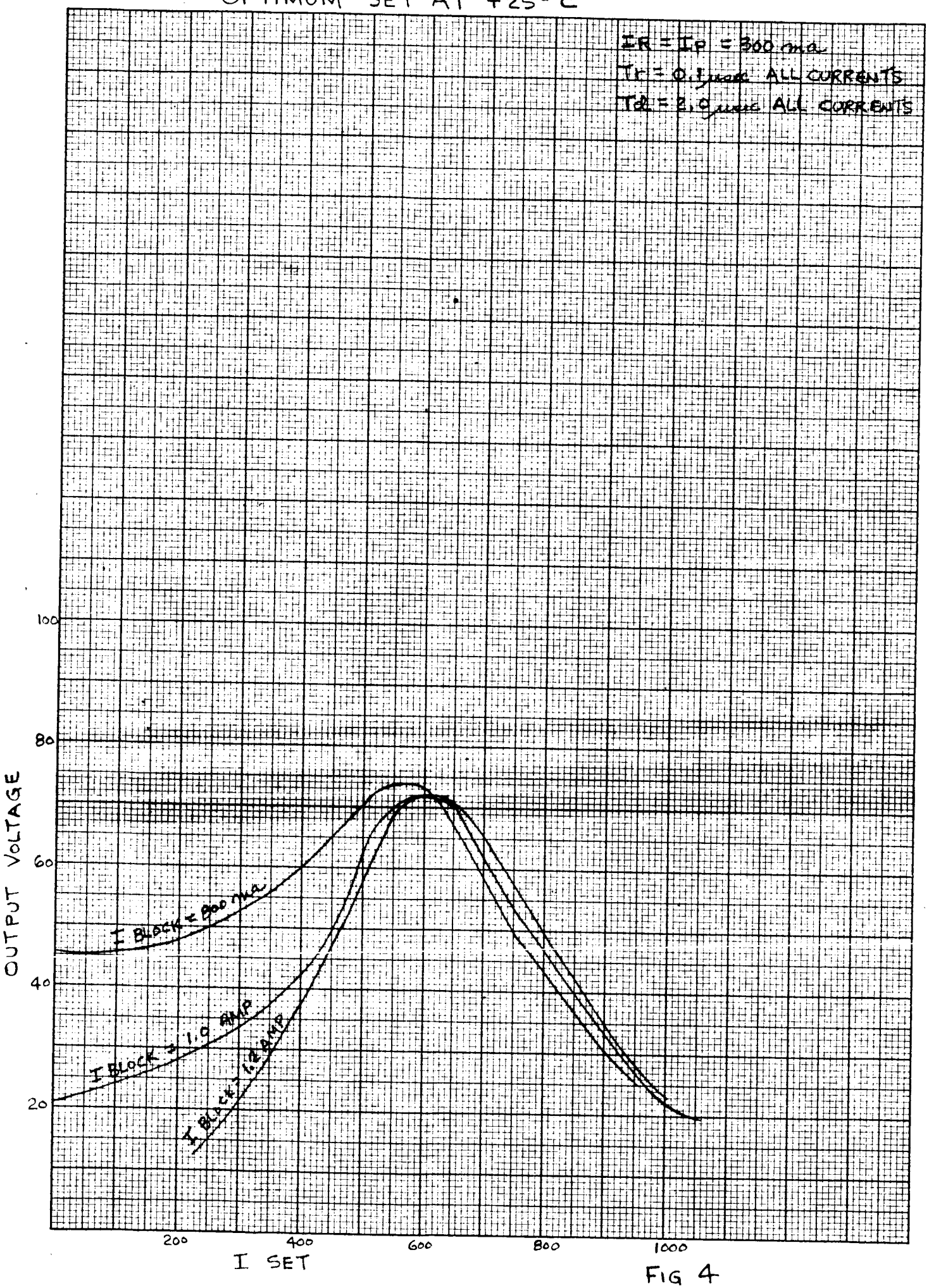

OPTIMUM SET AT +25° C
$I_R = I_P = 300$ ma.
$T_r = 0.1$ μsec ALL CURRENTS
$T_{rr} = 2.9$ μsec ALL CURRENTS
100
80
60
40
20
OUTPUT VOLTAGE
I BLOCK = 800 ma.
I BLOCK = 1.0 AMP
I BLOCK = 1.2 AMP
200
400
600
800
1000
I SET

FIG 4

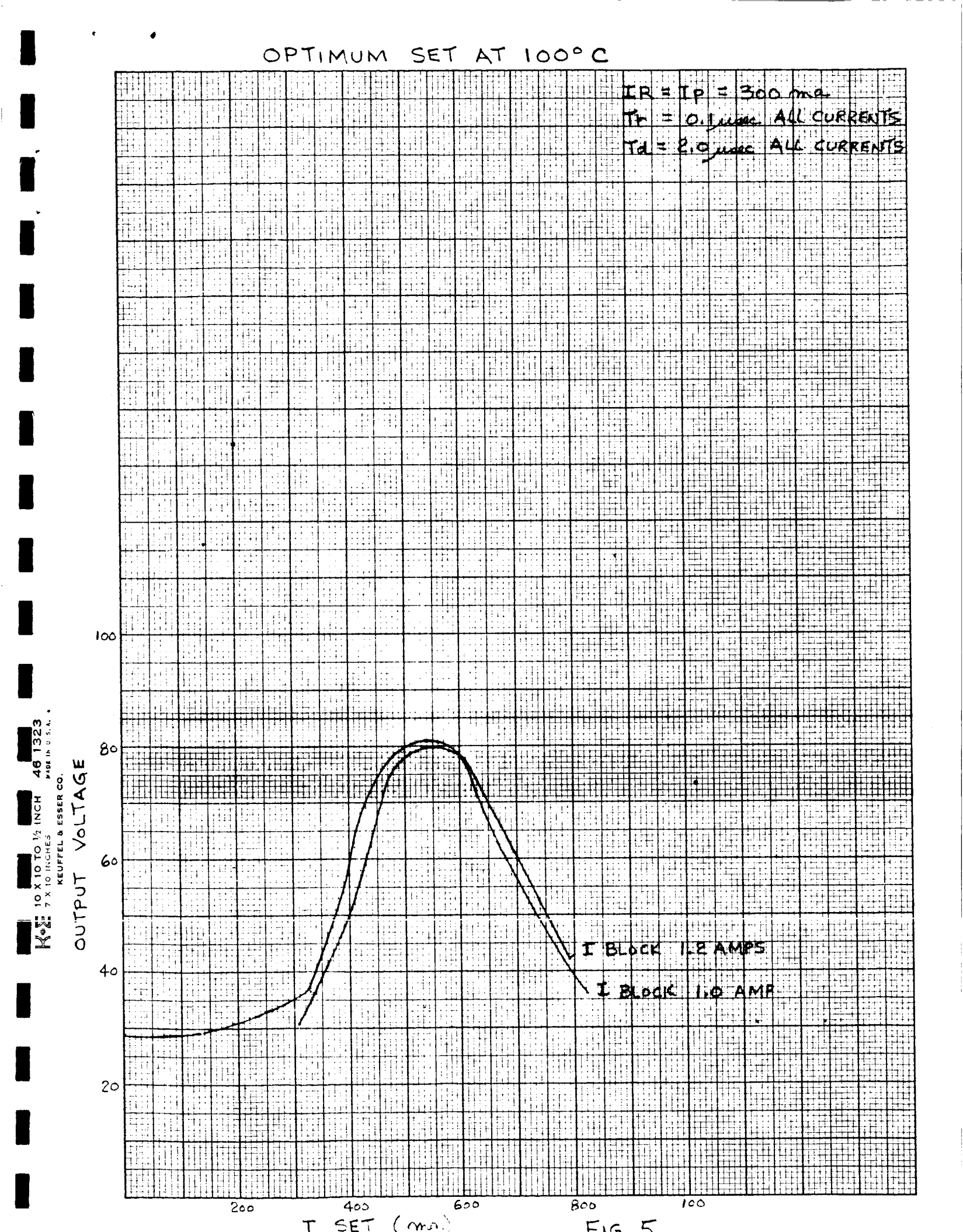

OPTIMUM SET AT 100° C
IR = Ip = 300 ma.
Tr = 0.1 μsec. ALL CURRENTS
Td = 2.0 μsec. ALL CURRENTS
OUTPUT VOLTAGE
100
80
60
40
20
I BLOCK 1.2 AMPS
I BLOCK 1.0 AMP
200
400
600
800
100
T SET (ma.)
10 X 10 TO ½ INCH 46 1323
7 X 10 INCHES MADE IN U.S.A.
KEUFFEL & ESSER CO.

FIG 5

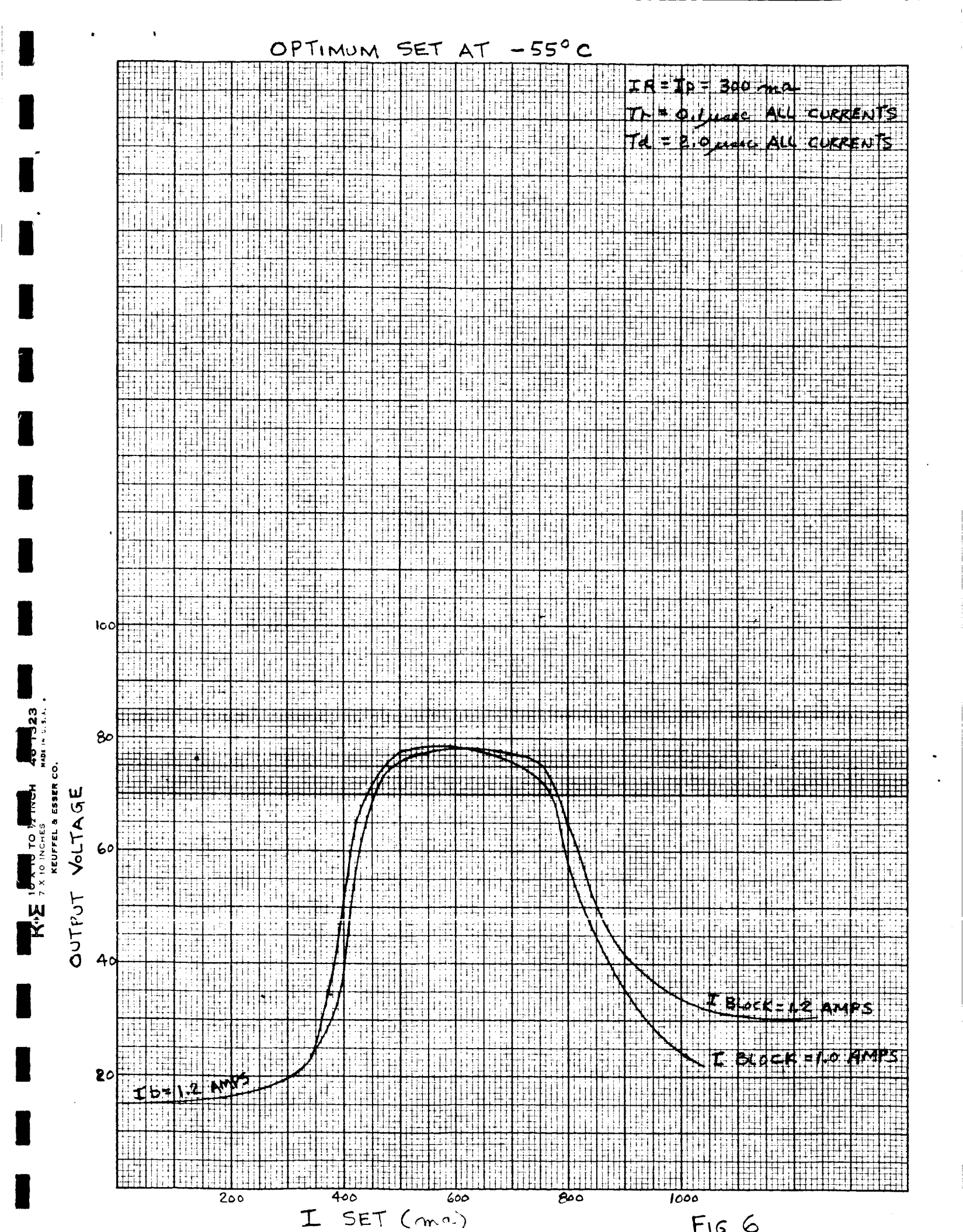

OPTIMUM SET AT -55°C
IR = Ip = 300 ma
Tr = 0.1 μsec ALL CURRENTS
Td = 2.0 μsec ALL CURRENTS
OUTPUT VOLTAGE
100
80
60
40
20
200
400
600
800
1000
I SET (ma)
I BLOCK = 1.2 AMPS
I BLOCK = 1.0 AMPS
Ib = 1.2 AMPS
KEUFFEL & ESSER CO.
MADE IN U.S.A.

FIG 6

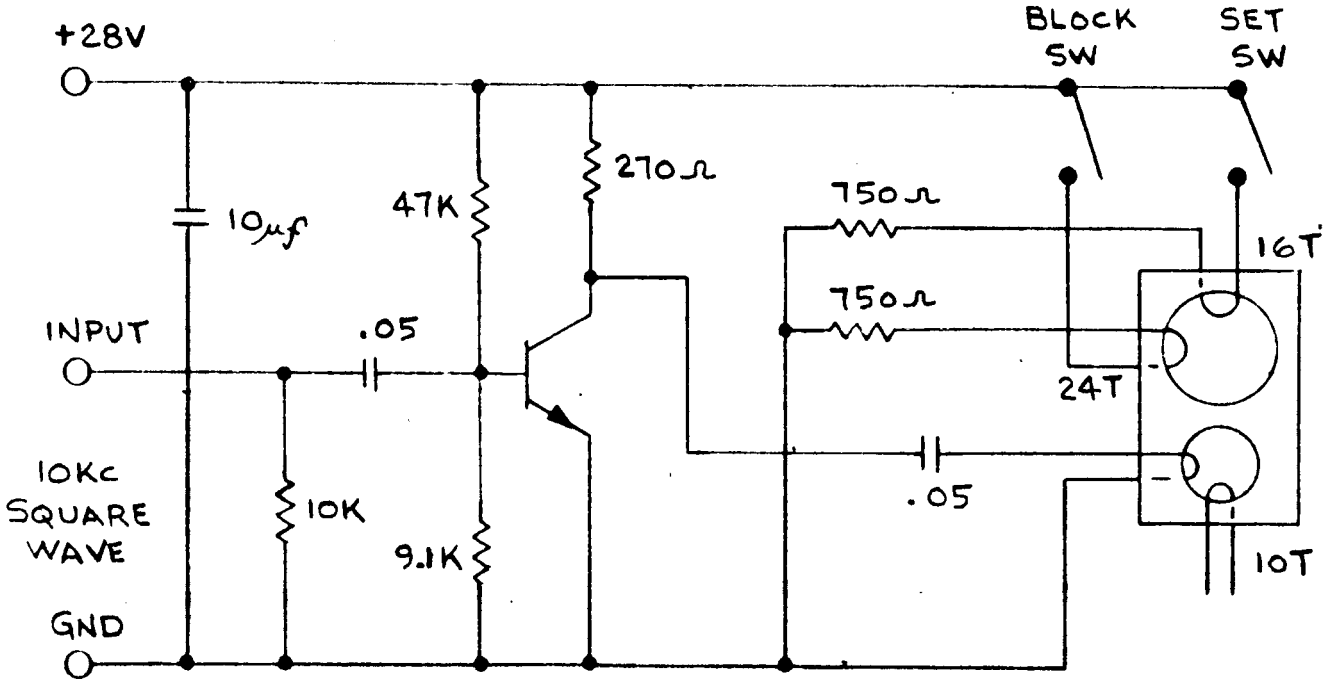
approximately 35 milliamperes, then the number of turns in the set winding must be at least;

$$T_s = \frac{575}{32} = 16 \text{ turns}$$

Using No. 44 guage wire, 16 turns were wound as the Set winding. The number of turns used for Block was simply a matter of the available physical room left in the major aperture. This allowed for 24 turns. The necessary current to Block was then 41 milliamperes.

The selection of the number of turns used on each winding of the minor aperture was based primarily on the required output signal necessary to operate external circuitry, in this case an integrated circuit monostable multivibrator. The resulting configuration was 5 turns on the Read-Prime winding, and 10 turns on the Output winding.

The first core wound, was tested with the circuit shown in Figure 7. Momentary switches were used to apply Block and Set currents to the major aperture windings. The Read-Prime winding was driven at a 10KC rate



TRANSFLUXOR TEST CIRCUIT

FIG 7

with 100 milliamperes peak current. The results of this test were promising providing the following data:

Output Voltage Blocked - 0.15 Volts

Output Voltage Set - 1.1 Volts

The effect of variations in Read-Prime current, which in this case is the continuous sampling drive derived initially from the system clock, was investigated. The results showed an essentially linear relationship between the magnitude of the drive current and the output voltage. The device saturates (reaches maximum output for Set condition) at approximately 150 milliamperes providing 1.5 volts output. However, the signal to noise ratio at drive currents above 125 milliamperes and below 50 milliamperes becomes intolerable.

The sampling drive circuit shown in Figure 7 was modified, for more efficient operation, to that shown in Figure 8. Nine additional cores were wound as described above and breadboarded as the Control Register shown in Figure 1. This circuit is identical to that discussed in the

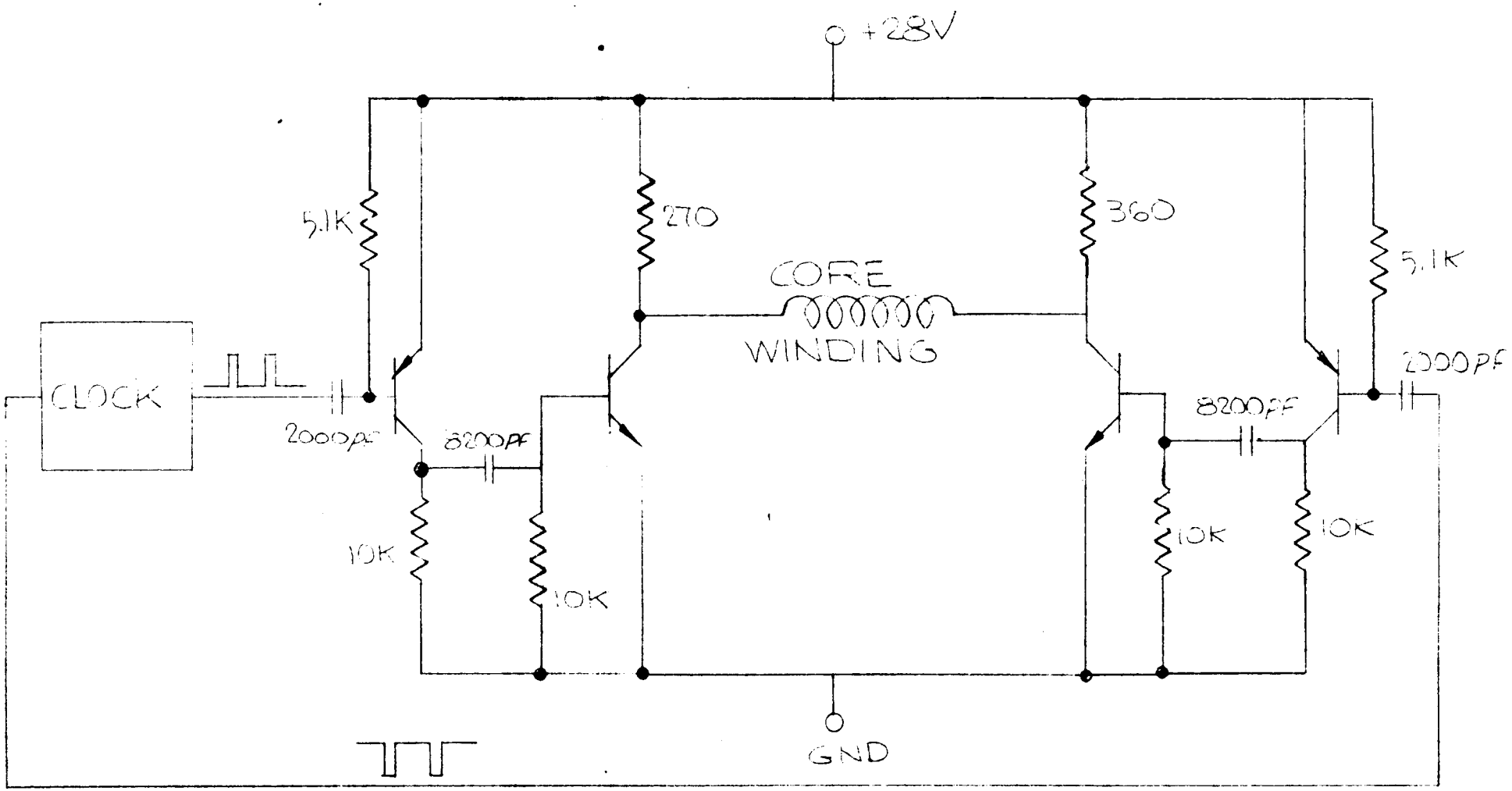


FIG-8- FINALIZED TRANSFLUXOR DRIVE

Phase I Completion Report. Here once again, due to the size of the cores, the task of breadboard fabrication and circuit interconnections was extremely time consuming.

The data obtained from each of the cores was not nearly as promising as had been indicated from the initial tests. The basic problem was the lack of an adequate signal to noise ratio (ratio of output voltage "Set" to output voltage "Blocked") which in one case was as low as 2 to 1. Further, the output voltage under Blocked conditions was dangerously close and in some cases greater than the maximum voltage (260 MV) which may be applied to the input terminal of the integrated circuit one-shot at 125°C without triggering. Several attempts were made to rewind the particular cores which operated unsatisfactorily, assuming that the original windings were improperly applied. These attempts were unsuccessful, and the devices were replaced with new cores. Ultimately, it was found impossible to obtain a set of ten cores all of which provided what were considered to be satisfactory signal-to-noise ratios. Overall circuit operation at room temperature was reliable,

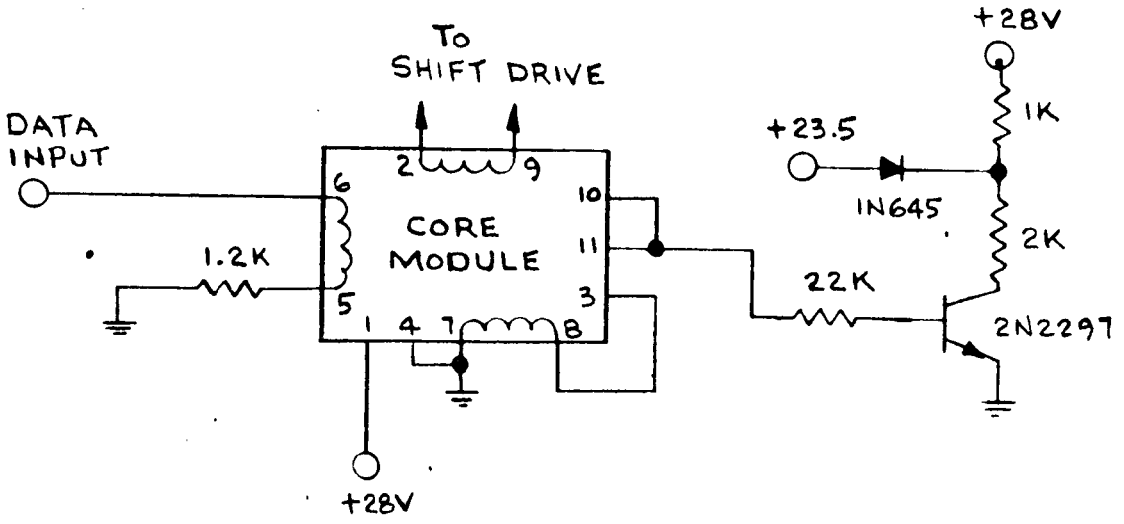
however indications were that at elevated temperatures the "Blocked" output signal of some cores would be excessive.

The breadboard was then placed in an oven and the temperature raised slowly towards 125°C. At approximately 100°C, the noise level from six of the cores was high enough to trigger their respective "one-shots". At 125°C only one core was operating satisfactorily. It became obvious at this time that a new approach to the design of the control register should be investigated concurrently with a continued effort to improve the performance of the Transfluxors.

A magnetic logic module manufactured by DI/AN Controls Corp., Boston, Massachusetts, was considered as a replacement for the multi-aperture cores. This device contains a conventional magnetic memory core of the destructive read-out variety. In addition, ancillary circuitry is provided as part of the module which when appropriately connected, re-loads the core after a read sample has been taken. This device provides an output of 20 volts when the core is set and less than 1 volt when reset, a very respectable signal-to-noise ratio.

One of these modules, a CTL-100-P/N LSQ model was breadboarded in the circuit shown in Figure 9. The transistor interface stage was included to transform the voltage output level to a form which would be compatible with the operating levels of the integrated circuit elements to be drive. The pulse waveforms obtained are shown in Figure 10. The width of the output pulse is extremely advantageous in that it obviates the necessity for the one-shot pulse stretcher previously required in conjunction with the Transfluxors. Operation of this circuit over environmental extremes was excellent and offered a much more reliable approach to the register design. One remaining problem, namely, the loss of stored information during momentary power interruptions was solved with the circuit shown in Figure 11. Operation of the overall circuit can be described as follows:

During normal operation, the shift winding of the core is constantly driven at the sampling clock rate of 10 KC. If the core is reset, no output appears when sampled. When the core is set, an output pulse is provided on the following shift pulse. The core is now momentarily reset. However, the output pulse is immediately fed back to the core (through the 1 μ sec



CORE MODULE BREADBOARD CIRCUIT

FIG 9

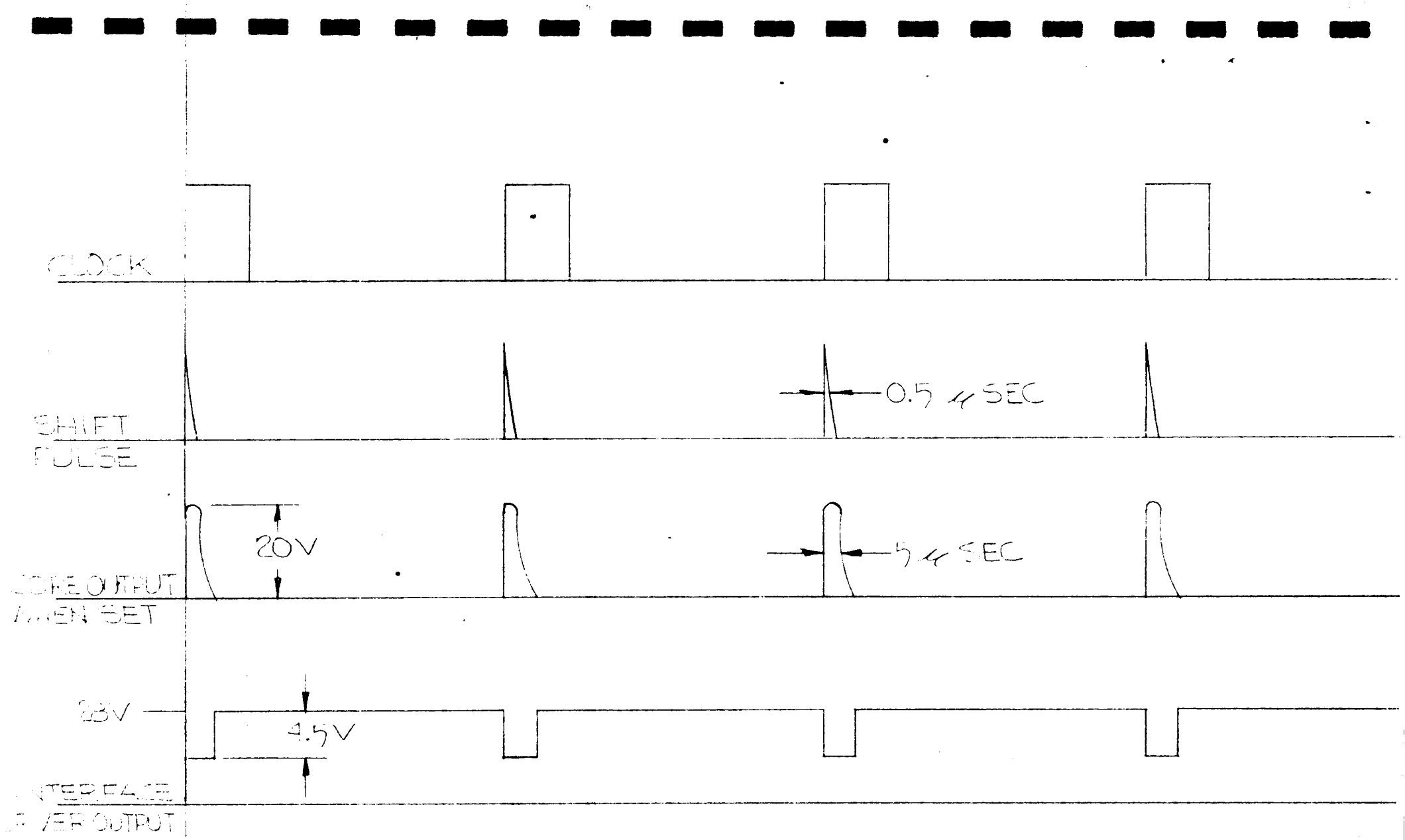
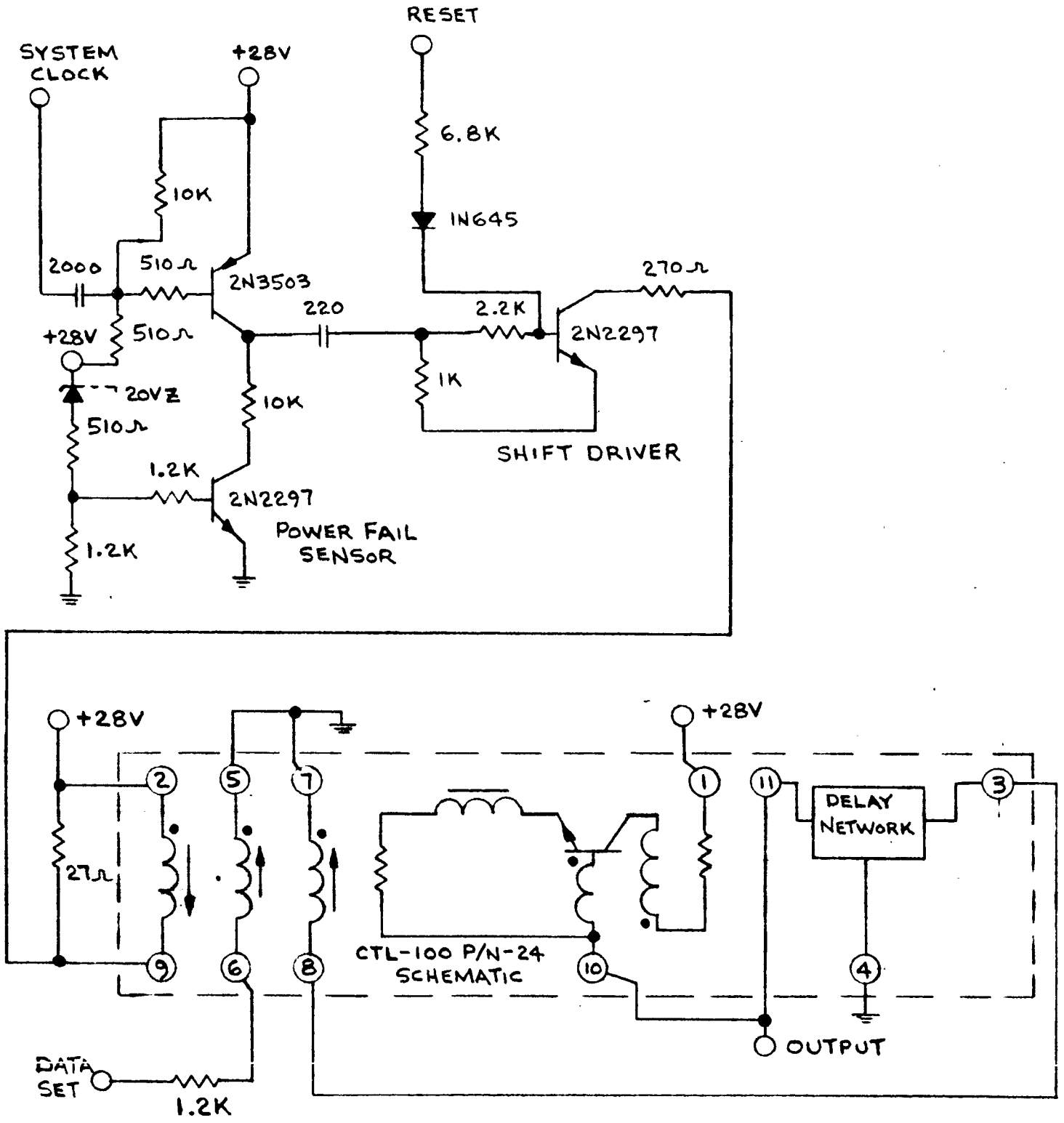


FIG.10 MAGNETIC MODULE CIRCUIT WAVEFORMS

delay network) instantly restoring it to its set condition. This cycle is repeated for each shift pulse applied. It is clear then, from the description above, that if a set core is shifted and no output results, the core does not reload itself, thus losing its memory. This would indeed be the case if a power failure occured in the line feeding the magnetic module while shift pulses were still being provided. For this reason, it is imperative that both the shift pulse circuitry and the magnetic modules operate from the same power source. Further, if this power source should fail, the shift pulse must be discontinued before the voltage applied to the magnetic module falls below its operating range. The power fail sensing circuit shown in Figure 11, assures this by disabling the shift drive when the power fails below 20 volts.

This circuit then, followed by the integrated circuit flip-flop can be considered a solid state latching relay.

The pulses applied to the shift winding provide 100 milliamperes peak current with a duration of 0.5 microseconds. If the width of this pulse is increased so that it over-rides the feedback signal, the core will be reset.



CORE MODULE CIRCUITRY
WITH SHIFT DRIVE & POWER FAIL SENSOR
FIG 11

This feature is utilized in the reset control circuitry, as follows. The reset command, (either manual or end-of-read), is applied to the Reset core. The output of this core, which is approximately 5 microseconds in duration is fed to the base of the shift pulse driver transistor resulting in a shift winding drive pulse of sufficient duration to reset all cores. The entire register then can be reset in this manner.

Due to the exceptionally good results obtained with this design, and its obvious advantages over the multi-aperture core approach, all efforts involving the application of Transfluxors were terminated.

B. STEADY STATE REGISTER

The steady state register circuitry utilized is identical with that described in the Phase I Completion Report. Fairchild Integrated Circuits Type DT μL 946 are employed as the sequence gates and flip-flops required to convert the information stored in the core register to steady state signals. The logical operation of this portion of the system is unchanged from previous descriptions. One exception however, the elimination of the one-shot pulse

stretchers, should be noted. As discussed earlier, these circuits are no longer required since the core output pulse is wide enough to permit its direct application in the "set-reset" sequence operating the flip-flops. The timing diagram describing this logical sequence is shown in Figure 12.

C. CONTROL CIRCUITRY

The Control Section of the system must provide the following functions:

(1) Arm the Control Register and enable the verify output lines upon receipt of the "Stage Select" Command,

(2) "Hold" the "Stage Select" Command for the duration of the program cycle,

(3) Generate the system clock, from which the core sampling (shift pulses), drive and "set-reset" pulse sequence must be derived,

(4) Enable the system outputs upon receipt of the "Read" Command, and,

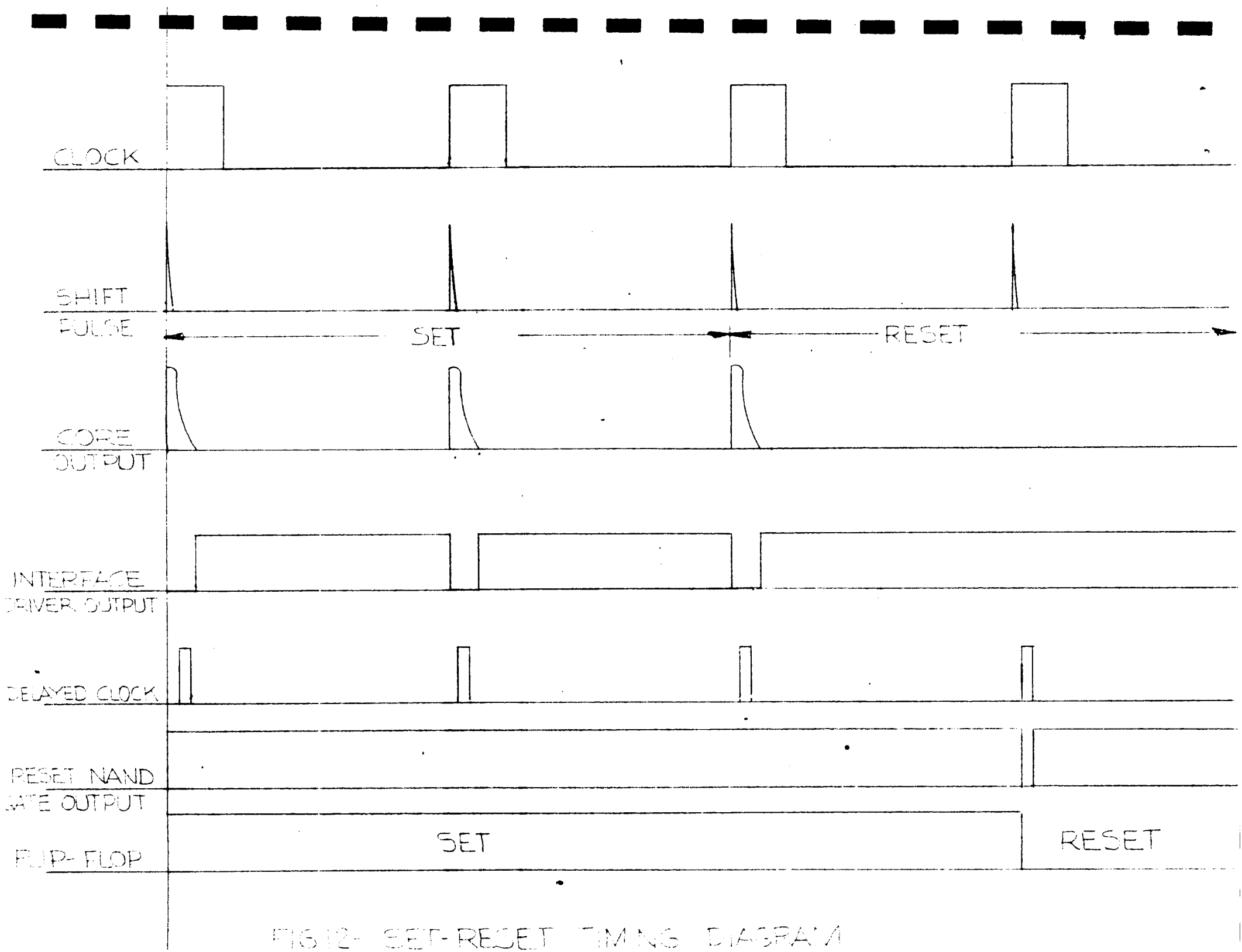


FIG 12- SET-RESET TIMING DIAGRAM

(5) Reset the entire system at the end of the program cycle (end of "Read").

The general Control circuitry design discussed in the Phase I Report has been expanded upon and refined as a result of the breadboard tests conducted.

The system "Clock" consists of two Fairchild M / L 910 integrated circuit elements operating as an asymmetrical astable multivibrator. // L8 and // L9 shown in Figure 14, are connected as a parallel redundant pair for increased reliability. The 10 KC pulse train produced is shaped and power amplified in the shift pulse driver (Q_9 and Q_{11}) providing 100 milliampere 0.5 // sec pulses to all core shift windings in series. A 27 ohm resistor is connected across each shift winding eliminating the possibility of an open circuit condition in the event of a winding "open" failure.

The Clock output also feeds the delay circuitry, consisting of Q_7, Q_8 and associated RC networks. The output signal at the junction of C_{12}, R_{54} and CR_9 is a negative going pulse which occurs one microsecond after

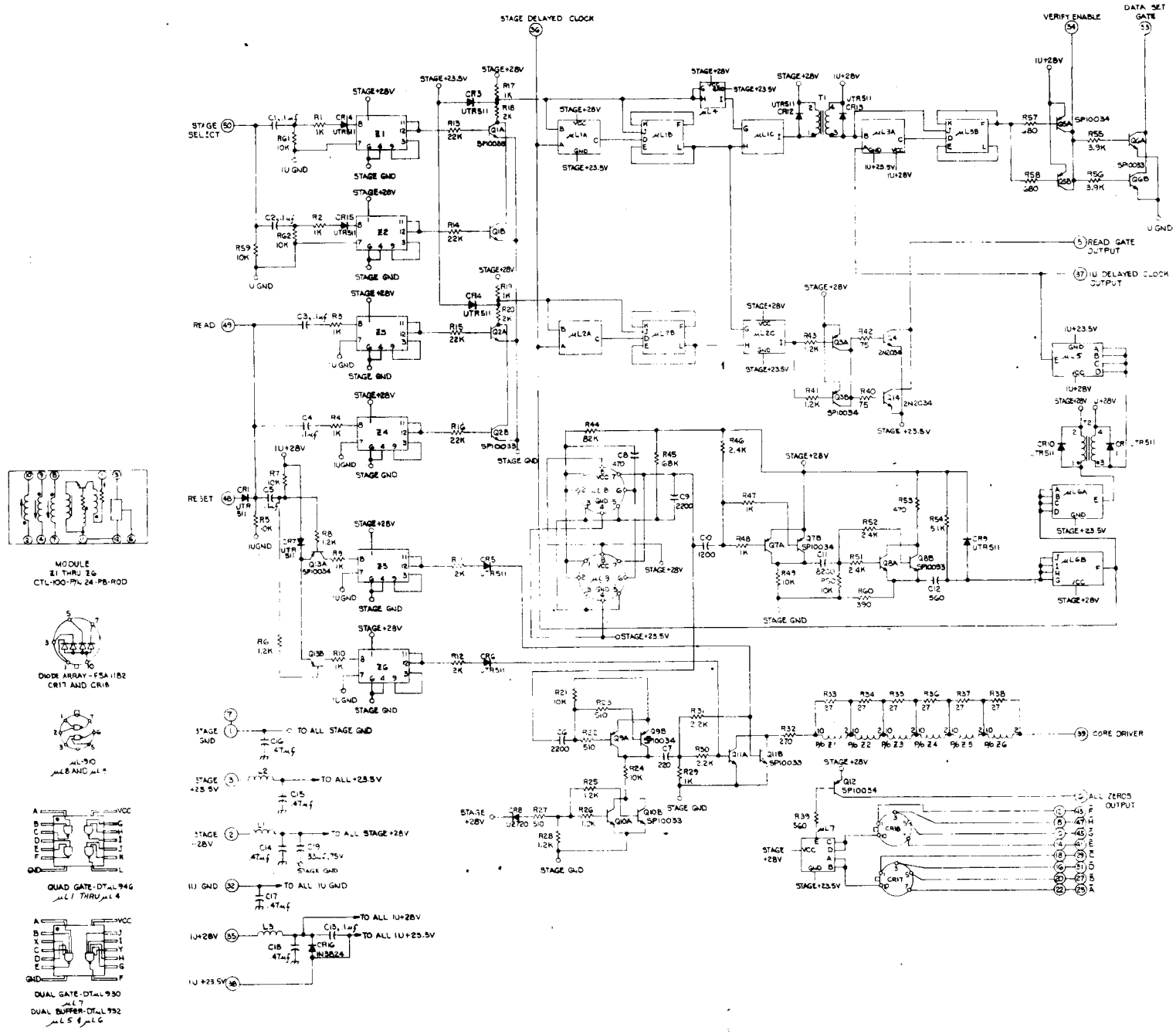


Figure 14. Control 2

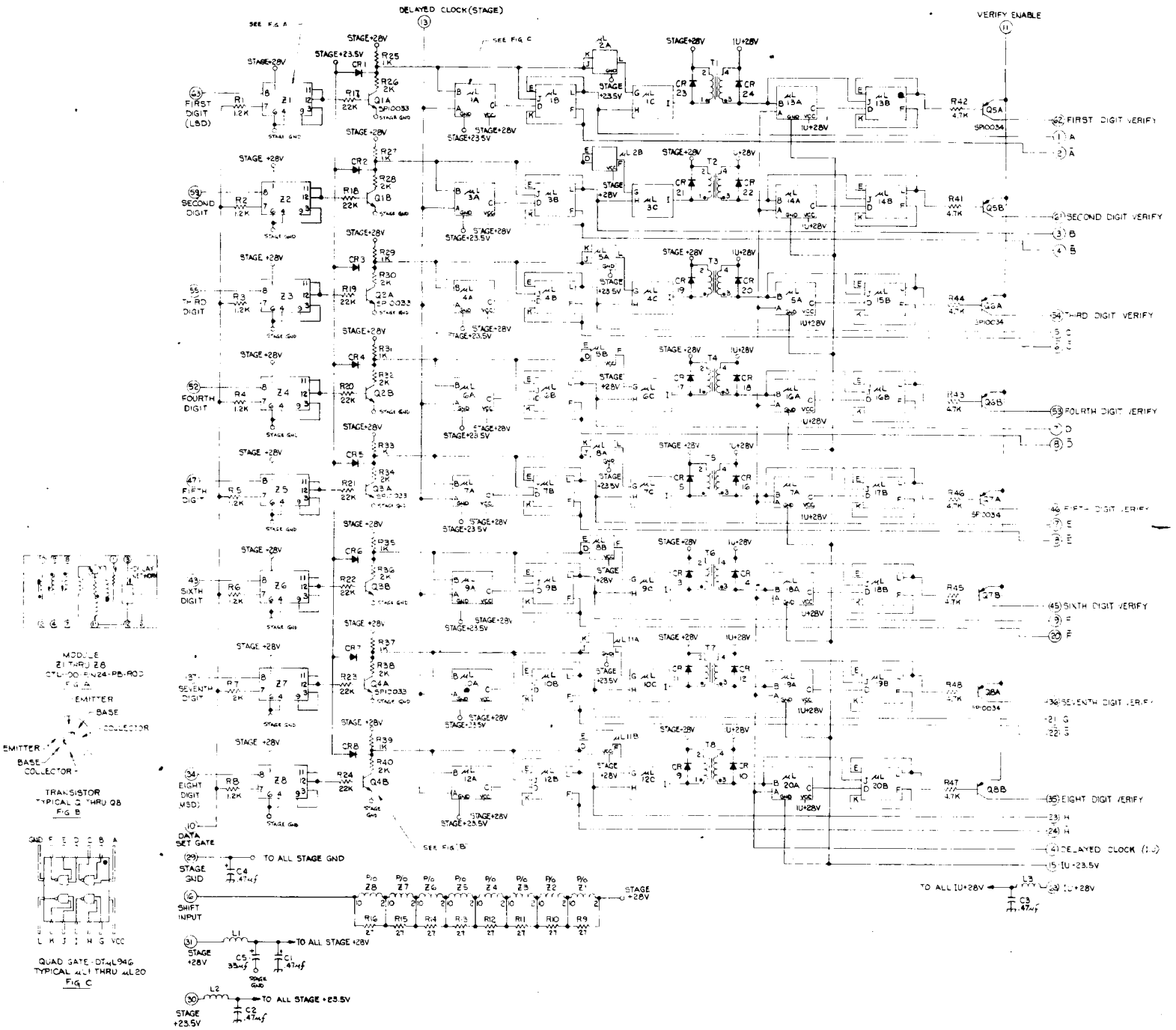


Figure 13. Control #1

the leading edge of the Clock pulse. Finally, the output of micrologic buffer μL6B is the delayed clock pulse train used in the set-reset timing sequence controlling all flip-flops operating on Stage Power. This pulse train is also transformer coupled to micrologic buffer μL5 thereby providing the delayed clock for all flip-flops operating on I.U. Power.

The "Stage Select" circuits, must be capable of controlling signals on both Stage Power, and I.U. Power. This is required for the following reasons; (1) arming of the Control Register is accomplished by gating the I.U. Data Set signals, (2) the verify outputs are on I.U. Power, and, (3) gating of the system outputs requires the control of Stage Power at the "Read" gate. Consequently, the steady state "Stage Select" data must be available on both Stage and I.U. Power. Reference is made to Figure 14 in describing the resulting circuitry. Cores Z_1 and Z_2 (parallel redundancy) are set on the leading edge of the "Stage Select" Command. The output pulses resulting from Q_{1A}, and Q_{1B}, set flip-flop μL1B, providing an output to be utilized for Stage Power gating. The state of flip-flop μL1B is transformer coupled to flip-flop μL3B providing the Stage

Select data to be utilized for I.U. Power gating. (A more detailed description of the transformer coupling techniques used is discussed below in the section entitled, Verify Circuitry).

Arming the Control Register is accomplished by enabling the Data Set Gate (Q6) through which core set currents flow. Figure 13 shows the "set" windings of each data core (Z_1 through Z_8) being returned to the "Data Set" gate through limiting resistors R_1 through R_8. Since data information is fed simultaneously to all four Switch Selectors in the Saturn Vehicle, it is important that only the Switch Selector in the particular "stage selected" will accept the data. This function is performed by the circuitry described above.

The Verify outputs are enabled in a manner identical to that above. Verify Gate (Q_5, Figure 14) enables verify output transistors Q_{5A} thru Q_{8B} (Figure 13) when the Stage Select Command is received. Both Verify Enable and Data Set functions are performed (see Figure 14) on I.U. Power as described previously.

The output of the Stage Select flip-flop (½ L1B, Figure 14) operating on Stage Power, is applied as one input to the two input "AND" gate ½ L2C. The "Read" cores (Z_3 and Z_4, Figure 14) are set on the leading edge of the "Read" Command and thereby control the state of flip-flop ½ L2B. The output of this flip-flop provides the second input to the "AND" gate ½ L2C thereby controlling the "Read" Gate ($Q_{4,14}$). The system output then, is present when both the Stage Select and Read flip-flops are set, satisfying the operational requirements of the system.

The reset cores (Z_5 and Z_6, Figure 14) are set on the trailing edge of the "Read" Command, and the output applied to the shift pulse driver (Q_{11}). The broadened shift pulse resulting resets all cores. The entire system is now reset and awaits the start of the next program cycle.

D. VERIFY CIRCUITRY

As was discussed in the Phase I Report, the major objective in the design of the verify circuitry was the transformation of data from the Stage Power Steady State Register to the I.U. Power verify register.

This was accomplished by means of the strobed transformer technique described in the report. One refinement was added to the design, an inverter stage (of L2A, 2B, 5A, 5B, 8A, 8B, 11A, 11B, Figure 13) in each set line feeding the strobe pulse to the transformer drive gates. The purpose of this addition is the reduction of the duty cycle required in the drive gates when transferring "ones". This can be better understood with the aid of Figure 15. It can be seen, that without the inverter stage, heavy current is drawn through the transformer and drive gates 95% of the time during which the bit is a "one". With the additional stage, the duty cycle is effectively inverted and becomes 5%, resulting in a major reduction in power consumption. No current is drawn through the transformer and drive gate when the bit is a zero, (this is seen to be true with or without the inverter stage), so that the overall operating efficiency of this circuit is high.

The verify register flip-flops control the eight verify driver transistors Q_{5A} through Q_{8B}, providing the complimented word for verification.

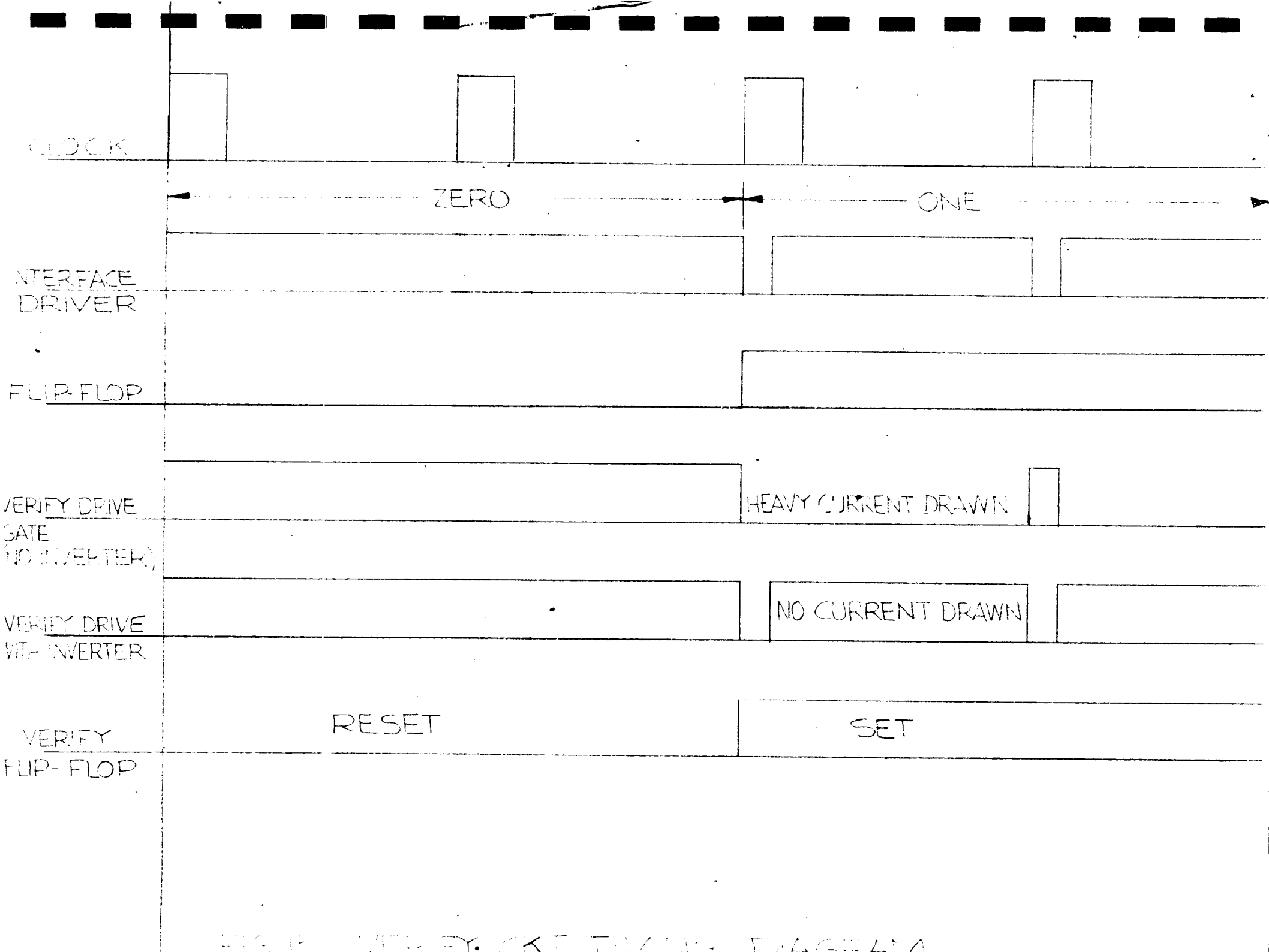
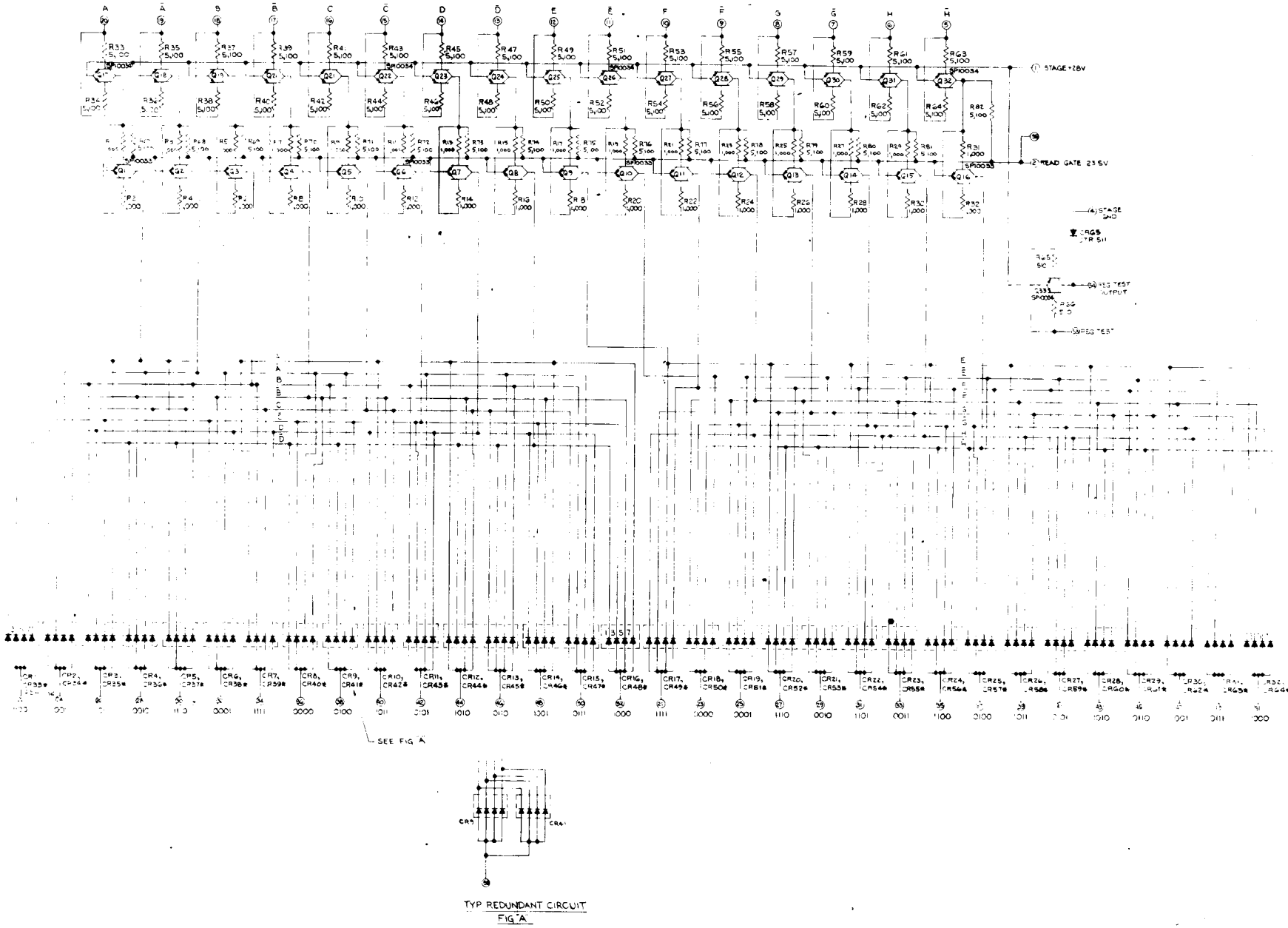


FIG. 3 — VERIFY CIRCUIT TIMING DIAGRAM



TYP REDUNDANT CIRCUIT
FIG 'A'

Figure 16. Diode Decode

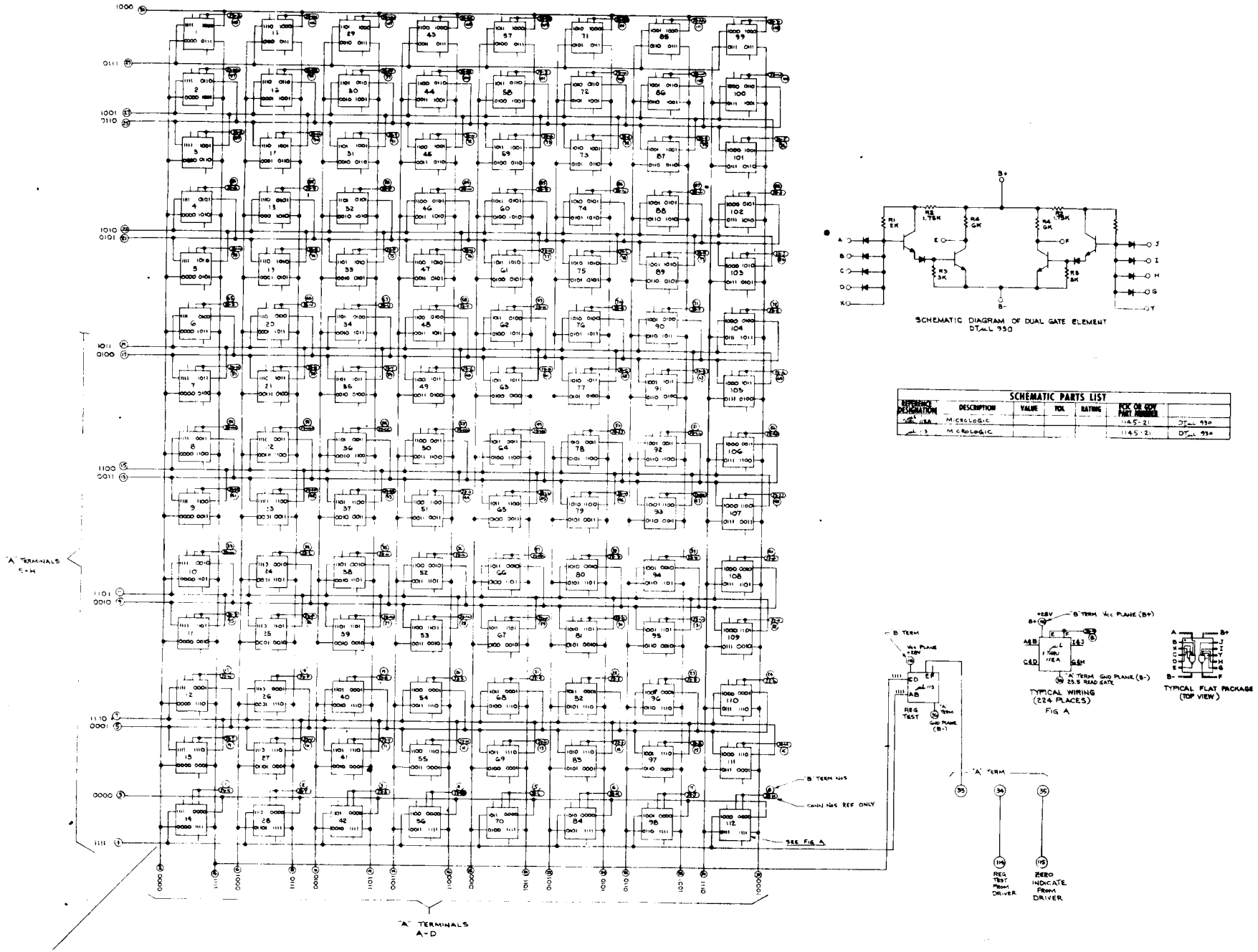


Figure 17. DTL Decode

E. DECODE LOGIC AND OUTPUT DRIVERS

With the exception of an operational modification made in the "Zero Indicate" output, this portion of the system required no design changes from the circuitry shown in the Phase I Report. Figures 16, 17, and 18 show the finalized circuitry.

A "Zero Indicate" output is required at all times during which the control register is reset. Further, this output must not be present at any time during which the control register is not all zeros. This function is accomplished by means of an eight input "AND" gate, (CR_{17} and CR_{18} Figure 14) fed from the compliment side of the control register. A Zero Indicate output will occur therefore, only for the specified condition.

F. SIMULATED SYSTEM BREADBOARD TESTS

Since it was impractical to breadboard the entire Switch Selector, both from the standpoint of materials expenditure and time required, only those portions of the system required to prove design feasibility were fabricated. These circuits included the following:

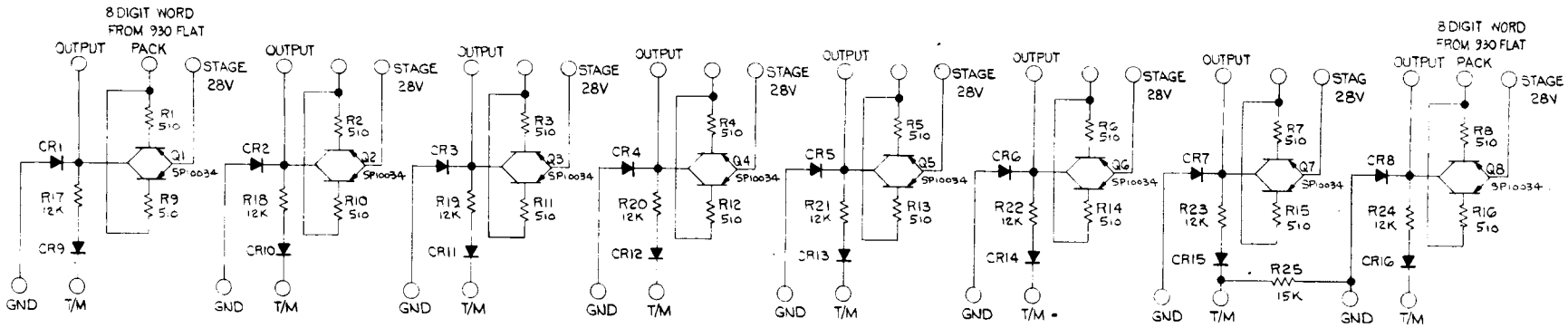


Figure 18. Driver Module

FAIRCHILD
SPACE AND DEFENSE SYSTEMS

1. Complete Control Logic Section consisting of

   (a) Clock

   (b) Shift Pulse Driver

   (c) Delayed Clock and Buffer (Stage Power Only)

   (d) Stage Select Circuitry including transformer coupling to I.U. Power

   (e) Read Circuitry

   (f) Reset Circuitry

2. Four Bit Core Register

3. Four Bit Steady State Register including

   (a) Interface Drivers

   (b) Nand Reset Gates

   (c) Flip-flop Register

4. Decode Channels and Output Drivers for Words 1111, and 1010.

5. Zero Indicate Output

6. I.U. Program Simulator

7. DC-DC Converter

8. All "Dummy" Loads necessary to simulate the exact load conditions which would exist in a complete system.

Figure 19 is a schematic of the breadboard which was fabricated and tested. No verify outputs were included since these circuits are essentially identical to the output circuits shown. Similarly, transformer coupling circuits were not duplicated since a representative circuit was used in the Stage Select channel. Two decode and output channels were breadboarded, typifying the 112 channels which will be ultimately used. The "Dummy" loads are identified in Figure 19 and include circuits which represent the worst case conditions of (a) load currents and (b) redundant circuit failure modes.

The operational performance of the breadboard during the initial environmental tests (-55°C to +125°C) was generally good. Waveforms and

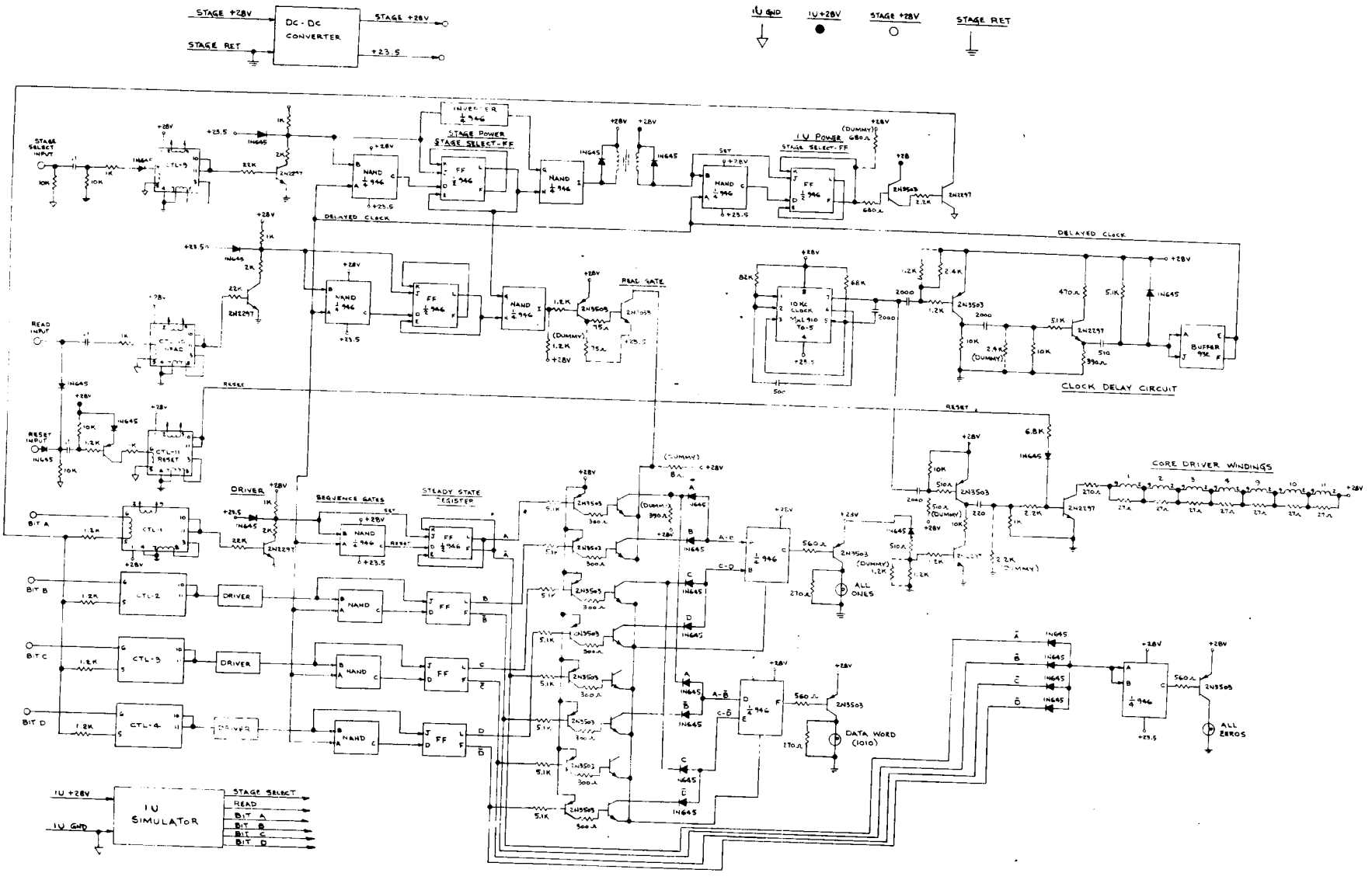


Figure 19. Selector Switch Breadboard

timing sequences at key points in the system were constantly monitored during these tests. In some instances, parameter values were changed slightly and minor circuit additions made to increase the "margin of safety" at the extremes of the operating range. Each change made was followed by a complete environmental test run. Some of these changes and the reasons for each are listed below.

1. The addition of diode CR_{14} and R_{61} in the Stage Select core set line to prevent the negative pulse at the trailing edge of the command from resetting the core.

2. A change in the values of Capacitors C_{12} and C_{11} from 2000 pf and 8000 pf to 560 pf and 2000 pf respectively to provide a more stable delayed clock pulse at -55°C.

3. A change in the value of R_{11} in the reset core output line from 6.8K to 2.0K to increase the reset current drive at -55°C.

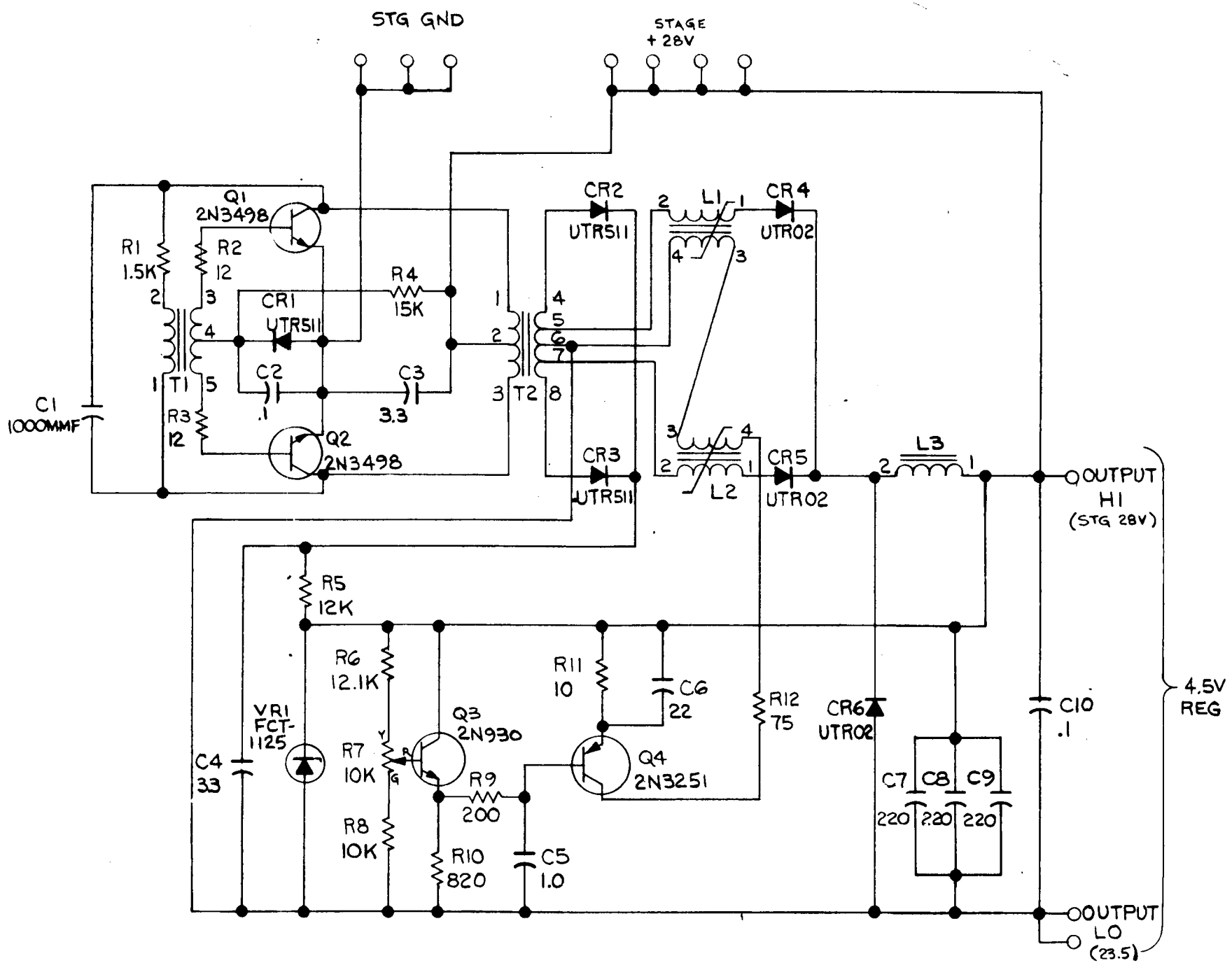


Figure 20. DC-DC Conv.

FAIRCHILD

G. SUMMARY

The results of the breadboard evaluation effort in Phase II were used as the basis for the finalized system schematics shown in Figures 13 through 18. During this task, every effort was made to simulate full scale operating conditions in an attempt to minimize the de-bugging chores which invariably accompany the construction of prototype systems of this complexity. The decoupling networks and RFI filters shown are evidence of such measures and have been included at this phase of the program, rather than later on when their addition may become a major problem.

SECTION III

PACKAGE DESIGN

A. INTRODUCTION

The overall package form factor, used as a basis for the design philosophy generated in this phase, was prescribed by the Mod I housing and installation specifications. A detailed description of the resulting package and interconnection design is given in the following discussion.

B. SWITCH SELECTOR ASSEMBLY

Figure 21 shows the entire Switch Selector assembly. The main housing, (casting), is similar to the Mod I, having identical mounting holes and connector interfaces, allowing for complete interchangeability of systems. The housing will be a machined magnesium casting capable of being pressurized to 30 psig per MSFC-09-5. The gasket utilized provides R.F.I. radiation shielding as well as the pressure seal required.

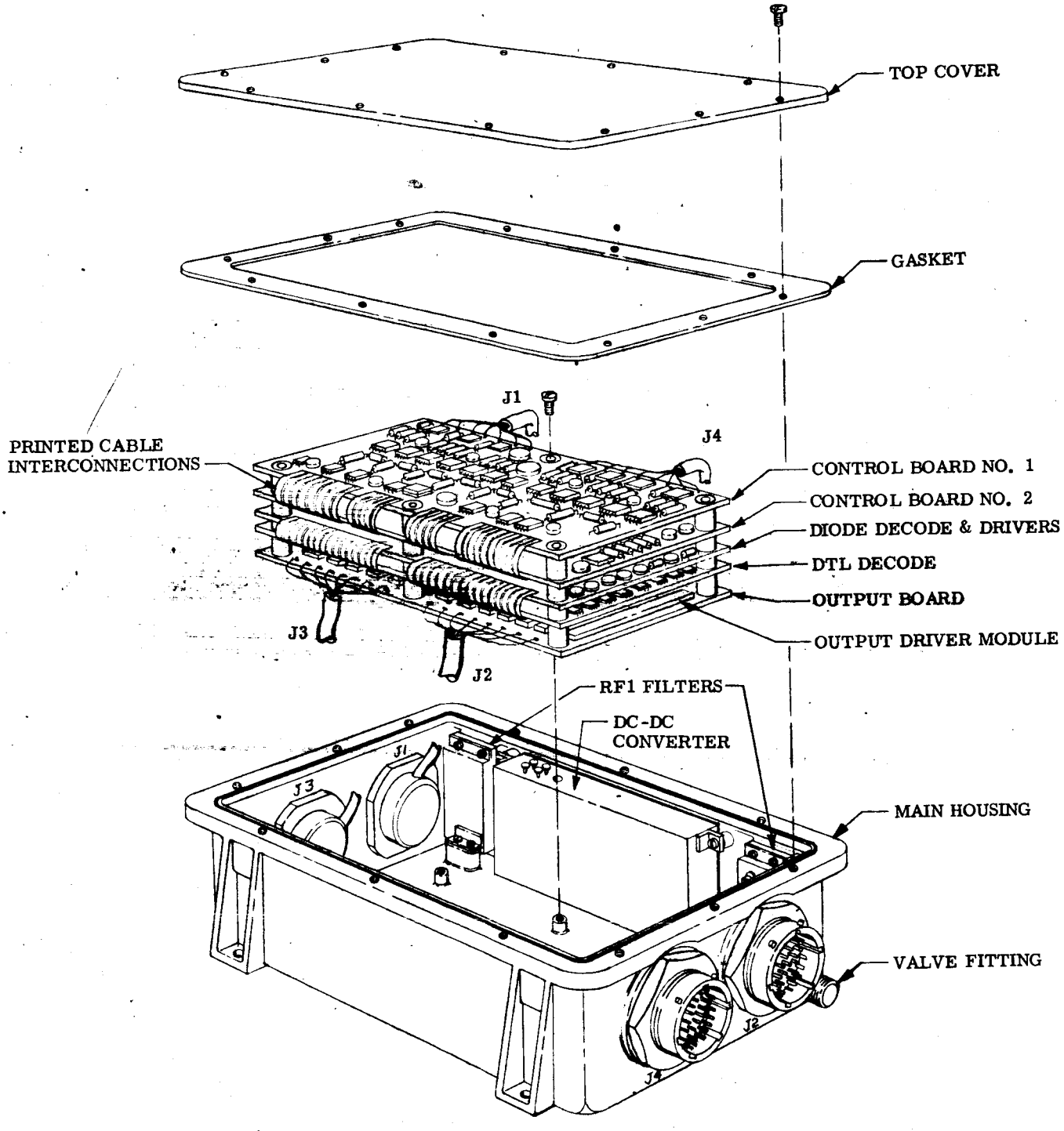


FIGURE 21

SWITCH SELECTOR ASSEMBLY

Mounted on the inner wall of the casting, are the DC-DC Converter package and two RFI filters. The converter unit is a completely self-contained, encapsulated and shielded package. The internal construction consists of a cordwood module with nickel ribbon welded interconnections. The RFI filters (one for Stage Power and one of I.U. Power) are included to prevent conduction of R.F. noise on the incoming power lines.

The electronic package is comprised of five printed circuit boards, namely,

(1) Control Board No. 1

(2) Control Board No. 2

(3) Diode Decode and Drive Board

(4) DT / L Decode Board

(5) Output Driver Board

The logic flow of this five board assembly is arranged so that all connector interfacing from J_1 and J_4 is routed to the input side of Control

Board No. 1 and all connector interfacing from J_2 and J_3 is routed to the output side of the Output Driver Board. All board to board wiring is accomplished by means of printed circuit cabling and flows from the top sub-assembly to the bottom as shown in Figure 21.

C. PRINTED CIRCUIT BOARDS

In the design of all printed circuit boards, every effort was made to adhere to the guide lines established in MSFC-STD-154. In several cases however, the utilization of multi-layer boards was necessary. Since specifications governing the design of such boards (because of the relatively new techniques used), are not included in MSFC-STD-154, this phase of the packaging design can be considered developmental and will contribute to the general investigation of multi-layer board reliability.

On the board containing the diode decode circuitry, where newly developed circuit modules are used (integrated diode array packages), it became extremely difficult to maintain a ten mil (.010") annular pad around the holes accepting the package leads. This was due to the proximity of the

leads on the package itself. Lead "spreaders" or "shapers" were investigated in this regard but were found to be difficult to apply and resulted in what was considered a less reliable structural mounting configuration. It is expected that close control over the plating process in these areas will provide annular rings of not less than seven mils (.007").

In all other aspects regarding the design of the printed circuit boards, MSFC-STD-154 specifications are strictly observed.

Control Boards No. 1 and No. 2 surface area and interconnection density allowed the design of 2-sided printed circuit boards. The Diode Driver and Array Board, the DT γ L Decode Board and the Output Driver Board are multi-layer printed wiring boards. The two controls boards and the DT γ L Decode board are designed so that flat packs can be either welded or soldered to the board surface. Recent investigation indicates that welded attachment of flat packs offers a greater degree of permanence and potential reliability than solder connections. Flat pack attachment with welding is a repeatable, closely controlled method of assembly and the

limited area (.020") of current application prevents heat being dissipated to the flat pack body during assembly. For added reliability each flat pack will be doubled welded to the pad.

A brief description of the salient features of the individual boards is included below. All five printed circuit boards are of the same physical size having dimensions of 5.25" x 9.0" x .090" thick, and have 6 peripheral mounting holes. They are laminated of glass epoxy per MIL-P-13949. All steady state power (I.U. and Stage and their respective returns), are routed to each board as required, directly from the R.F.I. filters, thus eliminating a series power connection.

D. CONTROL BOARD NO. 1

This board contains all word data inputs and verify signals from and to the I.U. computer. Redundant pins to carry these functions are arranged on one side of the board and are hard wired directly to connectors J_1 and J_4. Circuitry on this board includes the Control Register, Steady State Flip-Flop Register and Sequence Gates, Verify Register and Verify Drivers, shown

schematically in Figure 13. As stated previously, this board is of two-sided construction and will be the upper board in the electronic sub-assembly. All flat pack leads will be doubled welded. The edge opposite the input pins contains the plated thru padded holes which line up with similar holes on Control Board No. 2 and are interconnected with flexible printed cabling containing redundant conductors and termination pins.

E. CONTROL BOARD NO. 2

Inputs and outputs to Control Board No. 2 associated with Control Board No. 1 are interconnected as described above through use of flexible cabling. This board is of the same construction as Control Board No. 1 and contains the Stage Select, Read and Reset circuitry, System Clock, Delayed Clock and Shift Pulse Driver shown schematically in Figure 14. Control Board No. 2 and the Diode Driver and Array board are interconnected with redundant flexible printed circuit cabling.

F. DIODE DRIVER AND ARRAY BOARD

This board is of multilayer construction. All circuitry is routed on four internal layers which are interconnected by means of plated through holes. Power and ground are distributed to their required points by means of a power plane which minimizes IR drops that a single power conductor would see. The diode driver and array board is comprised of 16 driver circuits and the diode decode array. As described in the Phase I Completion Report, initial design layout was attempted utilizing the FSA-1184, eight, common cathode integrated diode array, to implement the decode function. Subsequent investigation showed that this function could be implemented with a minimum of interconnections, using the FSA-1182, four, common anode diode array. The diode driver and array board is interconnected to the DT L Decode board with redundant flexible printed circuit cable. This board contains all circuitry shown schematically in Figure 16. All transistors and diodes used in the drivers and array are in redundant pairs for added reliability.

G. DTμL DECODE BOARD

This board is of multilayer construction and is comprised of 7 layers, 5 of which are internal and used to route the circuitry required for the 226 (14 lead) flat packs mounted on the external layers. The flat packs contained on this board are connected in parallel redundant configuration. All flat pack leads will be doubled welded. Two of the internal layers are copper planes for power distribution. The three additional layers are used for routing input, output and interconnecting circuitry. The DTμL Board is interconnected to the output driver wiring board with flexible printed circuit cabling. All circuitry mounted on this board is shown schematically in Figure 17.

H. OUTPUT DRIVER WIRING BOARD

This board is of multilayer construction and is comprised of 6 layers. It is used for the mounting of the output modules described below. The internal layers route all input signals from the DTμL Decode board to their respective drivers and in turn route the output of the drivers to pins on the edge of the board. These pins are hard wired to the J_2 and J_3 connectors.

I. DRIVER MODULE

This module is a cordwood nickel ribbon welded assembly encapsulated with Stycast 1090 compound. Its physical dimensions are 4.0" x .500" x .400" high. All pins for inputs, outputs, power and T/M are located on the .500" x 4.0" side to match holes on the output driver board which carries the circuitry for the module. Figure 22 depicts the construction of the module type to be used.

J. INTERCONNECTIONS

As mentioned in the discussions above, all board-to-board interconnections will be accomplished by means of flexible printed cabling. The cable chosen for this application is currently being used in the Minuteman and Polaris programs. Manufactured by Digital Sensors Inc., under the trade name "Flex-Weld Cable", this cable offers a greater degree of reliability than the types previously available. This increase in reliability is brought about by virtue of the technique used in terminating the ribbon conductors at the edge of the assembly. This is accomplished by welding through the

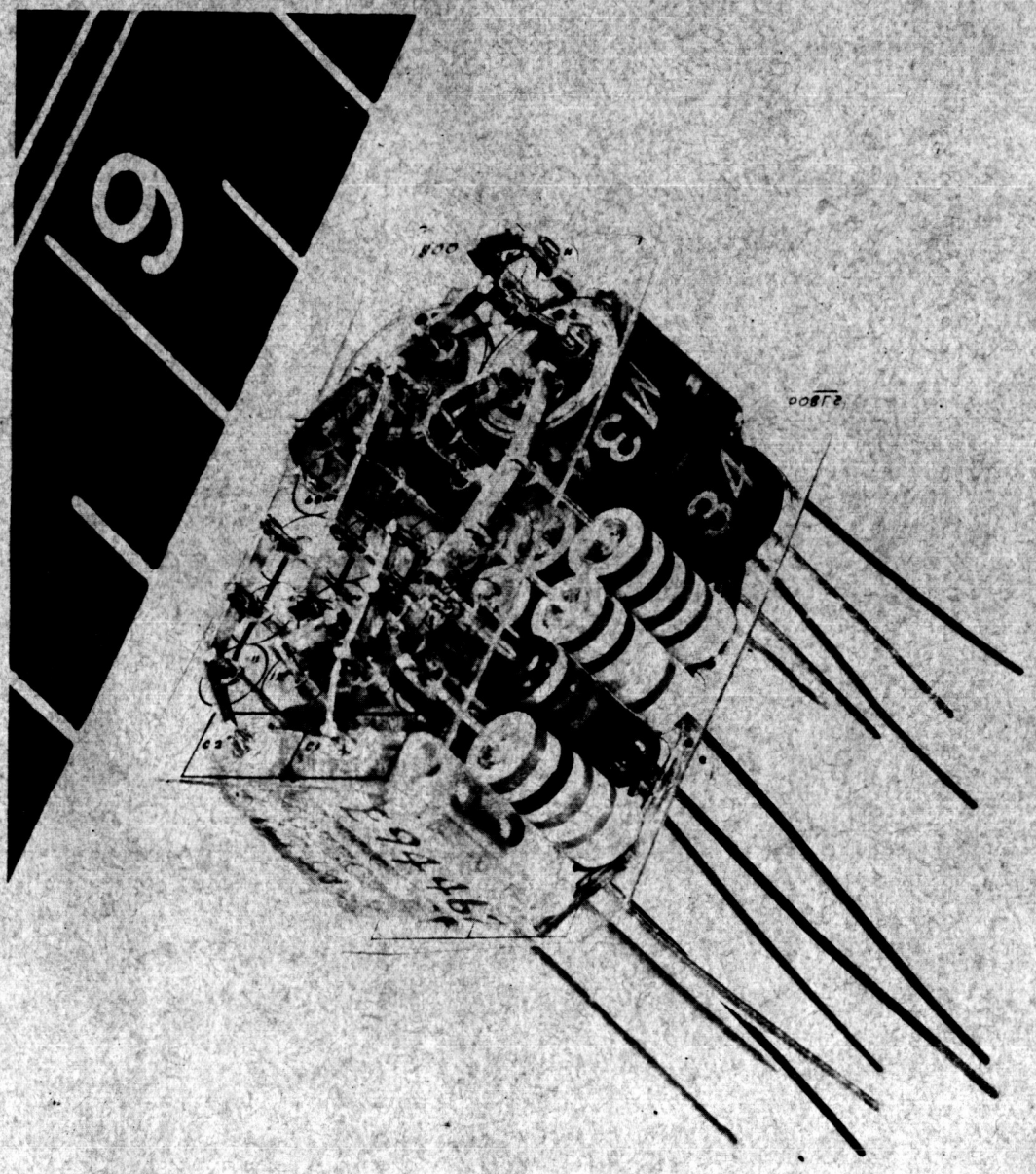


FIGURE 22. WELDED MODULE CONSTRUCTION

insulation to terminating pins and then stress relieving the entire edge with flexible potting to prevent a stress concentration where the change in cross-section occurs.

The use of these printed cables is shown in the Switch Selector Assembly Figure 21.

K. THERMAL DESIGN CONSIDERATIONS

The entire Switch Selector Assembly dissipates a total average power of approximately six watts. This power is equally divided between the I.U. and Stage supplies. The major portion of the power drawn from the I.U. supply is dissipated in the dropping resistor as part of the zener diode regulator supplying the Verify Register. This resistor is the single source of concentrated heat in the system and consequently is heat sinked directly to the casting. The resistor used is a MIL type RE-65 made specifically for heat sink mounting, and is situated on the bottom of the casting such that heat flow is directly through the mounting surface to the cold plate.

The dissipated power drawn from the Stage supply is distributed throughout the entire electronic sub-assembly. The major source of heat is the DT μL Board No. 3 where each of 226 flat packs dissipates an average of five milliwatts, totally 1.13 watts. In order to evenly distribute this heat over the entire board and allow for maximum thermal conduction, the surface is plated with a heat sink layer, the pattern of which is designed for optimum heat distribution. Each flat pack then is firmly mounted to the heat sink surface as desired.

Due to the physical distribution and minimal nature of other sources of heat in the system, no special thermal design precautions were necessary.

L. SUMMARY

The proposed Switch Selector assembly resulting from the package design phase is shown in Figure 21. Incorporated in this design are several techniques which are considered developmental in the field of high reliability micro-electronic packaging. These include, (a) multilayer printed circuit boards (b) board surfaces capable of being welded or soldered to, (c) double

welding of integrated circuit flat-pack leads, (d) flexible printed circuit cabling, (e) welded module construction, and, (f) redundancy of circuit components and interconnections.

SECTION IV

RELIABILITY ANALYSIS

A. INTRODUCTION

The reliability analysis presented in the Phase I Completion Report is reviewed and updated to include the results of the Phase II effort.

B. RELIABILITY CALCULATIONS

1. Tabulation of Component Failure Rates

The following table lists the failure rates utilized in the calculations below. The figures shown are based upon the utilization of high reliability components, i.e., preferred and guidance type semiconductors, Fairchild FACT semiconductors and integrated circuits, and Minuteman discrete components.

COMPONENT	FAILURE RATE
Fairchild Integrated Circuit	$.032 \times 10^{-6}$ failures/hour
Fairchild Planar Transistors	$.02 \times 10^{-6}$
Diode - Diffused Silicon - Unitrode	$.03 \times 10^{-6}$
Resistor Comp.	$.002 \times 10^{-6}$

COMPONENT	FAILURE RATE λ
Capacitor, Solid Tantalum	$.04 \times 10^{-6}$ failures/hour
Inductor R.F.	$.01 \times 10^{-6}$
Transformer, Pulse	$.02 \times 10^{-6}$
Magnetic Core	$.01 \times 10^{-6}$
Solder Connection	$.005 \times 10^{-6}$
Welded Connection	$.005 \times 10^{-6}$
Connector	$.005 \times 10^{-6}$ (per active pin)
Printed Circuit Board (2-sided)	$.07 \times 10^{-6}$
Printed Circuit Board (multi-layer)	$.03 \times 10^{-6}$ per layer (estimated)

2. Control Register and Interface Drivers λ_1

8 Magnetic Core Modules Including:

8 Magnetic Cores	$.08 \times 10^{-6}$
8 Fairchild Transistors	$.16 \times 10^{-6}$
8 Resistors	$.016 \times 10^{-6}$
8 Capacitors	$.32 \times 10^{-6}$
8 Pulse Transformers	$.16 \times 10^{-6}$
	0.736×10^{-6}

8 Redundant Interface Drivers including transistors, base resistors and interconnections	$.20 \times 10^{-10}$
24 Resistors $24(.002 \times 10^{-6})$	$.048 \times 10^{-6}$
8 Diodes $8(.03 \times 10^{-6})$	$.24 \times 10^{-6}$
168 Solder Connections $168(.005 \times 10^{-6})$	$.840 \times 10^{-6}$
TOTAL λ_1	1.864×10^{-6}

3. Steady State Register and Sequence Gates λ_2

6 Integrated Circuits $6(.032 \times 10^{-6})$	$.192 \times 10^{-6}$
84 Redundant Weld Connections	$.176 \times 10^{-12}$
TOTAL λ_2	

4. Diode Drivers λ_3

Non Redundant λ of Driver Circuits

32 Transistors $32(.02 \times 10^{-6})$	$.64 \times 10^{-6}$	
48 Resistors $48(.002 \times 10^{-6})$	$.096 \times 10^{-6}$	
192 Solder Connections $192(.005 \times 10^{-6})$	$.960 \times 10^{-6}$	
TOTAL REDUNDANT λ_3		2.9×10^{-10}

5. Diode Decode Array λ_4

Non Redundant λ	1.96×10^{-6}	
Total Redundant λ_4		3.85×10^{-10}

6. DTγL Integrated Circuit Decode Logic λ_5

Non Redundant λ	8.56×10^{-6}	
Total Redundant λ_5		73.4×10^{-10}

7. Output Drivers λ_6

Non Redundant λ	8.7×10^{-6}	
Total Redundant λ_6		76×10^{-10}

8. Control Logic λ_7

3 Redundant Magnetic Core Modules and Driver Circuitry	$.15 \times 10^{-10}$
15 Resistors	$.03 \times 10^{-6}$
10 Diodes	$.3 \times 10^{-6}$
7 Capacitors	$.28 \times 10^{-6}$
5 Integrated Circuits	$.160 \times 10^{-6}$

2 Pulse Transformers	$.04 \times 10^{-6}$
72 Non Redundant Solder Connections	$.036 \times 10^{-6}$
9 Redundant Transistors, Base Resistors and Interconnections	$.22 \times 10^{-10}$
TOTAL λ_7	0.846×10^{-6}

9. DC-DC Converter λ_8

4 Transistors $4(.02 \times 10^{-6})$	$.08 \times 10^{-6}$
10 Capacitors $10(.04 \times 10^{-6})$	$.40 \times 10^{-6}$
1 Inductor - $.01 \times 10^{-6}$	$.01 \times 10^{-6}$
4 Transformers $4(.02 \times 10^{-6})$	$.08 \times 10^{-6}$
12 Resistors $12 (.002 \times 10^{-6})$	$.024 \times 10^{-6}$
88 Solder Connections $88(.005 \times 10^{-6})$	$.44 \times 10^{-6}$
TOTAL λ_8	1.21×10^{-6}

10. Printed Circuit Boards λ_9

Control Logic Board 1	$.07 \times 10^{-6}$
Control Logic Board 2	$.07 \times 10^{-6}$
Diode Decode & Driver Board	$.18 \times 10^{-6}$
DT L Decode Board	$.21 \times 10^{-6}$
Output Driver Board	$.18 \times 10^{-6}$
TOTAL λ_9	$.71 \times 10^{-6}$

11. Interconnections λ_{10}

Main Connector to Board 1	
20 Redundant Connections	Negligible
3 Non Redundant Connections	$.015 \times 10^{-6}$
Board 1 to Board 2	
27 Redundant Connections	Negligible
Board 2 to Board 3	
19 Redundant Connections	Negligible
Board 3 to Board 4	
36 Redundant Connections	Negligible

Board 4 to Board 5

117 Non Redundant Connections $.585 \times 10^{-6}$

Board 5 to Main Connector

115 Non Redundant Connections $.575 \times 10^{-6}$

TOTAL λ_{10} 1.175×10^{-6}

12. Connectors λ_{11}

2 - 32 pin $.08 \times 10^{-6}$

2 - 64 pin $.15 \times 10^{-6}$

TOTAL λ_{11} $.23 \times 10^{-6}$

The failure rates λ_1 through λ_{11} represent the unreliability of those components in the system whose normal operation is considered essential for mission success.

The total system failure rate λ_T is;

$$\lambda_T = \lambda_1 + \lambda_2 + \text{-----} \lambda_{11}$$

$$\lambda_T = 6.24 \times 10^{-6} \text{ failures/hour}$$

The system reliability is;

$$R_T = e^{-6.24 \times 10^{-6} \times t}$$

where t = 100 hours

$$R_T = 0.99938$$

These calculations have assumed a K factor equal to unity for orbital time. If the worst case K factor, for a total of all stage burn times, is used, (see Table II of the Saturn Flight Control Study NAS8-5469, prepared by IBM Space Guidance Center, Oswego, New York) the following is obtained:

Total Stage Burn Time = 0.280 hours

$$K = 60$$

$$\therefore \; R_P \text{ (Burn Time)} = e^{-\lambda Kt}$$

$$= e^{-6.24 \times 10^{-6} (60)(.28)}$$

$$R_P = 0.999868$$

Therefore the environmental K factor effects the system reliability by,

$$R_T = .99938 \times .999868$$

and

$$\boxed{R_T = .999248}$$

C. SUMMARY

The system reliability has been calculated to be 0.99925 for a 100 hour orbital mission. In the analysis above, no consideration has been given to the increase in reliability obtained by virtue of the Verify function. The compliment

redundancy resulting protects against a number of single failures in the Control Register and Steady State Flip-Flop Register, any one of which was considered catastrophic in the analysis given. Further, no criticality analysis was performed but rather, all failures were considered.100% critical making the end result relatively conservative.