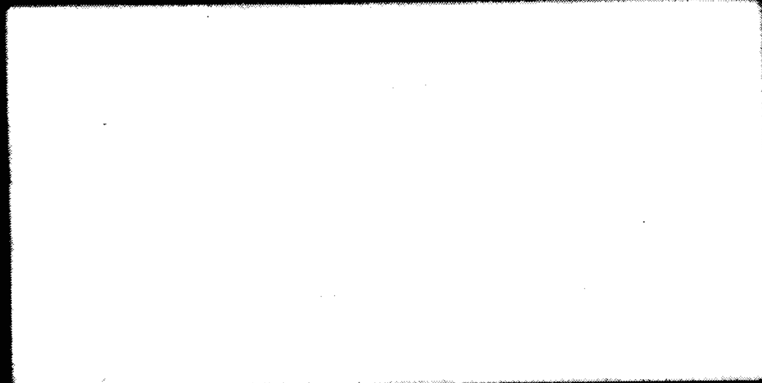
https://ntrs.nasa.gov/search.jsp?R=19650016372 2020-03-17T01:43:08+00:00Z

N65-25973
(ACCESSION NUMBER) (THRU)
70 1
(PAGES) (CODE)
CR 63334 09
(NASA CR OR TMX OR AD NUMBER) (CATEGORY)
FACILITY FORM 602

GPO PRICE $ ______
OTS PRICE(S) $ ______
Hard copy (HC) 3.00
Microfiche (MF) .75



development · research · manufacture

components · systems · instruments

BARNES ENGINEERING COMPANY

30 Commerce Road Stamford, Connecticut

BEC PROJECT NO. 4290

BARNES ENGINEERING COMPANY 30 COMMERCE ROAD STAMFORD, CONNECTICUT

Prepared For

JET PROPULSION LABORATORY
Pasadena, California

JPL Contract No. 950470
under NAS 7-100

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

LOW LEVEL COMMUTATION

USING MOS FET TRANSISTORS

(A Study Report)

Prepared By:

Monty M. Merlen
Project Manager

Jerome M. Pasternak
Project Engineer

Approved By:

E. A. Kallet, Manager
Space Systems Dept.

Robert W. Astheimer
Technical Director
Defense and Space Division

Dated: 2 April 1965

TABLE OF CONTENTS

SECTION		PAGE
1.0	INTRODUCTION	1-1
2.0	ENHANCEMENT MODE TYPE MOS FET	2-1
	2.1 MOS FET PROBLEMS	2-1
3.0	EXPERIMENTAL LOW LEVEL COMMUTATOR	3-1
4.0	COMMUTATOR SYSTEM PERFORMANCE	4-1
	4.1 TEMPERATURE TEST CONDITIONS	4-1
	4.2 TEMPERATURE TEST AND OVERALL COMMUTATOR PERFORMANCE RESULTS	4-5
5.0	CONCLUSION AND RECOMMENDATIONS	5-1
APPENDIX I	- LOW LEVEL COMMUTATOR SYSTEM DESCRIPTION	I-1
APPENDIX II	- TEMPERATURE TESTS OF GME TYPE 2N3610 MOS FET TRANSISTORS	II-1

LIST OF ILLUSTRATIONS

FIGURE NO.	TITLE	PAGE
2-1	CROSS-SECTIONAL VIEW OF MOS FET	2-2
2-2	MOS FET'S DRAIN CHARACTERISTICS NEAR THE ORIGIN	2-3
3-1	SYSTEM TO EVALUATE MOS FET TRANSISTORS, BLOCK DIAGRAM	3-3
3-2	WAVESHAPES AT VARIOUS POINTS INDICATED IN SYSTEM BLOCK DIAGRAM	3-4
4-1	PERFORMANCE OF MOS FET COMMUTATOR AT -50°C	4-2
4-2	PERFORMANCE OF MOS FET COMMUTATOR AT +25°C	4-3
4-3	PERFORMANCE OF MOS FET COMMUTATOR AT +90°C	4-4

ACKNOWLEDGEMENT

The illustrations showing the cross-sectional views of an MOS FET and their characteristics near the origin were obtained from General Micro-electronics, Inc. Application Notes; Vol. 1, No.2.

1.0 INTRODUCTION

An operative no moving parts Horizon Scanner was delivered to J.P.L. in October, 1964. The device incorporated a low level commutator that sequentially sampled the outputs of 90 thermopile detectors. Although the commutator operated adequately, it was relatively large (6" x 6" x 1"), heavy (over 1 lb.), and required appreciable drive power (approx. 0.5 watts). In addition, its speed of operation was inherently slow (3.3 milliseconds/sample) and it could operate satisfactorily only over a limited temperature range (+30 to + 70°C). If the scanner had to operate outside the restricted temperature range, additional power (up to 2 watts) would be required to heat or cool the commutator.

The delivered commutator operated by sequentially illuminating 90 cadmium selenide photo resistors (one in series with each thermopile detector) with the light output from 90 associated neon bulbs. (These bulbs required preselection to obtain satisfactory dark firing characteristics).

Each bulb was sequentially actuated by applying 200 volt pulses through associated series dropping resistors. The high voltage requirement precluded using standard preferred parts (all of which have relatively low voltage ratings) to perform this function.

The above mentioned disadvantages of photo-resistive commutation made it most desireable to consider alternate methods for low level switching. The most promising approach was to utilize the recently developed MOS type Field Effect Transistors, instead of the neon bulb- cadmium selenide cell combination currently used. In addition to requiring minimal drive power, and providing unrestricted operation over a wide temperature range, these MOS type transistors are also ideally suited for incorporation in microminiature integrated circuits.

2.0 ENHANCEMENT MODE TYPE MOS FET

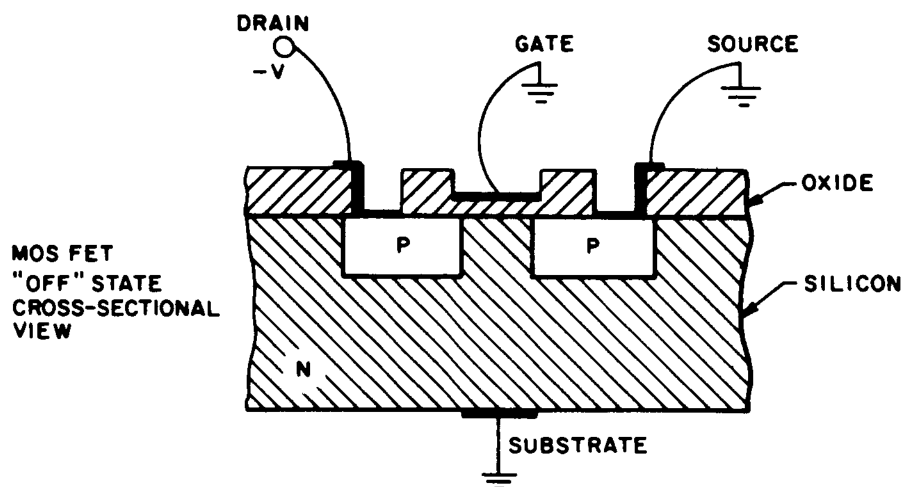
Metal Oxide Silicon Field Effect Transistors (MOS FET) of the enhanced mode type offer numerous advantages over other forms of solid state devices when used as low level commutator switch elements. This device, shown in Figure 2-1, consists of "drain" and "source" terminals of "P" type material diffused into an "N" type silicon substrate. (The complimentary form of FET has "N" type "drain" and "source" terminals diffused into a "P" type substrate). The surface of the material is oxide insulated, and a conducting area called the "gate" is deposited over the oxide. In operation, a negative field applied between the gate and substrate repels electrons at the "N" region surface and draws holes from the "P" terminals into this area. Thus, a thin layer of conducting "P" material is formed between the source and drain. The magnitude of the transverse field varies the thickness of this depletion layer (conduction is enhanced with increased potentials), and hence, path resistance.

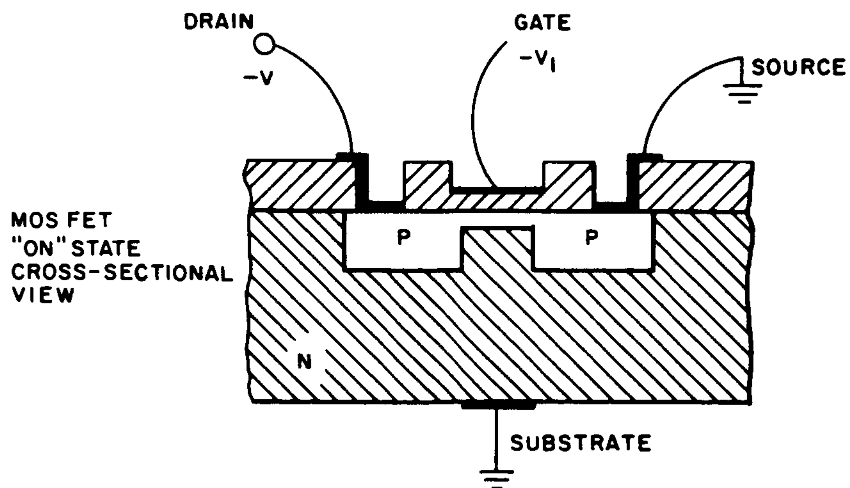
In this type of device no junctions are crossed when current flows between source and drain. The device therefore behaves as a variable resistor, whose value is controlled by the applied gate voltage. The resistance characteristics at any fixed gate voltage remain linear for values of source-drain voltage low enough to prevent field distortion. (See figure 2-2). In addition, because of the high insulation resistance ($>10^{12}$ ohms) of the oxide layer under the gate electrode, insignificant power is required from the driving source, and negligible leakage current flows into the signal path to create spurious potentials. Furthermore, in a multi-channel commutator configuration, only one enhanced mode transistor would be gated on at any one time. Therefore, only gating drive current from the single "on" transistor could leak through to the low level commutated signals output, irrespective of the number of channels being commutated.

Typical MOS FET devices display "on" resistance of several hundred ohms, and "off" resistances greater than 10^8 ohms. This high ratio provides extremely efficient switching action, while the gate leakage currents are normally too small to affect even microvolt level input signals.

2.1 MOS FET PROBLEMS

The foregoing properties of the MOS FET make it appear ideally suited for use in a multi-channel low level commutator. However, two significant problems exist.





21626

Figure 2-1 CROSS-SECTIONAL VIEW OF MOS FET

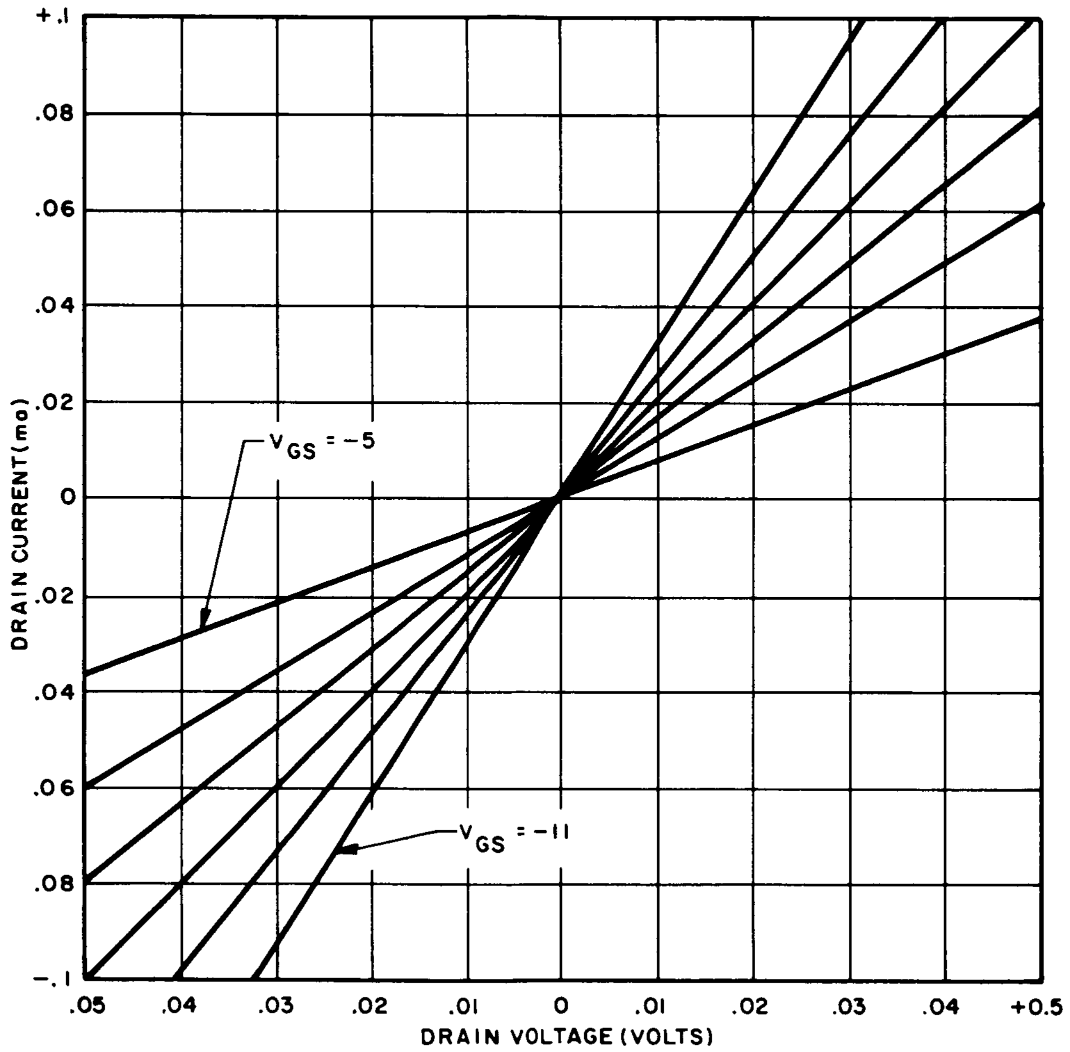


Figure 2-2 MOS FET'S DRAIN CHARACTERISTICS NEAR THE ORIGIN

The first problem involves a switching spike that appears on the signal output whenever an FET is gated "on" or "off". Although their durations are very short, these spikes could cause the amplifier following the commutator to saturate, and may induce spurious residual charges on band pass limiting capacitors. At the amplifier output, these residual charges would appear as spurious signals that varied as different FET's, with different inherent characteristics, were commutated. This problem can be solved by setting the amplifier's gain and bandwidth so saturation does not occur and by not "looking" at the amplifier output signal while the short duration transition spikes are present.

The second problem is caused by thermocouple action between the dissimilar materials of the device body and connecting leads. Typically, terminal leads connected to the silicon body produce EMF's in the order of 400 microvolts per degree centigrade. Therefore, a microvolt level switch must be constructed so as to avoid temperature differences along the device and its leads greater than $1/400^{\circ}C$.

3.0 EXPERIMENTAL LOW LEVEL COMMUTATOR

A single pole, five throw MOS FET Switch was constructed, along with the necessary associated electronics, to demonstrate the feasibility of a solid state, microvolt level commutator. Incorporated therein were the necessary techniques to eliminate the dual problems relating to spurious thermal potentials and to amplifier saturation from commutation transition spikes.

The commutator was tested at -50°C, +25°C and +90°C ambient temperatures. Spurious potentials generated within the commutator were less than ± 1 microvolt over the test range of ambient temperature conditions. This level is adequately low to permit satisfactory operation in the Lunar and Planetary Horizon Sensor. In addition, by refining the techniques utilized, these spurious potentials can be further reduced.

The basic commutator utilized five FET's . They were mounted on an isothermal test fixture designed to minimize temperature differences between each transistor and its associated leads. (See Appendix I). The five transistors were interconnected to function as a five input, single output commutator switch. Low level D.C. input signals were provided thereto by means of five associated logarithmic potentiometers and five subsequent 1000:1 attenuator networks. The output impedance of each attenuator network was 1000 ohms, which simulated the output impedances of the thermopile detectors that are eventually to be commutated.

A five stage ring counter were used to sequentially provide -20 volt pulses to the gates of the FET commutator transistors. These pulses caused the transistors to be sequentially gated on, permitting their associated imputs to be sampled one at a time.

The transition spikes at the commutator output (caused by the capacitive coupling of leading and trailing edges of the gating drives through the FET gate to source and drain capacitances) were reduced in amplitude by means of a .0047 mfd bypass capacitor. The resultant spikes were sufficiently small in amplitude so saturation did not occur in the subsequent low level (approximately 1 μ volt imput noise) 2800 gain signal amplifier. The amplifier's bandwidth (high and low frequency cutoffs of 3 and 3000 cps, respectively) was adequately wide to permit commutator sampling times of 2 milliseconds duration to be accommodated without causing excessive "overshoots", signal "droops", or "stretching" of the transient commutator spike into the sampling period.

The sampling time of two milliseconds was obtained from an external "clock" square wave oscillator. This drove a 500 micro-second monostable multivibrator, and the leading edge of the resultant pulses therefrom were used to trigger the five count ring counter.

The 500μ sec pulse was also applied to a high level transistor switch which was connected,in series, between the signal amplifier's output and a subsequent low pass final output filter which set the system's upper frequency response limit to 800 cps. The pulse from the monostable multivibrator "opened" the series output switch simultaneously with the arrival of the input commutator transient "spike", and held it open for a period of 500 microseconds. This effectively prevented the amplified spurious gating pulse (which, referred to the input, decayed to under a microvolt in less than 150 microseconds) from being fed into the 800 cps low pass output filter. The output switch was permitted to close for the 1.5 millisecond remainder of each 2 millisecond sample period allowing the output filter to be driven to the amplified level of the input signal being sampled.

The system block diagram is shown in figure 3-1. The various elements that comprise the system are described in detail in the appendix of this report. Figure 3-2 shows oscilloscope photographs of gating drive signals, transient "spike" waveshapes, and commutated signals taken at indicated points on the block diagram.

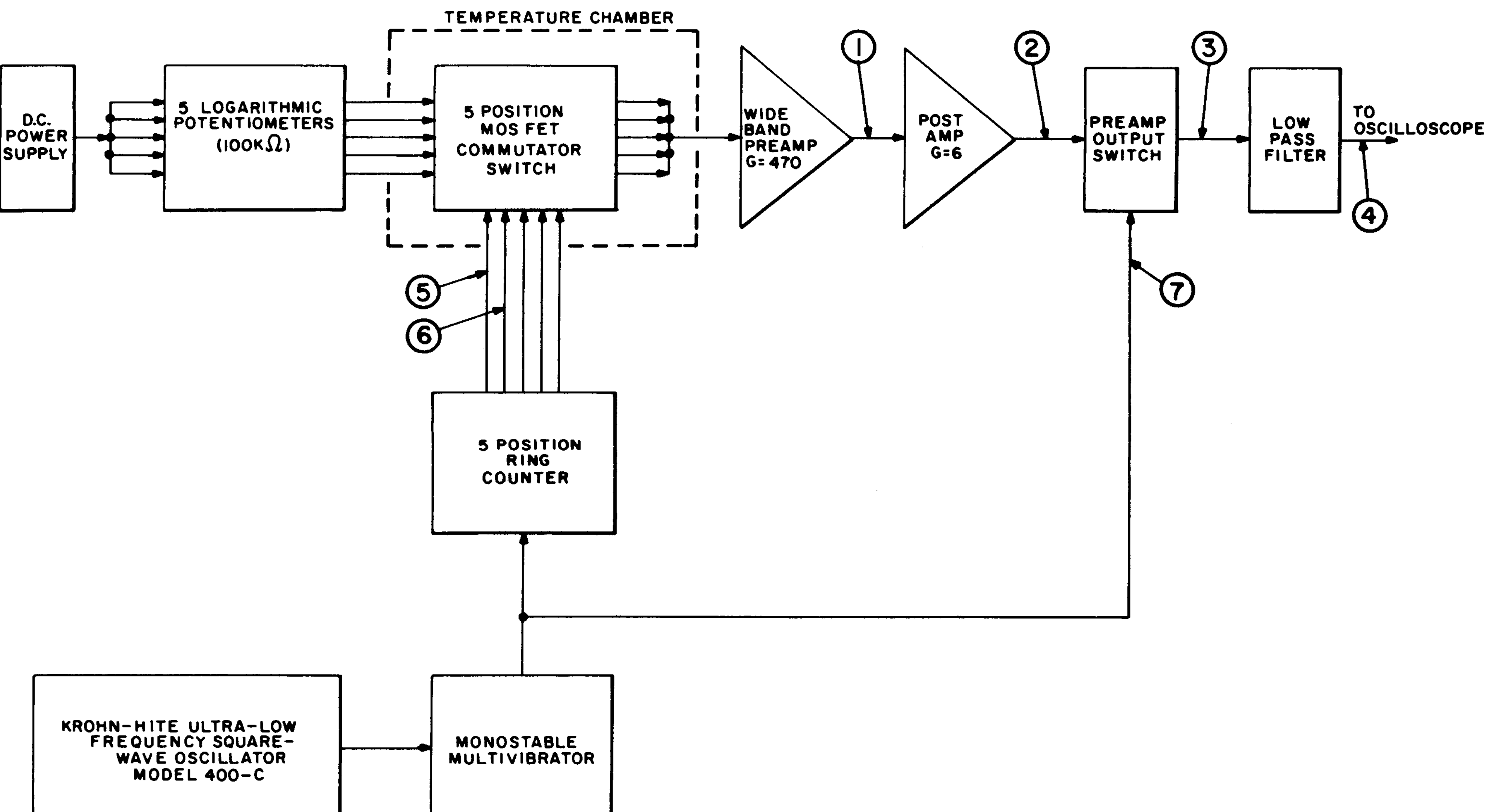
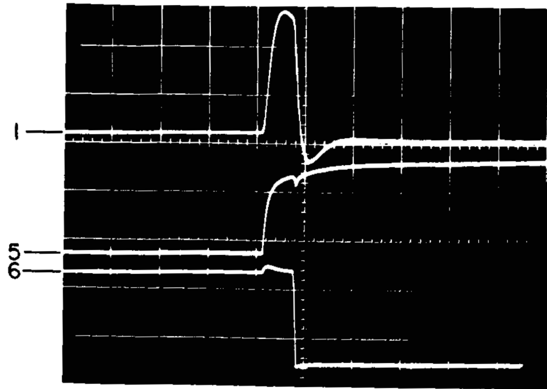
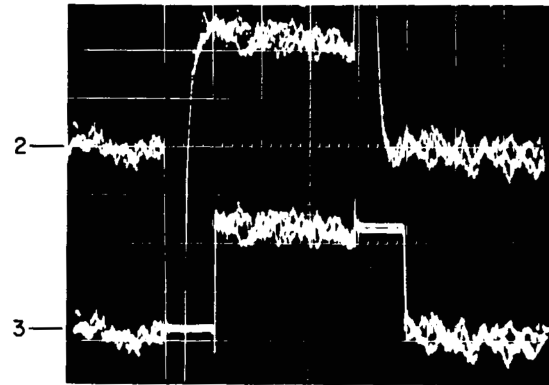


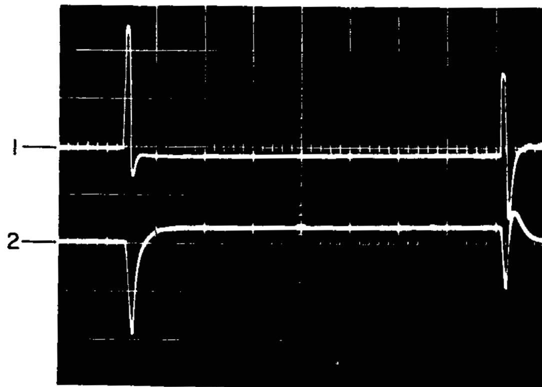
Figure 3-1 SYSTEM TO EVALUATE MOS FET TRANSISTORS, BLOCK DIAGRAM



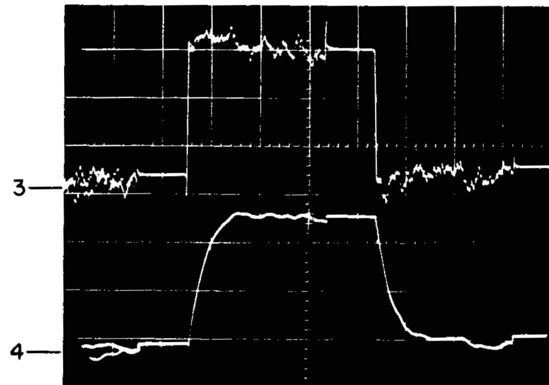
A



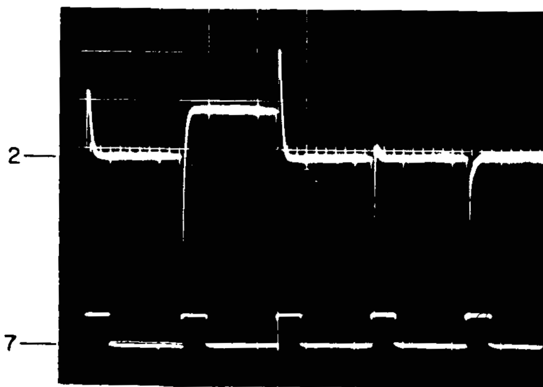
D



B



E



C

	REFERENCE (TO BLOCK DIA)	VERTICAL SCALE FACTOR	TIME BASE
A	1 5 6	0.5V / DIV. 10V / DIV 10V / DIV	50μ SEC / DIV. 50μ SEC / DIV 50μ SEC / DIV
B	1 2	0.5V / DIV 2.0V / DIV	250μ SEC / DIV 250μ SEC / DIV
C	2 7	0.5V / DIV 20V / DIV	1 MS / DIV 1 MS / DIV
D	2 3	10 MV / DIV 10 MV / DIV	500μSEC / DIV 500μSEC / DIV
E	3 4	10 MV / DIV 10 MV / DIV	500μ SEC / DIV 500μ SEC / DIV

21629

Figure 3-2 WAVESHAPES AT VARIOUS POINTS INDICATED IN SYSTEM BLOCK DIAGRM

4.0 COMMUTATOR SYSTEM PERFORMANCE

4.1 TEMPERATURE TEST CONDITIONS

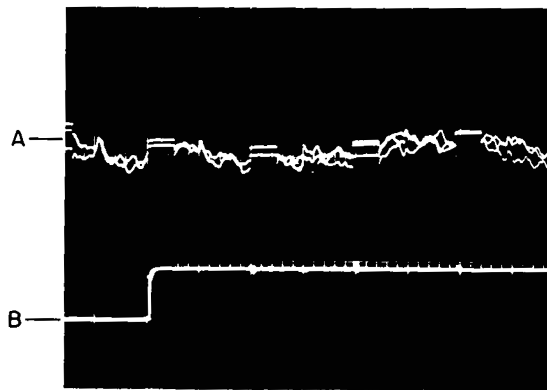
The commutator test fixture was placed within a small laboratory temperature environment chamber. The chamber temperature was then varied between -50°C and +90°C. At -50°, +25°, and +90°C the test fixture was allowed to achieve thermal equilibrium.

Figures 4-1, 4-2, and 4-3 show test results at -50°C, +25°C, amd +90°C. Six photographs were taken at each of these temperatures. The "A" photos show the system's output signal with zero microvolts input to all five commutator channels. The second trace on the "A" photos show the 20 volt negative gating drive into channel number 1. Photos B, C, D, E and F show the resultant outputs with 10 microvolts D.C. input signals into commutator channels one through five, respectively. The second trace on these photos show the 20 volt gating drives into the corresponding channels.

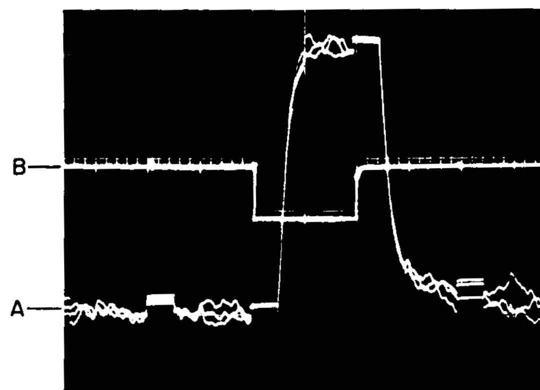
A dual channel Tektronix 504 oscilloscope and a polaroid scope camera were used to obtain the photographs. The signal display channel was set on A.C. input, which eliminated D.C. loading effects at the final breadboard system's output. D.C. loading at this point, in conjunction with the output switch opening and closing at a 500 cps rate, would have produced a spurious 500 cps triangular waveshape at the final system output (caused by the repetitive charging and discharging of the capacitor in the 800 cps output filter).

The measured signal gain of the system, from commutator input to final output, was $\approx$2,800. The signal channel deflection sensitivity of the oscilloscope was set to produce 1 cm of vertical deflection per 5 millivolts of system output signal. This yielded a vertical deflection sensitivity of 1.8 microvolts per centimeter, referred to the commutator input. (5×10^{-3} volts $\div$ 2800 gain = 1.8×10^{-6} volts).

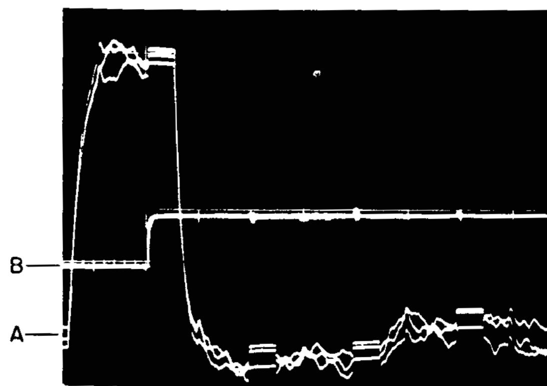
The horizontal time base used in all these photographs was one millisecond per centimeter. This sweep speed permitted all five commutated channels (two milliseconds sampling time duration/channel) to be displayed on every ten centimeter long oscilloscope trace. Two or more traces were utilized in each photograph. This permits some averaging of the signal amplifier's one microvolt (referred to the input) noise level.



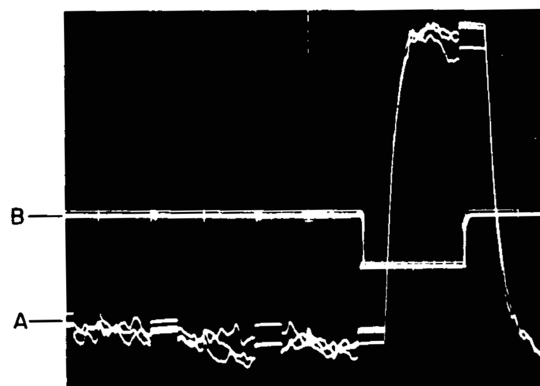
A
A) ZERO MICROVOLTS INPUT
B) GATING DRIVE TO CHANNEL 1



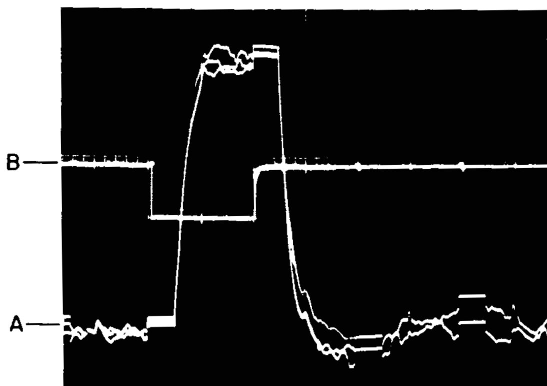
D
A) 10 MICROVOLTS INPUT TO CHANNEL 3
B) GATING DRIVE TO CHANNEL 3



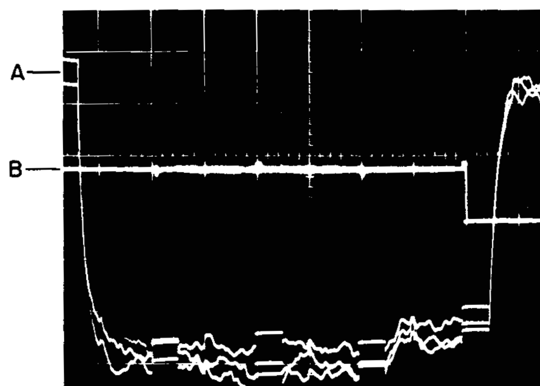
B
A) 10 MICROVOLTS INPUT TO CHANNEL 1
B) GATING DRIVE TO CHANNEL 1



E
A) 10 MICROVOLTS INPUT TO CHANNEL 4
B) GATING DRIVE TO CHANNEL 4



C
A) 10 MICROVOLTS INPUT TO CHANNEL 2
B) GATING DRIVE TO CHANNEL 2

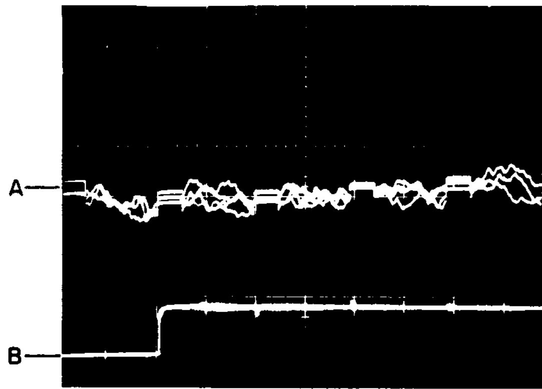


F
A) 10 MICROVOLTS INPUT TO CHANNEL 5
B) GATING DRIVE TO CHANNEL 5

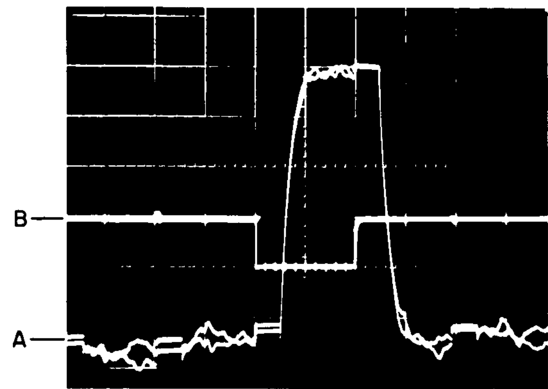
VERTICAL SENSITIVITY OF 'A' CHANNEL: 5 MILLIVOLTS/DIVISION
VERTICAL SENSITIVITY OF 'B' CHANNEL: 20 VOLTS/DIVISION
TIME BASE: 1 MILLISECOND/DIVISION

21630

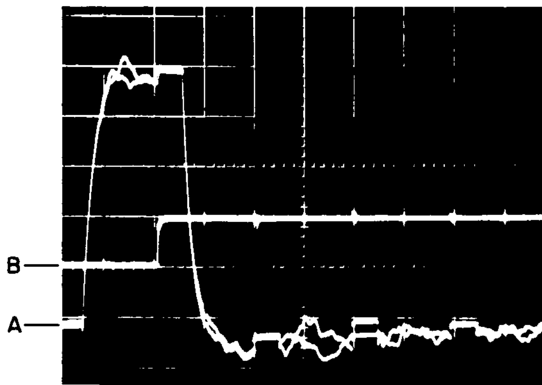
Figure 4-1 PERFORMANCE OF MOS FET COMMUTATOR AT −50°C



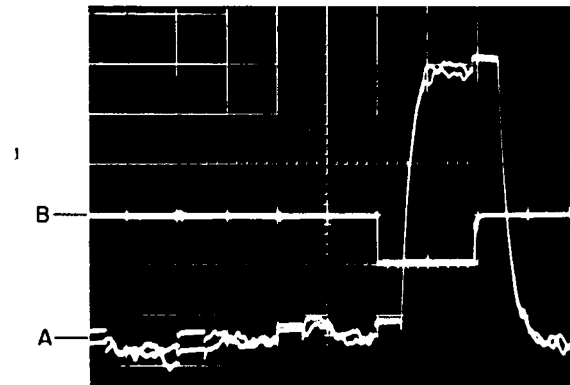
A
A) ZERO MICROVOLTS INPUT
B) GATING DRIVE TO CHANNEL I



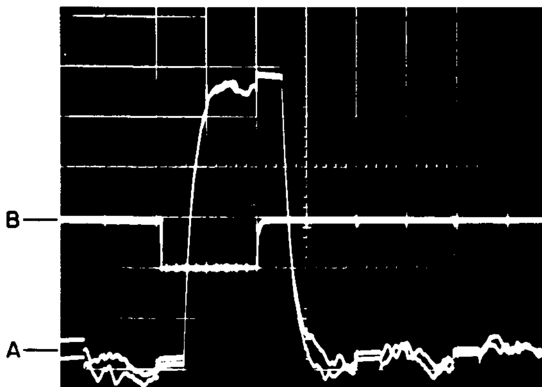
D
A) IO MICROVOLTS INPUT TO CHANNEL 3
B) GATING DRIVE TO CHANNEL 3



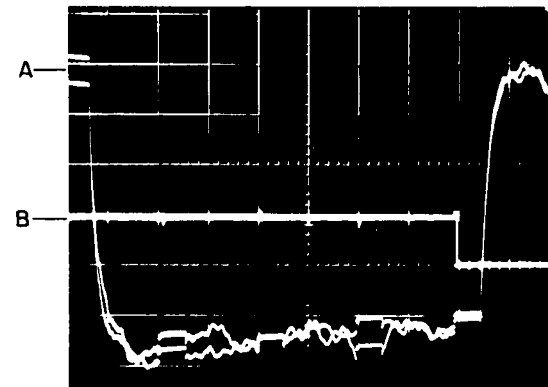
B
A) IO MICROVOLTS INPUT TO CHANNEL I
B) GATING DRIVE TO CHANNEL I



E
A) IO MICROVOLTS INPUT TO CHANNEL 4
B) GATING DRIVE TO CHANNEL 4



C
A) IO MICROVOLTS INPUT TO CHANNEL 2
B) GATING DRIVE TO CHANNEL 2

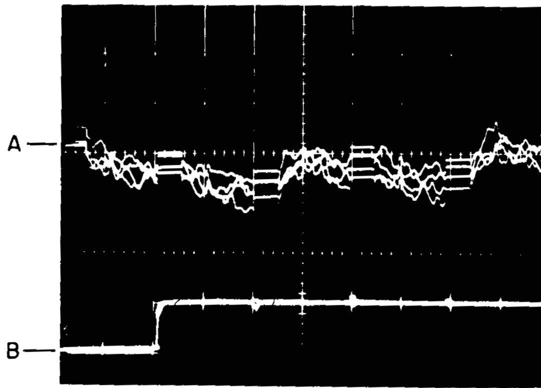


F
A) IO MICROVOLTS INPUT TO CHANNEL 5
B) GATING DRIVE TO CHANNEL 5

VERTICAL SENSITIVITY OF 'A' CHANNEL: 5 MILLIVOLTS / DIVISION
VERTICAL SENSITIVITY OF 'B' CHANNEL: 20 VOLTS / DIVISION
TIME BASE: I MILLISECOND / DIVISION

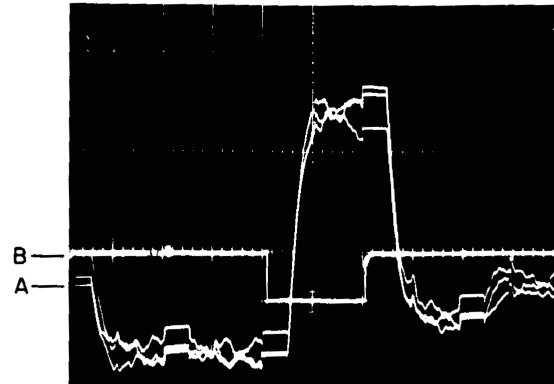
21631

Figure 4-2 PERFORMANCE OF MOS FET COMMUTATOR AT + 25°C



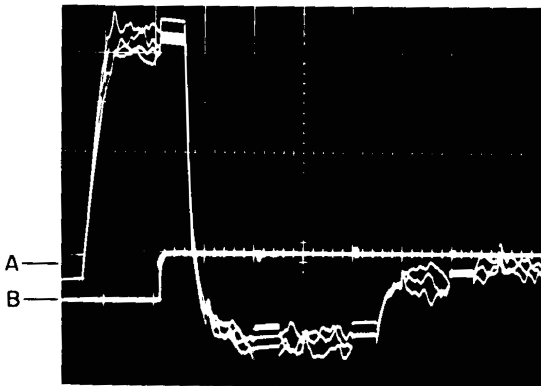
A

A) ZERO MICROVOLTS INPUT
B) GATING DRIVE TO CHANNEL I



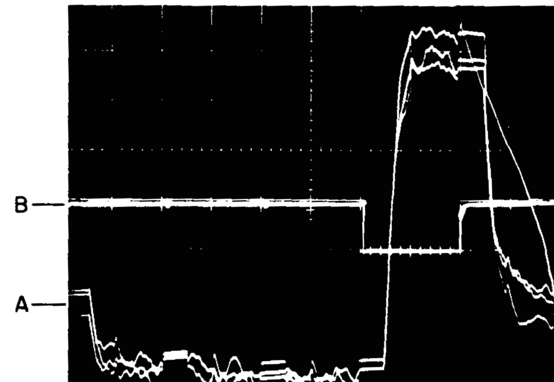
D

A) IO MICROVOLTS INPUT TO CHANNEL 3
B) GATING DRIVE TO CHANNEL 3



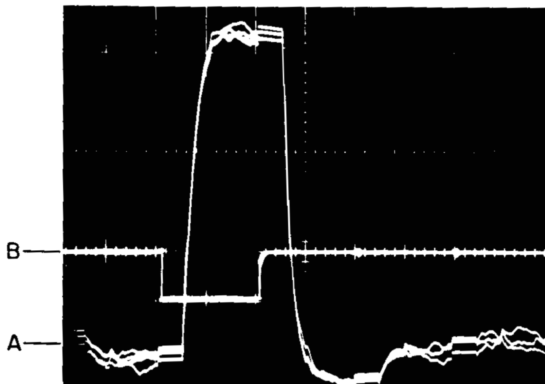
B

A) IO MICROVOLTS INPUT TO CHANNEL I
B) GATING DRIVE TO CHANNEL I



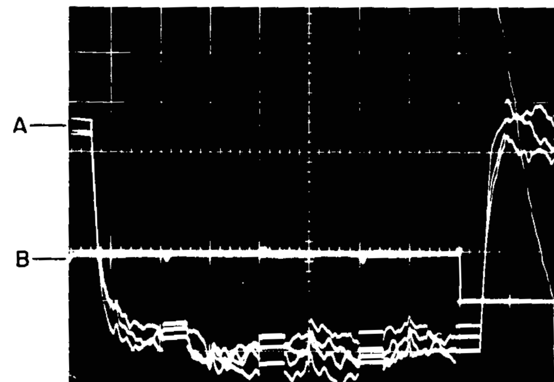
E

A) IO MICROVOLTS INPUT TO CHANNEL 4
B) GATING DRIVE TO CHANNEL 4



C

A) IO MICROVOLTS INPUT TO CHANNEL 2
B) GATING DRIVE TO CHANNEL 2



F

A) IO MICROVOLTS INPUT TO CHANNEL 5
B) GATING DRIVE TO CHANNEL 5

VERTICAL SENSITIVITY OF 'A' CHANNEL: 5 MILLIVOLTS / DIVISION
VERTICAL SENSITIVITY OF 'B' CHANNEL: 20 VOLTS / DIVISION
TIME BASE: I MILLISECOND / DIVISION

21632

Figure 4-3 PERFORMANCE OF MOS FET COMMUTATOR AT + 90° C

The oscilloscope sweep was triggered by the gating drive signal to commutator channel #1. In all photographs, the first sample occupies the first two horizontal divisions, the second sample occupies the next two horizontal divisions, and the third, fourth, and fifth samples are correspondingly displayed.

4.2 TEMPERATURE TEST AND OVERALL COMMUTATOR PERFORMANCE RESULTS

The photographs show the commutator's performance using GME type 1004 transistors, at the three temperatures of interest. With zero microvolts input into all channels, the maximum spurious signal from all five channels is less than plus or minus one microvolt. This test, utilizing another type of MOS FET (GME type 1009) was duplicated. Except for low frequency noise at low temperatures similar results were obtained. This low frequency noise was caused by the low temperature characteristics of the signal preamplifier, which was placed in the environmental chamber along with the commutator. (See Appendix II.C)

The photographs showing the test results obtained with the GME type 1009 transistors are included in Appendix II of this report. It should be noted that some of the transistors used in those tests were damaged. Inadvertant mishandling produced electrostatic charges, which broke down the gate insulation. These transistors were "repaired", but as indicated in the Appendix II photographs, their "on" impedances ranged from 2K ohms to 14K ohms.

The L.P.H.S. system would have accommodated the noted signal variations due to the differences in damaged transistor impedances. It also could have functioned with the low frequency noise that was present.

The photographs (Figures 4-1, 4-2, and 4-3) taken with ten microvolt input signal levels show overall system individual channel gain differences of less than plus or minus 10% under all temperature conditions of interest. The limit of input level setability,

coupled with the plus or minus 20% tolerance 1000: 1 input signal attenuators, could readily produce this degree of variation. Based on manufacturing tolerance variations of individual FET's "on" resistances, the actual gain variations of individual channels in the breadboard system were most likely under 1.5%. This could be further reduced if required in some system other than the L.P.H.S. (where gain variations between different input channels is relatively unimportant), by providing a high input impedance subsequent to the commutator. (In the commutator test setup, a 22K commutator output load resistor was utilized to accentuate, and thereby facilitate measurement of impedance differences of the individual gated "on" FET transistors. If a commutator output load impedance of 220K had been used instead, any gain variations due to variations or differences of "on" impedances of individual transistors would have been reduced by a factor of ten).

The limitations of the test setup most likely produced the plus or minus one microvolt of residual offsets that were noted. Residual temperature gradients in the environmental test chamber produced small temperature differences in the isothermal test fixture. Vertical, instead of lateral orientation of the commutator within the temperatue chamber produced over a microvolt change of the residual offset at the + 90°C test temperature.

A second order effect, that most likely is partially dependent on temperature, concerns the dissimilarity of the individual gating "spikes" produced whenever commutation occurs.

The actual dissymmetry produced is dependent on 1) the non-similarity of waveshapes at adjacent leading and trailing edges of ring counter stage outputs, and 2) the non-similarity and variations of the internal capacitance of the individual FET commutators. Item (2) is somewhat temperature dependent, and therefore, the characteristics of the "spikes" can vary as a function of temperature.

If a net resultant "spike" on a single channel is positive, a "droop" and coresponding negative "overshoot" will occur. This negative overshoot will decay towards zero volts at a rate dependent on the amplifier's low frequency effective time constant. If no other channel has any net resultant "spike", the resultant commutated waveshape would appear as a negative going sawtooth, the leading edge of which would occur coincidently with the positive "spike".

With the 2 cps low frequency break used in the signal amplifier, such an effect was noted, and produced a residual sawtooth of approximately 0.8 microvolts in amplitude. (See A, figure 4-2). When the commutator was operated at elevated temperatures, this effect was masked by the oven temperature gradients, and therefore, any variations thereof could not be noted. The degree of overshoot is dependent on the low frequency time constant of the system. The 0.8 microvolt sawtooth produced by the 2 cps low frequency cutoff of the experimental system amplifier would have been reduced by a factor of a hundred in the L.P.H.S. system, which had an effective low frequency cutoff of 1/50 cps. Therefore, this souce of offsets need not be of concern if an FET commutator is utilized in the L.P.H.S.

5.0 CONCLUSION AND RECOMMENDATIONS

Experimental results leave little doubt as to the practicability of utilizing MOS FET transistors in a low level commutator configuration.

Extremely small size, with minimal weight, can be achieved by fabricating the commutator as an integrated circuit. Gating drive current is minimal, therefore, power required to drive the MOS devices is negligible. This means power consumption is minimized without sacrificing the efficiency of circuit operation.

System noise and drift can be kept low by proper thermal design in critical areas. This includes designing the layout of the commutator transistors so that the drain and source lead terminations are placed immediately adjacent to one another on the silicon chip, and using low thermal conductivity leads to connect to these terminations. In addition, the gate lead termination should be distant from and symmetrically positioned in relation to the source and drain leads. By constructing the individual MOS FETs of the commutator in this fashion, temperature gradient effects due to thermal conduction into the commutator will be minimized beyond what was achieved in the present experiment.

BEC feels that the experimental results are conclusive, and that effort expended in developing an integrated circuit MOS FET commutator will be highly beneficial to the LPHS program.

APPENDIX I

TABLE OF CONTENTS

SECTION		PAGE
I.A	ELECTRONICS	I-1
I.A.1	DETECTOR SIGNAL SIMULATION	I-3
I.A.2	CLOCK OSCILLATOR	I-3
I.A.3	MONOSTABLE MULTIVIBRATOR	I-3
I.A.4	FIVE POSITION RING COUNTER	I-6
I.A.5	FIVE POSITION MOS FET COMMUTATOR	I-8
I.A.6	WIDE BAND PREAMPLIFIER	I-9
I.A.7	POST-AMPLIFIER	I-9
I.A.8	SERIES OUTPUT SWITCH AND OUTPUT FILTER	I-12
I.A.9	OVERALL SYSTEM GAIN VS. FREQUENCY RESPONSE CHARACTERISTICS	I-13
I.B	COMMUTATOR ASSEMBLY DESCRIPTION	I-15
I.B.1	ELECTRICAL CONFIGURATION	I-15
I.B.1.a	ELIMINATION OF COMMUTATOR SWITCHING TRANSIENTS	I-19
I.B.2	THERMAL DESIGN CONSIDERATIONS	I-25
I.B.2.a	THERMAL TEST JIG CALCULATIONS	I-26
I.B.2.b	THERMAL PERFORMANCE	I-29
I.B.2.c	CONCLUSION	I-31

LIST OF ILLUSTRATIONS

APPENDIX IA

NO.	TITLE	PAGE
IA-1	System to Evaluate MOS FET Transistors, Block Diagram	I-2
IA-2	MOS FET Commutator Switch and Detector Signal Simulator	I-4
IA-3	Monostable Multivibrator	I-5
IA-4	5 Position Ring Counter	I-7
IA-5	Wide Band Preamplifier	I-10
IA-6	Post Amplifier, Series Output Switch, and Output Filter	I-11
IA-7	Signal Channel Gain vs. Frequency	I-14

LIST OF ILLUSTRATIONS

APPENDIX IB

NO.	TITLE	PAGE
IB-1	Isothermal Commutator Test Fixture	I-16
IB-2	Typical Layout of a Transistor to its Associated Printed Circuit Pads ((≃ 3 times actual size)	I-17
IB-3	Electrical Schematic of Isothermal Test Fixture	I-18
IB-4	Test Circuit for one Commutator Postion	I-19
IB-5	Capacitive Characteristics of 2N3610 at 25°C	I-20
IB-6	Worst Case Equivalent Circuit (Electrical)	I-21
IB-7	Minimum Transient Equivalent Circuit	I-22
IB-8	Waveshapes at Points indicated in System Block Diagram (Fig. IA-1)	I-24
IB-9	MOS FET Transistor and its Associated Thermal Analog	I-26
IB-10	Thermal Analog: Transistor in Fixture	I-27
IB-11	Transistor Source and Drain: Thermal Analog	I-28
IB-12	Thermal Analog of Commutator Test Fixture (worst case)	I-30

Appendix I

LOW LEVEL COMMUTATOR SYSTEM DESCRIPTION

I.A ELECTRONICS

The system described below was designed to enable the testing of Metal Oxide Semiconductor Field Effect (MOS FET) Transistors for possible use in a low level (1μ volt) commutator. Fig. IA-1 is the system block diagram.

The basic system consists of a monostable multivibrator, driven by differentiated pulses from a 500 cps square wave oscillator. The resultant output is a 500 μ second pulse with a pulse repetition rate of 500 pulses per second. The leading edge of this pulse is used to trigger a 5 count ring counter. The five repetitive sequential outputs from the ring counter are used to drive the gates of field effect transistors, which are arranged in a single pole, 5 throw, solid state commutator switch configuration.

The D.C. inputs to be commutated by the FET transistors are 1000:1 attenuated outputs from five independent logarithmic potentiometers, supplied with 2.2 volts D.C. The sequentially sampled combined output is amplified by a low noise, extended frequency response preamplifier. A post amplifier further amplifies the commutated signal, which then is passed through a series switch. This, in turn, passes the signal into a low pass filter. The series switch is driven by the input monostable multivibrator. The switch disconnects the amplifier output during the 500 μ second time interval while commutation crossover transients are present at the post amplifier's output. The output low pass filter removes the small switching transient present when the output switch actuates and disconnects. It also determines the overall system high frequency cutoff. The individual blocks shown on the system block diagram are as described below.

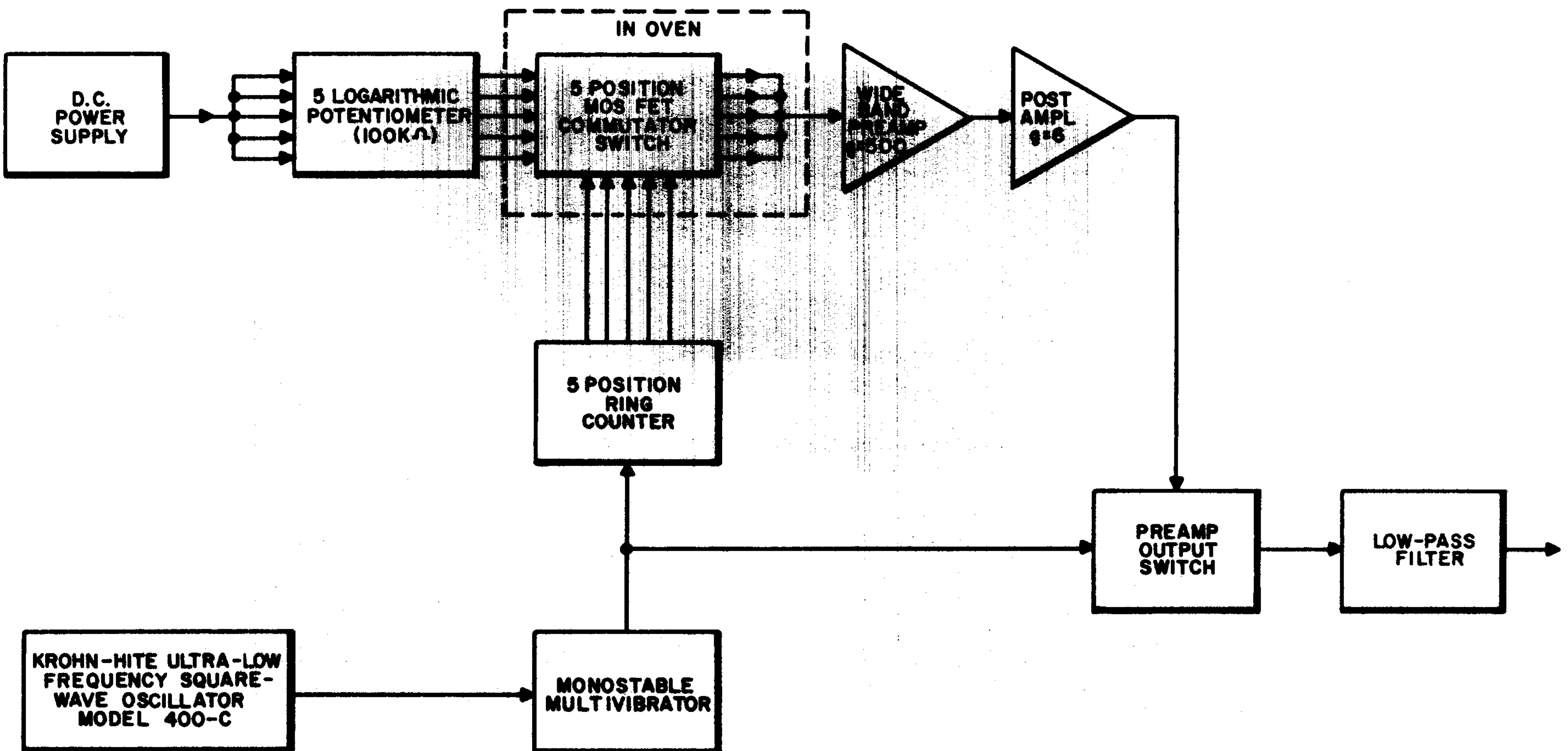


Figure IA-1 SYSTEM TO EVALUATE MOS FET TRANSISTORS, BLOCK DIAGRAM

I.A.1 DETECTOR SIGNAL SIMULATION (Figure IA-2)

Detector output levels are simulated by feeding -20 volts from a D.C. power supply into five variable voltage divider networks, each consisting of resistors R_1, R_2, R_3, R_4. The output voltages of these networks (junctions of R_1, R_2) are adjusted to the 0μv to 1 mv D. C. output levels expected from the thermopile detectors, and are coupled directly to the drains of the MOS FET commutator switches under test.

I.A.2 CLOCK OSCILLATOR (See Block Diagram, Figure IA-1)

A Krohn-Hite Model 400-C low frequency oscillator is used to supply approximately 10 volt, 500 cps square wave clock pulses to a monostable multivibrator. The differentiated positive going edge of the square wave is used to trigger the following monostable multivibrator.

I.A.3 MONOSTABLE MULTIVIBRATOR (Figure IA-3)

C_1, in conjunction with R_1 in parallel with R_2, comprised the differention network that produced the short duration input trigger pulses (waveshape A) for the monostable multivibrator. These positive pulses are fed through R_3 to the base of Q_1 turning Q_1 on. The resultant negative going signal on the collector of Q_1 (waveshape B) couples through capacitor C_2, which turns Q_2 off. R_7, in conjunction with C_2, determines the pulse time duration (waveshape C). Regenerative feedback (waveshape D) is obtained between the emitter of Q_2 and the emitter of Q_1, through the network comprising protect diodes D_1, D_2, and resistor R_5. The final output pulse (waveshape E) appears on the collector of Q_2. The differentiated leading edges of these repetitive pulses trigger the ring counter that follows, and the entire 500 μ second pulse is used to turn off the final output series switch.

-20V

DETECTOR SIGNAL SIMULATOR

COMMUTATOR SWITCH

R3A 820K
R3B 820K
R3C 820K
R3D 820K
R3E 820K

R4A 100K
R4B 100K
R4C 100K
R4D 100K
R4E 100K

R1A 1M
R1B 1M
R1C 1M
R1D 1M
R1E 1M

Q1A
Q1B
Q1C
Q1D
Q1E

D
S
G

R2A 1K
R2B 1K
R2C 1K
R2D 1K
R2E 1K

R5A 100K
R5B 100K
R5C 100K
R5D 100K
R5E 100K

22K

P8 4700

0 VOLTS

OUTPUT, TO PRE-AMP

FROM RING COUNTER OUTPUT NO. 1

FROM RING COUNTER OUTPUT NO. 2

FROM RING COUNTER OUTPUT NO. 3

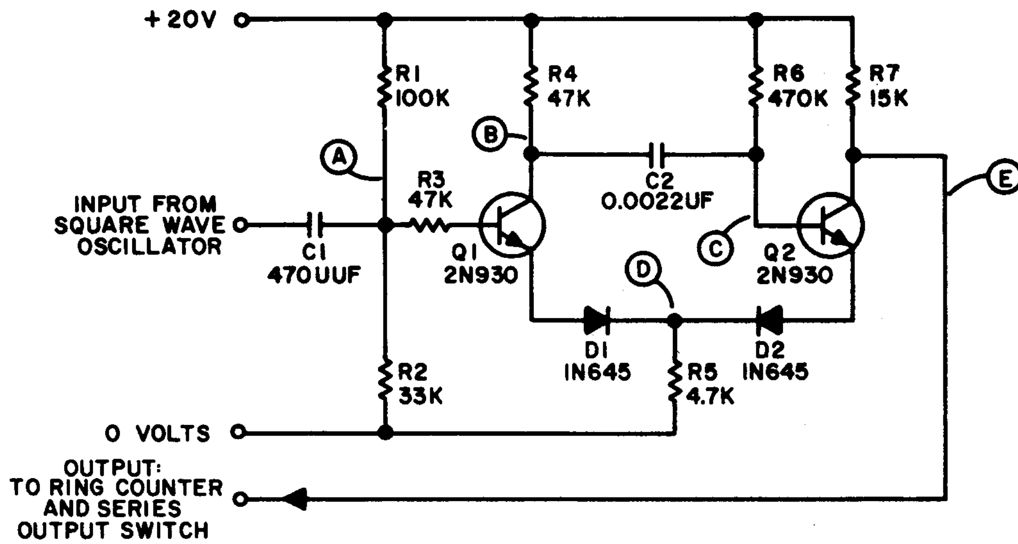
FROM RING COUNTER OUTPUT NO. 4

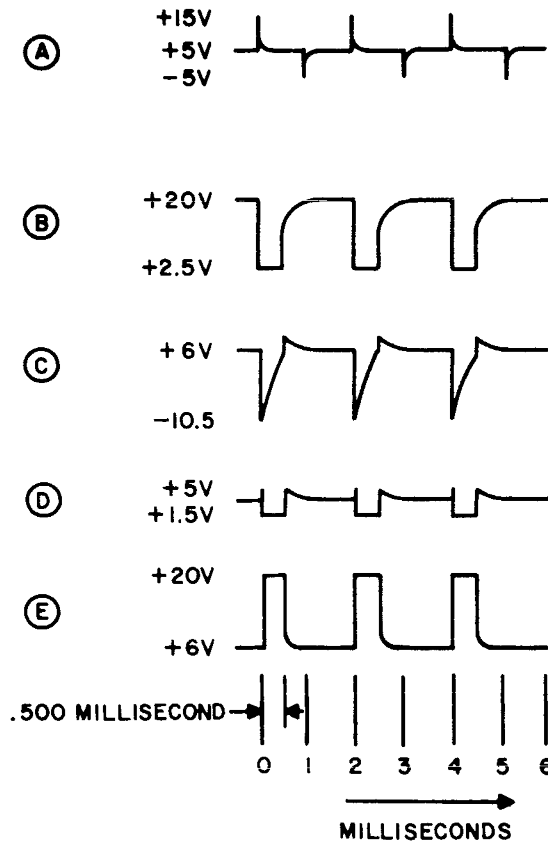
FROM RING COUNTER OUTPUT NO. 5

NOTE: ALL POTENTIOMETERS (5) HAVE LOGARITHMIC TAPER.
Q1 EATHER 2N2608 OR 2N2610

21654

Figure IA-2 MOS FET COMMUTATOR SWITCH AND DETECTOR SIGNAL SIMULATOR





21655

Figure IA-3 MONOSTABLE MULTIVIBRATOR

I.A.4 FIVE POSITION RING COUNTER (Figure IA-4)

The ring counter incorporates five trigistors and associated circuitry. The purpose of this circuit is to sequentially deliver -20 volt square wave pulses of two milliseconds duration to the gates of the MOS FET commutator transistors. This is accomplished by having one trigistor stage turned "on" while the remaining four stages are held "off". Every time a pulse (14 volts, 500 microsecond duration) is fed from the monostable multivibrator the leading edge of the pulse turns off the trigistor stage that is "on". Approximately 25 microseconds later the stage following it is turned on.

In order to insure that only one stage is "on", switch 1 is held closed for several seconds at the start of the test. This connects the base of Q_{1A} to zero volts thru R_{10} and heavily biases this stage "on". If any other stage was "on" it will transfer a pulse to the following stage and so on down the line until the pulse returns to Q_{1A}. As long as the switch is closed, Q_{1A} conducts and no pulse will pass on to the following stage. When Switch 1 is opened the ring counter is ready for operation.

The trigistors turn on when a positive current pulse is applied to their base terminal. Their internal structure is equivalent to a pair of transistors, one a pnp and the other an npn, with the collector of each transistor feeding the base of the other. With positive base current the internal current increases rapidly, and current thru the device is limited solely by the external circuitry (R_6, R_7), This internal action is self-sustaining and the trigistor will remain in the "on" mode until a sufficient quantity of the external load current is drawn from the external base terminal to stop conduction through the input base emitter junction. As this current is withdrawn, the device turns "off" until a positive base current again appears.

When switch 1 is opened, Q_{1A} is left in a conducting state. The positive going pulse from the monostable multivibrator is coupled thru differentiation network C_1, R_1 to the base of trigger drive transistor Q_2, turning it on. This allows current from the base of Q_{1A} to flow to the -20 volt supply thru forward biased diode D_{1A}, capacitor C_2

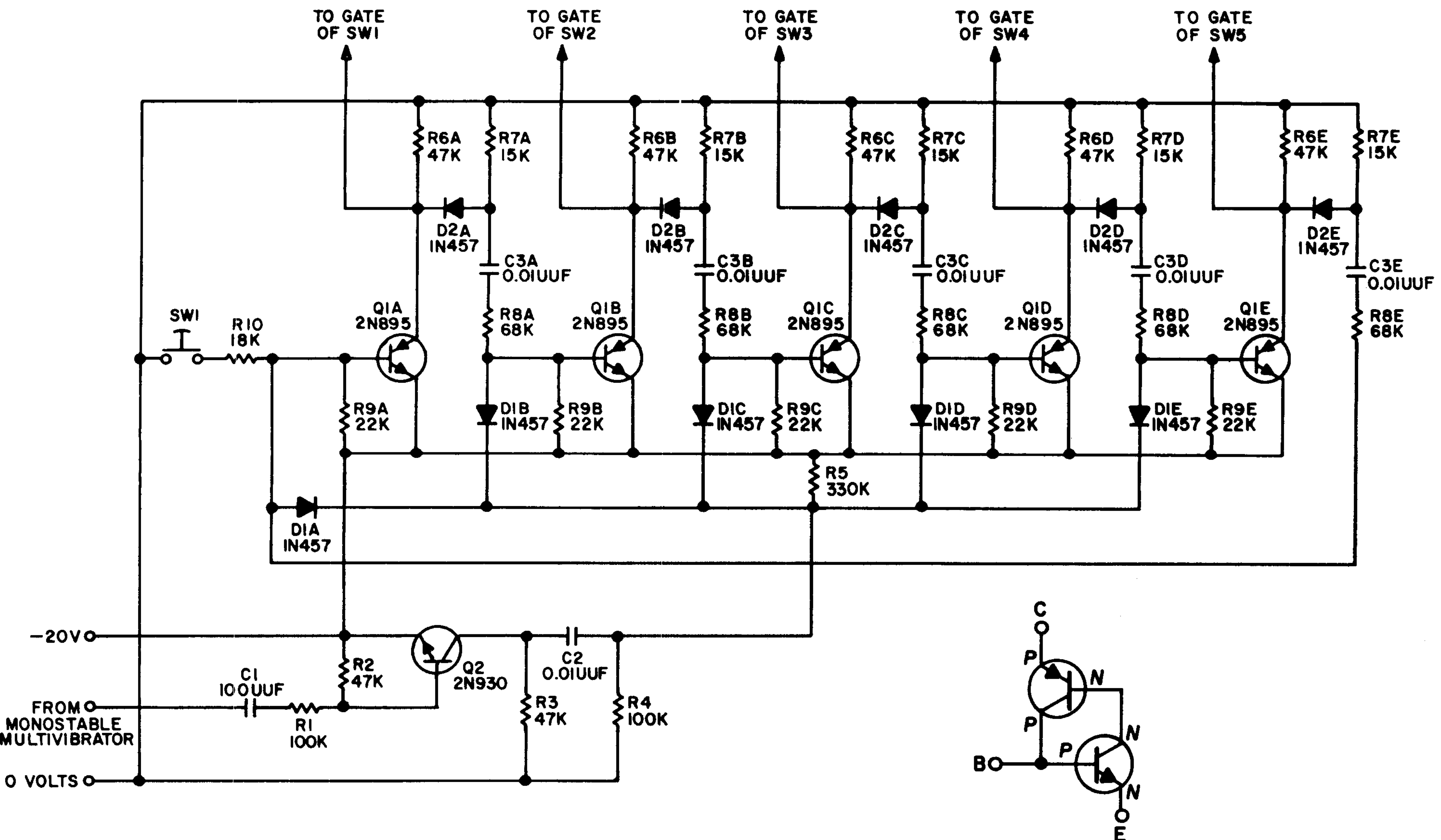


Figure IA-4 5 POSITION RING COUNTER

and transistor Q2. This turns Q_{1A} "off" (as described above). No other stage can turn "on" during this time as the negative trigger pulse at the junction of C_2, R_4 is coupled through diodes D_{1A}, D_{1B}, D_{1C}, D_{1D}, D_{1E}, holding all the trigistors bases negative. The impedance seen by C2 is such that hold-off is maintained for approximately 25 microseconds. While Q_{1A} was conducting its collector voltage was -20 volts. When the device was turned off, its collector voltage rose to zero volts. Capacitor C_{3A} having been charged to -20 volts begins to discharge thru R_{7A}, R_{8A} and the base of Q_{1B}. This pulse is positive going (toward zero volts), and by the action described earlier, turns on Q_{1B} after the 25 microsecond hold-off period terminates. The collector voltage of Q_{1B} then drops to -20 volts and retains this level for two milliseconds. Then a "turn-off" pulse arrives at D_{1B} and by the same process the -20 volt pulse is transferred to Q_{1C}.

As long as pulses are received from the monostable multivibrator the ring counter action will occur. The output of the fifth stage is RC coupled to the first stage, thereby completing the loop.

The 25 microsecond hold-off time interval (set primarily by C_2) was found to be critical and was largely dependent on the inherent characteristics of individual trigistors. Although a trigistor ring counter is relatively simpler than any other ring counter configuration this precludes its use for highly critical space applications.

I.A.5 FIVE POSITION MOS FET COMMUTATOR (Figure IA-2)

Each of the five trigistor stage collector outputs drives a corresponding gate of the commutator. When a gate is at zero volts, the drain to source impedance of this transistor is greater than 10^8 ohms. Consequently, the simulated detector output voltage present at the drain of the transistor (See I.A.1), is isolated from the source. When -20 volts is applied to the gate of a transistor, the drain to source impedance is sharply reduced (to less than 300 ohms with a 2N 3608). This allows any voltage

on the drain to be coupled to the source thru a low impedance. The previously described ring counter sequentially applies -20 volts to the gates of the MOS FET transistor switches, thus producing commutation of the d-c signal voltages present at their drains by virtue of the detector simulation voltage dividers.

The sources of the five commutator switches are tied together and the common output is coupled to the wide band preamplifier. A complete description of this commutator assembly is covered in section I.B of the appendix.

I.A.6 WIDE BAND PREAMPLIFIER (Figure IA-5)

The common output of the commutator is fed to the base of the input stage Q_1 of differential amplifier Q_1, Q_2. The output of this stage is coupled to gain stage Q_4 thru emitter follower Q_3. Overall circuit gain is determined by the ratio of R_6 to R_5 (gain $\approx$ 470). A wide band preamplifier is used so that the narrow switching spikes present at the commutator output can be faithfully amplified without introducing undesirable "stretch-out" of the switching pulses. The lower frequency -3 db point is $\approx$ 3 cps and the amplifier is flat to above 200 KC.

For 2N 3610 tests both the MOS FET transistors and the wide band preamplifier were placed in the environmental temperature chamber. This tended to produce noise at low test temperatures. When testing the 2N3608 transistors, the preamplifier was kept outside the chamber which avoided this spurious noise problem. The test results on the 2N3610 transistors are included in Appendix II of this report.

I.A.7 POST-AMPLIFIER (Figure IA-6)

In addition to triggering the ring counter, the monostable multivibrator also drives a series switch at the output of the amplifier. The switching pedestal produced by this switch was 1.5 millivolts ($\approx 3\mu$ volts referred to the systems input). An additional amplifier

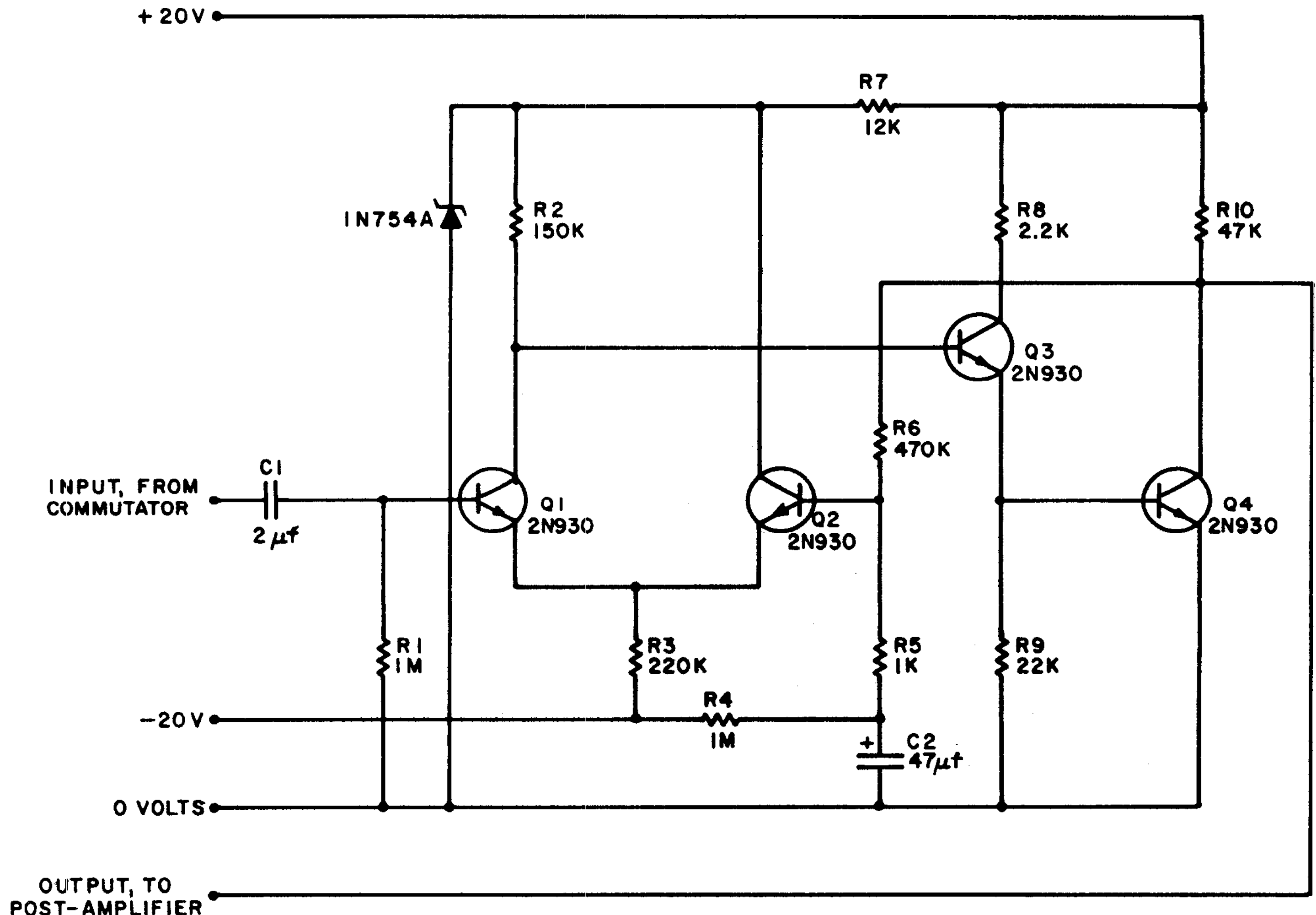
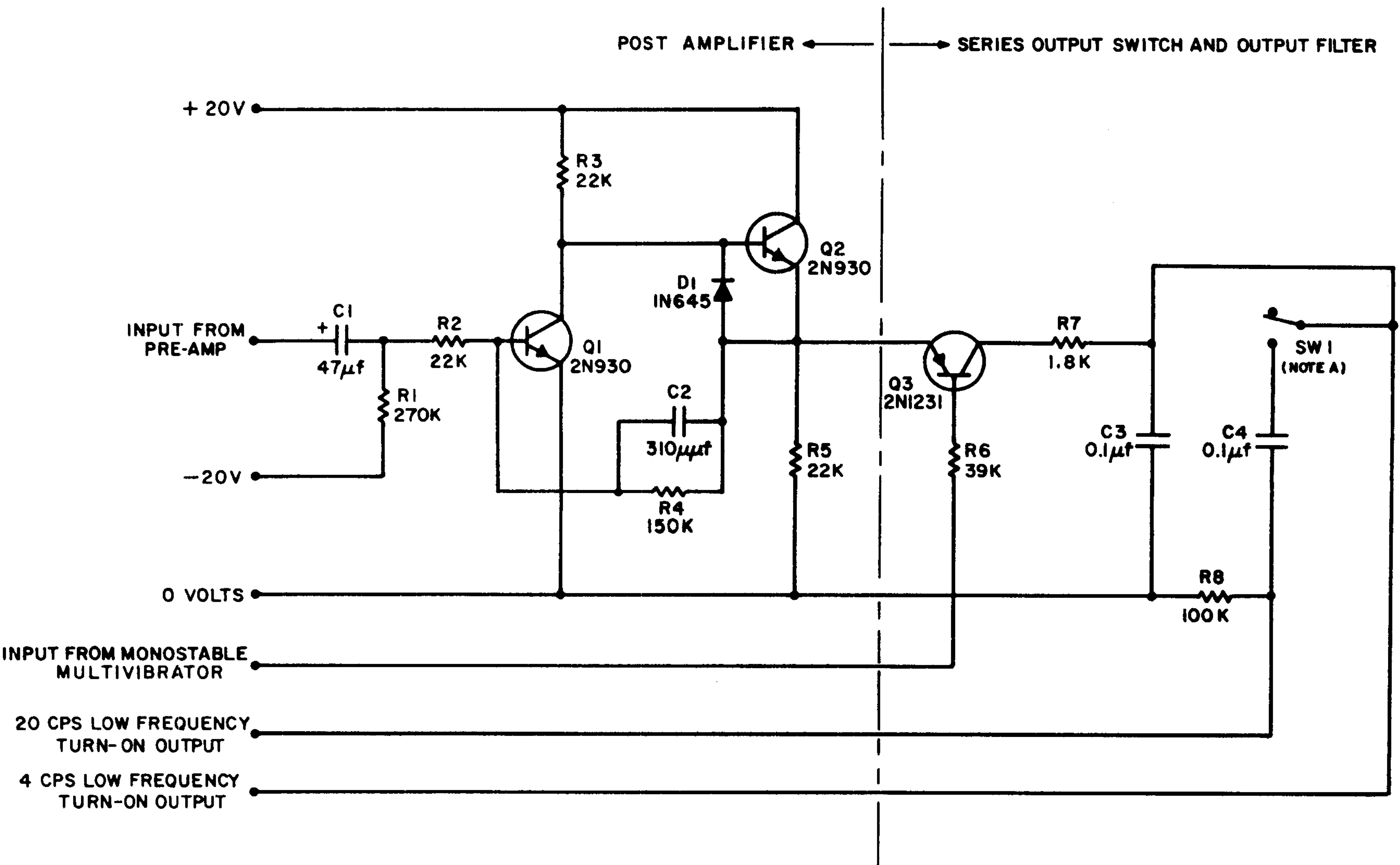


Figure IA-5 WIDE BAND PREAMPLIFIER



NOTE "A": SWITCH THE SERIES R-C NETWORK INTO CIRCUIT TO ELIMINATE LOW FREQ. NOISE WHEN OPERATING PREAMPLIFIER AT TEMPERATURES BELOW 0°C

Figure IA-6 POST AMPLIFIER, SERIES OUTPUT SWITCH, AND OUTPUT FILTER

(the post-amplifier) was added after the preamplifier to bring the overall gain of the system to 2840. This lowered the effective switching spike pedestal present at the series switch to ≲ 0.6 microvolts refered to the systems input, which is less than the system's input noise level.

Stage Q_1 is a gain stage and Q_2 is an emitter follower buffer stage. The overall gain of the post-amplifier is approximately determined by the ratio of R_4 to R_2. (150K ÷ 22K). The actual measured gain was 6.55. Capacitor C_2 and resistor R_4 determine the amplifier's high frequency cutoff of 3KC; capacitor C_1 and resistor R_2 the low frequency cutoff of 1/6 cps.

I.A.8 SERIES OUTPUT SWITCH AND OUTPUT FILTER (Figure IA-6)

As stated in I.A.7, the monostable multivibrator also drives the series output switch. The multivibrator opens this switch during the time the short duration commutation pulse is present at the output of the post amplifier, thus preventing the spike from appearing in subsequent processing circuitry. The output of the series switch is coupled to a 800 cps low pass filter composed of R_7 and C_3.

When testing the type 2N 3610 MOS FET switches at low temperatures (0°C to -50°C) with the preamplifier in the environmental chamber, the preamplifier's low frequency noise increased. This was minimized by reducing the system's low frequency response. Switch SW 1 adds a 20 cps high pass filter consisting of C4 and R8 after the 800 cps low pass output filter circuit. The final output is then taken across R8, instead of across C_3.

I.A.9 OVERALL SYSTEM GAIN VS. FREQUENCY RESPONSE CHARACTERISTICS

Figure IA-7 shows the measured gain vs. frequency response of the system's signal amplifiers (preamp and post-amplifier), 800 cps high frequency cutoff final output filter, and the low frequency response characteristics with and without the low frequency noise attenuator filter. This filter, as covered in Appendix II which follows, modified the low frequency turn-on of the breadboard setup to closely simulate the low frequency response characteristics of the L.P.H.S. system. It was only used during low temperature tests of the type 2N3610 MOS FET commutator transistors to reduce spurious low frequency preamplifier noise, and was not used during any other tests.

The overall system gain, frequency response, and dynamic signal range that could be accommodated by the signal amplifiers was more than adequate to bring the microvolt signal levels from the commutator output up to processable millivolt levels, without producing excessive spurious commutator gating pulse stretchout, or amplifier saturation.

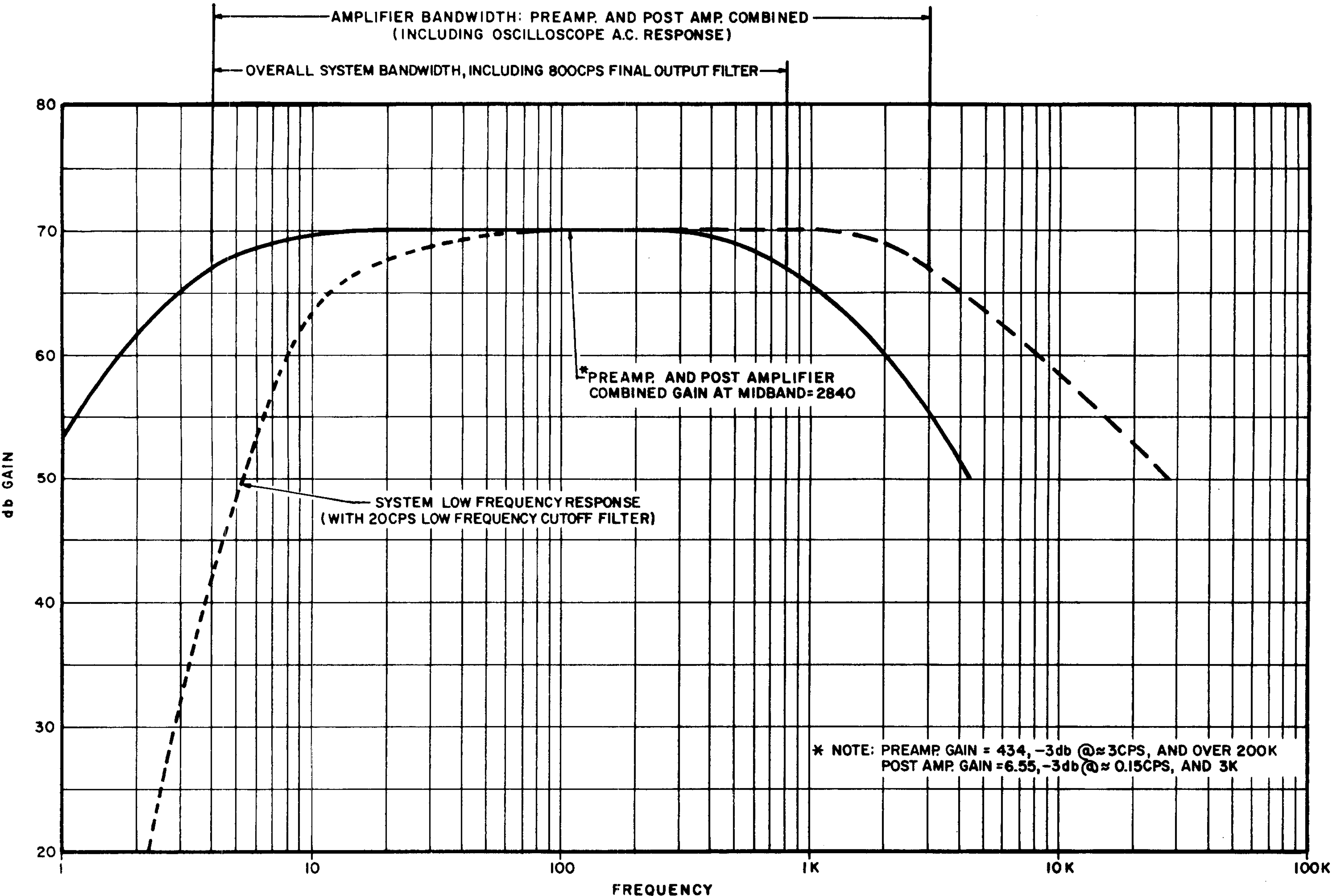


Figure IA-7 SIGNAL CHANNEL GAIN VS. FREQUENCY

I.B COMMUTATOR ASSEMBLY DESCRIPTION

I.B.1 ELECTRICAL CONFIGURATION

The commutator consisted of five MOS FET transistors mounted on an aluminum heat sink (see Figure IB-1). The transistor's leads were heat sunk via surrounding insulated printed circuit pads to the underlying aluminum. Additional heat sink pads provided termination points for 1000:1 input signal attenuator resistors associated with each transistor. Similar pads also terminated the high thermal impedance constantan lead wires that interconnected the transistors and external connecting cables.

100K resistors were placed in series with the gates of each transistor to guard against damaging the gate drive circuitry if a transistor inadvertantly shorted. Subsequently, it was realized that a short through the metal oxide gate insulating layer can sometimes be repaired by applying gating drive through a low series impedance. Therefore, in any future commutator, this series resistor should either be of a lower value, or eliminated.

A .0047 mfd capacitor and 22K resistor were connected in parallel and mounted across the common output and ground heat sink pads associated with transistor number 3. The capacitor served to attenuate the amplitude of the capacitively coupled commutator transistion spikes. The resistor was inserted to permit evaluation of the series resistances of individual commutator transistors when they were gated "on".

Figure IB-2 shows the typical layout of a transistor and its associated printed circuit pads. Figure IB-3 is an electrical schematic of the overall commutator isothermal test fixture.

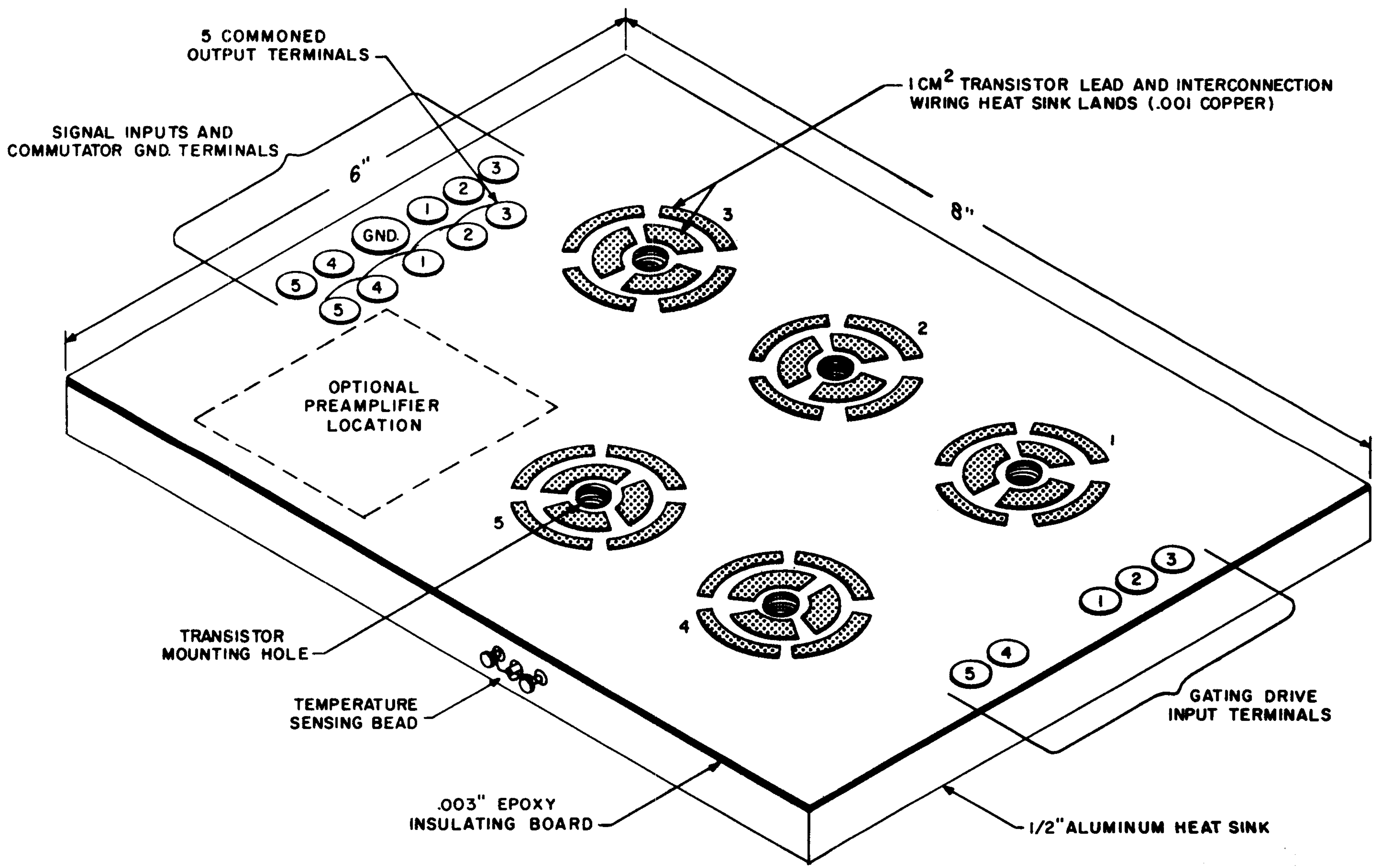
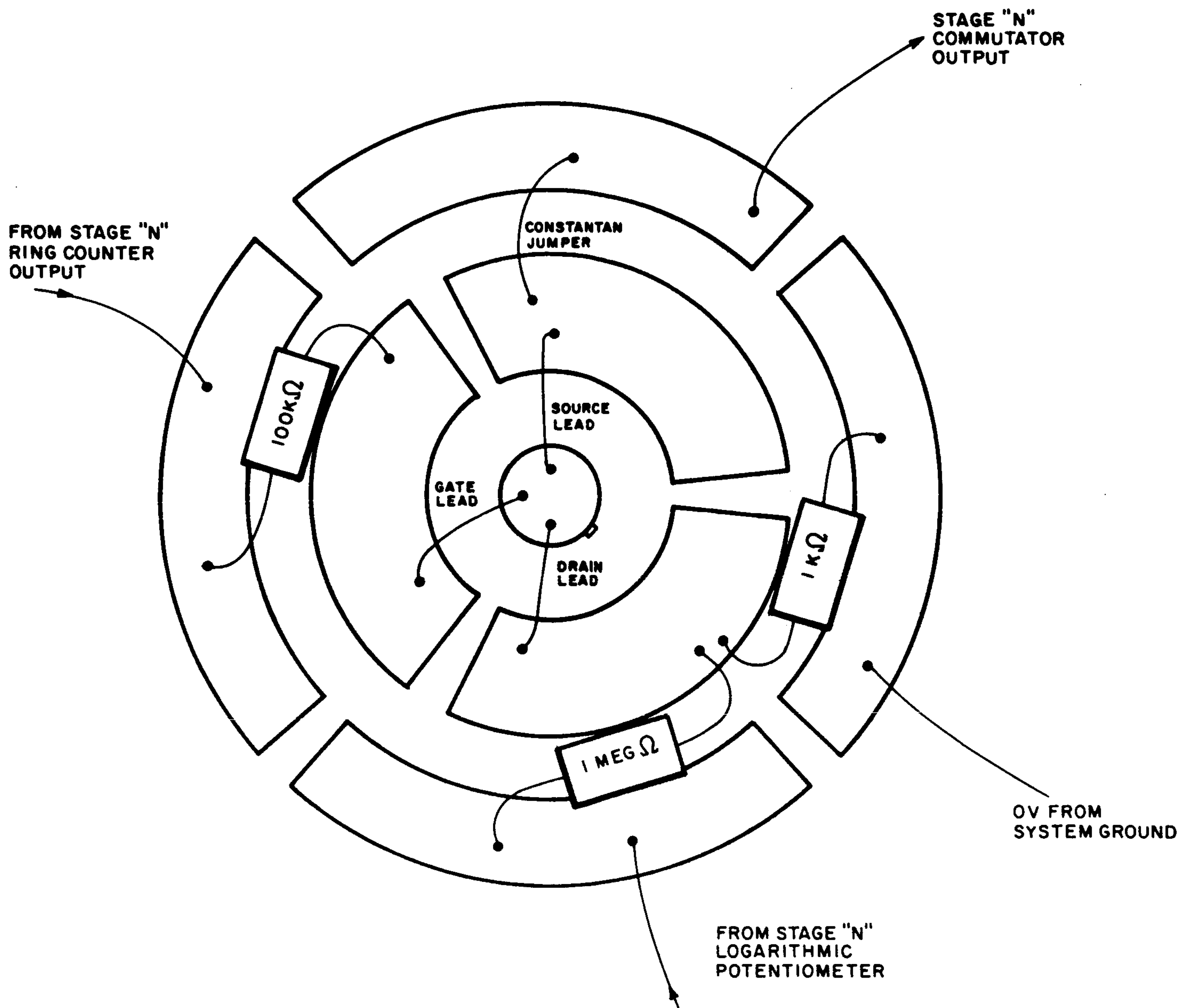


Figure IB-1 ISOTHERMAL COMMUTATOR TEST FIXTURE (WITHOUT INTERCONNECTIONS & EXTERNAL LEADS)



NOTE: 1. LEADS FROM TRANSISTOR: 1 CM LONG, 0.018" DIAMETER (KOVAR)
2. INTERCONNECTING WIRES: ≥ 1 CM LONG, 0.020" DIAMETER (CONSTANTAN)
3. ALL RESISTORS 1/4 W CARBON COMPOSITION

21660

Figure IB-2 TYPICAL LAYOUT OF A TRANSISTOR TO ITS ASSOCIATED PRINTED CIRCUIT PADS (= 3 TIMES ACTUAL SIZE)

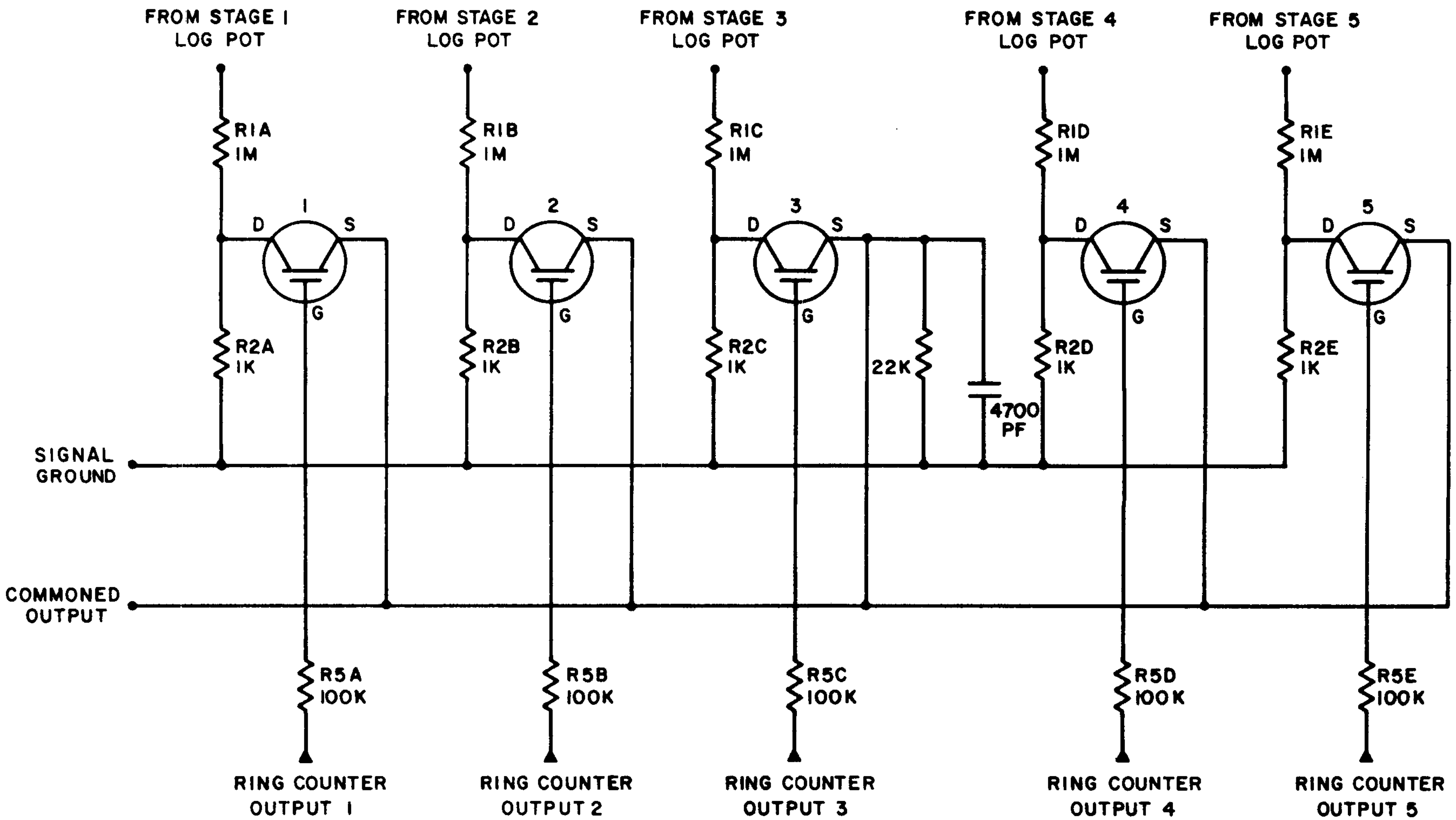


Figure IB-3 ELECTRICAL SCHEMATIC OF ISOTHERMAL TEST FIXTURE

Commutation of the 1000:1 attenuated inputs was achieved by sequentially gating on the five heat sunk transistors. The signal inputs to be commutated were applied to the transistor's drain terminals. The commutated output signals appeared on the transistors source terminations, which were commoned.

The commutator test jig was used to test both GME type 2N3608 and 2N3610 (1004 and 1009) transistors. Except for the following, the commutator interconnections were the same for all tests. The silicon substrate of the type 2N3608 transistor is connected to the transistor case internally. This was grounded to the aluminum heat sink block. The type 2N3610 transistor, however, had its body termination internally connected to the transistor's source. Although grounding the body has theoretical advantageous, both transistors performed adequately well in all tests.

I.B.1.a ELIMINATION OF COMMUTATOR SWITCHING TRANSIENTS

Switching transients result because of the gate to source and gate to drain capacities of the commutator FET transistors. The transients occur whenever an MOS FET is switched "on" or "off" by the relatively high voltage level gating drive.

The test circuit (for one commutator position) is as follows:

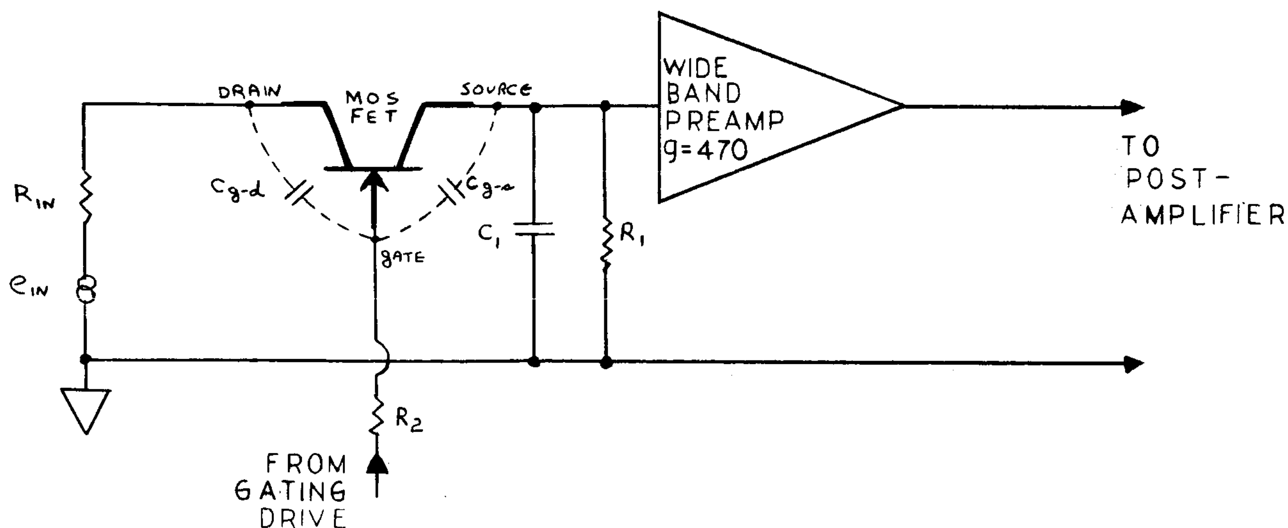


Figure IB-4 TEST CIRCUIT FOR ONE COMMUTATOR POSITION

<u>where:</u>

e_{in} = simulated detector output

R_{in} = simulated detector resistance = 1K

R_1 = commutator output resistor = 22K

R_2 = gate resistor = 100K

C_1 = commutator output capacitor = 4700 pf

C_{g-d} = gate to drain capacity

C_{g-s} = gate to source capacity

From the data sheet, General Micro-electronics type 2N3610 FET transistors have the following gated "on" capacitive characteristics at 25°C.

	MAXIMUM	MINIMUM
C_{g-d}	0.6 pf	0.4 pf
C_{g-s}	0.9 pf	0.7 pf

Figure IB-5 CAPACITIVE CHARACTERISTICS OF 2N3610 AT 25°C

When an FET is gated "on" R_{d-s} rapidly decreases to a small value and the two gate capacities can be considered in parallel. A worst case theoretical equivalent circuit can then be drawn:

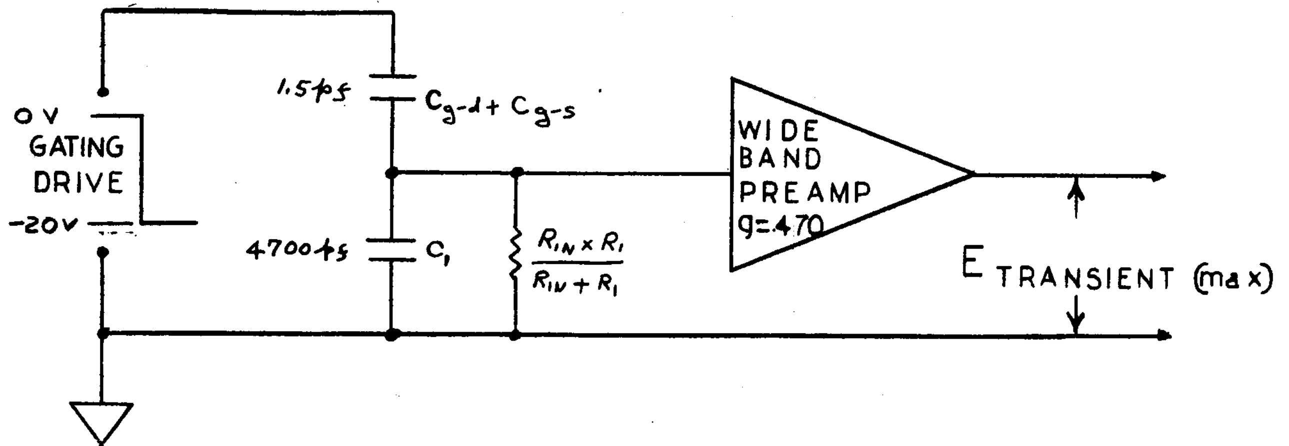


Figure IB-6 WORST CASE EQUIVALENT CIRCUIT (Electrical)

$$E \text{ transient (maximum)} = E \text{ gating drive} \left(\frac{C_{g-s} + C_{g-d}}{C_1 + C_{g-s} + C_{g-d}} \right) \left(\text{gain } 470 \right)$$

$$\simeq 20 \left(\frac{1.5 \text{ pf}}{4700 \text{ pf}} \right) \left(470 \right)$$

$$= 3.0 \text{ volts}$$

The theoretical minimum transient can be determined by considering what happens when an FET is gated "off". R_{d-s} rises rapidly tending to isolate C_{g-d} from the output of the commutator. Also, due to the time constant of a coupling network in the drive circuit, the gating drive decreases from -20 volts to only -6 volts (effectively a + 14 volt rise) before the next FET drive stage is actuated. Assuming minimum C_{g-s} only, a least spike amplitude equivalent circuit can be drawn:

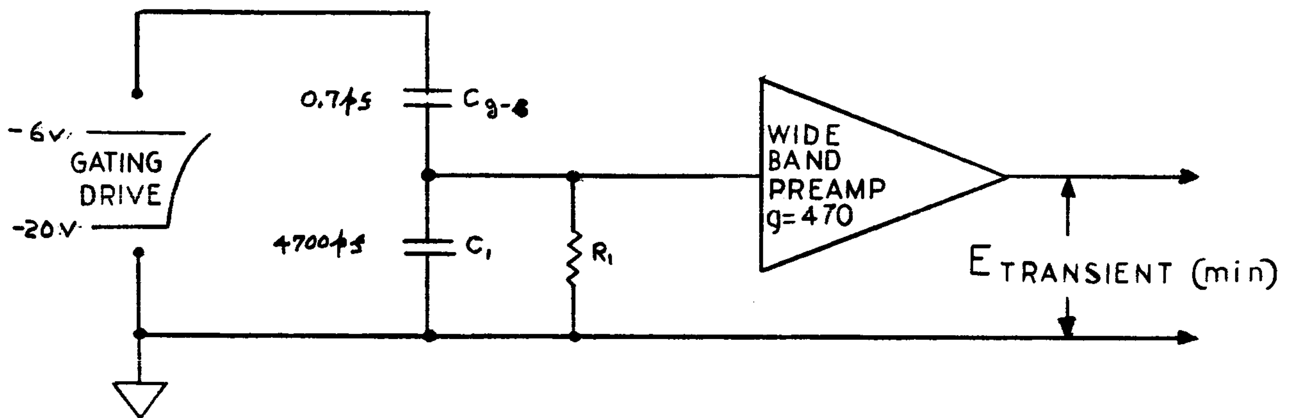


Figure IB-7 MINIMUM TRANSIENT EQUIVALENT CIRCUIT

$$E \text{ transient (minimum)} = E \text{ gating drive} \left(\frac{C_{g-s}}{C_1 + C_{g-s}} \right) \left(\text{gain } 470 \right)$$

$$\approx 14 \left(\frac{0.7 \text{ pf}}{4700 \text{ pf}} \right) \left(470 \right)$$

$$= 0.98 \text{ volts}$$

Therefore, it can be expected that the transient spike amplitude produced during commutation will be approximately between 1 and 3 volts at the output of the wide band preamplifier.

As seen in Figure IB-8, photo A, the amplitude of the switching spike was within the theoretical limits. Similarly, the type 2N3608 MOS FET also produced resultant spikes that were close to theoretical expectations. (See figure IB-8, photo B).

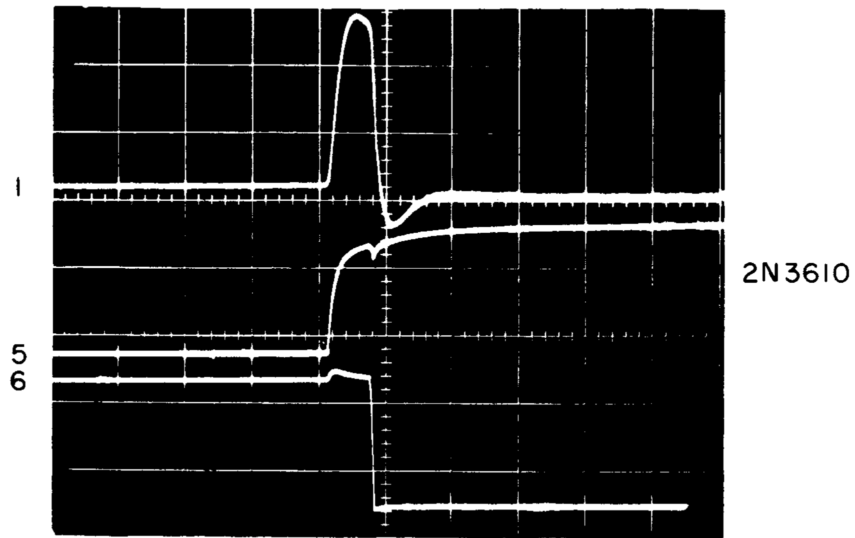
If the preamplifier can accommodate large signal amplitudes without saturation occurring, no spurious stored charges can develop on any capacitors therein. The amplifier used in the experiment could handle signal levels greater than twice the maximum transient pulse calculated, preventing this problem from occurring.

A transistor switch in series with the output was gated "open" simultaneously with the switching of MOS FET's at the input to the preamplifier. In this way the transient spikes were prevented from being passed to the system output. The drive for the output switch, however, impressed 1.5 millivolts spurious pulses on the signal. Referred to the input of the preamplifier this would be $\approx 3\mu v$ if this series switch were at the 470 gain preamp output. In order to decrease this effective level, a post amplifier of gain six was added between the preamplifier and the output switch. The 1.5 millivolt pulses present at the output switch due to gating of that switch was thereby decreased to about 0.6 μ volts referred to the input. This was well within system noise, and therefore, could be neglected.

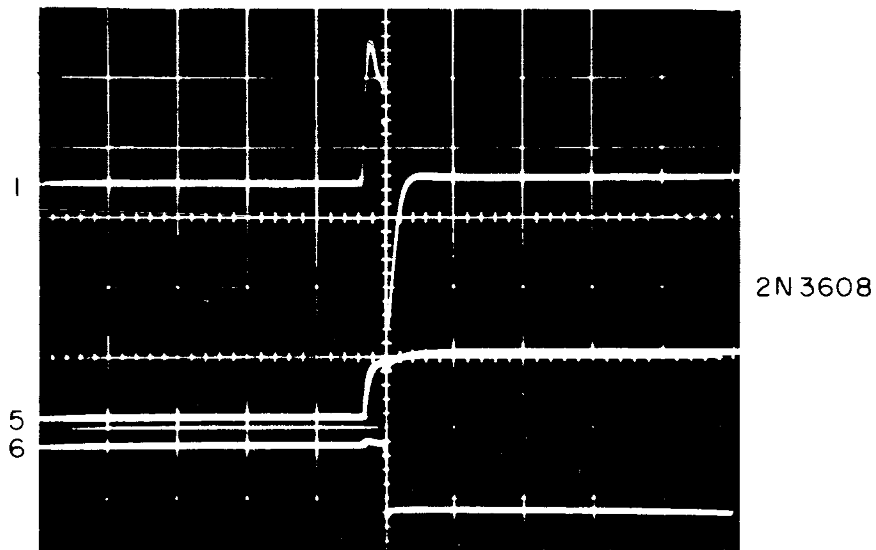
Input time constant is approximately determined by R_1 and C_1. With C_1 of 4700 pf and R_1 of 1K ohms, minimum $\tau = 4.7\mu$ sec.

This would produce no significant restriction of the speed of response to generator signals when a commutator sample time of 2 milliseconds is used.

However, the 4 millivolt transistion spikes require more than 10τ to decay to less than 1μ volt. The blanking time must therefore be at least 50μ seconds long in order not to "see" the gating drive transient on the signal trace.



A



B

	WAVESHAPE	VERTICAL DEFLECTION	REFERRED TO INPUT	TIME BASE
A	1	0.5V/DIV	1.2 MV/DIV	50 μ SEC/DIV
	5	10V/DIV	————	50μ SEC/DIV
	6	10V/DIV	————	50μ SEC/DIV
B	1	1.0V/DIV	2.4 MV/DIV	100μ SEC/DIV
	5	20V/DIV	————	100μ SEC/DIV
	6	20V/DIV	————	100μ SEC/DIV

21662

Figure IB-8 WAVESHAPES AT POINTS INDICATED IN SYSTEM BLOCK DIAGRAM (Fig. 1A-1)

For the experiment the blanking time was set at 500μ sec, or 25% of the sample period. This long blanking time was required due to the slow transition from "on" to "off" of the gating drive (approximately 150 μ seconds: See Figure IB-8). With fast transition, it is felt that the 50μ second theoretical limit can be achieved.

I.B.2 THERMAL DESIGN CONSIDERATIONS

The thermoelectric power of a silicon - aluminum junction, such as is used at the internal source and drain terminations in an MOS FET transistor, is approximately - 400 μv/°C. If the transistor's source and drain internal connections are kept physically close, the temperature difference between the two junctions will be small and the net voltage generated due to thermal effects will be minimal.

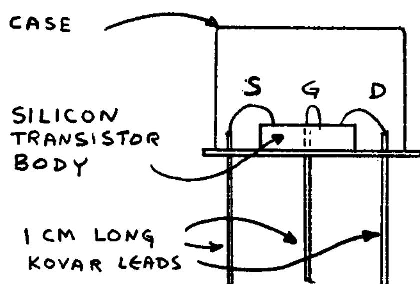
For the test, standard General Micro-electronics transistors, types 2N3608 and 2N3610 were used as the low level commutator switch elements. These were not primarily intended for use as microvolt level switches, and hence, thermal considerations were not incorporated in their design. To overcome this potential deficiency, an isothermal jig was fabricated, and the FET transistors were mounted thereon. The isothermal test jig's main function was to minimize any temperature differences between the transistors and their external leads. In effect, it was felt that this approach would reduce spurious temperature gradients within the transistors, compared to no precautions being taken.

For the experiment, it was desired to limit spurious thermal EMFs to one microvolt or less. Just considering the transistor chip's source and drain terminations, the greatest temperature difference that could be tolerated was

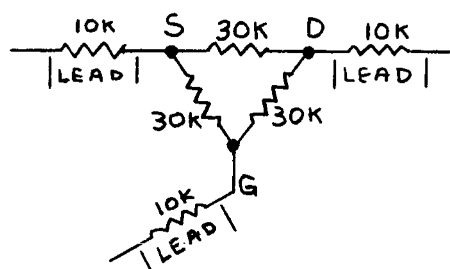
$$T = \frac{1 \mu v}{400 \ \mu v/^\circ C} = \frac{1}{400} \ ^\circ C$$

I.B.2.a THERMAL TEST JIG CALCULATIONS

The thermal impedance thru opposite faces of a cube of copper 1cm. on each side is analogously defined as one "ohm". Conservatively approximating thermal scale factors for the materials in the FET devices used, the following "worst case" model was evolved for the transistor (Figure IB-9).



PHYSICAL REPRESENTATION



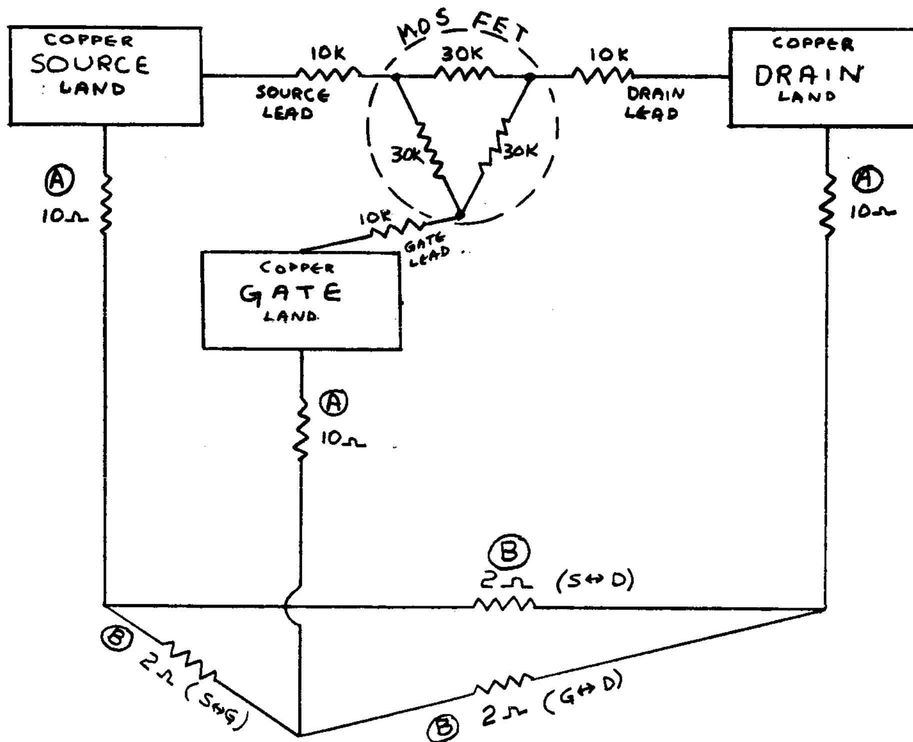
THERMAL ANALOGUE

Figure IB-9 - MOS FET TRANSISTOR AND ITS ASSOCIATED THERMAL ANALOG

The isothermal commutator test fixture shown in figure IB-1 consisted of a one-half inch thick aluminum block. Adhered to the block by Dow Corning 269 adhesive was an epoxy board, 0.003 inches thick with 0.001 inch thick copper film laminated to both sides. Clearance holes were drilled through the laminate and aluminum block, into which five FET's were inserted. The copper laminate surface was etched to form a pattern of one square centimeter lands surrounding each transistor.

Using the criterion stated above, a thermal impedance of approximately 10 ohms existed between each land and the underlying aluminum heat sink.

The following analogous thermal model shows an FET transistor connected to the isothermal test jig block (Fig. IB-10).



Note: (A) Thermal impedance thru 0.003" epoxy between heat sink pads and underlying aluminum block.

(B) Thermal impedance thru 1/2" aluminum block (assuming thermal impedance of aluminum is 2 times copper, and approximately 1 cm^3 of aluminum between areas under pads).

FIGURE IB-10 - THERMAL ANALOG: TRANSISTOR IN FIXTURE

Only considering the source and drain terminal pads, the following analogous equivalent model can be generated (Figure IB-11).

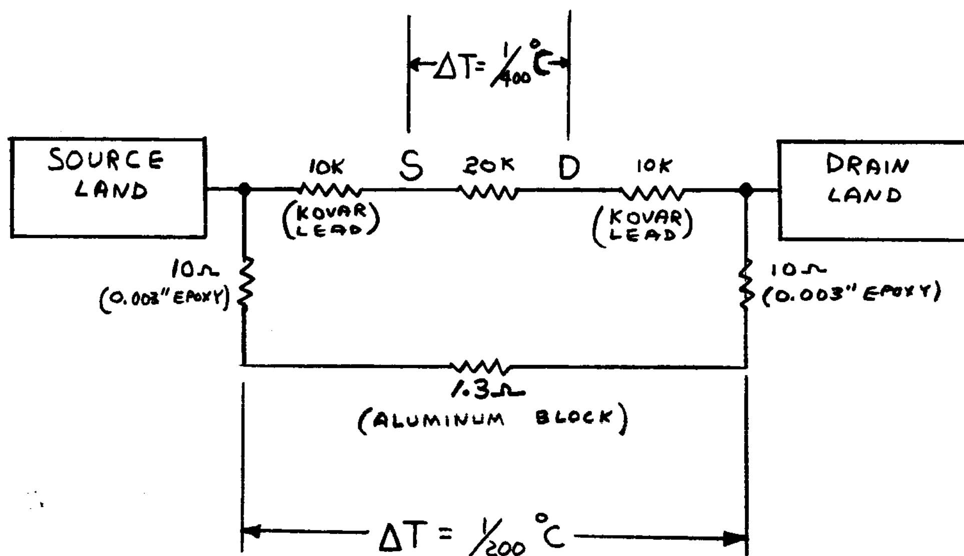


FIGURE IB-11 - TRANSISTOR SOURCE AND DRAIN: THERMAL ANALOG

The above depicts that a 1/200°C temperature difference under the source and drain terminal pads in the 1/2" aluminum block may produce 1/400°C temperature difference between source and drain terminations within the FET transistors, when mounted on the isothermal test fixture. In addition, caloric flow from external thermal sources along the external source and drain wiring is shunted through the low thermal impedance series path provided by the .003" epoxy board and the underlying aluminum block, rather than flowing through the transistor body.

Because of symmetry, the conditions depicted by the foregoing model would be similar if the gate and source or gate and drain lands were shown, instead of the source and drain lands. However, as the gate is electrically isolated from the source and drain, temperature differences at the transistor's internal gate termination point do not produce spurious signals at the commutator output. Therefore, the worst thermal case within the transistor will be due to caloric flow between the transistor's internal source and drain termination points.

Figure IB-12 is a thermal analogue of the test setup, showing this "worst case" condition. It indicates temperature distributions with a "static" thermal differential of 70°C across the external source and drain interconnecting leads. With the assumed worst case conditions shown, 1 microvolt of spurious commutator output could be produced.

Under "worst case" static temperature test conditions, much less than 70°C temperature differential would exist between the commutator's interconnecting lead wires. Therefore, with the thermal design utilized, thermal conduction through the external interconnecting lead wires can be neglected.

I.B.2.b THERMAL PERFORMANCE

It should be noted, however, that even small temperature differences along the 1/2" aluminum heat sink could produce significant outputs. With the previously assumed "worst case" assumptions, one microvolt of spurious commutator output could be produced if a .005°C temperature difference occured between the transistor's one cm. apart source and drain termination heat sink pads. Measurements were made of the thermal EMF's produced when a temperature difference was deliberately applied between 1 cm. long source and drain leads. These measurements (made subsequent to testing the overall commutator performance) showed that the type 2N3608 transistor developed six microvolts per degree centigrade. The type 2N3610 transistor produced

70°C

0.084°C

0.005°C

0.0025°C

10K
1 CM CONNECTING LEAD (CONSTANTAN)

INTERCONNECTING LEAD LAND

NOTE 1
10K
1 CM INTERCONNECTING LEAD (CONSTANTAN)

TRANSISTOR LEAD LAND

SOURCE LEAD (KOVAR)
10K

S
20K
D
SILICON DIE
TRANSISTOR BODY

DRAIN LEAD (KOVAR)
10K

TRANSISTOR LEAD LAND

NOTE 1
10K
INTERCONNECTING 1/4 WATT RESISTOR

INTERCONNECTING LEAD LAND

10K
1 CM CONNECTING LEAD (CONSTANTAN)

10 Ω 0.003 INCH EPOXY BOARD

10 Ω 0.003 INCH EPOXY BOARD

10 Ω 0.003 INCH EPOXY BOARD

10 Ω 0.003 INCH EPOXY BOARD

1.3 Ω
ALUMINUM BLOCK

1.3 Ω
ALUMINUM BLOCK

1.3 Ω
ALUMINUM BLOCK

0.005 °C
(ACROSS 1 CM LENGTH OF ALUMINUM)

0.014°C
(≈3 CM LENGTH OF 1/2 INCH ALUMINUM BLOCK)

NOTES: 1. TRIVIAL CALORIC FLOW THRU THESE PATHS.
2. ARROWS INDICATE SIGNIFICANT CALORIC FLOW PATHS.

21663

Figure IB-12 THERMAL ANALOG OF COMMUTATOR TEST FIXTURE (WORST CASE)

twelve microvolts per degree centigrade. Based on these tests, the performance of the commutator breadboard was not limited by the internal thermal EMF's generated within the FET transistors.

The major spurious thermal EMF's noted in the breadboard setup were produced by dissimilar metal connections to the copper leads of the 1K ohm composition resistors used to simulate the impedance of thermopile detectors. The 1K ohm resistors were connected between pairs of copper heat sink lands surrounding each transistor on the isothermal test jig. One land of each pair was also connected to the kovar drain lead of an associated FET "switch". The other land was connected to the constantan wire used as the ground bus on the commutator breadboard. Therefore, in series with each resistor were a pair of thermocouples, each of which produced approximately 35 microvolts per degree centigrade [measurements showed the following thermal EMFs (Constantan to copper; 38.5 μ volts/°C) (Kovar to copper; 33.5 μ volts/°C) (1K resistor, i.e. carbon composition to copper; 0.7 μ volts/°C)].

In addition to gradients produced in the aluminum due to changing temperatures (dynamic conditions), gradients in the surrounding air could also produce problems. This effect was noted during the temperature tests, for which a small, and therefore, less than ideal, environment chamber was used. It was noted that the orientation of the commutator assembly fixture (vertical vs horizontal) altered the "noise" waveshape over the commutator scan. This was most likely caused by stratified air inducing temperature gradients into the 1/2" aluminum block.

I.B.2.c <u>CONCLUSION</u>

By reducing the physical separation distances, and hence, the thermal impedance between each individual transistor's source and drain lead terminations, the foregoing commutator problems can be minimized. Maximum reduction of separation distance can best be achieved if the actual heat sinking of the transistor leads is done directly within

the transistor housing. Also, by placing the transistor's source and drain terminations in very close proximity on the silicon die that constitutes the transistor body, potential problems due to thermal EMFs from these terminations can be avoided.

From the foregoing, it is obvious that the best approach to eliminate MOS FET commutator thermal effect problems is by careful thermal design directly within the MOS-FET cases. This internal thermal design approach, rather than the external heat sink approach utilized for the test jig, will simultaneously optimize performance and yield a minimum overall size commutator package.

APPENDIX II

TABLE OF CONTENTS

SECTION		PAGE
II.A	INTRODUCTION	II-1
II.B	MOS FET GATE BREAKDOWN	II-3
II.C	TEMPERATURE TEST RESULTS	II-4
II.D	CONCLUSION	II-9

LIST OF ILLUSTRATIONS

APPENDIX II

NO.	TITLE	PAGE
II-1	Impedance Test of "Repaired" 2N3610 Transistors (25°C)	II-2
II-2	Impedance of Type 2N3610 Transistors After "Repair". FET #2 was not damaged	II-1
II-3	Commutator Performance at -50°C with 2N3610 Transistors	II-5
II-4	Commutator Performance at -0°C with 2N3610 Transistors	II-6
II-5	Commutator Performance at +25°C with 2N3610 Transistors	II-7
II-6	Commutator Performance at +90°C with 2N3610 Transistors	II-8

Appendix II

TEMPERATURE TESTS OF GME TYPE 2N3610 MOS FET TRANSISTORS

II.A INTRODUCTION

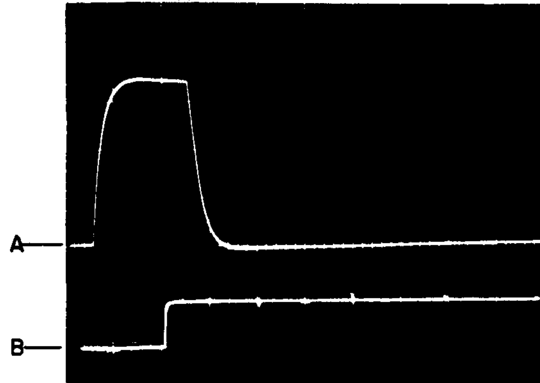
In addition to the tests conducted on type 2N3608 (type 1004) MOS FETs, five type 2N3610 (type 1009) transistors were also tested. The test results are included in this appendix for reference purposes, to indicate the non-critical nature of the commutator techniques utilized.

The photographs shown in Figure II-1 were taken at lab ambient conditions, and indicate the differences in impedance of the five type 2N3610 transistors that were tested. One millivolt input signal levels were utilizted, and a 22K load resistor was used at the commutator output to facilitate impedance measurements.

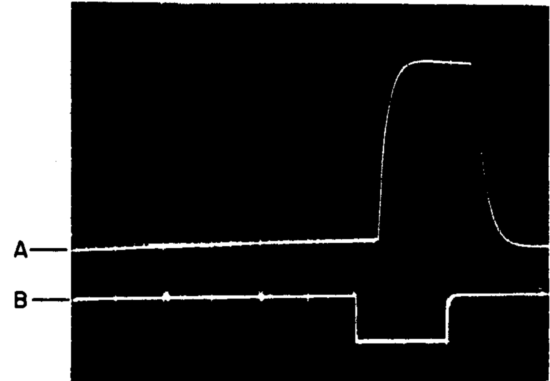
Due to inadvertant mishandling, electrostatic charges caused the gate insulation in four of the five test transistors to break down. These four transistors were subsequently repaired, but as indicated in the following table (II-2), their "on" impedances no longer were 2K ohms, as they were when originally received.

FET #	1	2	3	4	5
"on" Z	14K	2K	7K	10K	7K

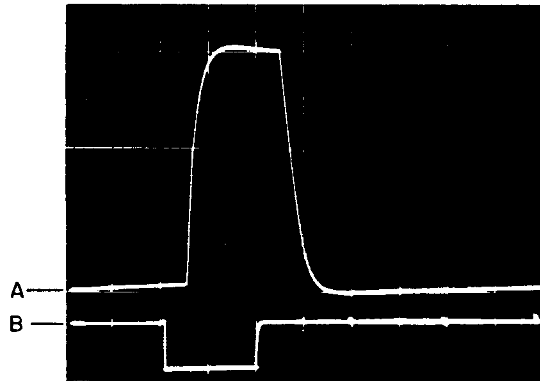
TABLE II-2 - IMPEDANCE OF TYPE 2N3610 TRANSISTORS AFTER REPAIR". (FET #2 WAS NOT DAMAGED)



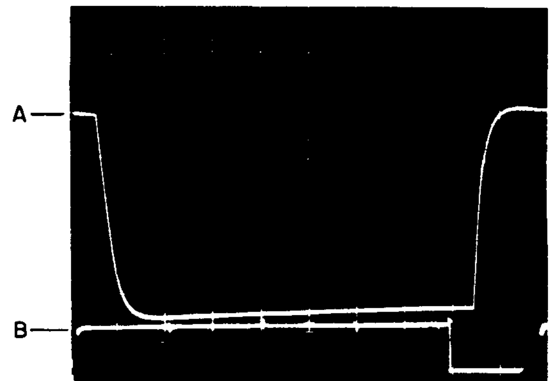
A) I MILLIVOLT INPUT TO CHANNEL I
B) GATING DRIVE TO CHANNEL I



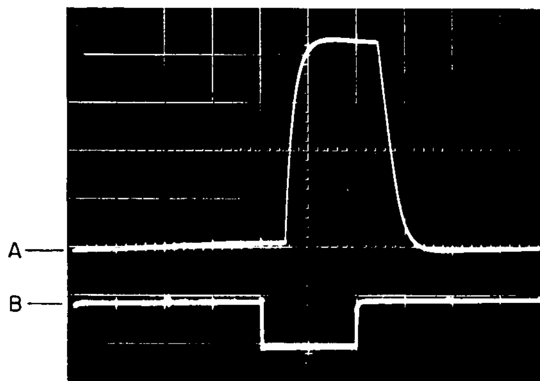
A) I MILLIVOLT INPUT TO CHANNEL 4
B) GATING DRIVE TO CHANNEL 4



A) I MILLIVOLT INPUT TO CHANNEL 2
B) GATING DRIVE TO CHANNEL 2



A) I MILLIVOLT INPUT TO CHANNEL 5
B) GATING DRIVE TO CHANNEL 5



A) I MILLIVOLT INPUT TO CHANNEL 3
B) GATING DRIVE TO CHANNEL 3

VERTICAL SENSITIVITY OF "A" CHANNEL:
0.5 VOLTS / DIVISION

VERTICAL SENSITIVITY OF "B" CHANNEL:
20 VOLTS / DIVISION

TIME BASE:
I MILLISECOND / DIVISION

21664

Figure II-I IMPEDANCE TEST OF "REPAIRED" 2N3610 TRANSISTORS (25°C)

Individual transistor "on" impedances varied widely and were considerably higher than obtained with the type 2N3608 transistors (whose test results are covered in the body of this report). The same commutator test setup was used to test these transistors as was used to test the type 2N3608 transistors.

II.B MOS FET GATE BREAKDOWN

Damage is caused when the maximum rated voltage between the transistor's gate and source or drain terminations is exceeded. Typically, they are rated between 20 and 50 volts. Excessive voltage causes the metal oxide dielectric insulating layer under the gate electrode to puncture, and an electrical short results. Static electricity charges can build up to over a hundred volts just by walking across a vinyl tile floor in rubber soled shoes. If a "charged" person touches an open gate lead after the other transistor leads are wired in circuit, this type of damage can result.

To avoid this occurrence, it was found necessary to return the circuit into which the FETs were wired to ground. In addition, the soldering irons and the people doing the wiring, also had to be grounded. When these precautions were taken, no further damage occurred.

The damaged transistors were "cured" by placing the rated transistor voltage, from a low impedance power supply, across the shorted gate and source or drain terminals. This caused heavy current to flow, and the heat produced at the puncture, due to the high current density at the restriction, evaporated the gate electrode material producing the short. This, in effect, restored the damaged transistors to operational condition. However, some of the gate and conducting channel area were no longer effective, as was evidenced by the higher "on" impedances of the repaired transistors.

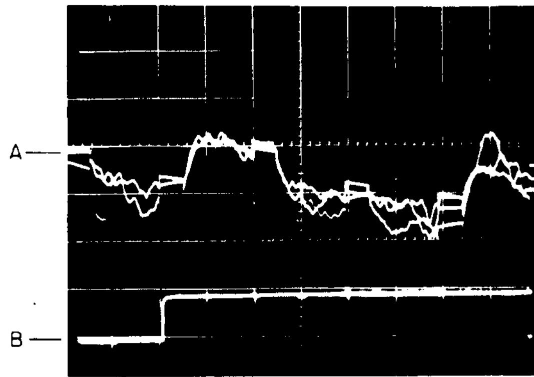
In applications where leakage from the gate drive to the device body is not significant, a zener type diode junction can be produced within the MOS FET device to act as a protect diode. This diode would limit the maximum static voltage charges that can build up on the gate electrode, and thereby prevent transistor damage. It is recommended that

this feature be incorporated in MOS FET devices to be used in the LPHS commutator.

II.C TEMPERATURE TEST RESULTS

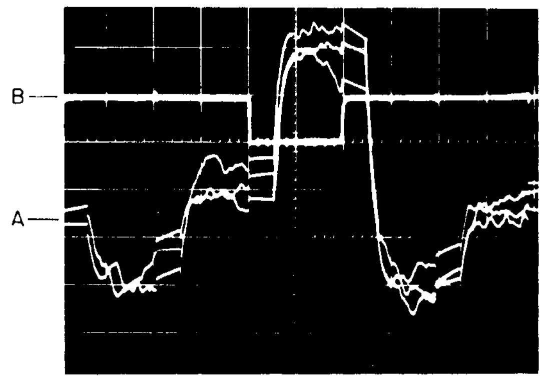
Figures II-3, II-4, II-5, and II-6 show the commutator performance using the repaired 2N3610 transistors at -50°, 0°, +25°, and at +90°C, respectively. Similar temperature tests (not shown) were also performed at -25° and +60°. The -25°C results were basically the same as those at -50°C, and the +60°C results were similar to the results at +25°C. For these tests, the preamplifier was placed in the environment chamber along with the commutator. At -50°C and -25°C, the amplifier's low frequency noise, referred to the input, was relatively high (approximately 5 microvolts) when the system low frequency turn on was 4 cps. To reduce this spurious noise, a 20 cps low frequency cut-off filter was added after the amplifier output for the low-temperature tests. With this filter, the spurious noise level was approximately 2 microvolts peak to peak. When these temperature tests were made with undamaged type 2N3608 MOS FETs, the preamplifier was maintained at lab ambient temperature, and the 20 cps filter was no longer required. The type 2N3608 test results are contained in the body of this report.

The low temperature preamplifier noise problem is strictly a function of the preamplifier's input transistors. Texas Instrument type 2N930 transistors were used. Subsequent to these tests, it was found that type 2N930 transistors made by El Menco have considerably less noise increase at low temperatures than those manufactured by Texas Instrument. Moreover, due to the nature of the threshold curcuit used in the LPHS system, the low frequency amplifier noise noted above would not have produced spurious outputs. The LPHS turn-on frequency for signals below threshold is approximately 20 cps. Therefore, the tests with the additional filter closely duplicated actual LPHS system comditions.



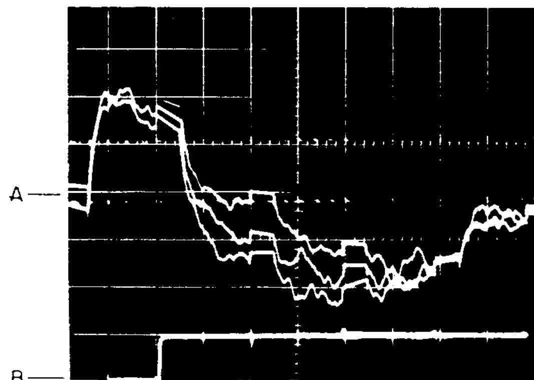
A

A) ZERO MICROVOLTS INPUT
B) GATING DRIVE TO CHANNEL I



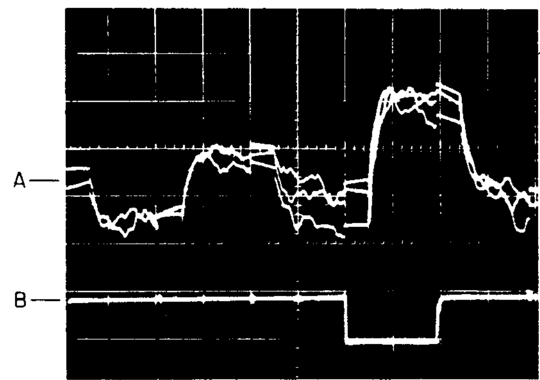
D

A) IO MICROVOLTS INPUT TO CHANNEL 3
B) GATING DRIVE TO CHANNEL 3



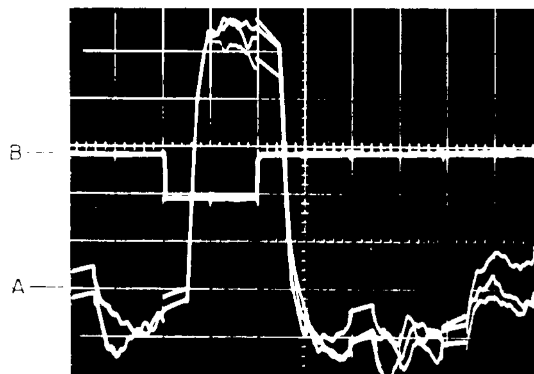
B

A) IO MICROVOLTS INPUT TO CHANNEL I
B) GATING DRIVE TO CHANNEL I



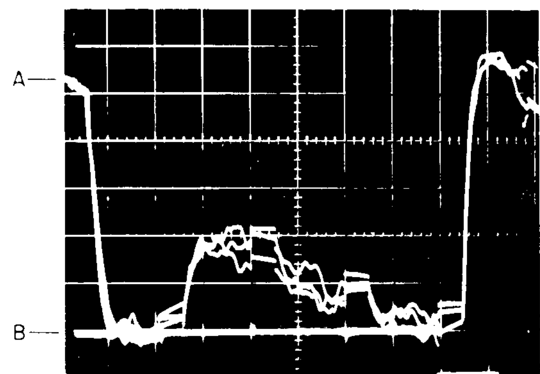
E

A) IO MICROVOLTS INPUT TO CHANNEL 4
B) GATING DRIVE TO CHANNEL 4



C

A) IO MICROVOLTS INPUT TO CHANNEL 2
B) GATING DRIVE TO CHANNEL 2



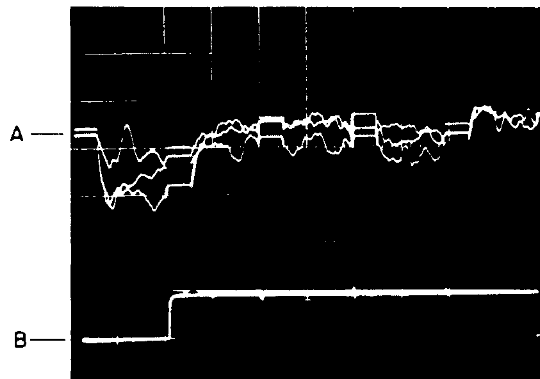
F

A) IO MICROVOLTS INPUT TO CHANNEL 5
B) GATING DRIVE TO CHANNEL 5

VERTICAL SENSITIVITY OF 'A' CHANNEL: 5 MILLIVOLTS / DIVISION
VERTICAL SENSITIVITY OF 'B' CHANNEL: 20 VOLTS / DIVISION
TIME BASE: I MILLISECOND / DIVISION

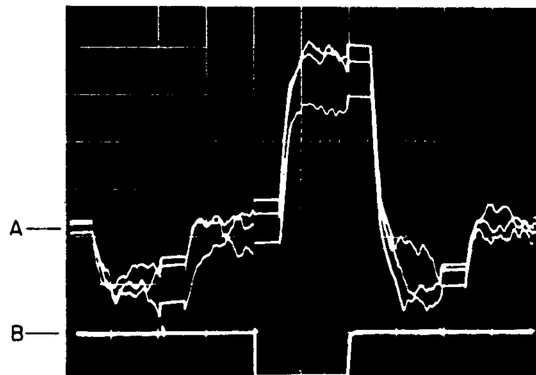
21665

Figure II-3 COMMUTATOR PERFORMANCE AT −50°C WITH 2N3610 TRANSISTORS



A

A) ZERO MICROVOLTS INPUT
B) GATING DRIVE TO CHANNEL I

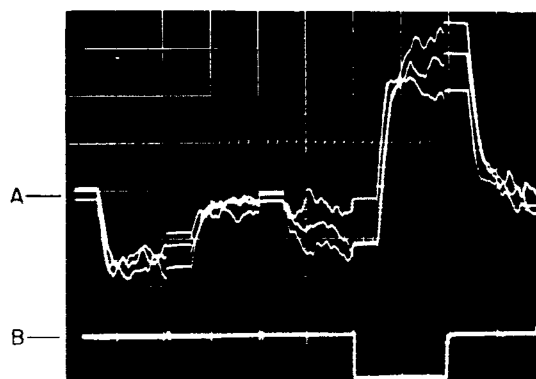


D

A) IO MICROVOLTS INPUT TO CHANNEL 3
B) GATING DRIVE TO CHANNEL 3

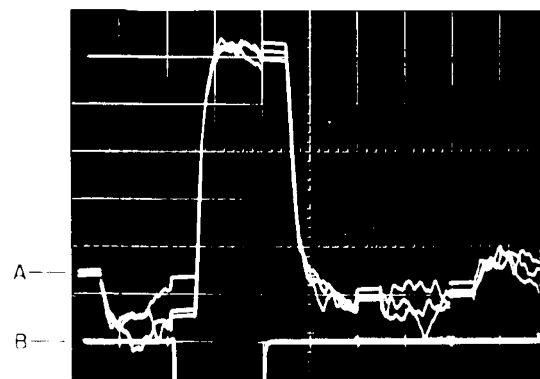
B

A) IO MICROVOLTS INPUT TO CHANNEL I
B) GATING DRIVE TO CHANNEL I



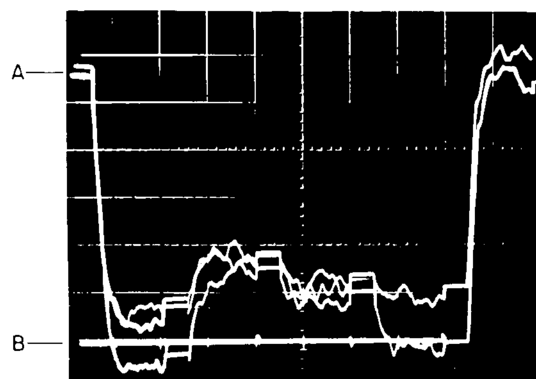
E

A) IO MICROVOLTS INPUT TO CHANNEL 4
B) GATING DRIVE TO CHANNEL 4



C

A) IO MICROVOLTS INPUT TO CHANNEL 2
B) GATING DRIVE TO CHANNEL 2



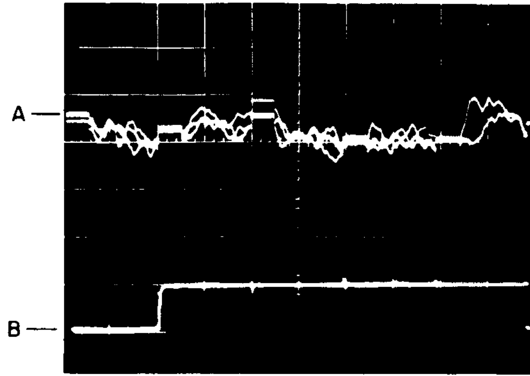
F

A) IO MICROVOLTS INPUT TO CHANNEL 5
B) GATING DRIVE TO CHANNEL 5

VERTICAL SENSITIVITY OF 'A' CHANNEL: 5 MILLIVOLTS / DIVISION
VERTICAL SENSITIVITY OF 'B' CHANNEL: 20 VOLTS / DIVISION
TIME BASE: I MILLISECOND / DIVISION

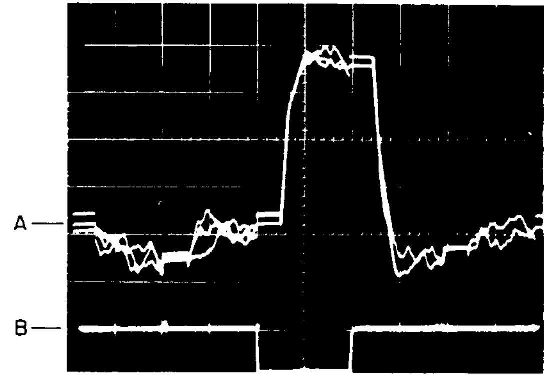
21666

Figure II-4 COMMUTATOR PERFORMANCE AT 0°C WITH 2N3610 TRANSISTORS



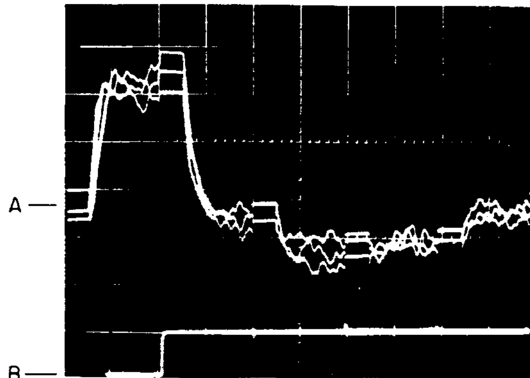
A

A) ZERO MICROVOLTS INPUT
B) GATING DRIVE TO CHANNEL I



D

A) IO MICROVOLTS INPUT TO CHANNEL 3
B) GATING DRIVE TO CHANNEL 3

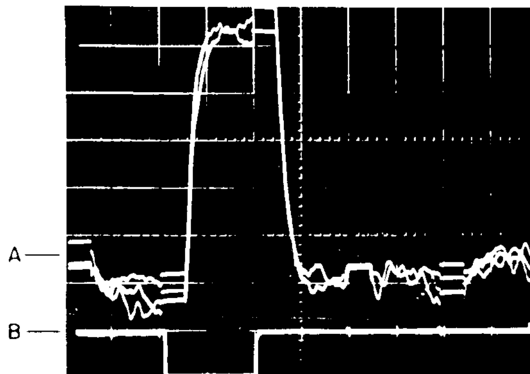


B

A) IO MICROVOLTS INPUT TO CHANNEL I
B) GATING DRIVE TO CHANNEL I

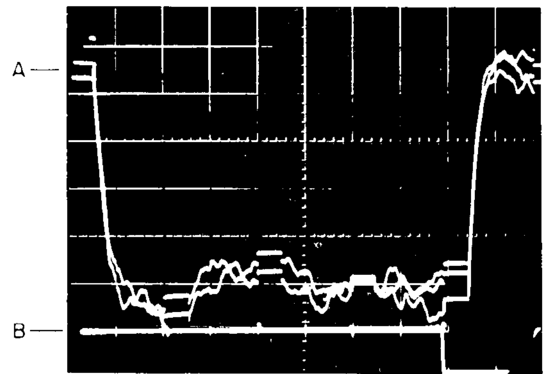
E

A) IO MICROVOLTS INPUT TO CHANNEL 4
B) GATING DRIVE TO CHANNEL 4



C

A) IO MICROVOLTS INPUT TO CHANNEL 2
B) GATING DRIVE TO CHANNEL 2



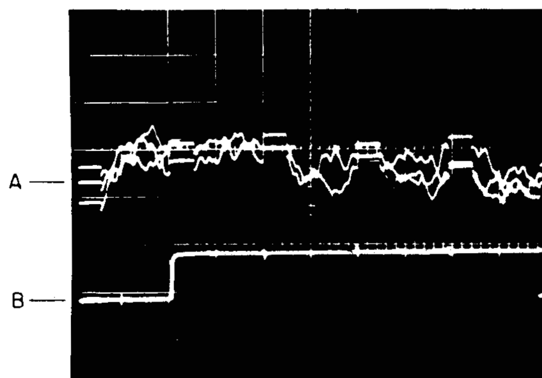
F

A) IO MICROVOLTS INPUT TO CHANNEL 5
B) GATING DRIVE TO CHANNEL 5

VERTICAL SENSITIVITY OF 'A' CHANNEL: 5 MILLIVOLTS / DIVISION
VERTICAL SENSITIVITY OF 'B' CHANNEL: 20 VOLTS / DIVISION
TIME BASE: I MILLISECOND / DIVISION

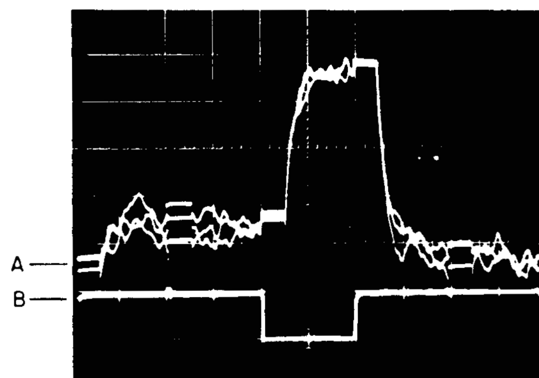
21667

Figure II-5 COMMUTATOR PERFORMANCE AT +25°C WITH 2N3610 TRANSISTORS



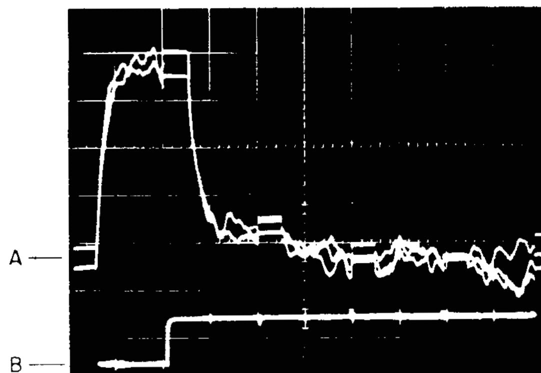
A

A) ZERO MICROVOLTS INPUT
B) GATING DRIVE TO CHANNEL I



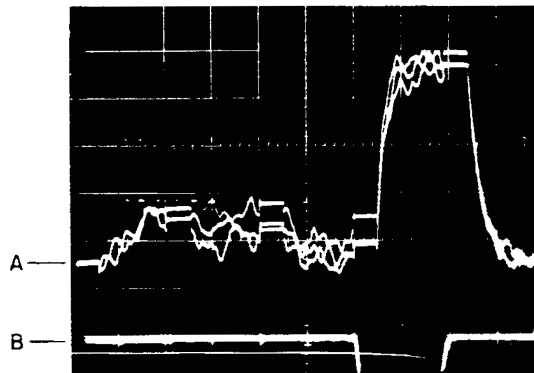
D

A) IO MICROVOLTS INPUT TO CHANNEL 3
B) GATING DRIVE TO CHANNEL 3



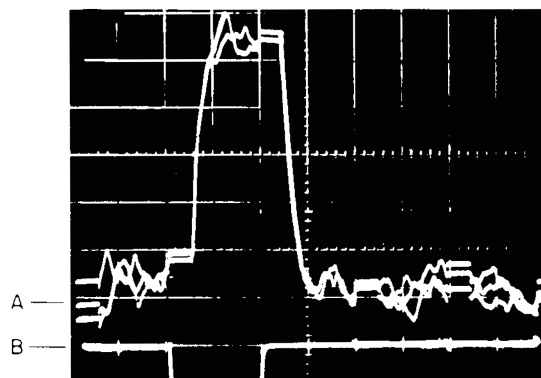
B

A) IO MICROVOLTS INPUT TO CHANNEL I
B) GATING DRIVE TO CHANNEL I



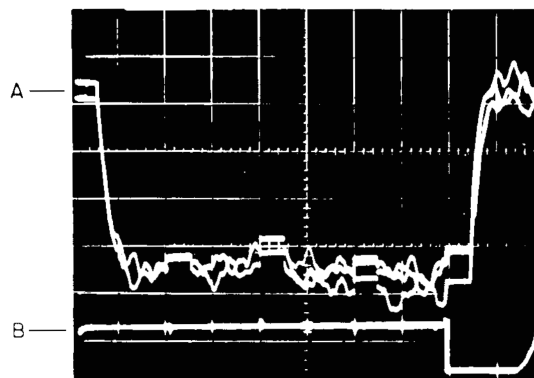
E

A) IO MICROVOLTS INPUT TO CHANNEL 4
B) GATING DRIVE TO CHANNEL 4



C

A) IO MICROVOLTS INPUT TO CHANNEL 2
B) GATING DRIVE TO CHANNEL 2



F

A) IO MICROVOLTS INPUT TO CHANNEL 5
B) GATING DRIVE TO CHANNEL 5

VERTICAL SENSITIVITY OF 'A' CHANNEL: 5 MILLIVOLTS / DIVISION
VERTICAL SENSITIVITY OF 'B' CHANNEL: 20 VOLTS / DIVISION
TIME BASE: I MILLISECOND / DIVISION

21668

Figure II-6 COMMUTATOR PERFORMANCE AT +90°C WITH 2N3610 TRANSISTORS

The 0°, +25°, and +90°C test results were obtained using the full system bandwidth of 4 to 800 cps. Except for the usage of the 20 cps high pass filter at low temperatures, all test conditions were the same as used for the type 2N3608 tests covered in the body of this report.

II.D CONCLUSION

The ability of the commutator test setup to accommodate the "repaired" type 2N3610 transistors, in spite of their widely differing characteristics, is indicative of the non-critical nature of the MOS FET commutator concept. The signal transfer efficiencies obtained thru each commutator channel was strictly a function of the "on" impedance of the associated MOS FET transistor and the commutator output load impedance. As with the more ideal undamaged type 2N3608 transistors, spurious signals due to the gate drives were eliminated by the subsequent circuitry. Also, only minimal thermal problems were experienced, which, as with the 2N3608 tests, were most likely due to the limitations of the commutator breadboard test setup, and not to any inherent problems within the MOS FET devices themselves, nor with the basic commutator concept.