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SEVENTH QUARTERLY and SUMMARY REPORT

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PREPARED FOR

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NASA
HUNTSVILLE, ALABAMA

INTERNATIONAL BUSINESS MACHINES CORPORATION
Federal Systems Division
ROCKVILLE, MARYLAND

ABSTRACT

This document is the Seventh Quarterly Report on NASA Contract No. NAS 8-11050, Special AROD System Studies. It constitutes a final report on all items of the amended Work Statement currently in effect, in the form of Technical Summaries (Section 2), which present major conclusions and identify the Quarterly Reports that should be referred to for greater detail.

Section 1 (Phase Lock Loop Advanced Circuit Investigations) contains both a technical summary of this task as well as a final report on an analog memory - aided loop engineering model for alleviating the reacquisition problem occasioned by booster flame attenuation of the AROD signals. The final circuit configuration is discussed in detail and represents some changes in technique beyond those presented in the Sixth Quarterly Report. The performance obtained upon this model permits signal reacquisition delay intervals of the order of 100 milliseconds for worst case simulated signal conditions. This work demonstrates the value of built-in loop memory of a Doppler rate estimate in eliminating the penalties associated with instituting a search and acquisition cycle for relatively short duration signal fades.

CONTENTS

CONTENTS (Continued)

ILLUSTRATIONS

ILLUSTRATIONS (Continued)

TABLES

Section 1

PHASE-LOCKED LOOP ADVANCED CIRCUIT INVESTIGATIONS

1.1 Technical Summary of Phase-Locked Loop Task

Phase-locked loops are used in AROD to achieve the high degree of information accuracy required in such systems. To improve the accuracy, the following approaches have been investigated:

a. Reducing loop noise due to oscillator instabilities.

b. Using signal-adaptive controls to optimize the loop for changing signal conditions.

c. Using double integration loops (Type II) to avoid static phase errors.

d. Using memory-aiding to track fading signals.

A lower limit to information accuracy is imposed by the stability of the variable frequency oscillator in the phase-locked loop. Usually the greatest internal contributors to the loop phase errors, these instabilities are caused by long term (aging) and environmental (drift) effects as well as short term (random noise) effects. Selecting the type of oscillator depends to a large extent on the required tracking range of the oscillator. In general, for a very narrow tracking range, a crystal-controlled oscillator, which has excellent stability characteristics is used; for a wide tracking range, an L-C type oscillator is used to avoid the otherwise required frequency multiplication process and the accompanying increase of instabilities. The Third Quarterly Report contained a calculation of practically obtainable stability characteristics as well as considerations of optimum design and selection of oscillator configurations. An empirical comparison of oscillators by substitution methods was made in the Fourth Quarterly Report.

To improve tracking capabilities under conditions of changing signal characteristics, adaptive measures on a Type I phase-locked loop were considered. As shown in the Fourth and Fifth Quarterly Reports, a loop incorporating an automatic variable-gain phase-detector adapts to low signal-to-noise (SNR) conditions by reducing its bandwidth, thus improving the SNR enhancement. Increased signal dynamics, occurring at the higher signal-to-noise ratios are met by an increase in bandwidth, thus improving the tracking capabilities. Several forms of phase detectors were investigated to obtain miniaturization and/or integrated circuit compatibilities.

Experimental investigation of a Type II phase-locked loop has been performed to evaluate methods for reducing tracking errors and improving signal acquisition. A state-controlled variable frequency oscillator provides the second "ideal" integration in the loop. Several materials were investigated for use in the resonator circuit. It was found that the available polycrystalline ferro-electric capacitors, usually used because of more desirable driving characteristics, were unable to deliver a useful amount of state-control action. Bias control action as occurs with varactor type elements prevented correct Type II loop operation by producing the non-desired "spring-loaded" operation. Multi-aperture cores, inherently harder to drive due to the fundamental current control nature of transistor devices, exhibit insufficient Q's or frequency deviation control characteristics. Employment of these elements resulted in a Type I loop with memory configuration but considerable difficulties were encountered to prevent loop instabilities, because of gain changes. Investigations of the use of minor loop, rather than series network compensation, to stabilize the loop lead to further increase in complexity. Supplier response indicated little interest in efforts to improve either type of resonator elements.

Although successful unaided acquisition for steady (i.e., zero doppler rate) loop inputs was achieved, the AROD System characteristics indicate that a perfect memory of doppler offset alone is insufficient to allow signal fading.

The presence of a doppler rate requires a memory of that signal parameter to achieve rapid reacquisition of a faded signal. The significance of a fully memory-aided loop has been described in the Fifth Quarterly Report and shows that a considerable reduction in required loop bandwidth (loop natural frequency) can be achieved. Several system configurations implementing the desirable memory-aiding were advanced. The most advantageous configuration uses a single analog memory device to store both doppler offset and rate. In both the Sixth Quarterly and in this final report, design considerations are presented. Using the AROD System requirements, a memory-aided phase-locked loop was designed and contructed. An empirical comparison with a non-aided loop is given and clearly indicates the vast improvement in reacquisition capabilities with memory-aiding over a wide range of signal conditions and durations of signal dropout.

1.2 Analog Memory-Aided Phase-Locked Loops

1.2.1 Design Considerations

In a signal tracking system such as AROD where signal fading can occur, it is highly desirable to design the phase-locked tracking loop with a capability for rapid reacquisition when the signal reappears. If a high degree of tracking accuracy or operation at low signal-to-noise ratios is required, the bandwidth of the phase-locked loop is narrow, and consequently the acquisition capabilities are limited. A system of switchable filters could be implemented where a wide-band filter is used during an acquisition mode and which is replaced by a narrow-band filter as soon as lock is achieved. However, under low signal-to-noise ratios, this scheme could fail since the wide-band loop will be poisoned by the noise and lock-on may not be achieved or the proximity of a signal may not even be detectable.

A more flexible system would incorporate some form of memory into the loop. Here the current signal parameters are continuously stored in a memory device which upon loss of signal uses the last available data in a non-volatile manner to maintain the loop in continuous readiness to accept a reappearing signal with a minimum of delay. It accomplishes this by steering the loop continuously along the path of expected signal values.

That a Type II phase-locked loop, which contains two perfect integrations, cannot fulfill this requirement has been discussed in the Fifth Quarterly Report.* Although it is capable of maintaining the last loop position indefinitely, the Type II loop, without external aiding, cannot predict and correct itself in anticipation of future signal characteristics. In the AROD System a Type II loop would maintain the doppler offset (A) at signal dropout, which is of doubtful value in the presence of a doppler rate ($\dot{A}$), which causes the loop to be in error when the signal does reappear. Although it could reacquire this signal if no doppler rate were present after a long delay, it would most often fail to lock against an existing doppler rate. This is shown in Figure 1-1 where the required loop natural frequency of a Type I or Type II loop is plotted vs doppler rate with dropout time as a variable. Experiments described in a later section verify this very closely.

It is therefore of vital importance not only to store both doppler offset (signal "position") and doppler rate (signal "velocity"), but also to correct the loop continuously during the dropout phase and the reacquisition period up to the moment of phase-lock using both stored signal data.

1.2.2 Design Approach for Memory-Aided Phase-Locked Loop

To achieve the doppler and doppler rate corrective measures during signal fade, two memory devices, which are continuously updated during the tracking

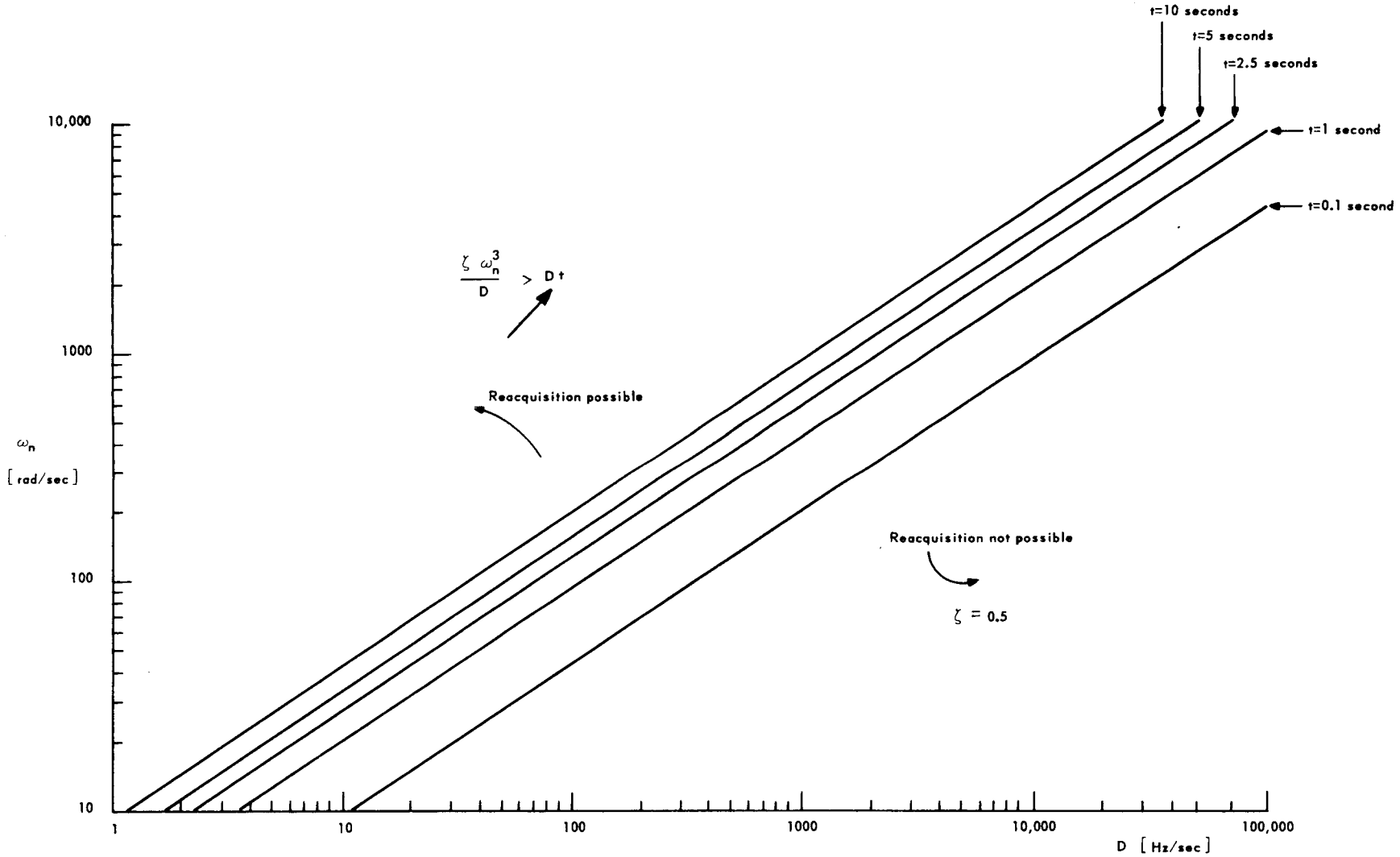


Figure 1–1. Maximum Permissible Doppler Rate vs Loop Natural Frequency

phase of the loop, can be used. After loss of signal normal loop operation is discontinued, and the voltage controlled oscillator (VCO) is supplied with the stored last data of doppler offset, corrected by the stored last doppler rate integrated with time from dropout. This control, representing an estimate of the signal, is continued upon reappearance of the signal until phase lock has been achieved. To allow for a permanent disappearance of the signal, the loop can, after a reasonable wait-time, discontinue the "memory-mode" and initiate a normal search procedure. The doppler information is available in analog form as the voltage controlling the VCO, while a measure of doppler rate information is present as the loop phase detector output, if the loop gain is high enough to make the doppler offset error at this point negligible.

As has been outlined in the Fifth Quarterly Report, a shortcoming of this method is that the memory steers the VCO directly and that upon reacquisition, a discontinuation of the memory-aiding will cause an immediate unlock, producing a large frequency offset error. Instead of an abrupt discontinuation of the memory-aiding, this approach would require a slow transfer of the memory data to the loop integrator (loop filter) to avoid an unlock. As this transfer process is equivalent to a doppler rate on the signal, the rate of transfer is determined by the tracking capabilities of the loop. This evidently means that a second signal fading cannot be tolerated until after some settling time.

The most advantageous approach to memory implementation uses a single analog storage device, which monitors the phase detector (loop multiplier) output. This output contains - besides the ever present noise - measures of both the necessary doppler offset and doppler rate information. The storage device continuously follows the detector output during the loop's "track mode" and produces a synthesized duplicate of doppler and doppler rate which, on a signal loss, is applied in a non-volatile manner to the loop as a substitute for the detector output. This control is continued until the loop achieves reacquisition of the reappeared signal. After lock, since it will be replaced immediately

(negligible time delay) by a corresponding shift in the phase detector output, generated by a small phase change of the VCO's frequency the control is removed safely.

Several modes of operation can be distinguished. Each has its particular required system configuration. During the initial acquisition mode or search mode, the loop in its normal configuration is supplied with a search control which sweeps the VCO through a predetermined range to find a signal. Since in the AROD System a signal is always moving in one direction in frequency, it is advantageous to sweep the VCO in an approaching rather than in a "chasing" manner. If the presence of a signal in proximity is detected and the search is removed, the signal will then "slide in" into the lock-on range of the loop. If the sweep is in the opposite (chasing) direction, it is possible that the search is removed at a point where capture is not achievable with the result that the signal will move even further away, restarting and restopping the search cycle. The sweep therefore is applied as a sawtooth rather than as a triangle. The period of the sawtooth sweep is determined by the system specifications and will determine some of the requirements of the proximity detector such as sensitivity and integration time, as will be shown later. A case can be made for sweeping over a narrower range of the doppler spectrum since, in the AROD application, a new signal always appears near one end of the range. However, the complexities of distinguishing between a recent signal which had an excessively long drop-out and a new signal do not seem to warrant the decrease in search time (or increase in lock detection sensitivity). Also, with the approach-search, it is not necessary to insert an additional sweep to simulate doppler rate since the signal will automatically move into the capture range. In this search-mode, the memory circuit is not connected to the loop and can be discharged if desired. Sensing of the sweep range must be accomplished to limit the sweep to the range of expected signal frequencies. A monitor of the control voltage of the VCO will suffice.

After capture of the signal has been achieved, the loop functions in the tracking mode. The search is disconnected while the memory circuit is now continuously monitoring the signal characteristics, present in analog form at the loop's phase detector output. The memory circuit in this mode operates as a unity gain amplifier, the output of which is disconnected from the loop. An integrator is required in the memory circuit to improve the signal-to-noise ratio and to smooth out any fluctuations in the doppler rate or in the tracking process. The time delay of this integrator is of even more importance when a signal drop-out occurs. It will prevent a serious decay of the information data before this circuit can be placed in the storage-memory mode. A time constant at least 100 times larger than the loss-of-signal detection time constant will maintain the information to a better than 1% accuracy. Too large a time constant will prevent a close signal characteristic approximation in the presence of a doppler rate derivative.

If the signal disappears the system transfers to its memory mode. The integrator of the memory circuit is (rapidly) disconnected from the loop phase detector and transformed into an analog storage device with low volatility. The output of the memory, representing in analog form the last known signal characteristics, is now gated into the loop to drive the loop filter/amplifier with a control that steers the VCO in a manner identical to the steering it received when still tracking the last signal. The loop, or VCO output, will therefore follow a path of expected signal values, maintaining the VCO in proximity of the estimated but absent signal. Because of the imperfect character of the loop integrator, the rate compensation during the dropout (but not the offset data) will slightly decay with the time constant of the loop. For instance, if the loop time constant is 150 secs and a 2.5 secs dropout is encountered, the rate compensation is in error by about 2% at the end of the dropout, and therefore of little significance. To obtain a perfect compensation, a current driven correction to the imperfect loop integrator would be required but is not considered

worthwhile. During the memory mode, the loop phase detector output contains only noise if properly in balance, and if desired can be left connected to the loop filter without adding a steering voltage.

When the signal reappears after the dropout, the loop will operate in its reacquisition mode. During the reacquisition process, the memory steering control continues until lock has been achieved while the pull-in and lock-on controls are obtained from the loop phase detector output. Thus, in this mode, both the phase detector and the loop memory unit must be connected to the loop filter. Because of the memory-aiding, reacquisition will occur rapidly. After reacquisition is achieved, the loop transfers back to its memory mode.

If the signal does not reappear within a reasonable time, it is desirable for the AROD System to initiate a new search cycle. In this case, the stored memory is of little value and can be wiped out if desired, e.g., by switching the memory into its sense-track configuration.

It is clear that the different modes of operation require a number of sense and control circuits in addition to some high performance gate switches and a sophisticated memory device. The gate switches and the memory device can be implemented using one of the latest developments in semiconductor technology, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), described in the Sixth Quarterly Report. The principal characteristics of interest are its zero offset switching capabilities in contrast to conventional bipolar transistors, and their extremely high input impedances, a necessary adjunct to obtaining a near perfect analog storage with a capacitor.

The sense and control circuitry, for which simplicity must be a major design goal, consists of several functional sections. A lock-detector is required to indicate when the loop is phase-locked on a signal. Since the phase-locked loop causes the phase detector to be null-seeking, a 90^{o} phase shifted lock-detector will produce a maximum dc indication at phase lock, while a normal

beat tone appears when the VCO is in proximity of the signal. As with the loop itself, filtering of the noise is required. The lock-detector is driven by both the VCO and the incoming signal (plus noise) while a 90^{o} phase shift is placed in either input. Following the detector, some amplification is required to increase the dc level to a useful control voltage. Following the amplification of the detection signal is the gate control circuit, used to switch the memory gates into their proper mode. As will be seen, the two gates of the memory device are always switched in opposition so that the control circuit requires just two opposite output drivers.

In addition to the use of the detector as a lock indicator, it serves as a proximity detector to initiate search when no signal is present or to prevent search when a signal is close enough to the VCO that acquisition is possible. Therefore, a delayed control circuit is required that, after a signal loss of a predetermined time, initiates a search, while the presence of a signal will immediately disable and reset the timer to prevent this search. The output of this timer is used to drive a search-gate, which passes a search control to the loop when required.

A search control voltage is derived from a multi-vibrator, which supplies a positive or negative voltage through the search-gate to the loop. Feedback is obtained by monitoring the drive voltage to the loop VCO. To sweep in a saw-tooth fashion, the voltage to the loop filter capacitor is supplied through a large resistor in one direction and through a high conductance, low-leakage diode in the other direction. Timing of the sweep is determined by proper selection of the series resistor to the loop filter capacitor and the driving voltage.

The system block diagram is shown in Figure 1-2. The loop input signal is derived from two inputs, one from a motor drive swept HP606A Signal Generator, through a Signal Interrupter to simulate signal dropouts, andthe other from a GR1390B Noise Generator, which are combined by filtering, addition and

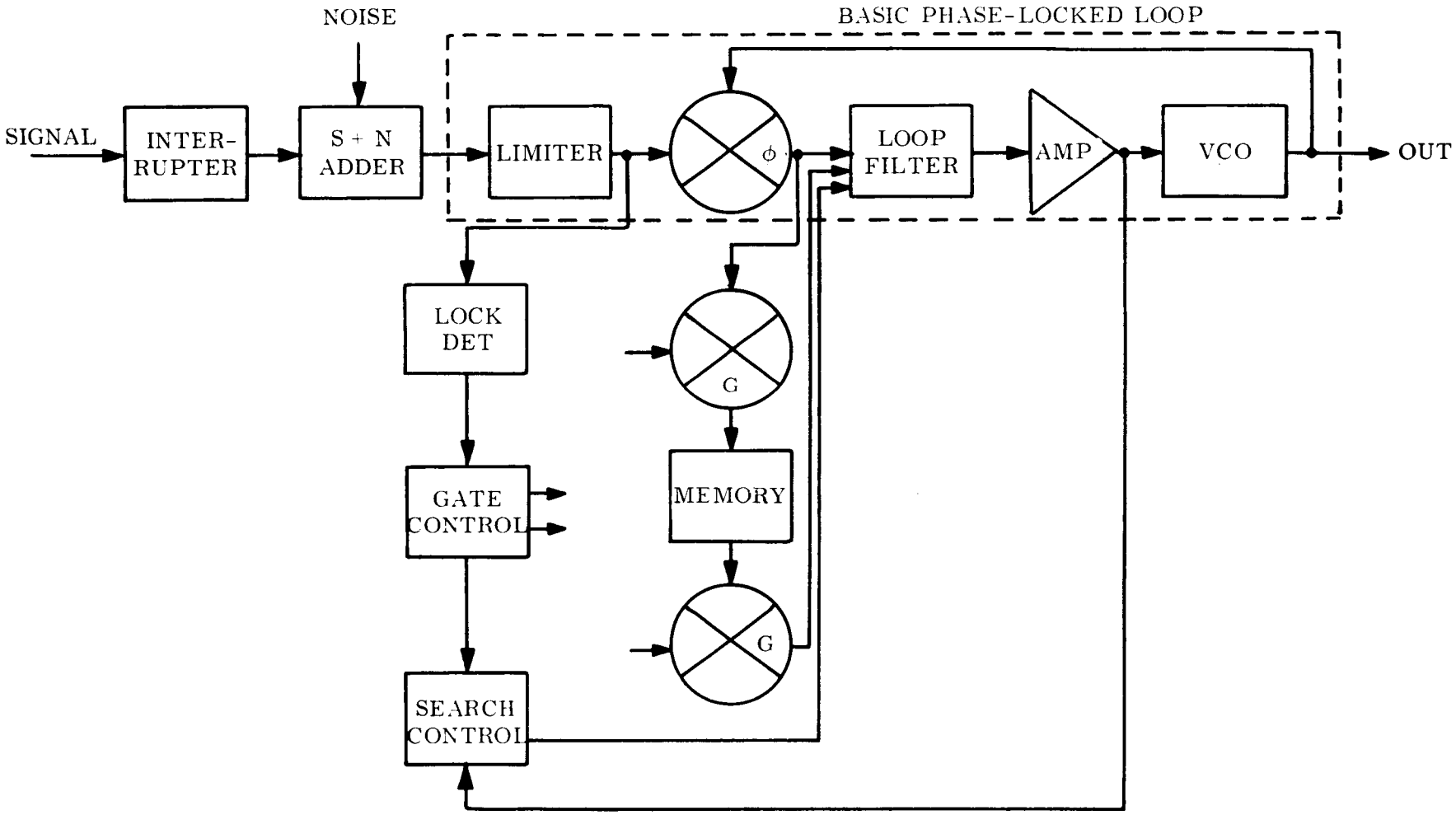


Figure 1–2. System Diagram of Memory-Aided Phase-Locked Loop

amplification processes in an S/N Simulator. The basic loop configuration is shown in dashed lines. The additional circuitry of memory, lock detection, and automatic search control is derived from the output of the loop limiter and phase detector and feeds into the loop filter.

The system parameters are given in Table 1-1. These parameters are selected to meet the various AROD specifications of sensitivity and accuracy as outlined in the Fifth Quarterly Report (p. 1.28). To obtain the required high degree of accuracy at all signal-to-noise ratios, while maintaining maximum tracking and acquisition capabilities, the loop is designed with a self-adapting gain feature. This feature results in a narrow bandwidth at low SNR's to reduce phase noise errors and an increasingly wider bandwidth at higher SNR's to accommodate existing higher signal dynamics. Table 1-1 illustrates this and shows the change of parameters of the loop with an accompanying change in tracking ability. All data is given for a non-aided, no-memory loop configuration. If the knowledge of expected signal characteristics is applied as aiding to the loop, acquisition behavior is drastically improved, as will be shown for reacquisition on memory. The tracking and phase noise errors, or the system accuracy are not affected by this method of aiding.

1.2.3 Design of System Components

1.2.3.1 Loop Limiter and Phase Detector

The loop limiter and phase detector (multiplier) used for the experimental investigation are essentially the same as used for a previous program (refer to the Fourth Quarterly Report, p. 1-17) and are shown in Figure 1-3. An additional output from the loop limiter has been provided to drive the lock detector.

The limiter, consisting of an integrated differential amplifier MC 1110 and a pair of clipper diodes, FD 600's, is used to limit the drive to the phase detector to a convenient level. The phase detector consists of a balanced pair of out-of-phase drivers using 2N916 transistors, and a pair of balanced high frequency

Table 1–1. System Parameters

	Symbol	SNR -20db	SNR ∞	Dimension
Loop Gain	K	1.5×10^6	15×10^6	sec^{-1}
Gain ϕ Det	K_ϕ	0.05	0.5	volts/rad
Gain Filter	K_F	0.5	0.5	-
Gain DC Amp	K_A	200	200	-
Gain VCO	K_O	3×10^5	3×10^5	rad/volt sec
Loop Time Constant	t'	150	150	sec
Loop Time Constant	t	15	15	msec
Natural Frequency	ω_n	100	316	rad/sec
Damping Factor	ζ	.707	2.24	-
Two-Sided Bandwidth	B_2	106	525	Hz
Static Phase Error ($\frac{A}{K}$) (100 KHz)	ϕ_s	0.4	0.04	Radians
Dynamic Phase Error ($\frac{A}{\omega_n 2}$) (667 Hz/sec)	ϕ_d	0.4	0.04	Radians
Pull-In Range (from C.F.) A = 0	Ω_{SS}	2.750	15500	Hz
Pull-In Range (from C.F.) A = 160 Hz/sec	Ω_{DD}	110	3500	Hz
Pull-In Range (from C.F.) A = 1600 Hz/sec	Ω_{DD}	-	350	Hz

diodes, arranged in a half bridge. Mixing the clipped loop input signals with a voltage from the voltage controlled oscillator produces the required difference frequency. Some filtering is added to remove the rf components of the output.

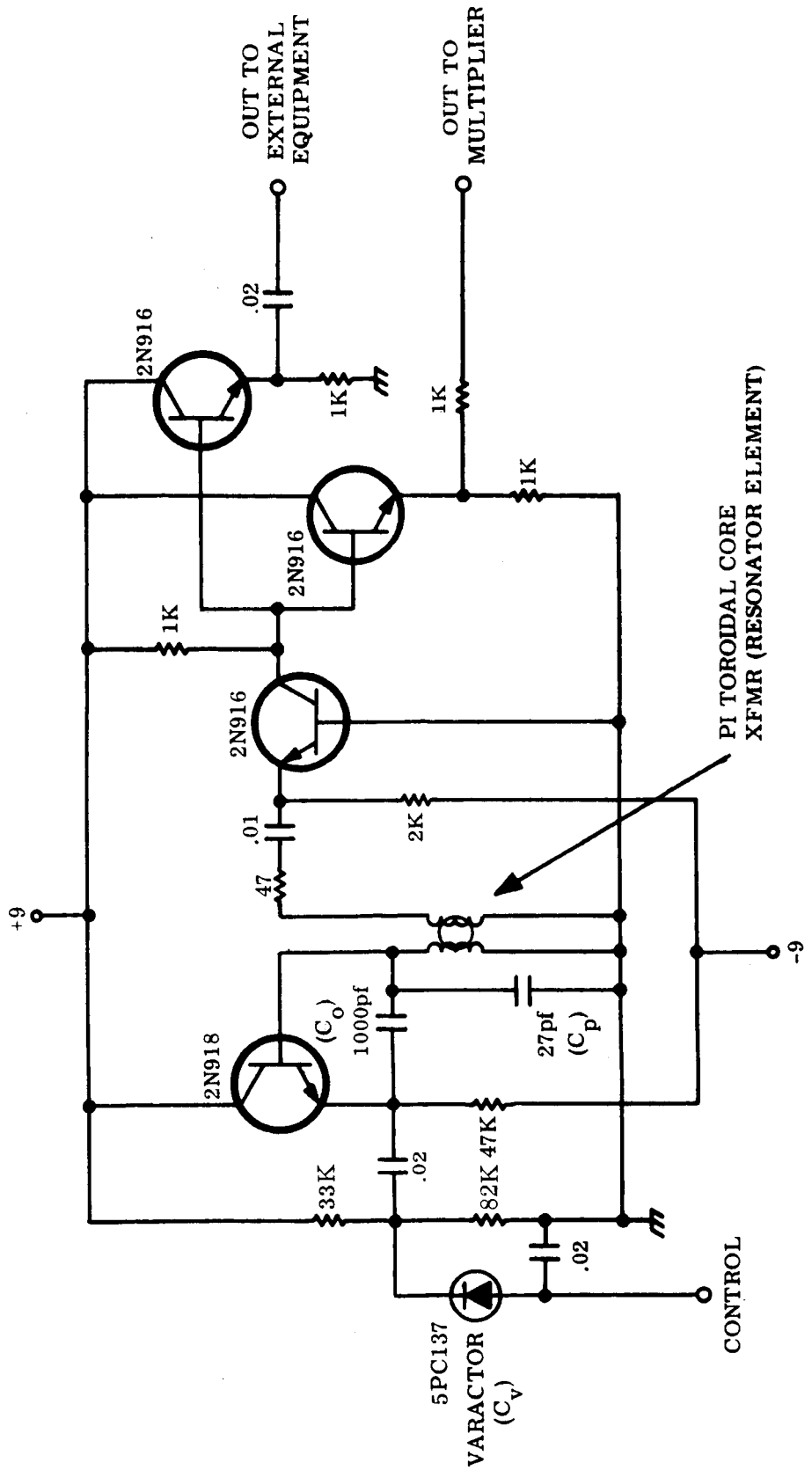


Figure 1–3. LC Voltage Controlled Oscillator

The non-linear gain characteristics of the limiter-phase detector combination, available at sufficient oscillator drive, can be successfully used as an adaptive measure of matching the loop characteristics to the signal parameters. A curve of multiplier gain as function of input signal-to-noise ratio is given in Figure 1-4, identical to Figure 1-7 of the Fourth Quarterly Report.

The important characteristics of the loop can therefore be summarized by the multiplier gain

K_m = 0.6 volts/rad, for SNR = + 20 db

K_m = 0.17 volts/rad, for SNR = - 10 db

1.2.3.2 Loop Voltage Controlled Oscillator

The voltage controlled oscillator used for the loop is essentially the same as used for a previous investigation (Fourth Quarterly Report Page 1-9) and is shown in Figure 1-5. The bias resistors on the varactors, the controllable elements of the oscillator's tuned circuit, have been changed to provide a stiffer bias.

The performance objectives of high stability and wide deviation range have been achieved using discrete L-C components for the tuned circuit of the oscillator. Isolation amplifiers following the basic oscillator prevent loading of the tuned circuit and provide drive signals to the loop phase detector and the associated lock-detector. The phase stability, or coherence time of the oscillator, was previously found to be adequate for the AROD application. The coherence time, calculated from measurements, was about 5000 seconds, which is equivalent to a phase noise error of about 0.7 milliradians RMS. This is well below the level of phase noise caused by random noise input signals to the loop. The long term instability caused by aging or environmental changes requires a slight widening of the minimum deviation range of the oscillator, and results in

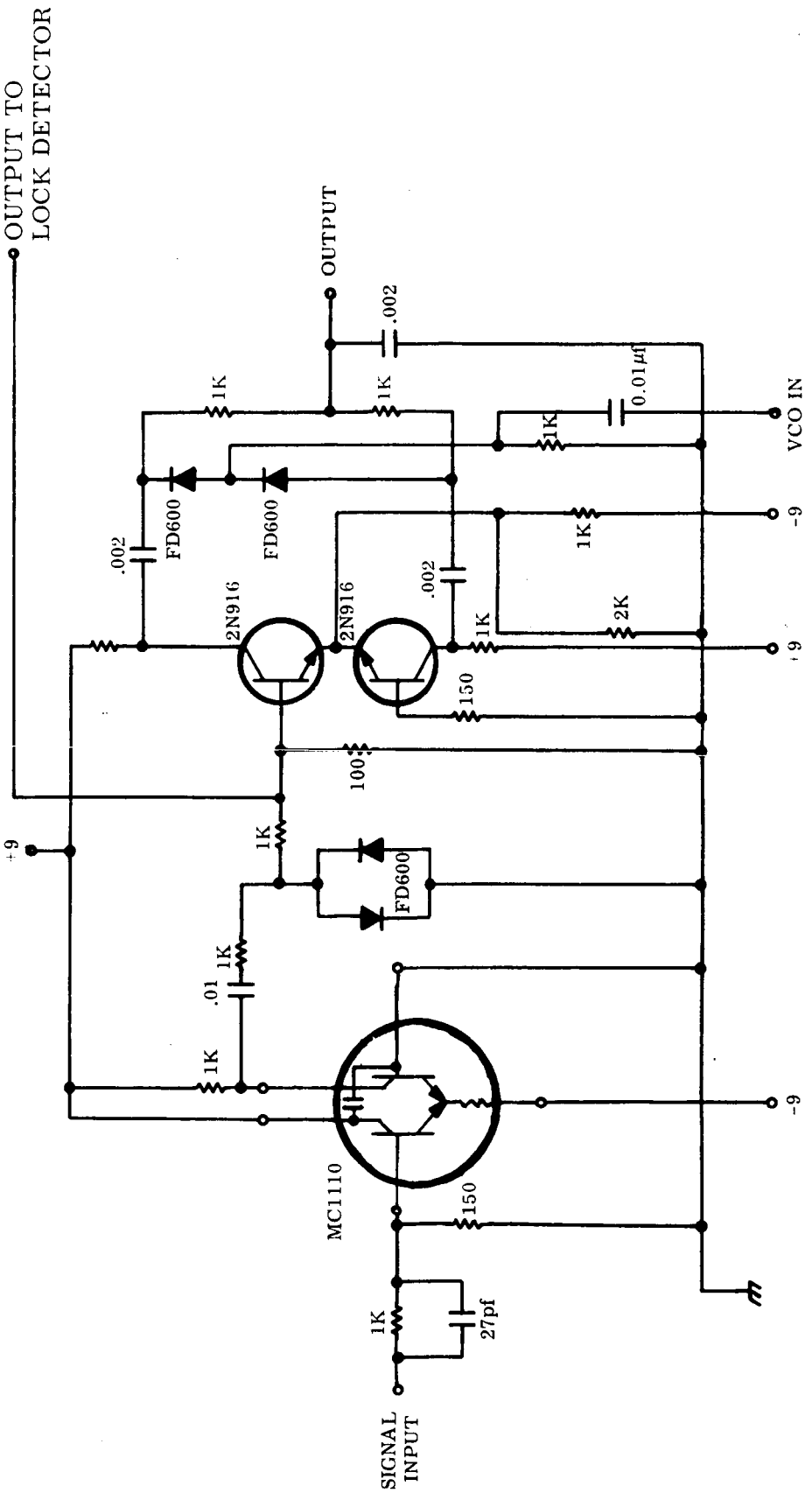


Figure 1–4. Loop Limiter-Phase Detector

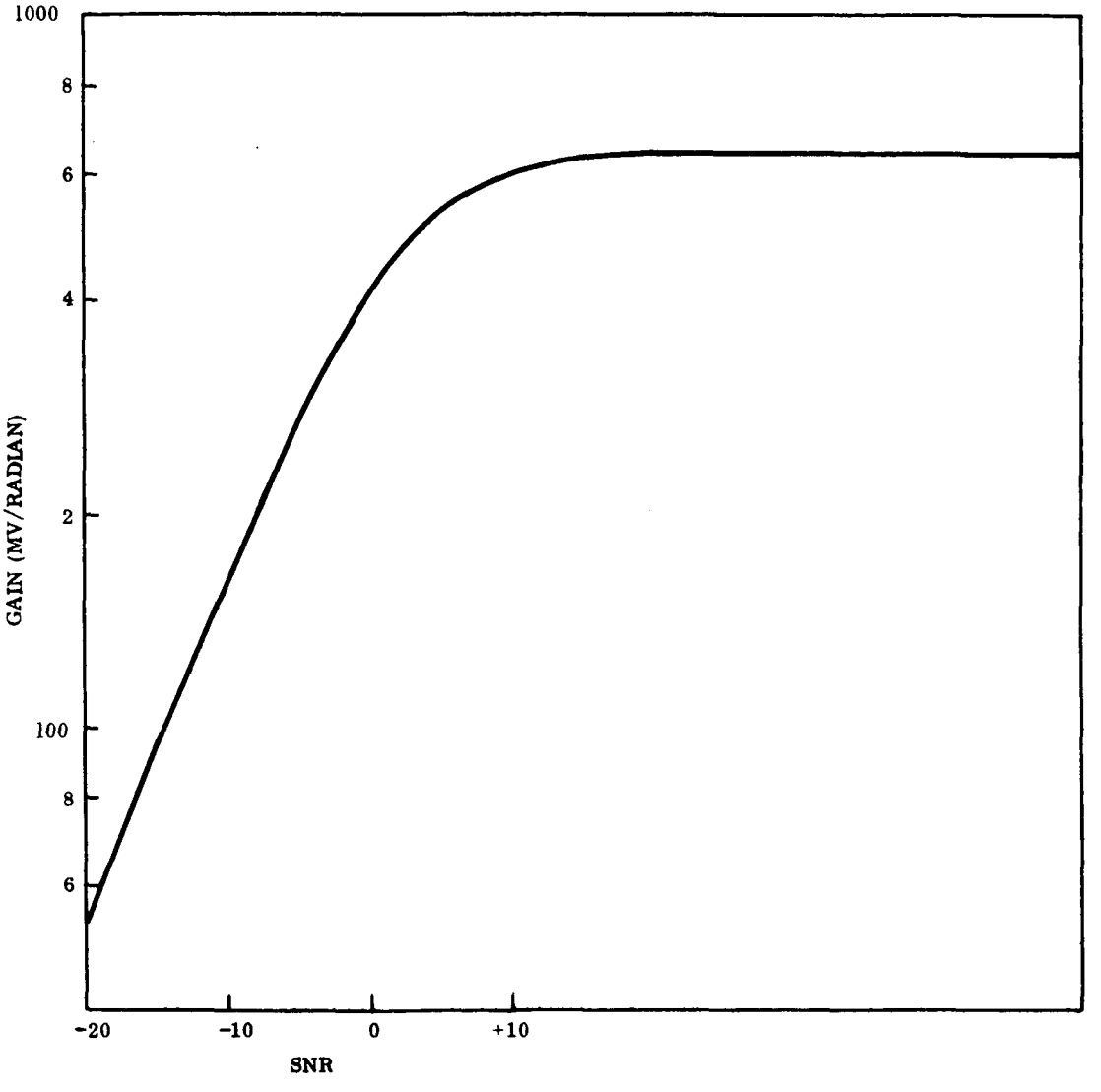


Figure 1–5. Multiplier Gain vs SNR

a small additional static phase error encountered when tracking a signal. This phase error is proportional to the drift of the oscillator but will be small for a reasonable stability specification.

The remaining important characteristic of the VCO is its transfer characteristic, which can be expressed as a gain, in rad/sec per volt. The gain for this oscillator is not constant over the total frequency deviation range, which will result in a change in loop gain with frequency. The gain at center frequency (2.0 MHz) is

$$K_{VCO} = 3 \times 10^5 \text{ rad/sec/volt.}$$

while at the extremes of the tracking range it differs about 25% from the value at center frequency. Although not desirable, this variation is not detrimental to the performance of the loop and no effort has been made to improve this characteristic. It, however, will affect some of the experimental behavior, causing tracking and acquisition to be weaker at the high end than at the low end of the frequency range.

1.2.3.3 Loop Filter and Amplifier

The transfer characteristics of the loop filter and amplifier are now determined and can be calculated from the required loop parameters and the established gain values of the loop VCO and phase detector. The most advantageous circuit is an active filter-amplifier configuration, using a differential operational amplifier to obtain the required gain. A highly stable gain is achieved and a considerable reduction in size of integrating capacitor. Because of the large value of required time constant (150 secs), a high quality capacitor must be used in addition to a minimization of parallel circuit leakage resistances. The circuit shown in Figure 1-6, uses the extremely high input impedance and feedback impedance of a pair of MOSFET devices, connected in a differential configuration.

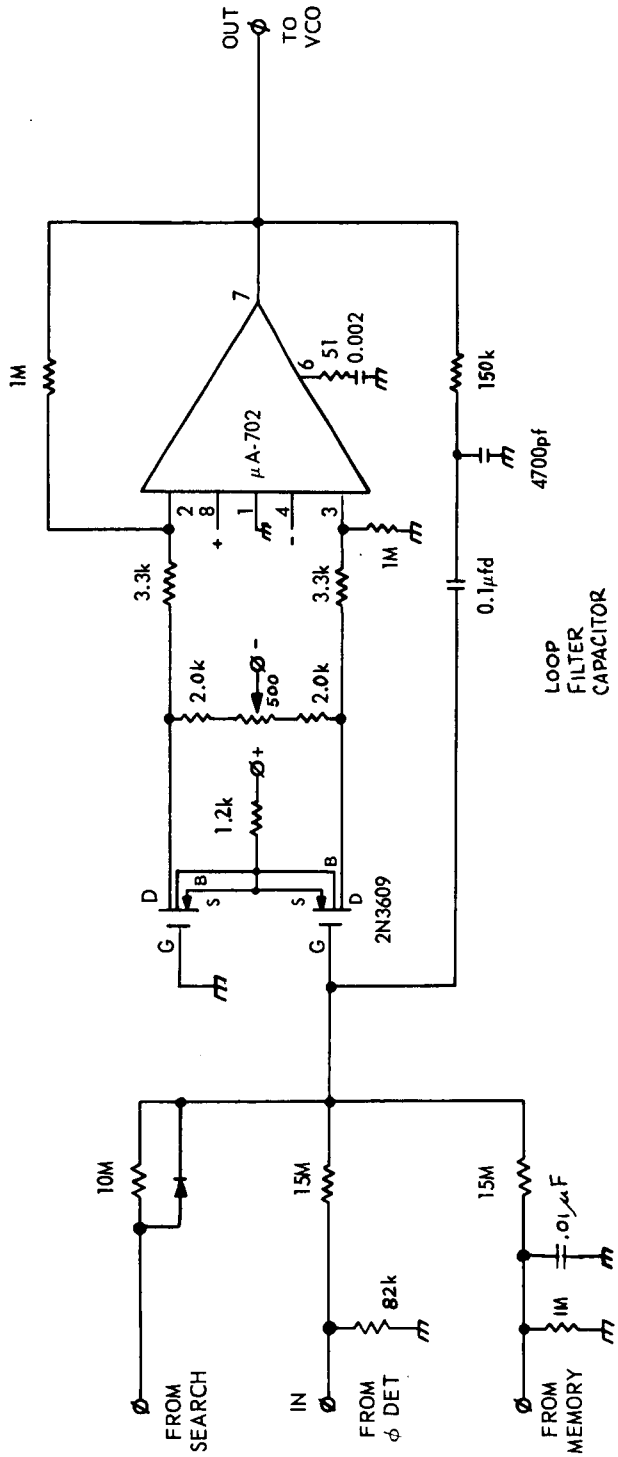


Figure 1–6. Loop Filter and Amplifier

This pair of transistors, mounted in a common can, drives an integrated differential operational amplifier, provided with d. c. feedback to maintain a constant amplifier gain of 200. A balance control is available to cancel any offset present in the double MOSFET or in the operational amplifier, which would otherwise affect the loop's center frequency.

The loop filter employed uses a high value of series resistance (15 megohm) with a capacitor-resistor network placed around the amplifier circuit. This arrangement effectively decreases the impedance of the feedback network by the open loop gain (200) resulting in an effective R-C network of 20 μF and 750 ohms. The d.c. gain of the filter is half because of the presence of a second 15 megohm series resistor required to supply memory information. This resistor also effectively reduces the large loop time constant by a factor of two. The overall characteristics of the filter-amplifier combination are therefore:

$$K = 1/2 \times 200 = 100$$

$$t' = 15/2 \times 10^{6} \times 20 \times 10^{-6} = 150 \text{ secs}$$

$$t = 750 \times 20 \times 10^{-6} = 15 \text{ msecs}$$

Some high frequency attenuation has been incorporated by means of bypass capacitors to eliminate a possibility of oscillation. The resistors connected to ground from the input terminals from the phase detector and from the memory insure a constant impedance and thus a transfer characteristic independent of the mode of loop operation.

A third input has been provided to insert a search control. A negative voltage applied to this terminal will charge the filter network resulting in a sweep of the VCO frequency. A positive voltage will rapidly charge the filter in the opposite direction, producing a re-cycle of the frequency sweep. This search terminal is open however during the track, memory, and reacquisition mode of operation.

1.2.3.4 Loop Memory

The loop memory must perform during the tracking mode of the loop as a perfect duplicator of the loop phase detector dc output signal, smoothed by the addition of a low pass filter. Upon loss of signal, the memory unit must convert to an essentially non-volatile storage device, presenting the duplicated voltage to the loop with no deterioration over time. This voltage, which contains the tracking errors of the loop, represents in analog form the dynamics of the received signal. Both the position of the signal as well as the future values are indicated.

The Loop Memory Unit, shown in Figure 1-7, must therefore contain an integrator to remove unwanted variations or noise, some analog signal gates to switch the unit in its two modes of operation and a unity gain storage device. For the gates, two MOSFET devices are used, using both the extremely high isolation impedance when switched "off" and the inherent zero offset when switched on. A drawback of this device usually is its relatively large on-impedance. However, this is of no significance because the on-impedance is very small compared with the series resistances used. Several resistors are added in the gate control circuit to protect against voltage transients on insertion and removal of the card. The input gate is used (in the track-mode) to connect the phase detector output to a filter consisting of a 2 megohm resistor and a 0.1 μF capacitor, while the output gate connects the memory output (in the memory, in the reacquisition, and, optionally, in the search mode) to the loop filter. The voltage on the integrating capacitor, representing the average signal data, is applied to a unity gain amplifier utilizing 100 percent feedback around a differential operational amplifier. This amplifier contains a pair of MOSFET devices and an integrated operational amplifier, with a balance control to cancel any offset. The open loop gain of about 10^3 insures that the closed loop gain is unity with an accuracy of about 0.1% providing a near perfect duplicate of the

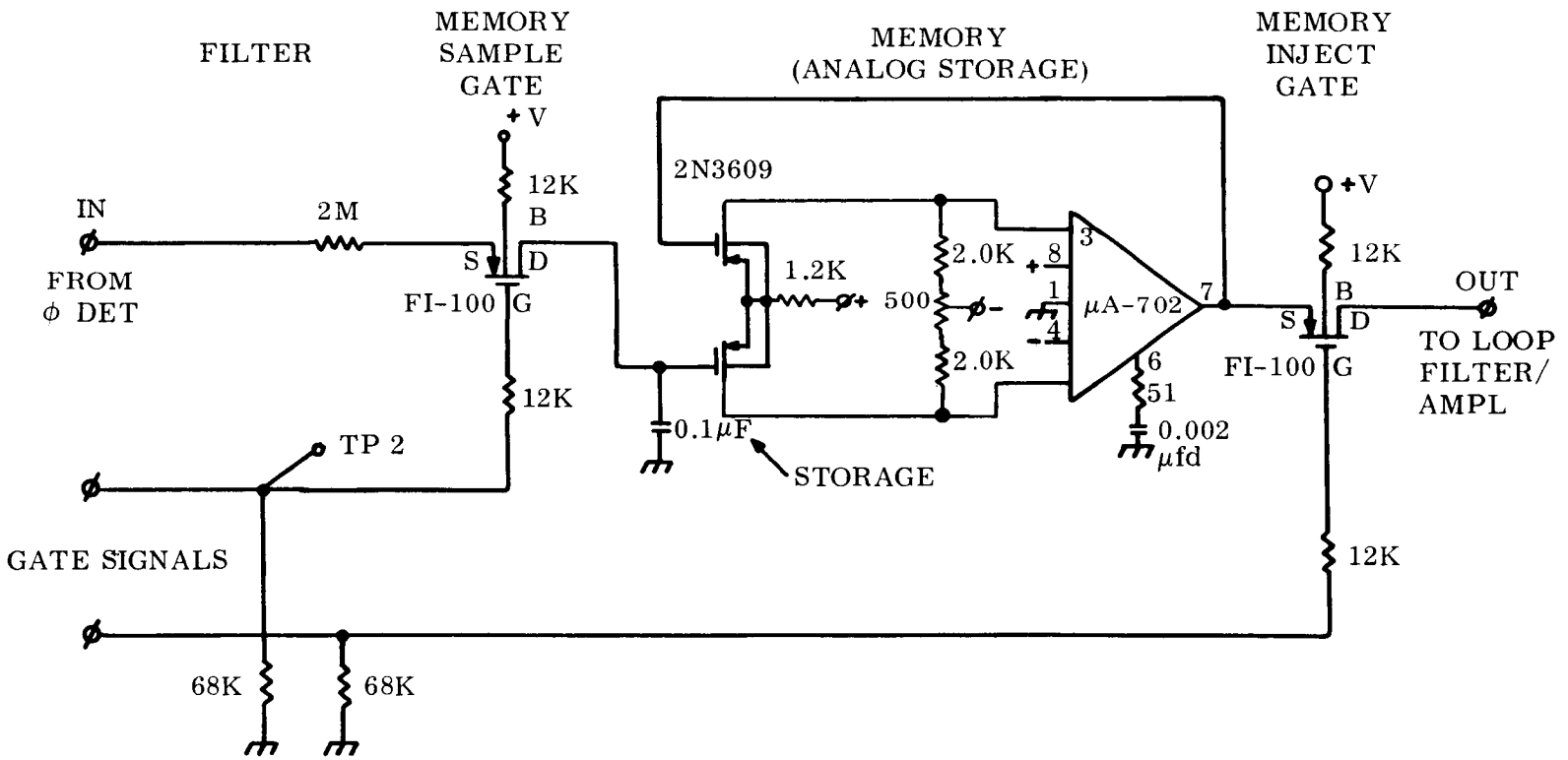


Figure 1–7. Loop Memory

input voltage at the output. After loss-of-signal, the input gate is switched "off". Since both the input impedance of the double MOSFET device and the gate off-impedance are extremely high, the voltage on the 0.1 μF storage capacitor is maintained with an extremely high time constant. Selection of a capacitor of proper material has resulted in time constants in the order of 10^5 -10^6 seconds or about a weekend, very much larger than the longest signal drop-out time anticipated. Since the capacitor voltage maintains its control on the "infinite" input-impedance amplifier, the output can supply a reasonable amount of power to its load at true fidelity.

The choice of time constant at the memory input, explained previously is determined by the following:

a. Amount of smoothing required.

b. Amount of decay encountered during the switching time of the gates.

c. Expected time between signal dropouts.

d. Derivative of the doppler rate on the signal.

The choice of 0.2 secs ensures that the memory will be correct within 1% against all expected values of dropout or switching times.

A further improvement in memory time constant could be obtained when using that same storage capacitor in a feedback arrangement around the operational amplifier, effectively increasing its time constant. However, the self leakage does not change and for any particular capacitor, a limit will be reached. Also, the circuit would then convert to a minus one amplifier, necessitating the use of an additional minus one amplifier to obtain the proper phase, and consequently increasing complexity and reducing reliability.

This type of Memory Device is useful possibly for a whole class of applications. In particular, in areas where the information to be stored is of a higher level, the disadvantage of offset and drift in offset will be less important. In

the phase-locked loop application, a phase detector with a higher gain would provide larger control voltages, minimizing the effects of offset drift in the memory.

1.2.3.5 Loop Control Circuit

The loop control circuit is added to the basic phase locked loop to provide the various control signals required for operation in different modes. This external circuit shown in Figure 1-8, consists of four major parts: an external phase detector with amplifier, a gate control circuit, a delayed search timer, and a search insertion circuit. The circuitry built for this investigation has not been fully optimized but is fully operational to supply the necessary functions.

The external phase detector is similar to the circuit used for the loop and also has the difficulty of maintaining its balance for various input conditions. A 90° phase shift network has been placed in the VCO input circuit. The result is that during signal locks when the loop phase detector seeks a null output, the lock detector will produce a maximum output, in this case a negative voltage. When unlocked, the output of the two phase detectors are essentially identical (but 90° shifted). The output of the lock detector is filtered to improve the signal-to-noise ratio, clipped, and amplified by a feedback-stabilized integrated operational amplifier. Its output is connected to a switch which is driven into saturation on signal-lock. If the loop is in the process of acquiring the signal, a beat tone will exist at the output of the lock-detector, which if passed by the filter will drive the switch in and out of saturation. This will cause the effect of periodic memory insertion at the rate of the beat tone into the loop during acquisition. During the initial acquisition, this effect will increase the amount of data supplied to the loop for acquisition and therefore will aid the acquisition process, although in a small amount. During reacquisition, after a signal has been lost temporarily, the periodic removal of memory-aiding will decrease the

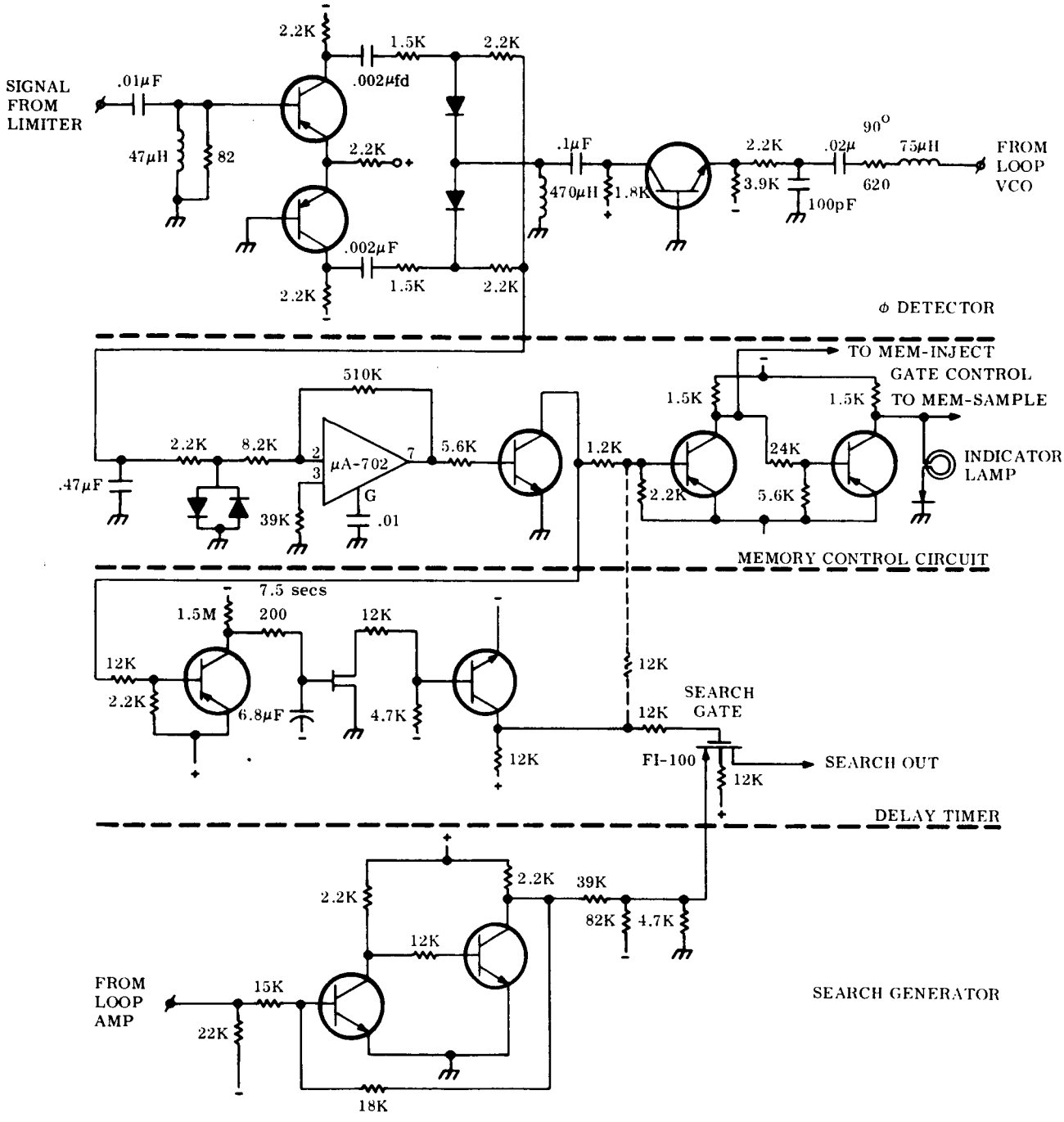


Figure 1–8. Loop Control Circuit

effect of aiding. This will occur only when the beat tone is of low frequency and the loop is very close to lock-on; therefore, this effect is also small. The amount of required filtering preceding the lock-detection amplification is therefore determined by several factors. The time constant should be high to obtain a high signal-to-noise ratio and to reduce the effect of memory switching. It should be low to afford a rapid search-cutoff when the presence of a signal in proximity has been detected after an initial search procedure. Although switched filters could be used, in this application, a filter with an approximate 1 msec time constant is sufficient.

The gate control circuit, driven from the lock detector switch, consists of two transistors driven in or out of saturation, supplying a positive or negative voltage in opposition to the two MOSFET gates in the memory unit. Additionally, either voltage can be used to indicate the presence of lock externally, as for computer or other measuring purposes. A small indicator lamp has been incorporated to supply visual lock-indication. During the measurement procedures, one of the output voltages has been used to trigger - after suitable filtering - a counter for measuring loop recovery time.

The output of the lock detector switch is used to drive a delay-search timer. The function of this timer is to allow the loop to reacquire a faded signal and to initiate a search after a reasonable, predetermined waiting time, in this case 7.5 secs to allow the observation of memory-aiding capabilities to the fullest extent. In addition, the circuit must be capable of removing the search with a minimum delay as soon as the lock-detector switch indicates signal in proximity, resetting at the same time the timer to its original state to provide for a possible next waiting period.

These requirements have been fulfilled in a simple switching arrangement with the addition of a charging network, consisting of a 1.5 megohm resistor and a 6.8 μF capacitor, driving a high input impedance field effect transistor. Rapid disabling is obtained by recharging the capacitor through a low impedance to its hold potential. The output of this timer is connected to a MOSFET gate, through which a search voltage is supplied to the loop in the search mode.

A MOSFET device is used here to ensure virtually complete isolation of the search in the other modes.

The search voltage is obtained from a bi-stable multivibrator, using the control voltage to the VCO as the feedback voltage to the multi. As has been shown before, the direction of search is important to the acquisition of the signal and should be in an "approaching" rather than in a "chasing" manner. A resistor-diode combination in series to the loop, Section 1.2.3.3 ensures that the search is conducted in a sawtooth fashion, driven from the multivibrator.

An optional function can be performed by the search control circuitry. With the addition of a resistor as shown in dotted lines in Figure 1-8, the application of search will also wipe the memory. A new signal can then be acquired without the effect of periodic insertion of a previous memory occurring when acquisition is imminent, even though this effect is relatively unimportant. With this arrangement, however, the signal previously available for indication of lock vs unlock now represents the states of lock and search vs memory. If only an indication of lock is desired, a separate indicator circuit would have to be constructed.

1.2.3.6 Signal Interrupter

To evaluate the behavior of the memory-aided loop under conditions of signal fading, a signal interrupter has been constructed capable of periodically removing the signal part of the input to the loop for a predetermined, controllable time.

The circuit shown in Figure 1-9 utilizes a unijunction transistor which fires at about 6.5 seconds intervals and delivers a pulse to the following circuitry. The period is determined by the charging network on the emitter of the unijunction, consisting of a 510 k ohm resistor and a 22 μF capacitor. The output pulse triggers a variable one-shot which remains in its non-stable state for a time determined by a 1 μF capacitor and the combination of a 68 k ohm resistor and a 2.5 M ohm potentiometer, and can be varied between 0.2 secs and 4 secs. This one-shot supplies a gating voltage to a FET gate which opens and closes the signal

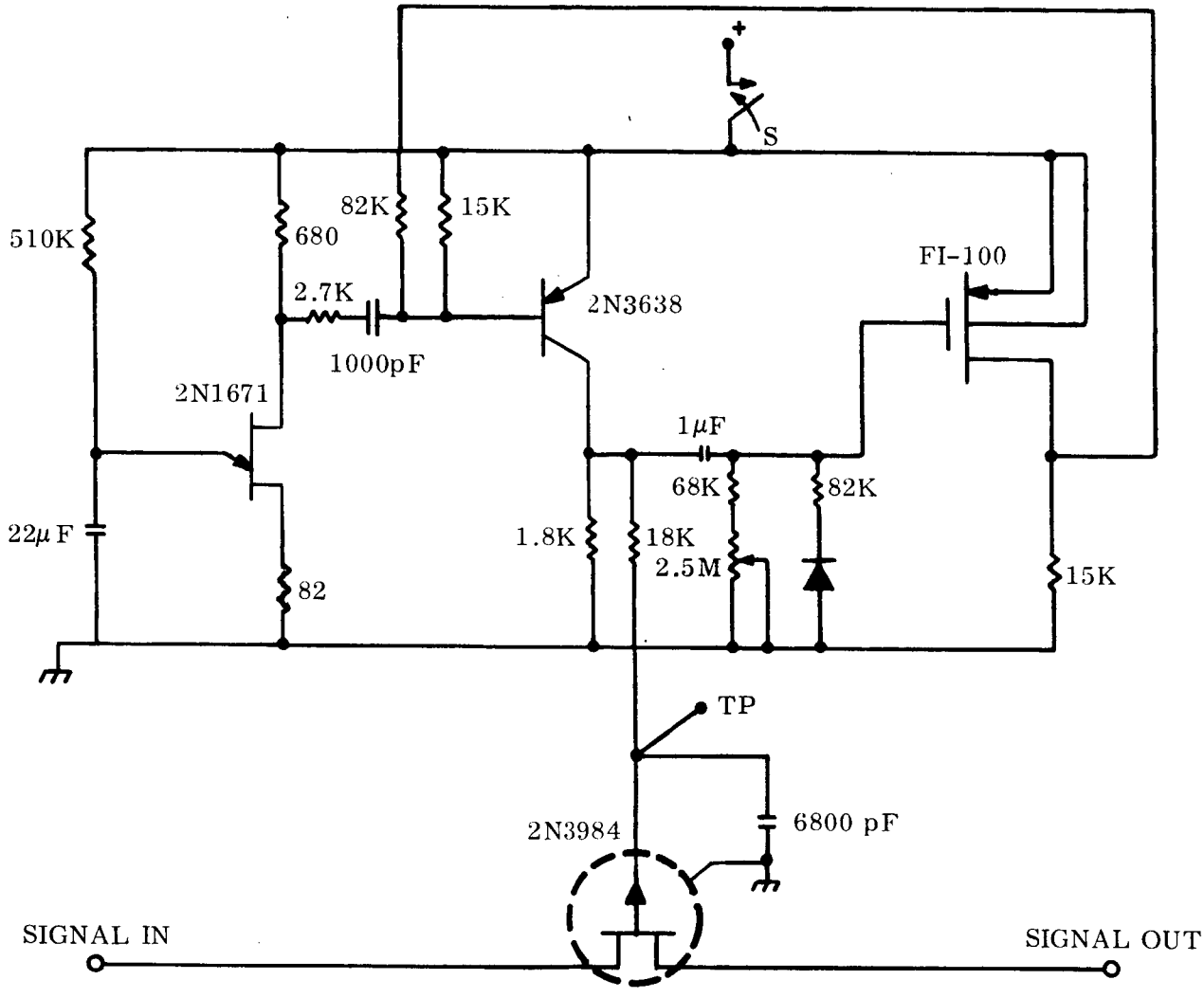


Figure 1–9. Signal Interrupter

path. Grounding of the case of this FET device in addition to an r-f bypass on its gate provides a switching isolation in excess of 60 db. The gate voltage can be monitored as an indication of the time of signal fade and can be used to trigger a counter for measurement of loop recovery time after a signal fade. A resistor-diode combination is placed in parallel with the one-shot timing resistor to provide a rapid reset of the one-shot without otherwise affecting the time. Since a positive voltage on the gate of the field effect transistor turns the signal off while a zero potential turns it on, removal of the supply power to this circuit provides a continuous signal.

1.2.4 Experimental Evaluation

The general characteristics of a phase-locked loop are well known. For this investigation, these characteristics have only been verified to ensure that the design met the requirements of accuracy and tracking capabilities. The various loop parameters have been checked on the individual loop components, and all data agreed well with the specifications listed in Table 1-1.

The addition to the basic phase-locked loop of a memory-aiding characteristic must be separately and empirically evaluated to obtain a knowledge of its effects on the acquisition problem of a narrow band phase-locked loop. The most significant and meaningful evaluation would compare a loop with memory-aiding with an unaided but otherwise completely identical loop for all values of signal drop-out time, doppler and doppler rates, and for the signal-to-noise ratios of interest.

The designed loop configuration lends itself well to such an investigation since a short on the output of the memory-gate will immediately convert the memory-aided loop to a non-aided loop and a comparison can be accomplished rapidly. In addition, the test equipment constructed or available is capable of providing any desired signal-to-noise ratio, doppler offset, signal drop-out time, while several values of doppler rate can be simulated.

A measure of effectiveness of memory-aiding is the recovery time of the loop. This recovery time or reacquisition pull-in time is the time interval between the moment of reappearance of a faded signal and the moment of frequency lock. Convenient test points are available to display this on a time interval counter.

Some general remarks can be made regarding all the measurements taken for this evaluation. Since the lock-indicator will also show the presence of a signal in proximity - by producing a square wave output - it could result in an erroneous time interval measurement if the count is stopped at the first zero crossing of this beat tone. To prevent this, the lock-signal is first passed through a filter network consisting of an 8.2 k ohm resistor and a .47 μF capacitor. Because of the unequal driving resistors feeding this network, not only filtering is obtained, but an average positive DC voltage will be built up when a beat tone is present, preventing the erroneous count. This can be seen clearly in the photographs taken of the filtered lock-detector output. However, a delay of about 7 msecs (when triggering at -6 volt) is now introduced in all data, limiting the sensitivity of all measurements. Since a loop reacquiring a signal in less than 10 msec can be considered an excellent device, this measurement delay can be considered insignificant.

In a number of loop conditions, several measurements had to be taken to obtain an average value of recovery time. The curves given are then drawn as the closest fit to the data points. Wherever the measured time is in the order of 7 msec, a straight line has been drawn to indicate the inability to read with higher sensitivity.

Wherever a curve comes to an abrupt end, as in the case of nearly all non-aided loop measurements, it shows the reacquisition beyond this end point does not occur because the signal falls outside the capture range of the loop.

For the non-aided loop, it can be expected that reacquisition becomes more difficult with longer signal drop-out times, lower signal-to-noise ratios, and increased doppler and doppler rates. For the memory-aided loop, the reacquisition time is theoretically independent of these signal characteristics. However, an unbalance in the memory device will cause a slow drift from ideal, causing a dependency on the signal characteristics, but to a much lesser degree than for the non-aided loop.

1.2.4.1 Recovery Time at a Fixed Doppler Offset

A comparison has been made at a doppler offset of 100 KHz between the two types of loops, in the absence of a doppler rate. Various signal-to-noise ratios have been used in addition to different signal drop-out times. As can be seen from Figure 1-10, the family of curves given for the no-memory loop indicates a very rapid increase in required pull-in time as the dropout time is increased, while a lower signal-to-noise ratio further deteriorates the reacquisition. Beyond a certain limit, which appears to be a pull-in time limit, no acquisition is possible because the VCO of the loop has, during the dropout time, drifted out of the pull-in range. This phenomenon would not occur with a Type II phase lock loop which, in the absence of a doppler rate, would always reacquire, although the pull-in time could become objectionably long.

In contrast, the loop with memory-aiding reacquires the faded signal rapidly as indicated by the second familiy of curves. In all cases of dropout time and signal-to-noise ratio reacquisition is achieved. It appears from these curves that the memory unit was improperly balanced, causing an increase in pull-in time as the dropout time is increased. A properly balanced memory would keep the VCO very close to the expected signal frequency and would make the pull-in time short and independent of fade-time. The graphs indicate however that even with this imbalance reacquisition is quickly achieved.

1.2.4.2 Recovery Time at a Fixed Doppler Offset and Rate

If a doppler rate is applied to the signal, the advantage of memory-aiding becomes even more apparent. Measurements were taken by applying a fixed doppler rate of 1.7 KHz/sec and interrupting the signal for various dropout intervals, all starting at a fixed doppler offset of 100 KHz, with the signal moving towards the center frequency of the VCO. This situation corresponds to a signal dropout soon after initial appearance. With reference to Figure 1-11, the same remarks can

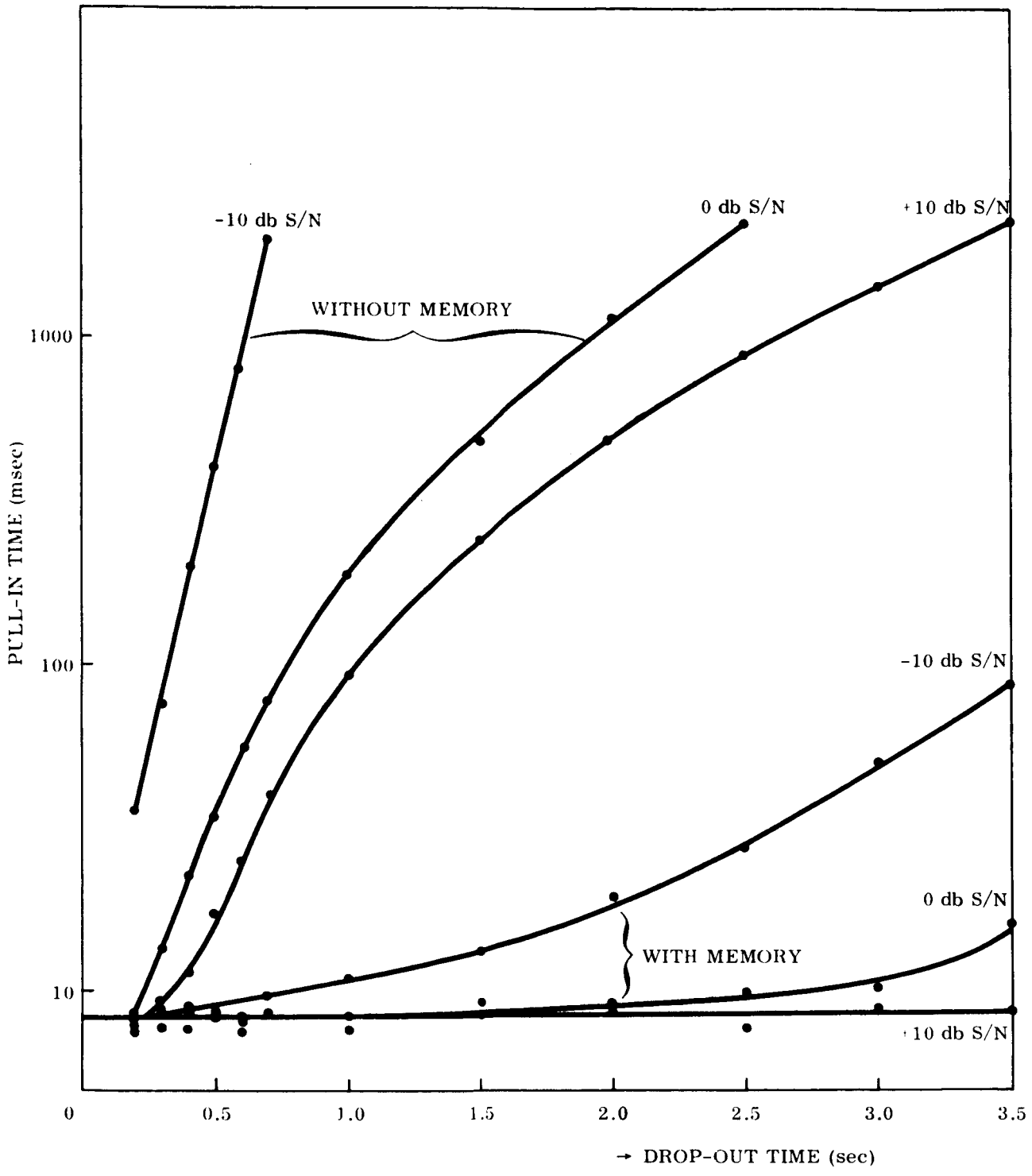


Figure 1–10. Reacquisition of a Faded Signal Doppler Offset = 100 KHz, Doppler Rate = Zero

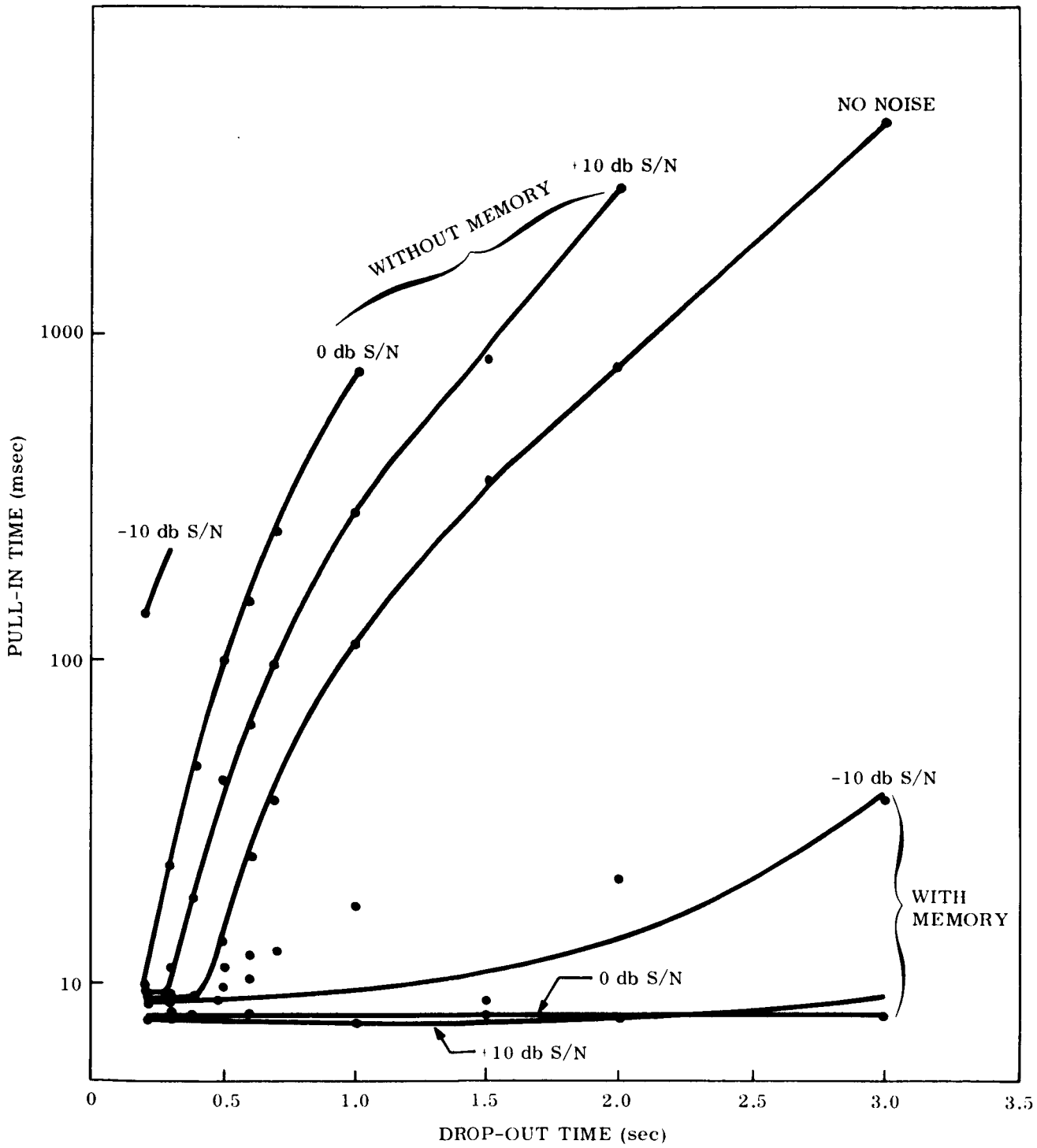


Figure 1–11. Reacquisition of a Faded Signal Doppler Offset = 100 KHz, Doppler Rate = 1.7 KHz/sec

be made regarding the reacquisition time for the sets of curves. The memory-aided loop reacquires very rapidly since its VCO is moved along with the absent signal by memory steering. Again, the non-aided loop fails to reacquire after a short dropout with a complete deterioration for the lower signal-to-noise ratios.

A comparison between Figures 1-10 and 1-11 shows that the application of a doppler rate - all other parameters being equal - gives a drastic decrease in re-acquisition performance of the non-aided loop. At the lowest system SNR of - 10db, the signal with doppler rate prevents acqusition beyond a 0.3 sec dropout (corresponding to a 150 Hz beat tone), while without doppler rate only a 0.7 sec dropout can be tolerated, (corresponding to a 350 Hz beat tone on reappearance). In contrast, the memory-aided loop is capable of reacquiring rapidly under all conditions.

1.2.4.3 Recovery Time Over the Tracking Range

If the signal is moving through the tracking range, simulating the normal AROD conditions, measurements of recovery time can be made at successive points of this range, dramatically demonstrating the shortcomings of a non-aided loop in actual conditions. When the first dropout occurs soon after the "first sighting", the signal and the VCO of the non-aided loop both move during the dropout towards the center frequency of the loop. At succeeding dropouts, the VCO will increasingly fall behind the signal and after the signal has passed the loop's center frequency ("overhead"), the VCO will actually drift in opposite direction from the signal during the dropout. It is therefore clear that reacquisition for the non-aided loop will be increasingly more difficult as the signal moves through the range and soon becomes impossible for the longer dropouts and lower signal-to-noise ratios. In contrast, the memory-aided loop will always follow the signal extremely close, and reacquisition is independent of the doppler offset. An imbalance in the memory unit will make reacquisition slightly dependent on the signal-to-noise ratio and the dropout time, but the loop will still reacquire rapidly. In Figures 1-12 through

1-15, the measurement results are shown with the signal moving through the tracking range from 1.90 MHz to 2.10 MHz, in that direction, each figure indicates the performance at a particular SNR. Data points at 1.90 MHz fall on the family of curves presented in Figure 1-11. From Figure 1-12, it can be seen that even for an infinite SNR, the loop fails to reacquire beyond the center frequency of the loop for as short a dropout time as 0.4 secs. The usable range rapidly decreases as dropout time is increased and as SNR is decreased. At an SNR of -10 db, only a 10 kHz range is available at the short dropout time of 0.21 secs. In contrast, the loop with memory-aiding has, even in the worst condition, a better than 65 msec average recovery time, and thus only the extremes of dropout conditions are shown in the graphs.

Several factors somewhat distort the pictures presented for the non-aided loop. The doppler rate applied is not constant over the range but changes linearly—from 1.66 kHz/sec to 1.95 kHz/sec—because of the non-linear frequency adjustment of the motor-driven signal generator used. This non-linearity will make it slightly more difficult for the non-aided loop to reacquire at the end of the tracking range. A second factor will have a somewhat larger effect, but its influence could not be measured precisely. The voltage controlled oscillator used for the loop is non-linear in its transfer characteristic resulting in a higher gain at the lower tracking frequencies, with consequently a reduced tracking and acquisition ability at the end of the tracking range. Linearization of the VCO transfer characteristic would produce a reacquisition behavior more predictable by calculation. However, the general results will be closely identical to those presented in Figures 1-12 through 1-15. The expected curves would be starting at the same data point (1.90 MHz) but would not slope quite as severely. Therefore, it would tend to increase the useful tracking range for a particular dropout time and SNR, but would still deteriorate very quickly with increased dropout time and decreased signal-to-noise ratio.

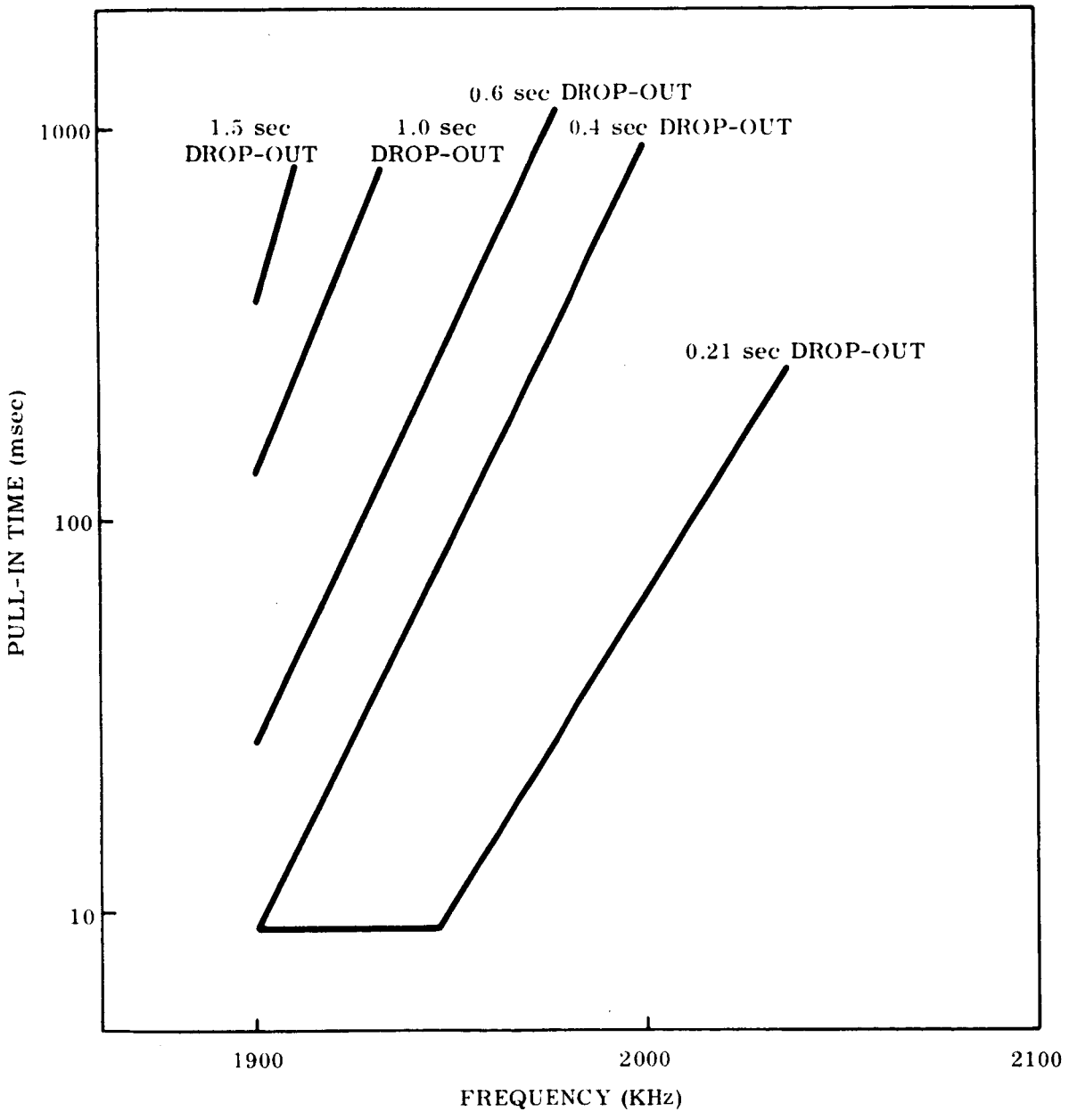


Figure 1–12. Reacquisition of a Faded Signal over the Tracking Range Doppler Rate = 1.7 KHz/sec, S/N Ratio = ∞

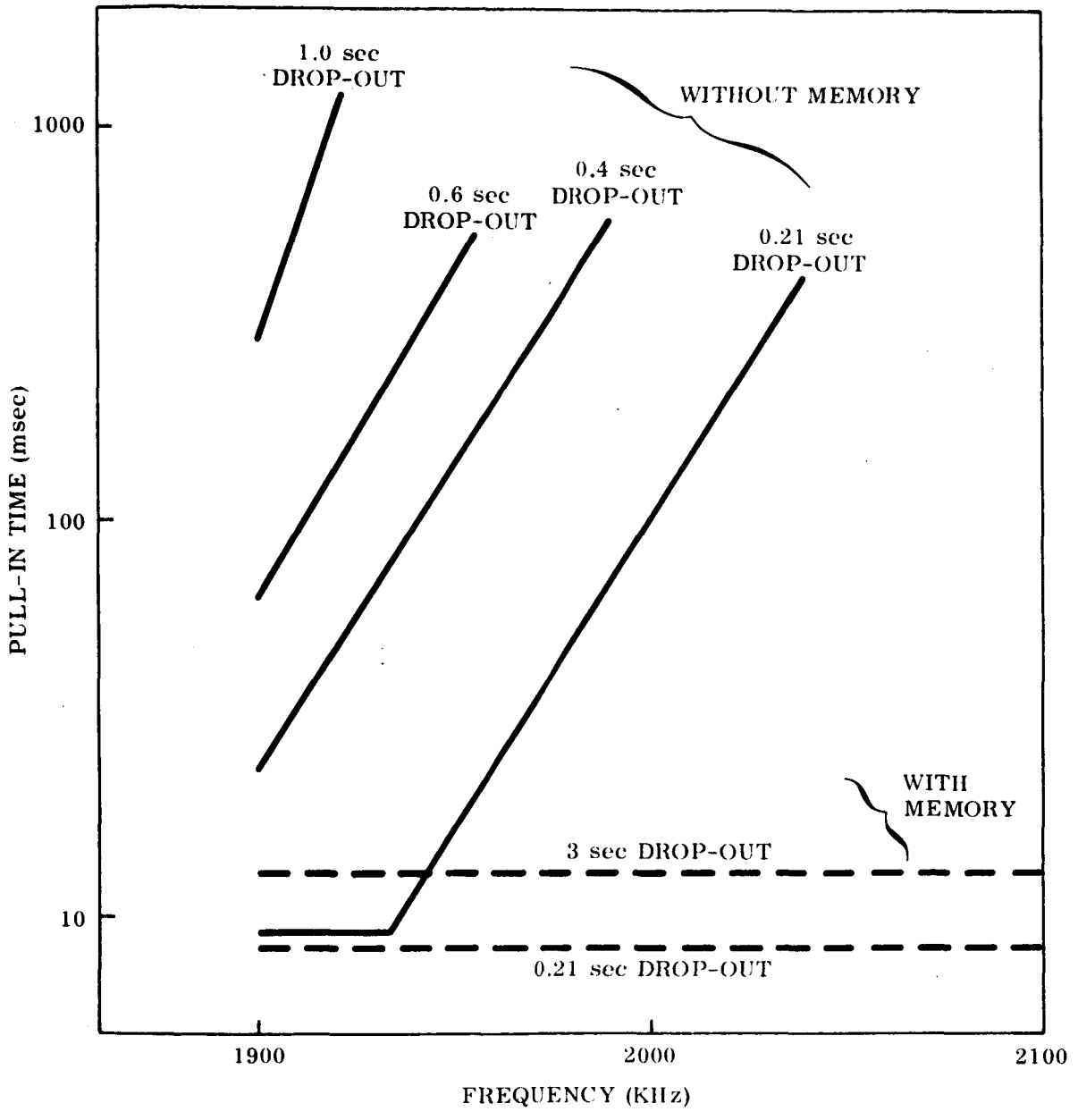


Figure 1–13. Reacquisition of a Faded Signal over the Tracking Range Doppler Rate = 1.7 KHz/sec, S/N Ratio = + 10 db

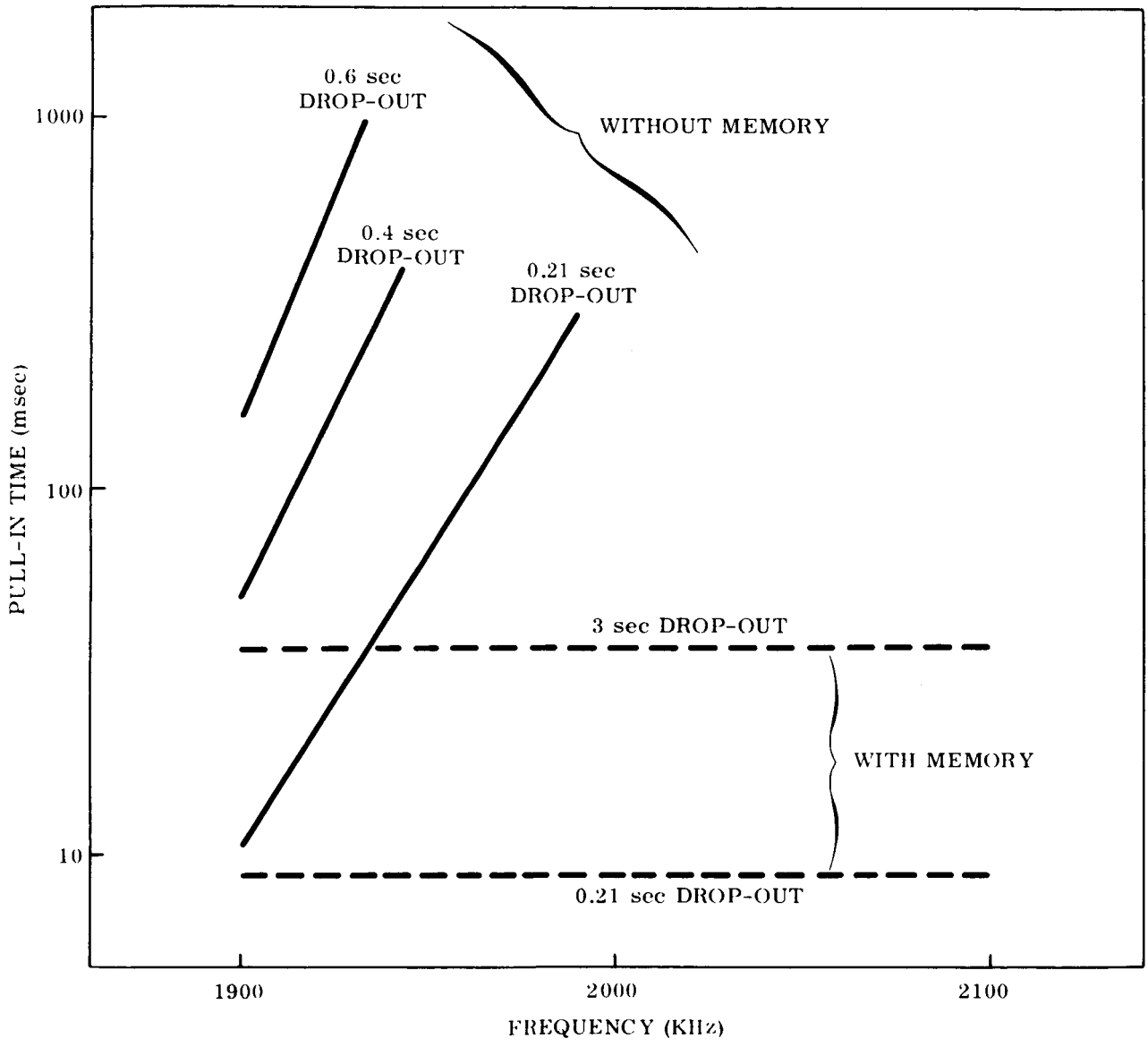


Figure 1–14. Reacquisition of a Faded Signal over the Tracking Range Doppler Rate = 1.7 KHz/sec, S/N Ratio = 0 db

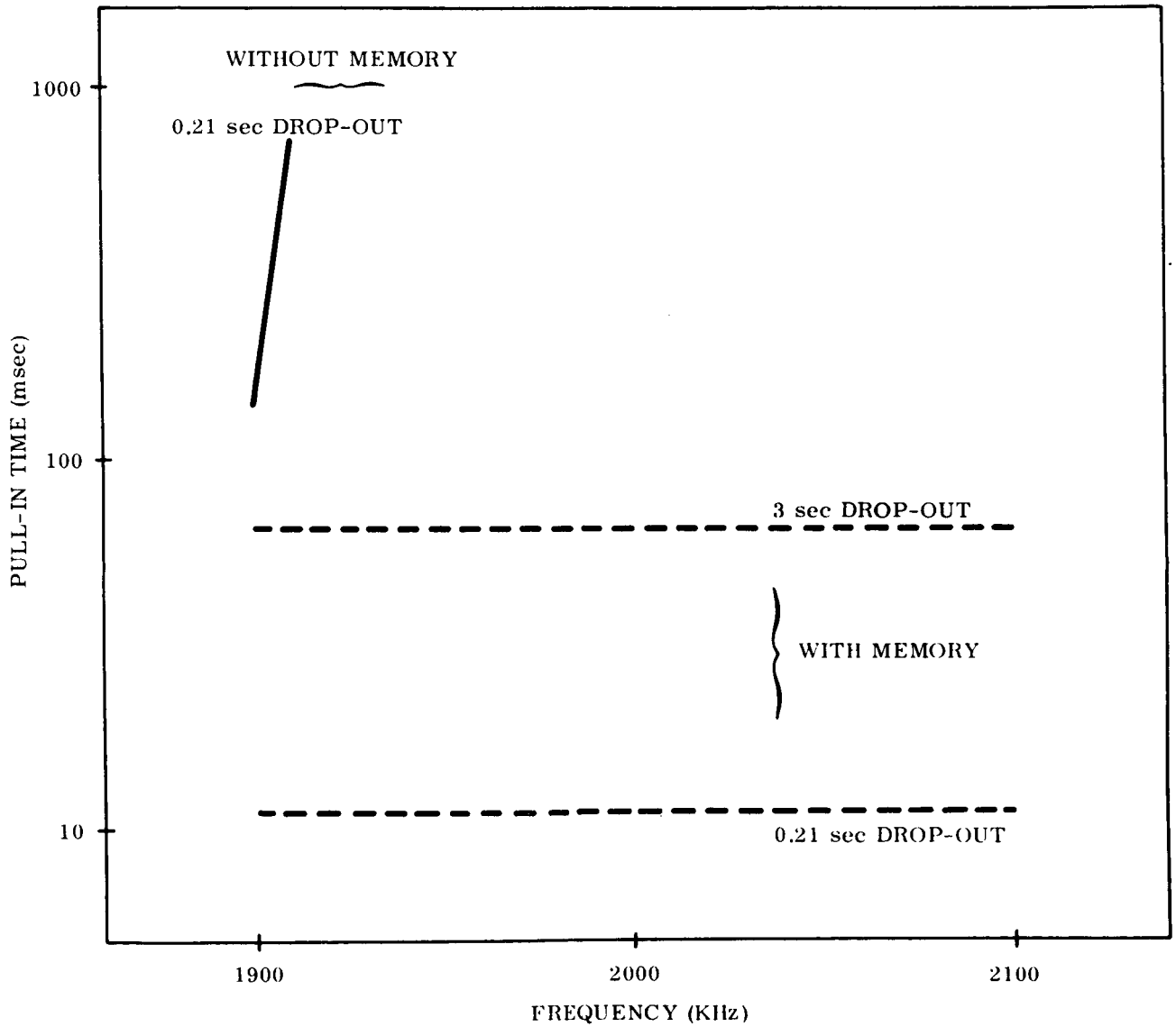


Figure 1–15. Reacquisition of a Faded Signal over the Tracking Range Doppler Rate = 1.7 KHz/sec, S/N Ratio = – 10 db

1.2.4.4 Reacquisition Process Performance

To observe the reacquisition process, pictures were taken of the waveform of the lock-indicator output. Simultaneously, the loop phase detector output or the signal level was displayed. For all photographs, the doppler offset was 100 kHz, with a zero doppler rate. In Figure 1-16, the reacquisition is shown for both a memory-aided (top photograph) and non-aided loop (bottom photograph). The 7 msec delay placed in the lock indicator output is clearly distinguishable, establishing a lower bound of recovery time measurement. As expected, the loop without aiding requires a longer pull-in time, while the pull-in process is visible from the beat tone which decreases in frequency as the loop pulls in.

The photographs Figure 1-17, display the same waveforms. For these pictures, the signal-to-noise ratio was reduced to 0 db, which results in an increase in phase noise present in the loop phase detector output, and the dropout time was increased, causing a longer reacquisition time for the non-aided loop. The display time is therefore increased to 100 msec/div. The memory-aided loop acquires immediately, while the non-aided loop requires quite a number of beat-tone cycles at reducing frequency before lock is achieved. In Figure 1-18, dropout time is further increased to 2.0 sec, with an accompanying increase in display time. While no visible delay is present in the acquisition of the memory-aided loop, the non-aided loop requires about 1.3 secs to lock. Since the signal interrupter is running freely, its period is observable as about 6.7 secs. In these figures, the signal level is also monitored. Because of the intensity of the scope trace in the absence of the signal, the line photographed too thick. A separate measurement of isolation indicated a better than 60 db ratio.

1.2.5 Conclusions

A narrow band phase-locked loop tracking a signal which undergoes severe fading will have extremely limited reacquisition capabilities. This is particularly true for

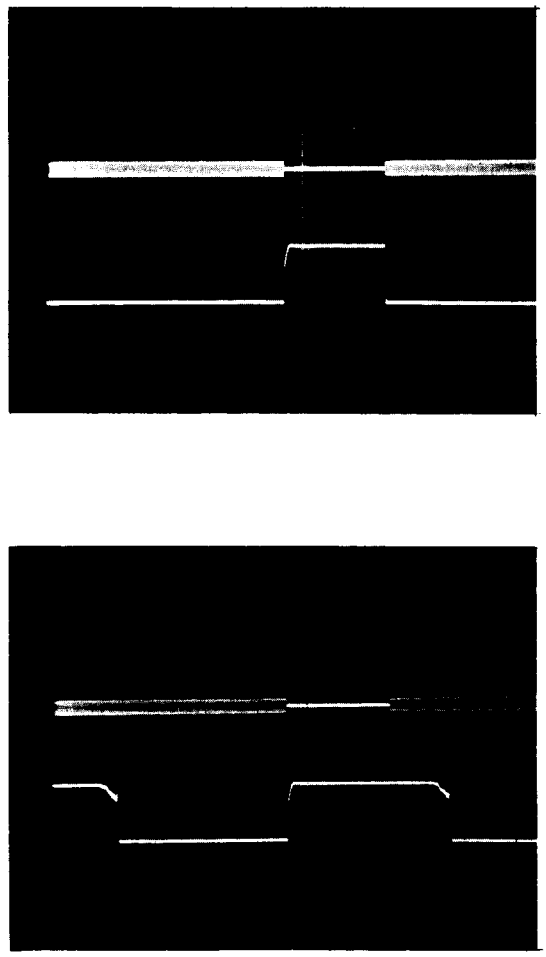


Figure 1–16. Reacquisition Behavior on Faded Signals for Memory-Aided and Non-Aided Phase-Locked Loops

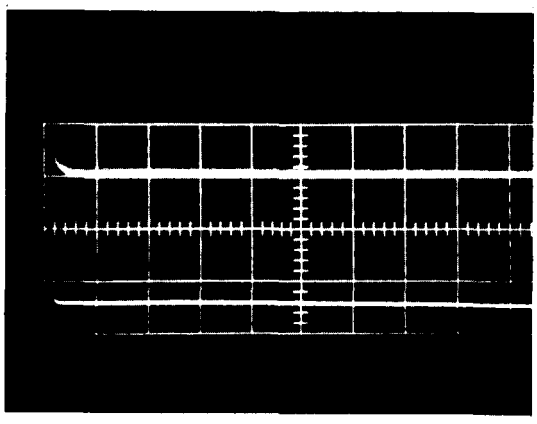


Figure 1–17. Reacquisition Behavior on Faded Signals for Memory-Aided and Non-Aided Phase-Locked Loops

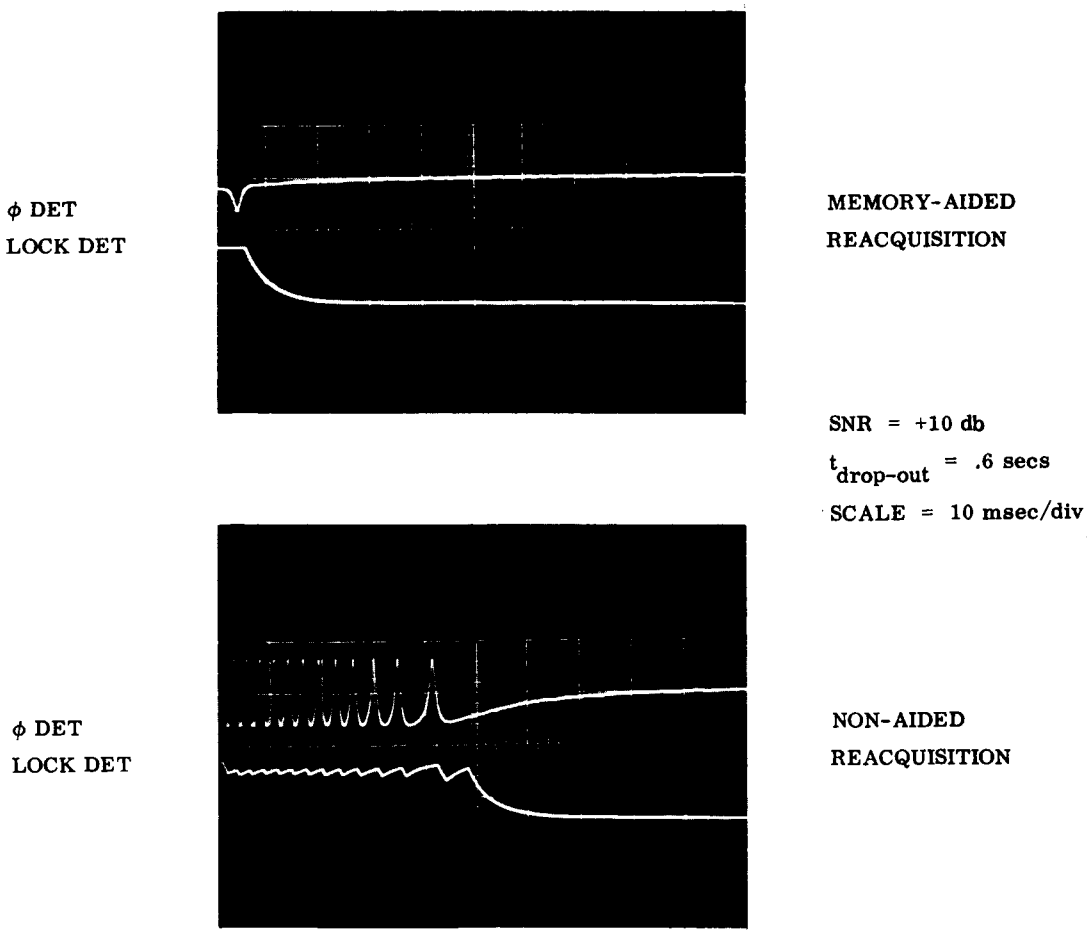


Figure 1–18. Reacquisition Behavior on Faded Signals for Memory-Aided and Non-Aided Phase-Locked Loops

signals with a high doppler rate such as encountered in the AROD System and for low signal-to-noise ratios. In most cases of signal fading, the signal will reappear outside the pull-in range of the loop and a time-consuming search cycle will be needed, resulting in a large loss of useful data.

If signal estimation is applied to the loop in the form of memory-aiding, during the fading and during reacquisition, the loop is maintained in vicinity of the signal, and the cancellation of doppler rate greatly enhances reacquisition. In the absence of a large doppler rate derivative, memory-aiding will allow a very rapid reacquisition under all signal conditions.

Section 2

TECHNICAL SUMMARY

2.1 Wideband Modulation Techniques

The wideband modulation techniques task was performed during October 1964 to April 1965. The purposes of the wideband modulation techniques task were to analyze and evaluate modulation techniques for use in the AROD System and to recommend the technique(s) most suitable for implementation. The study team investigated systems employing discrete sidetones, systems employing pure pseudo-noise (PN) signals, and hybrid systems (combining periodic signals and PN signals). This portion of the study resulted in the following conclusions as contained in the Fifth Quarterly Report.

a. A modulation system using only discrete sidetone components with a Fine Ranging Tone frequency of approximately 1 MHz can approach the AROD accuracy objectives, but such a system is too susceptible to CW interference.

b. A modulation system using only pseudo-noise (PN) sequences cannot provide satisfactory tracking accuracy for the AROD application; rather, a periodic component must be included in the modulation.

c. "Hybrid" systems combining periodic and PN signals can approach the AROD acquisition and tracking accuracy objectives and provide substantial interference rejection.

d. To approach the AROD objectives, the inherent adaptivity characteristics of phase-locked loops must be fully exploited. This requires essentially linear amplification (with no limiting) in the Tracking Receiver.

e. The slave PN generator in the Tracking Receiver must be driven by the "clean" signal available at the output of the phase-locked loop tracking the periodic component in the hybrid spectrum.

f. To achieve good dynamic range, the PN sidelobes must be suppressed by filtering. Baseband (premodulation) filtering, combined with analog (angle) modulation, appears to be the preferable approach.

g. During initial acquisition, the first step following acquisition of the (doppler-wiped-out) carrier should be the acquisition of the PN sequence. Only after this has been accomplished should the doppler be restored to the signal.

h. The Tracking Receiver should mix incoming signals with a local signal that essentially spreads an interfering sinusoid into a spectrum similar to that of pseudo-noise.

i. Proper selection of the harmonic relationship between the PN rate and the periodic component (FRT) can result in a power density spectrum that vanishes in the vicinity of the carrier.

Volume II of the Fifth Quarterly Report contains detailed mathematical analyses and derivations. These include the solution of the Range Equation, a phase-locked loop analysis showing the adaptivity of the loop with and without limiting of the input signal, derivations of the phase error caused by modulation on the input signal and errors caused by small amplitude interfering sine waves, and the spectra of a carrier angle modulated by sidetones or PN signals, or hybrid modulation waveforms.

The Sixth Quarterly Report reviews in more detail the three major conclusions concerning the wideband modulation techniques:

a. Linear amplification should be employed in the spacecraft receiver.

b. A "hybrid" modulation waveform is preferable to a pure PN waveform.

c. Common channel operation is not recommended because it would result in a very limited dynamic range.

In addition, Section 3 of the Sixth Quarterly Report presents several methods for obtaining the spectrum of signals resulting from the angle modulation of a carrier with filtered PN sequences. Results of a preliminary investigation of methods for reducing reacquisition time for PN sequences are also reported. It is shown that reacquisition of a PN-modulated carrier could be achieved in less than 1/2 second with a conventional intercept receiver.

2.2 Computer Requirements Study

During the first six months of the SASS Program, an investigation was made to define the Saturn V Guidance Computer requirements for converting range and range rate data from the AROD System into position and velocity information. The results of this study are described in Section 1 of the First Quarterly Report and Section 1 of the Second Quarterly Report.

Three methods were developed to solve the navigation equations for vehicle position. Each method requires a different amount of storage and a particular solution time using the Saturn V guidance computer. All three methods are developed in detail in Section 1 of the First Quarterly Report. The storage and computation time requirements are determined in Section 1 of the Second Quarterly Report.

The first method requires the least storage and solution time. It is a direct method which produces an analytical solution in closed form by using algebraic manipulation and solution of simultaneous equations to determine the position coordinates. This method requires 463 26-bit storage locations in the Saturn V guidance computer and requires a maximum of 81 milliseconds for execution.

The second method hypothesizes a solution to the navigation equations, tests the solution by substituting it into the original equations, and then applies differential corrections to this solution, repeatedly iterating until the solution satisfies the equations. This method requires 508 26-bit storage locations and requires 98 milliseconds for execution if the original guess is correct. It requires 140 milliseconds if the second guess is correct, and an additional 160 milliseconds for each further iteration.

The third method determines the position coordinates by analytic geometry. If the distances from the vehicle to each of the three ground stations are known, the position is one of the two points of intersection of the three spheres centered

on the ground stations and having radii equal to the respective distances from each ground station to the vehicle. Equations are solved for the intersections. 540 26-bit storage locations are required for this method with a computation time of 120 milliseconds. The computer requirements for these three methods of determining position are summarized in Table 2-1.

Determination of vehicle velocity requires an additional 110 26-bit storage locations and 31 milliseconds processing time, regardless of which of the three methods is used. This requirement is also given in Table 2-1.

Additional processing time is required for auxiliary computations which primarily include converting "raw" AROD data to range and range-rate data, testing validity of the data, and correcting range and range-rate data for propagation effects. A discussion of propagation errors is given in Appendix B of the AROD "Design Feasibility Report," Volume II. The range and range-rate corrections can be either stored in tabulated form and retrieved by table lookup, or the corrections can be computed directly from analytical expressions involving range, height, and other relevant parameters. The table lookup approach requires more storage than the computational approach, but the table lookup approach requires less computation time since less calculation is required. The optimum correction procedure uses the table lookup approach but utilizes the knowledge of the nature of the data in this correction table to reduce the storage requirements at a small expense in computation time. This procedure requires 257 storage locations and 7 milliseconds of computation time.

Table 2-1 summarizes the basic storage and computation time requirements. A final estimate on the totals (including auxiliary computations not included in the table) indicates that 1500 ± 750 storage locations will be required and the computation time will be 150 ± 50 milliseconds.

Table 2–1. AROD Storage and Computation Time Requirements Using the Saturn V Guidance Computer

	← Position Computations →					
	By Direct Method	By Differential Correction Method	By Analytic Geometry Method	Velocity Computation	Propagation Corrections Computation	Totals (Using Direct Method)
Storage Required (Number of 26-bit words)	463	508	540	107	257	827
Computation Time Required	81 millisec. maximum	98 millisec. first solution; 140 millisec. second solution; +160 millisec. per additional iteration	120 millisec. maximum	31 millisec.	7 millisec.	119 millisec.

2.3 AROD System Interface Investigations

As mentioned in the previous subsection, the Saturn V Guidance Computer (SVGC) is required by the AROD System, primarily to convert "raw" AROD data to range and range-rate information, to test the validity of this information, to correct the range and range-rate information for propagation effects, and to solve the navigation equations for vehicle position and velocity. In addition, the computer transmits command and control data back to the AROD System. This control data includes selection of the transponders to be used and also contains acquisition aid information. Since the computer is also used by other Saturn systems, the computer must be time-shared for the AROD application. The Saturn V Data Adapter (DA) is designed to accept data from several different systems for processing by the computer, and it provides the control and sequencing of input and output between these systems and the computer.

A complete discussion of the AROD System/Guidance Computer interface appears in Section 1.3 of the First Quarterly Report, Section 2 of the Second Quarterly Report, and in Section 1 of the Third Quarterly Report. This information is summarized in Figure 2-1, which is the recommended configuration for sending AROD sensor output data to the Data Adapter, and in Figure 2-2, which is the recommended configuration for sending command and control data from the computer to the AROD System.

2.4 Geometrical Dilution of Precision (GDOP)

AROD position and velocity errors are highly dependent on the location of the ground transponders and the accuracy with which the positions of the transponders are known. The AROD error evaluation computer program was designed to evaluate quantitatively the effects of vehicle-to-ground transponder geometry on AROD errors. Appendix A of the AROD Design Feasibility Report gives

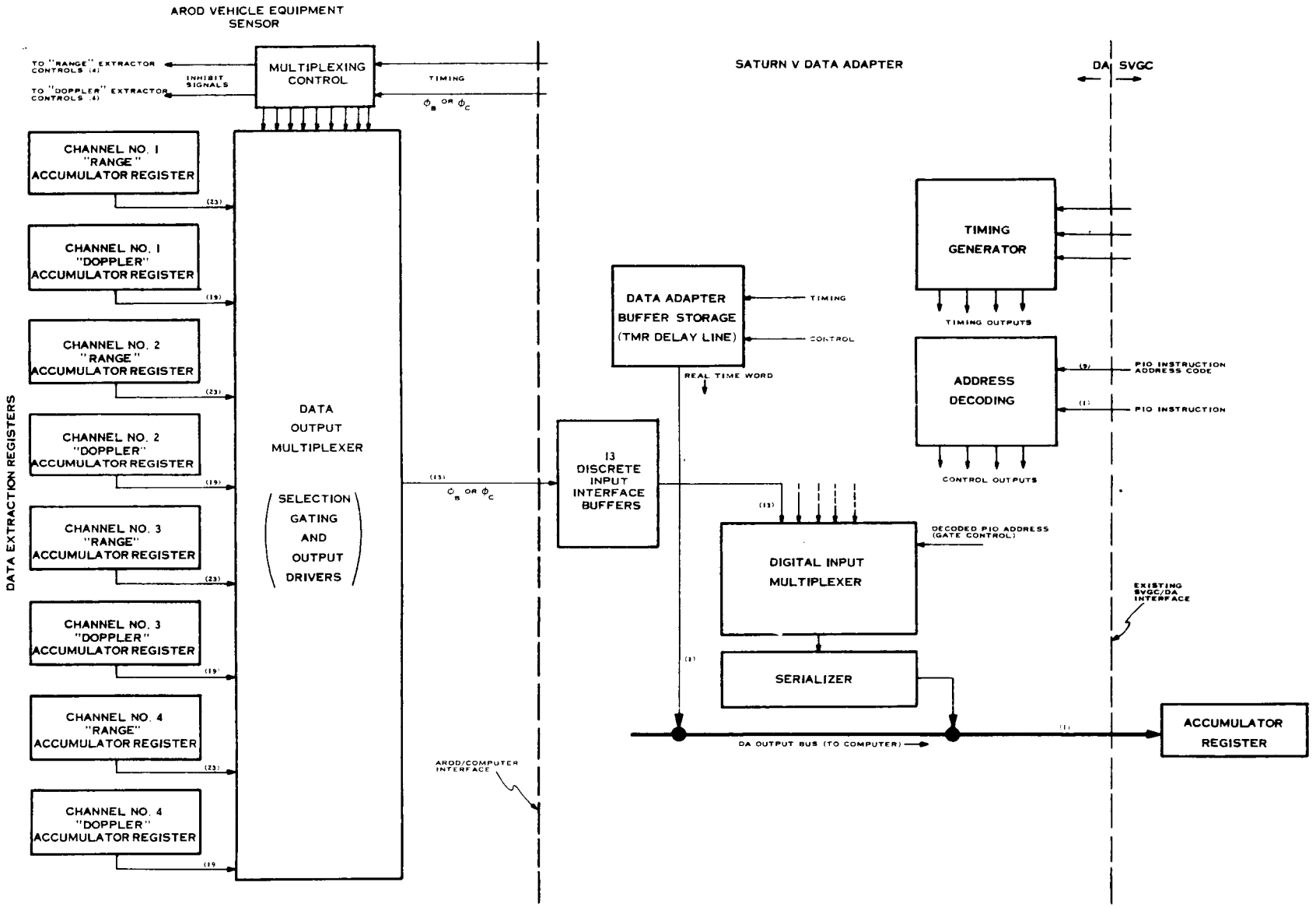


Figure 2–1. Recommended Configuration for Sending AROD Sensor Output Data to the Saturn V Guidance Computer

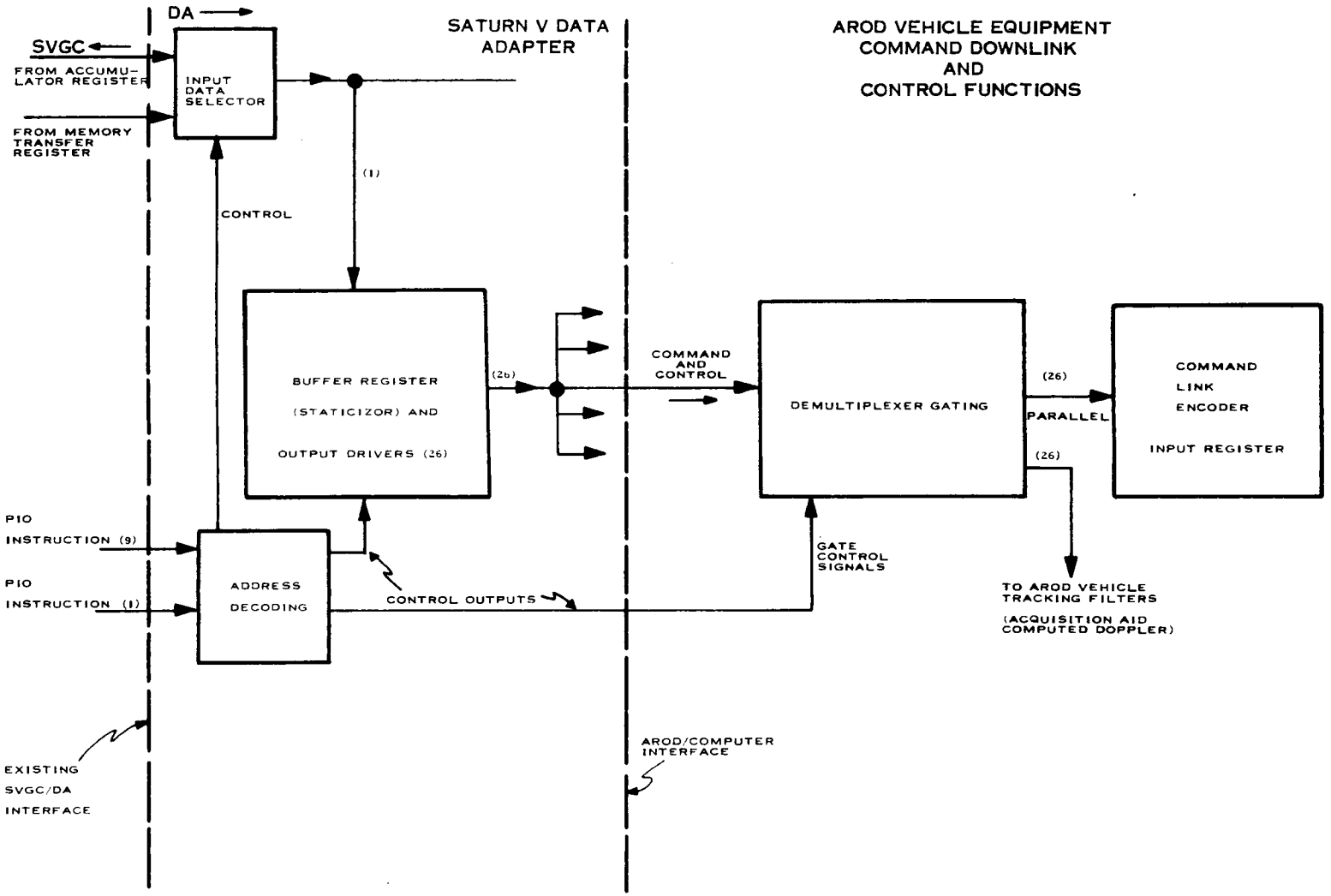


Figure 2–2. Recommended Configuration for Sending Command and Control Data from the Saturn V Guidance Computer to the AROD System

a description of the computer program and summarizes the results of several computer runs made to determine the AROD System accuracy as a function of transponder configuration and separation and of uncertainty in the position of the ground transponders. The results of additional runs using typical Saturn trajectories representing the launch phase and translunar phase of a lunar mission are reported in Section 1. 2 of the First Quarterly Report and Section 3 of the Second Quarterly Report.

As a result of these runs, several conclusions were made:

a. At least four oceanborne transponders will be required in addition to land-based transponders to provide continuous coverage of AMR launch trajectories (from essentially lift-off to orbital insertion) without gross geometrical distortions.

b. Position and velocity errors in the AROD System are essentially proportional to error or uncertainty in the positions of the ground transponders if oceanborne transponder configurations are used.

c. For oceanborne configurations, baselines greater than 800 kilometers should be employed whenever permitted by coverage requirements.

d. In the presence of oceanborne transponder position errors greater than 30 meters, only small changes in system performance result from large improvements in AROD range and range-rate measurement accuracies. It may be appropriate, therefore, to use relatively simplified transponders for the oceanborne installations since greater equipment errors will be more tolerable in these cases.

e. An all-Bermuda based AROD transponder triad is competitive (on a system accuracy basis) with a large-baseline oceanborne triad only if error or uncertainty in the position of the oceanborne transponders is greater than 100 meters.

f. Error or uncertainty in the altitude of oceanborne transponders is smaller than error or uncertainty in latitude and longitude and produces a correspondingly small effect on net AROD System errors.

g. Early coverage of AMR launch trajectories, using all land-based transponders, is both possible and desirable. To minimize GDOP effects, the larger baseline configurations should be used whenever permitted by coverage requirements.

The results of these studies indicate that both the launch phase and the translunar phase of a lunar mission are well within the capabilities of the AROD System.

2. 5 Oceanborne Transponders

As mentioned previously, maximum AROD System accuracy can only result if the positions of the ground transponders are known with high accuracy. For oceanborne transponders, this presents several problems since it is necessary to determine accurately the position of each oceanborne transponder, to stabilize the position of the transponders, and to provide unmanned operation with at least six months between servicing periods.

Section 2 of the First Quarterly Report and Section 4 of the Second Quarterly Report consider several alternate approaches to these problems. The recommended approach, described in Section 4. 3 of the Second Quarterly Report, uses a triply-moored lightweight buoy to use the high accuracy of trilateration systems. The lines are stretched under high tension at relative angles of 90 degrees so that each line is constrained from horizontal and upward movement perpendicular to its axis by the other two, and from downward perpendicular movement by the increased share of buoyant force such movement would incur. To maximize the tension-to-drag ratio, very high tensile strength wire, such as piano wire (320,000 psi) is used. The tension is made a large fraction of the ultimate (breaking) strength so that wave action and other changing forces on the buoy and wires create only minor fluctuations in the wire tension. Figure 2-3 shows the geometry of the lightweight buoy with its three moorings.

The triply moored lightweight buoy has several advantages over other approaches:

a. The approach is more economical than other possible methods.

b. The buoy does not require active stabilization; the mooring can maintain the position of the buoy within 30 feet.

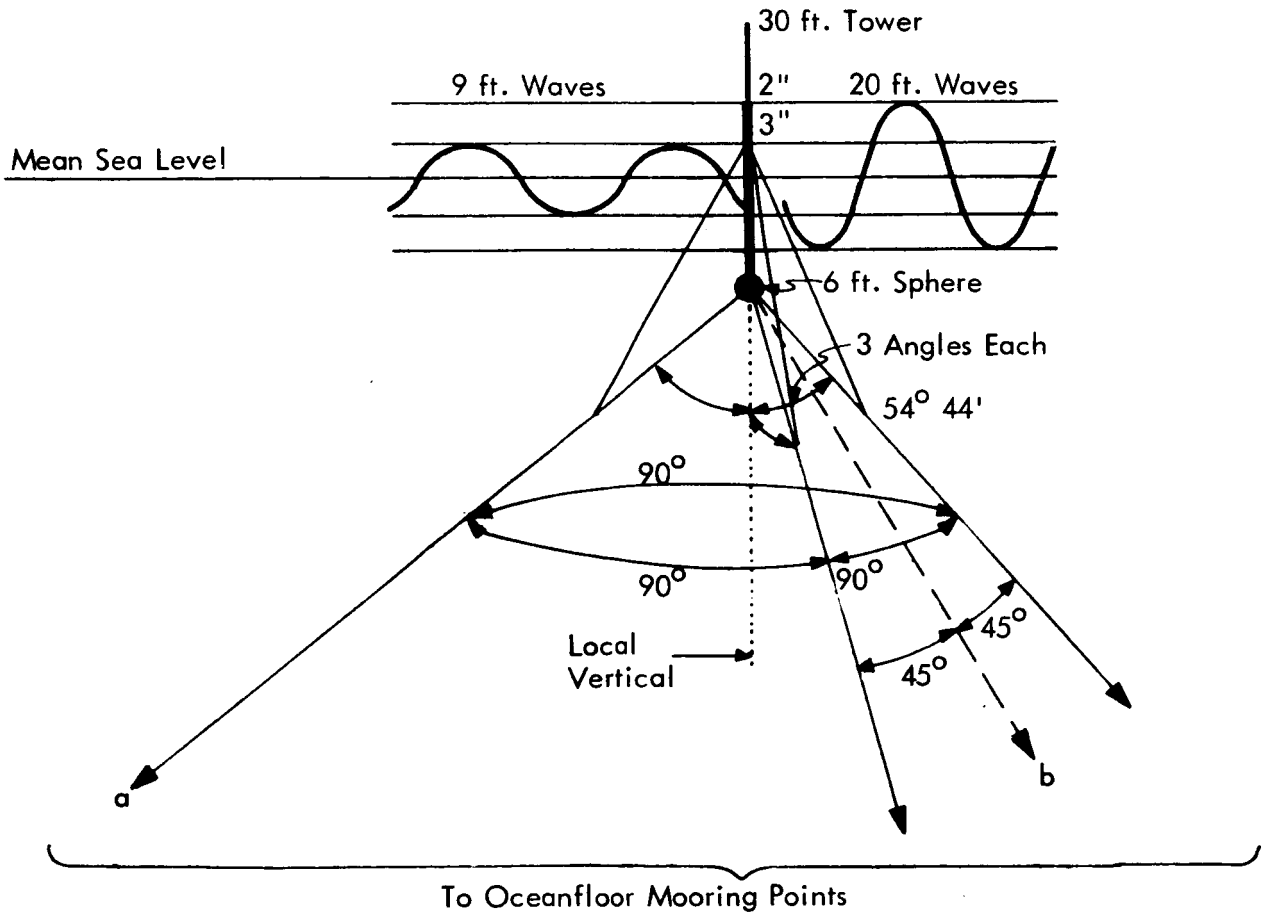


Figure 2–3. Triply Moored-Lightweight Buoy

c. Orientation of the transponder antenna can be maintained to within 2 degrees of the vertical. This is desirable to reduce undesirable multipath effects.

Other principal conclusions of this investigation, reported in Section 4 of the Second Quarterly Report, are:

a. The buoy should be held in position by three mutually perpendicular mooring lines, each of which is step-tapered and made of high strength piano wire.

b. To simplify accurate installation of the buoy, a sonar transponder should be mounted on each mooring line anchor.

c. Further knowledge of the ocean environment at selected mooring sites is necessary before a more exact error and transient analysis of the position of the buoy can be made.

d. The bulk of the weight associated with the buoy will be Leclanche carbon-zinc batteries for transponder operation.

To establish design feasibility of this recommended approach, a detailed hydrodynamic analysis should be performed. In addition, a suitable installation technique must be evolved. After these steps are taken, physical models of the buoy should be tested to optimize the design.

2. 6 Linearized Transponder Transmitter Chain

A six-week investigation was conducted by the Maxson Electronics Corporation to determine if linear amplifier performance capabilities at microwave frequencies are satisfactory for effective SSB operation of an AROD ground station transponder transmitter. For the transponder single-sideband up-transmission spectrum, it is required that all spurious outputs and intermodulation products must be at least 30 db down relative to the principal spectral components of the transmission.

The final report of the Maxson investigation containing a detailed description of the linear amplifier tests is given in Section 2 of the Fourth Quarterly Report.

A simulated two-tone test was performed on an L band cavity tetrode amplifier. For reasons of component availability, the work was carried out at L band rather than S band. The intermodulation products of the two test signals were measured, and envelope feedback, a technique used around a wideband loop to linearize a cavity amplifier, was employed to determine if significant reduction in the level of the intermodulation products could be achieved. The frequencies of the test tones were 1160 and and 1162. 3 MHz and the amplitudes were sufficient to generate 10 watts PEP out of the amplifier.

An RCA J1618 coaxial cavity, designed for the RCA 7651 pulse tetrode, was used in the amplifier. The 7650 tube, a CW version of the 7651 designed for class AB amplifier service, was later used in these tests when it became evident that third order intermodulation components of the 7651 could not be reduced below the 15 to 20 db region. The grid characteristic curves for the 7650 and the 7651 were plotted so that the optimum operating region could be selected for each tube. Both tubes gave a maximum gain of 6 db.

Representative performance data for the open-loop amplifier compared to the amplifier with envelope feedback are listed in Table 2-2. Typical waveforms that have been observed are shown in Figure 2-4. Figure 2-4a is the envelope of the input (reference) waveform. Figure 2-4b is the envelope of the output waveform without feedback added to the amplifier. Figure 2-4c is the open-loop error signal, and Figure 2-4d is the waveform with the loop gain adjusted for minimum third order intermodulation components. The instrumentation did not permit observations of the effect of the feedback loop on the output envelope under closed-loop conditions.

The work performed pointed up some of the technical difficulties that must be overcome before applying a negative feedback loop to linearize an amplifier. The bandpass of the RF amplifier must be wide compared with the frequency separation of the two tones to minimize differential phase delay through the

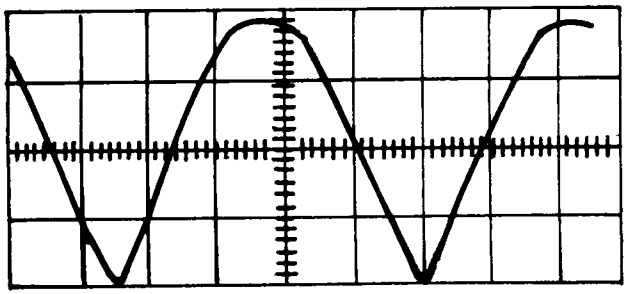
Table 2–2. Performance Data – Basic Power Amplifier Compared to Same Amplifier with Envelope Feedback

Two Tone Test
Tube Type: 7650 in RCA J1618 cavity

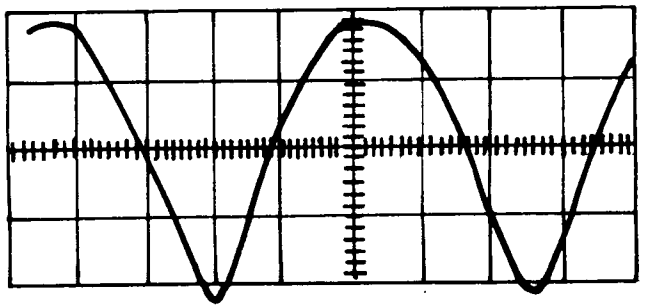
f_1 = 1160 MHz
f_2 = 1162.3 MHz

E_{bb} = 2,000 volts
e_{c2} = 300 volts

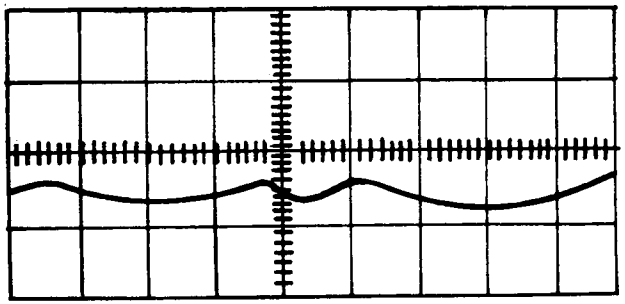
	3rd Order Intermodulation Distortion (with respect to level of f_1 or f_2)				5th Order Intermodulation Distortion (with respect to level of f_1 or f_2)			
	← $2f_2-f_1$ →		← $2f_1-f_2$ →		← $3f_2-2f_1$ →		← $3f_1-2f_2$ →	
Tube Operating Conditions	Open Loop	With Feedback	Open Loop	With Feedback	Open Loop	With Feedback	Open Loop	With Feedback
Large Bias High Input Power	-21db	-28db	-20db	-24db	-34db	-38db	-36db	-33db
Low Bias High Input Power	-26	-29	-22	-26	-38	-34	-38	-38
Low Bias Low Input Power	-31	(negligible)	-27	(negligible)	-50	(negligible)	-44	(negligible)



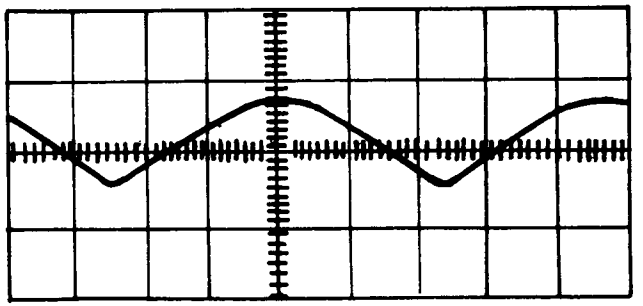
a. REFERENCE ENVELOPE



b. OUTPUT ENVELOPE



c. OPEN-LOOP ERROR SIGNAL



d. CLOSED-LOOP ERROR FOR MINIMUM INTERMODULATION

NOTE: Sweep = 0.1μsec/CM

Figure 2–4. Waveforms Showing Amplifier Linearity

amplifier. The input and output signals must be compared from a common d-c base level and the feedback amplifier must be capable of passing the d-c level.

Working within these limitations, the feedback was able to provide a 5 db reduction in the third order intermodulation distortion at open-loop levels of -20 to -25 db. If the amplifier bandwidth were wider and a common d-c base level were used, significant improvements in performance should be possible.

The envelope feedback techniques can be readily applied to S band amplifiers, of which there are several available commercially. At S band, amplifiers with greater bandwidth can be realized, thus reducing the differential phase delay through the amplifier.

The conclusions of this study indicate that it should be possible to obtain an S band amplifier having sufficient linearity for effective SSB operation of an AROD ground station transponder transmitter.