DOCUMENT 68-25299E
VOLUME 1 OF 3

Prepared For................

CALIFORNIA INSTITUTE OF TECHNOLOGY
JET PROPULSION LABORATORY
PASADENA, CALIFORNIA

FINAL REPORT

MARINER "C" DSIF EQUIVALENT GROUND SUPPORT EQUIPMENT

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WF-3006-1
15 August 1964

MARINER "C"
DSIF EQUIVALENT
GROUND SUPPORT EQUIPMENT
(Contract No. 950879)

VOLUME 1

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68-25299E

VOLUME 1

TABLE OF CONTENTS

Section		Page
1.	INTRODUCTION	1-1
1.1	Scope of Report	1-1
2.	DESCRIPTION OF EQUIPMENT	2-1
2.1	General	2-1
2.1.1	Physical Description	2-1
2.2	GSE Rack	2-1
2.2.1	Circuit Breaker Panel 1A1	2-4
2.2.2	Telemetry Narrow Band Subsystem 1A2	2-4
2.2.3	Telemetry Wide Band Subsystem 1A3	2-7
2.2.4	Test Receiver	2-10
2.2.5	Frequency Converter 1A8	2-15
2.2.6	Test Transmitter 1A9	2-17
2.2.7	Ranging Conversion Unit 1A10	2-21
2.2.8	Power Meter 1A10	2-21
2.2.9	±15 Volt Power Supply 1A11	2-22
2.2.10	±28 Volt Power Supply 1A12	2-23
3.	THEORY OF OPERATION	3-1
3.1	General	3-1
3.2	Summary of Operation	3-1
3.3	Telemetry Narrow Band Subsystem 1A2	3-3
3.3.1	Telemetry Bandpass Filter 1A2A1	3-3
3.3.2	Narrow Band 10 MC IF Amplifier 1A2A2	3-4
3.3.3	10 MC Phase Detector 1A2A3	3-4
3.3.4	Video Amplifier 1A2A4	3-5
3.3.5	10 MC Phase Shifter 1A2A5	3-5
3.4	Telemetry Wide Band Subsystem 1A3	3-5
3.4.1	Telemetry Bandpass Filter 1A3A1	3-6
3.4.2	Wide Band 10 MC IF Amplifier 1A3A2	3-6
3.4.3	10.02 MC Mixer-Oscillator 1A3A3	3-6
3.4.4	10-30 MC Converter 1A3A4	3-7
3.5	Test Receiver	3-7
3.5.1	Automatic Phase Control (APC) Loop	3-8
3.5.2	Automatic Gain Control (AGC) Loop	3-11
3.5.3	Calibrated Variable Attenuator 1A7AT1	3-12
3.5.4	Cavity Preselector, 1A7Z1	3-12
3.5.5	Local Oscillator Filter Cavities 1A7Z2 and Z3	3-13
3.5.6	Mixer, S-Band 1A7A1	3-13
3.5.7	50 MC IF Amplifier and Mixer 1A7A2	3-13
3.5.8	10 MC Distribution Amplifier 1A7A3	3-14
3.5.9	10 MC IF Amplifier 1A7A4	3-14
3.5.10	Loop 10 MC Phase Detector (AGC) 1A5A4	3-15

TABLE OF CONTENTS (Cont)

Section		Page
3.5.11	Loop 10 MC Phase Detector (APC) 1A5A2	3-15
3.5.12	10 MC Phase Shifter 1A5A3	3-16
3.5.13	X½ Frequency Multiplier 1A4A2	3-16
3.5.14	20 MC Oscillator and X3 Multiplier 1A4A1	3-17
3.5.15	Loop Filter (APC) 1A6A2	3-17
3.5.16	5-Channel VCO Assembly 1A6A1	3-18
3.5.17	X3 Frequency Multiplier Assembly 1A4A5	3-19
3.5.18	X32 Frequency Multiplier 1A4A4	3-19
3.5.19	AGC Amplifier and Filter Assembly 1A5A1	3-20
3.6	Frequency Converter 1A8	3-21
3.6.1	5-Channel Oscillator 1A8A1	3-21
3.6.2	Mixer-Filter 1A8A2	3-21
3.7	Test Transmitter 1A9	3-22
3.7.1	5-Channel Voltage-Controlled Oscillator (VCO) 1A9A1	3-22
3.7.2	X3 Multiplier and Phase Modulator 1A9A2	3-22
3.7.3	X32 Frequency Multiplier 1A9A3	3-23
3.7.4	VCO Bias Assembly	3-24
3.7.5	Calibration and Monitoring	3-24
3.7.6	Calibration Curves	3-25
3.7.7	Rear Panel RF Output	3-25
3.7.8	Power Monitor Output	3-26
3.7.9	Filtering and Shielding	3-26
3.8	Ranging Conversion Unit 1A10	3-27
3.8.1	10 MC Phase Shifter 1A10A1	3-27
3.8.2	10 MC Phase Switch 1A10A2	3-27
3.8.3	10 MC Balanced Detector 1A10A3	3-27
4.	DRAWER AND ASSEMBLY ALIGNMENT AND CHECKOUT PROCEDURES	4-1
4.1	General	4-1
4.2	Telementry Narrow Band Subsystem 1A2, Alignment	4-1
4.2.1	Test Equipment Required	4-1
4.2.2	Alignment	4-1
4.2.3	Test Requirements	4-2
4.3	Telemetry Bandpass Filter 1A2A1, Alignment	4-2
4.4	Narrow Band 10 MC IF Amplifier 1A2A2, Alignment	4-2
4.5	10 MC Phase Detector 1A2A3, Alignment	4-3
4.6	Video Amplifier 1A2A4, Alignment	4-3
4.7	10 MC Phase Shifter 1A2A5, Alignment	4-3
4.8	Telemetry Wide Band Subsystem 1A3, Alignment	4-3
4.8.1	Test Equipment Required	4-3
4.8.2	Alignment	4-3
4.8.3	Test Requirements	4-3

VOLUME 1

TABLE OF CONTENTS (Cont)

Section		Page
4.9	Telemetry Bandpass Filter 1A3A1, Alignment	4-5
4.10	10.02 MC Mixer-Oscillator 1A3A2, Alignment	4-5
4.11	Wide Band 10 MC IF Amplifier 1A3A3, Alignment	4-5
4.12	Test Receiver Drawers 1A4 Through 1A7, Alignment	4-5
	4.12.1 Test Equipment Required	4-5
	4.12.2 Initial Alignment	4-6
	4.12.3 Test Requirements	4-6
4.13	20 MC Oscillator and X3 Multiplier 1A4A1, Alignment	4-10
4.14	X½ Frequency Multiplier 1A4A2, Alignment	4-10
4.15	10 MC Isolation and Distribution Amplifier 1A4A3, Alignment	4-10
4.16	X32 Frequency Multiplier 1A4A4, Alignment	4-10
4.17	X3 Frequency Multiplier 1A4A5, Alignment	4-10
4.18	AGC Amplifier and Filter 1A5A1, Alignment	4-10
4.19	10 MC Phase Detector 1A5A2, Alignment	4-10
4.20	10 MC Phase Shifter 1A5A3, Alignment	4-11
4.21	10 MC Phase Detector 1A5A4, Alignment	4-11
4.22	5-Channel Receiver VCO 1A6A1, Alignment	4-11
4.23	Loop Filter 1A6A2, Alignment	4-11
4.24	Balanced Mixer-Preamplifier 1A7A1, Alignment	4-11
4.25	50 MC IF Amplifier and Second Mixer 1A7A2, Alignment	4-11
4.26	10 MC IF Distribution Amplifier 1A7A3, Alignment	4-11
4.27	10 MC IF Amplifier 1A7A4, Alignment	4-11
4.28	Frequency Converter 1A8, Alignment	4-12
	4.28.1 Test Equipment Required	4-12
	4.28.2 Alignment	4-12
	4.28.3 Test Requirements	4-13
4.29	5-Channel Oscillator 1A8A1, Alignment	4-14
4.30	Mixer-Filter 1A8A2, Alignment	4-14
4.31	Test Transmitter 1A9, Alignment	4-14
	4.31.1 Test Equipment Required	4-14
	4.31.2 Initial Alignment of Power Supplies	4-15
	4.31.3 Test Requirements	4-15
4.32	5-Channel Transmitter VCO 1A9A1, Alignment	4-19
4.33	X3 Multiplier and Phase Modulator 1A9A2, Alignment	4-19
4.34	X32 Frequency Multiplier 1A9A3, Alignment	4-19
4.35	Ranging Conversion Unit 1A10, Alignment	4-19
4.36	10 MC Phase Shifter 1A10A1, Alignment	4-19
4.37	10 MC Phase Switch 1A10A2, Alignment	4-19
4.38	10 MC Balanced Detector 1A10A3, Alignment	4-20

TABLE OF CONTENTS (Cont)

Section		Page
5.	DEVELOPMENTAL TECHNICAL IMPROVEMENTS, PROBLEMS, AND RECOMMENDATIONS	5-1
5.1	General	5-1
5.2	Telemetry Narrow Band Subsystem 1A2	5-1
5.3	Test Receiver, 1A4, 1A5, 1A6, and 1A7	5-1
5.3.1	In-Lock Indicator	5-1
5.3.2	Loop Filter Time Constants	5-1
5.3.3	Loop Filter Switching Transients	5-1
5.4	Test Transmitter, 1A9	5-2
6.	DIAGRAMS	6-1
6.1	General	6-1
6.2	Index of Drawings	6-1

VOLUME 1

LIST OF ILLUSTRATIONS

Figure		Page
2-1	Mariner C DSIF Equivalent Ground Support Equipment, Front View	2-2
2-2	Mariner C DSIF Equivalent Ground Support Equipment, Rear View	2-3
2-3	Circuit Breaker Panel 1A1, Top View	2-5
2-4	Telemetry Narrow Band Subsystem 1A2, Top View	2-6
2-5	Telemetry Wide Band Subsystem 1A3, Top View	2-8
2-6	Test Receiver, Part One (1A4), Top View	2-12
2-7	Test Receiver, Part Two (1A5), Top View	2-12
2-8	Test Receiver, Part Three (1A6), Top View	2-13
2-9	Test Receiver, Part Four (1A7), Top View	2-13
2-10	Frequency Converter 1A8, Top View	2-16
2-11	Test Transmitter 1A9, Top View	2-18
2-12	Test Transmitter 1A9, Bottom View	2-18
2-13	Ranging Conversion Unit 1A10, Top View	2-22
3-1	Mariner "C" Equivalent GSE, Simplified Block Diagram	3-2
4-1	Typical VCO Linearity Curve for Test Receiver	4-8
4-2	Typical VCO Linearity Curve for Test Transmitter	4-17
4-3	Test Transmitter, Test Setup	4-18
6-1	GSE, Over-all Block Diagram	6-5
6-2	GSE, Power Interconnection Diagram	6-7
6-3	GSE, Signal Interconnection Diagram	6-9
6-4	Circuit Breaker Panel (1A1), Schematic Diagram	6-11
6-5	Telemetry Narrow Band Subsystem (1A2), Schematic Diagram	6-13
6-6	Telemetry Bandpass Filter (1A2A1 and 1A3A1), Schematic Diagram	6-15
6-7	Narrow Band 10 MC IF Amplifier (1A2A2), Schematic Diagram	6-17
6-8	10 MC Phase Detector (1A2A3), Schematic Diagram	6-19
6-9	Video Amplifier (1A2A4), Schematic Diagram	6-21
6-10	10 MC Phase Shifter (1A2A5, 1A5A3, and 1A10A1), Schematic Diagram	6-23
6-11	Telemetry Wide Band Subsystem (1A3), Schematic Diagram	6-25
6-12	Wide Band 10 MC IF Amplifier (1A3A2), Schematic Diagram	6-27
6-13	10.02 MC Mixer-Oscillator (1A3A3), Schematic Diagram	6-29
6-14	Test Receiver, Interconnection Diagram	6-31
6-15	Test Receiver, Part One (1A4), Schematic Diagram	6-33
6-16	20 MC Oscillator and X3 Multiplier (1A4A1), Schematic Diagram	6-35
6-17	X½ Frequency Multiplier (1A4A2), Schematic Diagram	6-37
6-18	10 MC Isolation and Distribution Amplifier (1A4A3), Schematic Diagram	6-39
6-19	X32 Frequency Multiplier (1A4A4 and 1A9A4), Schematic Diagram	6-41
6-20	X3 Frequency Multiplier (1A4A5), Schematic Diagram	6-43
6-21	Test Receiver, Part Two (1A5), Schematic Diagram	6-45
6-22	AGC Amplifier and Filter (1A5A1), Schematic Diagram	6-47

LIST OF ILLUSTRATIONS (Cont)

Figure		Page
6-23	10 MC Phase Detector (1A5A2 and 1A5A4), Schematic Diagram . . .	6-49
6-24	Test Receiver, Part Three (1A6), Schematic Diagram	6-51
6-25	5-Channel VCO (1A6A1 and 1A9A1), Schematic Diagram	6-53
6-26	Loop Filter (1A6A2), Schematic Diagram	6-55
6-27	Test Receiver, Part Four (1A7), Schematic Diagram	6-57
6-28	Balanced Mixer-Preamplifier (1A7A1), Schematic Diagram	6-59
6-29	50 MC IF Amplifier and Second Mixer (1A7A2), Schematic Diagram .	6-61
6-30	10 MC Distribution Amplifier (1A7A3), Schematic Diagram	6-63
6-31	10 MC IF Amplifier (1A7A4), Schematic Diagram	6-65
6-32	Frequency Converter (1A8), Schematic Diagram	6-67
6-33	5-Channel Oscillator (1A8A1), Schematic Diagram	6-69
6-34	Mixer-Filter (1A8A2), Schematic Diagram	6-71
6-35	Test Transmitter (1A9), Schematic Diagram	6-73
6-36	X3 Multiplier and Phase Modulator (1A9A2), Schematic Diagram . .	6-75
6-37	Ranging Conversion Unit (1A10), Schematic Diagram	6-77
6-38	10 MC Phase Switch (1A10A2), Schematic Diagram	6-79
6-39	10 MC Balanced Detector (1A10A3), Schematic Diagram	6-81

VOLUME 1

LIST OF TABLES

Number		Page
II-1	GSE Rack (Serial No. 1 and Serial No. 2) Assemblies	2-1
II-2	Telemetry Narrow Band Subsystem Assemblies	2-6
II-3	Telemetry Wide Band Subsystem Assemblies	2-9
II-4	Test Receiver Frequencies	2-10
II-5	Test Receiver Assemblies	2-11
II-6	Frequency Converter Assemblies	2-16
II-7	Frequency Converter Frequencies	2-16
II-8	Test Transmitter Assemblies	2-19
II-9	Test Transmitter Frequencies	2-19
II-10	Ranging Conversion Unit Assemblies	2-21
III-1	Attenuator Dial Spacing in Degrees Per DB	3-25
IV-1	GSE List of Diagrams	6-1

VOLUME 1

SECTION I

INTRODUCTION

1.1 SCOPE OF REPORT

This document is a final report on the Mariner "C" DSIF Equivalent Ground Support Equipment, Part Numbers 01-25243E (Serial No. 1) and 01-25286E (Serial No. 2), designed and manufactured by Motorola Inc. for the Jet Propulsion Laboratory under Contract No. 950879. The report is composed of (1) a detailed description of the system and subassemblies, (2) theory of operation, (3) test setups and procedures including detailed alignment procedures with tolerances, (4) the results of developmental investigations, and (5) schematics, block diagrams, and other pertinent data. Standard assembly test procedures outlined in Section IV of this volume are referenced to the proper test procedures bound in Volume 2 and Volume 3.

Under the authority of Contract NAS7-100 and JPL Contract 950879, and in response to JPL Specification No. MGC-50252-DSN-A, Motorola has provided the design, fabrication, assembly, and test of the Ground Support Equipment (hereinafter referred to as the GSE) consisting of a narrow-band, automatic phase-tracking receiver, a stable variable phase-modulated transmitter, a frequency converter, a ranging conversion unit to be used with a ranging subsystem, two telemetry subsystems, and modified commercial equipment. This test set is based on utilization of DSIF RF Subsystem modules as used in the DSIF ground equipment. The GSE is used for the checkout of the S-Band Communications Subsystem of the Mariner C Spacecraft. Two GSE test sets (Serial No. 1 and Serial No. 2) were delivered to the Jet Propulsion Laboratory under this program. The contract was authorized by JPL on March 25, 1964 and equipment was delivered in the months of July and August 1964. One additional Test Transmitter drawer and two power supplies were delivered to JPL in the month of August 1964.

VOLUME 1

SECTION II

DESCRIPTION OF EQUIPMENT

2.1 GENERAL

The GSE, shown in figure 2-1, is designed to utilize DSIF RF Subsystem modules as used in the DSIF ground equipment and is capable of performing the following four functions on the S-Band Communication Subsystem of the Mariner "C" Spacecraft.

1. Provides a stable transmitter signal for checking the spacecraft receiver performance.

2. Provides a phase-locked loop receiver for checking the spacecraft receiver and transmitter characteristics.

3. Provides a means of coherently detecting and utilizing the pseudo-random ranging modulation on the spacecraft transmitter output signal.

4. Provides a means to detect and amplify telemetry signals present on the spacecraft transmitter output signal.

2.1.1 Physical Description

The GSE (see figure 2-1) consists of two standard rack enclosures, GSE, Serial No. 1 and GSE, Serial No. 2. GSE, Serial No. 1 contains the same equipment as GSE, Serial No. 2, except for drawer 1A10. Drawer 1A10 is a Ranging Conversion Unit in Serial No. 1 and a Power Meter in Serial No. 2. The rack enclosures are 71½ inches high. The rack enclosures are designed to mount standard 19-inch wide panel drawers. Each drawer, except the Power Meter 1A10, may be removed from the slide-rails for servicing. Each drawer is secured to the rack enclosure in the closed position by screws through the front panels. Handles are provided on the front panel for opening and closing the drawers when the screws have been removed. Cooling for the rack enclosures is provided by a fan that is mounted in the rear door. The combination of the fan and fins (located on the top panel of the cabinet) provides an internal positive pressure cooling system. Both rack enclosures operate from 115 vac, 60 cps, power. Each rack enclosure assembly is described in paragraph 2.2. Figure 2-2 is a rear view of the GSE.

2.2 GSE RACK

The two separate racks contain the equipment listed in table II-1.

TABLE II-1. GSE RACK (SERIAL NO. 1 AND SERIAL NO. 2) ASSEMBLIES

Unit No.	Title	Part No.	Manufacturer
1	GSE Rack, Serial No. 1	01-25243E	Motorola
1	GSE Rack, Serial No. 2	01-25286E	Motorola
1A1	Circuit Breaker Panel	01-25244E	Motorola
1A2	Telemetry Narrow Band Subsystem	01-25245E	Motorola
1A3	Telemetry Wide Band Subsystem	01-25246E	Motorola

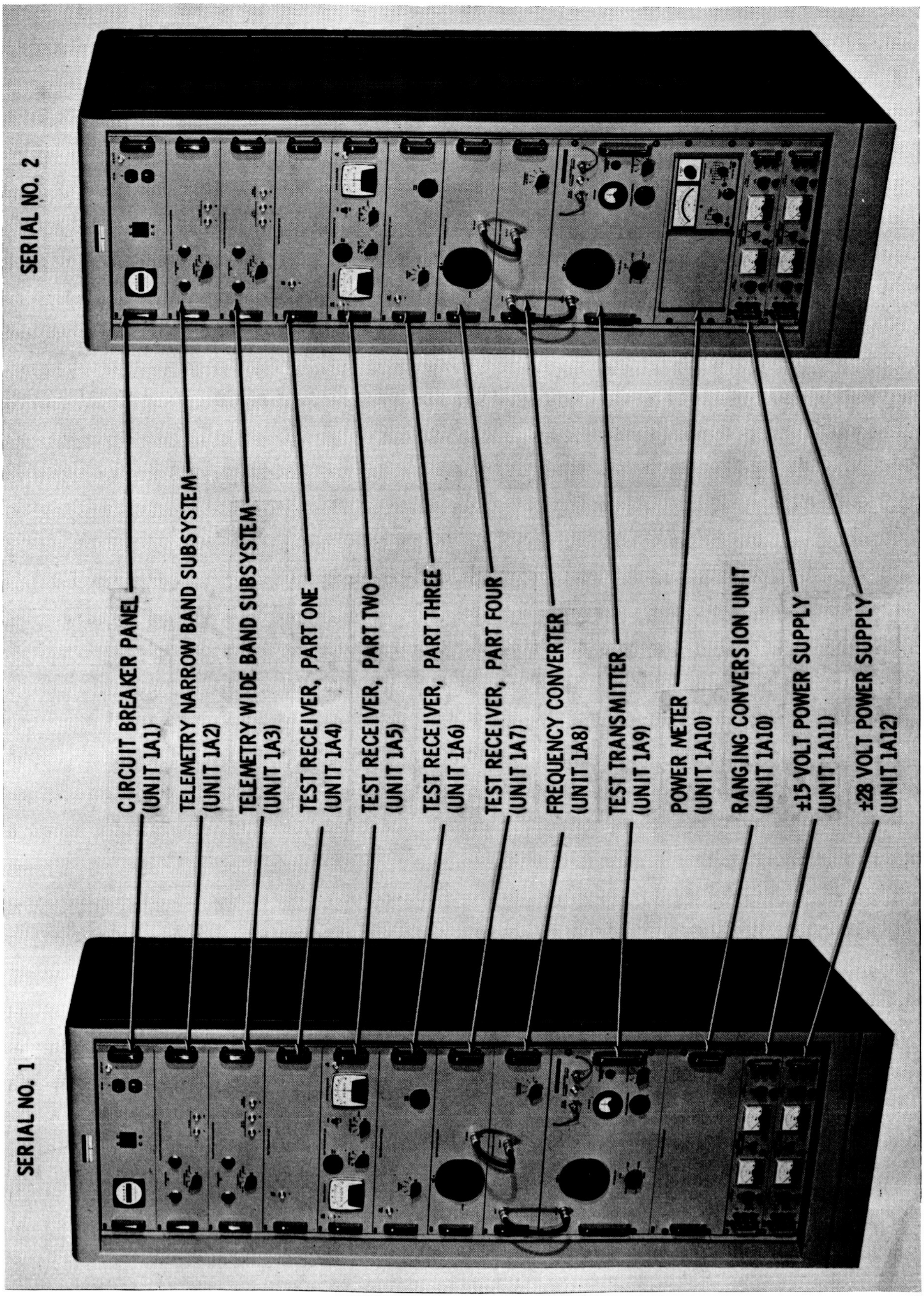


Figure 2-1. Mariner C DSIF Equivalent Ground Support Equipment, Front View

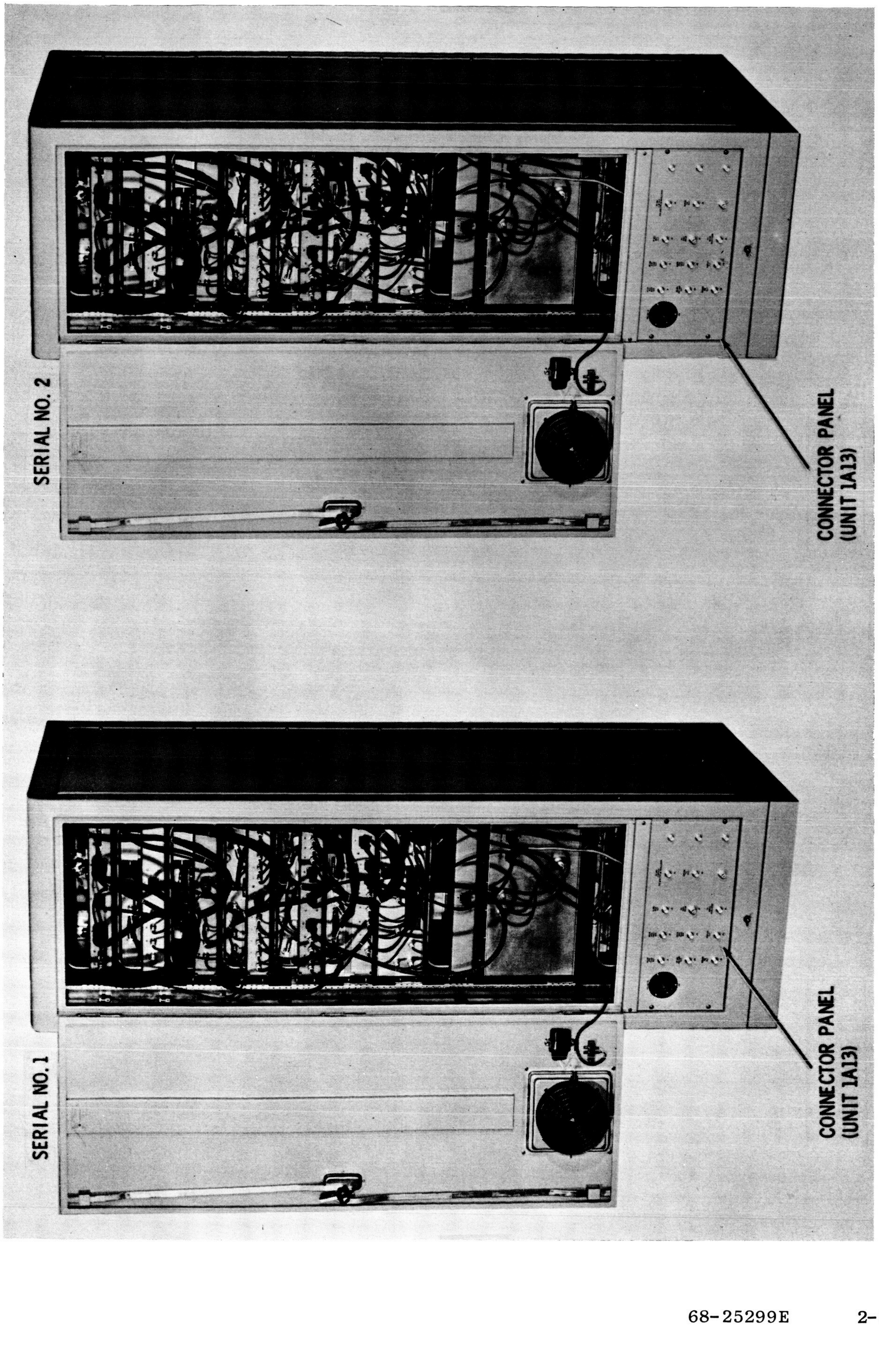


Figure 2-2. Mariner C DSIF Equivalent Ground Support Equipment, Rear View

TABLE II-1. GSE RACK (SERIAL NO. 1 AND SERIAL NO. 2) ASSEMBLIES(cont)

Unit No.	Title	Part No.	Manufacturer
1A4	Test Receiver, Part One	01-25247E	Motorola
1A5	Test Receiver, Part Two	01-25248E	Motorola
1A6	Test Receiver, Part Three	01-25249E	Motorola
1A7	Test Receiver, Part Four	01-25250E	Motorola
1A8	Frequency Converter	01-25251E	Motorola
1A9	Test Transmitter	01-25252E	Motorola
*1A10	Ranging Conversion Unit	01-25253E	Motorola
**1A10	Power Meter	01-25256E (HP-431B)	Hewlett-Packard
1A11	±15 Volt Power Supply	01-25254E (802B)	Harrison
1A12	±28 Volt Power Supply	01-25255E (802B)	Harrison

* GSE Serial No. 1 only

** GSE Serial No. 2 only

2.2.1 Circuit Breaker Panel 1A1

Circuit Breaker Panel 1A1 (figure 2-3) is a standard 5¼ inch high panel that contains a master power circuit breaker, running time meter, and two 115 vac convenience outlets. Also contained within this drawer are provisions for the future mounting of the Single Sideband unit, 22 mc isolation amplifier units, and the necessary coax connectors and cables.

2.2.1.1 Controls and Indicators

The function of the controls and indicators on Circuit Breaker Panel 1A1 are as follows:

Control or Indicator	Function
Circuit Breaker	Provides on-off switching and overload protection to all equipment in the GSE Rack and any equipment utilizing the front panel 115 vac outlets on the Circuit Breaker Panel.
Running Time Meter	Provides a visual indication of the accumulated total operating time for the GSE Rack.

2.2.2 Telemetry Narrow Band Subsystem 1A2

2.2.2.1 Functional Description

Telemetry Narrow Band Subsystem 1A2 is used in conjunction with the Test Receiver to produce the following three characteristics:

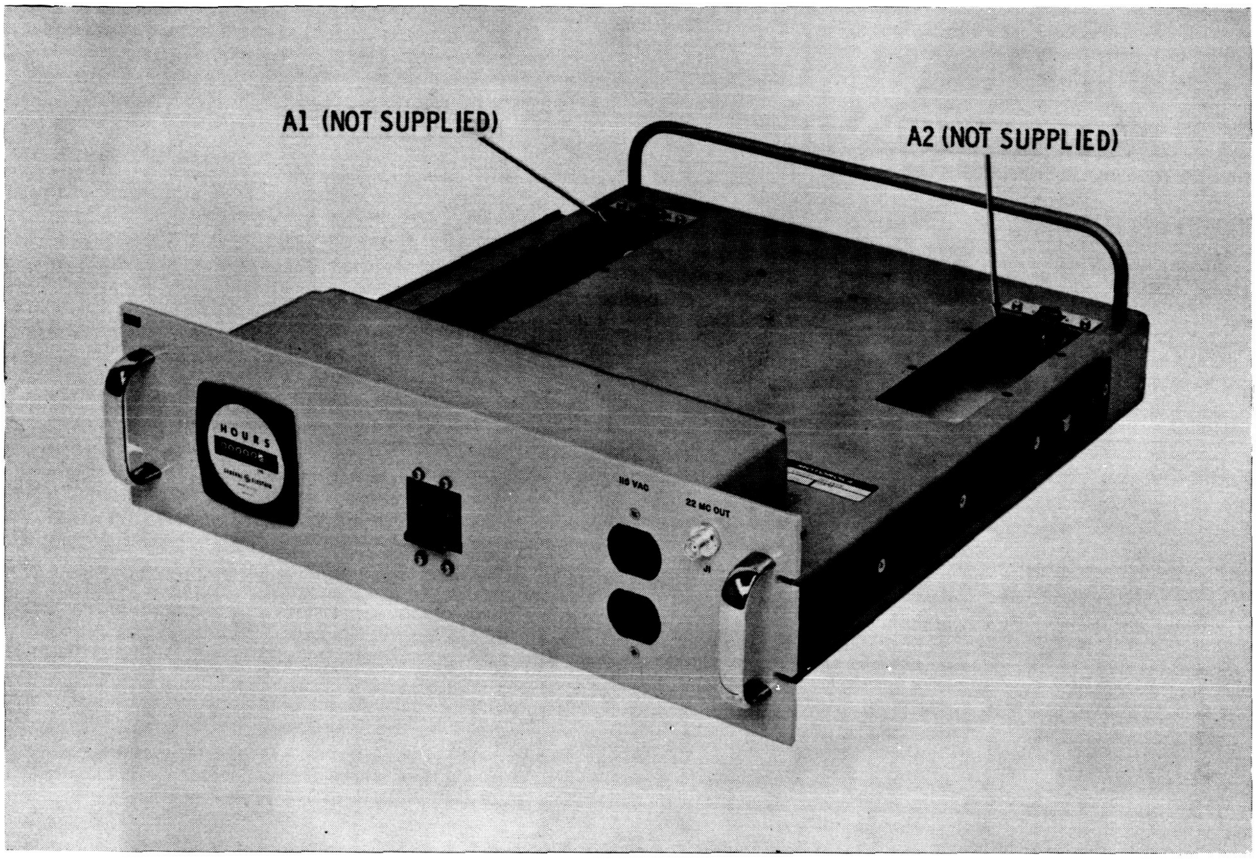


Figure 2-3. Circuit Breaker Panel 1A1, Top View.

1. Provides demodulated telemetry signal outputs.
2. Provides selectable predetection bandwidths.
3. Provides 10 MC IF output signal for analysis of modulated telemetry information in the narrowband channel.

2.2.2.2 Physical Description

Telemetry Narrow Band Subsystem 1A2 (figure 2-4) is physically located in a slide-mounted drawer in the GSE Rack. The assembly components are housed in a standard $5\frac{1}{4}$ inch drawer. The drawer contains five major plug-in assemblies and two variable attenuators which may be removed for alignment, test, or repair. Table II-2 lists the assemblies and attenuators used in the telemetry subsystem.

Two variable attenuators, located on the front panel, allow the proper input attenuation to the Bandpass Filter assembly. Also, a BANDWIDTH switch, located on the front panel, allows the selection of one of four different bandwidths.

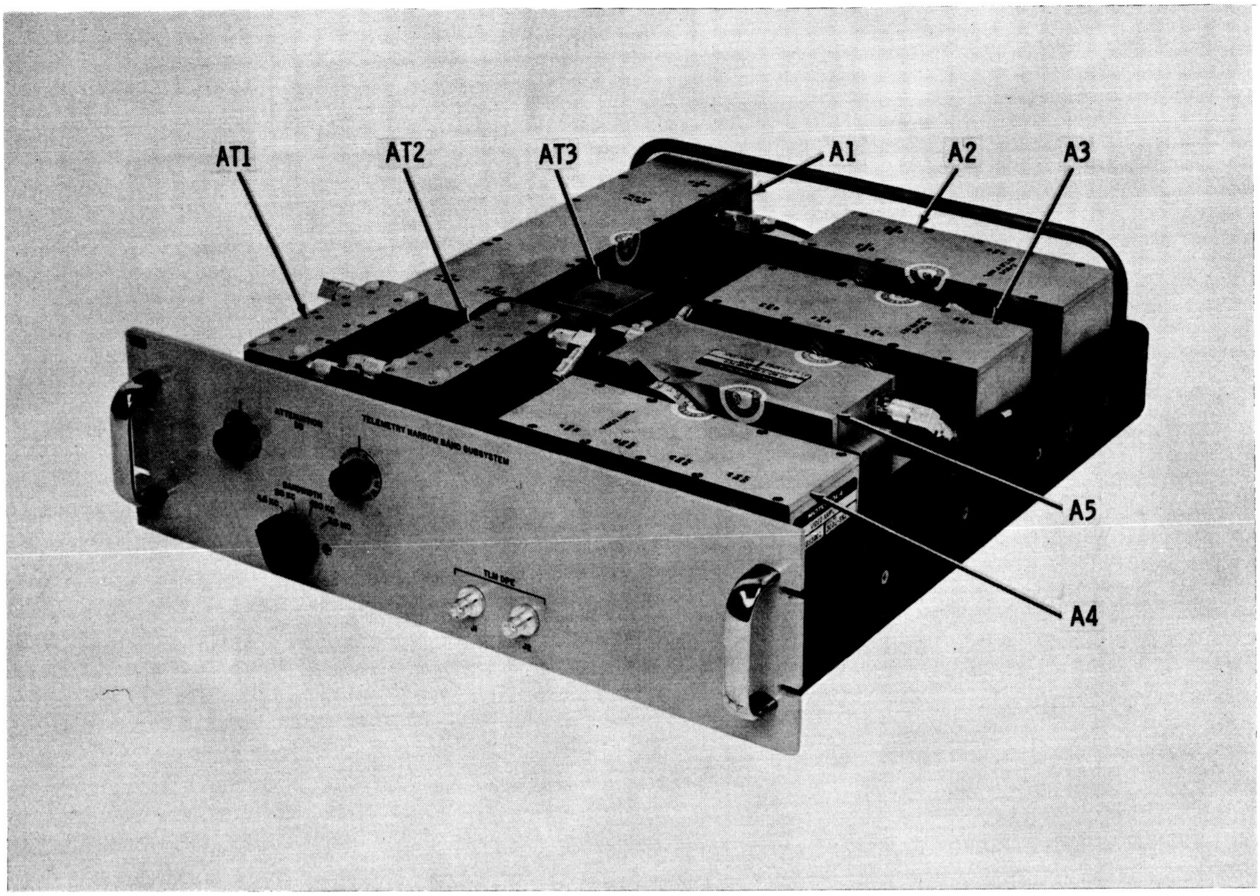


Figure 2-4. Telemetry Narrow Band Subsystem 1A2, Top View

TABLE II-2. TELEMETRY NARROW BAND SUBSYSTEM ASSEMBLIES

Unit No.	Title	Part No.	Manufacturer
1A2A1	Telemetry Bandpass Filter	01-23800D01	Motorola
1A2AT1	Variable Attenuator	HP- C05-355C	Hewlett-Packard
1A2AT2	Variable Attenuator	HP- C05-355D	Hewlett-Packard
1A2A2	Narrow band 10 MC IF Amplifier	01-24272D01	Motorola
1A2A3	10 MC Phase Detector	01-24273D01	Motorola
1A2A4	Video Amplifier	01-23853D01	Motorola
1A2A5	10 MC Phase Shifter	01-23793D01	Motorola

2.2.2.3 Technical Characteristics

The technical characteristics for the Telemetry Narrow Band Subsystem 1A2 are as follows:

Bandpass Frequencies	4.5 kc, 20 kc, 420 kc, 3.3 mc (selectable)
Narrow Band IF Input Signal	10 mc at -65 dbm
Reference Input Signal	10 mc at +10 dbm
HP-CO5-355C Variable Attenuator	
Attenuation	12 db in 1 db steps
Frequency Range	Dc to 1000 mc
Impedance	50 ohms
Power Dissipation	0.5 watt average, 350 volts peak
HP-CO5-355D Variable Attenuator	
Attenuation	120 db in 10 db steps
Frequency Range	Dc to 1000 mc
Impedance	50 ohms
Power Dissipation	0.5 watt average, 350 volts peak

2.2.2.4 Controls

The function of the controls on the Telemetry Narrow Band Subsystem 1A2 is as follows:

Control	Function
ATTENUATION DB Switches	
0-12 DB Switch (12-position rotary)	Selects 0 to 12 db attenuation in 1 db increments to provide (with the 0-120 DB attenuator) the proper signal level to the narrowband telemetry IF amplifier and Phase Detector.
0-120 DB Switch (12-position rotary)	Selects 0-120 db attenuation in 10 db increments to provide (with the 0-12 DB attenuator) the proper signal level to the narrowband telemetry IF amplifier and Phase Detector.
BANDWIDTH Switch (4-position rotary)	Selects one of the four available bandwidths as follows:
4.5 KC Position	Selects a 4.5 kc bandpass.
20 KC Position	Selects a 20 kc bandpass.
420 KC Position	Selects a 420 kc bandpass.
3.3 MC Position	Selects a 3.3 mc bandpass.

2.2.3 Telemetry Wide Band Subsystem 1A3

2.2.3.1 Functional Description

Telemetry Wide Band Subsystem 1A3 is used in conjunction with the Test Receiver to produce the following four characteristics:

1. Provides modulated telemetry signal outputs for monitoring purposes.
2. Provides selectable predetection bandwidths.
3. Provides 10 mc IF output signals for telemetering and spectral analysis.
4. Provides a 30 mc output signal to be used for spectrum analysis.

2.2.3.2 Physical Description

Telemetry Wide Band Subsystem 1A3 (figure 2-5) is physically located in a slide-mounted drawer in the GSE. The assembly components are housed in a standard $5\frac{1}{4}$ inch drawer. The drawer contains four major plug-in assemblies and two variable attenuators which may be removed for alignment, test, or repair. Table II-3 lists the assemblies and attenuators used in the drawer.

Two variable attenuators, located on the front panel, allow the proper input signal level to be applied to the wide band telemetry IF amplifier. Also, a BANDWIDTH switch, located on the front panel, allows the selection of one of four different bandwidths.

Two types of front panel outputs are provided. One at J1 and J2, is the output of the 10 mc wide band telemetry IF amplifier and the other at J3 is a 20 kc nominal output, heterodyned down from the 10 mc wide band telemetry IF amplifier, for use on an external wave analyzer.

Additionally the 20 kc output,available at the rear panel, is a 30 mc signal heterodyned up from the 10 mc IF output for use on a fixed tuned external spectrum analyzer.

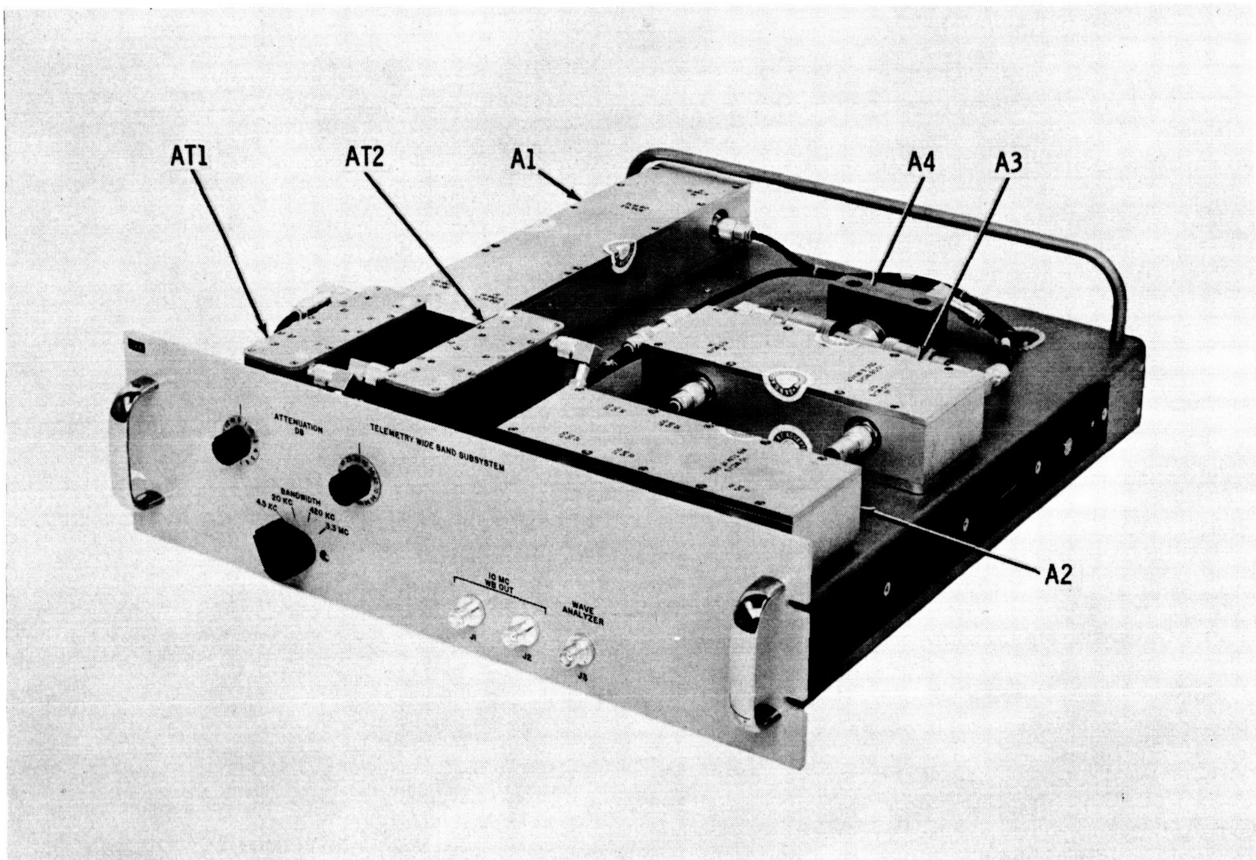


Figure 2-5. Telemetry Wide Band Subsystem 1A3, Top View

TABLE II-3. TELEMETRY WIDE BAND SUBSYSTEM ASSEMBLIES

Unit No.	Title	Part No.	Manufacturer
1A3A1	Telemetry Bandpass Filter	01-23800D01	Motorola
1A3AT1	Variable Attenuator	HP CO5-355C	Hewlett-Packard
1A3AT2	Variable Attenuator	HP CO5-355D	Hewlett-Packard
1A3A2	Wide Band 10 MC IF Amplifier	01-23795D01	Motorola
1A3A3	10.02 MC Mixer-Oscillator	01-23844D01	Motorola
1A3A4	10-30 MC Converter	874-MRL	General Radio

2.2.3.3 Technical Characteristics

The technical characteristics for the Telemetry Wide Band Subsystem 1A3 are as follows:

Bandpass Frequencies	4.5 kc, 20 kc, 420 kc, or 3.3 mc (selectable)
Wide Band IF Input Signal	10 mc at -65 dbm
HP CO5-355C Variable Attenuator	
Attenuation	12 db to 1 db steps
Frequency Range	Dc to 1000 mc
Impedance	50 ohms
Power Dissipation	0.5 watt average, 350 volts peak
HP CO5-355D Variable Attenuator	
Attenuation	120 db in 10 db steps
Frequency Range	Dc to 1000 mc
Impedance	50 ohms
Power Dissipation	0.5 watt average, 350 volts peak

2.2.3.4 Controls

The function of the controls for the Telemetry Wide Band Subsystem 1A3 is as follows:

Control	Function
ATTENUATION DB Switches	
0-12 DB Switch (12-position rotary)	Selects 0 db to 12 db attenuation in 1 db increments to permit application (with the 120 db attenuator) of the proper signal level to the wide band telemetry IF amplifier.
0-120 DB Switch (12-position rotary)	Selects 0 to 120 db attenuation in 10 db increments to permit application (with the 0 to 10 db attenuator) of the proper signal level to the wide band telemetry IF amplifier.

Control	Function
BANDWIDTH Switch (4-position rotary)	Selects one of the four available bandwidths as follows:
4.5 KC Position	Selects a 4.5 kc bandwidth.
20 KC Position	Selects a 20 kc bandwidth.
420 KC Position	Selects a 420 kc bandwidth.
3.3 MC Position	Selects a 3.3 mc bandwidth.

2.2.4 Test Receiver

2.2.4.1 Functional Description

The Test Receiver is a dual conversion phase-locked loop utilizing coherent automatic phase control and an automatic gain control system. The nominal input frequency to the Test Receiver is 2295 mc with the ability to track or be manually fine tuned ±200 kc and coarse tuned +3.7 mc by the selection of oscillator crystals within a multi-crystal oscillator or by automatic frequency tuning by the interconnection of cables between the Test Transmitter VCO output and the single sideband modulator input. See figures 6-15, 6-21, 6-24 and 6-27 for schematic diagrams of the Test Receiver. The Test Receiver is designed to provide the following information concerning the Spacecraft receiver and transmitter performance:

a. Low-frequency readout of the transmitter frequency
b. Calibrated measurement of transmitter power output (SIGNAL STRENGTH)
c. Transmitter modulation characteristics (TELEMETRY OUTPUT)
d. Incidental phase noise (DYNAMIC PHASE ERROR)
e. Transmitter modulation spectrum
f. In addition, the Test Receiver permits acquisition of a transmitter signal whose frequency differs from the nominal center frequency over the range of ±86 kc. All nominal center frequencies are listed in table II-4.

TABLE II-4. TEST RECEIVER INPUT FREQUENCY

Coarse Tune Switch Position	Test Receiver Input Frequency (MC)	VCO Crystal Frequency (MC)	VCO Frequency Control Range (CPS)
1	2295.000000	23.38542 ±1 pt in 10^6	±900
2	2297.592593	23.41242 ±1 pt in 10^6	±900
3	2297.962963	23.41628 ±1 pt in 10^6	±900
4	2298.333333	23.42014 ±1 pt in 10^6	±900
5	2298.703704	23.42400 ±1 pt in 10^6	±900

2.2.4.2 Physical Description

The Test Receiver is physically located in four separate rack-mounted drawers (1A4 through 1A7) as shown in figure 2-1. Also, Circuit Breaker Panel 1A1 (figure 2-3) contains provisions for the future mounting of the Single Sideband unit and 22 MC Isolation amplifier assembly for the Test Receiver. Each Test Receiver drawer in the GSE is a standard $5\frac{1}{4}$-inch drawer. Each drawer (see figures 2-6 through 2-9) is contained in a slide-mounted enclosure installed in the GSE Rack. The drawer can be pulled forward on the slide-rails to provide convenient access to all assemblies for servicing.

Shielded assemblies, which are listed in table II-5, compose the major portion of the Test Receiver. The use of shielded module construction aids in testing and maintenance procedures, and reduces spurious signal problems.

Five different crystal controlled input frequencies can be selected by means of a front panel control. These VCO frequencies are listed in table II-4. The Test Receiver automatically tracks or can be manually tuned by a front panel control to input signals which may vary ±86 kc within the coarse frequency range selected by the COARSE TUNE switch. A continuously variable ATTEN control is provided on the front panel for attenuating the nominal input signal. The attenuator is variable over a 100 db range with the dial calibrated in increments of 0.5 db. An AGC BW CPS switch allows the selection of three different AGC bandwidths. A LOOP BW CPS switch allows the selection of four different loop bandwidths or an open loop.

The Test Receiver operates from ±15 vdc power from Power Supply 1A11 and ±28 vdc from Power Supply 1A12.

TABLE II-5. TEST RECEIVER ASSEMBLIES

Unit No.	Title	Part No.	Manufacturer
1A1A1	Single Sideband Unit	(Not supplied by Motorola)	
1A1A2	22 MC Isolation Amplifier	(Not supplied by Motorola)	
1A4A1	20 MC Oscillator and X3 Multiplier	01-23781D01	Motorola
1A4A2	X1/2 Frequency Multiplier	01-21456C01	Motorola
1A4A3	10 MC Isolation and Distribution Amplifier	01-23778D01	Motorola
1A4A4	X32 Frequency Multiplier	01-23786D01	Motorola
1A4A5	X3 Frequency Multiplier	01-23772D01	Motorola
1A5A1	AGC Amplifier and Filter	01-23610D01	Motorola
1A5A2	AGC 10 MC Phase Detector	01-21432C01	Motorola
1A5A3	10 MC Phase Shifter	01-23793D01	Motorola
1A5A4	Loop 10 MC Phase Detector	01-21432C01	Motorola
1A6A1	5-Channel Receiver VCO	01-25260E01	* Motorola
1A6A2	Loop Filter	01-23784D01	Motorola

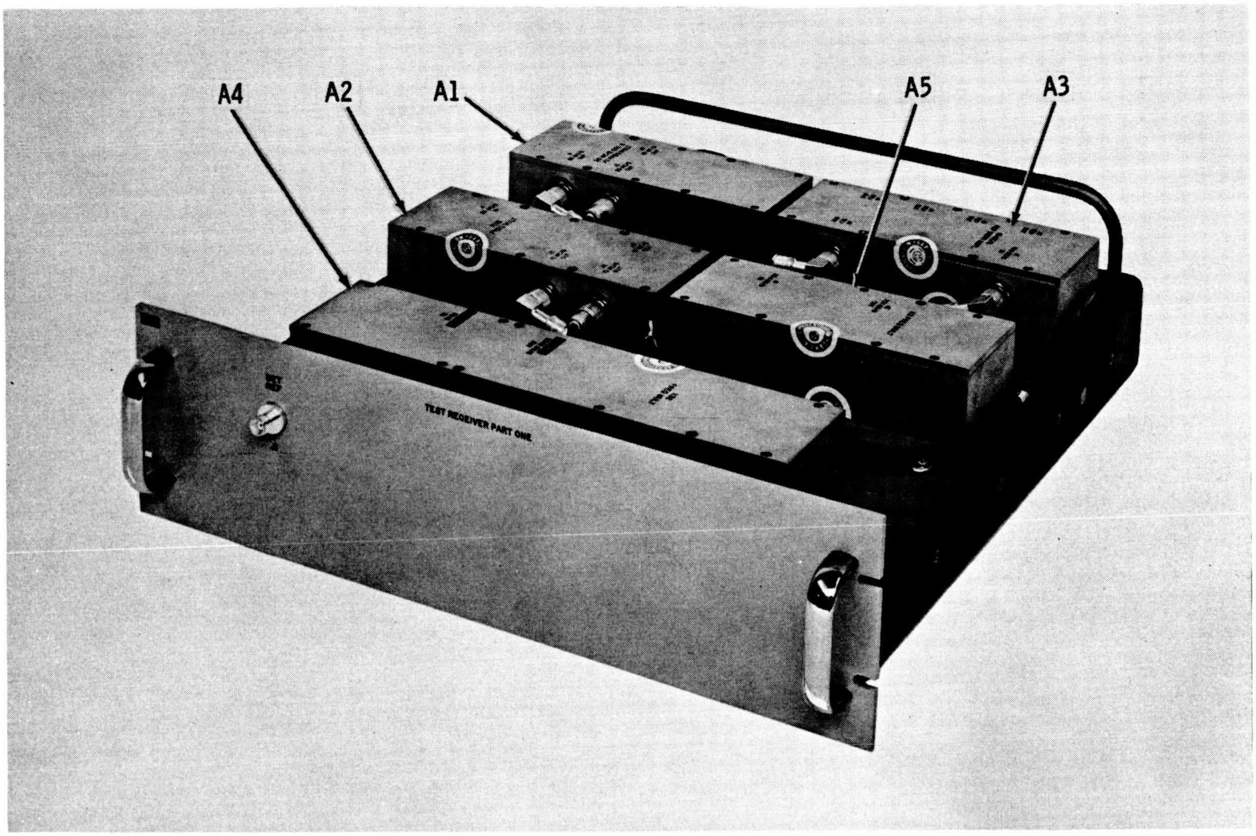


Figure 2-6. Test Receiver, Part One (1A4), Top View

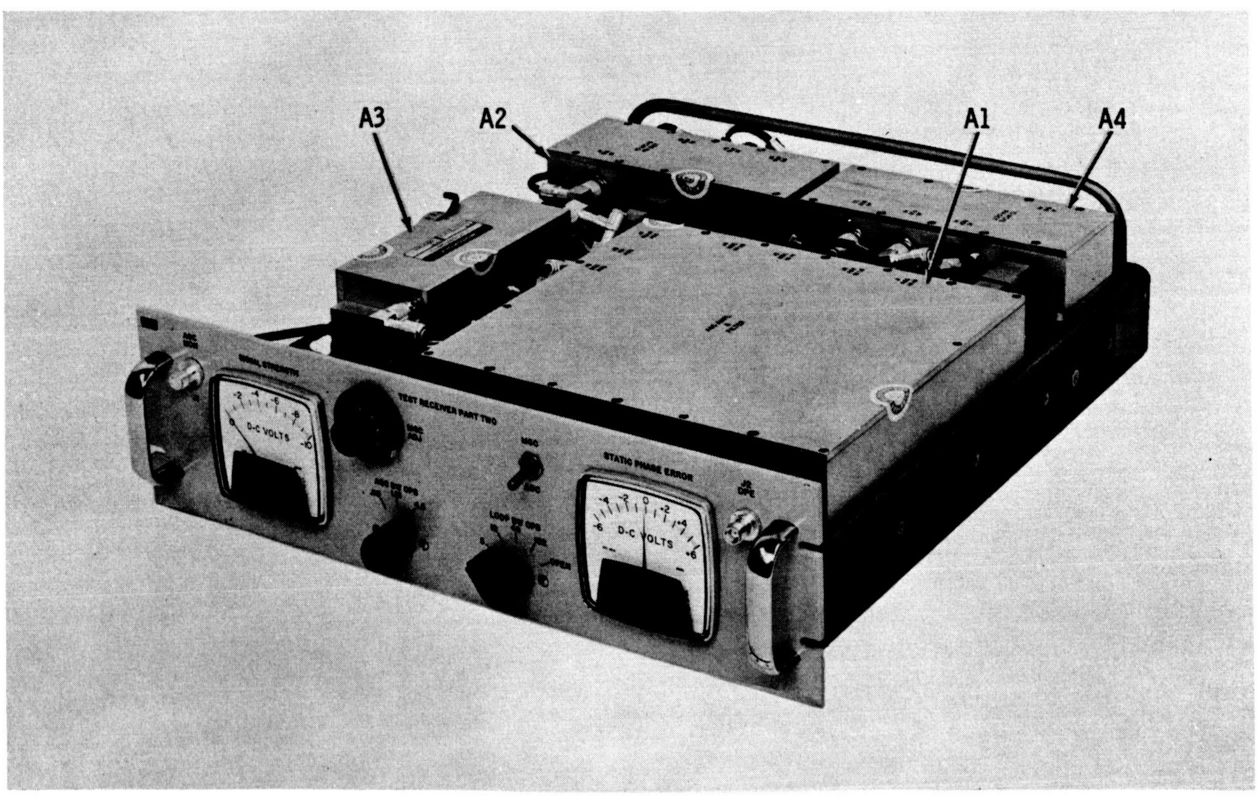


Figure 2-7. Test Receiver, Part Two (1A5), Top View

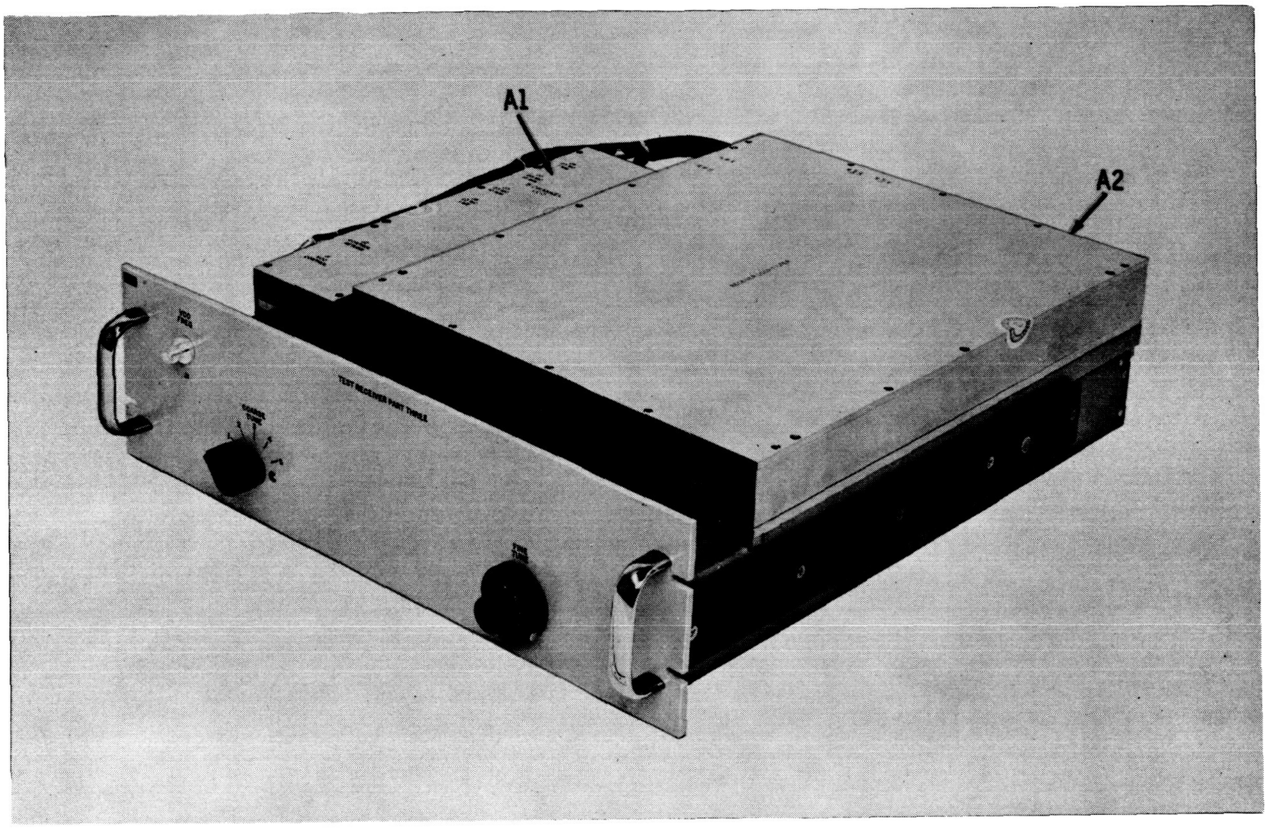


Figure 2-8. Test Receiver, Part Three (1A6), Top View

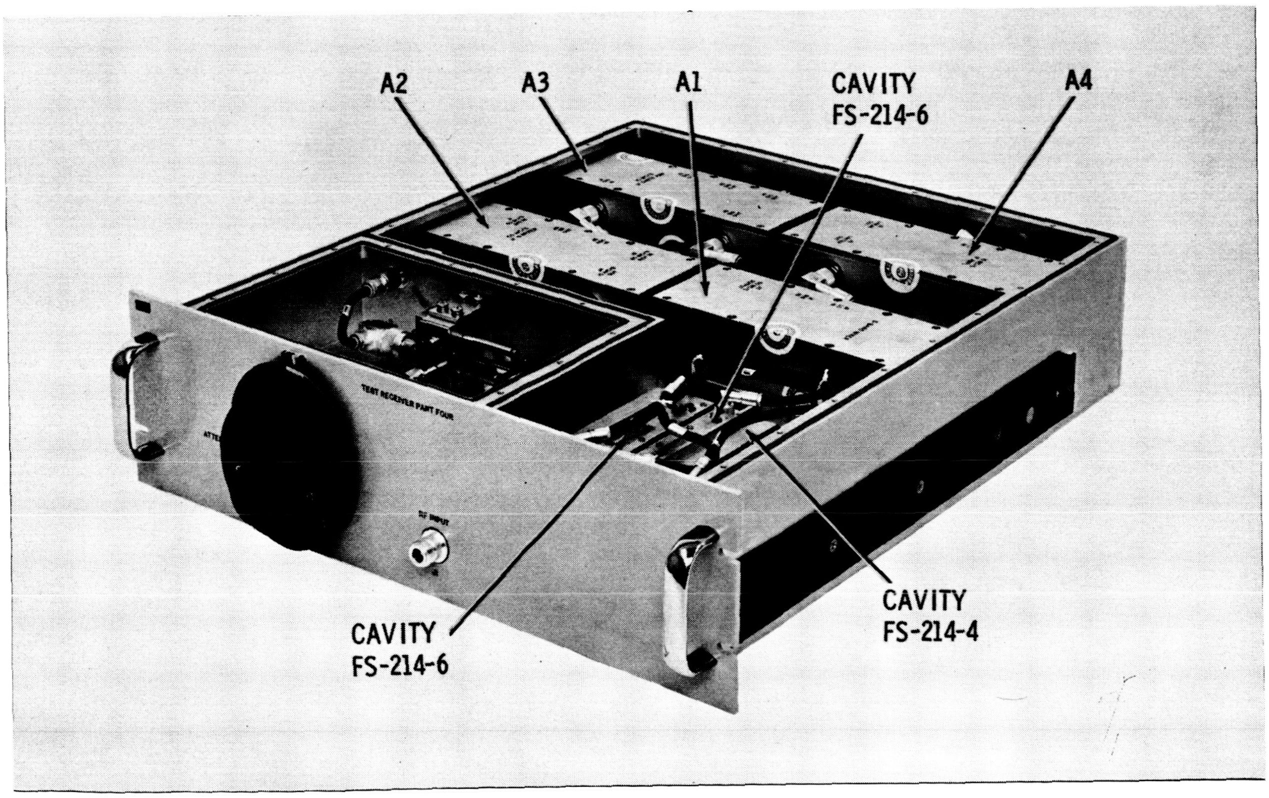


Figure 2-9. Test Receiver, Part Four (1A7), Top View
With Top Cover Plate Removed

TABLE II-5. TEST RECEIVER ASSEMBLIES (cont)

Unit No.	Title	Part No.	Manufacturer
1A7AT1	Variable Attenuator	198S	* PRD
--	Cavity	FS-214-4	* Rantek
1A7A1	Balanced Mixer-Preamplifier	01-23773D01	Motorola
1A7A2	50 MC IF Amplifier and Second Mixer	01-23774D01	Motorola
1A7A3	10 MC IF Distribution Amplifier	01-23775D01	Motorola
1A7A4	10 MC IF Amplifier	01-23776D01	Motorola
--	Cavity (two)	FS-214-6	* Rantec

All above modules except those marked with * are DSIF RF Subsystem designs.

2.2.4.3 Technical Characteristics

The technical characteristics for the Test Receiver are listed as follows:

Operating Frequency (Refer to table II-4)

Bandwidth:

Automatic Phase Control (APC) Loop 5,12,48,152 cps, or open loop (selectable)

Automatic Gain Control (AGC) Loop .118, 1.18, or 4.5 cps (selectable)

Input signal levels (threshold at 1A7J1)

5 cycle APC Loop Bandwidth -136.5 dbm

12 cycle APC Loop Bandwidth -132.7 dbm

48 cycle APC Loop Bandwidth -126.7 dbm

152 cycle APC Loop Bandwidth -121.7 dbm

NOTE: The above are typical numbers based on the following:

Threshold dbm = -174 dbm + N.F. + 10 log B + I.L.

where NF = Receiver Noise Figure

B = APC Loop Bandwidth

IL = Insertion loss of components and cables between 1A7J1 and mixer input with variable attenuator at minimum

Typical numbers are N.F. = 11.5 db, I.L. = 19 db.

Input Signal Level (max.) At least 100 db above threshold by use of variable attenuator.

Input Impedance 50 ohms

Residual Phase Modulation 5 degrees peak for a 20 cps bandwidth

Outputs 10 mc IF signal to Telemetry Wide Band Subsystem 1A3

10 mc IF signal to Telemetry Narrow Band Subsystem 1A2

10 mc IF signal to Ranging Conversion Unit 1A10

10 mc IF reference signal to Ranging Conversion Unit 1A10

2.2.4.4 Controls and Indicators

The functions of the controls and indicators for the Test Receiver are as follows.

Control or Indicator	Drawer	Function
SIGNAL STRENGTH Meter	1A5	Reads directly the AGC or MGC voltage of the test receiver.
MGC/AGC Switch (2-position toggle)		
AGC Position	1A5	Allows the system to be gain controlled automatically.
MGC Position	1A5	Allows the system to be manually gain controlled with the manual gain control.
MGC ADJ Control	1A5	Adjusts the gain of the system manually when the MGC/AGC switch is in the MGC position.
AGC BW CPS Switch (3-position rotary)	1A5	Allows selection of an AGC bandwidth of 4.5, 1.18, or .118 cps.
SPE Meter	1A5	Reads directly the static phase error.
LOOP BW CPS Switch (4-position rotary)	1A5	Allows selection of a loop bandwidth of 5, 12, 48, or 152 cps. In the OPEN position, the filter is removed and the loop is opened.
COARSE TUNE Switch (5-position rotary)	1A6	Selects the desired VCO frequency for the 22 MC VCO unit (see table II-4 for the VCO frequencies of each switch position).
FINE TUNE Control	1A6	Allows the VCO bias voltage to be varied from -6 to +6 vdc.
ATTEN Control	1A7	Provides variable attenuation for attenuating the nominal input signal (continuously variable over a 100 db range).

2.2.5 Frequency Converter 1A8

2.2.5.1 Functional Description

Frequency Converter 1A8 converts one of five different frequencies from the Test Transmitter to an output frequency in the frequency range of the Test Receiver. Also, the Frequency Converter supplies a 45 mc output to be used with a frequency counter.

2.2.5.2 Physical Description

Frequency Converter 1A8 (figure 2-10) is physically located in a slide-mounted drawer in the GSE Rack. The assembly components are housed in a standard 5¼ inch drawer. The drawer contains two major plug-in assemblies which may be removed for alignment, test, or repair. Table II-6 lists the assemblies used in the Frequency Converter.

A front panel FREQUENCY SELECTOR switch allows the operator to select any one of five oscillator frequencies listed in table II-7 to mix with the frequency obtained from the Test Transmitter.

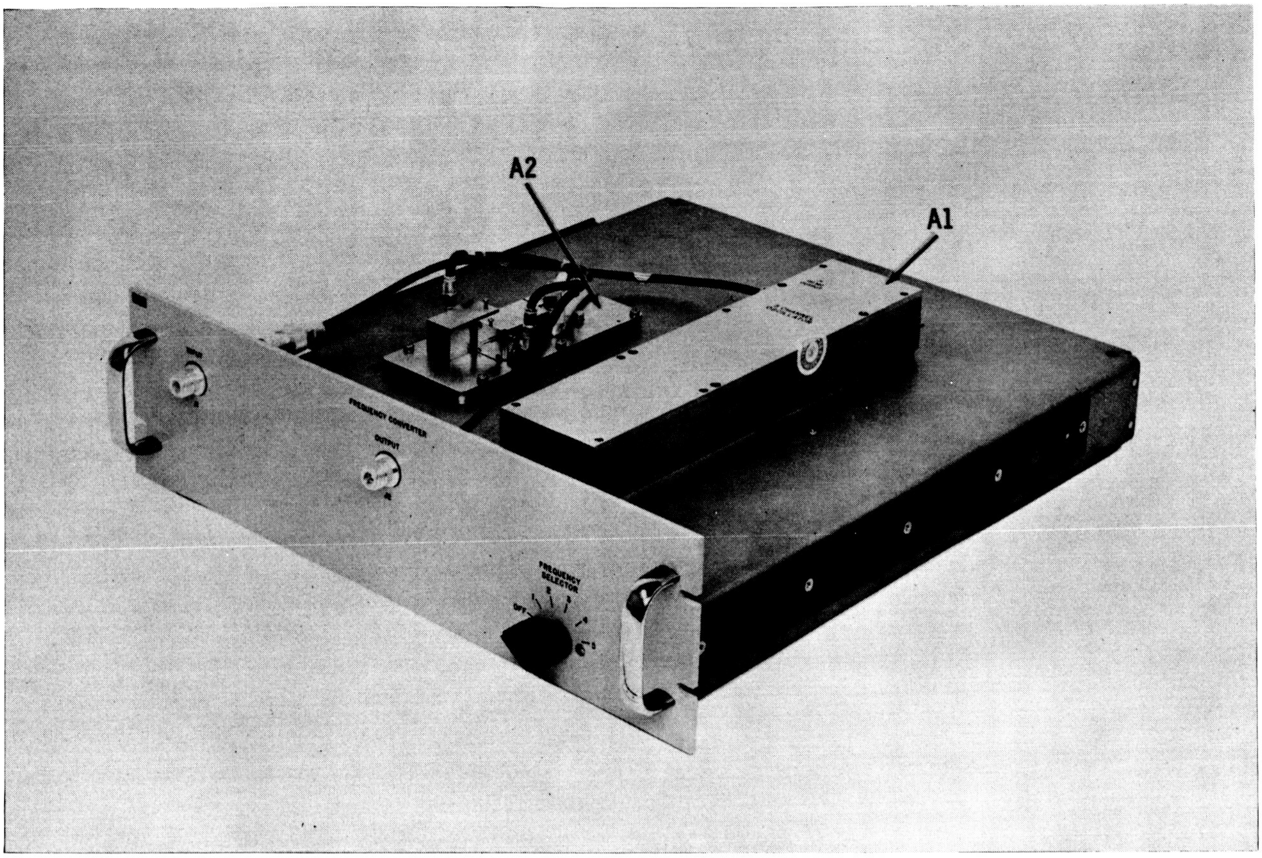


Figure 2-10. Frequency Converter 1A8, Top View

TABLE II-6. FREQUENCY CONVERTER ASSEMBLIES

Unit No.	Title	Part No.	Manufacturer
1A8A1	5-Channel Oscillator	01-25277E01	*Motorola
1A8A2	Mixer-Filter	01-20247E01	*Motorola

* Not DSIF designs.

TABLE II-7. FREQUENCY CONVERTER FREQUENCIES

Crystal Oscillator Center Frequency	Converter Input Frequency	Converter Output Frequency	X4 Frequency Multiplier Output (L.O. Frequency)
45.49518 mc	2116.722994 mc	2298.703704 mc	181.980708 mc
45.48785 mc	2116.381944 mc	2298.333333 mc	181.851388 mc
45.48052 mc	2116.040895 mc	2297.962963 mc	181.922071 mc
45.47319 mc	2115.699846 mc	2297.592593 mc	181.892748 mc
45.42187 mc	2113.312500 mc	2295.000000 mc	181.687480 mc

2.2.5.3 Technical Characteristics

The technical characteristics for the Frequency Converter are listed as follows:

Input Frequencies	(Refer to table II-7 for the five input frequencies.)
Output Frequencies	(Refer to table II-7 for the five output frequencies.) 45 mc to counter

2.2.5.4 Controls

The function of the control on the Frequency Converter is as follows.

Control	Function
FREQUENCY SELECTOR Switch (5-position rotary)	Selects one of the crystal oscillator center frequencies listed in table II-7 for conversion of the Test Transmitter output frequency to the Test Receiver input frequency.

2.2.6 Test Transmitter 1A9

2.2.6.1 Functional Description

Test Transmitter 1A9 provides a stable RF output signal at the proper signal level to the Spacecraft for checking the Spacecraft receiver performance. A signal to RWV RECEIVER jack, located on the lower rear of the drawer, provides an RF output signal at the proper signal level to use with the Read-Write-Verify (RWV) equipment (not a part of the GSE Rack).

2.2.6.2 Physical Description

The Test Transmitter (figures 2-11 and 2-12) is housed in a single, 10½ inch slide-mounted RF tight panel assembly in the GSE Rack. The drawer contains four major plug-in assemblies and various variable and step attenuators which may be removed for alignment, test, or repair. All other filtering and signal processing functions are a fixed part of the Test Transmitter chassis. Table II-8 lists the assemblies and main components used in the Test Transmitter.

Five different crystal controlled output frequencies can be selected by means of a front panel VCO SELECTOR switch. The VCO frequencies that the VCO SELECTOR switch can select and the resultant Test Transmitter output frequency are listed in table II-9. A front panel FREQUENCY CONTROL permits manual adjustment of any of the output frequencies over the range of ±76.8 kc minimum. In addition, a front panel RF LEVEL ADJ switch (step attenuator) and a variable attenuator permit manual adjustment of test transmitter output signal level over the range of -40 dbm to -190 dbm. The Test Transmitter operates from the ± 15 and -28 vdc power supplies.

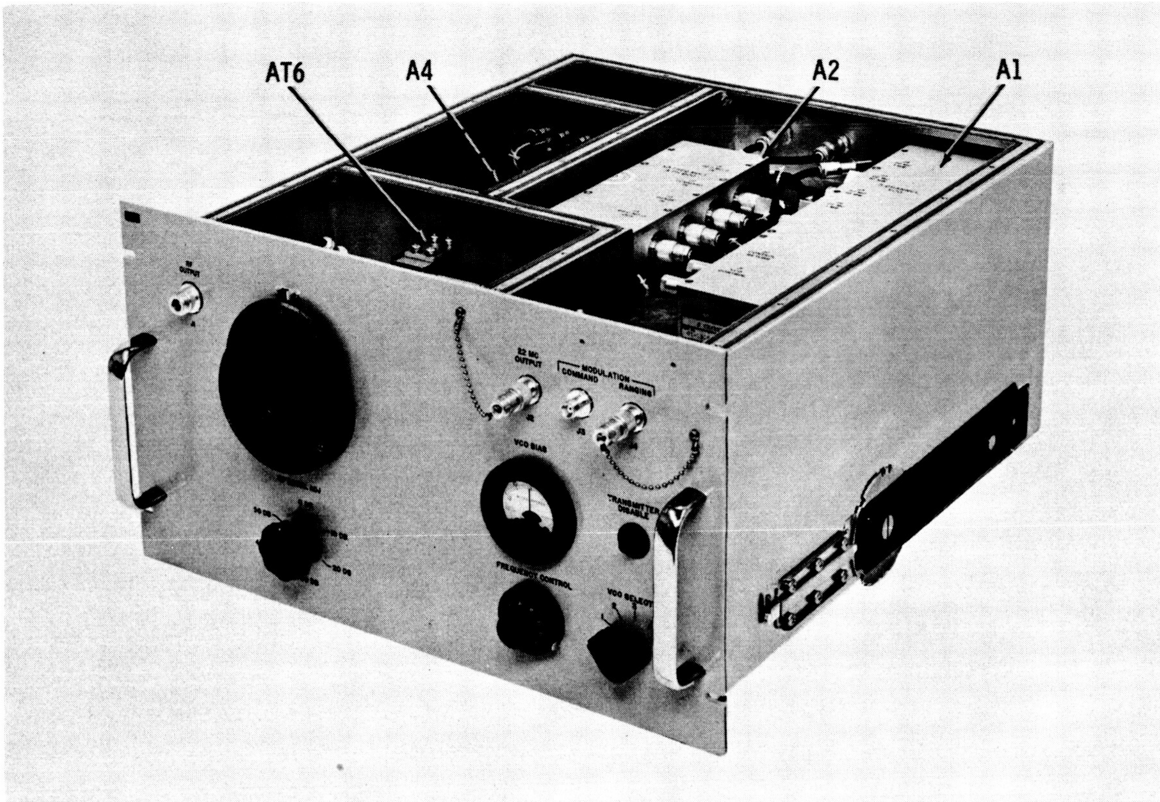


Figure 2-11. Test Transmitter 1A9, Top View, Cover Removed

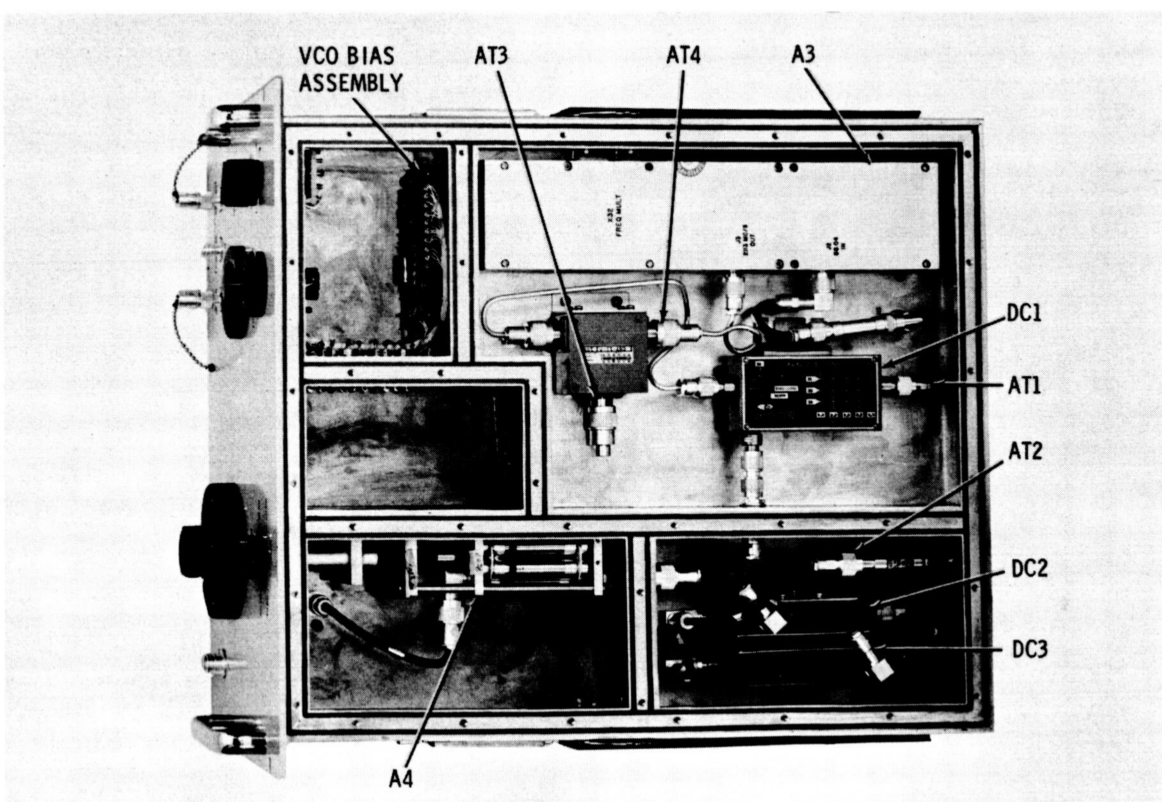


Figure 2-12. Test Transmitter 1A9, Bottom View, Cover Removed

TABLE II-8. TEST TRANSMITTER ASSEMBLIES

Unit No.	Title	Part No.	Manufacturer
1A9A1	5-Channel Transmitter VCO	01-25260E01	* Motorola
1A9A2	X3 Multiplier and Phase Modulator	01-23760D01	Motorola
1A9A3	X32 Frequency Multiplier	01-23786D01	Motorola
1A9A4	Thermistor Mount	HP-478A	* Hewlett-Packard
1A9AT6	Variable Attenuator	198S	* PRD
1A9AT1	Termination	TA 5 MT	* Microlab
1A9AT2	30 DB Attenuator	9513-30	* Stoddart
1A9DC1	20 DB Directional Coupler	3003-20	* Narda
1A9DC2	20 DB Directional Coupler	3003-20	* Narda
1A9DC3	20 DB Directional Coupler	3003-20	* Narda

TABLE II-9. TEST TRANSMITTER FREQUENCIES

VCO SELECTOR Switch Position	Transmitter Output Frequency (MC)	VCO Frequency (MC)	VCO Frequency Control Range (CPS)
1	2113.312500	22.013670 ±1 pt in 10^6	±800
2	2115.699846	22.038540 ±1 pt in 10^6	±800
3	2116.040895	22.042092 ±1 pt in 10^6	±800
4	2116.381944	22.045645 ±1 pt in 10^6	±800
5	2116.722994	22.049198 ±1 pt in 10^6	±800

2.2.6.3 Technical Characteristics

The technical characteristics for the Test Transmitter are as follows:

Switch Position	Center Frequency (MC)	Minimum Range (KC)
1	2113.312500	±76.8
2	2115.699846	±76.8
3	2116.040895	±76.8
4	2116.381994	±76.8
5	2116.722994	±76.8

NOTE

Any of the five center frequencies above are selectable by means of a front panel control. In each position, the output frequency can be varied by means of the front panel control over the minimum range specified.

*Not DSIF Design.

Power Output	-40 dbm to -190 dbm. Continuously variable by means of a step attenuator covering a 50 db range in 10 db steps and a variable attenuator covering a 100 db range.
Reference Output Level	The transmitter RF power reference level is provided to allow continuous monitoring of the transmitter output power by means of an internally contained thermistor mount and an external power bridge.
Power Output Accuracy	The power output to a matched load is indicated by the reference output and the attenuator calibration to an accuracy within ±5 db over the entire output range.
Spurious Signals	Output terminal: All spurious signals and sidebands are at least 30 db below the desired output signal level. Radiated: Radiation from the unit is less than -150 dbm as detected on a tuned dipole located 1 meter away from the Test Transmitter in any direction.
Output Impedance	50 ohms
Output to RWV Receiver	A rear panel connector furnishes a -45 dbm ±5 db output to enable monitoring of the signal by the Read-Write-Verify (RWV) Receiver in the system test complex.

2.2.6.4 Controls and Indicators

The functions of the indicators and controls for the Test Transmitter are as follows.

VCO SELECTOR Switch (5-position rotary)	Permits selection of each of the five crystal-controlled oscillators used to control the Test Transmitter output frequency.
FREQUENCY CONTROL Dial	A ten-turn potentiometer which permits adjustment of each of the Test Transmitter output frequencies over a ±76.8 kc range.
VCO BIAS Meter	Permits monitoring of the bias voltage applied to the 22 MC Voltage-Controlled Oscillator assembly.
RF LEVEL ADJUST Switch	A six-position step attenuator calibrated in 10 db steps from 0 to 50 db and a continuously variable attenuator which permits adjustment of the Test

RF LEVEL ADJUST Switch (cont)	Transmitter output signal to any level from -40 dbm to -190 dbm with ½ db increments.
TRANSMITTER DISABLE Switch (Momentary push button)	When depressed, this switch removes the Test Transmitter output signal to allow the power meter to be zeroed without affecting the transmitter stability.

2.2.7 Ranging Conversion Unit 1A10

2.2.7.1 Functional Description

The Ranging Conversion Unit 1A10 (located in GSE Rack, Serial No. 1) detects the 498 kc pseudo-random ranging modulation from a 10 mc IF signal (supplied from the 10 mc Distribution Amplifier in the Test Receiver) and supplies it to an external Ranging Receiver. A 10 mc reference required is obtained from the 10 mc Reference Distribution Amplifier in the Test Receiver. The Ranging Receiver function description is covered in the final report for the Mariner "C" S-Band Communication Subsystem Operational Support Equipment (Document No. 68-20399E).

2.2.7.2 Physical Description

The Ranging Conversion Unit 1A10 (figure 2-13) is mounted in a single, slide-mounted drawer in the GSE Rack (Serial No. 1). The drawer is a standard 12¼ inch drawer that contains three major plug-in assemblies which may be removed for alignment, test, or repair. Table II-10 lists the assemblies used in the Ranging Conversion Unit 1A10.,

TABLE II-10. RANGING CONVERSION UNIT ASSEMBLIES

Unit No.	Title	Part No.	Manufacturer
1A10A1	10 MC Phase Shifter	01-23793D01	Motorola
1A10A2	10 MC Phase Switch	01-23840D01	Motorola
1A10A3	10 MC Balanced Detector	01-23845D01	Motorola

2.2.7.3 Technical Characteristics

The technical characteristics for the Ranging Conversion Unit are as follows:

Reference Input Signal	10 mc at +10 dbm
Wide Band IF Input Signal	10 mc at -65 dbm
Output Frequency	498 kc at -70 dbm

2.2.8 Power Meter 1A10

Power Meter 1A10 (located in GSE Rack, Serial No. 2) is a Hewlett-Packard model 431B power meter used to monitor the relative RF power output of the Test Transmitter. The Test Transmitter is connected to the power meter through a modified Hewlett-Packard cable. Operating and maintenance instructions for the RF power meter are contained in a separate technical manual.

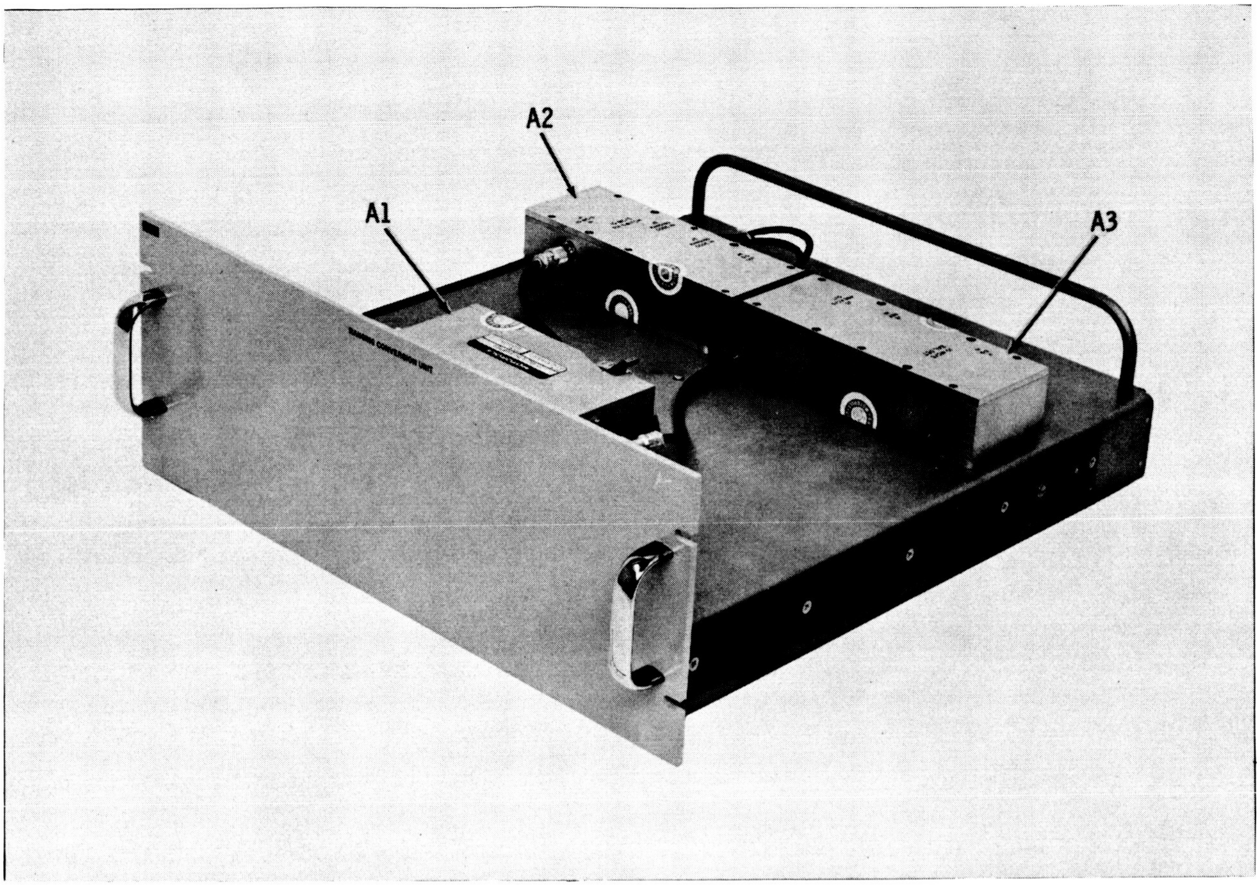


Figure 2-13. Ranging Conversion Unit 1A10,
Top View

2.2.8.1 Technical Characteristics

The technical characteristics for the power meter are as follows:

Power Ranges	7 ranges with full scale readings of 10, 30, and 100 μw; 1,3, and 10 mw. Also calibrated in dbm from -30 to +10 dbm.
Accuracy	±3% of full scale on all ranges from 20° to $35^{\circ}C$; ±5% from 0° to $55^{\circ}C$

2.2.9 <u>±15 Volt Power Supply 1A11</u>

The ±15 Volt Power Supply 1A11 provides +15 and -15 vdc to the Circuit Breaker Panel, Telemetry Narrow Band and Wide Band Subsystems, Test Receiver, Frequency Converter, Test Transmitter, and Ranging Subsystem. The unit is an unmodified Harrison Model 802B power supply. Operating and maintenance instructions for the power supply are contained in a separate technical manual.

2.2.9.1 Technical Characteristics

The technical characteristics for the power supply are as follows:

Voltage Range	0 to 32 vdc
Current Range	0 to 1 ampere
Regulation (load)	Better than 0.15% or 20 mw (whichever is greater) for load variations from 0 to full load
Regulation (line)	Better than 0.15% of 20 mw (whichever is greater) for input variations from 105 to 125 vac
Internal Impedance	Less than 0.05 ohms
Ripple and Noise	Less than 1 mw rms
AC Input	105 to 125 vac, 50-400 cps, 115 watts

2.2.10 ±28 Volt Power Supply 1A12

The ±28 Volt Power Supply 1A12 provides regulated +28 and -28 vdc to the Circuit Breaker Panel, Telemetry Narrow Band and Wide Band Subsystems, Test Receiver, and Test Transmitter. The unit is an unmodified Harrison Model 802B power supply that is identical to the ±15 Volt Power Supply 1A11. Operating and maintenance instructions are contained in a separate technical manual.

2.2.10.1 Technical Characteristics

The technical characteristics for the power supply are the same as the technical characteristics described in paragraph 2.2.9.1.

VOLUME 1

SECTION III

THEORY OF OPERATION

3.1 GENERAL

This section contains general design theory for the GSE. Detailed theory discussions are included for each of the major units designed specifically for the GSE. Theory discussions for commercial equipment contained in the GSE are included in the individual technical manuals supplied with the GSE.

3.2 SUMMARY OF OPERATION

The following subparagraphs contain a brief summary of the function of each of the units contained in the GSE arranged in the order of the unit designations in the rack enclosures. Refer to figure 3-1 for a simplified block diagram showing the relationship of the major assemblies. An over-all block diagram of the test set is presented in figure 6-1.

(1) Circuit Breaker Panel, 1A1 - Contains a circuit breaker for the rack assembly and provides for inclusion of two assemblies which are not supplied with the rack assembly. These two assemblies are a Single-Sideband unit and a 22 mc Isolation Amplifier assembly.

(2) Telemetry Narrow Band Subsystem, 1A2 - Provides a demodulation capability when used in conjunction with the Test Receiver. Attenuation and bandwidth selection are provided in the drawer to accommodate a wide range of input signal conditions (see paragraph 3.3).

(3) Telemetry Wide Band Subsystem, 1A3 - Is similar to 1A2, but has no demodulation capability. It provides selectable bandwidths and 10 mc intermediate frequency outputs for telemetering and spectral analysis (see paragraph 3.4).

(4) Test Receiver Parts 1, 2, 3, and 4; Panels 1A4, 1A5, 1A6, and 1A7 - are described in paragraph 3.5.

(5) Frequency Converter, 1A8 - Is a heterodyne frequency converter with a front panel selectable local oscillator frequency (see paragraph 3.6).

(6) Test Transmitter, 1A9 - Is described in paragraph 3.7.

(7) Ranging Conversion Unit, 1A10 - Is a conversion unit only, which transforms the Test Receiver intermediate frequency to a form which is compatible with other external ranging equipment.

(8) Power Supply, 1A11 - Supplies regulated ±15 vdc to various drawers in the test set.

(9) Power Supply, 1A12 - Supplies regulated ±28 vdc to the transmitter and receiver and energizing power for relays throughout the system.

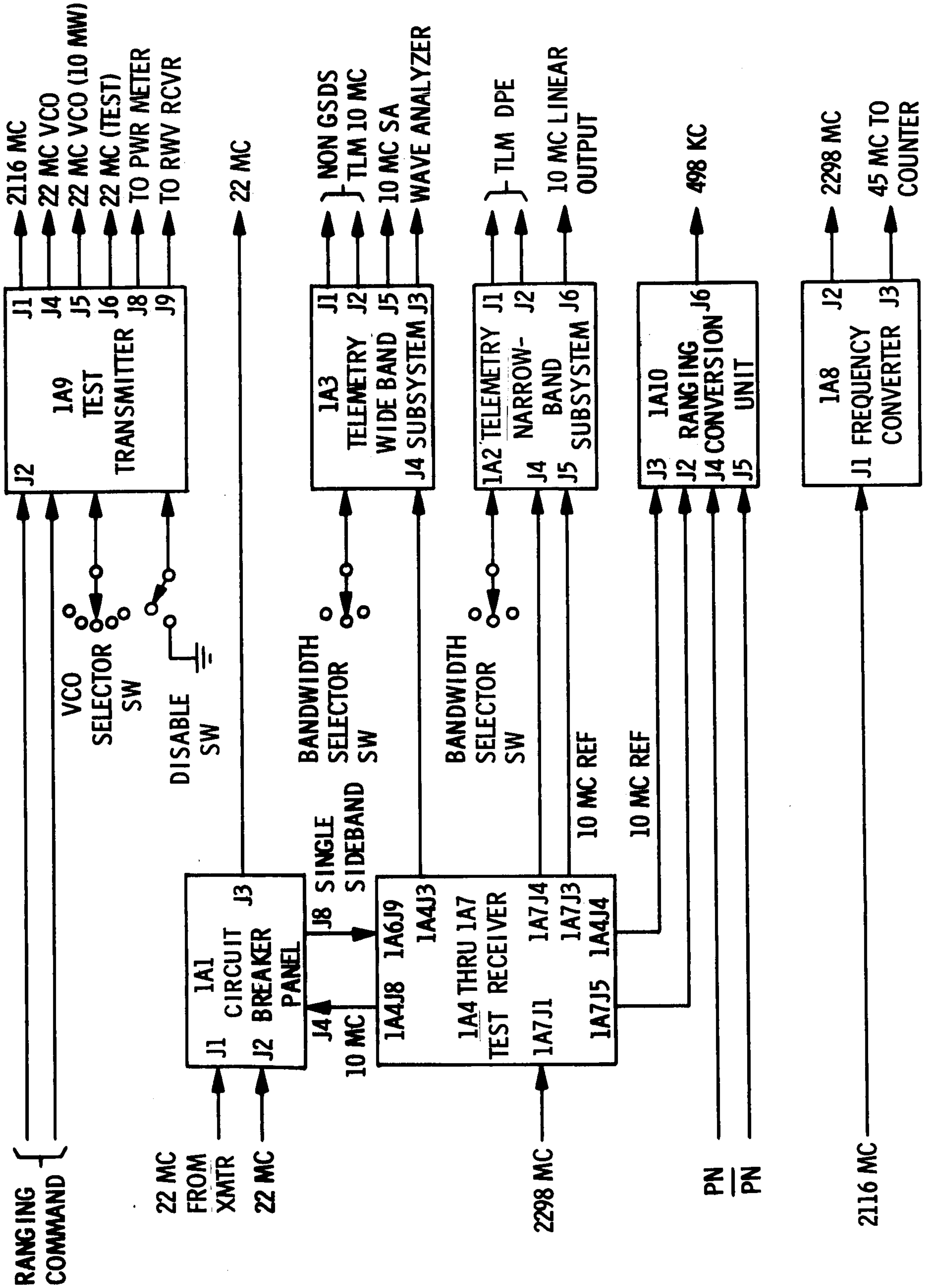


Figure 3-1. Mariner "C" Equivalent GSE, Simplified Block Diagram

3.3 TELEMETRY NARROW BAND SUBSYSTEM 1A2

The schematic diagram for the Telemetry Narrow Band Subsystem is shown in figure 6-5. This drawer is designed to demodulate the phase modulated 10 mc IF signal from the Test Receiver. The drawer consists of a selectable bandwidth amplifier, two step attenuators, an IF amplifier, a phase detector, a 10 mc phase shifter and an output video amplifier.

3.3.1 Telemetry Bandpass Filter 1A2A1

The schematic diagram for the Telemetry Bandpass Filter assembly is shown in figure 6-6. A two stage direct-coupled amplifier is used as a driver for the bandpass filter. Bandpass filters are selected by relays which are controlled by applying 28 volts to relay pairs, which transfer the filter inputs and outputs. The relay contacts used for indicator functions are not used in this system. The output signal from the bandpass filters is transformer coupled into a three transistor isolation-output amplifier, which provides for the two output amplitude levels required. The technical specifications for the Telemetry Bandpass Filter assembly are as follows:

Motorola No.	01-23800D01
Frequency	10 mc
Noise Figure	<10 db within 3 db bandwidth
Output Impedance	50 (±20) + j0 (±20) ohms
Gain	10 (±0.5) and 0 (±1.0) db
Linearity	Within ±0.5 db @ -55 dbm to +5 dbm output level
Isolation	20 db minimum

The four selectable bandwidth positions shall provide bandpass characteristics as follows:

4.5 Kc Bandpass Position

a. 4.5 KC (-1 db) minimum bandwidth
b. 7 KC (-3 db) maximum bandwidth
c. 3/30 db shape factor 1 to 5 maximum
d. Ripple within -1 db bandwidth, ±0.5 db maximum
e. All spurious responses at least 30 db down.
f. Phase linearity within ±10% across -1 db bandpass
g. Phase symmetry ±10 degrees maximum across -1 db bandpass

20 KC Bandpass Position

a. 20 KC (-1 db) minimum bandwidth
b. 30 KC (-3 db) maximum bandwidth
c. 3/30 db shape factor 1 to 5 maximum
d. Ripple, within -1 db bandwidth, ±0.5 db maximum
e. All spurious responses at least 30 db down.
f. Phase linearity within ±10% across -1 db bandpass
g. Phase symmetry ±10 degrees maximum across -1 db bandpass

420 KC Bandpass Position

a. 420 KC (-1 db) minimum bandwidth
b. 600 KC (-3 db) maximum bandwidth
c. 3/30 db shape factor 1 to 7 maximum
d. Ripple, within -1 db bandwidth, ±0.5 db maximum
e. All spurious responses at least 30 db down.
f. Phase linearity within ±10% across the -1 db bandpass
g. Phase symmetry within ±10 degrees across the -1 db bandpass

3.3 MC Bandpass Position

a. ±8.0 MC (-3 db) minimum
b. ±9.0 MC (-3 db) maximum
c. Ripple, within the -1 db bandwidth, ±0.5 db maximum
d. All spurious responses at least 20 db down.
e. Phase linearity ±10% across the -1 db bandpass
f. Phase symmetry within ±10 degrees across the -1 db bandpass

3.3.2 Narrow Band 10 MC IF Amplifier 1A2A2

The schematic diagram for the Narrow Band 10 MC IF Amplifier assembly is shown in figure 6-7. The circuit consists of two synchronously tuned cascode amplifiers. The output signal from the second cascode amplifier is divided to drive a linear output amplifier Q5 and a limiting stage, consisting of Q6 and CR1 and CR2. The output from the linear amplifier is provided at the rear panel (J2) for possible future use. Transistors Q7 and Q8 provide isolation and impedance matching for the limited output. Technical specifications for the Narrow Band 10 MC IF Amplifier assembly are as follows:

Motorola No.	01-24272D01
Frequency	10 mc
Gain	40 (±1) db
Bandwidth	1.8 mc minimum, 2.2 mc maximum
Input Impedance	50 ohms, VSWR <1.2:1
Output Impedance	50 (±20) + j0 (±20) ohms
Output Level(limited)	+4 dbm
Linearity	±2 db @ -22 to +8 dbm output
Phase Symmetry	±20° maximum within 3 db bandwidth
Spurious Outputs	<40 db below the desired signal
Noise Figure	13 db maximum

3.3.3 10 MC Phase Detector 1A2A3

The 10 MC Phase Detector schematic diagram is shown in figure 6-8. The circuit is basically the same as the phase detector used in the Test Receiver (1A5A2 or 1A5A4) with added circuitry to increase the bandwidth characteristics. A reference signal for the detector is provided by Q1, a common base limiter amplifier. Transistor Q2 is a linear amplifier used to supply the phase modulated signal to the detector. Coils L5 through L8 and capacitors C15, C20, C27, and C28 form a bandpass shaping network to provide the necessary bandwidth. Technical specifications for the 10 MC Phase Detector assembly are as follows:

Motorola No.	01-24373D01
Frequency	10 mc nominal input
Input Impedance	50 ohms, VSWR <1.2:1 at center frequency, VSWR <1.5:1 within 3 db
Gain	0.013 volts per degree @ +4 dbm input and 1K load
Limiter	Full value at +7 dbm reference input
Linearity	<±10% @ -6 to +6 dbm input
Output Impedance	500 ohms ±20%
Frequency Response	Dc to 700 kc @ -1 db
Balance	±3 mv @ 500 kc out or noise input
Load Impedance	1000 ohms

3.3.4 <u>Video Amplifier 1A2A4</u>

The schematic diagram for the Video Amplifier assembly is shown in figure 6-9. The video signal is amplified by a two stage direct-coupled amplifier consisting of Q1 and Q2. The signal is then used to drive two identical output amplifiers. The output of Q6 is used to provide two parallel outputs. The technical specifications for the Video Amplifier assembly are as follows:

Motorola No.	01-23853D01
Frequency	50 cps to 3 mc minimum @ -3 db
Gain	20 (±1) db
Input Level	-30 to -10 dbm
Output Level	Linear to +10 dbm, all outputs within 1 db @ -10 to +10 dbm output
Output Noise Power	Less than -55 dbm in 50 ohm load
Input Impedance	50 ohms, VSWR <1.2:1 center VSWR 1.5:1 @ -1 db frequencies
Output Impedance	50 (±10) + j0 (±10) ohms
Spurious Outputs	40 db down from the desired output

3.3.5 <u>10 MC Phase Shifter 1A2A5</u>

The 10 MC Phase Shifter assembly is identical to the 10 MC Phase Shifter 1A5A3 (paragraph 3.5.12) and the circuit discussion and specifications are included in the Test Receiver section.

3.4 TELEMETRY WIDE BAND SUBSYSTEM 1A3

The schematic diagram for the Telemetry Wide Band Subsystem is shown in figure 6-11. The drawer provides four selectable predetection bandwidths. There is no demodulation capability in the drawer, the outputs being 10 mc IF signals, except the 30 mc spectrum analyzer output, for telemetering and spectral analysis with external equipment.

3.4.1 Telemetry Bandpass Filter 1A3A1

The schematic diagram for the Telemetry Bandpass Filter assembly is shown in figure 6-6. This assembly is identical to 1A2A1 (paragraph 3.3.1) and provides the same bandwidth selection characteristics.

3.4.2 Wide Band 10 MC IF Amplifier 1A3A2

The schematic diagram for the Wide Band 10 MC IF Amplifier assembly is shown in figure 6-12. The circuit consists of two similar two-transistor direct-coupled amplifiers. The amplifiers incorporate feedback, which aids the band shaping characteristics. The output of the second amplifier pair, Q3 and Q4, is paralleled to drive four identical output amplifiers. The output amplifiers are two-transistor direct-coupled amplifiers with sufficient power handling capability to satisfy the linearity requirement. The technical specifications for the Wide Band 10 MC IF Amplifier assembly are as follows:

Motorola No.	01-23795D01
Frequency	10 mc center
Noise Figure	<10 db
Bandwidth	±5.5 mc minimum ±8 mc maximum
Gain	58 (±1) db
Impedance, Input	50 (±5) + j0 (±5) ohms
Impedance, Output	50 (±10) + j0 (±10) ohms
Linearity	±0.5 db, @ -20 to +10 dbm output
Relative Outputs	All within 1 db
Phase Characteristics	±10 degrees @ ±2 mc
	±10 degrees relative to input
Output Isolation	>30 db

3.4.3 10.02 MC Mixer-Oscillator 1A3A3

The schematic diagram for the 10.02 MC Mixer-Oscillator assembly is shown in figure 6-13. This assembly provides for converting the 10 mc IF spectrum to a frequency range compatible with analyzer equipment. The input signal is amplified by two synchronously tuned amplifier stages, Q5 and Q2. The local oscillator signal is produced in an internal crystal oscillator operating at 10.020 mc, thus producing a nominal 20 kc output when mixed with the 10 mc IF input signal. Mixing is accomplished in diodes CR1 and CR2 in a balanced mixer circuit. TP1 allows monitoring of the 10 mc signal at the mixer input. The output signal of the mixer is fed to a direct coupled two stage amplifier. The output signal leaves the assembly through pin 4 of P1. The technical specifications for the 10.02 MC Mixer-Oscillator assembly are as follows:

Motorola No.	01-23844D01
Frequency	10 mc nominal input
Input Signal Level	-22 dbm maximum
Input Impedance	50 ohms, VSWR <1.2:1 <1.5:1 @ -3 db frequencies
Bandwidth	±2 mc @ -3 db (at J3)
Isolation	LO Signal >40 db down at the input
Stability	1×10^{-6} minimum for 3 hr period at ambient temperature 15^{o} to $45^{o}C$
Output Frequency	20 kc nominal
Bandwidth	20 cps to 60 kc @ -3 db
Output Impedance	1000 ohms maximum
Signal Level	3 (±0.3) VRMS across a load of 100 K ohms in parallel with 1000 pf @ -22 dbm input
Linearity	<±5% @ 0.1 to 3 VRMS output
Spurious Signals	>40 db below the desired output

3.4.4 <u>10-30 MC Converter 1A3A4</u>

The 10-30 MC Converter assembly (figure 6-11) is a commercial mixer manufactured by General Radio Company. It is used to convert the 10 mc to 30 mc for compatability with external spectrum analysis equipment. The technical specifications for the 10-30 MC Converter are as follows:

Frequency Range	40 mc to 5 gc; at lower and higher frequencies with decreased sensitivity
Crystal	1N21B
Crystal Current	5 ma maximum, 0.2 ma minimum
LO Input	2 volts maximum
Output Filter	40 mc cutoff frequency
Output Impedance	Approximately 400 ohms

3.5 TEST RECEIVER

The Test Receiver is contained in four drawers, 1A4, 1A5, 1A6, and 1A7. An interconnection diagram of the drawers is shown in figure 6-14. The schematic diagrams for the Test Receiver drawers are shown in figures 6-15, 6-21, 6-24, and 6-27. The Test Receiver is a dual conversion type which uses phase-lock techniques for automatic tracking of the input signal and a phase-coherent automatic gain control. A strip-line hybrid-ring diode mixer converts the S-Band signal to a 50 mc first intermediate frequency in the S-Band Mixer (1A7A1), where it is mixed with the S-Band local oscillator signal from the X32 Multiplier 1A4A4. The second conversion is accomplished in the 50 MC IF Amplifier and Second Mixer assembly (1A7A2) by mixing the first intermediate frequency and a 60 mc signal, from the 20 MC Oscillator and X3 Multiplier assembly (1A4A1), to produce the second intermediate frequency of 10 mc.

A 10 MC Isolation and Distribution Amplifier assembly (1A7A3) provides output signals for the telemetry and ranging drawers. The last IF amplifier output drives the phase detector and the coherent amplitude detector. The IF signals are detected by these detectors to provide the tracking control voltage and the automatic gain control voltage. The output of the phase detector drives the RF loop voltage-controlled oscillator. The oscillator, in turn, drives the local oscillator multiplier,which provides the phase coherent injection to the first mixer.

3.5.1 Automatic Phase Control (APC) Loop

The receiver automatic phase control loop includes the 10 MC IF Amplifier, 50 MC IF Amplifier and Second Mixer, 10 MC IF Distribution Amplifier, RF Loop-phase Dectector, Loop Filter, Receiver Voltage-controlled Oscillator, X3 Multiplier, X32, Multiplier and Mixer Preamplifier. The transfer function and the mechanization of the transfer function are described in the following paragraphs.

3.5.1.1 Transfer Function (APC)

The normalized transfer function of the APC loop is defined by:

$$H(S) = \frac{1 + \frac{3}{4\beta_L} (S)}{1 + \frac{3}{4\beta_L} (S) + \frac{9}{32\beta_L 2} (S^2)}$$

where β_L = low pass noise bandwidth

$$= \frac{1}{2\pi} \int_{-\infty}^{\infty} \left| H (jw) \right|^2 df$$

When the APC loop is operating under varying signal-to-noise ratios as a result of a small signal input, the noise bandwidth of the APC loop is affected in the following manner:

$$\beta_L = \beta_{L_o} \left(\frac{1}{3} + \frac{2\alpha}{3\alpha_o} \right)$$

Where $\beta_{L_o} = \frac{1}{2}$ effective noise bandwidth at design point,

$$\alpha = \frac{1}{\sqrt{1 + \frac{4}{\pi} \left(\frac{N}{S}\right)}}$$

α_o = unity at strong signal

N = noise power in IF passband

S = signal power in IF passband

$$\beta_{L_o} = \left(\frac{9G_o}{32T_1} \right)^{1/2}$$

and $T_1 = (R_1 + R_2)C$ tracking filter lagging time constant

G_o = Open loop gain at design point

$= K_D K_V K_M \alpha_o$ (360)

where K_D = phase detector constant in volts/degree,
K_V = VCO constant in cycles/volt, and
K_M = frequency multiplication.

The loop filter is composed of two time constants:

$T_1 = (R_1 + R_2)C$ = tracking filter lagging time constant
$T_2 = R_2C$ = tracking filter leading time constant

These time constants are related to one-half the effective noise bandwidth (β_{Lo}) at the design point by:

$$T_1 = \frac{9G_o}{32\beta_{L_o}^{\ 2}}$$

$$T_2 = \frac{3}{4\beta_{L_o}}$$

The static phase error (SPE) for an input signal offset frequency in cps of ΔF from the design point is:

$$SPE = \frac{\Delta F}{K_D K_V K_M} \text{ degrees}$$

3.5.1.2 Mechanization of Transfer Function

The design point for the APC Loop is for a signal carrier level at threshold. The phase gain constants of the Test Receiver are:

K_D = 0.350 volts/degree (20-volt peak 'S' curve)
K_V = 150 cps/volt
K_M = 96
$G_o = K_d K_v K_m \ 360 \ \alpha_o$

The threshold signal suppression factor, α_o is calculated from the following expression:

$$\alpha_o = \frac{1}{\sqrt{1 + \frac{4}{\pi} \left({}^N/S \right)}} \text{ , since } \frac{N}{S} = \frac{B_n}{2\beta_L}$$

$$= \frac{1}{\sqrt{1 + \frac{4}{\pi} \left(\frac{B_n}{\beta_L} \right)}}$$

where B_n = 2000 cps = the predetection bandwidth

for $2\beta_L$ = 5 cps

$$\alpha_o = \frac{1}{\sqrt{1 + \frac{4}{\pi}(400)}} = 0.0442$$

for $2\beta_L$ = 12 cps

$$\alpha_o = \frac{1}{\sqrt{1 + \frac{4}{\pi}(167)}} = 0.0688$$

for $2\beta_L$ = 48 cps

$$\alpha_o = \frac{1}{\sqrt{1 + \frac{4}{\pi}(83.3)}} = 0.136$$

for $2\beta_L$ = 152 cps

$$\alpha_o = \frac{1}{\sqrt{1 + \frac{4}{\pi}(13.2)}} = 0.237$$

Now G_o may be calculated for the various bandwidths as follows:

$$2\beta_{L_o} = 5 \text{ cps}$$
$$G_o = K_D K_V K_M (360)\ (\alpha_o)$$
$$= (0.350)(150)(96)(360)(0.0442)$$
$$= 80{,}196$$

$$2\beta_{L_o} = 12 \text{ cps}$$
$$G_o = (0.350)\ (150)(96)(360)(0.0685)$$
$$= 124{,}286$$

$$2\beta_{L_o} = 48 \text{ cps}$$
$$G_o = (0.350)(150)(96)(360)(0.136)$$
$$= 246{,}758$$

$$2\beta_{L_o} = 152 \text{ cps}$$
$$G_o = (0.350)(150)(96)(360)(0.237)$$
$$= 430{,}013$$

The loop filter time constants for a β_{Lo} of 2.5, 6, 24, and 76 are:

$$T_{1(2.5)} = \frac{9G_o}{32\beta_{L_o}^{\ 2}} = \frac{(9)(80{,}196)}{(32)(6.25)} = 3593 \text{ seconds}$$

$$T_{1(6)} = \frac{(9)(124{,}286)}{(32)(36)} = 967 \text{ seconds}$$

$$T_{1(24)} = \frac{(9)(246{,}758)}{(32)(576)} = 120 \text{ seconds}$$

$$T_{1(76)} = \frac{(9)(430{,}013)}{(32)(5776)} = 20.8 \text{ seconds}$$

$$T_{2(2.5)} = \frac{3}{(4)(2.5)} = 0.3 \text{ second}$$

$$T_{2(6)} = \frac{3}{(4)(6)} = 0.125 \text{ second}$$

$$T_{2(24)} = \frac{3}{(4)(24)} = 0.031 \text{ second}$$

$$T_{2(76)} = \frac{3}{(4)(76)} = 0.0098 \text{ second}$$

The loop filter uses extremely low leakage (380 μf and 20 μf) capacitors. The nominal resistance values for this filter are:

$$T_{1(2.5)} = (R_4 + R_6 + R_{11} + R_{12})(380 \times 10^{-6}) = 3593 \text{ seconds}$$

$$R_4 + R_6 + R_{11} + R_{12} = 9.45 \text{ megohms}$$

$$T_{1(6)} = (R_6 + R_{12})\ (380 \times 10^{-6}) = 967 \text{ seconds}$$

$$R_6 + R_{12} = 2.54 \text{ megohms}$$

$$T_{1(24)} = (R_5 + R_7 + R_8 + R_9)\ (20 \times 10^{-6}) = 120 \text{ seconds}$$

$$R_5 + R_7 + R_8 + R_9 = 6.0 \text{ megohms}$$

$$T_{1(76)} = (R_7 + R_9)\ (20 \times 10^{-6}) = 20.8 \text{ seconds}$$

$$R_7 + R_9 = 1.04 \text{ megohms}$$

$$T_{2(2.5)} = (R_{11} + R_{12})\ (380 \times 10^{-6}) = 0.3 \text{ second}$$

$$R_{11} + R_{12} = 789 \text{ ohms}$$

$$T_{2(6)} = R_{12}(380 \times 10^{-6}) = 0.125 \text{ second}$$

$$R_{12} = 329 \text{ ohms}$$

$$T_{2(24)} = (R_8 + R_9)\ (20 \times 10^{-6}) = 0.031 \text{ second}$$

$$R_8 + R_9 = 1550 \text{ ohms}$$

$$T_{2(76)} = R_9(20 \times 10^{-6}) = 0.0098 \text{ second}$$

$$R_9 = 490 \text{ ohms}$$

3.5.2 Automatic Gain Control (AGC) Loop

The receiver automatic gain control loop includes the IF and distribution amplifiers, the AGC detector and the AGC filter. The transfer function and its mechanization are described in the following paragraphs.

3.5.2.1 Transfer Function (AGC)

The transfer function of the coherent AGC loop is defined by:

$$H(S) = \frac{1}{1 + \frac{1}{G} + \frac{T}{G} S}$$

where T = RC time constant of the AGC loop filters.

G = loop gain
$= K_d K_a K_o$
= 21 average value

where K_d = amplitude detector gain constant
= 0.06 v/db nominal
K_a = IF amplifier AGC gain constant
= 3.4 db/volt nominal
K_o = operational amplifier gain
= 100

The noise bandwidth of the AGC loop is at the design point as defined by:

$$2\beta_L = \frac{G}{2T}$$

where $2\beta_L$ = noise bandwidth

The bandwidth is selectable by a front panel switch. The bandwidths are 0.118, 1.18 and 4.5 cps.

3.5.3 Calibrated Variable Attenuator 1A7AT1

The calibrated variable attenuator (see Test Receiver Part 4, schematic diagram, figure 6-27) permits adjustment of the 2298 mc input signal level as desired for the test to be performed. The calibrated variable attenuator was manufactured by PRD Electronics Co., Inc. Typical insertion loss is 16 to 18 db. The calibration curve of attenuation vs degrees of shaft rotation at the operating frequency for each unit was used to determine the graduation increments applied to the attenuator dial mounted on the receiver front panel. Each dial is engraved with the serial number of the attenuator which it matches. In addition, a "T" or "R" following the serial number indicates that the attenuator was calibrated for either the transmitter frequency of 2116 mc or the receiver frequency of 2298 mc.

3.5.4 Cavity Preselector 1A7Z1

The 2298 mc input signal is fed to the S-Band Mixer assembly through the Cavity Preselector 1A7Z1, which is an S-Band filter manufactured by the Rantec Corporation. The electrical specifications for the filter are as follows:

Model No.	FS-214-4
Center Frequency	2295 mc
Insertion Loss	0.9 db maximum
VSWR (f_o)	1.2:1 maximum

3.5.5 Local Oscillator Filter Cavities, 1A7Z2 and Z3

The local oscillator signal for the S-Band Mixer assembly is supplied from the X96 multiplier chain (X32 Frequency Multiplier and X3 Frequency Multiplier Assemblies) by way of two tandem connected Rantec Filter cavities (figure 6-27), which remove any spurious signals from the local oscillator signal. The electrical specifications for the filters are as follows:

Model No.	FS-214-6
Center Frequency (f_o)	2245 mc
Insertion Loss	0.9 db maximum
VSWR (f_o)	1.2:1 maximum

3.5.6 Mixer, S-Band 1A7A1

The 2295 mc input signal and the 2245 mc local oscillator signal are mixed in the S-Band Mixer 1A7A1 (figure 6-28). The 50 mc IF signal produced is amplified by three synchronously tuned cascode stages to give an over-all conversion gain of 50 db. Crystal current in the mixer may be measured at TP 1-A and B and PT2-A and B for each of the two mixer crystals. Technical Specifications are as follows:

Motorola No.	01-23773D01
Frequency	2298 mc
L.O. Power	1.0 mw nominal
VSWR	1.8:1 maximum
Noise Figure	10 db maximum
Power Gain	49 ±1 db
Intermediate Frequency	50 mc
IF 3 db Bandpass	±4 mc minimum, ±5 mc maximum
Output Impedance	50 (±20) + j0 (±20) ohms

3.5.7 50 MC IF Amplifier and Mixer 1A7A2

The second conversion, from 50 mc to 10 mc, takes place in the 50 mc IF Amplifier and Second Mixer assembly (figure 6-29). This assembly is essentially a continuation of the 50 mc IF amplifier portion of the preceding one. It consists of four additional cascode stages, synchronously tuned, which drive a balanced diode mixer to produce a 10 mc output. The 60 mc local oscillator signal is supplied by the 20 MC Oscillator and X3 Multiplier (figure 6-16). The first three amplifier stages are designed to provide a variable gain control. Gain is controlled by base current variations on Q1, Q3, and Q5. Regulated reference current is provided by CR1, CR2, R42, R15, and R43. Components R18, CR4, CR5, R19, CR3, and R20 provide slope adjustment for gain versus AGC voltage. Diodes CR4 and CR5 aid in temperature stabilization. Technical specifications for the 50 MC IF Amplifier and Second Mixer assembly are as follows:

Motorola No.	01-23774D01
Center Frequency	50 mc
Gain (conversion)	53 ±1 db at 0 volts AGC

Dynamic Range	-72 to +52 db (See the typical graph on figure 9 of assembly 1A7A2, located in Volume 3.)
Gain Linearity	±0.5 db from -60 dbm to -10 dbm at 0 volts AGC
Impedance	Output - 50 (±10) + j0 (±10) ohms
	Input - 50 ohms, VSWR < 1.2:1
Leakage	All RF signals 10 μv maximum on power leads
Bandwidth	±4 mc minimum, ±5 mc maximum
Mixer Balance	15 db minimum
Noise Figure	15 db maximum at gain 30 db
Phase Shift	(See the typical graph on figure 8 of assembly 1A7A2, located in Volume 3.)
Input Signal Level	-16 dbm to -120 dbm

3.5.8 10 MC Distribution Amplifier 1A7A3

The 10 mc output signal from the 50 MC IF Amplifier and Second Mixer assembly drives the 10 MC Distribution Amplifier assembly. This assembly (figure 6-30) consists of two amplifier sections. One is an RC-coupled two-stage common emitter amplifier whose outputs drive the telemetry and ranging converter drawers. The other section is a cascode stage which is used to drive the following 10 MC IF Amplifier assembly (1A7A4). Technical specifications for the 10 MC Distribution Amplifier are as follows:

Motorola No.	01-23775D01
Frequency	10 mc nominal
Input Signal Level	-80 dbm nominal
Noise Power	-10 dbm maximum
Input Impedance	50 ohms, VSWR <1.2:1
Noise Figure	7 db maximum
Linearity	±0.5 db from -75 dbm to +5 dbm
Gain	15 ±0.5 db
Output Impedance	50 (±20) + j0 (±20) ohms
Bandwidth	(J2, J3, and J4) ±5.5 mc minimum, ±8 mc maximum (J5) ±1 mc minimum, ±2 mc maximum
Gain Stability	±1 db at 15^o to 45^{o}C

3.5.9 10 MC IF Amplifier 1A7A4

The final assembly (figure 6-31) in the 10 MC IF Amplifier chain is used to drive the phase and amplitude detectors. The input signal is fed to a crystal filter which limits the IF bandwidth to approximately 2 kc. The signal is then amplified by two cascode amplifier stages. The signal at this point is divided to drive a linear amplifier, Q5, which provides a linear output signal for the AGC detector. The other signal path goes to Q6 and then to Q7, which are tuned RF amplifiers used to provide a limiting level signal to Q8, which provides a constant power output at J3 for the loop phase detector. Technical specifications for the 10 MC IF Amplifier assembly are as follows:

Motorola No.	01-23776D01
Center Frequency	10 mc
Gain	54 ±1 db (linear)
Bandwidth	2.0 kc ±180 cps
Output Impedance	50 ±10 ohms
Output Level	Linear ±2 db from -22 dbm to +8 dbm at linear output. Limited output +4 dbm.
Input Impedance	50 ohms VSWR <1.2:1

3.5.10 Loop 10 MC Phase Detector (AGC) 1A5A4

The linear 10 mc signal from the 10 MC IF Amplifier assembly is used to drive Q2 in the 10 MC Phase Detector assembly (figure 6-23), which is operated as a linear amplifier. The signal is tuned in a double-tuned link-coupled network and then fed to the phase detector network through C14 and C13. A reference signal for the detector is supplied from the X½ Multiplier (1A4A2) to the reference input, J2. This signal drives Q1, a limiting amplifier, which provides a reference signal of constant amplitude. The detector produces a dc output voltage, which is approximately equal to twice the peak signal voltage in the detector. The tuned circuits are peaked for maximum dc voltage at the test point. Technical specifications are shown in 3.5.11 as both detectors are identical.

3.5.11 Loop 10 MC Phase Detector (APC) 1A5A2

The APC Loop 10 MC Phase Detector assembly is identical to the AGC Loop 10 MC Phase Detector assembly. The difference is in application only. The reference signal portions are operated under identical conditions. The signal amplifier, Q2, is driven with a level of +4 dbm from the 10 MC IF amplifier assembly at a constant level so that the amplitude of the reference input and signal input are constant, and the dc output voltage becomes a function of the phase difference between the reference input and the signal input. This dc voltage, after filtering, is used to control the VCO frequency to maintain the loop in a phase-locked condition. Technical specifications for the 10 MC Loop Detector assembly are as follows:

Motorola No.	01-21432C01
Frequency	10 mc nominal
Output Impedance	40K maximum
Input Impedance	50 ohms, VSWR <1.2:1
Gain	1.0 (±5%)V out at -22 dbm signal input
Limiter	Output within 1 db with a reference variation of +4 dbm to +7 dbm
Linearity	±10% at -22 to +7 dbm, and <3 db down at +10 dbm
Bandwidth	±5 kc at 3 db

Balance	±10 mv maximum at -22 dbm non-coherent signal, or noise at +10 dbm
Phase Characteristics	±10 degrees over temperature
Phase Stability	2 degrees peak in 20 cps BW
Transfer Function	350 (±10) mv/degree at +4 dbm signal input level
Symmetry	Maximum and minimum output voltage within 500 mv

3.5.12 10 MC Phase Shifter 1A5A3

The phase and amplitude detectors require a 90^{o} phase shift between detector reference signals to produce a maximum output signal out of the amplitude detector since the phase detector must operate near zero output. This phase shift is accomplished in the 10 MC Phase Shifter assembly (figure 6-10). The phase shift is accomplished in Z1, a Variogon type (V53), which is followed by an untuned isolation amplifier, Q1. This amplifier is followed by three synchronously tuned amplifiers which accomplish the gain, limiting and output impedance matching. Technical specifications for the 10 MC Phase Shifter assembly are as follows:

Motorola No.	01-23793D01
Frequency	10 mc (±0.0025%)
Input Impedance	50 ohms, VSWR 1.2:1
Output Impedance	50(±20) +j0 (±20) ohms
Input Voltage	0.5 to 1.0 V RMS (±10 dbm nominal)
Gain	0 (±2 db) dbm
Distortion	Less than 40 db
Overall Phase Shift	±10^{o} (±0.5^{o} RMS jitter) over any 10^{o} increment, 15 to 45^{o}C.
Adjustable Phase Shift	0 to 360^{o}
Accuracy	±7^{o}, repeatable ±3.0^{o} over short time periods

3.5.13 X½ Frequency Multiplier 1A4A2

The reference signal for the loop detectors is generated by the reference oscillator at 20 mc. This frequency is reduced by a factor of two by the X1/2 Frequency Multiplier assembly (figure 6-17). The input stage of the X1/2 Frequency Multiplier assembly is a double-tuned input, tuned output amplifier which drives the varactor divider, which includes a 10 mc tuned circuit consisting of silicon capacitors, C15 and C16, and the primary of the transformer, T4. The 20 mc signal drives this tuned circuit, which generates a signal at half the frequency of the input signal. This 10 mc signal drives Q2, which is fixed-tuned to 10 mc by L3 and C17, which in turn drives three output amplifier stages. The output tank circuits provide, with selected components, a 50-ohm output impedance. Technical specifications for the X1/2 Frequency Multiplier assembly are as follows:

Motorola No.	01-21456C01
Frequency	20 mc input 10 mc output
Input Impedance	50 (±5) + j0 (±5) ohms
Output Impedance	50 (±10) + j0 (±10) ohms
Isolation	10 mc signal at input -70 dbm maximum >95 db output to input at 50 mc
Spurious Signals	>20 db below fundamental frequency
Phase Characteristics	$<5^{\circ}$, w/temperature between the 3 outputs
Level	+10 dbm ±3 db input +10 dbm ±2 db output
Bandwidth	±0.5 mc, 3 db at output frequency

3.5.14 20 MC Oscillator and X3 Multiplier 1A4A1

The source for the reference signal and the second mixer local oscillator frequency is the 20 MC Oscillator and X3 Multiplier assembly (figure 6-16). This assembly consists of a crystal controlled oscillator Q1, which is a common emitter configuration followed by two isolation stages, Q2 and Q3. Transistor Q3 drives two output stages; one a straight through amplifier, Q4, with a double-tuned output tank circuit driving two 50-ohm outputs, and the other is a frequency tripler with double-tuned input and output tank circuits. Both output stages are common base configurations. Technical specifications for the 20 MC Oscillator and X3 Multiplier assembly are as follows:

Motorola No.	01-23781D01
Frequency	20 mc, ±0.002%, -10 to $+70^{\circ}$C, J2 and J3 60 mc, J1
Output Level	+10 dbm (±3 db), J1 and J2 +1.5 dbm (±1.5 db), J3
Spurious Signals	First and second crystal harmonics >40 db down, others >30 db down Non-harmonic signals >60 db down
Long-term Stability	Better than 1×10^{-6}
Output Impedances	50 (±10) + j0 (±10) ohms
Signal Isolation	>50 db at 10 mc between the X3 output and the 10 mc outputs
Frequency Resetability	Adjustable ±200 cps about the nominal frequency

3.5.15 Loop Filter (APC) 1A6A2

The Loop Filter assembly (figure 6-26) is an R-C phase lag network which provides the four bandwidths required by means of relay switches. The relays switch resistances and capacitances that make up the particular time constant required. The schematic shows all relays in the de-energized state which provides the proper resistances and capacitors for the 12 cps bandwidth position. Technical specifications for the Loop Filter assembly are as follows:

Motorola No.	01-23784D01
Transfer Function:	(all ±10% tolerance time constants)
a. T_1 = 3560 seconds T_2 = 0.300 seconds	$2\beta_{Lo}$ = 5 cps
b. T_1 = 950 seconds T_2 = 0.023 seconds	$2\beta_{Lo}$ = 12 cps
c. T_1 = 119.5 seconds T_2 = 0.0313 seconds	$2\beta_{Lo}$ = 48 cps
d. T_1 = 20.9 seconds T_2 = 9.87×10^{-3} seconds	$2\beta_{Lo}$ = 152 cps
Input Voltage Range	+30 vdc to -30 vdc
Source Impedance	Approximately 40 K ohms
Load Impedance	150 megohms (±50%)
Filter Constant Selection	Output voltage must be greater than 85% of the input with load
Capacitor Discharge	Must contain provisions to remotely discharge the filter capacitor
Signal Terminals	Ungrounded (floating) input and output terminals

3.5.16 5 Channel VCO Assembly 1A6A1

The output of the Loop Filter assembly is a dc phase error analog voltage, which is used to control the 5-Channel VCO assembly (figure 6-25). VCO's 1 through 5 are identical common base oscillators except for the crystal frequencies. Frequency deviation from each crystal frequency is accomplished by varying the dc voltage applied to the PC-116 varactor diodes in the feedback loop of the oscillators. The operating oscillator is selected by applying the 10 vdc collector voltage to that particular oscillator by means of an external switch. The oscillator outputs are tied in parallel and applied to Q6, a common emitter, tuned buffer amplifier, which drives a common base tuned output amplifier, Q7. The output stages are two emitter follower isolation amplifiers, whose inputs are tied together and are driven by Q7. Specifications for the 5-Channel VCO assembly are:

Deviation	150 cps/V ±10% for ±2 vdc, ±900 cps/V (±10%) for ±6.0 vdc
Power Output	10 mw minimum at J3 and J5 1 mw nominal at J4 and J6
VCO Center Frequency	
VCO #1	23.385420 (±146 cps) mc
#2	23.412420 (±146 cps) mc
#3	23.416280 (±146 cps) mc

#4	23.420140 (±146 cps) mc
#5	23.424000 (±146 cps) mc
Linearity	150 cps/V ±10% for ±2.0 vdc in, and ±900 cps/V ±10% for ±6.0 vdc

3.5.17 X3 Frequency Multiplier Assembly 1A4A5

The VCO output signal is used to drive a multiplier chain,which supplies the S-Band local oscillator signal to the first mixer. The X3 multiplication in the X3 Frequency Multiplier assembly (figure 6-20) is accomplished in Q1, a grounded base tripler stage. Coil L1 and capacitor C6 form a series trap to reduce the 46 mc component in the output of the tripler stage. The three remaining amplifier stages are tuned common base amplifiers with sufficient gain to provide the 70 mc output requirements. The network between Q2 and Q3 is the remnant of a phase modulation circuit used only in the X3 Multiplier and Phase Modulator assembly (1A9A2) in a preceding version of this assembly, and it serves no useful function in this assembly. Specifications for the X3 Multiplier assembly are:

Motorola No.	01-23772D01
Frequency	23.4 mc nominal input
Bandwidth	>±4 mc about nominal output
Output Level	+19.5 (±1.5 db) dbm
Impedance, Input	50 ohm, VSWR, <1.2: 1
Impedance, Output	50 (±10) + j0 (±10) ohms
Input Power Level	+10 dbm ±2 db
Spurious Outputs	>30 db below desired output
Saturation	±0.5 db change in output for ±3 db change in input

3.5.18 X32 Frequency Multiplier 1A4A4

The output of the X3 Frequency Multiplier assembly is used to drive the X32 Frequency Multiplier assembly (figure 6-19), giving a total multiplication factor of X96. Transistor Q1 is a X2 frequency multiplier with a pi network matching in the input and a double tuned coupling to Q2. Transistor Q2 is a buffer-limiter common-emitter amplifier,which drives the driver stage Q3. A pi network is used to couple Q3 and the power amplifier stage Q4. The power amplifier is a common base tuned amplifier, which is capable of producing approximately 3 watts output at 140 mc. This output signal drives a X4 multiplier using varactor diode CR1. The output of the power amplifier is tuned and the impedance matched by coils L10 and L11 and capacitors C17 through C22. Coil L12 and capacitor C23 are a series resonant idler circuit tuned to twice the X4 input frequency. Coils L13, L14 and capacitors C46, C24 through C26 provide tuning and impedance matching out of the X4 multiplier. An isolation pad, consisting of R14, R16 and R17, is included between the X4 multiplier and the cavity multiplier to provide a more stable load for the X4 multiplier and a source for the cavity multiplier. The cavity multiplier multiplies by a factor of four, and is driven through the matching network of L15 and C18. Tuned cavity Z1 is the cavity assembly, which is actually a double cavity consisting of an output quarter-wave filter at the output frequency and an idler cavity to increase the multiplication efficiency of the multiplier. Specifications for the X32 Frequency Multiplier assembly are:

Motorola No.	01-23787D01
Frequency	70 mc (approximate)
Multiplication Ratio	32
Power Input	+15 dbm, ±2 db
Power Output	+21.5 dbm minimum
Saturation	±0.5 db change in output with a ±3 db change in input level.
Output Impedance	Minimum power output into a 50(±5) +j0 ohms load only.
Bandwidth, Modulation	200 kc to 3.5 mc @ 3 db down on first sideband for 0.2 radian modulation index
Bandwidth, RF	25 mc minimum @ 3 db
Input Impedance	50 ohms, VSWR <1.2:1 center VSWR <1.5:1 within 3 db bandwidth
Spurious Signals	>40 db below desired output

3.5.19 AGC Amplifier and Filter Assembly 1A5A1

The dc signal derived from the AGC 10 MC Loop Phase Detector assembly is used to supply the gain correction voltage for the 50 MC IF Amplifier and Second Mixer assembly. This correction voltage is first conditioned by the AGC Amplifier and Filter assembly (figure 6-22). The filter is an active type using a Philbrick P2 operational amplifier and a P5 booster amplifier with appropriate R-C feedback to provide the bandwidths required. Bandwidth selection is performed with relays which are controlled by the front panel switch. Much of the auxiliary circuitry of the AGC Amplifier and Filter assembly is not used in this application. Manual gain control is provided for by connecting an external variable resistor from J3 to J4. This variable resistor applies a portion, determined by the variable resistance, of the voltage across VR2 to the input to the amplifier input. Resistors R1 and R5 are zero and balance controls. The output of the filter is monitored by measuring the booster amplifier voltage output. This measuring device is a front panel meter entitled SIGNAL STRENGTH and indicates the voltage feedback to the 50 MC IF Amplifier and Second Mixer assembly. Specifications for the AGC Loop Filter assembly are:

Motorola No.	01-23610D01
Gain	100 ±1%
Time Constants	τ_1 = 3.8 (±10%) seconds
	τ_2 = 0.38 (±10%) second
	τ_3 = 0.1 (±10%) second
Input Impedance	>500K
Source Impedance	40K maximum

Input Voltage Range	+0.8 to +1.5 vdc, and 35 Vp-p noise
Bias Adjustment	+0.25 to 1.5 vdc at the signal input
Output Impedance	<300 ohms @ dc
Output Voltage Range	0 to -10 vdc (linear ±10%) with 6K load
Output Voltage Limiting	+1.25 to -11 vdc
DC Drift and Noise Error	<1 mv referred to the input @ +1 vdc in and bias adjusted for -2 vdc output
Amplifier Bandpass	dc to 1 kc minimum, roll off 12 db/ octave @ -0.5 to -10 vdc

3.6 FREQUENCY CONVERTER 1A8

The Frequency Converter (figure 6-32) contains a plug-in 5-Channel Oscillator assembly (1A8A1), which provides a minimum of 5 mw output at 181.9 mc. This output is applied through a resistor network to the Mixer-Filter assembly (1A8A2) and provides a nominal 1 mw of conversion oscillator power. The 2116.7 mc input signal is applied to the RF mixer. The RF mixer output is tuned to the sum frequency of 2298 mc, which is the desired output. A 6 db attenuator at the input ensures a satisfactory input voltage standing wave ratio.

3.6.1 5-Channel Oscillator 1A8A1

The 5-Channel Oscillator assembly (Motorola P/N 01-20246E01) schematic is shown in figure 6-33. All the crystal frequencies for each assembly are listed on the schematic diagram. A front panel FREQUENCY SELECTOR switch is used to select Oscillator No. 1 through 5. The oscillator output is fed to a buffer stage followed by two stages of X2 multiplication to obtain an output frequency which is four times the selected oscillator frequency.

Summary of specifications:

Frequencies	(See table II-7.)
Output Level	5 mw (minimum)
Output Impedance	50 ohms ±10%

3.6.2 Mixer-Filter 1A8A2

The schematic diagram of the Mixer-Filter assembly is shown in figure 6-34. The mixer accepts the 2116 mc frequency of the 2116 MC Test Transmitter 1A9 and one of the output frequencies from the 5-Channel Oscillator assembly (1A8A1). The conversion is accomplished by a diode mixer and a cavity tuned to the sum of the two input frequencies (2297 mc).

Summary of specifications:

Input Frequencies	(See table II-7.)
Input Power Level	1 mw
Output Frequency	(See table II-7.)
Output Power Level	-60 dbm

Bandwidth, 3 db	12 mc (minimum)
Conversion Loss	18 db (maximum)

3.7 TEST TRANSMITTER 1A9

The Test Transmitter (figure 6-35) contains five Voltage Controlled Oscillators (1A9A1), a X3 Multiplier and Phase Modulator (1A9A2), a X32 Frequency Multiplier (1A9A3), a Voltage-Controlled Oscillator bias assembly and RF couplers. Operating controls are mounted on the front panel. Only one of the Voltage-Controlled Oscillators (1A9A1) is used at a time; the desired output frequency determining the active oscillator.

3.7.1 5-Channel Voltage-Controlled Oscillator (VCO) 1A9A1

Figure 6-25 is a schematic diagram of the 5-Channel Voltage Controlled Oscillator assembly. This oscillator is a plug-in assembly containing five 22 mc crystal controlled oscillators, an isolation amplifier, a driver amplifier, and two emitter follower output amplifiers. The VCO frequency is controlled by the VCO Bias control. The VCO SELECTOR switch is located on the front panel. The VCO SELECTOR switch applies a regulated +10 volts to the desired VCO. A disabling circuit prevents the operation of the amplifier,Q6, while allowing the oscillator to continue to operate. The disabling ability allows zero adjustment of an external power meter. Technical characteristics for the 5-Channel Voltage-Controlled Oscillator assembly are the same as for the Test Receiver 5-Channel VCO (1A6A1). Refer to paragraph 3.5.16 for the technical characteristics of the assembly.

3.7.2 X3 Multiplier and Phase Modulator 1A9A2

Figure 6-36 shows a schematic diagram of the X3 Multiplier and Phase Modulator assembly. This assembly consists of a conventional grounded base X3 multiplier, a tuned isolation amplifier, a voltage sensitive variable reactance phase modulator, another isolation driver, and an output stage. Coil L1 and capacitor C6 are provided to trap the unwanted second harmonic in the multiplier output. The phase modulator reactance varies with the voltage, applied to J2 or J3, due to the capacitance variation of the PC113 varactors. Technical specifications for the X3 Multiplier and Phase Modulator assembly are as follows:

Motorola No.	01-23760D01
Frequency	22 mc input, 66 mc output nominal
COMMAND MODULATION	
Sensitivity	0.031 (±0.0015) radians/volt @ 10 kc
Linearity	+0.5 db from dc to 50 kc
Maximum Deviation Capability	0.1 radian peak maximum @ 10 kc
Frequency Response	Dc to 100 kc @ 3 db

Modulation Input Impedance	>2000 ohms @ dc to 100 kc
Symmetry	Peak positive and peak negative phase deviation within 5% @ 10 kc
RANGE MODULATION	
Sensitivity	0.165 (±0.008) radians/volt @ 500 kc
Linearity	±1 db ± dc to 1 mc
Modulation Input Voltage	-0.55 (±0.1) to 1.35 (±0.1) volts with a rectangular waveform
Modulation Input Impedance	50 ohms, VSWR <1.3 @ dc to 3 mc
Output Power Level	19.5 (±1.5) dbm
Output Bandwidth	>±4 mc @ 3 db
RF Input Impedance	50 ohms, VSWR <1.2:1
Output Impedance	50 (±10) + j0 (±10) ohms
Input Power Level	+10 dbm (±2 db)
Incidental Amplitude Modulation	<±1 db about carrier from dc to 2 mc measured at maximum phase deviation
Spurious Outputs	>30 db below desired output
Power Gain Variation	<±1 db

3.7.3 X32 Frequency Multiplier 1A9A3

Figure 6-19 is a schematic diagram for the transmitter X32 Frequency Multiplier assembly. Transistor Q1 is a X2 frequency multiplier with a pi network matching in the input and a double tuned coupling to Q2. Transistor Q2 is a buffer-limiter amplifier, which drives Q3 at a constant power level. A pi network is used to couple Q3 and the power amplifier Q4. The power amplifier is a common base tuned amplifier, which is capable of producing approximately three watts output at 132 mc. This signal drives a X4 multiplier using varactor diode CR1. The output of the power amplifier is tuned and the impedances matched by L10 and L11 and C17 through C22. Coil L12 and capacitor C23 are a series resonant idler circuit tuned to twice the X4 input frequency. Coils L13 and L14 and capacitors C46 and C24 through C26 provide tuning and impedance matching out of the X4 multiplier. An isolation pad, consisting of R14, R16, and R17, is included between the X4 and the cavity multiplier to provide a more stable load for the X4 and a source for the cavity multiplier. The cavity multiplier (by a factor of four) is driven through the matching network of L15 and C18. Tuned cavity Z1 is the cavity assembly, which is actually a double cavity consisting of an output quarter-wave filter at the output frequency, and an idler cavity to increase the multiplication efficiency of the multiplier. Technical specifications for the X32 Frequency Multiplier assembly are:

Motorola No.	01-23786D01
Frequency	66 mc approximate
Multiplication Ratio	32

Power Input	+15 dbm, ±2 db
Power Output	+21.5 dbm minimum
Saturation	±0.5 db change in output with a ±3 db change in input level
Output Impedance	Minimum power output with a 50(±5) + j0 ±(5) ohms load only
Bandwidth, Modulation	200 kc to 3.5 mc @ 3 db down on first sideband for 0.2 radian modulation index
Bandwidth, RF	25 mc minimum @ 3 db
Input Impedance	50 ohms, VSWR <1.2:1 center frequency VSWR <1.5:1 within 3 db bandwidth
Spurious Signals	>40 db below desired output

The output of the X32 Frequency Multiplier assembly is isolated from the output couplers and attenuators by an isolator, AT-1. The isolator is a standard model manufactured by Rantec Corporation. The technical characteristics of the isolator are as follows:

Model No.	CST-11-3
Frequency	2116 mc nominal (1900-2700 mc)
Isolation	20 db minimum
Insertion Loss	0.4 db maximum
VSWR	1.25:1 maximum
Power Handling	50 watts maximum

3.7.4 VCO Bias Assembly

The VCO Bias Assembly is built on a terminal board in the drawer. The oscillator selection and variable frequency voltage for the 22 mc VCO is provided for in the VCO Bias Assembly. The VCO voltage is monitored by a front panel VCO BIAS meter. The TRANSMITTER DISABLE switch is located in the bias assembly compartment. Figure 6-35 shows the VCO Bias Assembly (part of Test Transmitter drawer). Extensive filtering is used in the bias assembly compartment to comply with the radiated interference specification for the transmitter. The variable frequency control is accomplished by R3, a ten-turn potentiometer, which varies the varactor bias voltage in the 22 mc VCO. The TRANSMITTER DISABLE switch removes the power supply, +15 vdc, to the 22 mc VCO isolation amplifier.

3.7.5 Calibration and Monitoring

In addition to the front and rear panel 22 mc outputs, the Test Transmitter also provides three other outputs. These outputs are the front and rear panel outputs at 2116 mc, and the power monitor output, as shown in figure 6-35. The front panel RF signal is attenuated by approximately 60 db by the two 20 db couplers, 18 to 20 db insertion loss in the PRD attenuator and the remainder in the cable and connector losses. This results in an approximately -40 dbm output signal level with the step attenuator and the calibrated attenuator set to zero. Accurate measurement of the minimum insertion loss of the variable attenuators, directional couplers and cabling inserted between the power monitoring point and the transmitter output, permits percise output power level settings.

3.7.6 Calibration Curves

The calibration curves for the PRD-198 attenuator are plotted in attenuation in db above insertion loss as a function of dial setting in degrees. These calibration curves as supplied by the manufacturer for the specific frequency differ to such an extent that a single specification for applying the graduations to the General Radio dial cannot be developed. Each transmitter (and each receiver) attenuator has a different calibration on the dial and, therefore, the units are not interchangeable. The graduations applied to the dials of both receiver and transmitter are shown in Table III-1.

TABLE III-1. ATTENUATOR DIAL SPACING IN DEGREES PER DB

Serial No.	0-10 DB	10-20 DB	20-30 DB	30-100DB
SN131T (2116 mc)	$0^{o}52'30''$	$1^{o}15'00''$	$1^{o}20'40''$	$1^{o}21'30''$
SN130R (2298 mc)	$0^{o}50'15''$	$1^{o}17'00''$	$1^{o}20'10''$	$1^{o}21'50''$
SN132T (2116 mc)	$0^{o}50'40''$	$1^{o}14'10''$	$1^{o}20'10''$	$1^{o}21'40''$
SN133T (2116 mc)	$0^{o}47'50''$	$1^{o}15'50''$	$1^{o}21'00''$	$1^{o}21'30''$
SN129R (2298 mc)	$0^{o}47'45''$	$1^{o}13'20''$	$1^{o}21'0''$	$1^{o}22'15''$

Graduated dial marking lengths indicate ½, 1, 5 and 10 db calibrations. The maximum error occurs in the nonlinear portion of the attenuation curve between 0 and 10 db. At 6 db, the error is approximately 0.5 db. Over the linear portion of the curve, the maximum error is less than 0.1 db. The serial number of the attenuator for which the dial is calibrated is engraved on the dial. A "T" or "R" following this serial number indicates attenuator calibration for either the transmitter or receiver frequency.

3.7.7 Rear Panel RF Output

The rear panel RF output is attenuated 70 db in two 20 db directional couplers and a 30 db fixed attenuator. This results in a nominal signal level of -50 dbm available at the rear panel to enable monitoring by a Read-Write-Verify (RWV) Receiver.

3.7.8 Power Monitor Output

The power monitor output enables connection of an external power meter to the Hewlett-Packard 478A thermistor mount in the Test Transmitter. The self-contained thermistor output passes through a single section, high frequency, low-pass filter which is part of the transmitter chassis. This filter attenuates the 2116 mc RF signal by an additional 60 db, but has a negligible insertion loss to the power meter signal. The reference power level measured at the power monitor is a minimum of 1 mw.

3.7.9 Filtering and Shielding

Figure 6-35 is an interconnection diagram for the transmitter and shows the power and signal filtering. The individual assemblies contain filtering which attenuates all RF signals generated in the assemblies to a level less than 10 micro-volts (-87 dbm). This -87 dbm signal level is isolated from the low level output at the front panel by compartmentalization. An estimate of indicated signal levels contained in these compartments is as follows:

Transmitter assembly compartment	less than -80 dbm
Transmitter attenuator section	less than -120 dbm
RF output and power monitor section	less than -150 dbm

The attenuator control shafts enter the front panel through waveguide beyond cutoff tubing. The calculated value of attenuation for the three-inch tube is 192 db. Since the tube enters an area which is estimated at -120 dbm, an adequate safety factor is assured.

3.8 RANGING CONVERSION UNIT 1A10

The Ranging Conversion Unit (figure 6-37) consists of three assemblies, a 10 MC Phase Shifter (1A10A1), a 10 MC Phase Switch (1A10A2) and a 10 MC Balanced Detector (1A10A3).

3.8.1 10 MC Phase Shifter 1A10A1

The 10 MC Phase Shifter assembly is included in the Ranging Conversion Unit to allow the 498 kc output phase to be adjusted for proper phase relationship with the external ranging equipment. The technical specifications and circuit description for the identical unit in the Test Receiver (assembly 1A5A3) are given in paragraph 3.5.12.

3.8.2 10 MC Phase Switch 1A10A2

The schematic for the 10 MC Phase Switch assembly is shown in figure 6-38. The circuit is essentially a push-push amplifier with the inputs driven 180° apart in phase and the outputs are in parallel. The two amplifiers are switched on or off, by Q1 and Q4, alternately by the PN-$\overline{PN}$ square wave input modulation signals. When one RF amplifier is on the other is off, thus producing the 180° modulated output signal. The modulation frequency is a 498 kc square wave. Technical specifications for the 10 MC Phase Switch assembly are as follows.

Motorola No.	01-23840D01
Frequency	10 mc
Input Impedance	50(±5) + j0 (±5) ohms
Input Impedance	50 ohms, VSWR <1.2:1 maximum 1.5:1 within 3 db bandwidth
Input Level (RF)	10 (±3) dbm
Output Level (RF)	5 (±1) dbm @ +7 dbm input
Modulation Signal:	
Amplitude	0.8V p-p
Polarity	-0.6 (±0.1 to -1.35 (±0.1) assertion -1.35 (±0.1 to -0.6 (±0.1) negation
Frequency	498 kc
Pulse & Decay Time	0.03 microseconds
Balance	Reference signals > 30 db below the first order sideband.
Spurious Signals	All signals >35 db below the desired output signal.

3.8.3 10 MC Balanced Detector 1A10A3

The schematic diagram for the 10 MC Balanced Detector assembly is shown in figure 6-39. The phase modulated signal from the 10 MC Phase Switch (1A10A2) at J1 is amplified by two cascode amplifier stages, Q1 through Q4. Transistor Q5 is an emitter follower stage, which provides the signal injection to the balanced diode detector. The output is monitored by TP1 and TP2, which are on opposite sides of a 10 mc rejection filter. The 498 kc signal from the detector is filtered and amplified by Q6 and Q7 and the associated circuitry. Transistor Q7 is an emitter follower amplifier, which provides the output level and impedance matching required. Technical specifications for the 10 MC Balanced Detector assembly are as follows:

Motorola No.	01-23845D01
Frequency	10 mc
Input Signal Level	-60 dbm maximum
Output Amplifier Response	±10 kc minimum @ 3 db, 498.047 kc center frequency
Conversion Gain	19 (±3) db
Noise Figure	13 db maximum
Bandwidth	>±2 mc, <2.5 mc @ 10 mc center frequency
Output Impedance	50 (±10) + j0 (±10) ohms
Input Impedance	50 ohms, VSWR 1.2:1 maximum

VOLUME 1

SECTION IV

DRAWER AND ASSEMBLY ALIGNMENT AND CHECKOUT PROCEDURES

4.1 GENERAL

This section describes the alignment and checkout procedures for each drawer and assembly in the GSE. All schematic diagrams used with the procedures throughout this section are located in section VI. All assembly alignment procedures outlined in this section are referenced to the proper assembly alignment procedure that is bound in Volume 2 or Volume 3.

NOTE

> Locate the desired assembly alignment procedure by referring to the table of contents and indexed tabs in each separately bound volume of test and alignment procedures.

To ensure maximum performance of each drawer, each assembly should be realigned after repairs or parts replacement have been accomplished on the assembly.

4.2 TELEMETRY NARROW BAND SUBSYSTEM 1A2, ALIGNMENT

This alignment and test procedure covers the tests required for the Telemetry Narrow Band Subsystem, Motorola Part No. 01-25245E. Refer to figure 6-5 for a schematic diagram of the drawer. This alignment and checkout procedure assumes the assembly checkout procedures outlined in paragraphs 4.3 through 4.7 were completed prior to the alignment of the drawer in the following procedure.

4.2.1 Test Equipment Required

The following test equipment, or equivalent, is required to align and test the Telemetry Narrow Band Subsystem.

Signal Generator, HP-608C
Test Receiver, 1A6
Frequency Counter, HP-524C
AC VTVM, HP-400D
Spectrum Analyzer, Panoramic SPA-4a
Power Supply, ±15 vdc

4.2.2 Alignment

a. Interconnect the system and lock the Test Receiver on the incoming signal from the signal generator.

b. Connect a VTVM to the output of the 10 MC Phase Detector assembly at 1A2A3-J3 (disconnect cable W7).

c. Adjust the dial on the 10 MC Phase Shifter assembly (1A2A5) to obtain 0 vdc on the VTVM.

d. Disconnect the VTVM and reconnect cable W7 on the assembly.

4.2.3 Test Requirements

4.2.3.1 Bandwidth Selector

a. Connect a HP-606A signal generator to jack 1A2J4 (rear panel).
b. Set signal generator output signal to 10.000 mc and -65 dbm.
c. Set variable attenuator to 0 db.
d. Connect a spectrum analyzer to jack 1A2J6.
e. Set the BANDWIDTH switch to the 4.5 KC position.
f. Measure the 1 db bandwidth at jack 1A2J6 (limit: 4.5 kc minimum).
g. Set the BANDWIDTH switch to the 20 KC position.
h. Measure the 1 db bandwidth at jack 1A2J6 (limit: 20 kc minimum).
i. Set the BANDWIDTH switch to the 420 KC position.
j. Measure the 1 db bandwidth at jack 1A2J6 (limit: 420 kc minimum).
k. Set the BANDWIDTH switch to the 3.3 MC position.
l. Measure the 3 db bandwidth at jack 1A2J6 (limit: ±8 mc minimum ±9 mc maximum).

4.2.3.2 Narrow Band Telemetry Channel Outputs

a. Connect the test equipment as described in paragraph 4.2.3.1.
b. Connect the 10 mc reference signal from the Test Receiver to the 10 mc reference input of jack 1A2J5.
c. Connect an oscilloscope to the TLM DPE output at 1A2J1.
d. Observe the oscilloscope and vary the input frequency at the 10 mc reference input at 1A2J5 for an output beat note of approximately 1000 cps.
e. Connect an AC VTVM and a 50 ohm load to jack 1A2J2.
f. Measure the output amplitude (limit: 0 dbm nominal).
g. Verify that the amplitude of the output signal at 1A2J1 and 1A2J3 are identical outputs to the output of 1A2J2.

4.3 TELEMETRY BANDPASS FILTER 1A2A1, ALIGNMENT

This alignment and test procedure covers the tests required for the Telemetry Bandpass Filter, Motorola Part No. 01-23800D01. Refer to figure 6-6 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.4 NARROW BAND 10 MC IF AMPLIFIER 1A2A2, ALIGNMENT

This alignment and test procedure covers the tests required for the Narrow Band 10 MC IF Amplifier, Part No. 01-24272D01. Refer to figure 6-7 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.5 10 MC PHASE DETECTOR 1A2A3, ALIGNMENT

This alignment and test procedure covers the tests required for the 10 MC Phase Detector, Motorola Part No. 01-24273D01. Refer to figure 6-8 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.6 VIDEO AMPLIFIER 1A2A4, ALIGNMENT

This alignment and test procedure covers the tests required for the Video Amplifier, Motorola Part No. 01-23853D01. Refer to figure 6-9 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.7 10 MC PHASE SHIFTER 1A2A5, ALIGNMENT

This alignment and test procedure covers the tests required for the 10 MC Phase Shifter, Motorola Part No. 01-23793D01. Refer to figure 6-10 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.8 TELEMETRY WIDE BAND SUBSYSTEM 1A3, ALIGNMENT

This alignment and test procedure covers the tests required for the Telemetry Wide Band Subsystem, Motorola Part No. 01-25246E. Refer to figure 6-11 for a schematic diagram of the drawer. This alignment and checkout procedure assumes the assembly checkout procedures outlined in paragraphs 4.9 through 4.11 were completed prior to the alignment of the drawer in the following procedure.

4.8.1 Test Equipment Required

The following test equipment, or equivalent, is required to align and test the Telemetry Wide Band Subsystem.

Signal Generator, HP-606A
Spectrum Analyzer, Panoramic SPA-4a
Test Receiver, Drawer 1A6
AC VTVM, HP-400D
Frequency Counter, HP-524C

4.8.2 Alignment

No alignment is required for the drawer.

4.8.3 Test Requirements

4.8.3.1 Bandwidth Selector

a. Connect a HP-606A signal generator to jack 1A3J4 (rear panel).
b. Set signal generator output signal to 10.000 mc and -65 dbm.
c. Connect a frequency counter to jack 1A3J1 (front panel).
d. Connect a spectrum analyzer to jack 1A3J2.

e. Set the BANDWIDTH switch to the 4.5 KC position.

f. Set the ATTENUATION DB switches to the 0 DB positions.

g. Vary the signal generator output frequency while observing the spectrum analyzer and frequency counter for both the upper and lower 1 DB frequencies.

h. Determine the bandwidth by subtracting the two frequencies. The bandwidth should be as follows. Also, determine the bandwidth of the 20 KC, 420 KC, and 3.3 MC positions of the BANDWIDTH switch.

BANDWIDTH Switch Position	1 DB Bandwidth Tolerance
4.5 KC	4.5 kc minimum
20 KC	20 kc minimum
420 KC	420 kc minimum
3.3 MC	3.3 mc minimum

4.8.3.2 Wide Band Telemetry Channel Outputs (NON-GSDS and TLM)

a. Connect the test equipment as described in paragraph 4.8.3.1.

b. Set signal generator output signal to 10.000 mc and -65 dbm.

c. Measure the amplitude of the output signal at 1A3J2 on the spectrum analyzer (limit: -7 dbm ±1.5 db).

d. Repeat the above procedure with the spectrum analyzer connected to 1A3J1.

4.8.3.3 Wave Analyzer Input (1A8J3 and J7)

a. Connect the wide band telemetry output signal from the Test Receiver to jack 1A3J4 (WB IN).

b. Lock the Test Receiver to the output signal from the Test Transmitter. The locked condition may be observed with an oscilloscope connected at the DPE jack on 1A5J2.

c. Connect the spectrum analyzer to the NON-GSDS output (1A3J1).

d. Set the variable attenuators for a -7 dbm signal output at 1A3J1.

e. Connect a frequency counter to the wave analyzer input (1A3J3).

f. Verify that the output frequency at 1A3J3 is 20 kc (nominal).

g. Verify that the output frequencies at 1A3J6 and 1A3J3 are identical frequencies.

4.8.3.4 Wave Analyzer Input Level

a. Connect the test equipment as described in paragraph 4.8.3.1.

b. Connect an AC VTVM to the wave analyzer input (1A3J3).

c. Measure the output voltage at 1A3J3 (limit: 3 volts ±0.3 V_{RMS}).

d. Verify that the output voltage at 1A3J6 is identical to the voltage at 1A3J3.

4.8.3.5 Spectrum Analyzer Input

a. Connect the test equipment as described in paragraph 4.8.3.1.

b. Lock the Test Receiver to the output signal from the Test Transmitter.

c. Connect the spectrum analyzer to the 10 MC WB OUT input (1A3J1).
d. Adjust the variable attenuators for -7 dbm at 1A3J1.
e. Connect the 20 MC input from 1A3J7 to 1A4J17.
f. Set the output signal of the signal generator to 20 mc and 0 dbm.
g. Connect the spectrum analyzer to the input at 1A3J5.
h. Measure the output signal level at 1A3J7 (limit: -42 dbm nominal).

4.9 TELEMETRY BANDPASS FILTER 1A3A1, ALIGNMENT

Alignment of this assembly is performed in the same manner as the alignment of Telemetry Bandpass Filter 1A2A1 (located in Volume 2). Refer to figure 6-6 for a schematic diagram of the assembly.

4.10 10.02 MC MIXER-OSCILLATOR 1A3A2, ALIGNMENT

This alignment and test procedure covers the tests required for the 10.02 MC Mixer-Oscillator, Motorola Part No. 01-23844D. Refer to figure 6-13 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.11 WIDE BAND 10 MC IF AMPLIFIER 1A3A3, ALIGNMENT

This alignment and test procedure covers the test required for the Wide Band 10 MC IF Amplifier, Motorola Part No. 01-23795D01. Refer to figure 6-12 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.12 TEST RECEIVER DRAWERS 1A4 THROUGH 1A7, ALIGNMENT

The Test Receiver alignment procedure is performed with the four Test Receiver drawers (1A4 through 1A7) mounted and interconnected in the GSE Rack. The procedure in the following paragraphs covers the complete drawers listed as follows.

Name	Drawer	Figure No.	Schematic Diagram
Test Receiver, Block Diagram	1A4 thru 1A7	6-14	69-25443E
Test Receiver, Part One	1A4	6-15	63-25447E
Test Receiver, Part Two	1A5	6-21	63-25448E
Test Receiver, Part Three	1A6	6-24	63-25449E
Test Receiver, Part Four	1A7	6-27	63-25450E

This alignment and checkout procedure assumes the assembly checkout procedures outlined in paragraphs 4.13 through 4.27 were completed prior to the alignment of the four drawers in the following procedure.

4.12.1 Test Equipment Required

The following test equipment, or equivalent, is required to align and test the Test Receiver.

Power Meter, HP-430C
Thermistor Mount, HP-477B
Frequency Counter, HP-524C
Oscilloscope, Tektronix Type 543A
Signal Generator, HP-616B
Function Generator, HP-202A
Spectrum Analyzer, Panoramic SPA-4a
VTVM, HP-410B
VTVM, HP-412A
Test Transmitter, 1A9
Frequency Converter, 1A8

4.12.2 Initial Alignment

4.12.2.1 Power Supplies

Adjust the power supplies as follows.

a. Adjust the +15 vdc as indicated by panel meter.
b. Adjust the -15 vdc as indicated by panel meter.
c. Adjust the +28 vdc as indicated by panel meter.
d. Adjust the -28 vdc as indicated by panel meter.

4.12.2.2 Local Oscillator Power Measurement

With a power meter connected at the Mixer-Preamplifier assembly (J2, 1A7A1), measure the amplitude of the local oscillator (limit: 0 dbm ±3 db).

4.12.2.3 Input Attenuation and Preselector Insertion Loss

a. Connect the HP-616B signal generator to the 2298 MC input (1A7J1).
b. Set the signal generator to 2298 mc and -40 dbm.
c. Connect the spectrum analyzer to the signal input of the Mixer-Preamplifier assembly (1A7A1, J1).
d. Set the variable attenuator to zero.
e. Measure the insertion loss (limit: 23 db maximum).

4.12.2.4 Crystal Current

With no signal input, measure the crystal current at TP1 and TP2 (limit: 0.7 to 0.8 ma).

4.12.3 Test Requirements

4.12.3.1 10 MC Isolation and Distribution Amplifier Outputs (Reference)

a. Connect a power meter to jack 1A4J8.
b. Terminate jacks 1A4J1, 1A4J3, 1A4J4, and 1A4J5 with a 50 ohm termination.
c. Measure the power output at jack 1A4J8 (limit: 10 dbm ±2 db).
d. Repeat the above procedure to determine the power output at 1A4J1, 1A4J3, 1A4J4, and 1A4J5.

e. Connect a frequency counter to jack 1A4J8.

f. Measure the output frequency at jack 1A4J8 (limit: 10 mc ±100 cps).

g. Verify the output frequency at 1A4J1, 1A4J3, 1A4J4, and 1A4J5 are the same frequency as the output frequency at 1A4J8.

4.12.3.2 VCO Tuning Range

4.12.3.2.1 Power Output and Center Frequency

a. Set the LOOP BW CPS switch to the OPEN position.

b. Set the FINE TUNE control to 5.00.

c. Connect a VTVM to the center arm of the FINE TUNE control, and adjust the trimpot for 10 vdc at the center arm.

d. Connect a power meter to the VCO output at 1A6J2.

e. Measure the power output (limit: 10 mw minimum).

f. Repeat the procedure in steps (d) and (e) for VCO SELECTOR switch positions 1 through 5.

g. Connect the power meter to the VCO output at 1A6J5.

h. Measure the power output for VCO SELECTOR switch positions 1 through 5. (limit: 10 mw minimum).

i. Connect a frequency counter to the VCO frequency output at 1A6J1 (front panel).

j. Verify that the frequencies are within the limits specified as follows.

VCO SELECTOR Switch Position	VCO Output Frequency (MC)
1	23.385420 ±146 cps
2	23.412420 ±146 cps
3	23.416280 ±146 cps
4	23.420140 ±146 cps
5	23.424000 ±146 cps

4.12.3.2.2 VCO Linearity

a. With the VCO SELECTOR switch placed in the No. 1 position, jacks J5 and J9 terminated with 50 ohm terminations, and a frequency counter connected to J1, vary the FINE TUNE control from 1.0 to -10 and measure the output frequencies at 0.0, 1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, and 10.0.

b. Plot the results of step (a) on a graph. Figure 4-1 is a typical graph (limit: VCO frequency shall not deviate more than ±900 cps from the center frequency).

c. Repeat the procedure outlined in steps (a) and (b) for VCO SELECTOR switch positions 2 through 5.

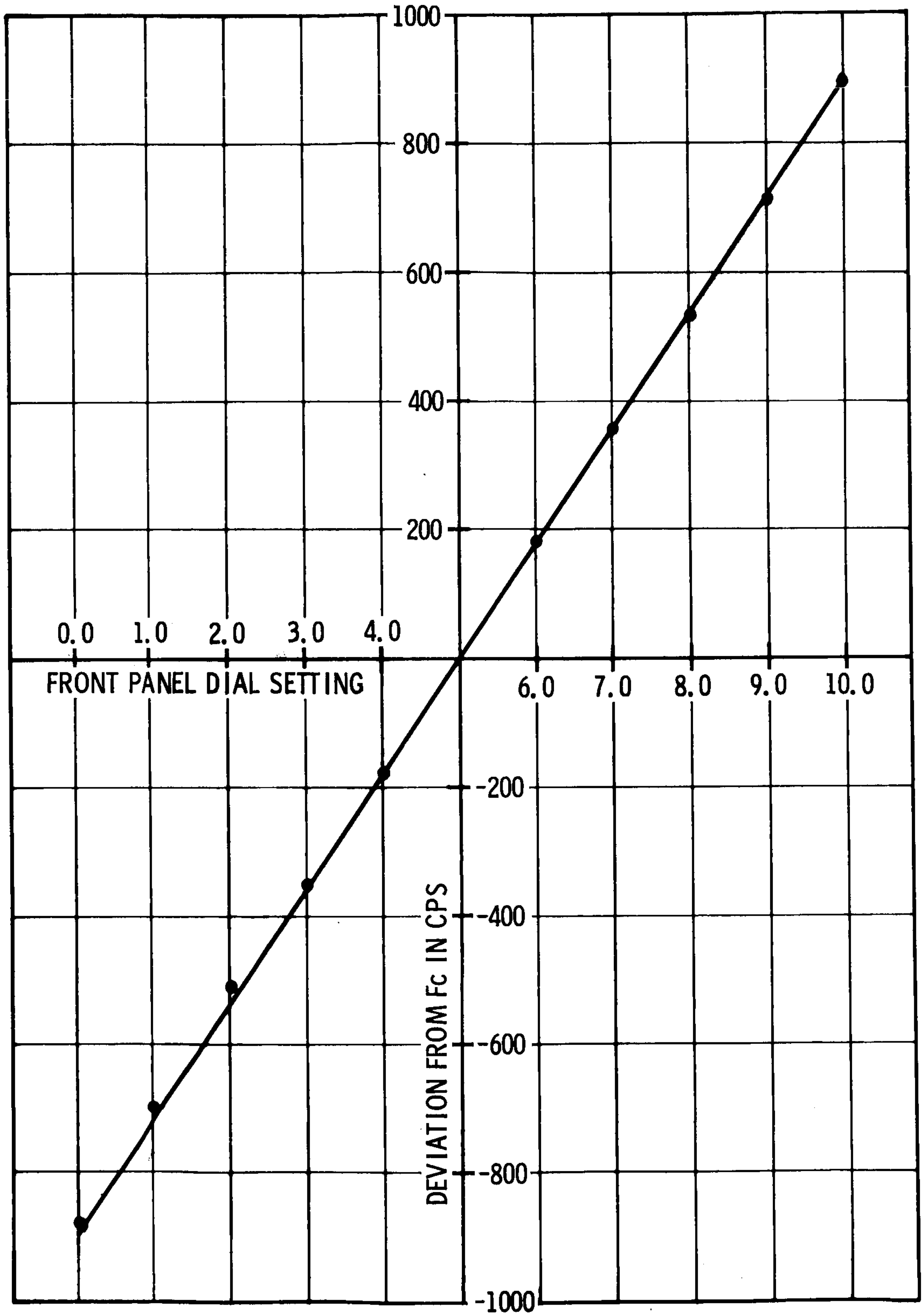


Figure 4-1. Typical VCO Linearity Curve for Test Receiver

4.12.3.3 Predetection Bandwidth

a. Connect the Test Transmitter and Frequency Converter to the Test Receiver as the signal source.
b. Set all variable attenuators to zero.
c. Obtain a linear output signal from the 10 MC IF Amplifier assembly (1A7A4) at J2 by switching the MGC/AGC switch to the MGC position, and adjusting the MGC control until a signal is obtained on the spectrum analyzer in the linear area of the 10 MC IF Amplifier assembly.
d. While monitoring the Test Transmitter VCO frequency, vary the FINE TUNE control until an upper and lower 3 db frequency is obtained on the spectrum analyzer.
e. Multiply the difference of the two frequencies by 96 (limit: 2 kc ±180 cps).

4.12.3.4 Tracking Loop Bandwidth

a. Lock the Test Receiver to the output signal from the Test Transmitter under strong signal conditions.
b. Connect an AC VTVM to the DPE output at J2 on the Test Receiver.
c. Connect a function generator to the ranging input at J4 on the Test Transmitter.
d. Set the function generator signal level at the beginning of each test to obtain approximately 3 VRMS modulation level at the high frequency reference for each response curve.

4.12.3.5 Signal Strength Calibration and Output Variation with Signal Level

a. Connect the Test Transmitter and Frequency Converter to the Test Receiver as the signal source.
b. Apply a nominal -40 dbm signal to the Test Receiver.
c. Measure the exact amplitude of the input signal to the Test Receiver.
d. Observe the SIGNAL STRENGTH meter readings for 5, 12, 48, and 152 CPS BANDWIDTH switch positions, and the -65 dbm ranging output amplitude (1A7J5) vs attenuator dial settings.
e. Verify that the signals at 1A7J3 and 1A7J4 have identical outputs as 1A7A5.

4.12.3.6 Residual Phase Modulation

a. Connect the Test Transmitter and Frequency Converter to the Test Receiver as the signal source.
b. Observe the Test Receiver direct phase error (DPE) output on an oscilloscope, and calibrate the oscilloscope in degrees with the peak S-curve.
c. Lock the loop and measure noise in degrees peak on the oscilloscope with the LOOP BW switch placed in the 5 CPS position (8 degrees peak maximum).

d. Repeat the procedure in steps (b) and (c) for all five VCO switch positions.

4.13 20 MC OSCILLATOR AND X3 MULTIPLIER 1A4A1, ALIGNMENT

This alignment and test procedure covers the tests required for the 20 MC Oscillator and X3 Multiplier, Motorola Part No. 01-23781D01. Refer to figure 6-16 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.14 X1/2 FREQUENCY MULTIPLIER 1A4A2, ALIGNMENT

This alignment and test procedure covers the tests required for the X1/2 Frequency Multiplier, Motorola Part No. 01-21456C01. Refer to figure 6-17 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.15 10 MC ISOLATION AND DISTRIBUTION AMPLIFIER 1A4A3, ALIGNMENT

This alignment and test procedure covers the tests required for the 10 MC Isolation and Distribution Amplifier, Motorola Part No. 01-23778D01. Refer to figure 6-18 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.16 X32 FREQUENCY MULTIPLIER 1A4A4, ALIGNMENT

This alignment and test procedure covers the tests required for the X32 Frequency Multiplier, Motorola Part No. 01-23786D01. Refer to figure 6-19 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.17 X3 FREQUENCY MULTIPLIER 1A4A5, ALIGNMENT

This alignment and test procedure is a part of the alignment procedure for the X3 Multiplier and Phase Modulator 1A9A2 (located in Volume 3). Refer to figure 6-20 for a schematic diagram of the assembly.

4.18 AGC AMPLIFIER AND FILTER 1A5A1, ALIGNMENT

This alignment and test procedure covers the tests required for the AGC Amplifier and Filter, Motorola Part No. 01-23610D01. Refer to figure 6-22 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.19 10 MC PHASE DETECTOR 1A5A2, ALIGNMENT

This alignment and test procedure covers the tests required for the 10 MC Phase Detector, Motorola Part No. 01-21432C01. Refer to figure 6-23 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.20 10 MC PHASE SHIFTER 1A5A3, ALIGNMENT

Alignment of this assembly is performed in the same manner as the alignment of 10 MC Phase Shifter 1A2A5 (located in Volume 2). Refer to figure 6-10 for a schematic diagram of the assembly.

4.21 10 MC PHASE DETECTOR 1A5A4, ALIGNMENT

Alignment of this assembly is performed in the same manner as the alignment of 10 MC Phase Detector 1A5A2 (located in Volume 2). Refer to figure 6-23 for a schematic diagram of the assembly.

4.22 5-CHANNEL RECEIVER VCO 1A6A1, ALIGNMENT

This alignment and test procedure covers the tests required for the 5-Channel Receiver VCO, Motorola Part No. 01-25260E01. Refer to figure 6-25 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.23 LOOP FILTER 1A6A2, ALIGNMENT

This alignment and test procedure covers the tests required for the Loop Filter, Motorola Part No. 01-23784D. Refer to figure 6-26 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.24 BALANCED MIXER-PREAMPLIFIER 1A7A1, ALIGNMENT

This alignment and test procedure covers the tests required for the Balanced Mixer-Preamplifier, Motorola Part No. 01-23773D01. Refer to figure 6-28 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.25 50 MC IF AMPLIFIER AND SECOND MIXER 1A7A2, ALIGNMENT

This alignment and test procedure covers the tests required for the 50 MC IF Amplifier and Second Mixer, Motorola Part No. 01-23774D01. Refer to figure 6-29 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.26 10 MC IF DISTRIBUTION AMPLIFIER 1A7A3, ALIGNMENT

This alignment and test procedure covers the tests required for the 10 MC IF Distribution Amplifier, Motorola Part No. 01-23775D01. Refer to figure 6-30 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.27 10 MC IF AMPLIFIER 1A7A4, ALIGNMENT

This alignment and test procedure covers the tests required for the 10 MC IF Amplifier, Motorola Part No. 01-23776D01. Refer to figure 6-31 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.28 FREQUENCY CONVERTER 1A8, ALIGNMENT

This procedure covers the required alignment and test for the Frequency Converter, Motorola Part No. 01-25251E. Refer to figure 6-32 for a schematic diagram of the drawer. This alignment and checkout procedure assumes the assembly checkout procedures outlined in paragraphs 4.29 and 4.30 were completed prior to the alignment of the drawer in the following procedure.

4.28.1 Test Equipment Required

The following test equipment, or equivalent, is required to align and test the Frequency Converter.

Frequency Counter, HP-524C
Counter Converter Head, HP-525B
VTVM, HP-412A
Spectrum Analyzer, Panoramic SPA-4a
Signal Generator, HP-616A
Test Transmitter, 1A9

4.28.2 Alignment

4.28.2.1 5-Channel Oscillator

a. Apply power to the drawer.
b. Connect a frequency counter to TP1 on the 5-Channel Oscillator assembly (1A8A1).
c. Set the FREQUENCY SELECTOR switch in each of the five VCO positions, and check the oscillator frequency on the frequency counter for the proper frequencies tabulated as follows. (A slight readjustment of coils L1 through L5 may be necessary to obtain the proper frequency.) Multiply the frequency obtained on the frequency counter times 4 for the following readings.

Switch Position	Oscillator Frequency (MC)	Output Frequency (MC)
1	45.421870 ±45 cps	181.687480 ±180 cps
2	45.473190 ±45 cps	181.892748 ±180 cps
3	45.480520 ±45 cps	181.922071 ±180 cps
4	45.487850 ±45 cps	181.951388 ±180 cps
5	45.495180 ±45 cps	181.980708 ±180 cps

4.28.2.2 Crystal Current

a. Connect a DC VTVM at TP1 on the Mixer-Filter assembly (1A8A2).
b. Switch the FREQUENCY SELECTOR switch to the No. 1 position.
c. Observe the voltage reading on the VTVM. The voltage should be 0.05 vdc or greater.
d. Determine the crystal current by dividing the voltage obtained in step (c) by 100 ohms (limit: 0.5 ma minimum).
e. Repeat the above procedure for FREQUENCY SELECTOR switch positions 2 through 5.

4.28.2.3 RF Mixer

a. Connect the output signal from the Test Transmitter (1A9J1) to the input of the Frequency Converter (1A8J1).
b. Set both variable attenuators on the Test Transmitter to zero.
c. Set Test Transmitter VCO SELECTOR switch to position No. 1.
d. Set Test Transmitter FREQUENCY CONTROL to 5.00.
e. Set Frequency Converter FREQUENCY SELECTOR switch to position No. 1.
f. Connect a spectrum analyzer to the output of the Frequency Converter (1A8J2).
g. Observe the desired output signal on the spectrum analyzer, and turn the tuning screws on cavities Z1 and Z3 of the Mixer-Filter assembly (1A8A2) for a maximum signal.

4.28.3 <u>Test Requirements</u>

4.28.3.1 Mixer Conversion

a. Set up the test equipment as described in paragraph 4.28.2.3.
b. Measure the amplitude of the Frequency Converter output signal.
c. Connect the Test Transmitter output signal to the spectrum analyzer and measure the amplitude of the signal.
d. Subtract the two readings obtained in steps (b) and (c), and then subtract 6 db to allow for the 6 db attenuator in the Frequency Converter drawer (limit: -18 db maximum).

4.28.3.2 Spurious Signals

a. Set up the test equipment as described in paragraph 4.28.2.3.
b. Vary the spectrum analyzer over a frequency range of 850 mc to 4000 mc and verify that spurious signals are -50 dbm or less below the desired output signal.

4.28.3.3 RF Bandwidth

a. Connect a HP-616A signal generator to the input of the Frequency Converter (1A8J1).
b. Set the output signal from the signal generator to approximately 2116 mc and -40 dbm.
c. Connect the spectrum analyzer to the output of the Frequency Converter (1A8J2).
d. Set the spectrum analyzer amplitude control to linear operation, and tune the spectrum analyzer to display the output signal from the Frequency Converter at the center graticule of the cathode ray tube.
e. Vary the signal generator output signal to determine the 3 db passband of the Frequency Converter (limit: 12 mc minimum).

NOTE

To determine the Frequency Converter bandwidth, the spectrum analyzer should be adjusted so that the display is always presented on the center of the vertical graticule. When the maximum output occurs (center frequency of passband), adjust spectrum analyzer amplitude controls to display the output to full scale. The upper and lower frequencies are determined when the output amplitude drops to 0.7 of the center frequency output. Subtract the two frequencies to determine the passband.

4.29 5-CHANNEL OSCILLATOR 1A8A1, ALIGNMENT

This alignment and test procedure covers the tests required for the 5-Channel Oscillator, Motorola Part No. 01-25277E01. Refer to figure 6-33 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.30 MIXER-FILTER 1A8A2, ALIGNMENT

This alignment and test procedure covers the tests required for the Mixer-Filter, Motorola Part No. 01-20247E01. Refer to figure 6-34 for a schematic diagram of the assembly. The Mixer-Filter assembly requires no alignment.

4.31 TEST TRANSMITTER 1A9, ALIGNMENT

This procedure covers the required alignment and test for the Test-Transmitter, Motorola Part No. 01-25252E. Refer to figure 6-35 for a schematic diagram of the drawer. This alignment and checkout procedure assumes the assembly checkout procedures outlined in paragraphs 4.32 through 4.34 were completed prior to the alignment of the drawer in the following procedure.

4.31.1 <u>Test Equipment Required</u>

The following test equipment, or equivalent, is required to align and test the Test Transmitter.

Power Meter, HP-430C
Thermistor Mount, HP-477B
Frequency Counter, HP-524C
Counter Converter Head, HP-525C
Spectrum Analyzer, Panoramic SPA-4a
Signal Generator, HP-608C
Signal Generator, HP-614B

Signal Generator, HP-606A
Signal Generator, HP-616A
VTVM, HP-410B
Audio Oscillator, HP-200CD
Power Meter, HP-431B

4.31.2 Initial Alignment of Power Supplies

a. Adjust the +15 vdc power supply to +15 ±0.5 vdc.
b. Adjust the -15 vdc power supply to -15 ±0.5 vdc.
c. Adjust the -28 vdc power supply to -28 ±0.5 vdc.

4.31.3 Test Requirements

4.31.3.1 VCO Power Outputs

a. Set the FREQUENCY CONTROL dial to 5.0.
b. Terminate jacks J2 and J6 (22 MC outputs) with 50 ohm terminations.
c. Connect a power meter to jack J5 (22 MC output).
d. Measure the power output of the Test Transmitter (limit: 10 mw minimum).
e. Terminate jacks J5 and J6 with 50 ohm terminations.
f. Connect a power meter to jack J2.
g. Measure the power output (limit: 1 mw nominal).
h. Terminate jacks J2 and J5 with 50 ohm terminations.
i. Connect a power meter to J6.
j. Measure the power output (limit: 1 mw nominal).

4.31.3.2 VCO Center Frequencies

a. Set FREQUENCY CONTROL dial to 5.0.
b. Terminate jacks J5 and J6 with 50 ohm terminations.
c. Connect a frequency counter to jack J2.
d. Set the VCO SELECTOR switch to the following five positions and measure the output frequencies at jack J2.

VCO SELECTOR Switch Position	Frequency (MC)
1	22.013670 ±144 cps
2	22.038540 ±144 cps
3	22.042092 ±144 cps
4	22.045645 ±144 cps
5	22.049198 ±144 cps

e. Verify that the frequencies at jacks J2, J5, and J6 are identical frequencies.

4.31.3.3 VCO Deviation

a. With the VCO SELECTOR switch placed in No. 1 position, jacks J5 and J6 terminated with 50 ohm terminations, and a frequency counter connected to jack J2, vary the FREQUENCY CONTROL dial from 1.0 to -10 and measure the output frequencies at 0.0, 1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, and 10.0.

b. Plot the results of step (a) on a graph. Figure 4-2 is a typical graph (limit: VCO frequency shall deviate ±800 cps from 5.0 frequency dial reading).

c. With the VCO SELECTOR switch placed in the No. 2 position, vary the FREQUENCY CONTROL dial from 1.0 to -10 and plot the results on a graph as described in steps (a) and (b). Figure 4-2 is a typical graph.

d. With the VCO SELECTOR switch placed in the No. 3 position, vary the FREQUENCY CONTROL dial from 1.0 to -10 and plot the results on a graph as described in steps (a) and (b) . Figure 4-2 is a typical graph.

e. With the VCO SELECTOR switch placed in the No. 4 position, vary the FREQUENCY CONTROL dial from 1.0 to -10 and plot the results on a graph as described in steps (a) and (b). Figure 4-2 is a typical graph.

f. With the VCO SELECTOR switch placed in the No. 5 position, vary the FREQUENCY CONTROL dial from 1.0 to -10 and plot the results on a graph as described in steps (a) and (b). Figure 4-2 is a typical graph.

4.31.3.4 Transmitter Power Outputs

4.31.3.4.1 RF Power Monitor Output (J8)

a. Connect a power meter to the RF power monitor at jack J8.

b. Set VCO SELECTOR switch to No. 1 position.

c. Vary the FREQUENCY CONTROL dial from 10.0 to 0.0 and back to 10.0 and measure the maximum and minimum power output (limit: 0 to 10 dbm).

d. Repeat the procedure outlined in steps (b) and (c) for VCO SELECTOR switch positions 2 through 5.

4.31.3.4.2 RF Output (J1)

a. Connect a spectrum analyzer in series with a 50-ohm, 6 db pad at the Test Transmitter RF output (J1).

b. Set step attenuator and variable attenuator to 0 db.

c. Use the comparison method with a HP-616B signal generator and measure the power output (limit: -40 dbm minimum).

4.31.3.4.3 RWV Output

a. Connect a 6 db pad in series with the spectrum analyzer to the RWV output jack (J9).

b. Use the comparison method and measure the power output (limit: -50 dbm ±5 db).

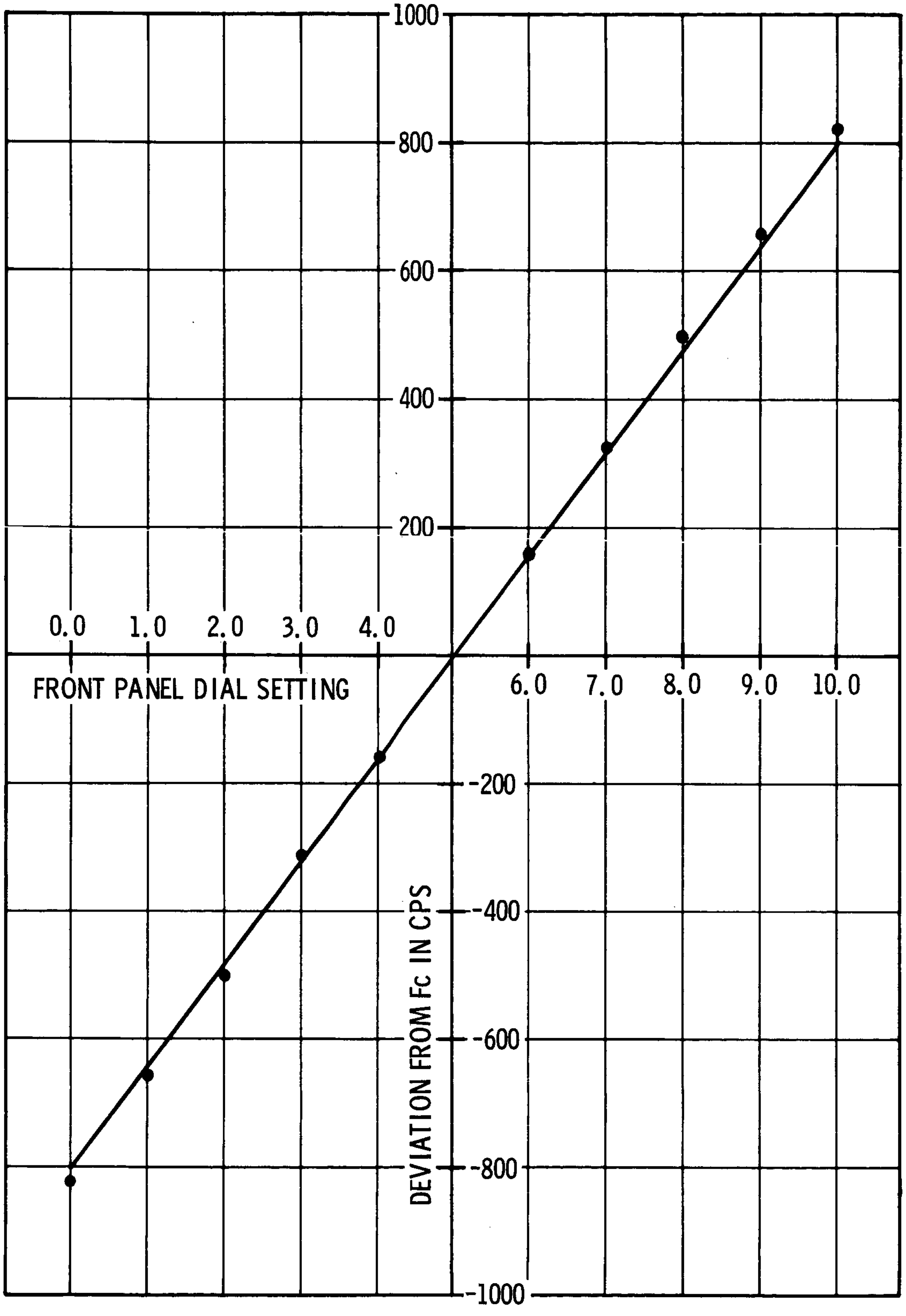


Figure 4-2. Typical VCO Linearity Curve for Test Transmitter

4.31.3.5 Phase Modulation

4.31.3.5.1 Phase Modulation Sensitivity (Command Modulation Input, J3)

a. Set up the test equipment as shown in figure 4-3.

b. Set signal generator output frequency to 50 kc and a minimum output.

c. Adjust the spectrum analyzer until a carrier signal is observed on the spectrum analyzer. (Increase the output signal level until the carrier null is obtained.)

d. Measure the signal generator output signal level on the AC VTVM (limits: 1.7 ±0.8V RMS).

4.31.3.5.2 Phase Modulation Sensitivity (Range Modulation Input, J4)

a. Connect the HP-606A signal generator and AC VTVM to the range modulation input (J4).

b. Terminate the command modulation input (J3) with a 2.2K resistive load.

c. Set signal generator output frequency to 500 kc.

d. Repeat the procedure outlined in steps (c) and (d) of paragraph 4.31.3.5.1 (limit: 0.426 ±0.02V RMS).

e. Repeat the procedure in step (d) for signal generator settings of 50 kc, 100 kc, 500 kc, and 1 mc (sensitivity shall remain constant within ±1 db over all the above frequencies).

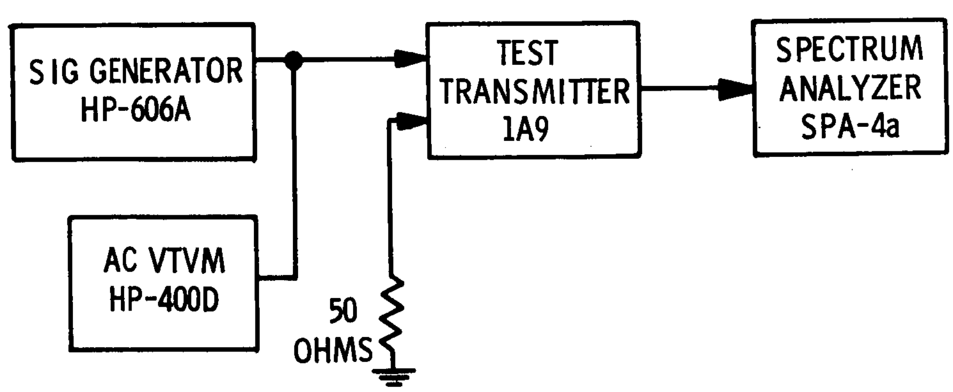


Figure 4-3. Test Transmitter, Test Setup

4.31.3.6 Transmitter Disable

a. Connect the spectrum analyzer to the Test Transmitter RF output (J1).

b. Depress the **TRANSMITTER DISABLE** switch and verify that the signal output drops to zero.

4.31.3.7 Spurious Signals

a. With the equipment set up as described in paragraph 4.31.3.5.2, search for spurious signals between 850 mc and 4000 mc.

b. Verify that spurious signals and sidebands are a minimum of 30 db below the desired output signal.

4.32 5-CHANNEL TRANSMITTER VCO 1A9A1, ALIGNMENT

This alignment and test procedure covers the tests required for the 5-Channel Transmitter VCO, Motorola Part No. 01-25260E01. Refer to figure 6-25 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.33 X3 MULTIPLIER AND PHASE MODULATOR 1A9A2, ALIGNMENT

This alignment and test procedure covers the tests required for the X3 Multiplier and Phase Modulator, Motorola Part No. 01-23760D. Refer to figure 6-36 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 2 on the assembly.

4.34 X32 FREQUENCY MULTIPLIER 1A9A3, ALIGNMENT

Alignment of this assembly is performed in the same manner as the alignment of X32 Frequency Multiplier 1A4A4 except for the frequency (located in Volume 2). Refer to figure 6-19 for a schematic diagram of the assembly.

4.35 RANGING CONVERSION UNIT 1A10, ALIGNMENT

No alignment procedure is necessary for the Ranging Conversion Unit, Motorola Part No. 01-25253E. Refer to paragraphs 4.36 through 4.38 for alignment of the assemblies. Refer to figure 6-7 for a schematic diagram of the Ranging Conversion Unit.

4.36 10 MC PHASE SHIFTER 1A10A1, ALIGNMENT

Alignment of this assembly is performed in the same manner as the alignment of 10 MC Phase Shifter 1A2A5 (located in Volume 2). Refer to figure 6-10 for a schematic diagram of the assembly.

4.37 10 MC PHASE SWITCH 1A10A2, ALIGNMENT

This alignment and test procedure covers the tests required for the 10 MC Phase Switch, Motorola Part No. 01-23840D. Refer to figure 6-38 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

4.38 10 MC BALANCED DETECTOR 1A10A3, ALIGNMENT

This alignment and test procedure covers the tests required for the 10 MC Balanced Detector, Motorola Part No. 01-23845D. Refer to figure 6-39 for a schematic diagram of the assembly. Perform the alignment procedure outlined in Volume 3 on the assembly.

VOLUME 1

SECTION V

DEVELOPMENT TECHNICAL PROBLEMS AND RECOMMENDATIONS

5.1 GENERAL

This section contains information pertaining to problems encountered and recommendations for their possible solution.

5.2 TELEMETRY NARROW BAND SUBSYSTEM 1A2

During checkout of this section of the test set it was noted that readjustment of the 10 MC Phase Shifter (1A2A5) was required, as different bandwidths were selected by the front panel switch, to keep the Phase Detector (1A2A3) operating at the correct point.

Two solutions to this problem appear possible. The most obvious solution is to change the drawer layout so the adjustment is made accessible from the front panel. The other solution is to incorporate some form of phase correction network in connection with the bandwidth change so that no readjustment is required.

5.3 TEST RECEIVER, 1A4, 1A5, 1A6, and 1A7

5.3.1 In-Lock Indicator

During test set checkout it became obvious that a self-contained positive indication of lock was desirable. The only indication at present is the SIGNAL STRENGTH meter, which provides such an indication when the unit is using AGC operation. (On MGC operation, even this indication is lost.) On AGC operation, near threshold, it is difficult to determine by the meter when "lock" is lost, and it is possible to have an AGC meter indication of lock-up on a beat note, which may not be detected unless observed on an oscilloscope at the time.

It appears that provisions to drive some type of amplifier-indicator from the AGC Amplifier and Filter Assembly (1A5A1) are designed in and may be satisfactory if proper indicating devices were utilized. Also, if this approach is not desired in the test set, an audio indication may be used by monitoring the DPE output with something as simple as a pair of headphones.

5.3.2 Loop Filter Time Constants

The time constants used in the Loop Filter Assembly (1A6A2) do not center on the bandwidth stated on the front panel. The actual bandwidth provided is below the value indicated by the front panel switch. This was a design objective of the assembly to provide a bandwidth that would never be greater than that indicated on the front panel.

5.3.3 Loop Filter Switching Transients

When changing Loop Filter bandwidths between 12 cps and 48 cps positions, different capacitors are switched in or out of the circuit. Due to a difference in the charge on the switched-in capacitor and the one switched out, the receiver may be knocked out of lock. No immediately apparent cure for this problem was found without modification of the assemblies.

5.4 TEST TRANSMITTER, 1A9

The performance of the Test Transmitter appears to be very good. The primary area where improvement could be made on future models is to incorporate a bandpass filter following the X32 Multiplier. (This incorporation of a bandpass filter is done in the DSIF system before going to power amplifiers.) Several spurious outputs are present at a sufficient level to possibly be of difficulty to some systems. They are far enough removed from the main signal that filter bandwidth could be fairly wide and still reduce them considerably. Thus, one filter would suffice for transmitters over a fairly wide frequency range.

VOLUME 1

SECTION VI

DIAGRAMS

6.1 GENERAL

This section contains all the interconnection, block, and schematic diagrams for the GSE, with the one exception that all diagrams for the commerical equipment are located in each commercial manual.

6.2 INDEX OF DRAWINGS

Table VI-1 lists the first page number for each diagram pertaining to the GSE. The drawings are identified in table VI-1 according to the reference designation for each drawer or assembly.

TABLE VI-1. GSE LIST OF DIAGRAMS

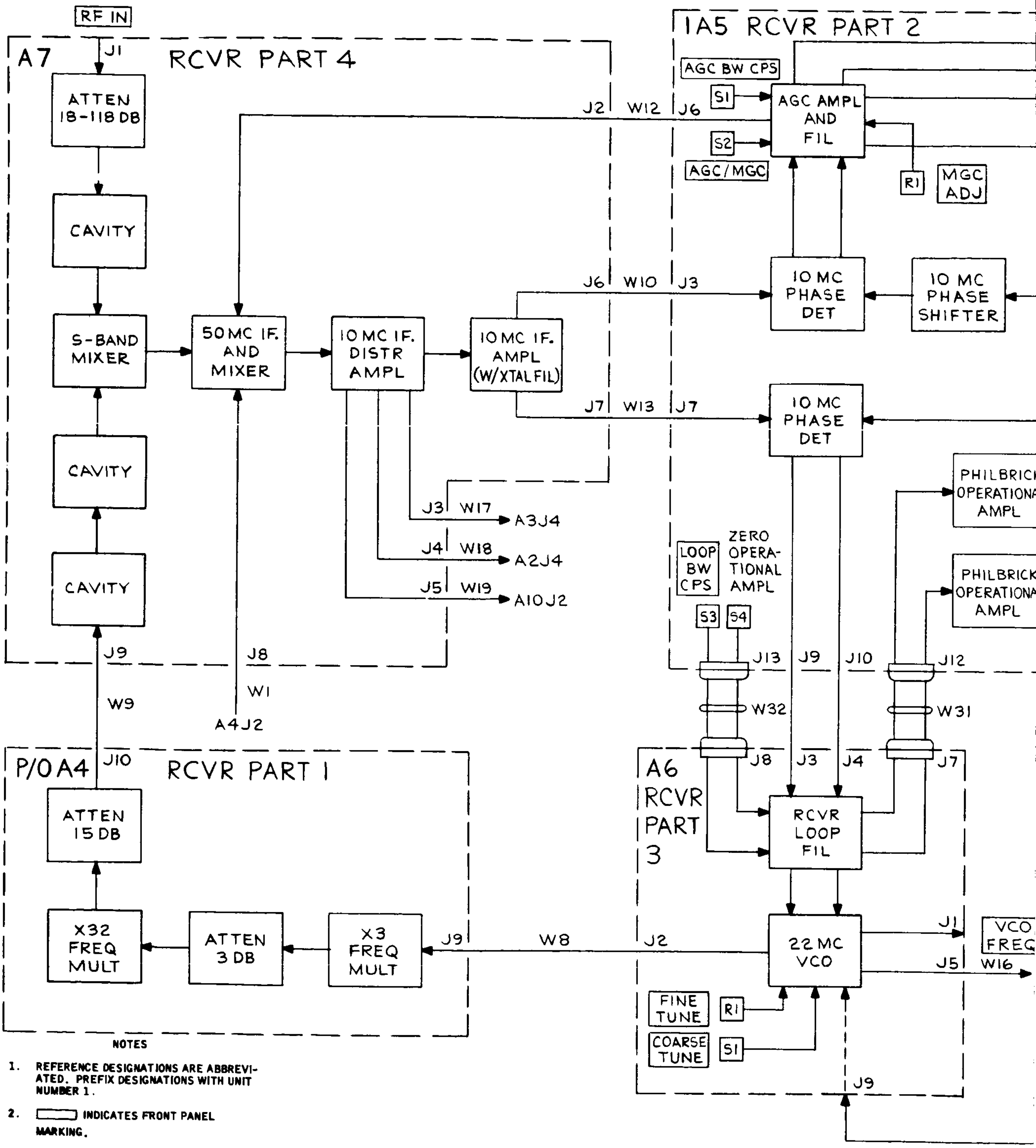
Drawing No.	Figure No.	Page No.	Reference Designation	Title
69-25440E	6-1	6-5	--	GSE, Over-all Block Diagram.
69-25442E	6-2	6-7	--	GSE, Power Interconnection Diagram.
63-25441E	6-3	6-9	--	GSE, Signal Interconnection Diagram.
63-25444E	6-4	6-11	1A1	Circuit Breaker Panel, Schematic Diagram.
63-25445E	6-5	6-13	1A2	Telemetry Narrow Band Subsystem, Schematic Diagram.
63-23881D	6-6	6-15	1A2A1, 1A3A1	Telemetry Bandpass Filter, Schematic Diagram.
63-24038D	6-7	6-17	1A2A2	Narrow Band 10 MC IF Amplifier, Schematic Diagram.
63-25032E	6-8	6-19	1A2A3	10 MC Phase Detector, Schematic Diagram.
63-23883D	6-9	6-21	1A2A4	Video Amplifier, Schematic Diagram.
63-23860D	6-10	6-23	1A2A5, 1A5A3, 1A10A1	10 MC Phase Shifter, Schematic Diagram.
63-25446E	6-11	6-25	1A3	Telemetry Wide Band Subsystem, Schematic Diagram.
63-23882D	6-12	6-27	1A3A2	Wide Band 10 MC IF Amplifier, Schematic Diagram.

TABLE VI-1. GSE LIST OF DIAGRAMS (cont)

Drawing No.	Figure No.	Page No.	Reference Designation	Title
63-23893D	6-13	6-29	1A3A3	10.02 MC Mixer-Oscillator, Schematic Diagram.
69-25443E	6-14	6-31	1A4 thru 1A7	Test Receiver, Interconnection Diagram.
63-25447E	6-15	6-33	1A4	Test Receiver, Part One, Schematic Diagram.
63-21453C	6-16	6-35	1A4A1	20 MC Oscillator and X3 Multiplier, Schematic Diagram.
63-21454C	6-17	6-37	1A4A2	X½ Frequency Multiplier, Schematic Diagram.
63-23868D	6-18	6-39	1A4A3	10 MC Isolation and Distribution Amplifier, Schematic Diagram.
63-23875D	6-19	6-41	1A4A4,1A9A3	X32 Frequency Multiplier,Schematic Diagram.
63-23625D	6-20	6-43	1A4A5	X3 Frequency Multiplier, Schematic Diagram.
63-25448E	6-21	6-45	1A5	Test Receiver, Part Two, Schematic Diagram.
63-25023E	6-22	6-47	1A5A1	AGC Amplifier and Filter, Schematic Diagram.
63-21447C	6-23	6-49	1A5A2,A4	10 MC Phase Detector, Schematic Diagram.
63-25449E	6-24	6-51	1A6	Test Receiver, Part Three, Schematic Diagram.
63-25280E	6-25	6-53	1A6A1,1A9A1	5-Channel VCO, Schematic Diagram.
63-23863D	6-26	6-55	1A6A2	Loop Filter, Schematic Diagram.
63-25450E	6-27	6-57	1A7	Test Receiver, Part Four, Schematic Diagram.
63-23879D	6-28	6-59	1A7A1	Balanced Mixer-Preamplifier, Schematic Diagram.
63-21450C	6-29	6-61	1A7A2	50 MC IF Amplifier and Second Mixer, Schematic Diagram.
63-23886D	6-30	6-63	1A7A3	10 MC Distribution Amplifier, Schematic Diagram.

TABLE VI-1. GSE LIST OF DIAGRAMS (cont)

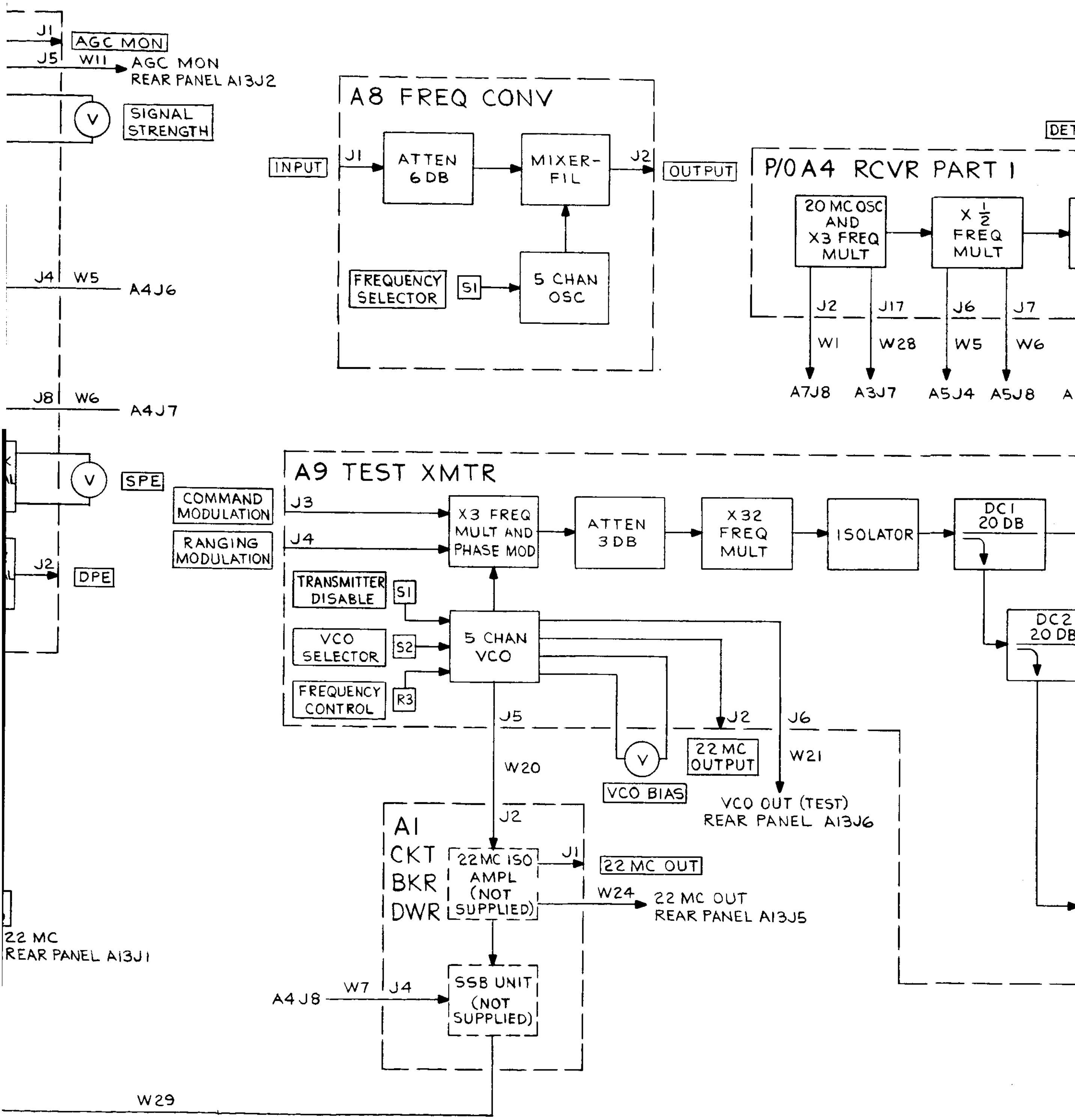
Drawing No.	Figure No.	Page No.	Reference Designation	Title
63-21449C	6-31	6-65	1A7A4	10 MC IF Amplifier, Schematic Diagram.
63-25451E	6-32	6-67	1A8	Frequency Converter, Schematic Diagram.
63-25281E	6-33	6-69	1A8A1	5-Channel Oscillator, Schematic Diagram.
63-20348E	6-34	6-71	1A8A2	Mixer-Filter, Schematic Diagram.
63-25452E	6-35	6-73	1A9	Test Transmitter, Schematic Diagram.
63-23862D	6-36	6-75	1A9A2	X3 Multiplier and Phase Modulator, Schematic Diagram.
63-25453E	6-37	6-77	1A10	Ranging Conversion Unit, Schematic Diagram.
63-23895D	6-38	6-79	1A10A2	10 MC Phase Switch, Schematic Diagram.
63-23897D	6-39	6-81	1A10A3	10 MC Balanced Detector, Schematic Diagram.



NOTES

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER 1.

2. ▭ INDICATES FRONT PANEL MARKING.



J1
AGC MON
J5
W11
AGC MON
REAR PANEL A13J2
V
SIGNAL STRENGTH
J4
W5
A4J6
J8
W6
A4J7
V
SPE
J2
DPE
22 MC
REAR PANEL A13J1
W29
A8 FREQ CONV
INPUT
J1
ATTEN 6 DB
MIXER-FIL
J2
OUTPUT
FREQUENCY SELECTOR
S1
5 CHAN OSC
P/O A4 RCVR PART I
DET
20 MC OSC AND X3 FREQ MULT
X 1/2 FREQ MULT
J2
J17
J6
J7
W1
W28
W5
W6
A7J8
A3J7
A5J4
A5J8
A
A9 TEST XMTR
COMMAND MODULATION
RANGING MODULATION
J3
J4
X3 FREQ MULT AND PHASE MOD
ATTEN 3 DB
X32 FREQ MULT
ISOLATOR
DC1 20 DB
DC2 20 DB
TRANSMITTER DISABLE
S1
VCO SELECTOR
S2
FREQUENCY CONTROL
R3
5 CHAN VCO
J5
J2
J6
W20
V
VCO BIAS
22 MC OUTPUT
W21
VCO OUT (TEST)
REAR PANEL A13J6
A1 CKT BKR DWR
J2
22MC ISO AMPL (NOT SUPPLIED)
J1
22 MC OUT
W24
22 MC OUT
REAR PANEL A13J5
A4J8
W7
J4
SSB UNIT (NOT SUPPLIED)

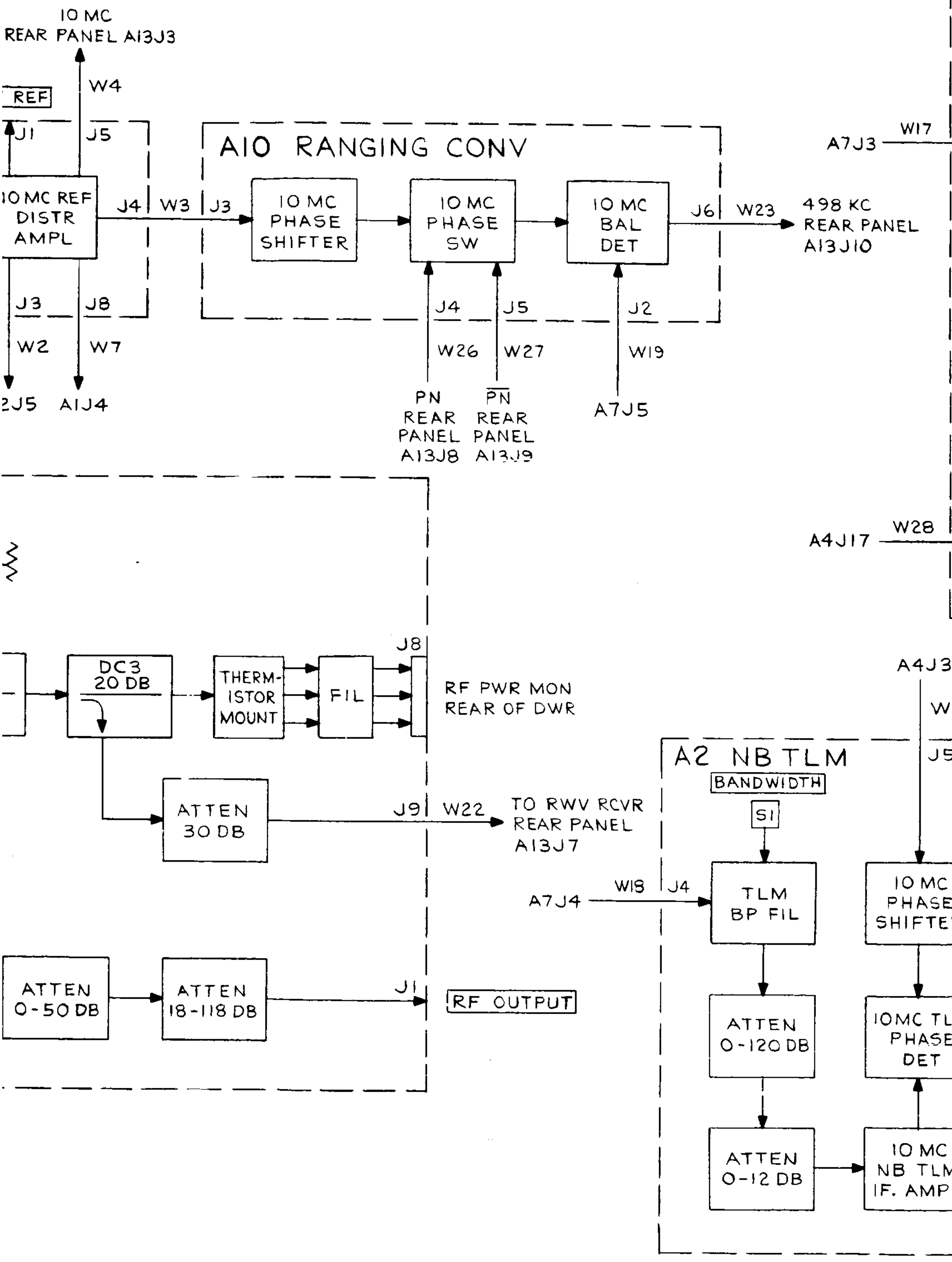
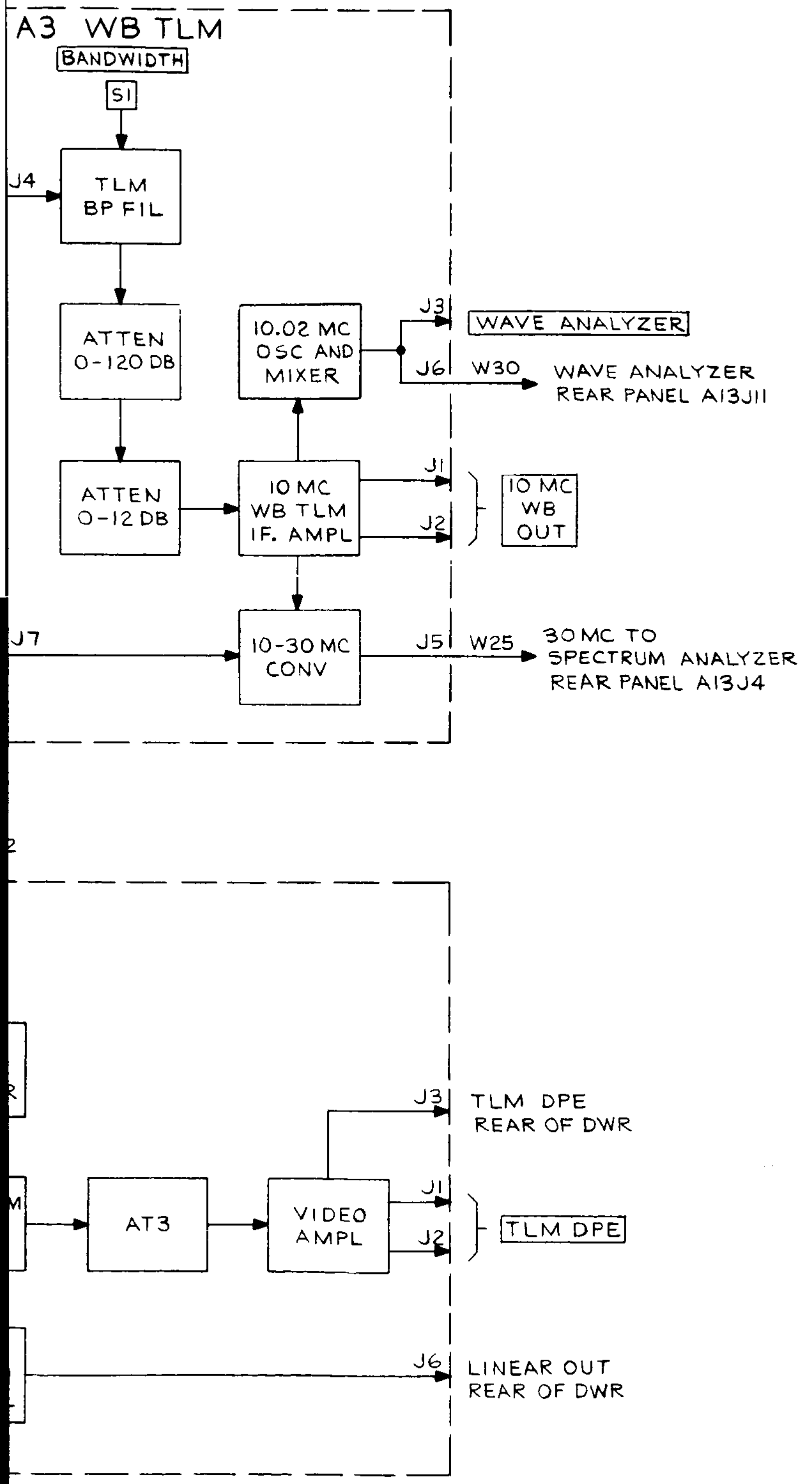

10 MC
REAR PANEL A13J3
W4
REF
J1
J5
10 MC REF
DISTR
AMPL
J4
W3
J3
J8
W2
W7
2J5
A1J4
A10 RANGING CONV
J3
10 MC
PHASE
SHIFTER
10 MC
PHASE
SW
10 MC
BAL
DET
J6
W23
498 KC
REAR PANEL
A13J10
J4
J5
J2
W26
W27
W19
PN
REAR
PANEL
A13J8
PN
REAR
PANEL
A13J9
A7J5
A7J3
W17
A4J17
W28
J8
DC3
20 DB
THERM-
ISTOR
MOUNT
FIL
RF PWR MON
REAR OF DWR
ATTEN
30 DB
J9
W22
TO RWV RCVR
REAR PANEL
A13J7
ATTEN
0-50 DB
ATTEN
18-118 DB
J1
RF OUTPUT
A2 NB TLM
BANDWIDTH
S1
A7J4
W18
J4
TLM
BP FIL
ATTEN
0-120 DB
ATTEN
0-12 DB
A4J3
10 MC
PHASE
10 MC
NB TLM
IF. AMP

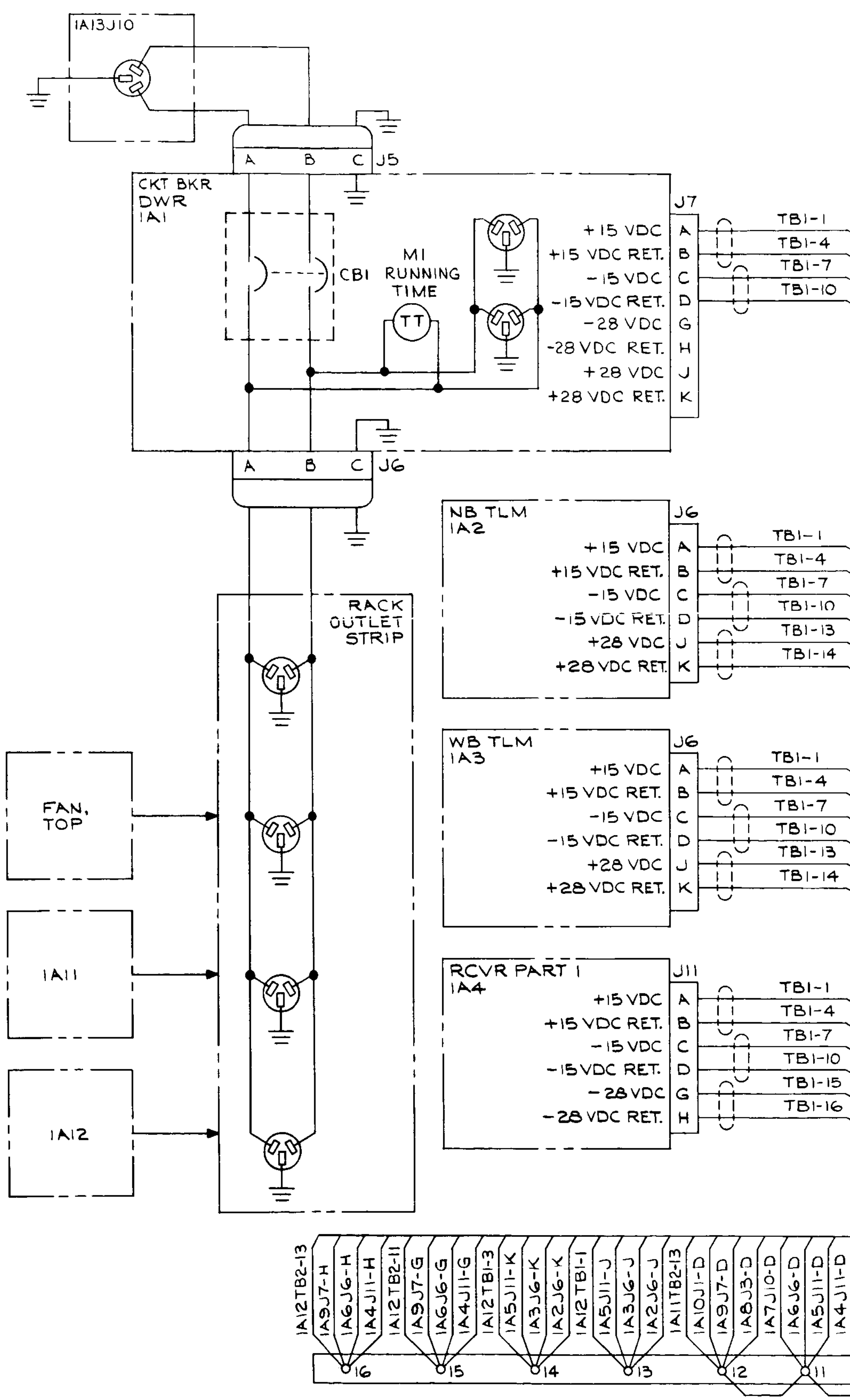
Figure 6-

3



-1. GSE, Over-all Block Diagram (69-25440E)

4


1A13J10
A B C J5
CKT BKR DWR 1A1
CB1
M1 RUNNING TIME
TT
J7
+15 VDC A
+15 VDC RET. B
-15 VDC C
-15 VDC RET. D
-28 VDC G
-28 VDC RET. H
+28 VDC J
+28 VDC RET. K
TB1-1
TB1-4
TB1-7
TB1-10
A B C J6
NB TLM 1A2
J6
+15 VDC A
+15 VDC RET. B
-15 VDC C
-15 VDC RET. D
+28 VDC J
+28 VDC RET. K
TB1-1
TB1-4
TB1-7
TB1-10
TB1-13
TB1-14
RACK OUTLET STRIP
WB TLM 1A3
J6
+15 VDC A
+15 VDC RET. B
-15 VDC C
-15 VDC RET. D
+28 VDC J
+28 VDC RET. K
TB1-1
TB1-4
TB1-7
TB1-10
TB1-13
TB1-14
FAN, TOP
1A11
1A12
RCVR PART 1 1A4
J11
+15 VDC A
+15 VDC RET. B
-15 VDC C
-15 VDC RET. D
-28 VDC G
-28 VDC RET. H
TB1-1
TB1-4
TB1-7
TB1-10
TB1-15
TB1-16
1A12TB2-13
1A9J7-H
1A6J6-H
1A4J11-H
1A12TB2-11
1A9J7-G
1A6J6-G
1A4J11-G
1A12TB1-3
1A5J11-K
1A3J6-K
1A2J6-K
1A12TB1-1
1A5J11-J
1A3J6-J
1A2J6-J
1A11TB2-13
1A10J1-D
1A9J7-D
1A8J3-D
1A7J10-D
1A6J6-D
1A5J11-D
1A4J11-D
16
15
14
13
12
11

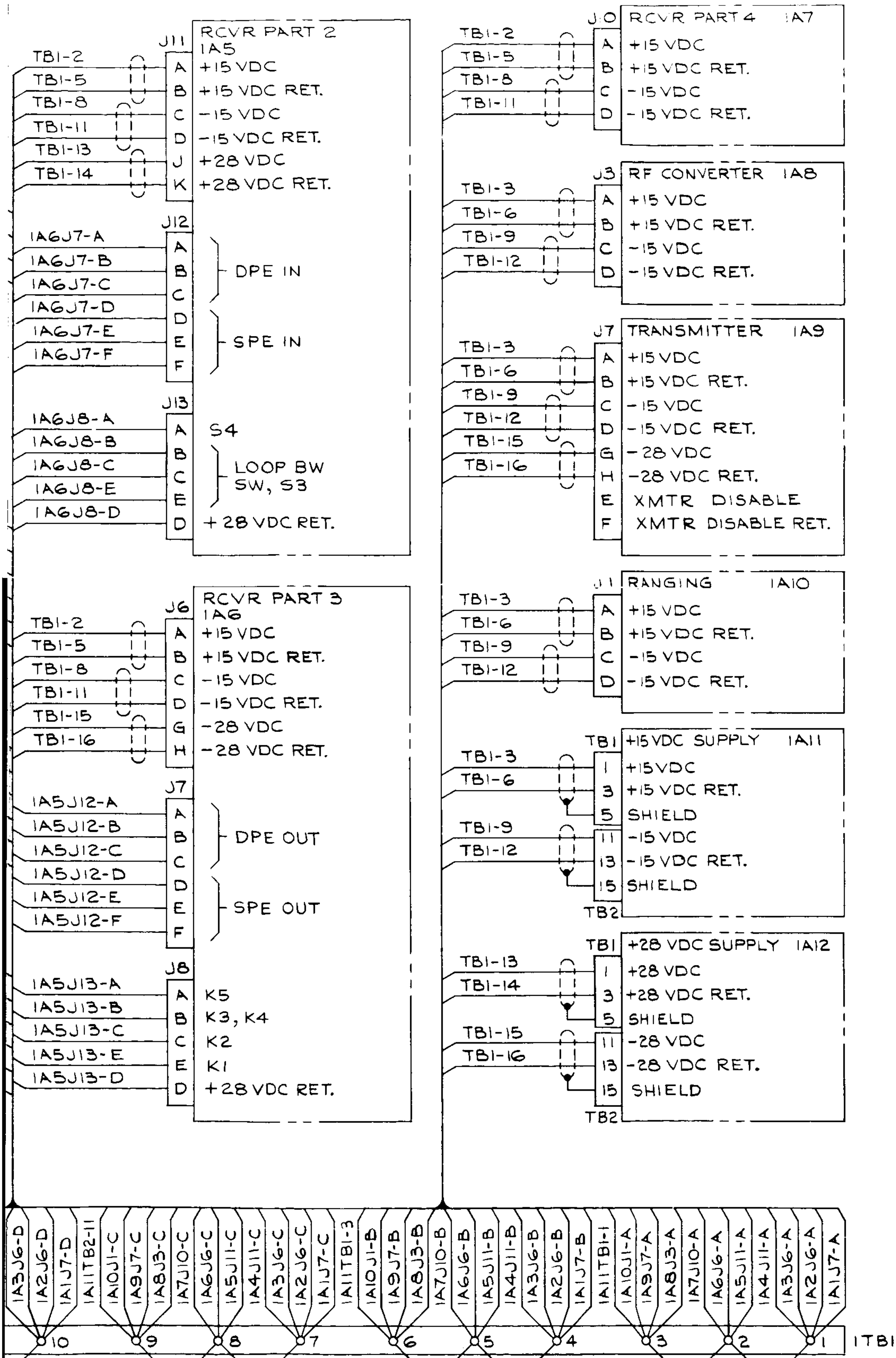
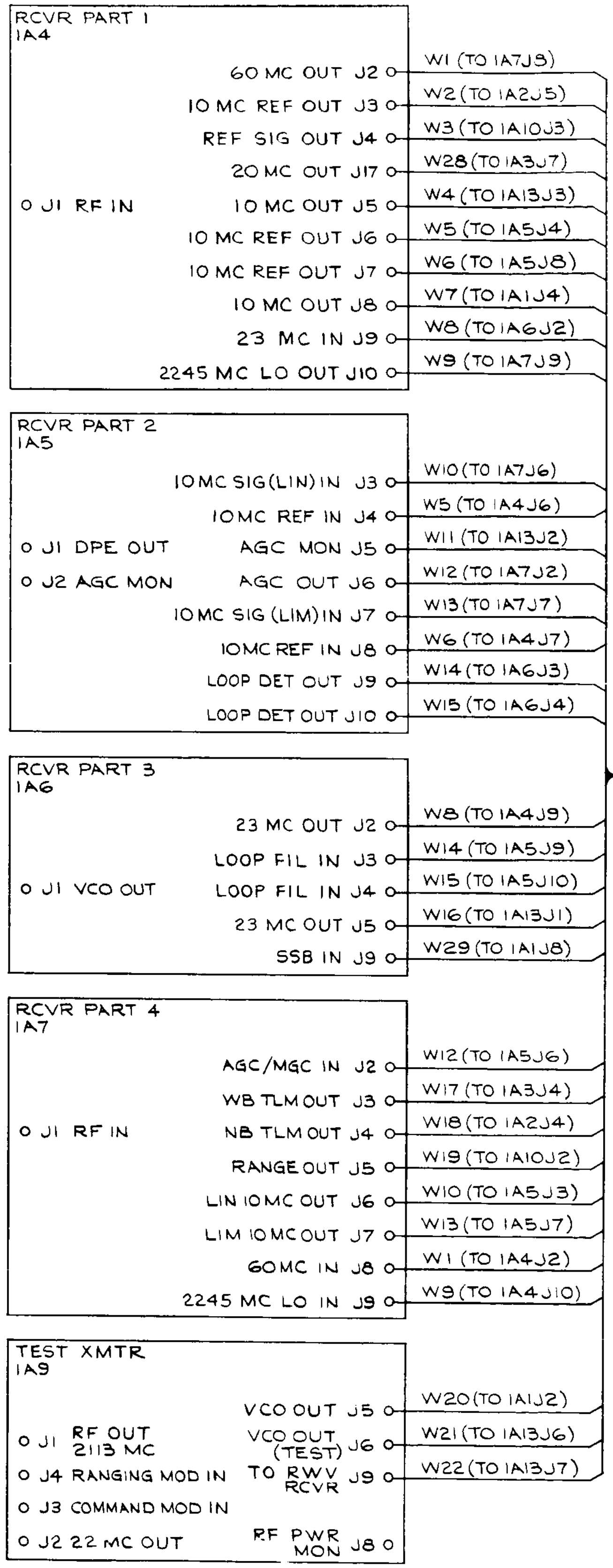


Figure 6-2. GSE, Power Interconnection Diagram (69-25442E)


RCVR PART 1
1A4
60 MC OUT J2
10 MC REF OUT J3
REF SIG OUT J4
20 MC OUT J17
O J1 RF IN
10 MC OUT J5
10 MC REF OUT J6
10 MC REF OUT J7
10 MC OUT J8
23 MC IN J9
2245 MC LO OUT J10
W1 (TO 1A7J8)
W2 (TO 1A2J5)
W3 (TO 1A10J3)
W28 (TO 1A3J7)
W4 (TO 1A13J3)
W5 (TO 1A5J4)
W6 (TO 1A5J8)
W7 (TO 1A1J4)
W8 (TO 1A6J2)
W9 (TO 1A7J9)
RCVR PART 2
1A5
10 MC SIG (LIN) IN J3
10 MC REF IN J4
O J1 DPE OUT
AGC MON J5
O J2 AGC MON
AGC OUT J6
10 MC SIG (LIM) IN J7
10 MC REF IN J8
LOOP DET OUT J9
LOOP DET OUT J10
W10 (TO 1A7J6)
W5 (TO 1A4J6)
W11 (TO 1A13J2)
W12 (TO 1A7J2)
W13 (TO 1A7J7)
W6 (TO 1A4J7)
W14 (TO 1A6J3)
W15 (TO 1A6J4)
RCVR PART 3
1A6
23 MC OUT J2
LOOP FIL IN J3
O J1 VCO OUT
LOOP FIL IN J4
23 MC OUT J5
SSB IN J9
W8 (TO 1A4J9)
W14 (TO 1A5J9)
W15 (TO 1A5J10)
W16 (TO 1A13J1)
W29 (TO 1A1J8)
RCVR PART 4
1A7
AGC/MGC IN J2
WB TLM OUT J3
O J1 RF IN
NB TLM OUT J4
RANGE OUT J5
LIN 10 MC OUT J6
LIM 10 MC OUT J7
60 MC IN J8
2245 MC LO IN J9
W12 (TO 1A5J6)
W17 (TO 1A3J4)
W18 (TO 1A2J4)
W19 (TO 1A10J2)
W10 (TO 1A5J3)
W13 (TO 1A5J7)
W1 (TO 1A4J2)
W9 (TO 1A4J10)
TEST XMTR
1A9
VCO OUT J5
O J1 RF OUT 2113 MC
VCO OUT (TEST) J6
O J4 RANGING MOD IN
TO RWV RCVR J9
O J3 COMMAND MOD IN
O J2 22 MC OUT
RF PWR MON J8
W20 (TO 1A1J2)
W21 (TO 1A13J6)
W22 (TO 1A13J7)

Figure

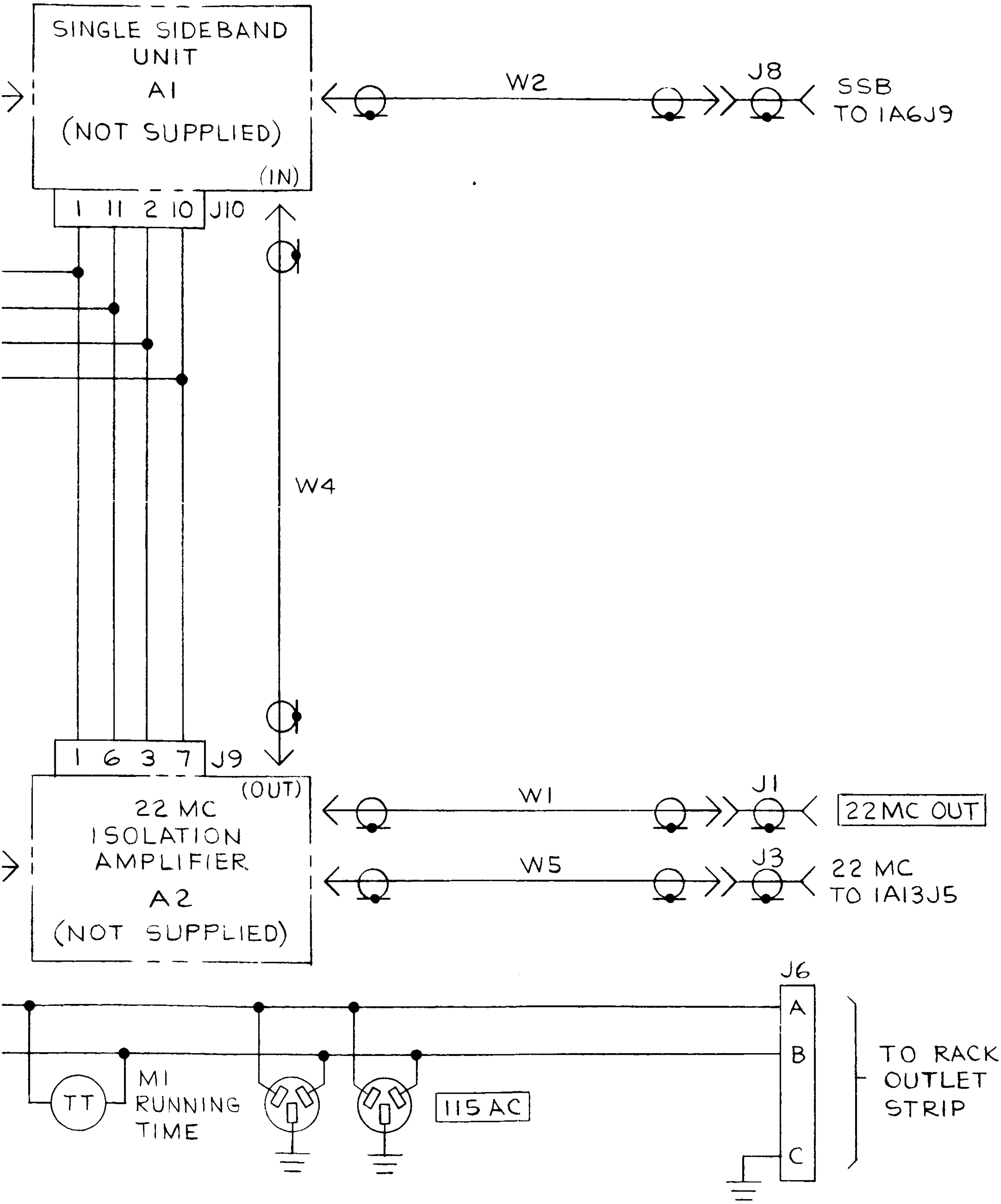


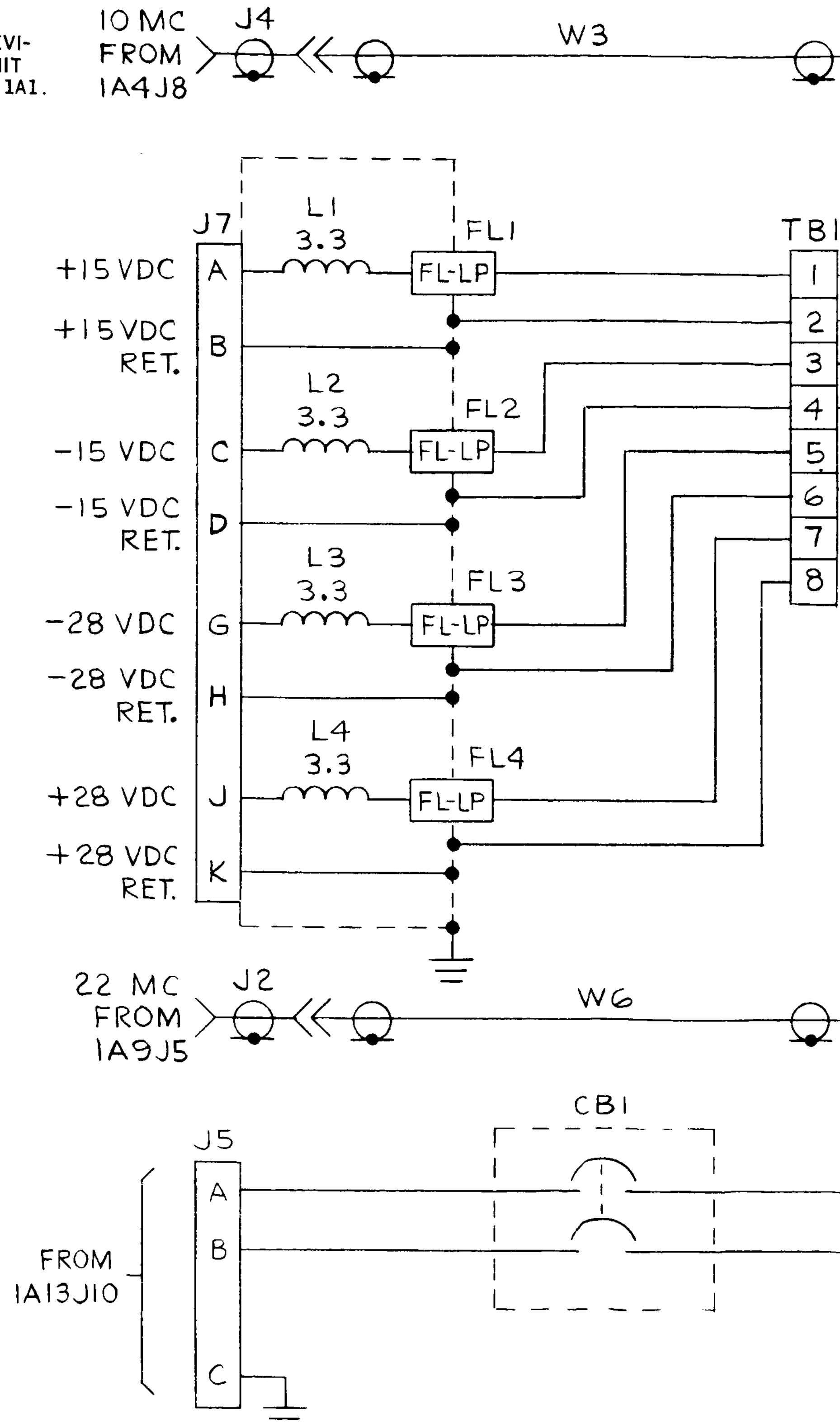
Figure 6-4. Circuit Breaker Panel (1A1), Schematic Diagram (63-25444E)

NOTES

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION 1A1.

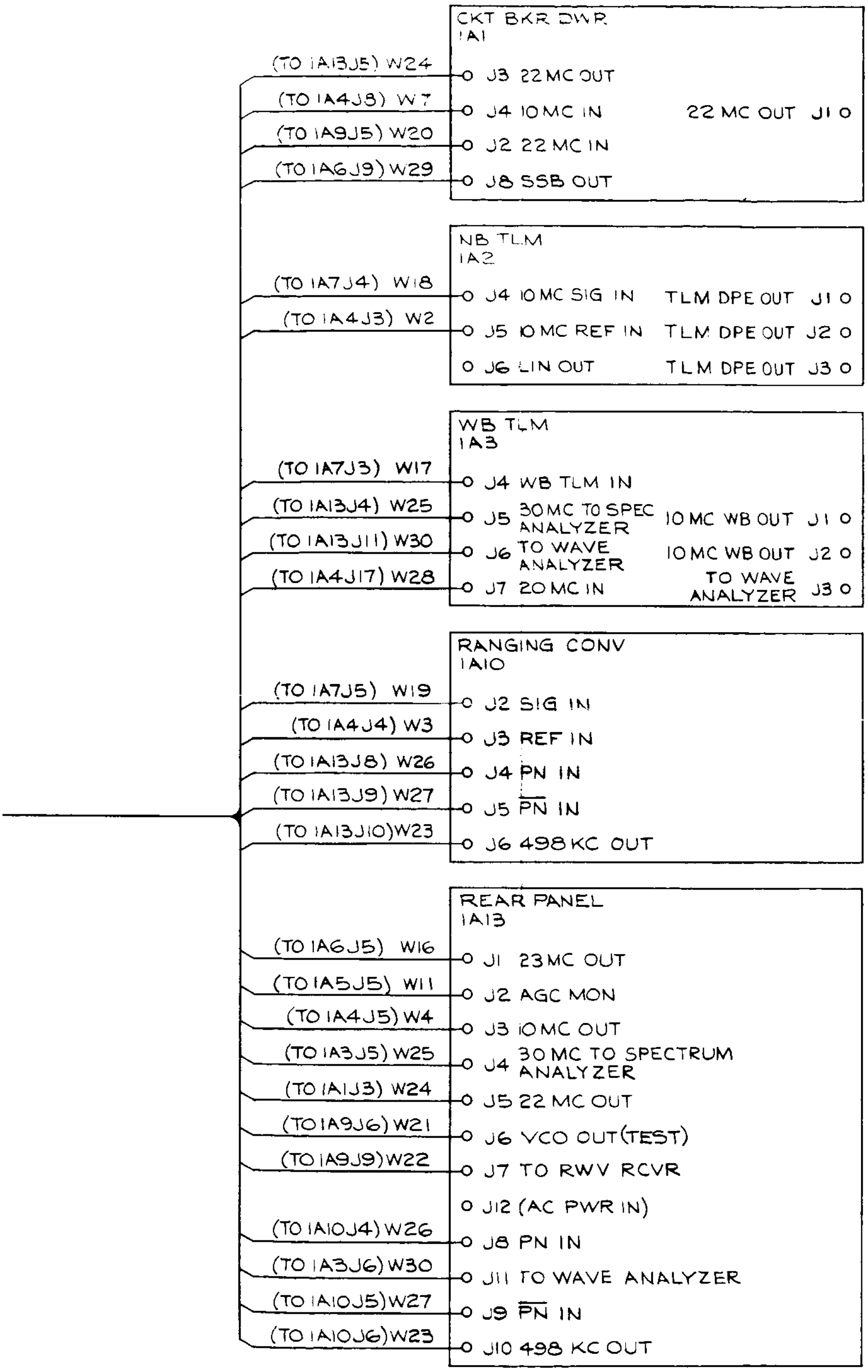
2. UNLESS OTHERWISE SPECIFIED:
   ALL INDUCTORS ARE IN UH.

3. [ ] INDICATES FRONT PANEL MARKING.



2

VOLUME 1



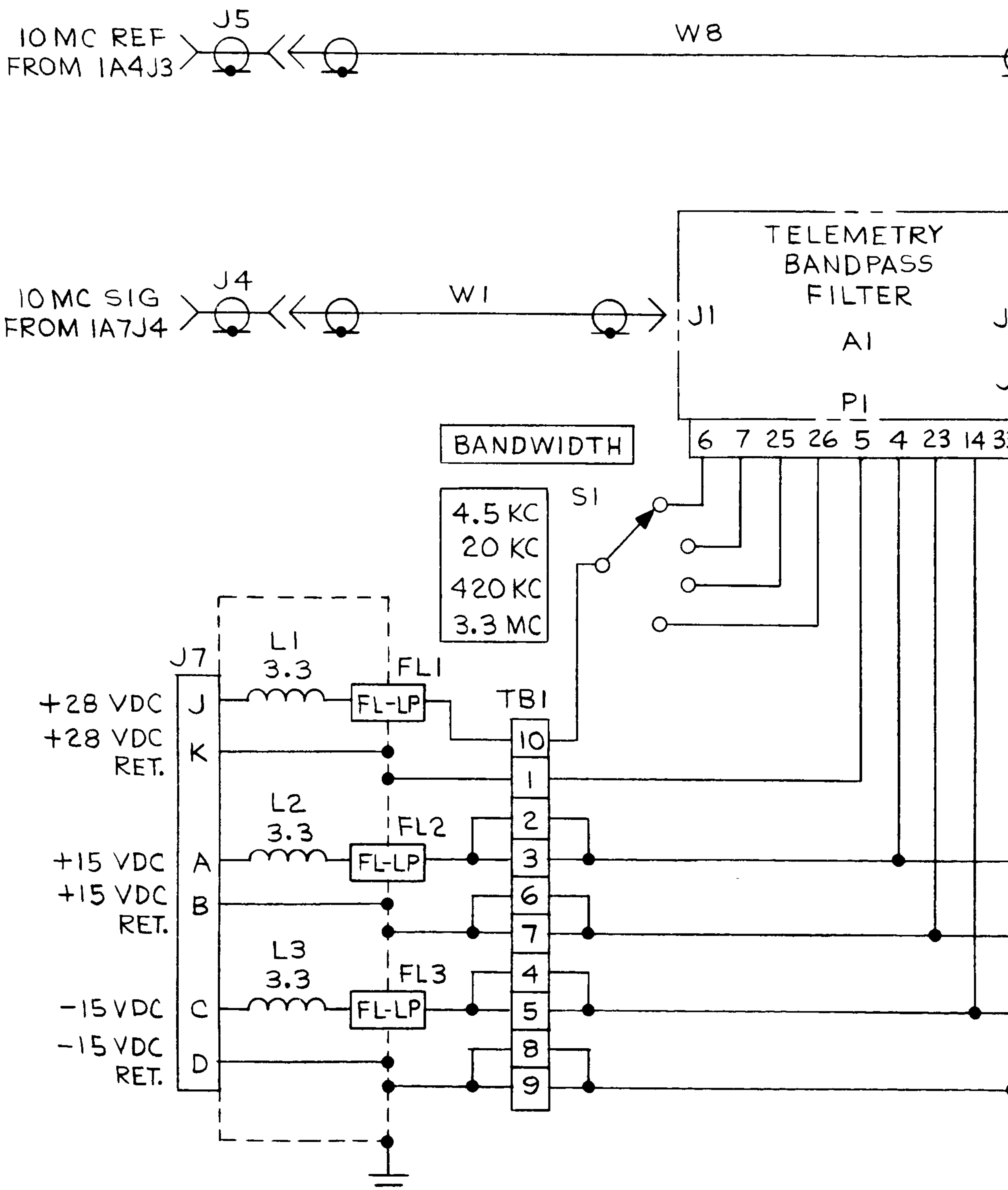
6-3. GSE, Signal Interconnection Diagram
(63-25441E)

NOTES

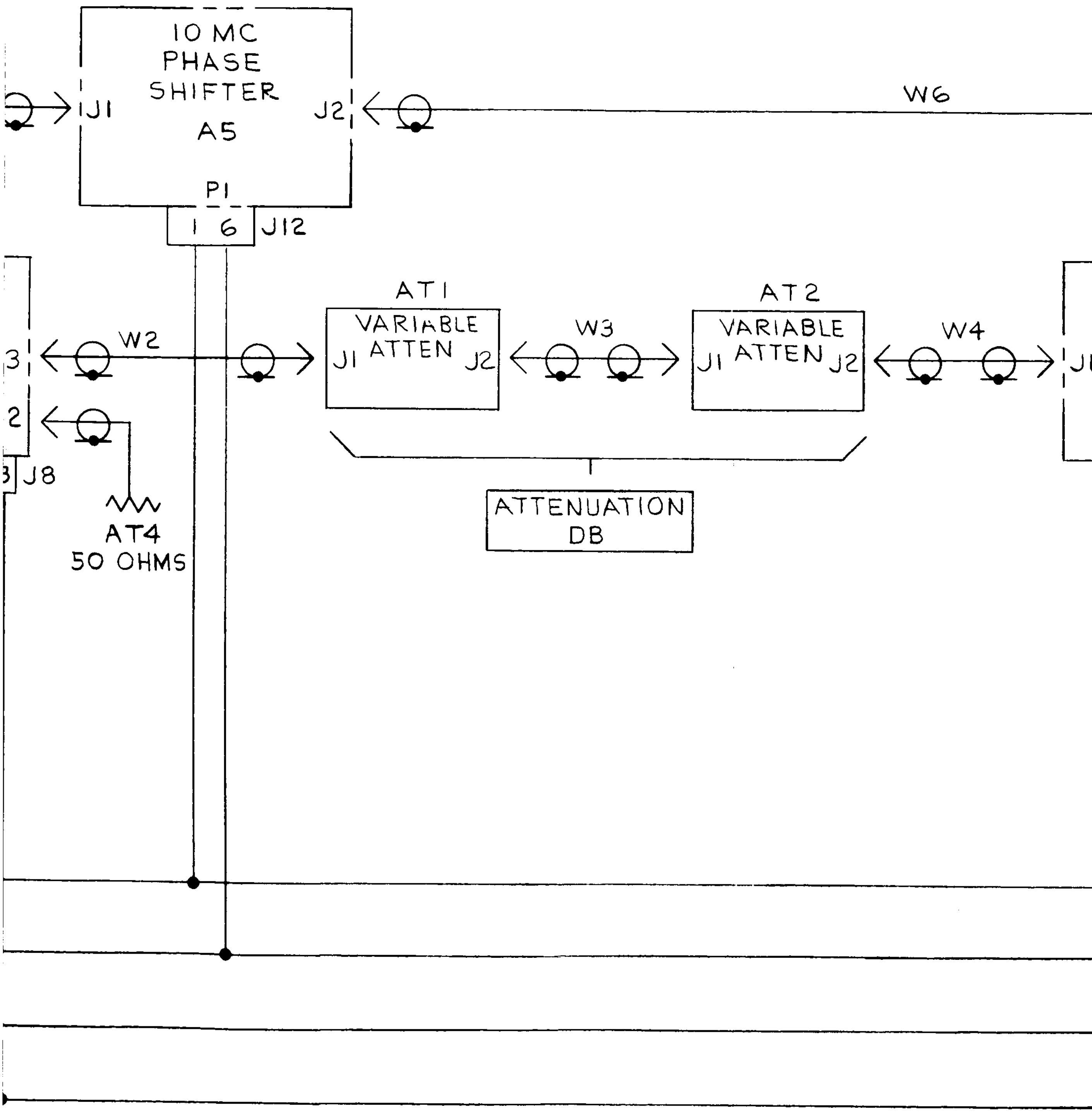
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION 1A2.

2. UNLESS OTHERWISE SPECIFIED:
   ALL INDUCTORS ARE IN UH.

3. ▭ INDICATES FRONT PANEL MARKING.



1


10 MC
PHASE
SHIFTER
A5
J1
J2
P1
1 6
J12
W6
W2
3
2
J8
AT4
50 OHMS
AT1
VARIABLE
ATTEN
J1
J2
W3
AT2
VARIABLE
ATTEN
J1
J2
W4
ATTENUATION
DB

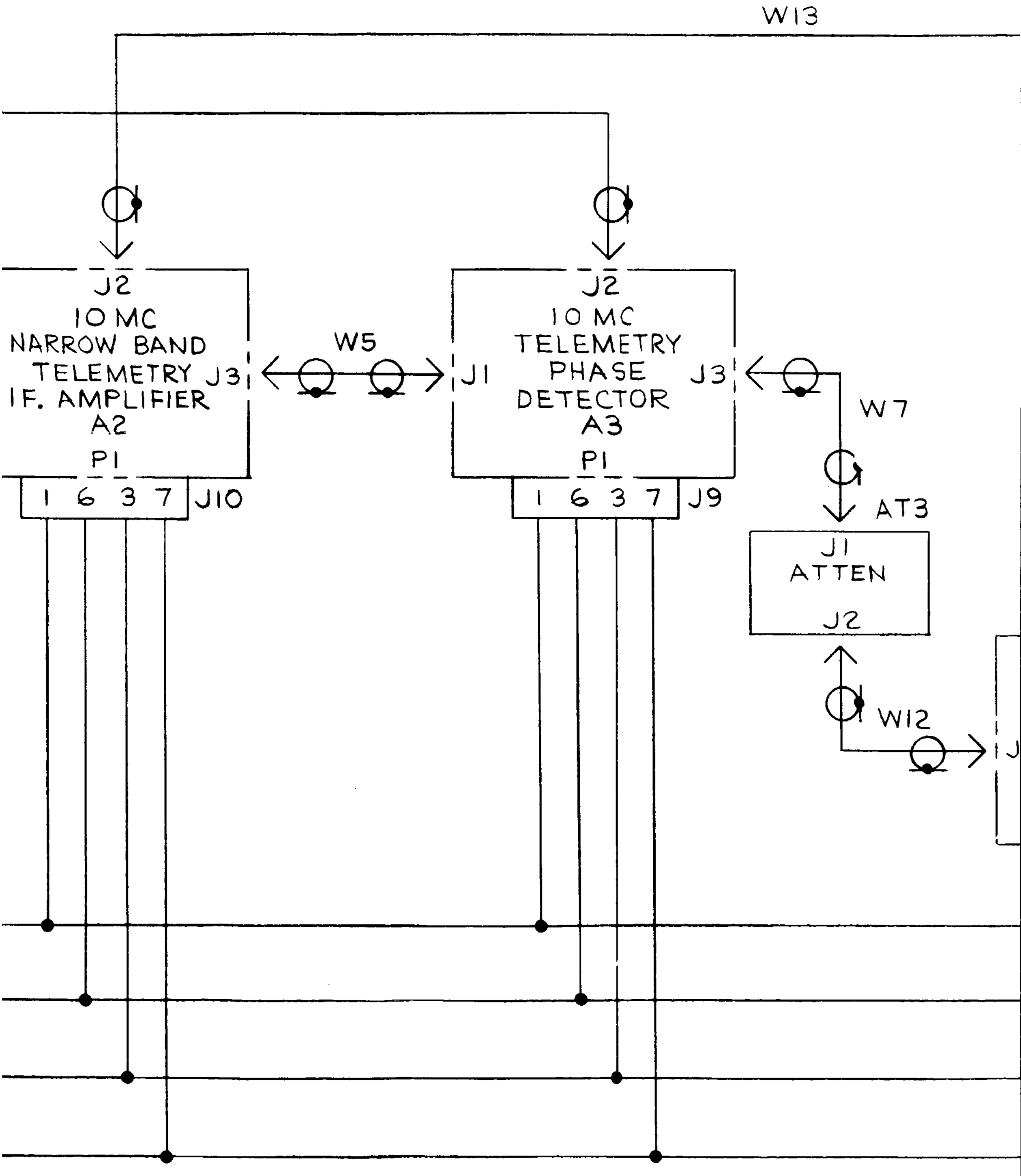
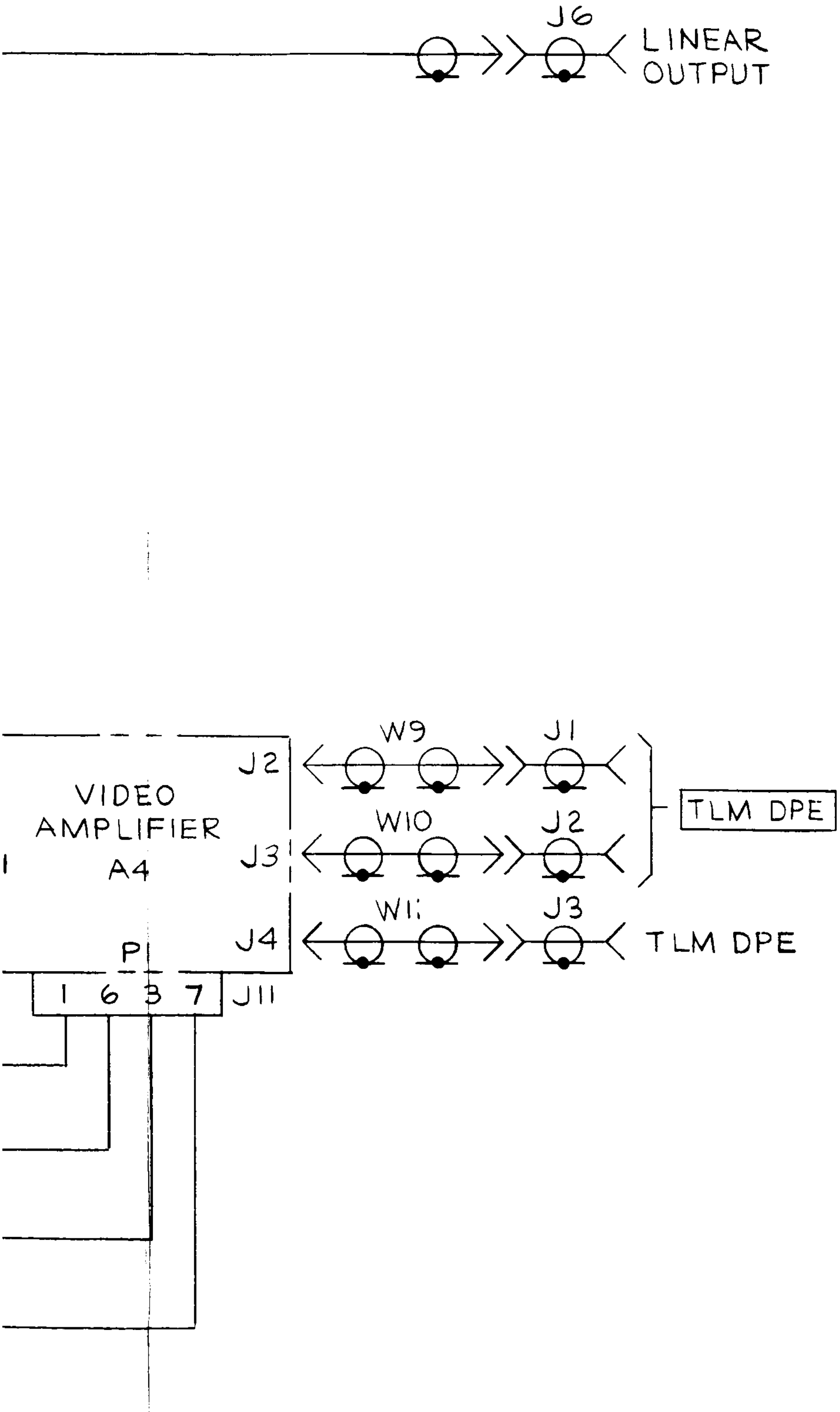
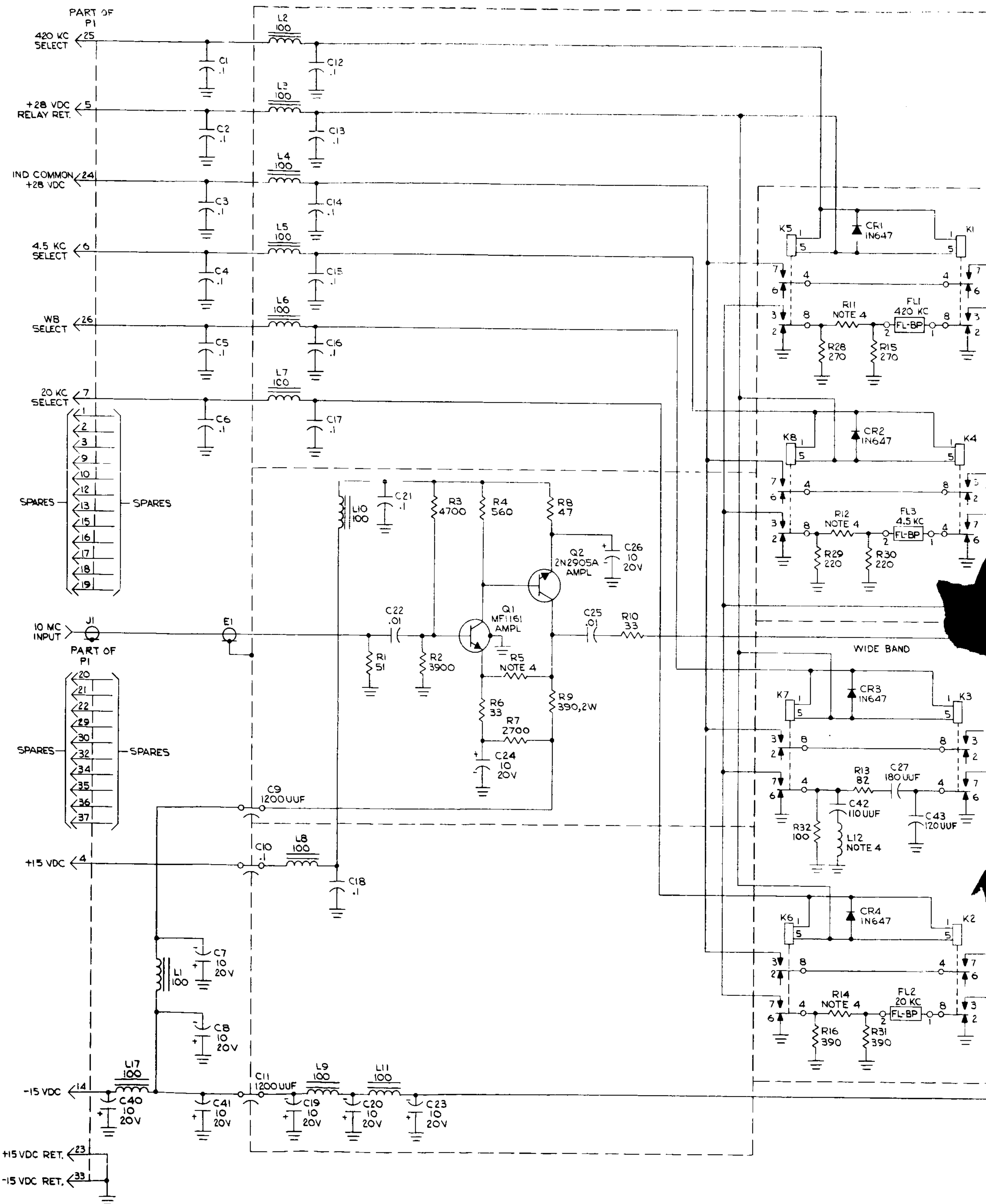


Figure 6-5. Telemetr



Narrow Band Subsystem (1A2), Schematic Diagram (63-25445E)

4


PART OF P1
420 KC SELECT
+28 VDC RELAY RET.
IND COMMON +28 VDC
4.5 KC SELECT
WB SELECT
20 KC SELECT
SPARES
10 MC INPUT
+15 VDC
-15 VDC
+15 VDC RET.
-15 VDC RET.
Q1 MF1161 AMPL
Q2 2N2905A AMPL
WIDE BAND
FL1 420 KC
FL3 4.5 KC
FL2 20 KC
FL-BP
NOTE 4

4. VALUE TO BE SELECTED IN TEST.

REFERENCE NO.	APPROXIMATE VALUE
R5	430
R11	22
R12	22
R14	10
R22	1600
L12	.47

3 ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4 WATT.
ALL CAPACITORS ARE IN UF
ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED, PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330530 (MOTOROLA NO. 01-23800D).

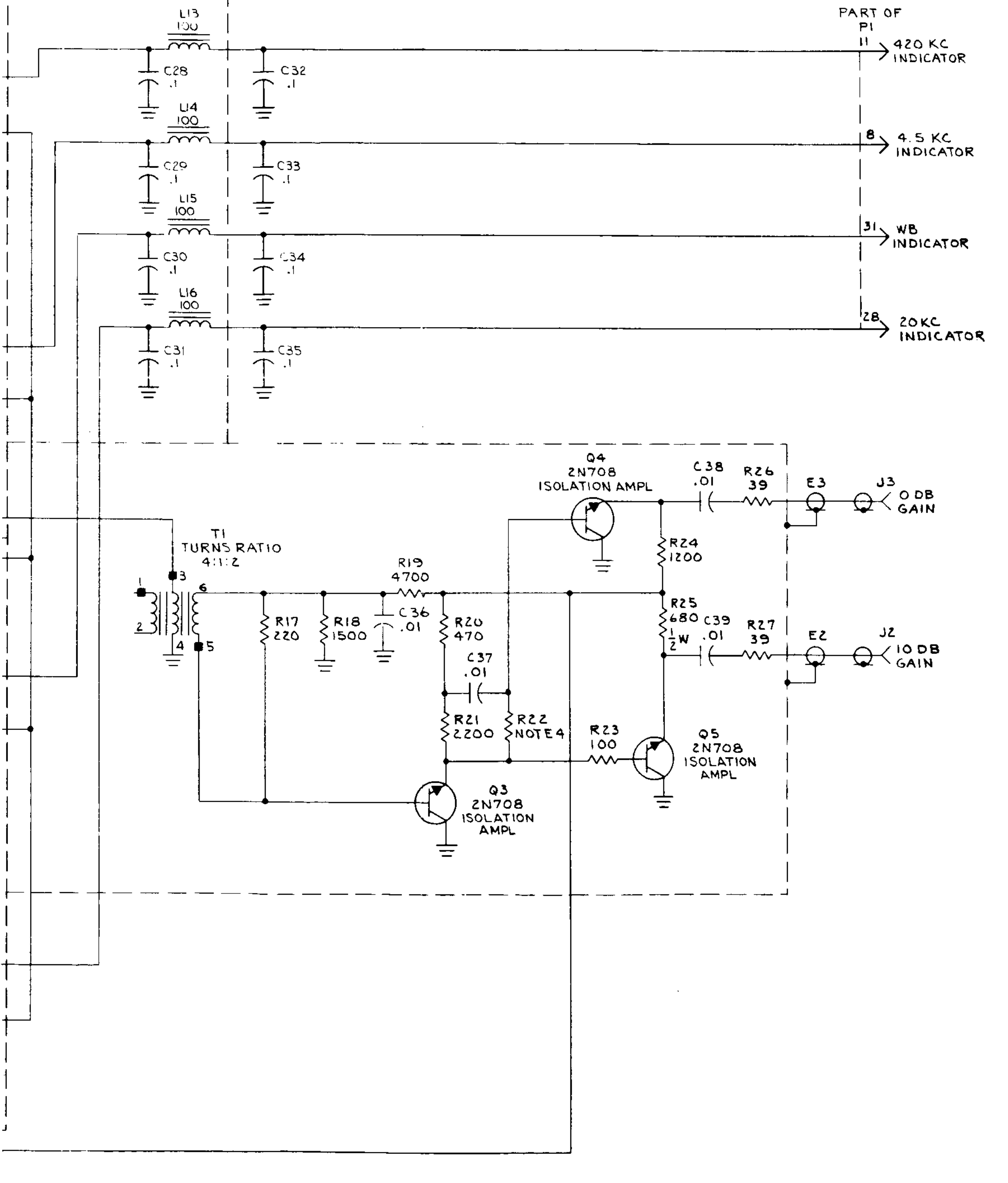


Figure 6-6. Telemetry Bandpass Filter (1A2A1, 1A3A1), Schematic Diagram (63-23881D)

NOTES

4. VALUE TO BE SELECTED IN TEST.

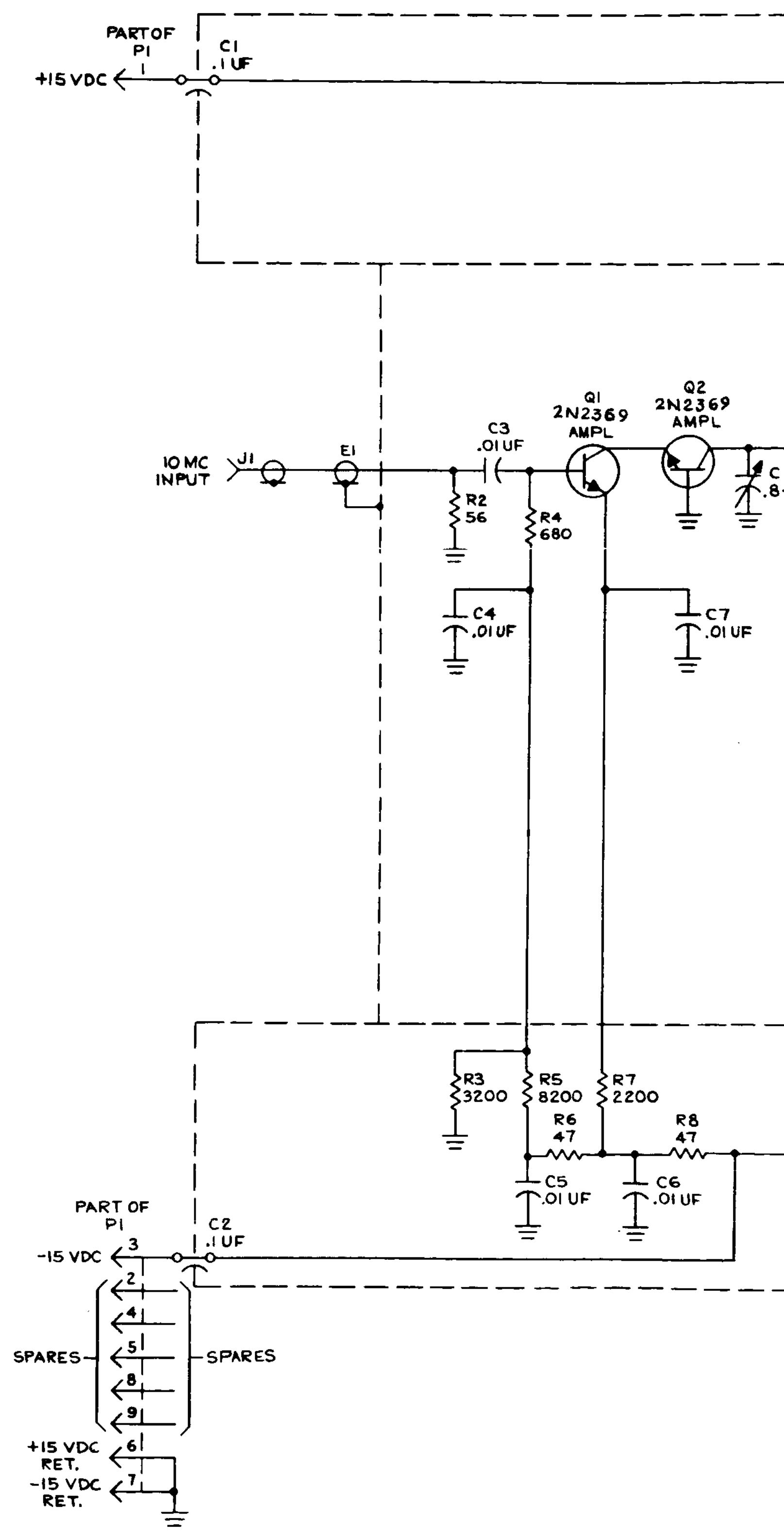
REFERENCE NO.	APPROXIMATE VALUE
C15	10
C17	10
C21	10
C28	10
C32	10
R16	120
C9	10
R32	330
R33	33
R34	330
R9	1K

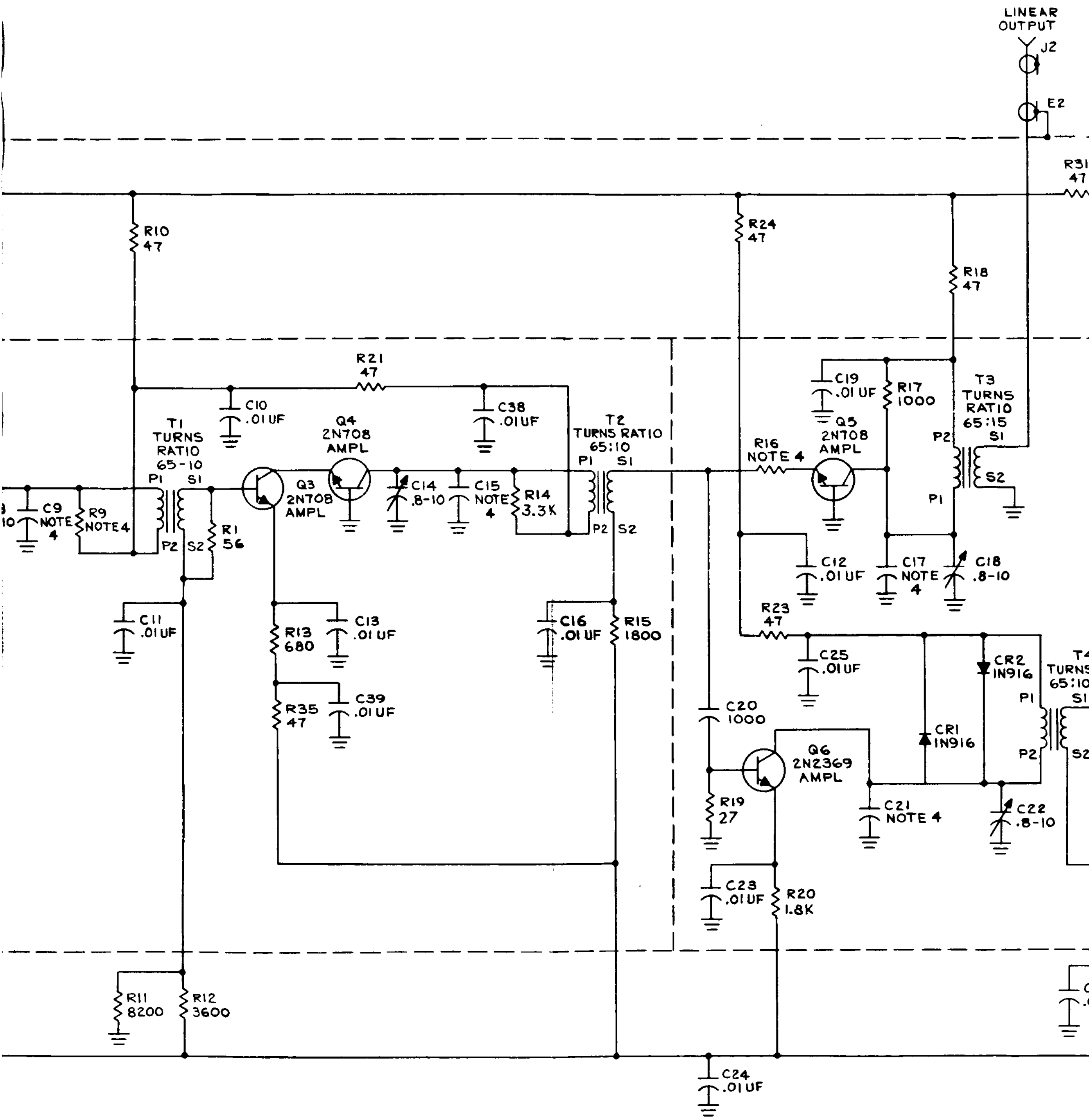
3. ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4 WATT.
ALL CAPACITORS ARE IN UUF.
ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330888.(MOTOROLA 01-242720).

NOTES: UNLESS OTHERWISE SPECIFIED




LINEAR OUTPUT
J2
E2
R31 47
R10 47
R24 47
R18 47
R21 47
C10 .01 UF
C38 .01 UF
T1 TURNS RATIO 65-10
P1 S1 P2 S2
Q4 2N708 AMPL
T2 TURNS RATIO 65:10
P1 S1 P2 S2
R16 NOTE 4
Q5 2N708 AMPL
C19 .01 UF
R17 1000
T3 TURNS RATIO 65:15
P2 S1 S2 P1
C9 NOTE 4
R9 NOTE 4
Q3 2N708 AMPL
C14 .8-10
C15 NOTE 4
R14 3.3K
R1 56
C12 .01 UF
C17 NOTE 4
C18 .8-10
C11 .01 UF
R13 680
C13 .01 UF
C16 .01 UF
R15 1800
R23 47
C25 .01 UF
CR2 IN916
R35 47
C39 .01 UF
C20 1000
Q6 2N2369 AMPL
CR1 IN916
P1 P2 S1 S2
R19 27
C21 NOTE 4
C22 .8-10
C23 .01 UF
R20 1.8K
R11 8200
R12 3600
C24 .01 UF

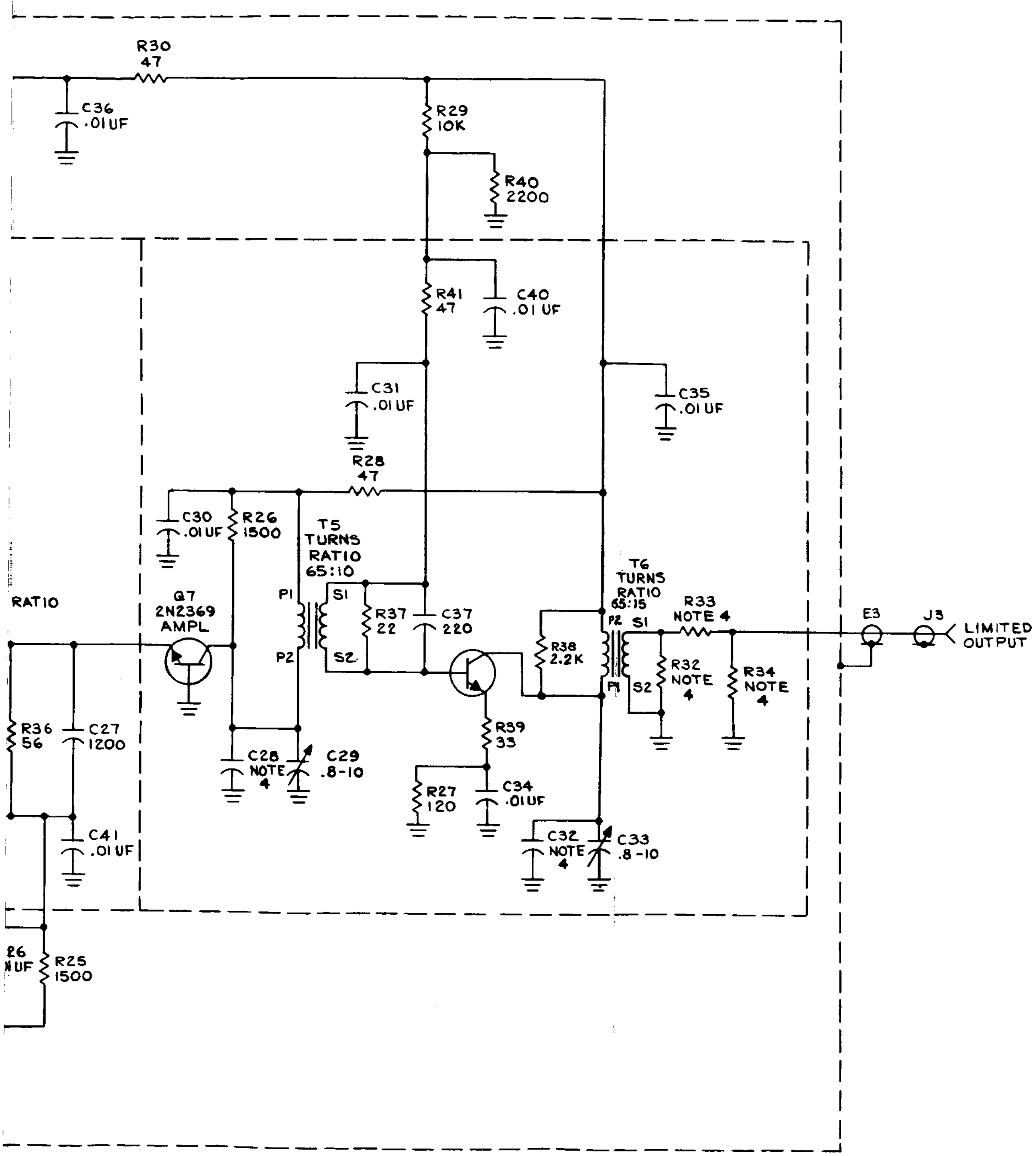


Figure 6-7. Narrow Band 10 MC IF Amplifier (1A2A2), Schematic Diagram (63-24038D)

5. VALUE TO BE SELECTED IN TEST

REFERENCE NO.	APPROXIMATE VALUE
R1	120
R13	22
R19	150
C4	56
C12	5
C21	39
C34	15
C35	100

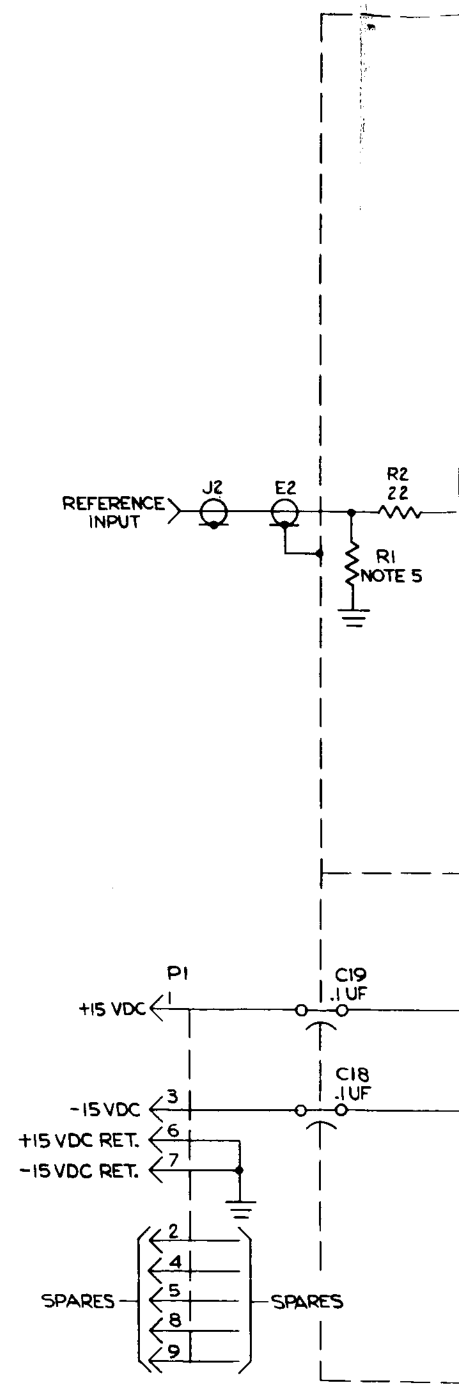
4. CR1 AND CR2 ARE A MATCHED PAIR.

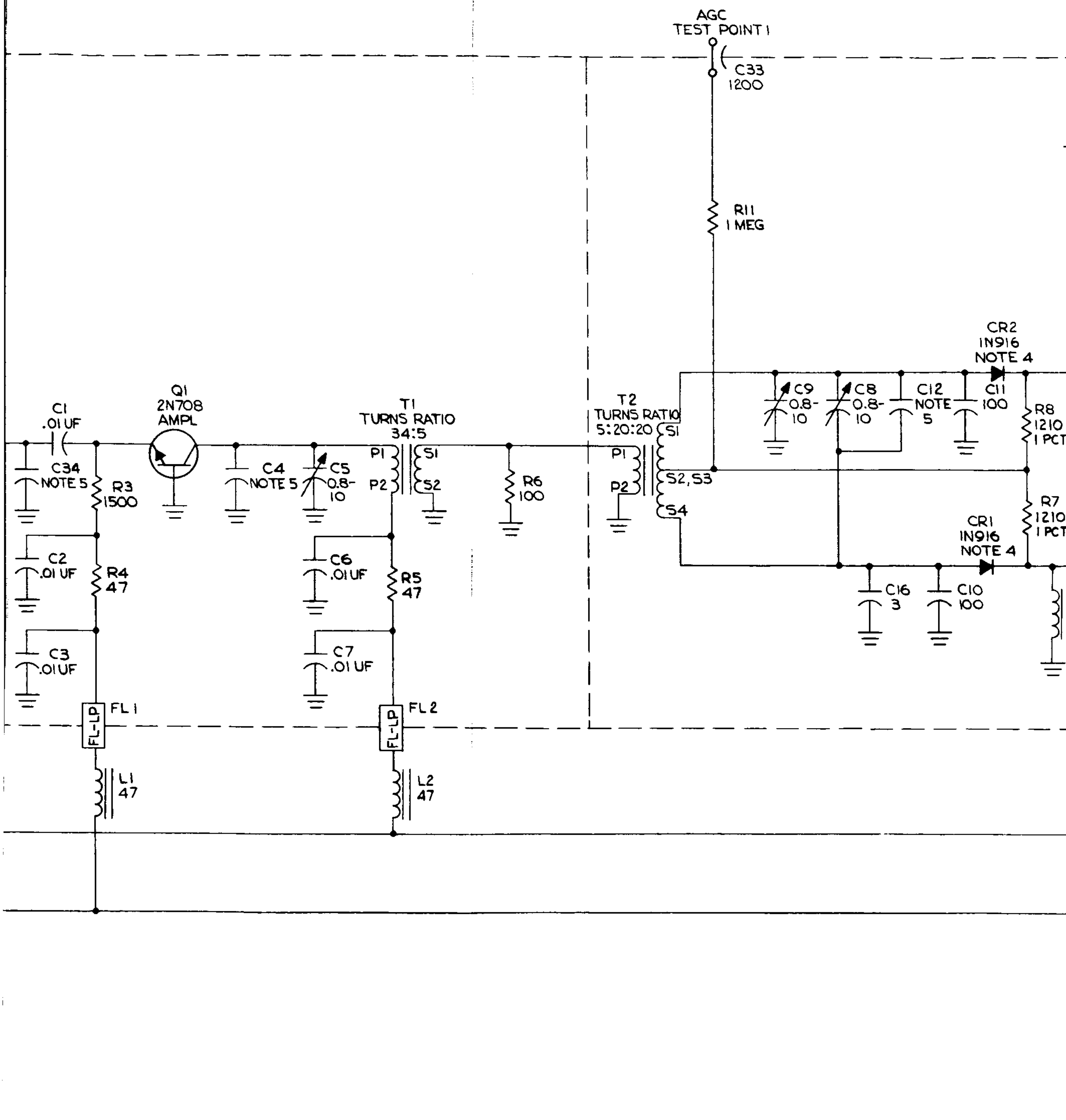
3. ALL RESISTORS ARE IN OHMS, ± 5 PCT, 1/4 WATT.
• ALL CAPACITORS ARE IN UUF.
ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED, PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9331050 (MOTOROLA NO. 01-24273D).

NOTES: UNLESS OTHERWISE SPECIFIED




AGC
TEST POINT 1
C33
1200
R11
1 MEG
CR2
1N916
NOTE 4
C1
.01 UF
Q1
2N708
AMPL
T1
TURNS RATIO
34:5
T2
TURNS RATIO
5:20:20
C9
0.8-
10
C8
0.8-
10
C12
NOTE
5
C11
100
R8
1210
1 PCT
C34
NOTE 5
R3
1500
C4
NOTE 5
C5
0.8-
10
P1
P2
S1
S2
R6
100
S2,S3
S4
R7
1210
1 PCT
CR1
1N916
NOTE 4
C2
.01 UF
R4
47
C6
.01 UF
R5
47
C16
3
C10
100
C3
.01 UF
C7
.01 UF
FL 1
FL-LP
FL 2
L1
47
L2
47

2

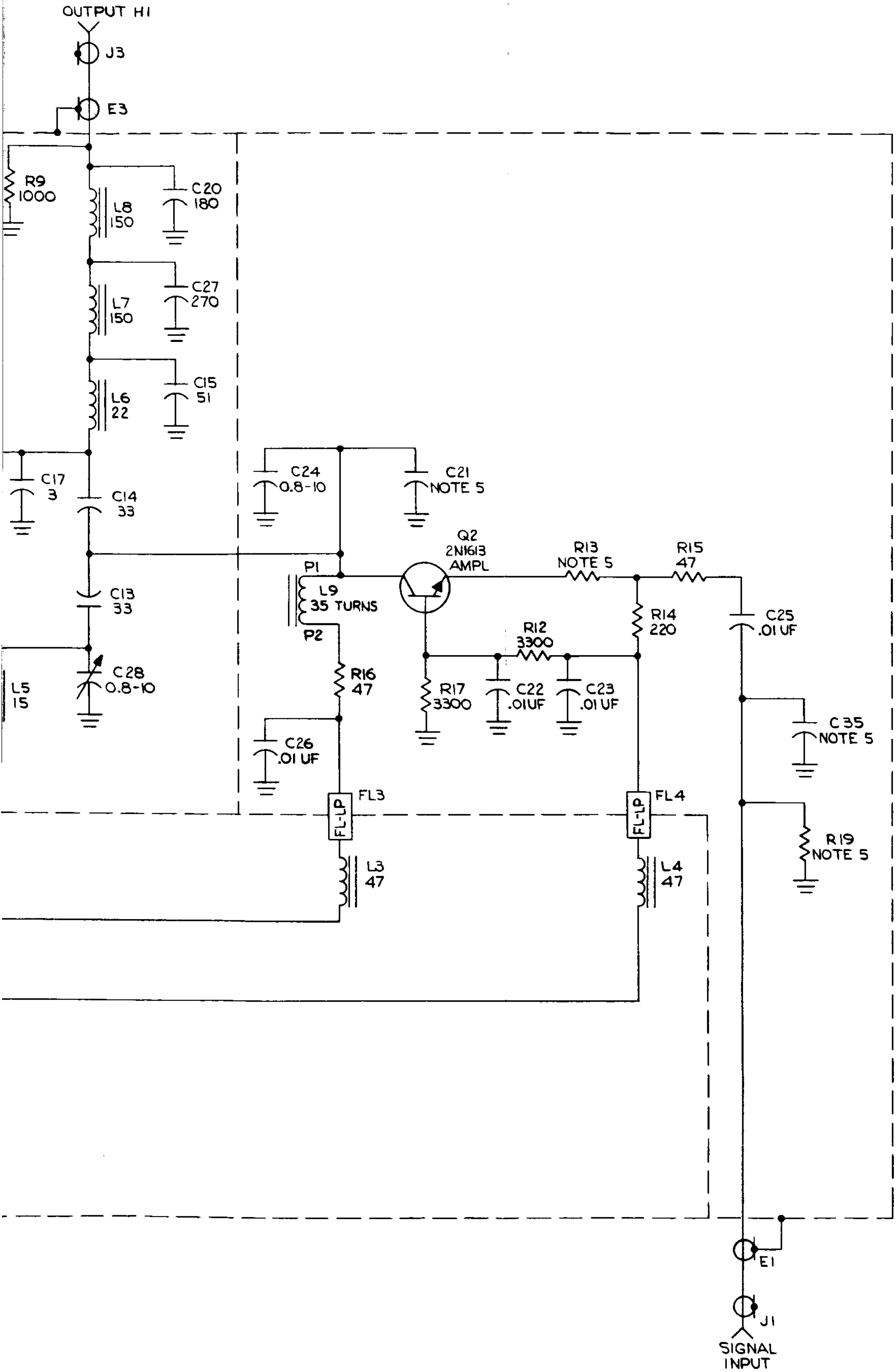
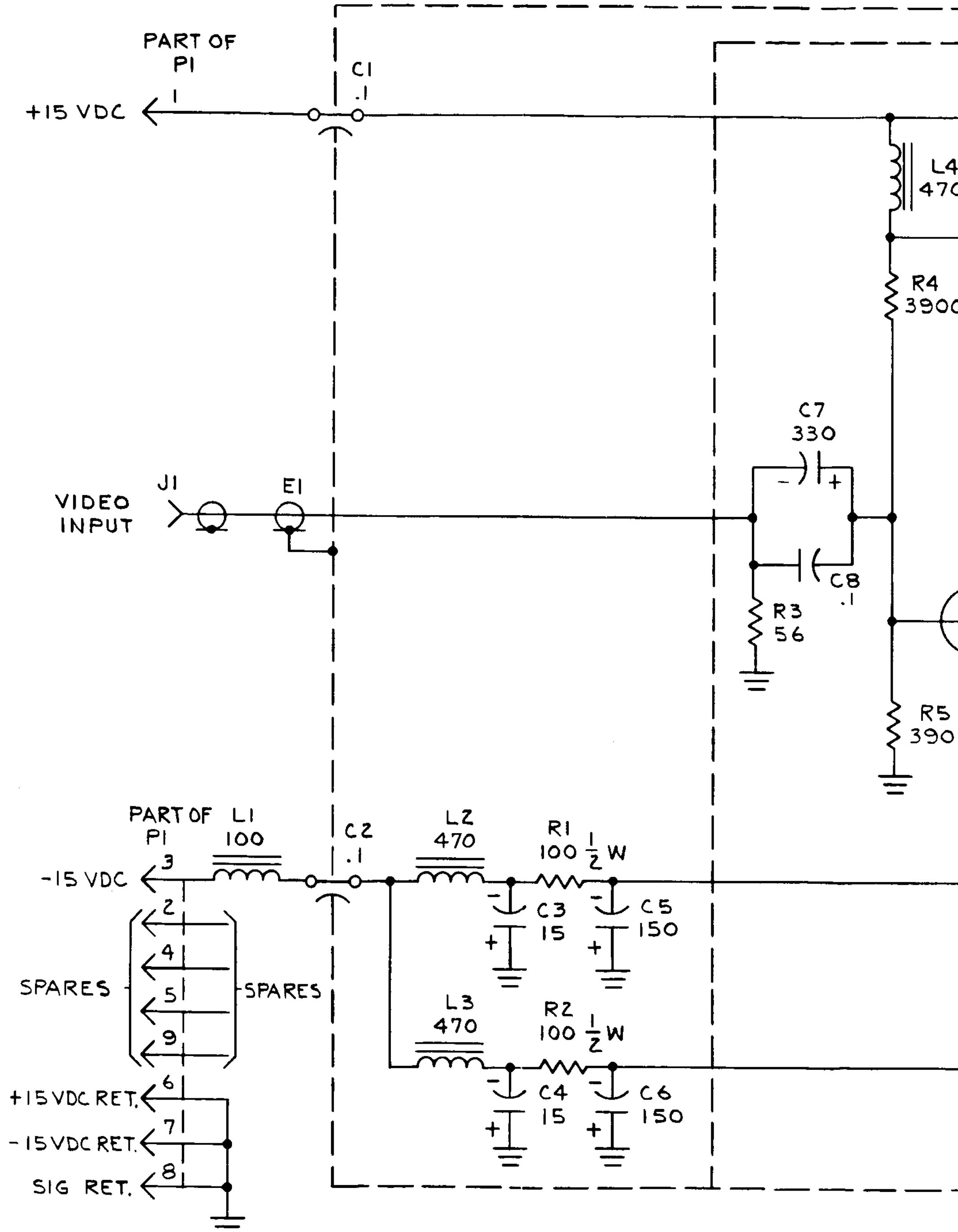
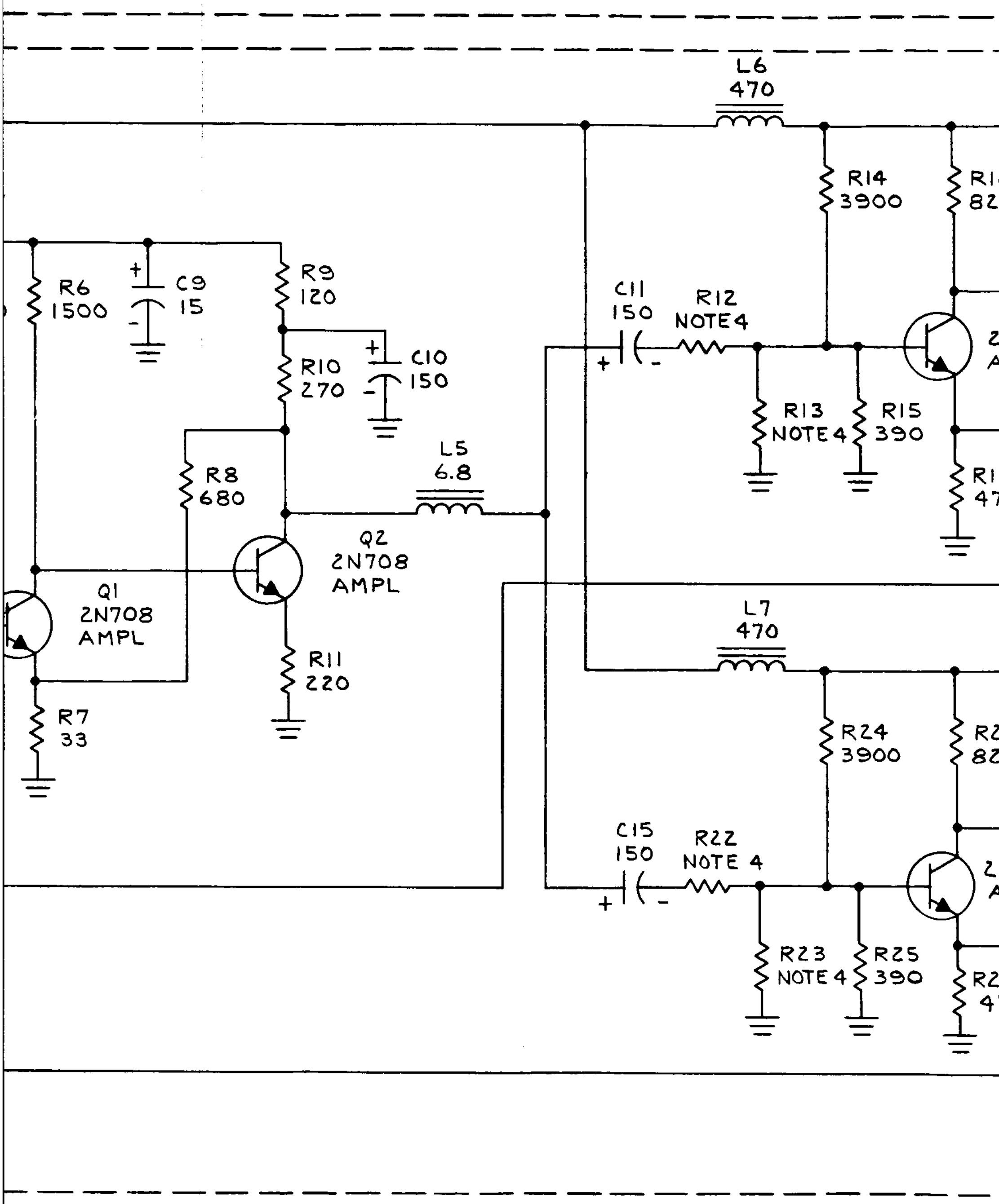


Figure 6-8. 10 MC Phase Detector (1A2A3), Schematic Diagram (63-25032E)



2. REFERENCE DESIGNATIONS ARE
IGNATIONS WITH UNIT NUMBER A

1. FOR ASSEMBLY SEE DRAWING D
01-23853D).



4. VALUES TO BE SELECTED IN TEST.

REFERENCE DESIGNATION	APPROXIMATE VALUE
R12, R22	1K
R13, R23	10K
R21, R31	33

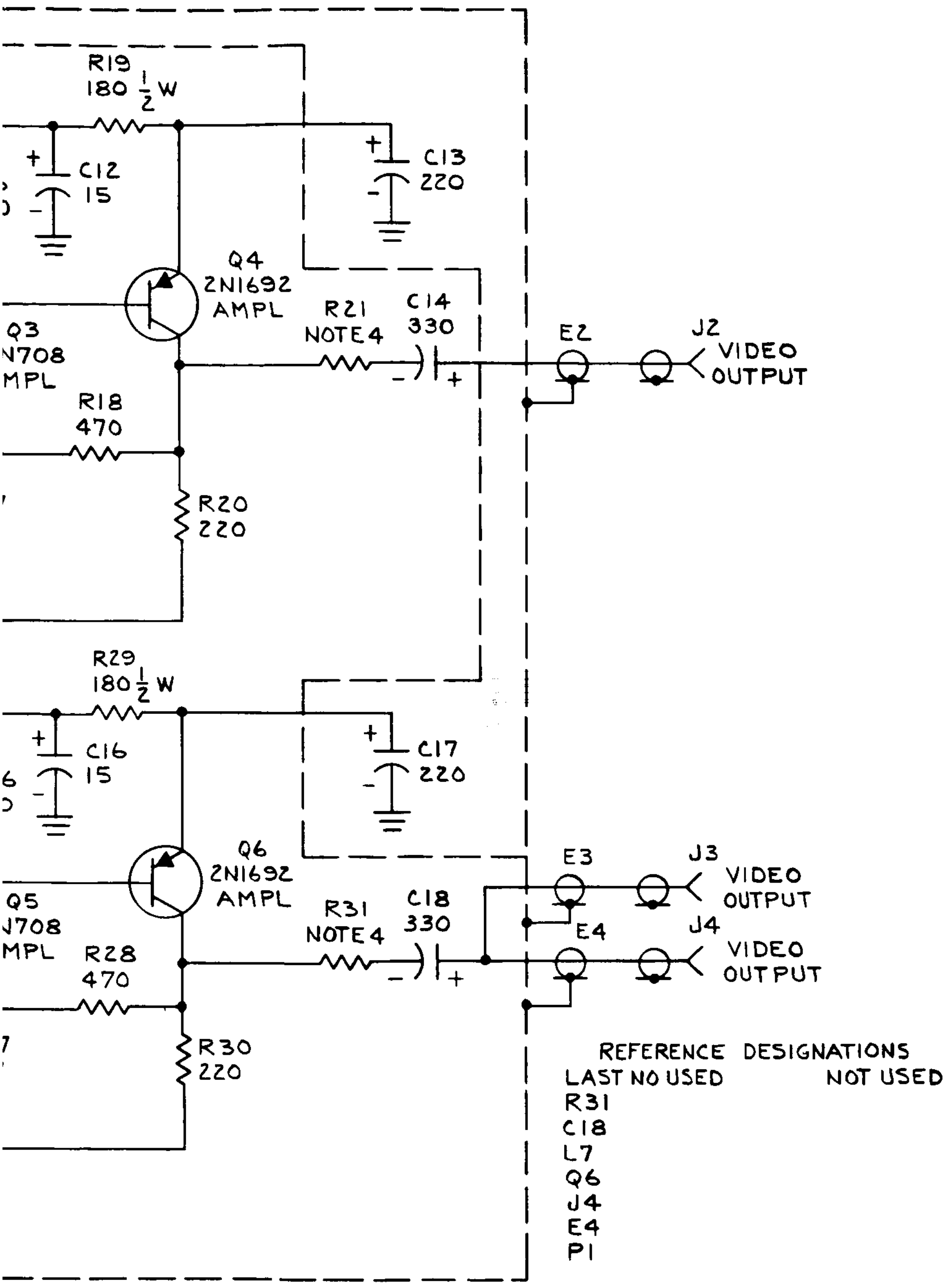
ABBREVIATED. PREFIX THE DES-
ND ASSEMBLY DESIGNATION.

330547 (MOTOROLA NO.

3. ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4 WATT.
ALL CAPACITORS ARE IN UF.
ALL INDUCTORS ARE IN UH.

Fig

2



ıre 6-9. Video Amplifier (1A2A4), Schematic Diagram
(63-23883D)

4. VALUE TO BE SELECTED IN TEST.

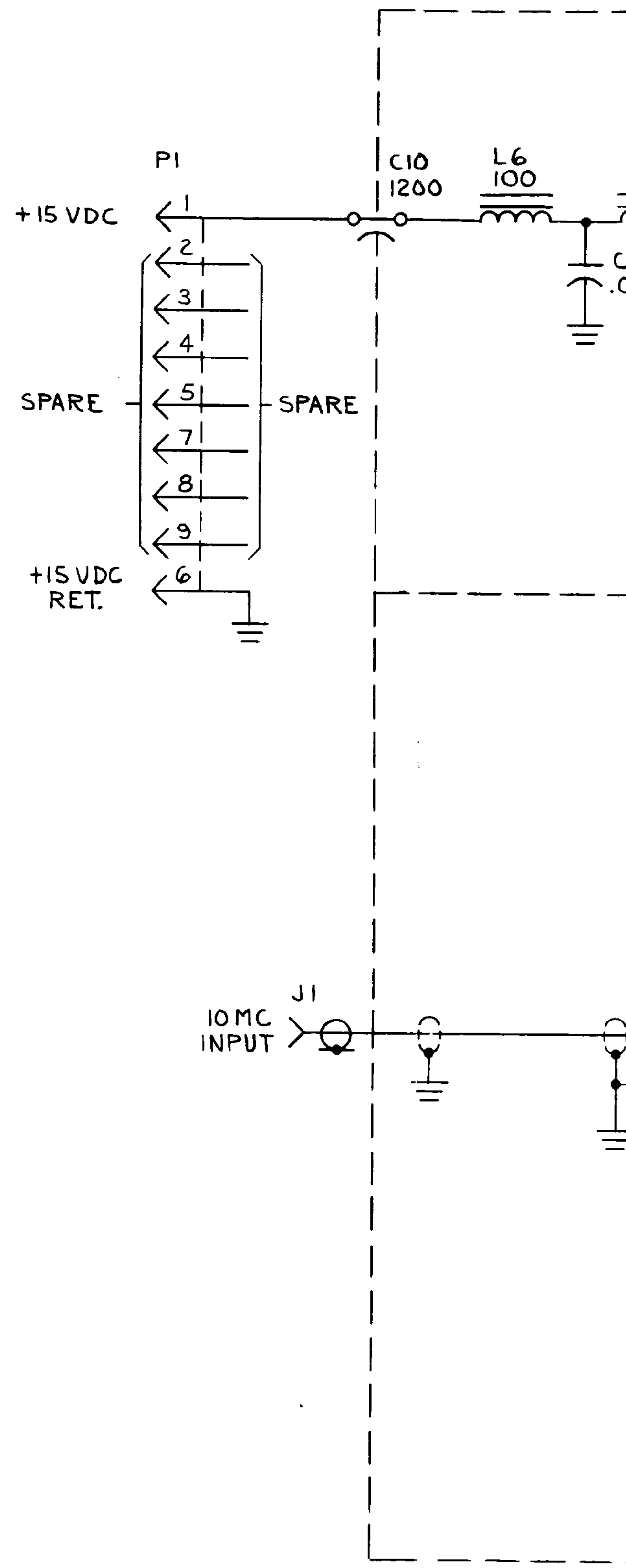
REFERENCE NO.	APPROXIMATE VALUE
R23	56

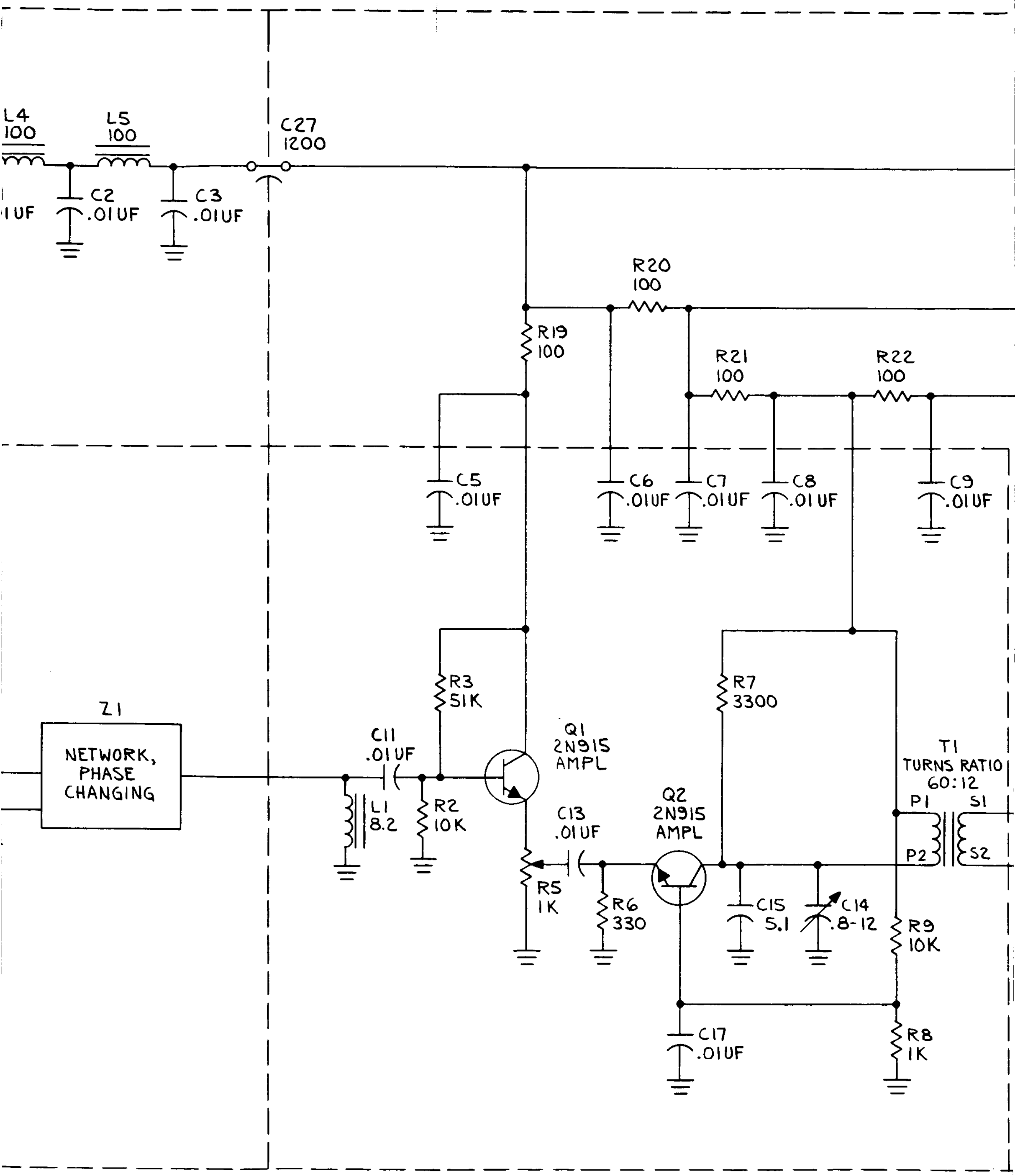
3. ALL RESISTORS ARE IN OHMS, (5 PCT, 1/4 WATT.)
   ALL CAPACITORS ARE IN UUF.
   ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED, PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING J9330524 (MOTOROLA NO. 01-23793D).

NOTES: UNLESS OTHERWISE SPECIFIED





L4
100
.01UF
L5
100
C2
.01UF
C3
.01UF
C27
1200
R20
100
R19
100
R21
100
R22
100
C5
.01UF
C6
.01UF
C7
.01UF
C8
.01UF
C9
.01UF
R3
51K
R7
3300
Z1
NETWORK, PHASE CHANGING
C11
.01UF
Q1
2N915
AMPL
T1
TURNS RATIO
60:12
P1
S1
P2
S2
L1
8.2
R2
10K
C13
.01UF
Q2
2N915
AMPL
R5
1K
R6
330
C15
5.1
C14
.8-12
R9
10K
C17
.01UF
R8
1K

2

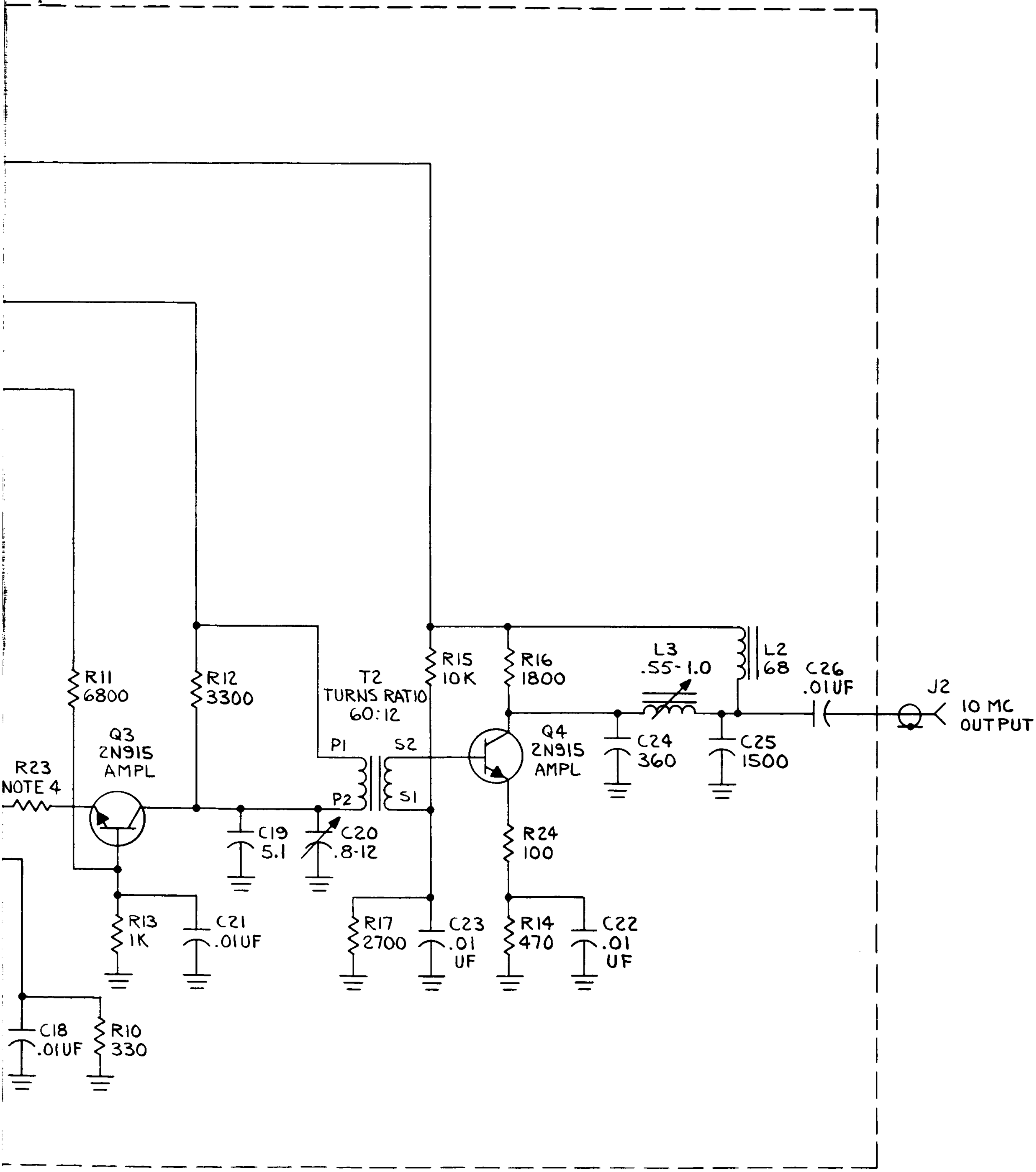


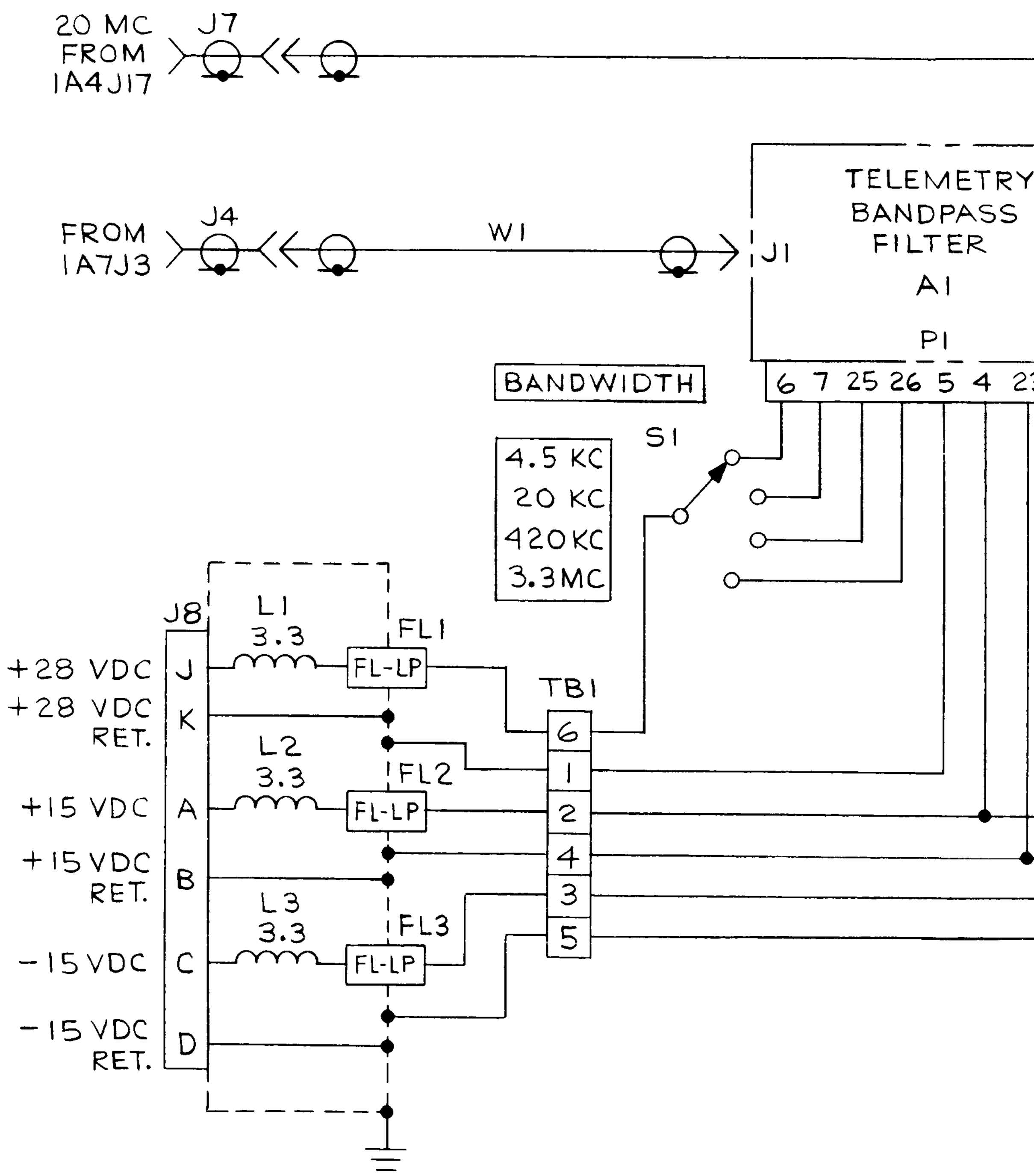
Figure 6-10. 10 MC Phase Shifter (1A2A5, 1A5A3, and 1A10A1), Schematic Diagram (63-23860D)

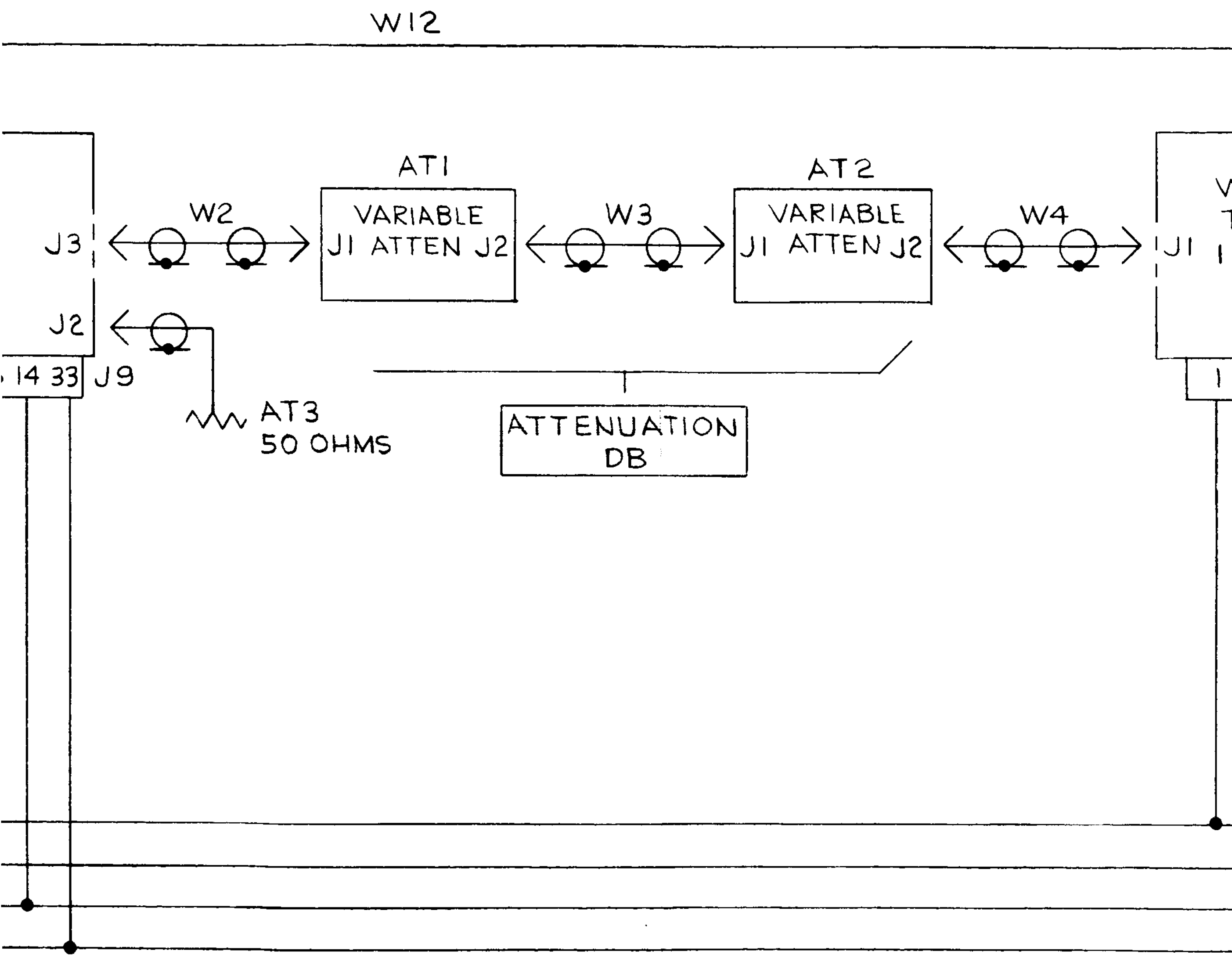
NOTES

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION 1A3.

2. UNLESS OTHERWISE SPECIFIED:
   ALL INDUCTORS ARE IN UH.

3. ▭ INDICATES FRONT PANEL MARKING.




W12
AT1
VARIABLE
J1 ATTEN J2
AT2
VARIABLE
J1 ATTEN J2
W2
W3
W4
J3
J2
J1
14 33 J9
AT3
50 OHMS
ATTENUATION
DB

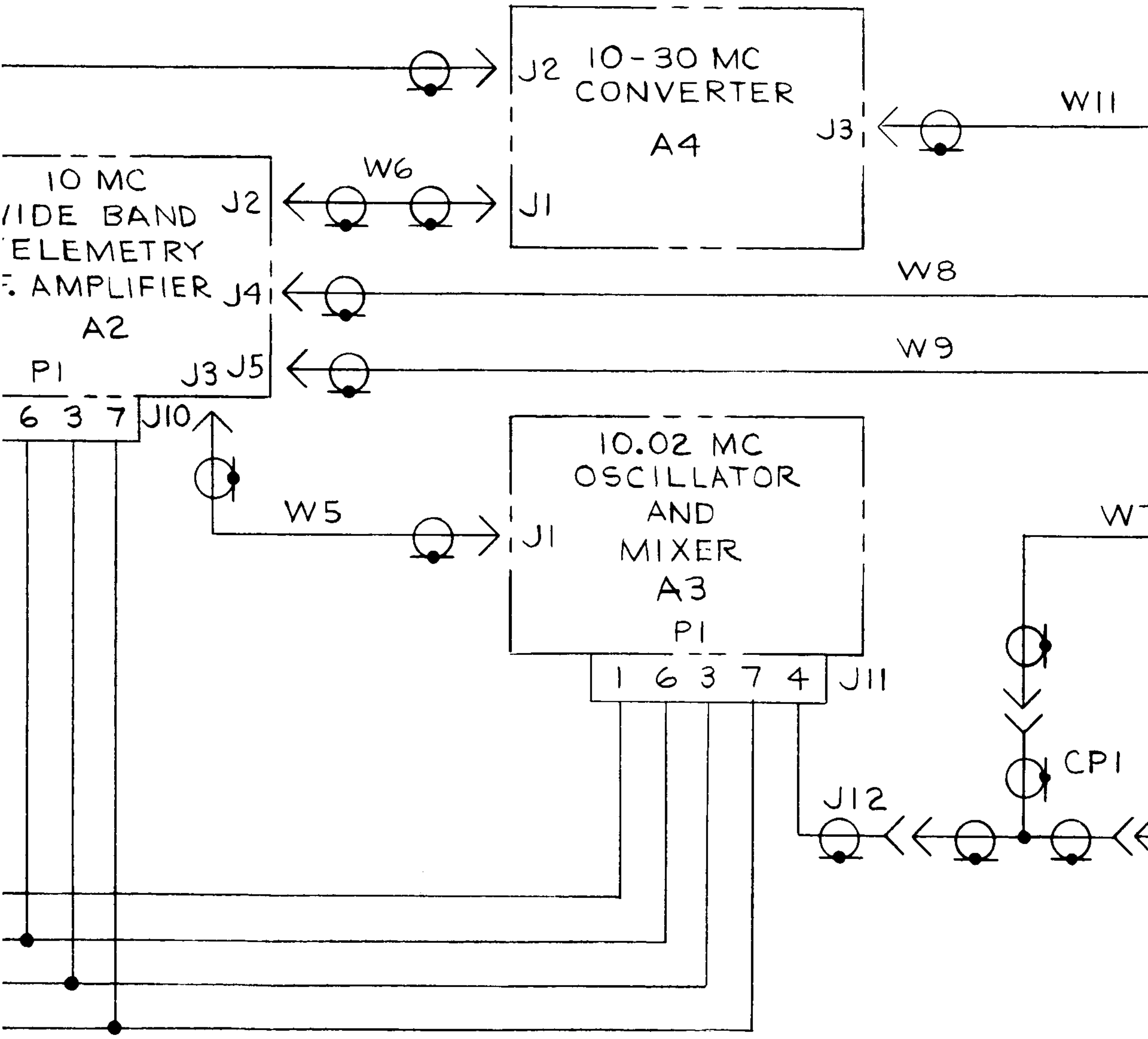
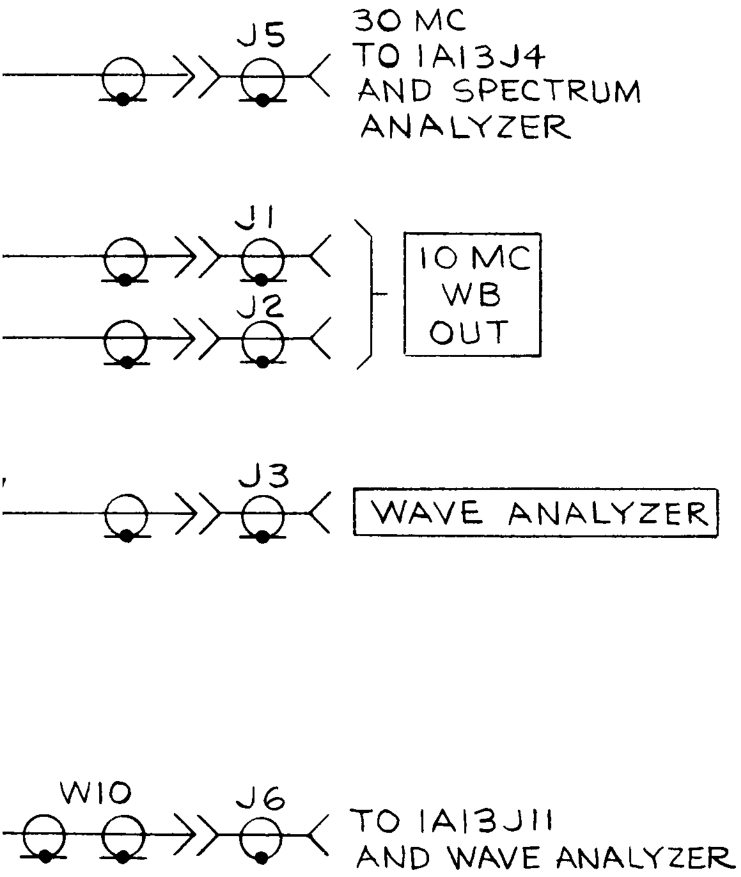


Figure 6-11. Telemetry Wide Ban



d Subsystem (1A3), Schematic Diagram (63-25446E)

4. VALUE TO BE SELECTED IN TEST

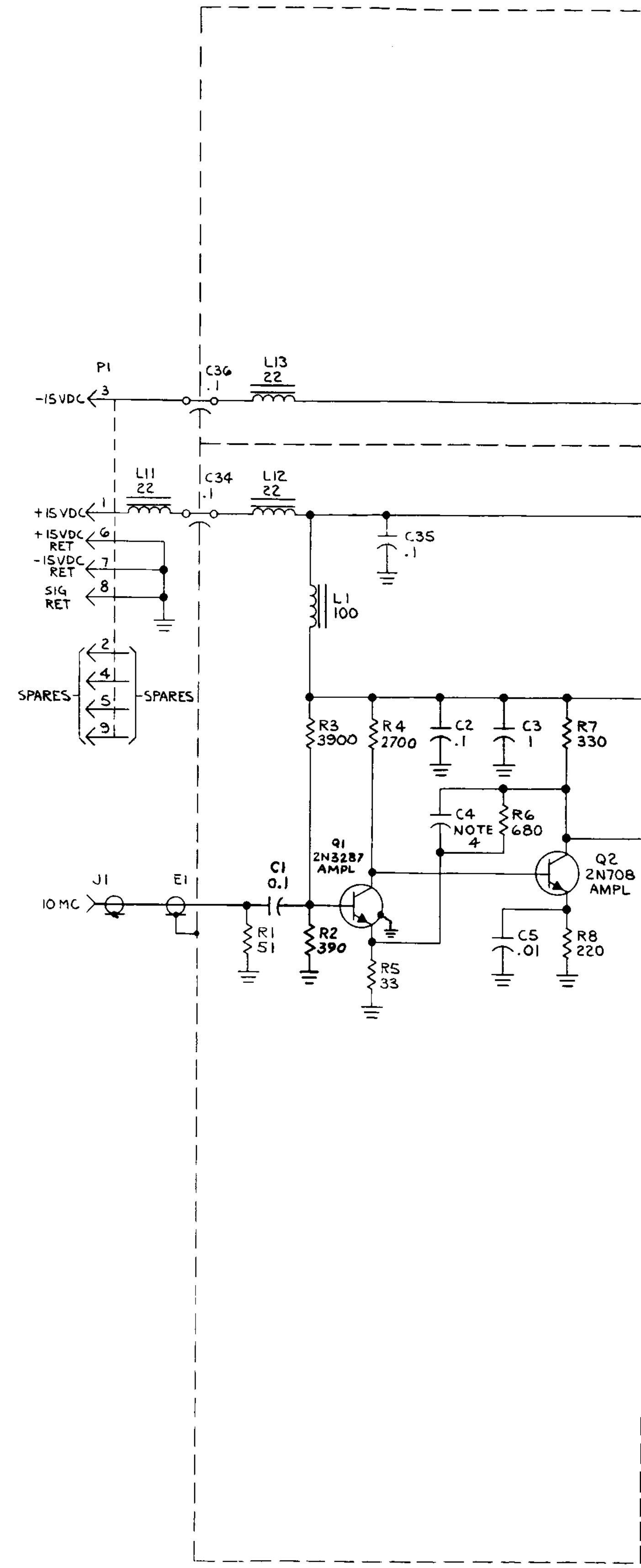
REFERENCE NO.	APPROXIMATE VALUE
R16	82
R26	82
R36	82
R46	82
C4	5
C6	82
C8	5

3. ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330526 (MOTOROLA NO. 01-23795D).

NOTES: UNLESS OTHERWISE SPECIFIED



2

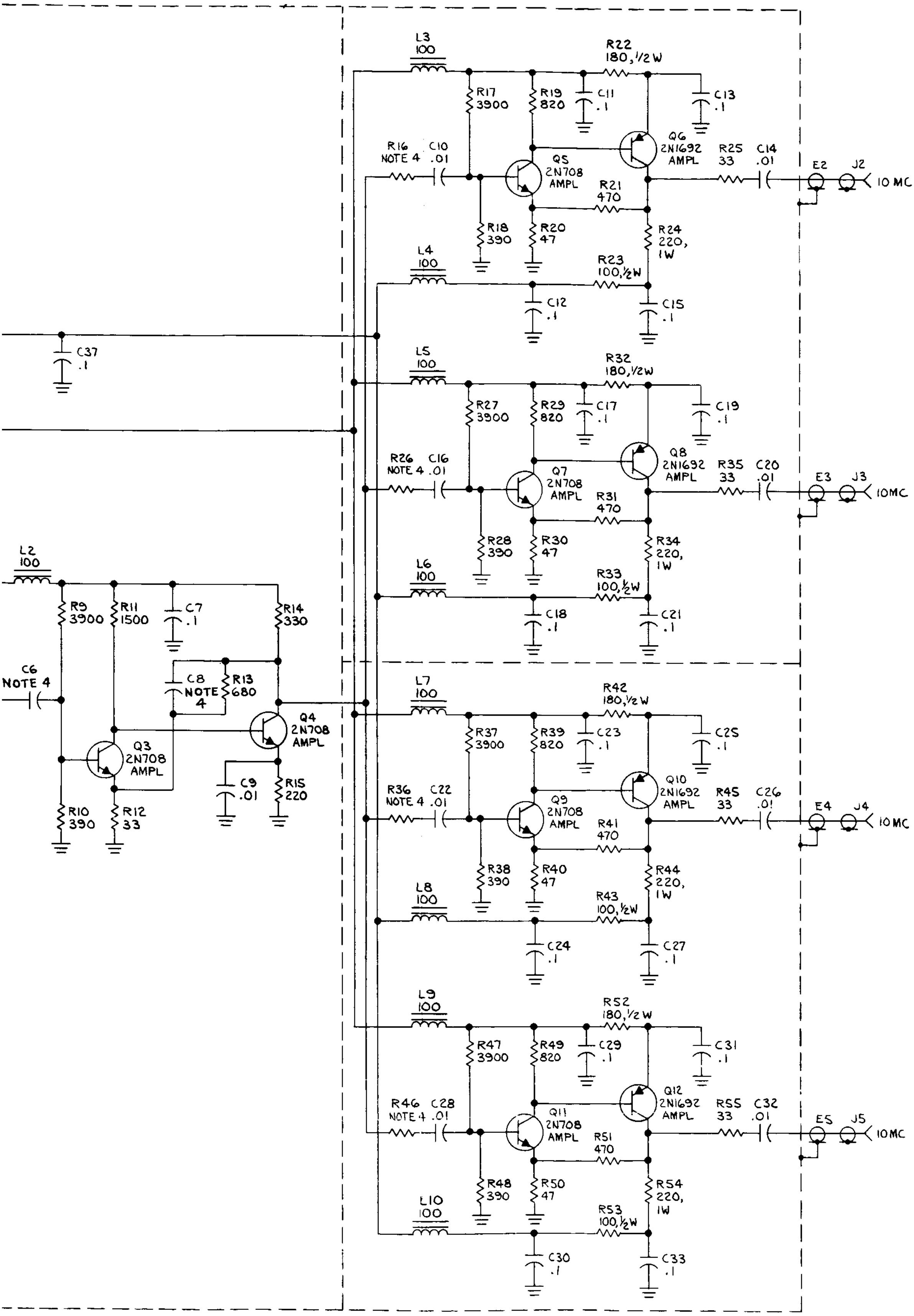


Figure 6-13. 10.02 MC Mixer-Oscillator (1A3A3), Schematic Diagram (63-23893D)

4. VALUE TO BE SELECTED IN TEST.

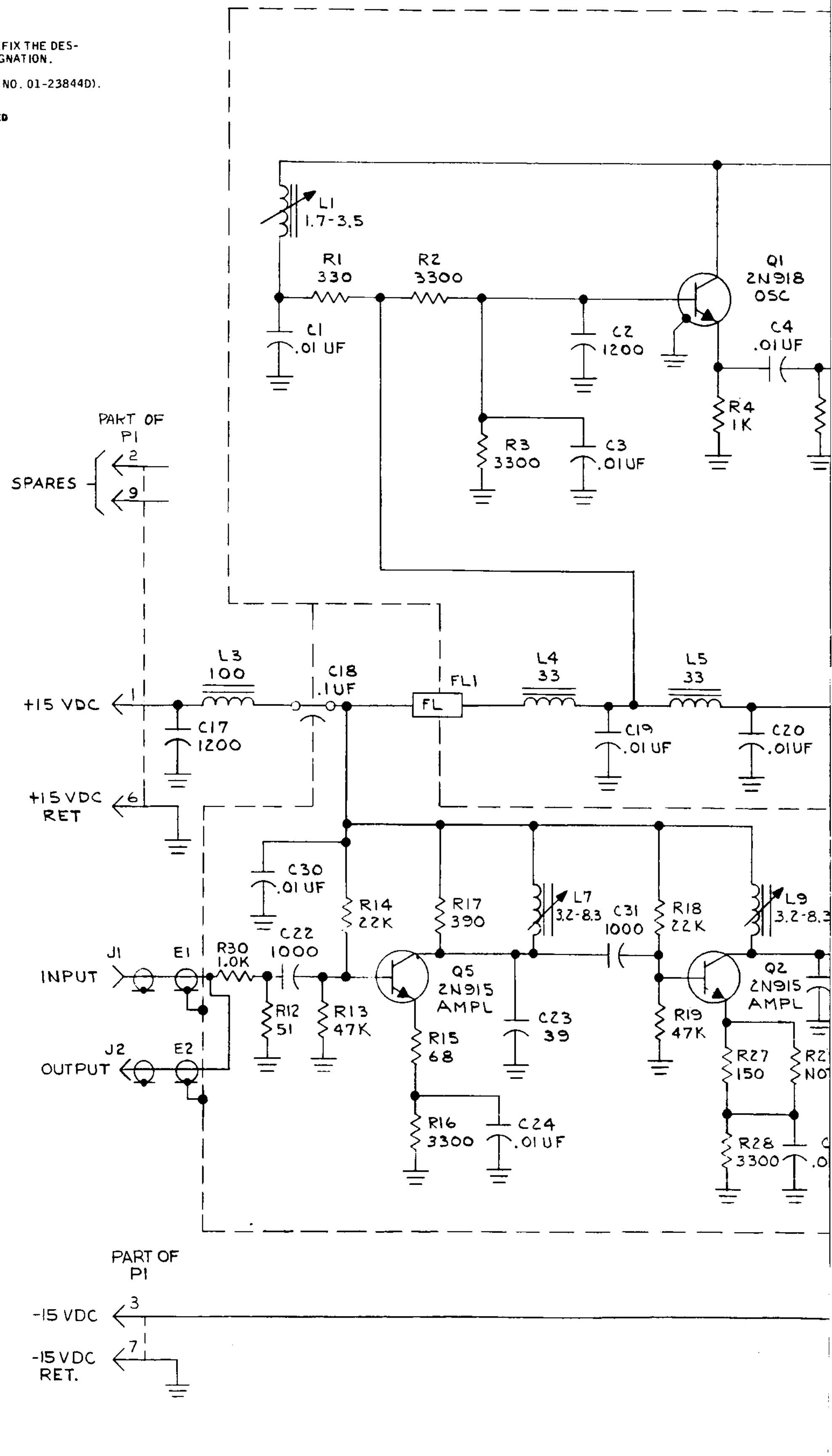
REFERENCE NO.	APPROXIMATE VALUE
R29	150

3. ALL RESISTORS ARE IN OHMS, ± 5 PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UUF.
   ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330538 (MOTOROLA NO. 01-23844D).

NOTES: UNLESS OTHERWISE SPECIFIED



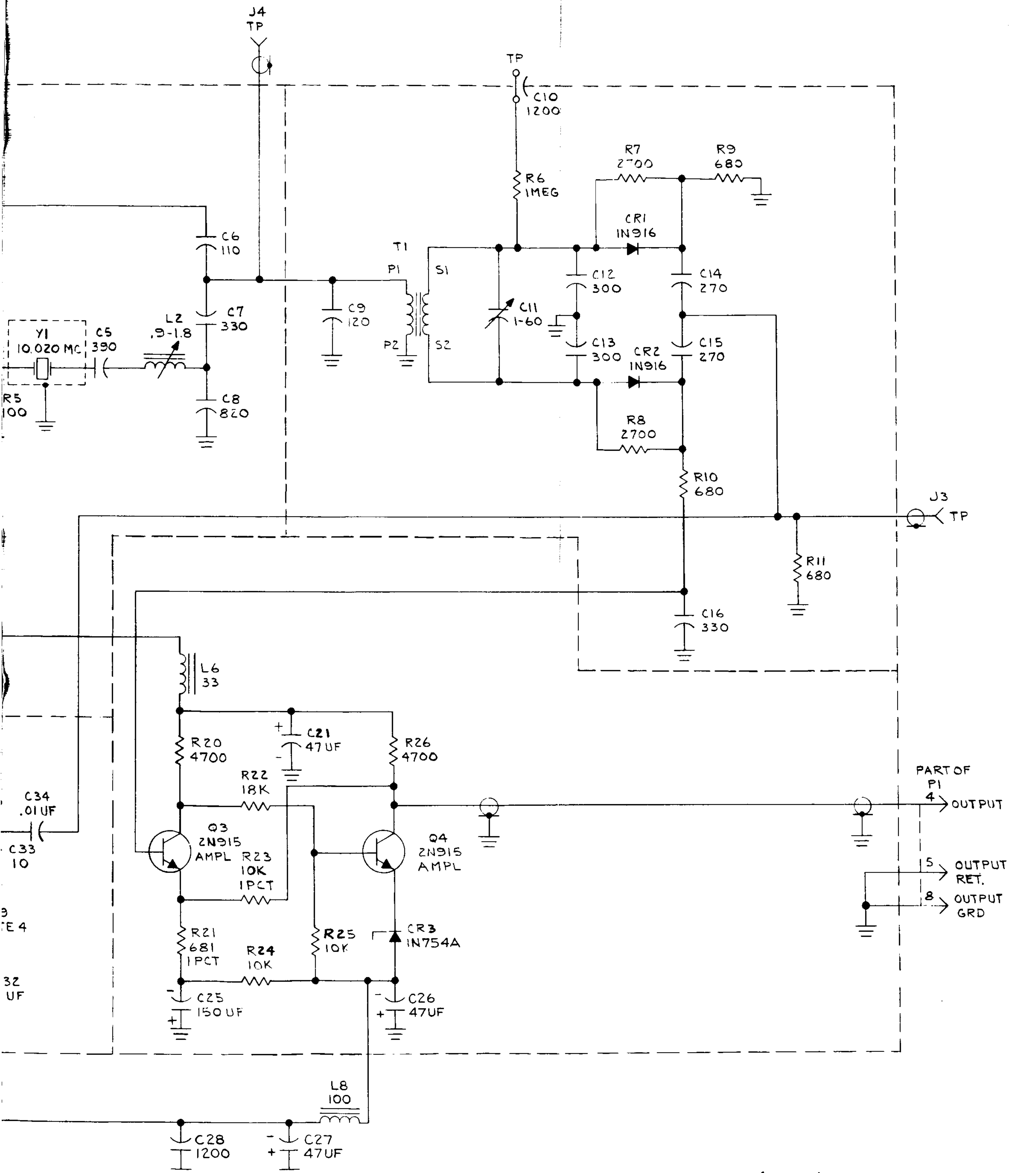
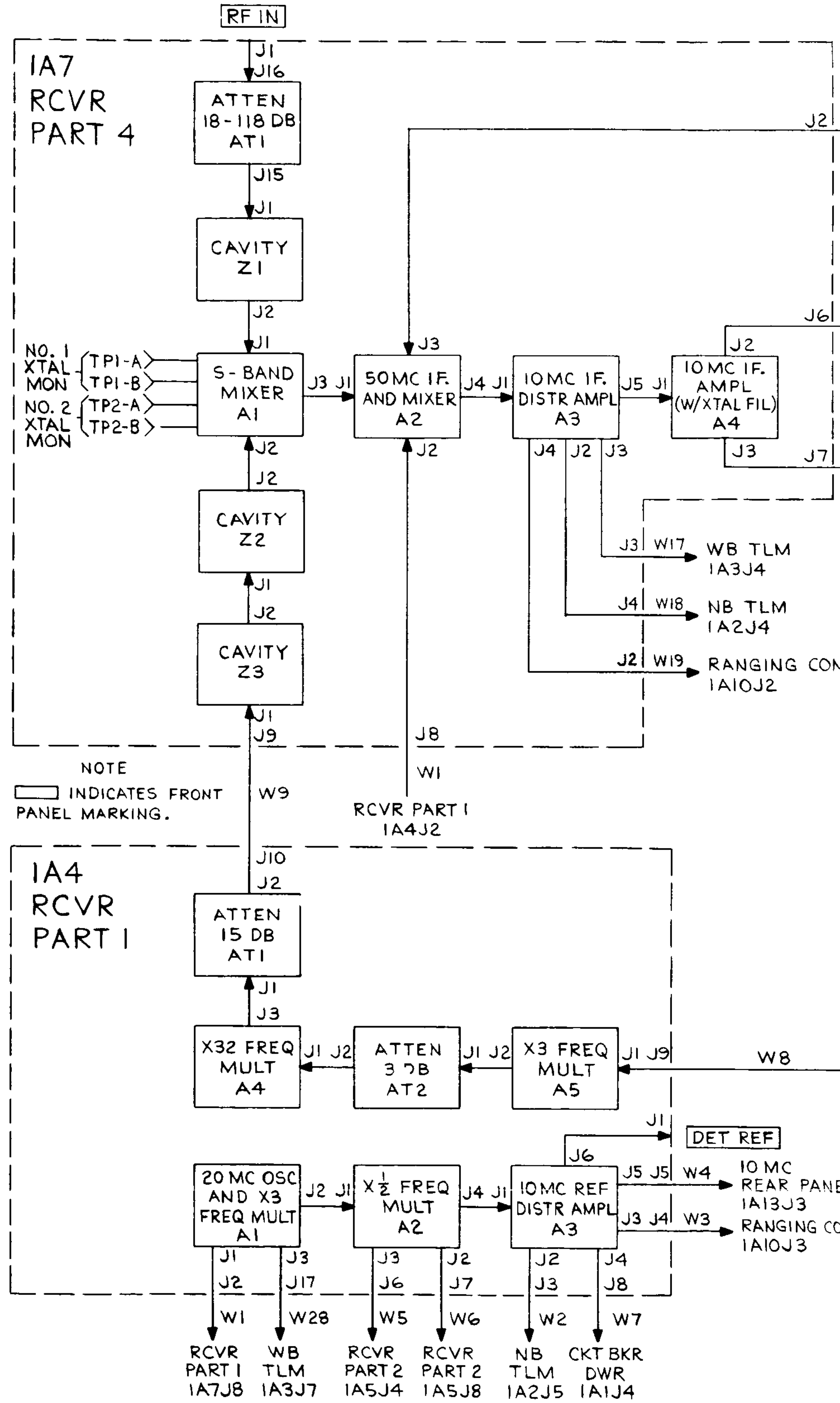


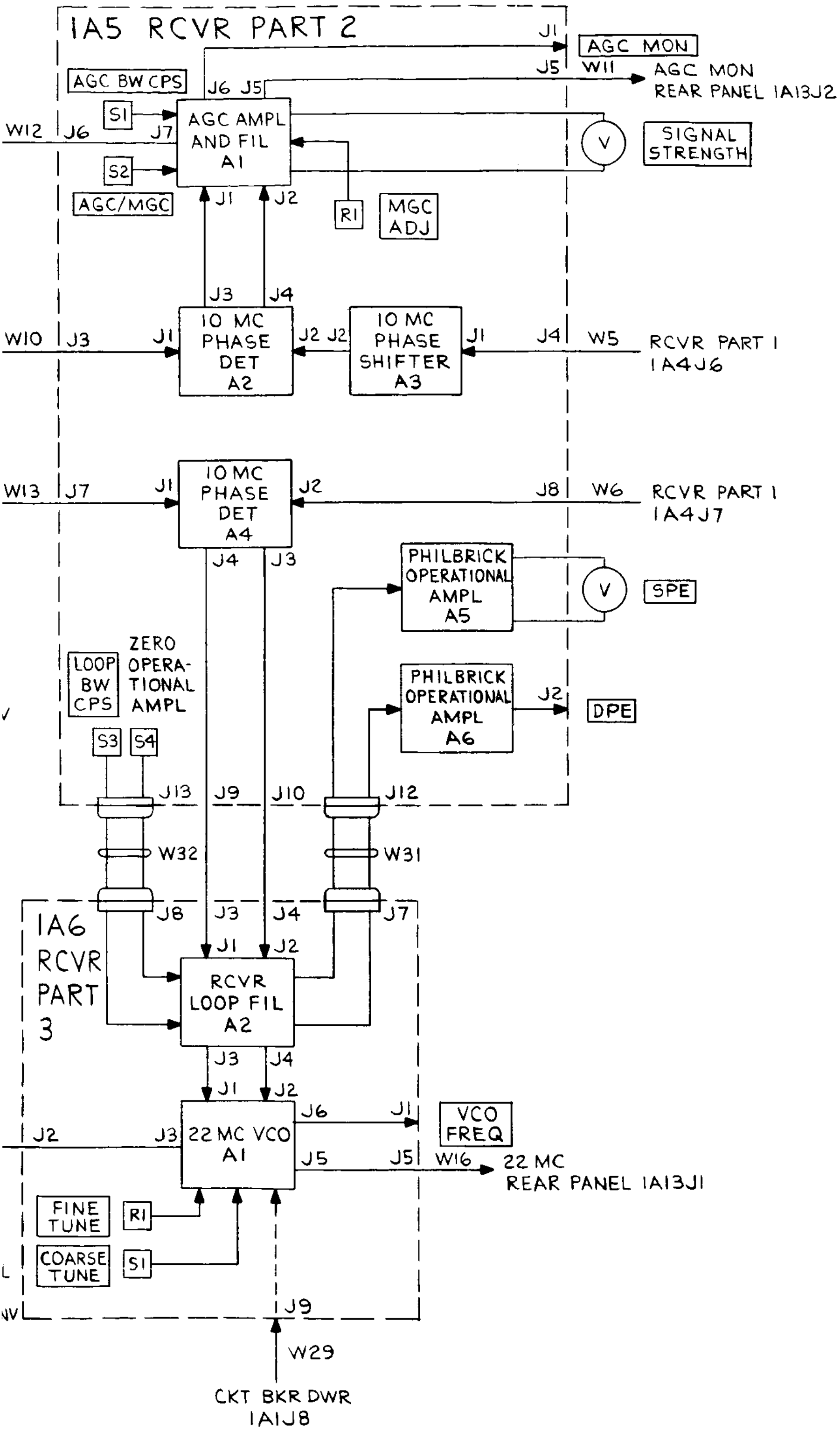
Figure 6-12. Wide Band 10 MC IF Amplifier (1A3A2), Schematic Diagram (63-23882D)



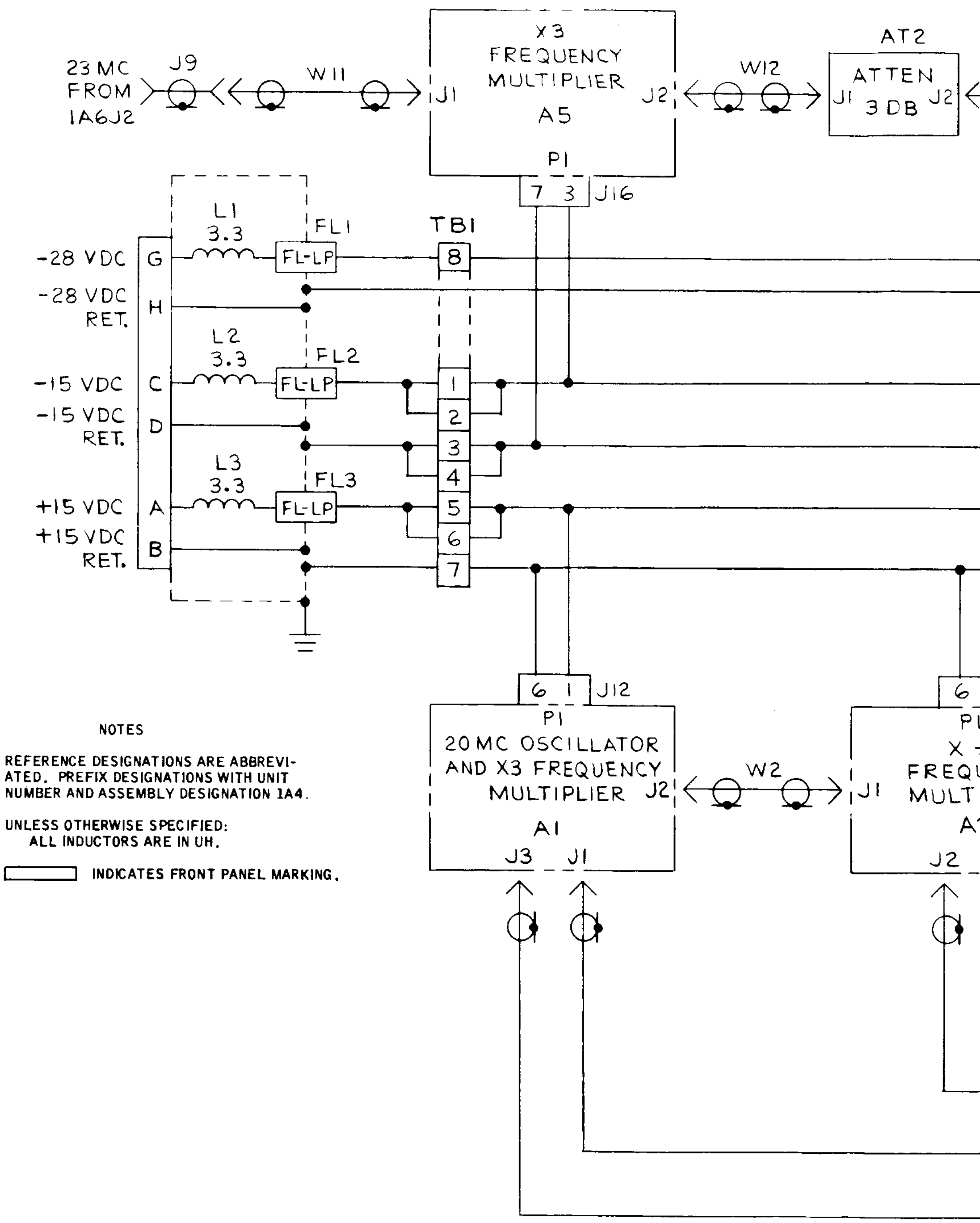
RF IN
IA7
RCVR
PART 4
ATTEN
18-118 DB
AT1
CAVITY
Z1
NO. 1 XTAL MON
TP1-A
TP1-B
NO. 2 XTAL MON
TP2-A
TP2-B
S-BAND MIXER
A1
50MC I.F. AND MIXER
A2
10MC I.F. DISTR AMPL
A3
10MC I.F. AMPL (W/XTAL FIL)
A4
CAVITY
Z2
CAVITY
Z3
WB TLM
1A3J4
NB TLM
1A2J4
RANGING CON
1A10J2
NOTE
INDICATES FRONT PANEL MARKING.
RCVR PART 1
1A4J2
IA4
RCVR
PART 1
ATTEN
15 DB
AT1
X32 FREQ MULT
A4
ATTEN
3 DB
AT2
X3 FREQ MULT
A5
W8
DET REF
20 MC OSC AND X3 FREQ MULT
A1
X½ FREQ MULT
A2
10MC REF DISTR AMPL
A3
10 MC
REAR PANE
1A13J3
RANGING CO
1A10J3
RCVR PART 1
1A7J8
WB TLM
1A3J7
RCVR PART 2
1A5J4
RCVR PART 2
1A5J8
NB TLM
1A2J5
CKT BKR DWR
1A1J4

Figure 6-1

2



4. Test Receiver, Interconnection Diagram (69-25443E)



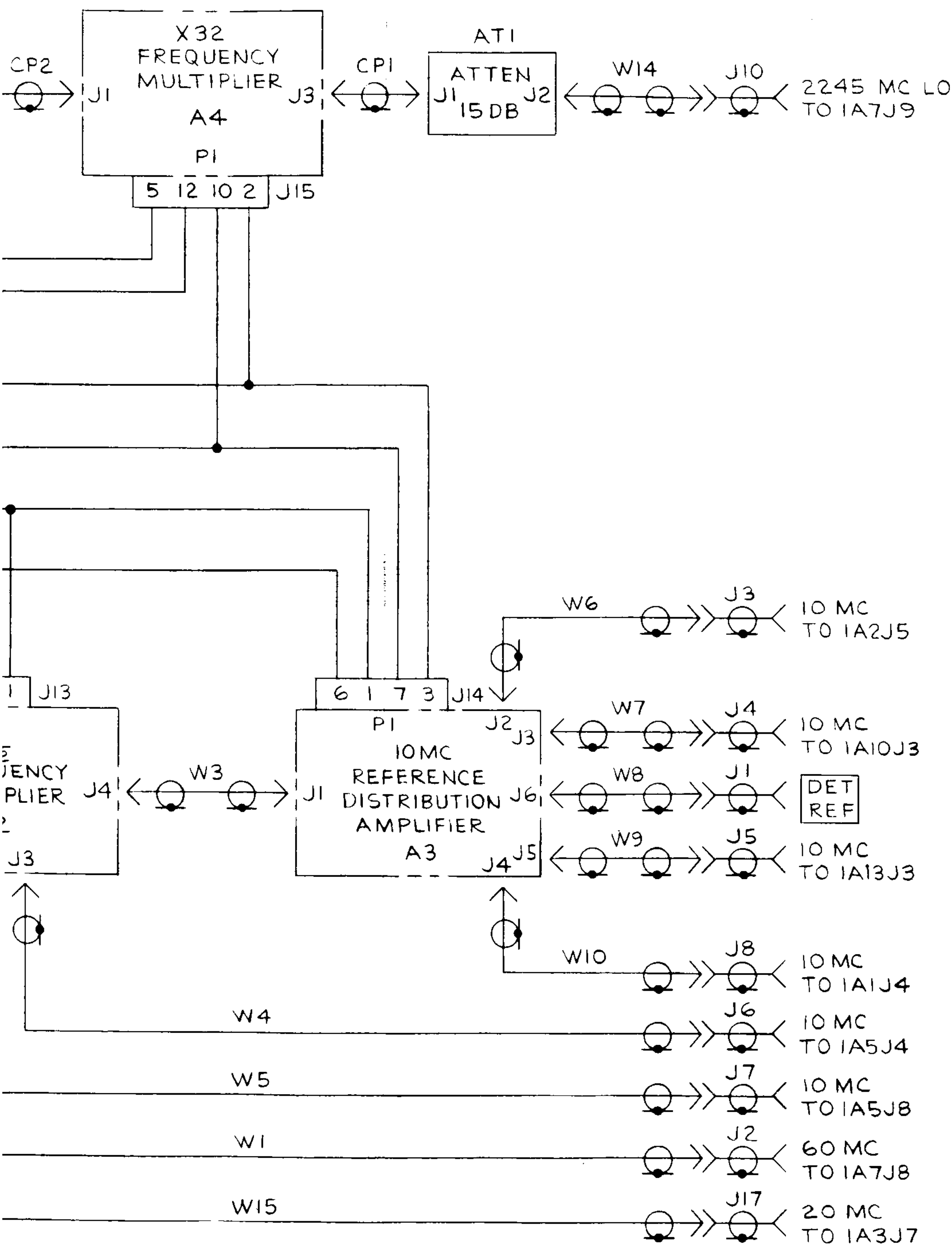
NOTES

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION 1A4.
2. UNLESS OTHERWISE SPECIFIED: ALL INDUCTORS ARE IN UH.
3. ▭ INDICATES FRONT PANEL MARKING.

Figure

2

VOLUME 1



6-15. Test Receiver, Part One (1A4), Schematic Diagram (63-25447E)

4. VALUE TO BE SELECTED IN TEST

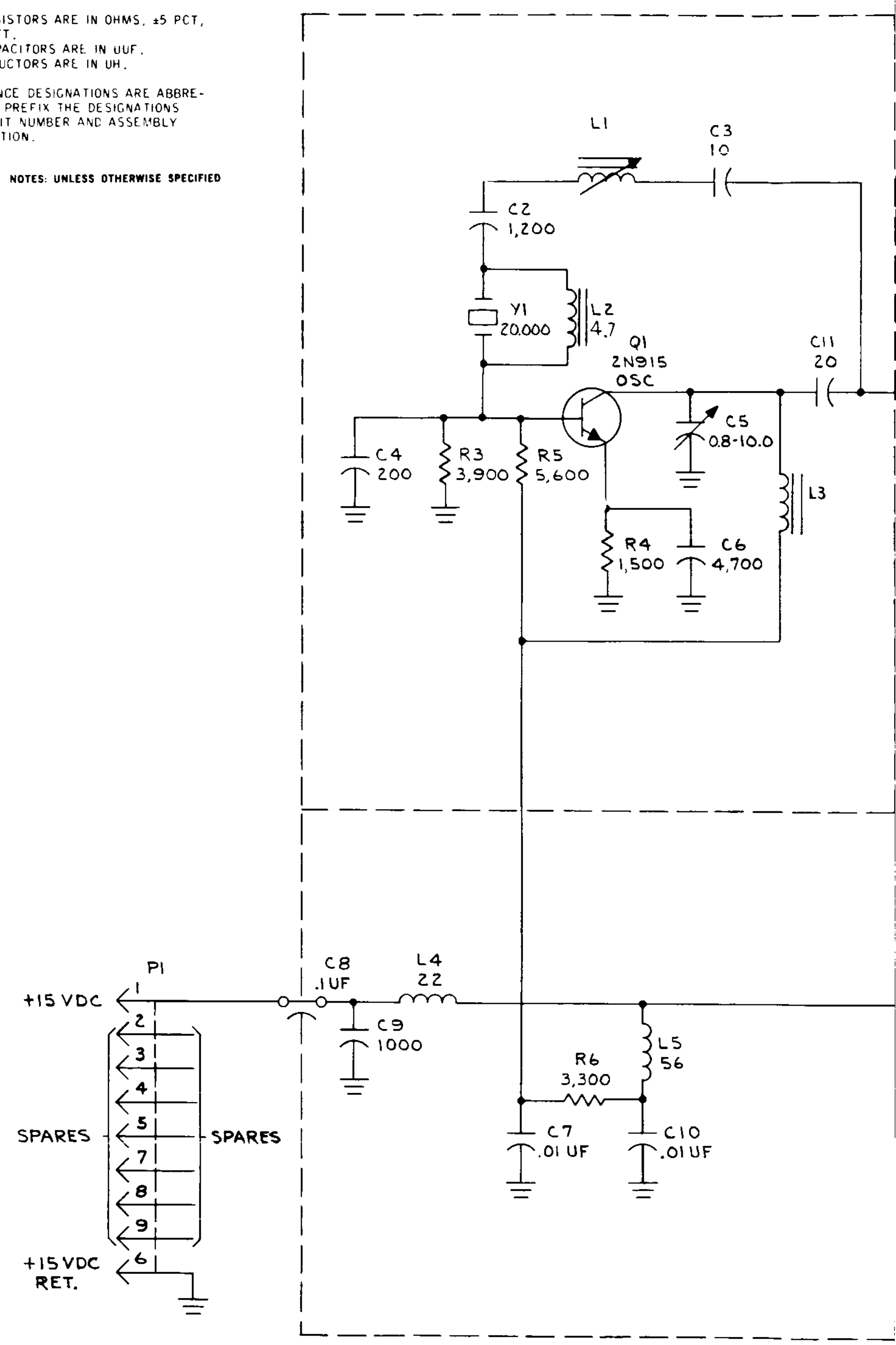
REFERENCE NO.	APPROXIMATE VALUE
C24	24
C27	100
C39	1
C41	10
C42	5.1
R27	82
R28	100
R29	18
R30	330
R31	150

3 C45 SELECTED IN TEST OR OMITTED AS REQUIRED. APPROXIMATE VALUE 5.1

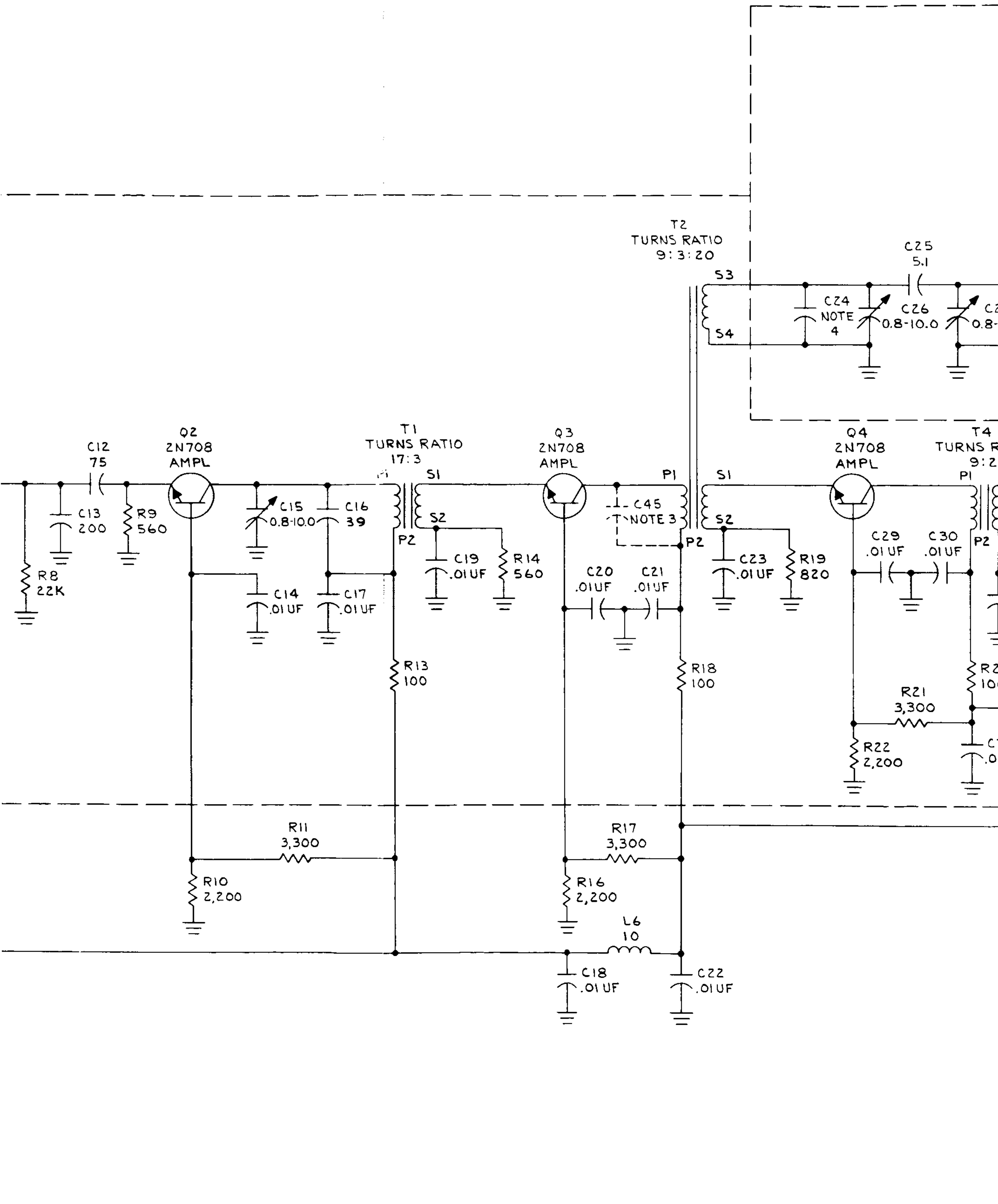
2 ALL RESISTORS ARE IN OHMS, ±5 PCT, 1/4 WATT.
ALL CAPACITORS ARE IN UUF.
ALL INDUCTORS ARE IN UH.

1 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

NOTES: UNLESS OTHERWISE SPECIFIED

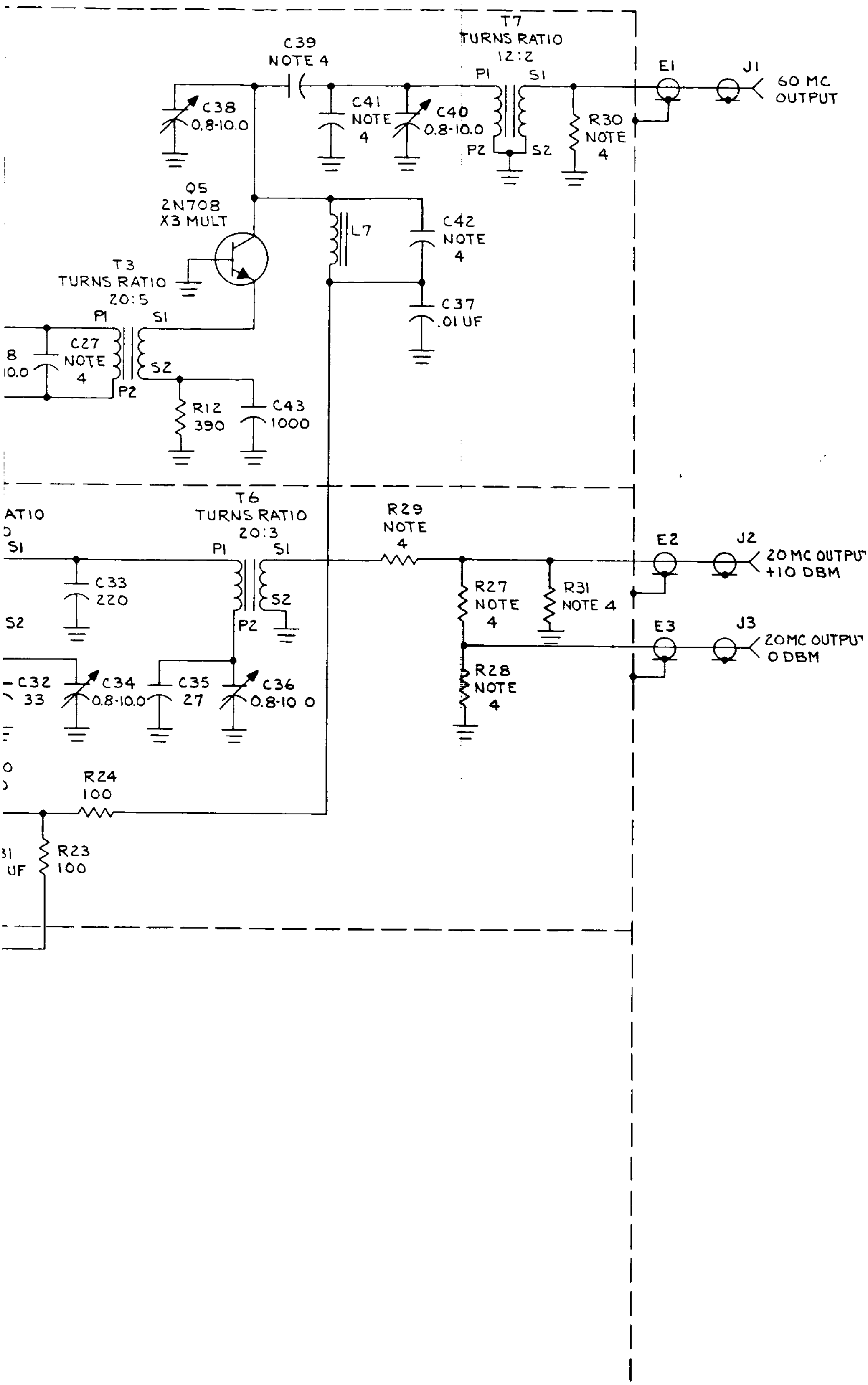


I


T2
TURNS RATIO
9:3:20
S3
S4
C25
5.1
C24
NOTE
4
C26
0.8-10.0
Q2
2N708
AMPL
C12
75
C13
200
R9
560
R8
22K
C15
0.8-10.0
C16
39
C14
.01 UF
C17
.01 UF
T1
TURNS RATIO
17:3
S1
S2
P2
C19
.01 UF
R14
560
Q3
2N708
AMPL
P1
C45
NOTE 3
P2
C20
.01 UF
C21
.01 UF
R13
100
R18
100
S1
S2
C23
.01 UF
R19
820
Q4
2N708
AMPL
T4
C29
.01 UF
C30
.01 UF
R21
3,300
R22
2,200
R11
3,300
R10
2,200
R17
3,300
R16
2,200
L6
10
C18
.01 UF
C22
.01 UF

Figure

2



6-16. 20 MC Oscillator and X3 Multiplier (1A4A1), Schematic Diagram (63-21453C)

4. VALUE TO BE SELECTED IN TEST.

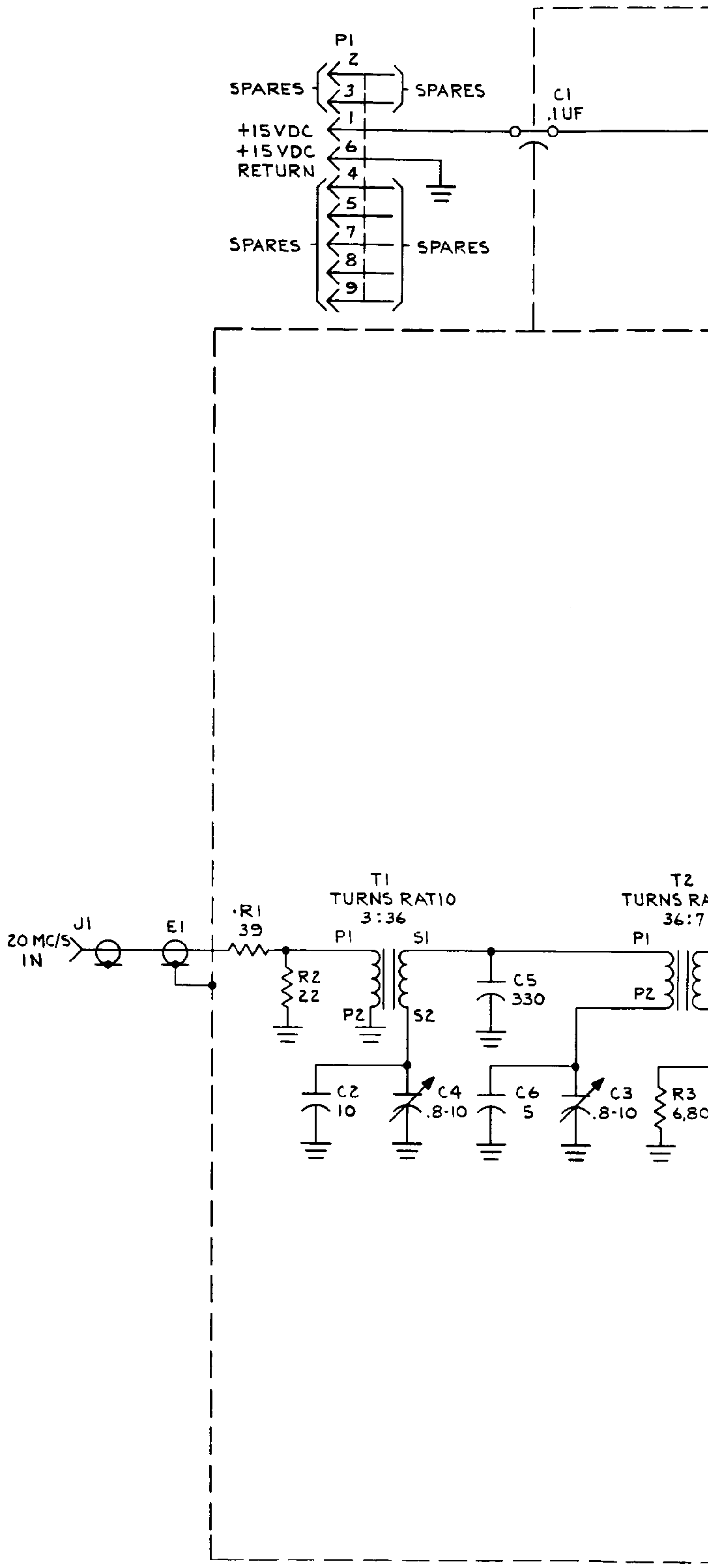
REFERENCE NO.	APPROXIMATE VALUE
R18	100
R23	100
R30	100
R32	27
R33	27
R34	27

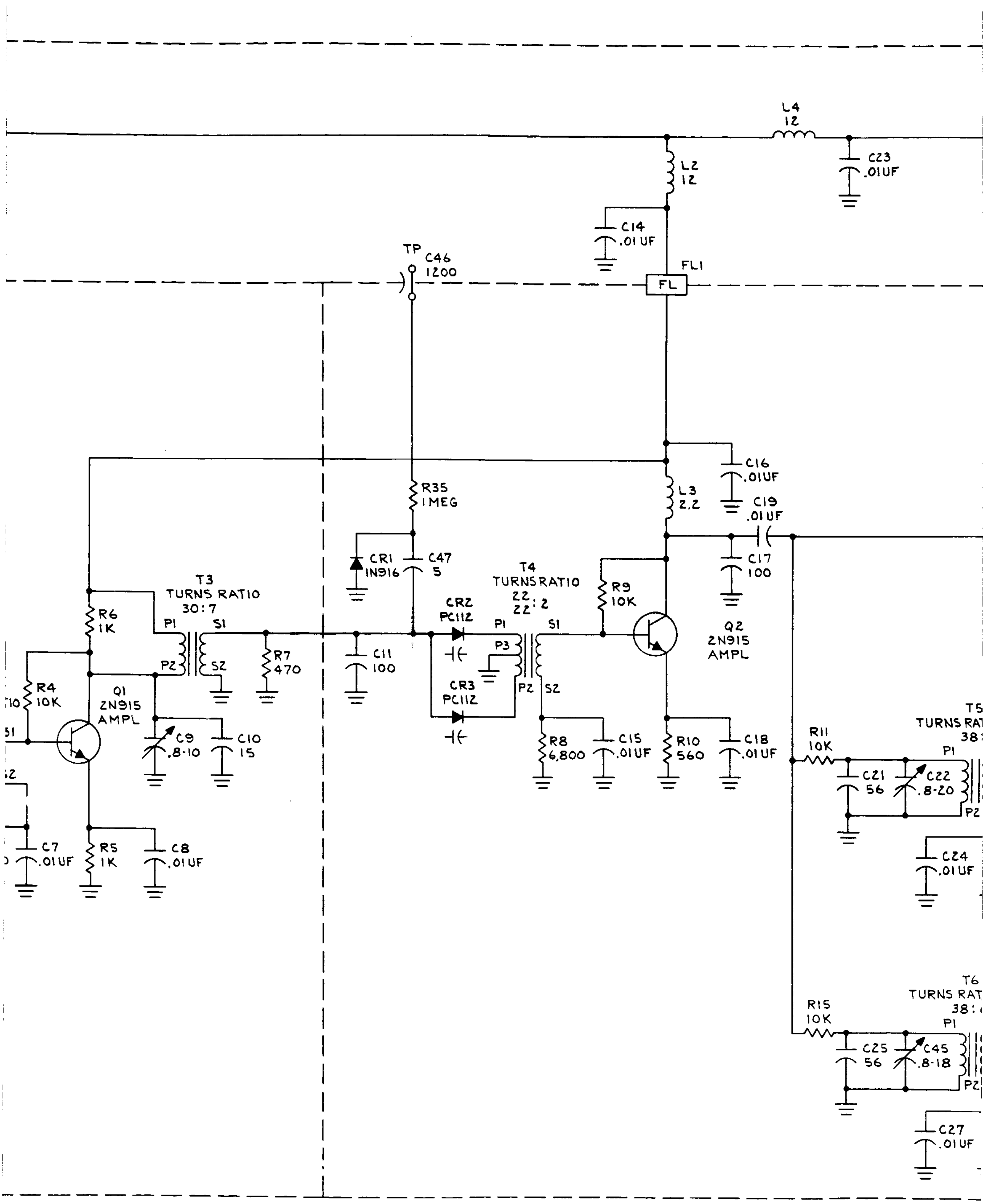
3. ALL RESISTORS ARE IN OHMS, (5 PCT, 1/4 WATT). ALL CAPACITORS ARE IN UUF. ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330508 (MOTOROLA NO. 01-21456).

NOTES: UNLESS OTHERWISE SPECIFIED




L4
12
L2
12
C23
.01UF
C14
.01 UF
TP
C46
1200
FL1
FL
C16
.01UF
R35
1MEG
L3
2.2
C19
.01 UF
CR1
1N916
C47
5
C17
100
T3
TURNS RATIO
30:7
T4
TURNS RATIO
22:2
22
CR2
PC112
R9
10K
Q2
2N915
AMPL
R6
1K
P1
S1
P2
S2
P3
R7
470
C11
100
CR3
PC112
R4
10K
Q1
2N915
AMPL
C9
.8-10
C10
15
R8
6,800
C15
.01UF
R10
560
C18
.01UF
R11
10K
C21
56
C22
.8-20
C7
.01UF
R5
1K
C8
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C24
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R15
10K
C25
56
C45
.8-18
C27
.01UF

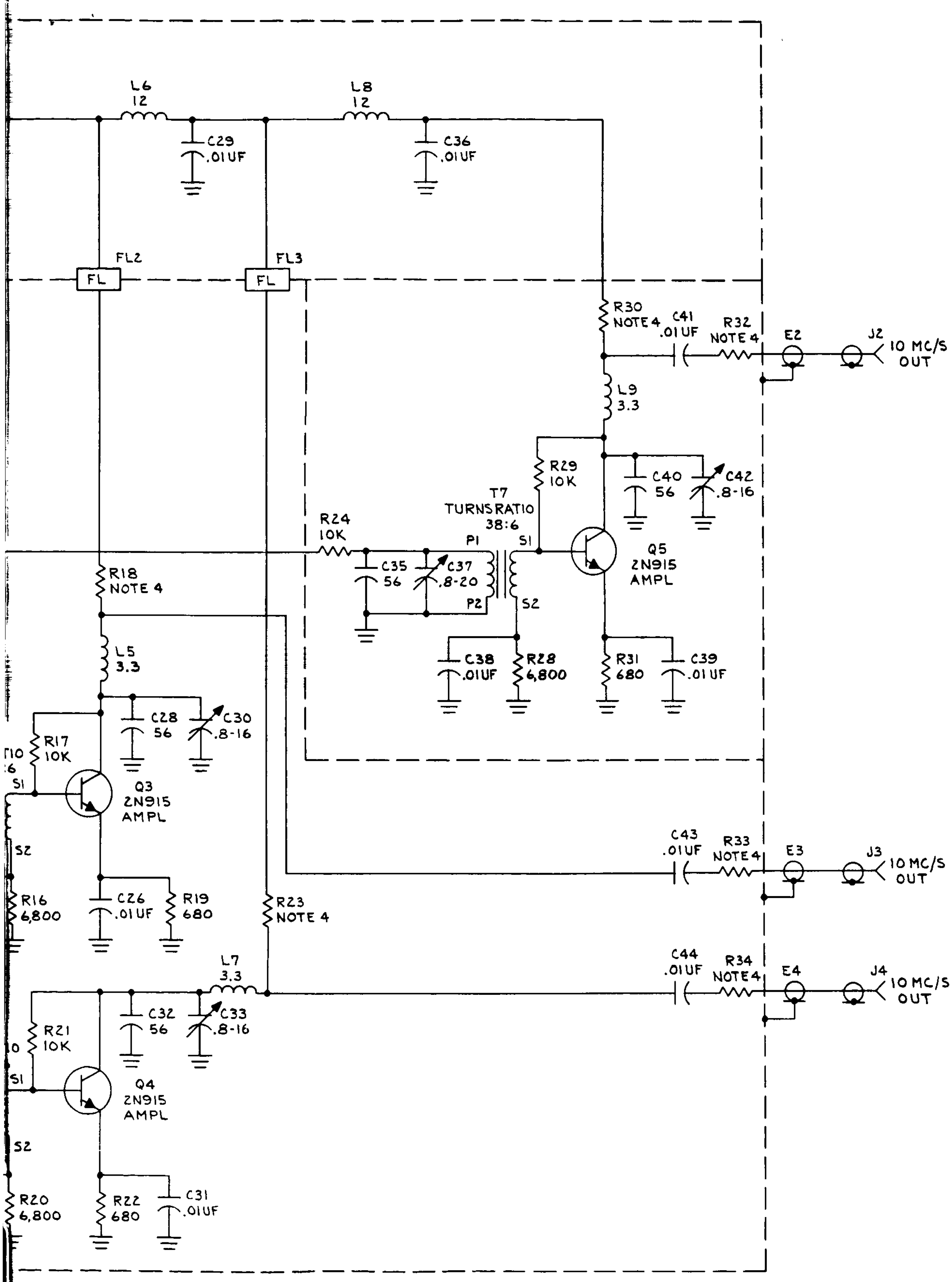


Figure 6-17. X½ Frequency Multiplier (1A4A2), Schematic Diagram (63-21454C)

4. FOR ASSEMBLY SEE DRAWING D9330507 (MOTOROLA PART NO. 01-23778D).

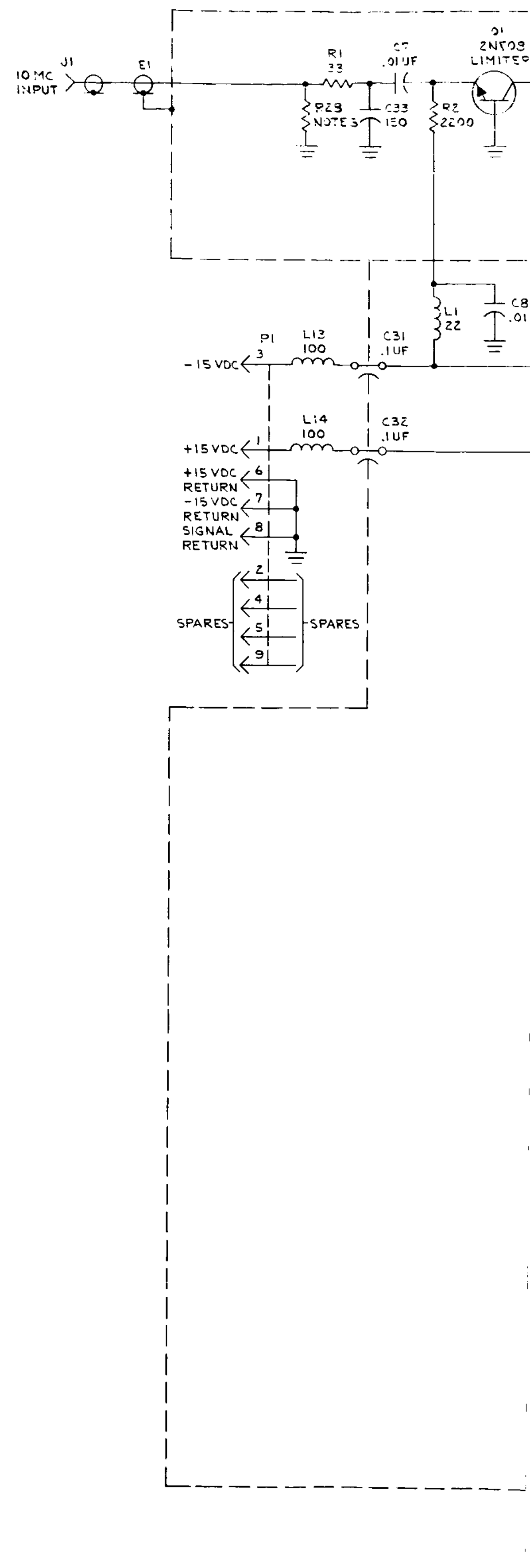
3. SELECTED IN TEST APPROXIMATE VALUE 120.

2. ALL RESISTORS ARE IN OHMS, ± 5 PCT, 1/4 WATT.

   ALL CAPACITORS ARE IN UUF.

   ALL INDUCTORS ARE IN UH.

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.



2

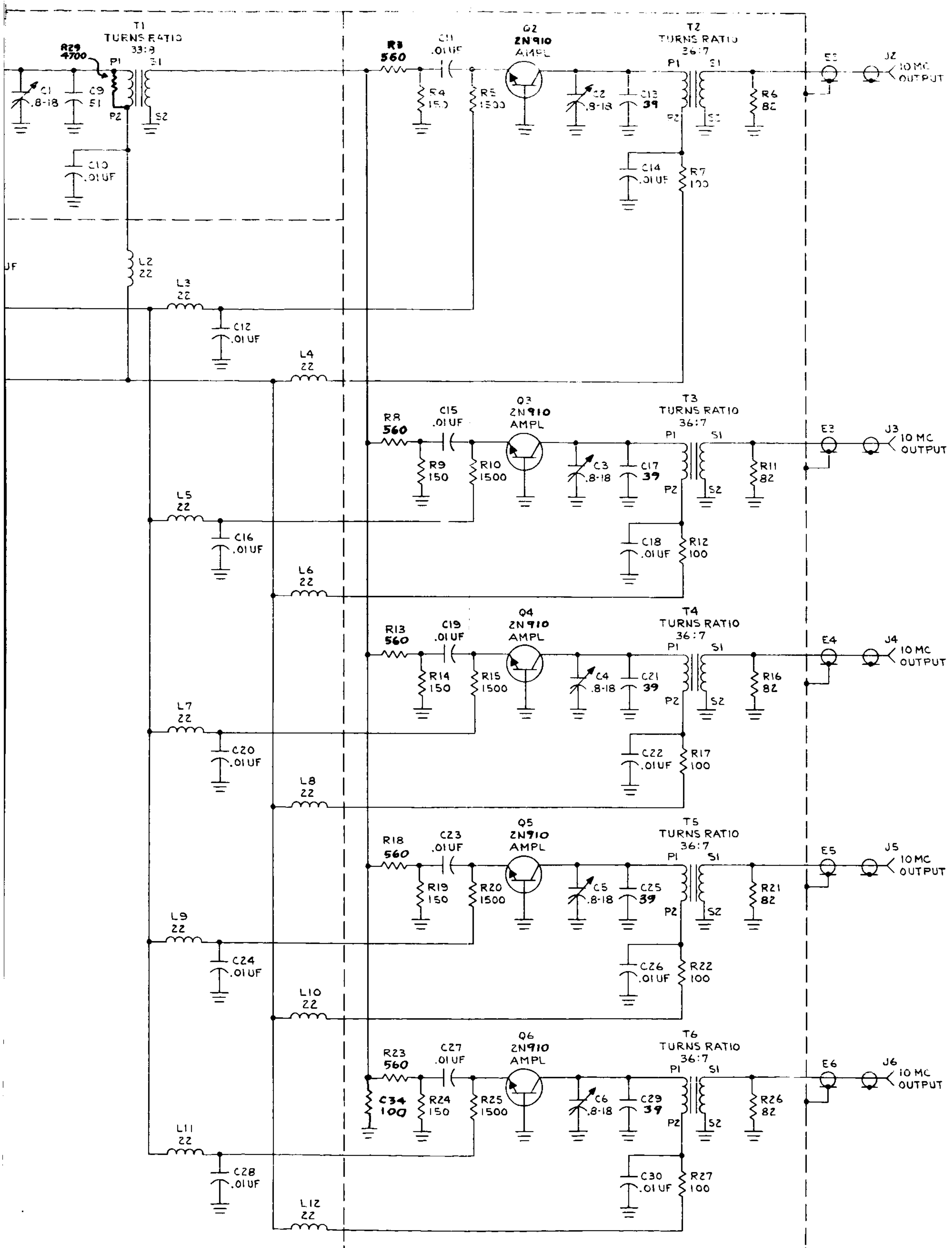


Figure 6-18. 10 MC Isolation and Distribution Amplifier (1A4A3), Schematic Diagram (63-23868D)

5. THE TWO MOUNTING SCREWS FOR L15 ARE SELECTED AT TEST, SEE DRAWING J9331139, (MOTOROLA 01-236130, NOTE 29).

4. VALUE TO BE SELECTED IN TEST

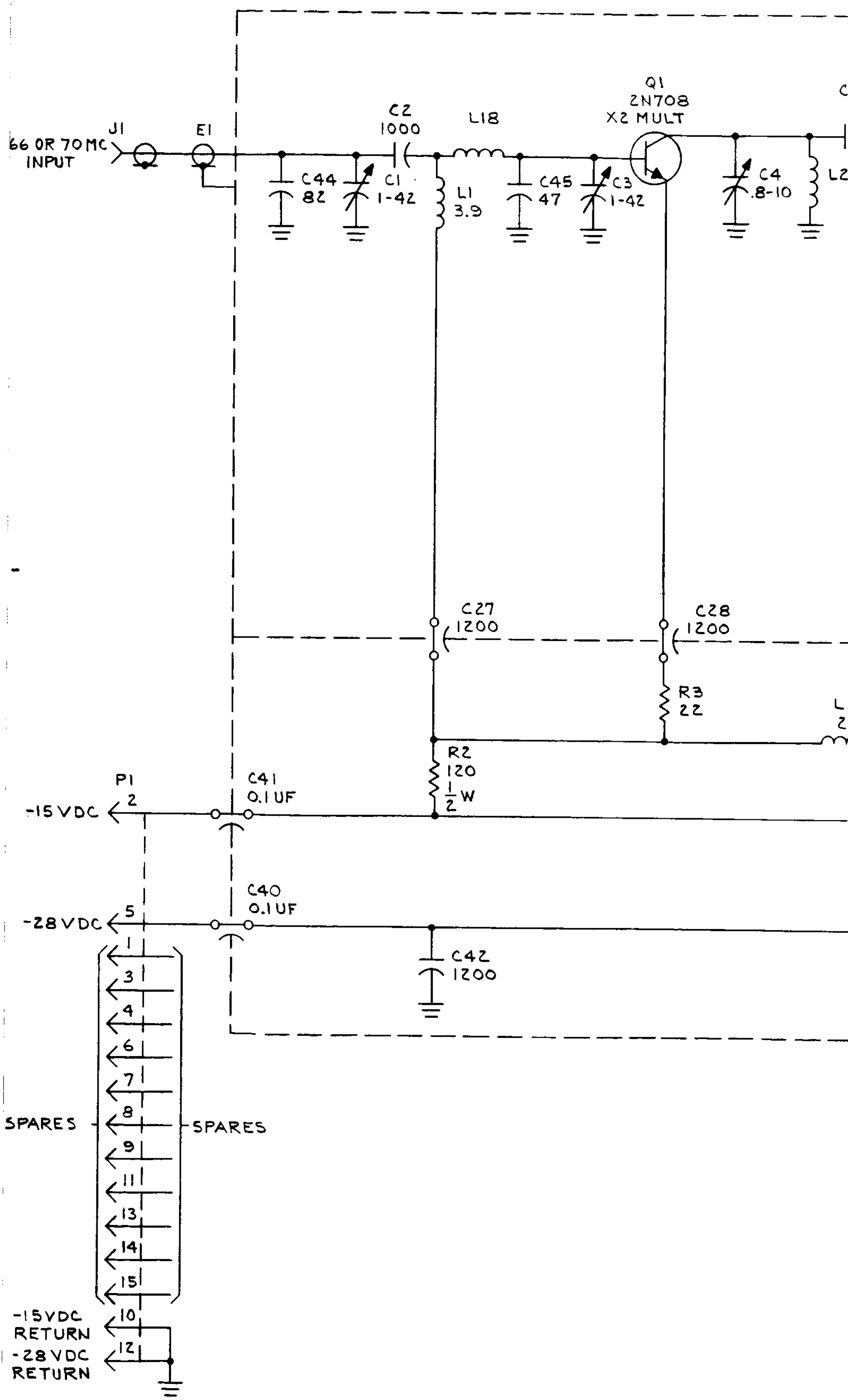
REFERENCE NO.	APPROXIMATE VALUE
C14	47
C22	5

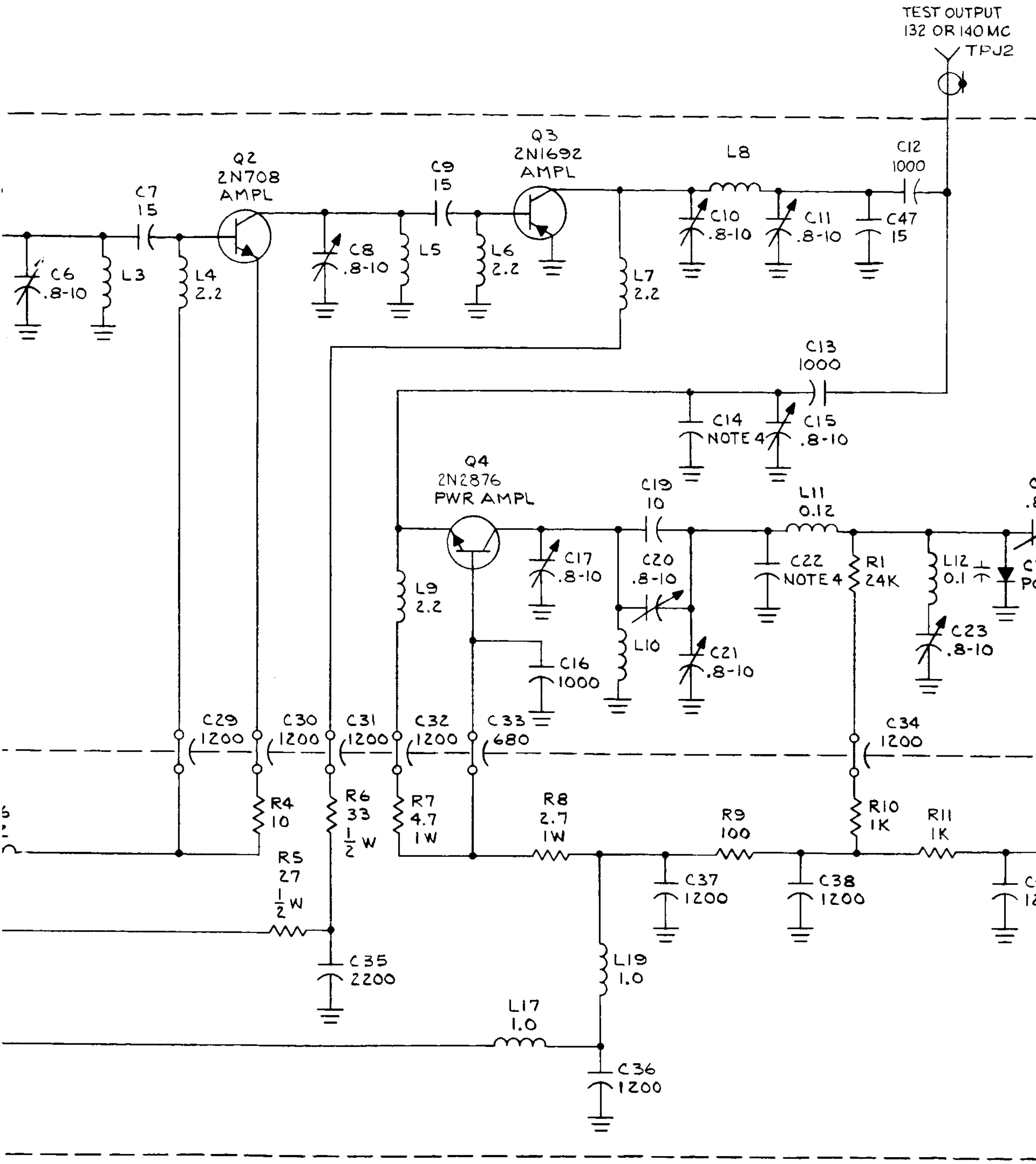
3. ALL RESISTORS ARE IN OHMS, 5 PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UUF.
   ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED, PREFIX THE DES IGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING J9330517, (MOTOROLA NO. 01-23786D)

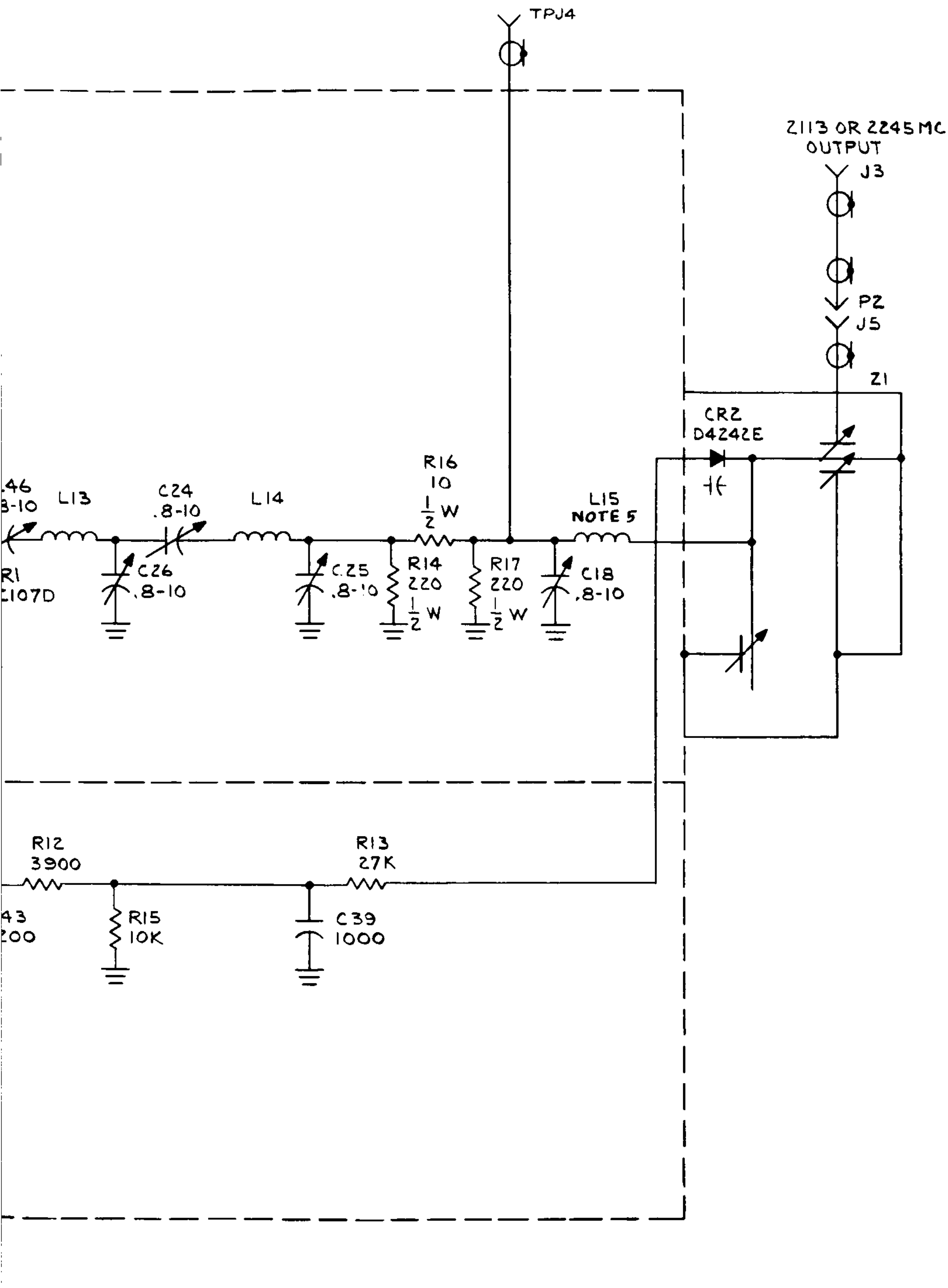
NOTES: UNLESS OTHERWISE SPECIFIED


66 OR 70 MC
INPUT
J1
E1
C44
82
C2
1000
C1
1-42
L18
L1
3.9
C45
47
C3
1-42
Q1
2N708
X2 MULT
C4
.8-10
C27
1200
C28
1200
R3
22
R2
120
$\frac{1}{2}$ W
P1
-15 VDC
C41
0.1 UF
-28 VDC
C40
0.1 UF
C42
1200
SPARES
SPARES
-15 VDC
RETURN
-28 VDC
RETURN


TEST OUTPUT
132 OR 140 MC
TPJ2
Q2
2N708
AMPL
Q3
2N1692
AMPL
Q4
2N2876
PWR AMPL
C6 .8-10
L3
C7 15
L4 2.2
C8 .8-10
L5
C9 15
L6 2.2
L7 2.2
L8
C10 .8-10
C11 .8-10
C12 1000
C47 15
C13 1000
C14 NOTE 4
C15 .8-10
C19 10
L11 0.12
C17 .8-10
C20 .8-10
C22 NOTE 4
R1 24K
L12 0.1
C23 .8-10
L9 2.2
L10
C21 .8-10
C16 1000
C29 1200
C30 1200
C31 1200
C32 1200
C33 680
C34 1200
R4 10
R6 33 1/2 W
R7 4.7 1W
R8 2.7 1W
R9 100
R10 1K
R11 1K
R5 27 1/2 W
C37 1200
C38 1200
C35 2200
L19 1.0
L17 1.0
C36 1200

Figure

3



6-19. X32 Frequency Multiplier (1A4A4, 1A9A3), Schematic Diagram (63-23875D)

4. VALUE TO BE SELECTED IN TEST.

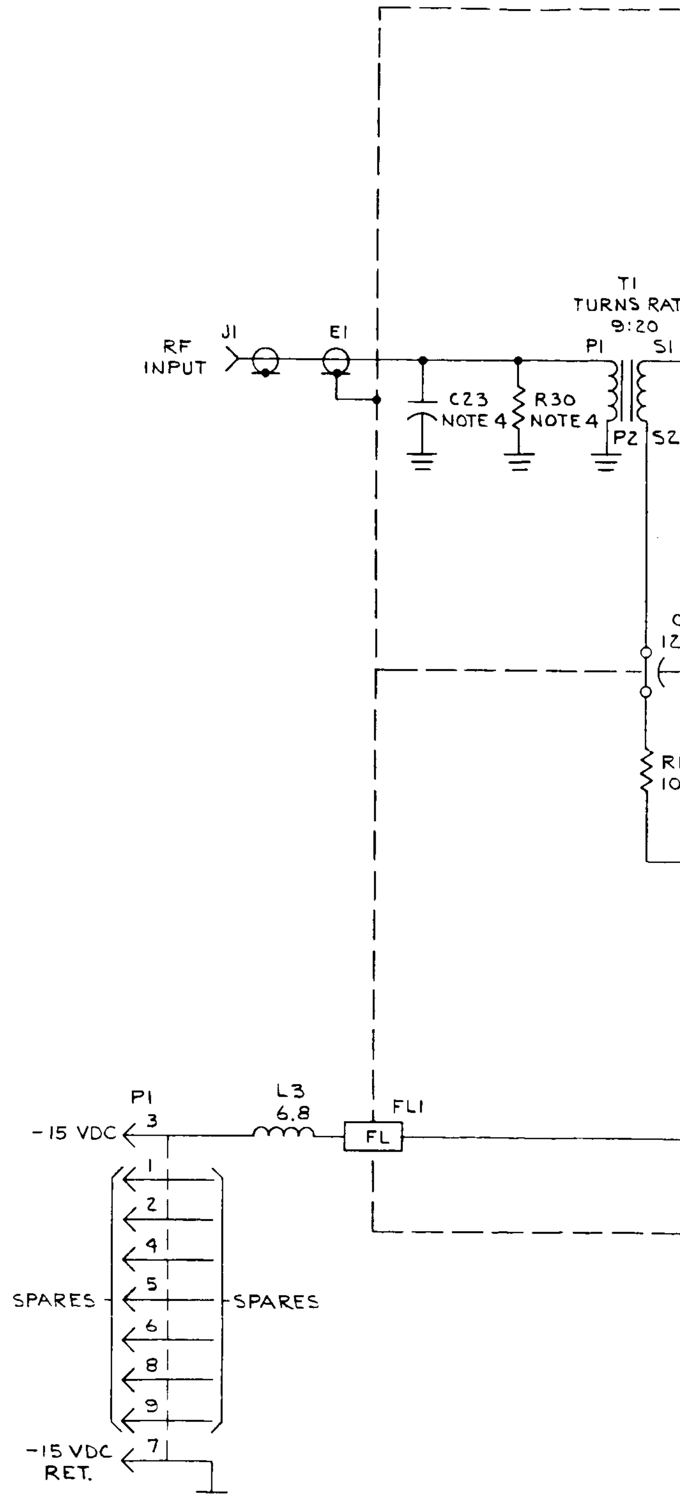
REFERENCE NO.	APPROXIMATE VALUE
C11	22
C21	22
C22	22
C23	120
R29	220
R30	120

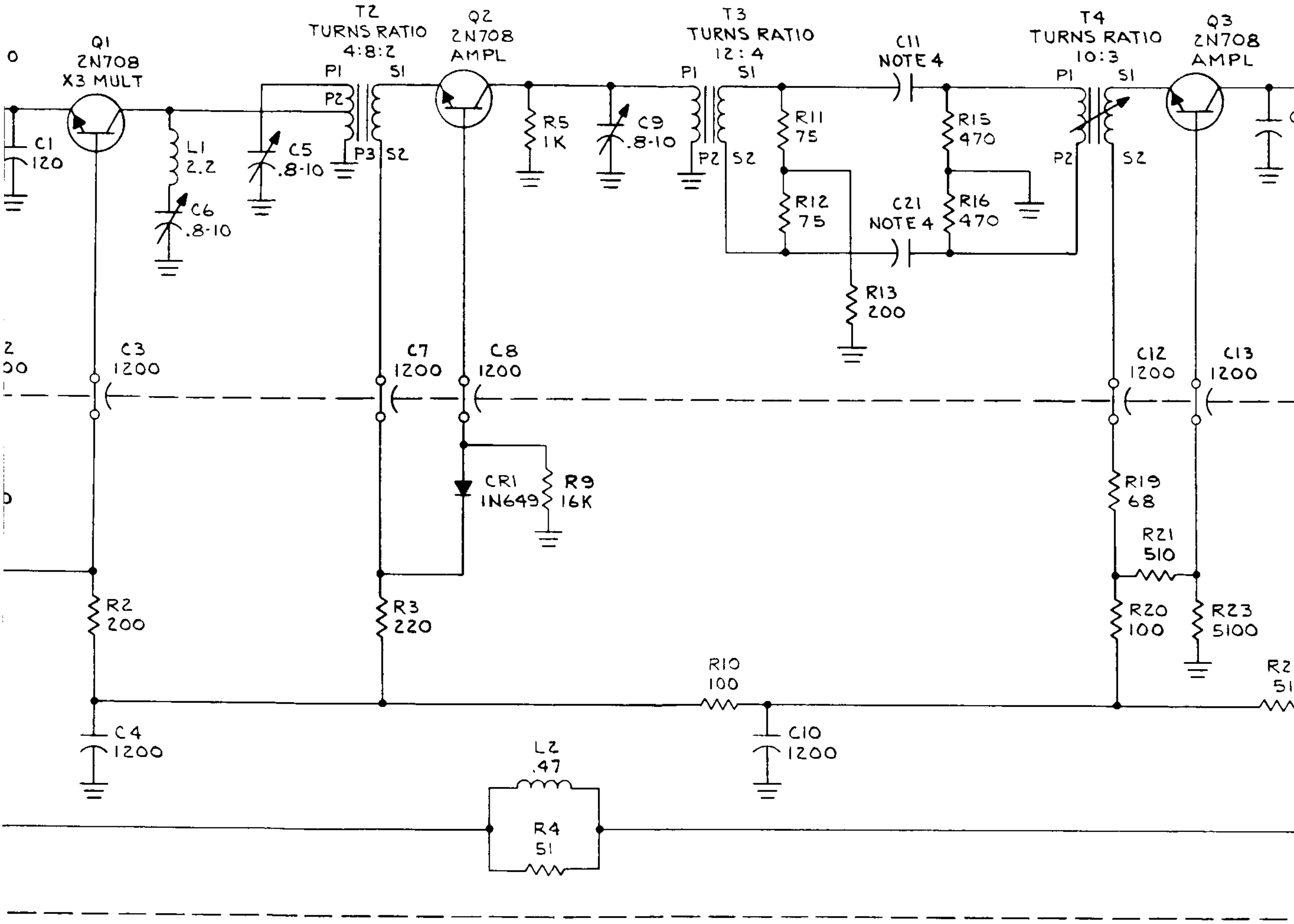
3. ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UUF.
   ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330516, D9331065 (MOTOROLA NO. 01-23772D, 01-24102D).

NOTES: UNLESS OTHERWISE SPECIFIED

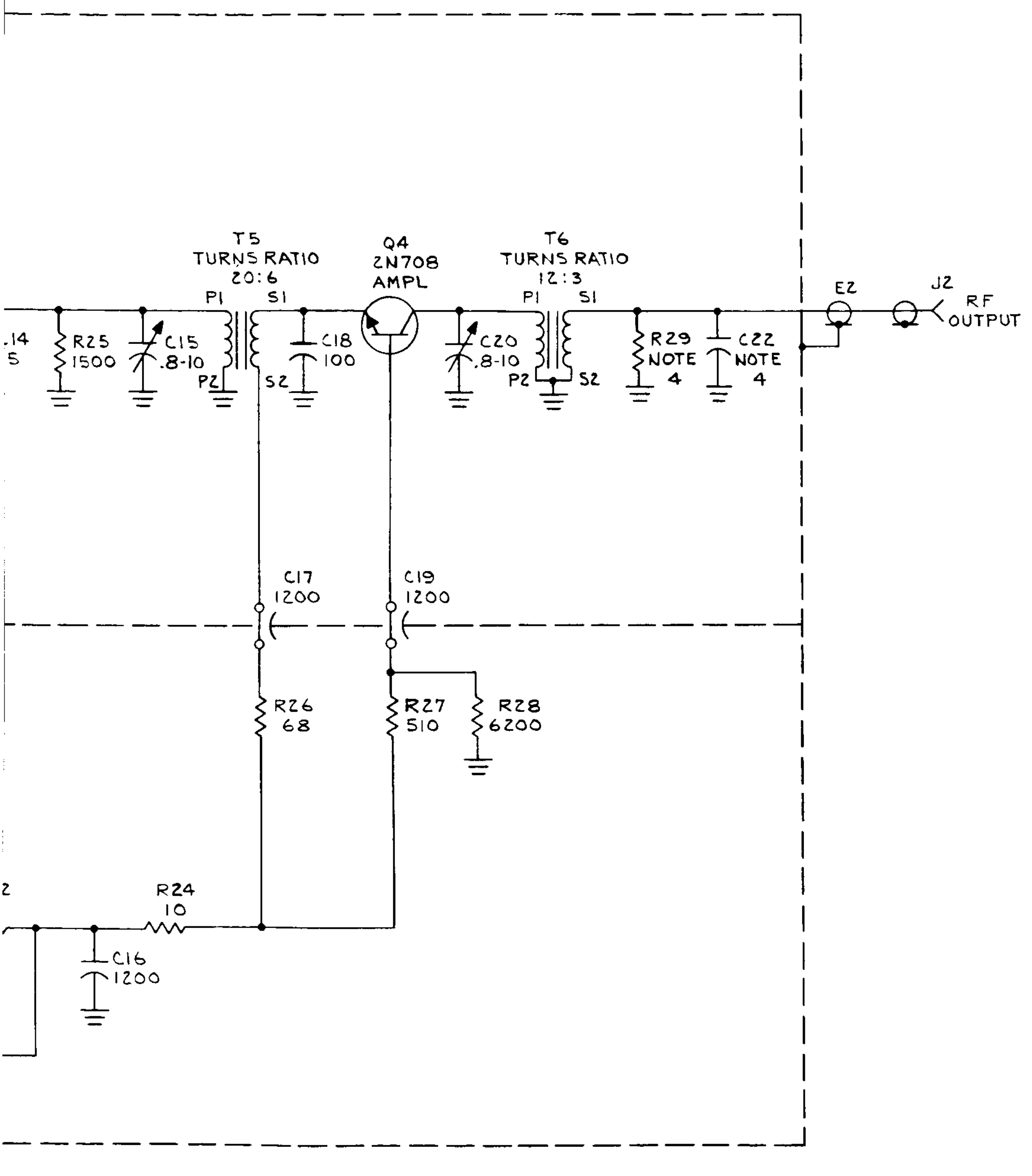




Q1
2N708
X3 MULT
C1
120
L1
2.2
C6
.8-10
C5
.8-10
T2
TURNS RATIO
4:8:2
P1
P2
P3
S1
S2
Q2
2N708
AMPL
R5
1K
C9
.8-10
T3
TURNS RATIO
12:4
P1
P2
S1
S2
R11
75
R12
75
C11
NOTE 4
C21
NOTE 4
R13
200
R15
470
R16
470
T4
TURNS RATIO
10:3
P1
P2
S1
S2
Q3
2N708
AMPL
C3
1200
C7
1200
C8
1200
CR1
1N649
R9
16K
C12
1200
C13
1200
R19
68
R21
510
R20
100
R23
5100
R2
200
R3
220
R10
100
C4
1200
C10
1200
L2
.47
R4
51

Figure

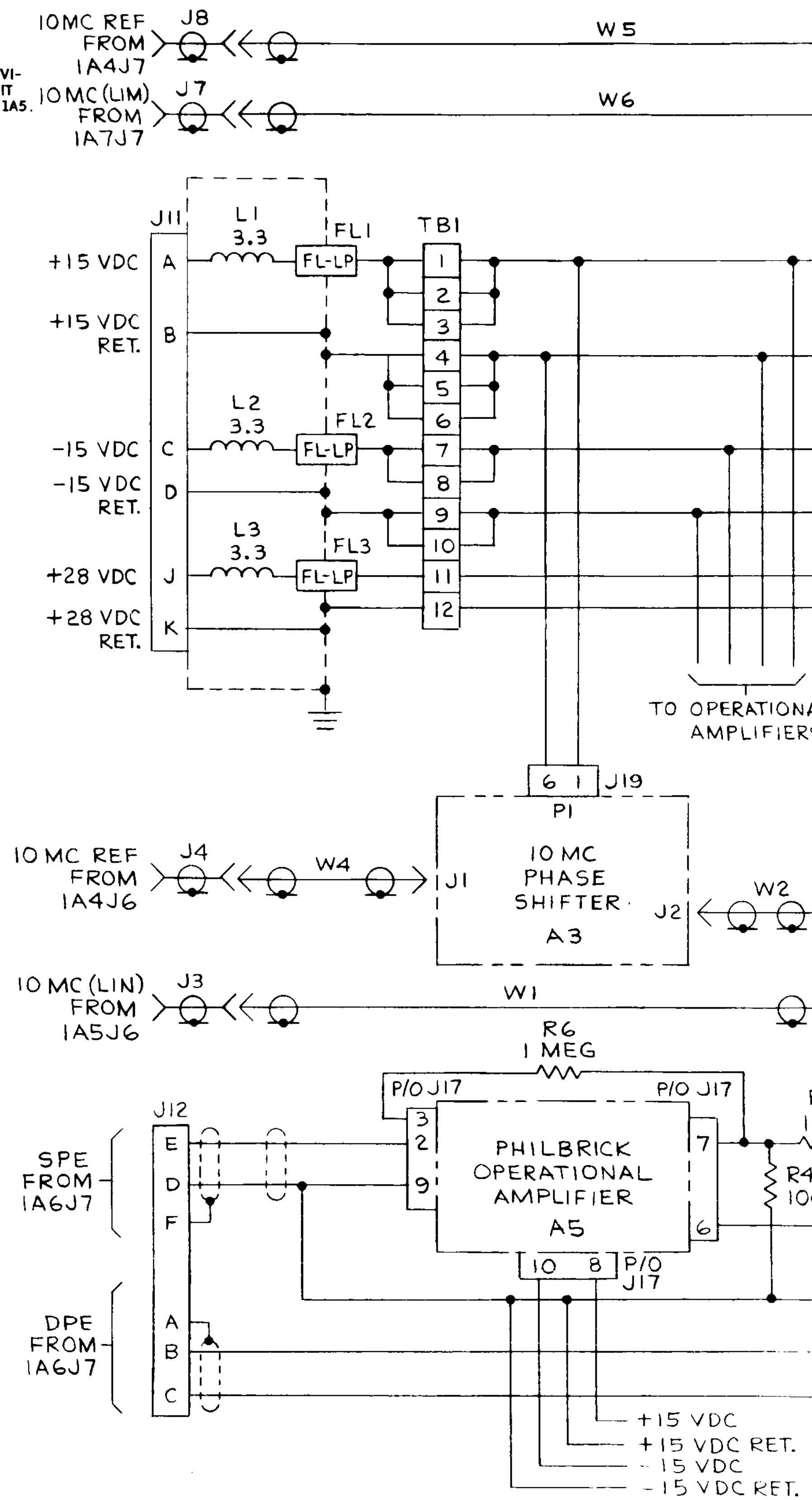
2



6-20. X3 Frequency Multiplier (1A4A5), Schematic Diagram (63-23625D)

NOTES

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION 1A5.
2. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS, ± 1 PCT, 1/4 WATT.
   B. ALL INDUCTORS ARE IN UH.
3. [ ] INDICATES FRONT PANEL MARKING.
4. PUSH S4 TO ZERO OPERATIONAL AMPLIFIERS.



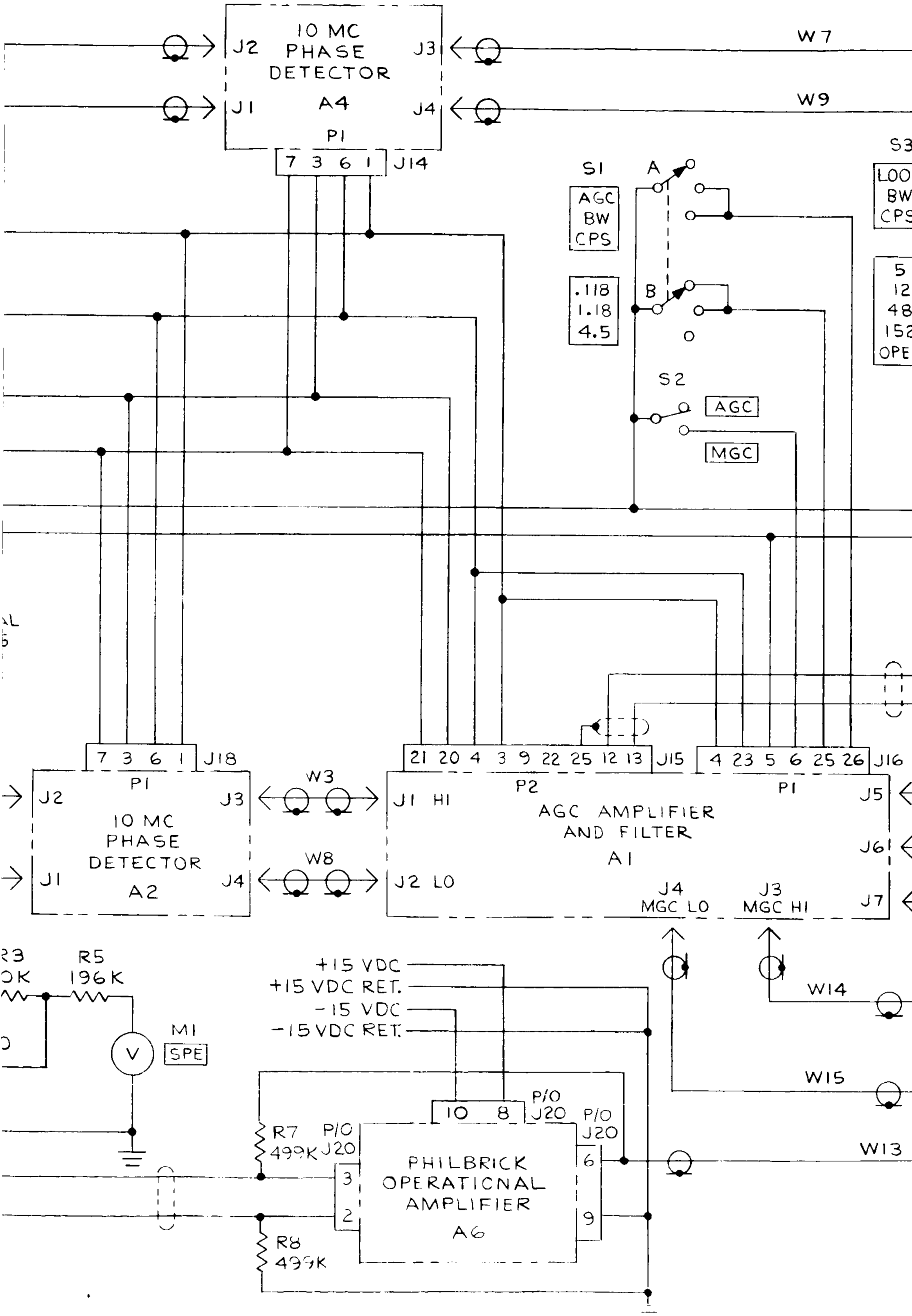
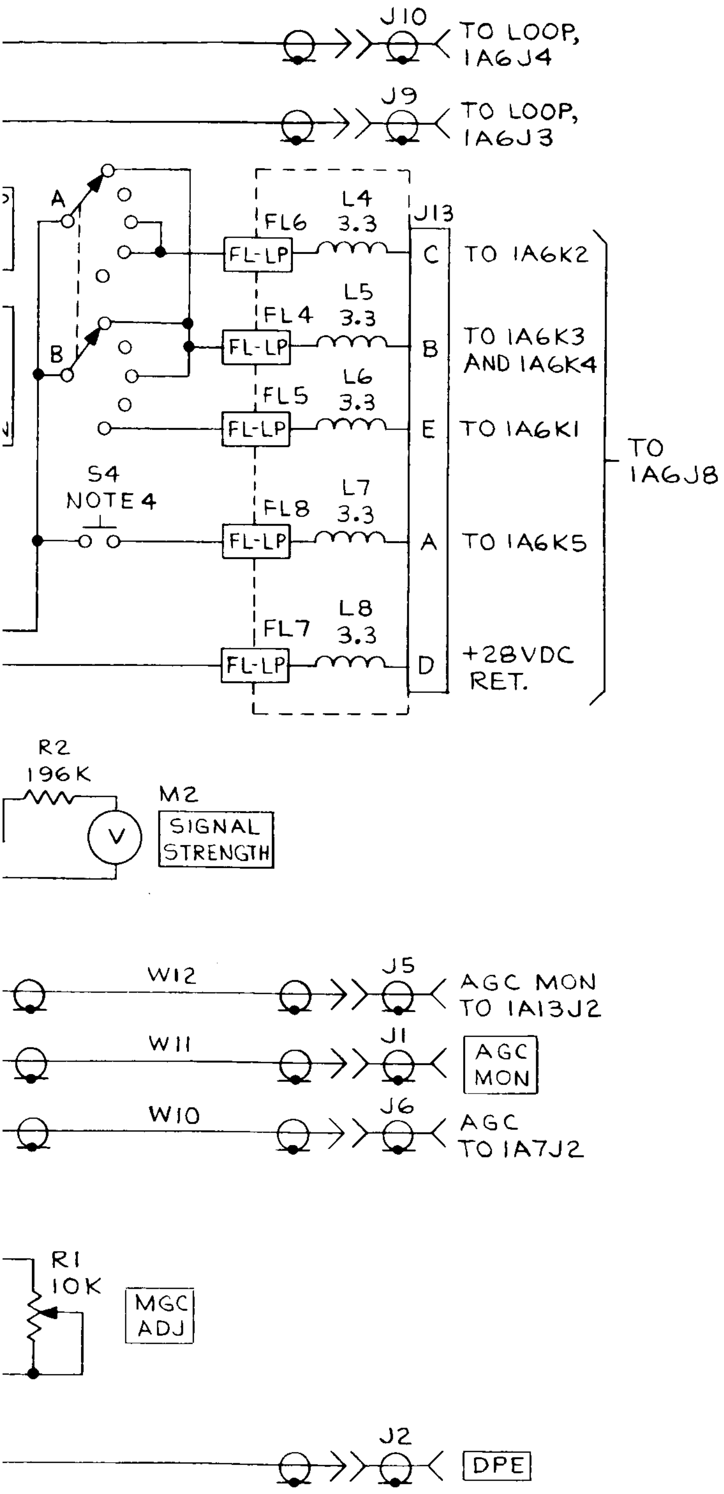


Figure 6-21. Test Receiver, I

2



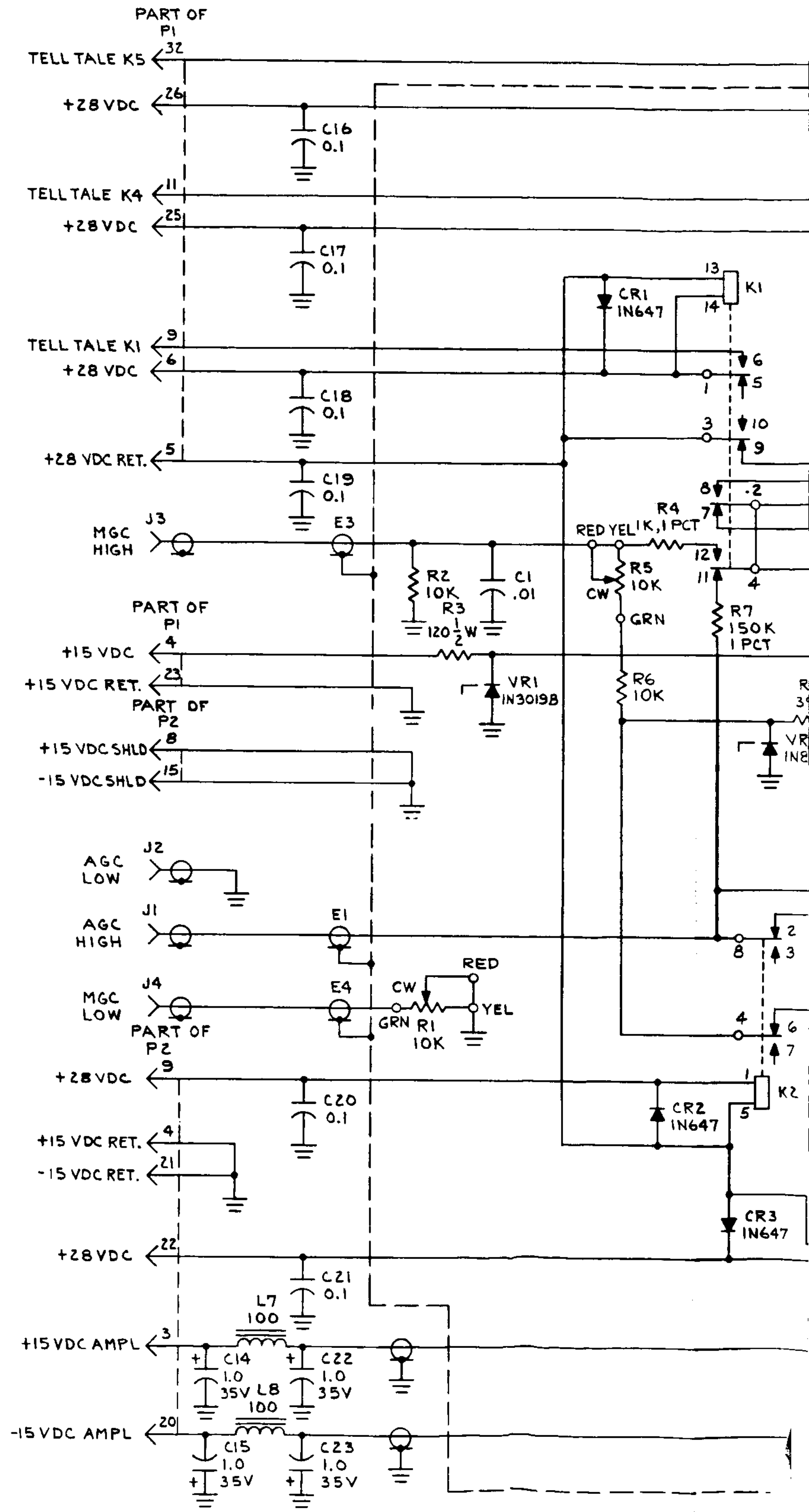
'art Two (1A5), Schematic Diagram (63-25448E)

3. ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4 WATT.
ALL CAPACITORS ARE IN UF.
ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING C9331100 (MOTOROLA NO. 01-23610D).

NOTES: UNLESS OTHERWISE SPECIFIED



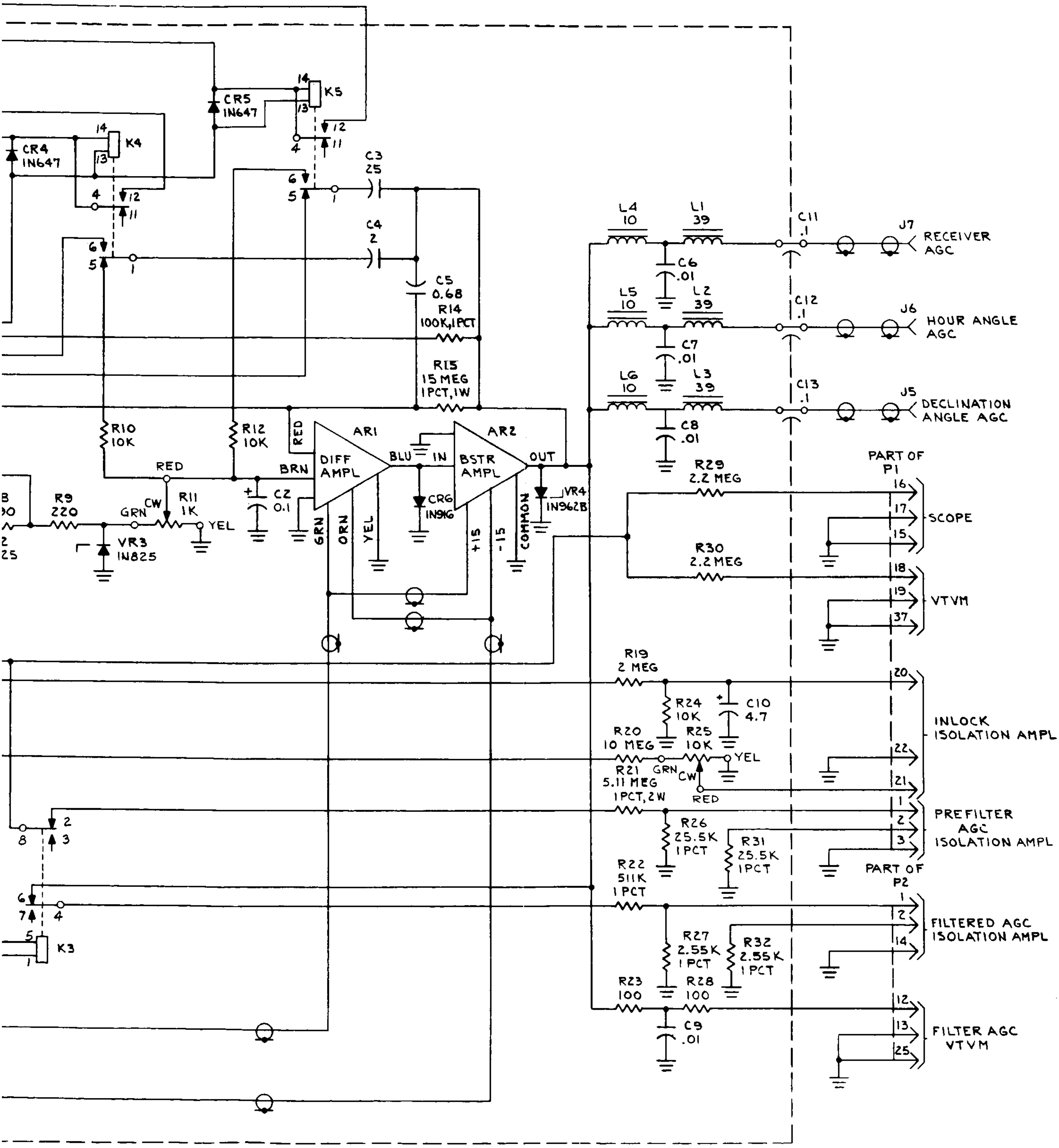


Figure 6-22. AGC Amplifier and Filter (1A5A1), Schematic Diagram (63-25023E)

5 VALUE TO BE SELECTED IN TEST

REFERENCE NO	APPROXIMATE VALUE
R1	120
R13	22
R19	180
C4	10
C34	15
C35	100
C21	68

REFERENCE NO.	APPROXIMATE VALUE
C27	2.2
C10	130
C11	130
C28	1.5
C29	1.5

4 CR1 AND CR2 ARE A MATCHED PAIR

3 ALL RESISTORS ARE IN OHMS, (5 PCT, 1/4 WATT.)
ALL CAPACITORS ARE IN UUF
ALL INDUCTORS ARE IN UH

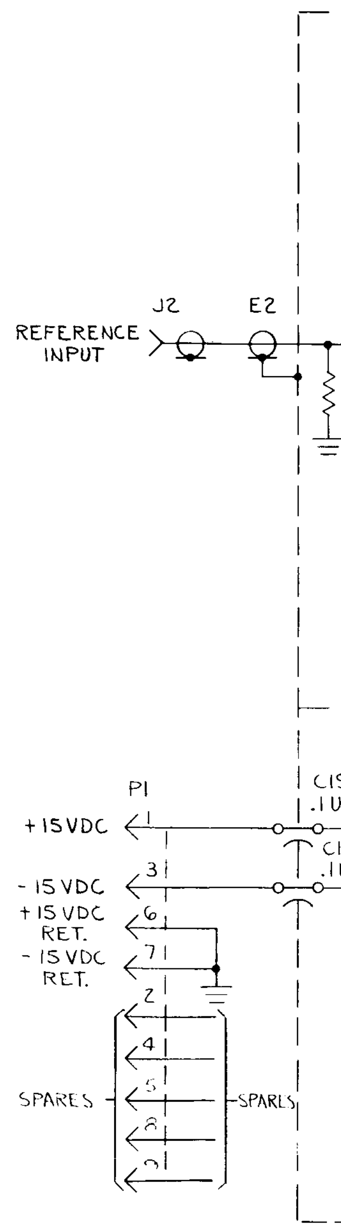
2 REFERENCE DESIGNATIONS ARE ABBREVIATED, PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION

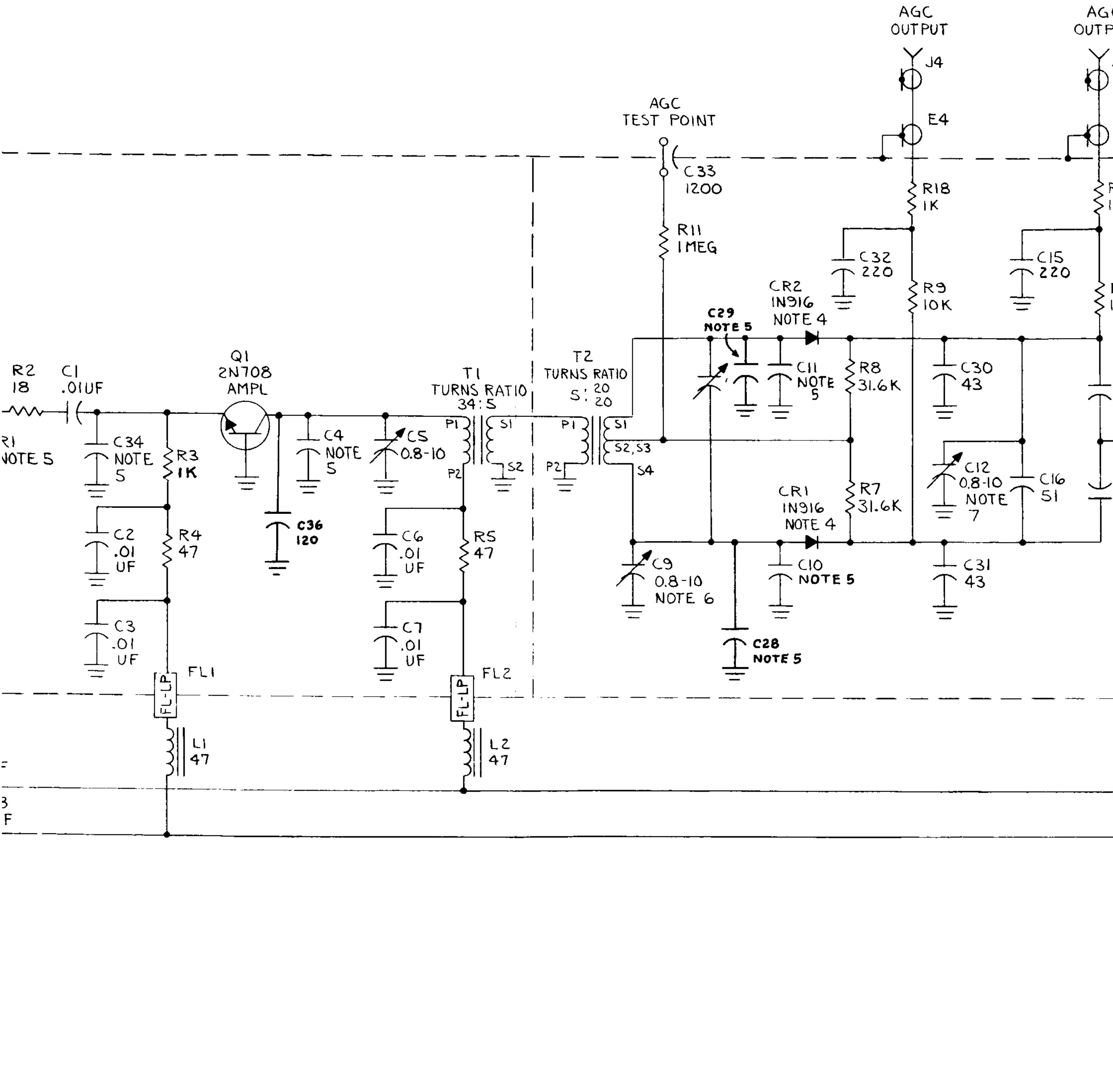
1 FOR ASSEMBLY SEE DRAWING D9330514 (MOTOROLA NO 01-21432C).

7 C12 MAY BE CONNECTED TO COMMON POINT OF C14 AND CR2 OR C13 AND CR1 AS REQUIRED IN TEST.

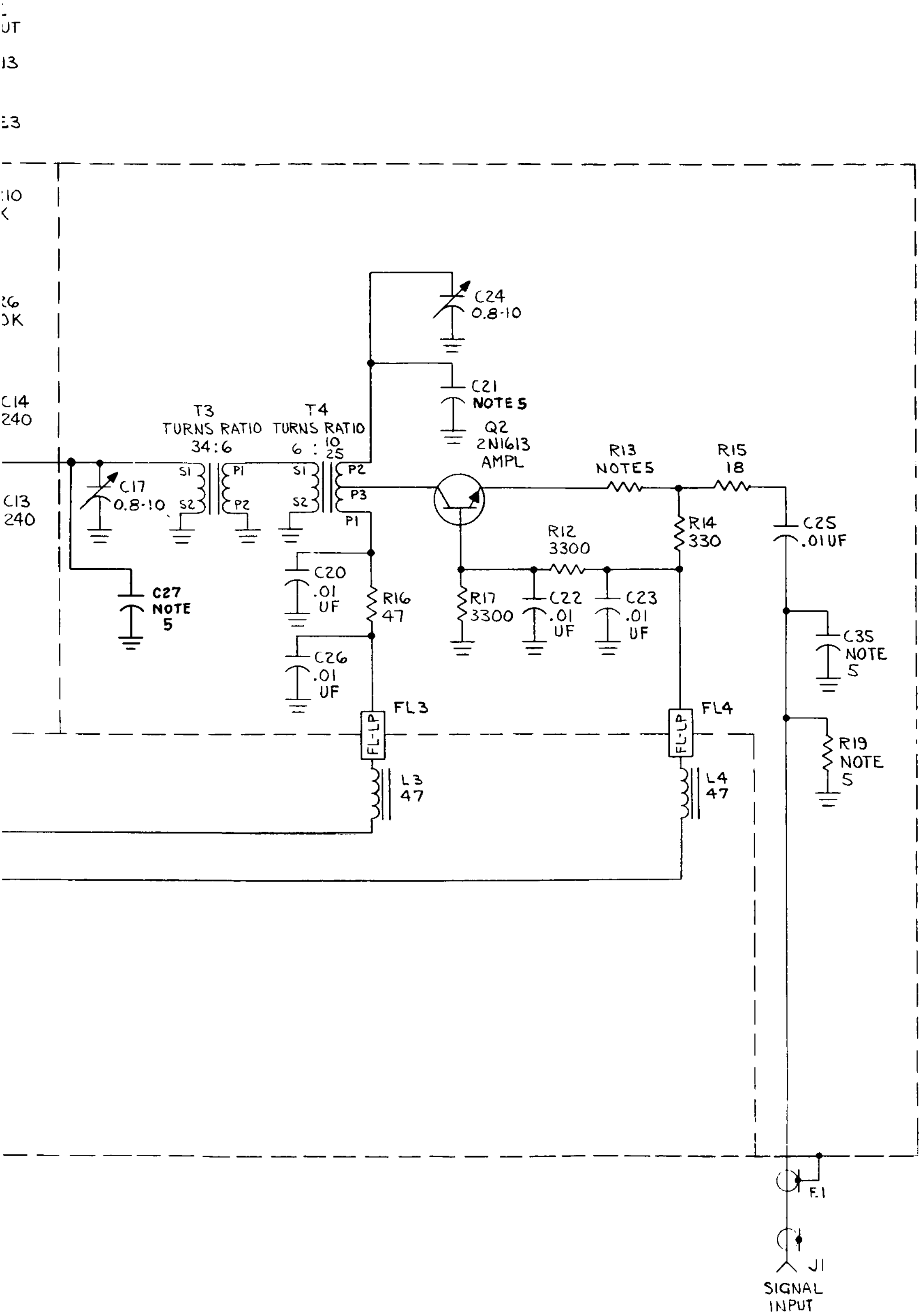
6 C9 MAY BE CONNECTED TO COMMON POINT CR1 AND C10 OR CR2 AND C11 AS REQUIRED IN TEST

NOTES: UNLESS OTHERWISE SPECIFIED




AGC OUTPUT
J4
E4
AGC TEST POINT
C33 1200
R18 1K
R11 1MEG
C32 220
C15 220
R9 10K
CR2 IN916 NOTE 4
C29 NOTE 5
R2 18
C1 .01UF
Q1 2N708 AMPL
T1 TURNS RATIO 34:5
T2 TURNS RATIO 5: 20 20
C11 NOTE 5
R8 31.6K
C30 43
NOTE 5
C34 NOTE 5
R3 1K
C4 NOTE 5
C5 0.8-10
P1
P2
S1
S2
S2, S3
S4
C12 0.8-10 NOTE 7
C16 51
CR1 IN916 NOTE 4
R7 31.6K
C2 .01 UF
R4 47
C36 120
C6 .01 UF
R5 47
C9 0.8-10 NOTE 6
C10 NOTE 5
C31 43
C3 .01 UF
C7 .01 UF
C28 NOTE 5
FL1
FL2
FL-LP
L1 47
L2 47

F



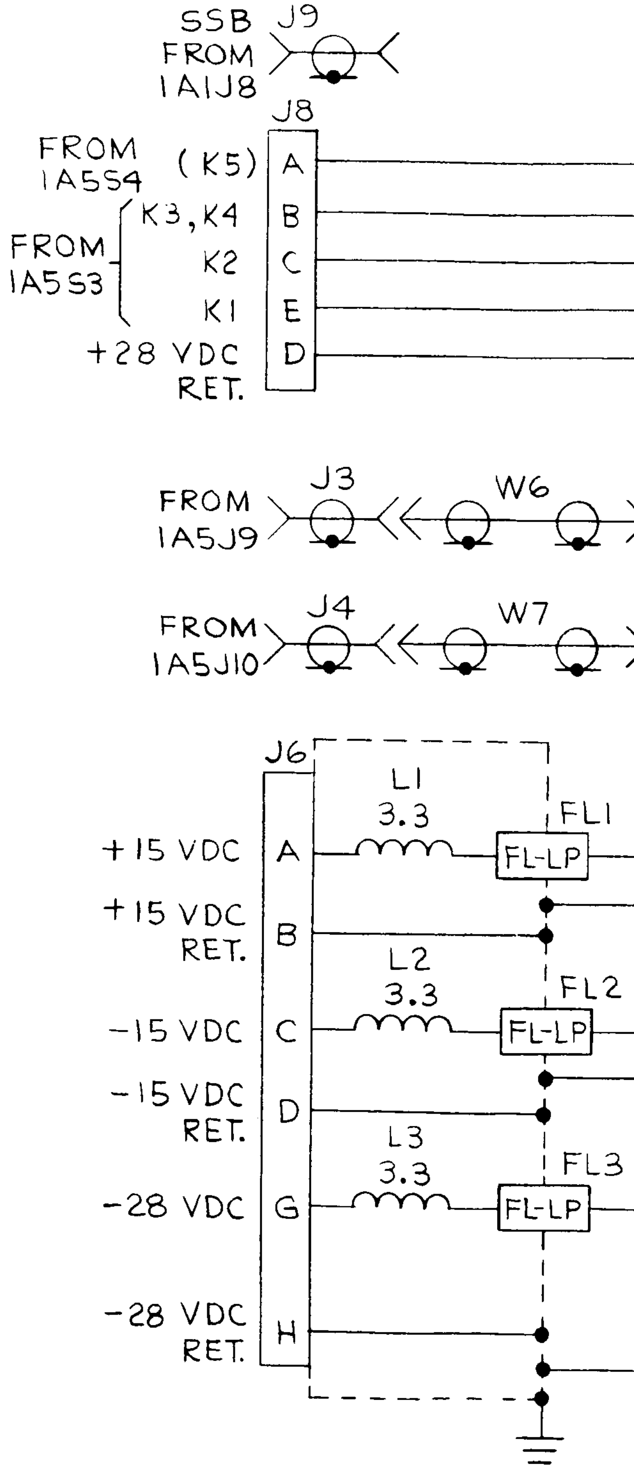
gure 6-23. 10 MC Phase Detector (1A5A2 and 1A5A4), Schematic Diagram (63-21447C)

NOTES

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION 1A6.

2. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS, ±5 PCT, 1/4 WATT.
   B. ALL INDUCTORS ARE IN UH.

3. [ ] INDICATES FRONT PANEL MARKING.



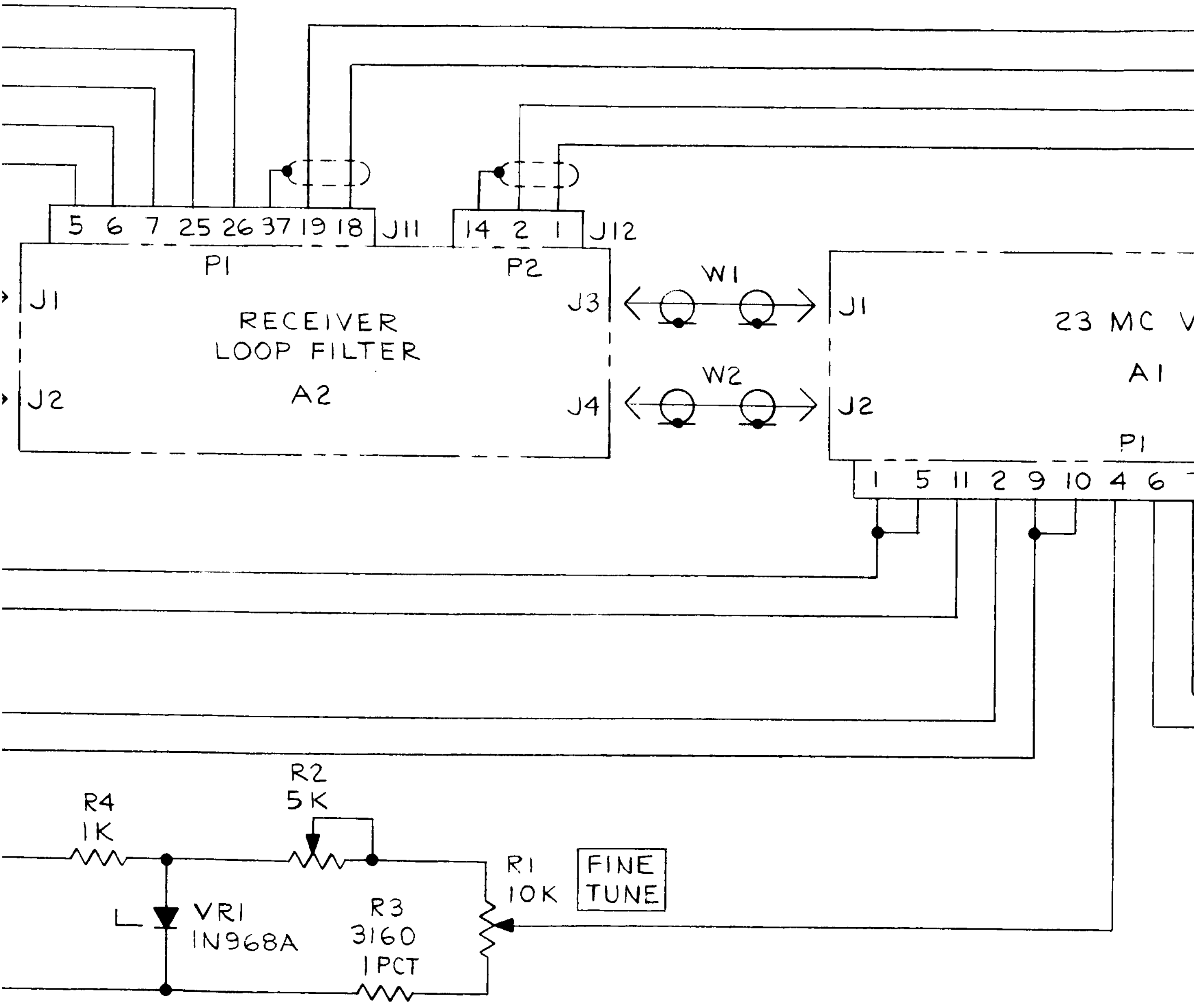
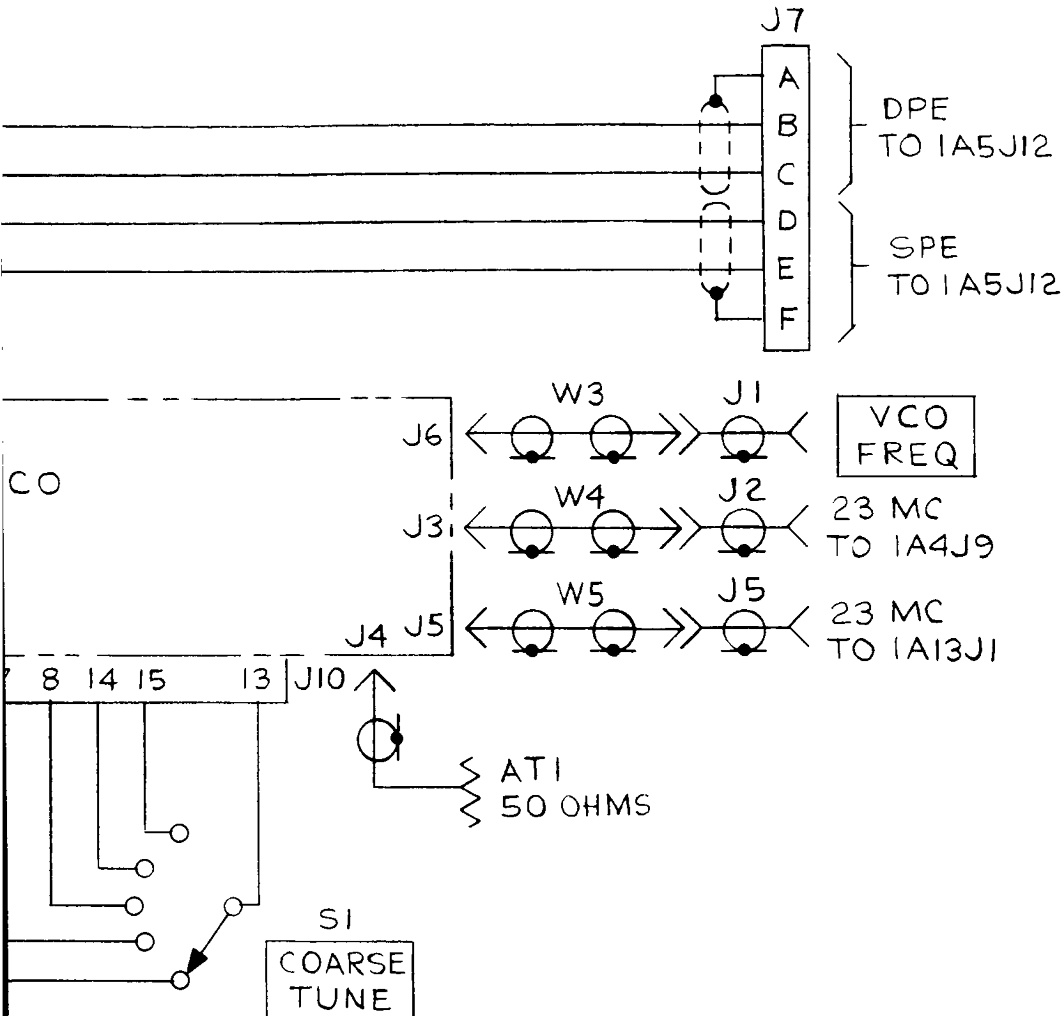

5 6 7 25 26 37 19 18
J11
14 2 1
J12
P1
P2
J1
J2
RECEIVER
LOOP FILTER
A2
J3
J4
W1
W2
J1
J2
23 MC V
A1
P1
1 5 11 2 9 10 4 6
R2
5K
R4
1K
VR1
1N968A
R3
3160
1 PCT
R1
10K
FINE
TUNE

Figure 6-2

2



4. Test Receiver, Part Three (1A6), Schematic Diagram (63-25449E)

NOTES

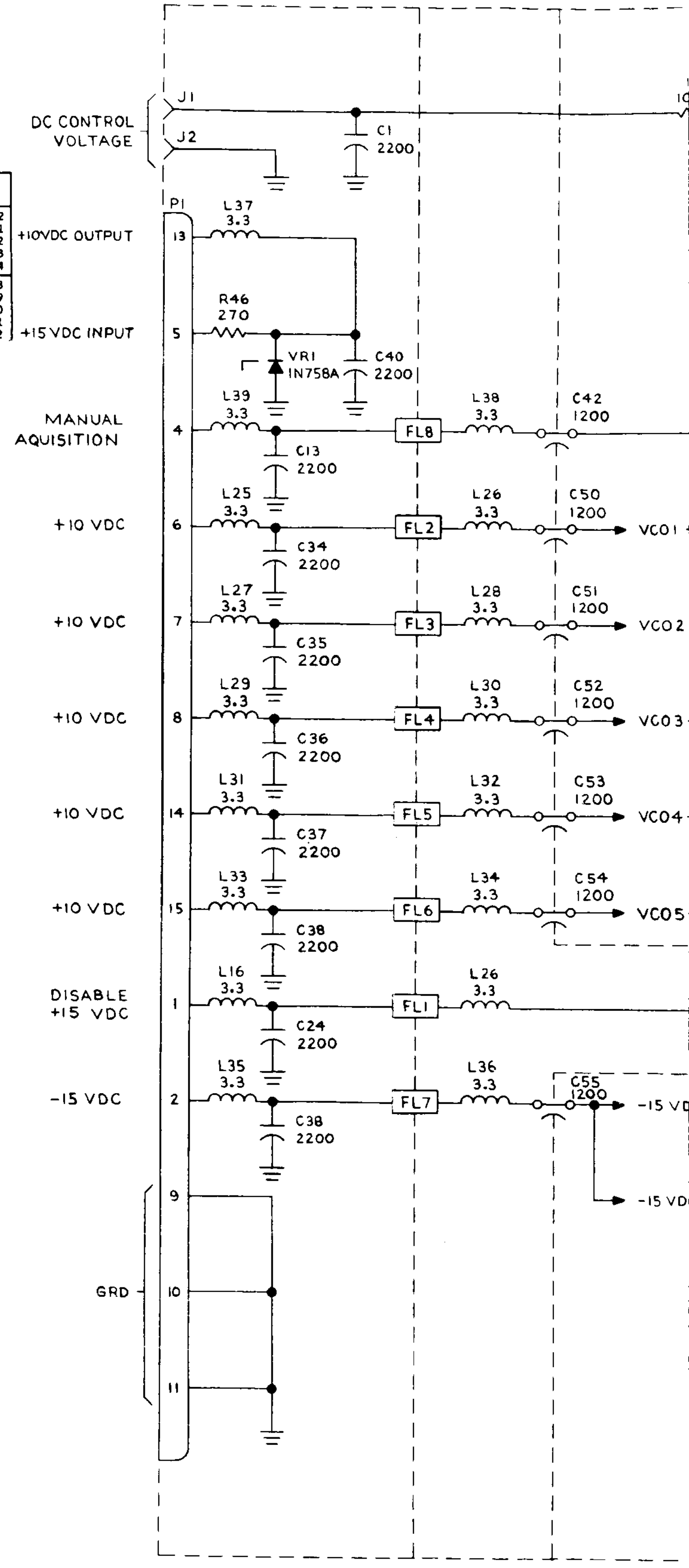
UNLESS OTHERWISE NOTED:
ALL RESISTORS ARE IN OHMS, ± 5 PCT, 1/4 WATT.
ALL CAPACITORS ARE IN UUF.
ALL INDUCTORS ARE IN UH.

2. FOR MODULE 01-25260E01. L1-5 ARE 3.2 - 8.3 UH. CAMBION PART NO. 1505-4 FOR MODULE 01-25260E02. L1-5 ARE 1.7 - 3.5 UH. CAMBION PART NO. 1505-3.

3. C3-7 VALUE CHANGE FROM 110 PF TO 2200 PF. SELECT IN TEST.

1.

REFERENCE DESIGNATION	MODULE PART NO.	CRYSTAL FREQUENCY MC	CRYSTAL PART NO.
1A9A1 Y1	01-25260E01	22.01367	48-26403C12
1A9A1 Y2	01-25260E01	22.03854	48-26403C41
1A9A1 Y3	01-25260E01	22.04209	48-26403C42
1A9A1 Y4	01-25260E01	22.04565	48-26403C43
1A9A1 Y5	01-25260E01	22.04920	48-26403C44
1A6A1 Y1	01-25260E02	23.38542	48-26403C68
1A6A1 Y2	01-25260E02	23.41242	48-26403C69
1A6A1 Y3	01-25260E02	23.41628	48-26403C70
1A6A1 Y4	01-25260E02	23.42014	48-26403C71
1A6A1 Y5	01-25260E02	23.42400	48-26403C72



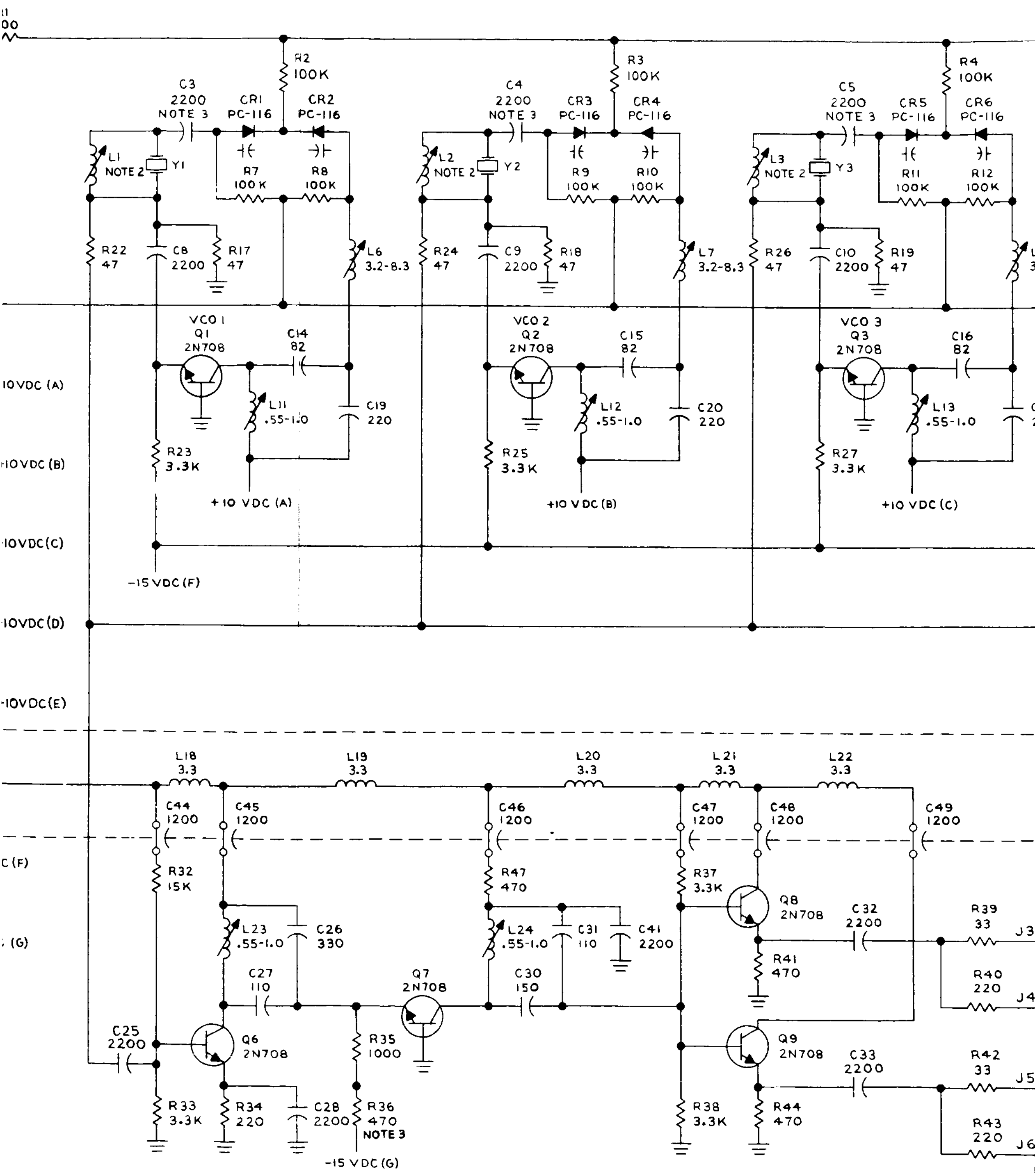
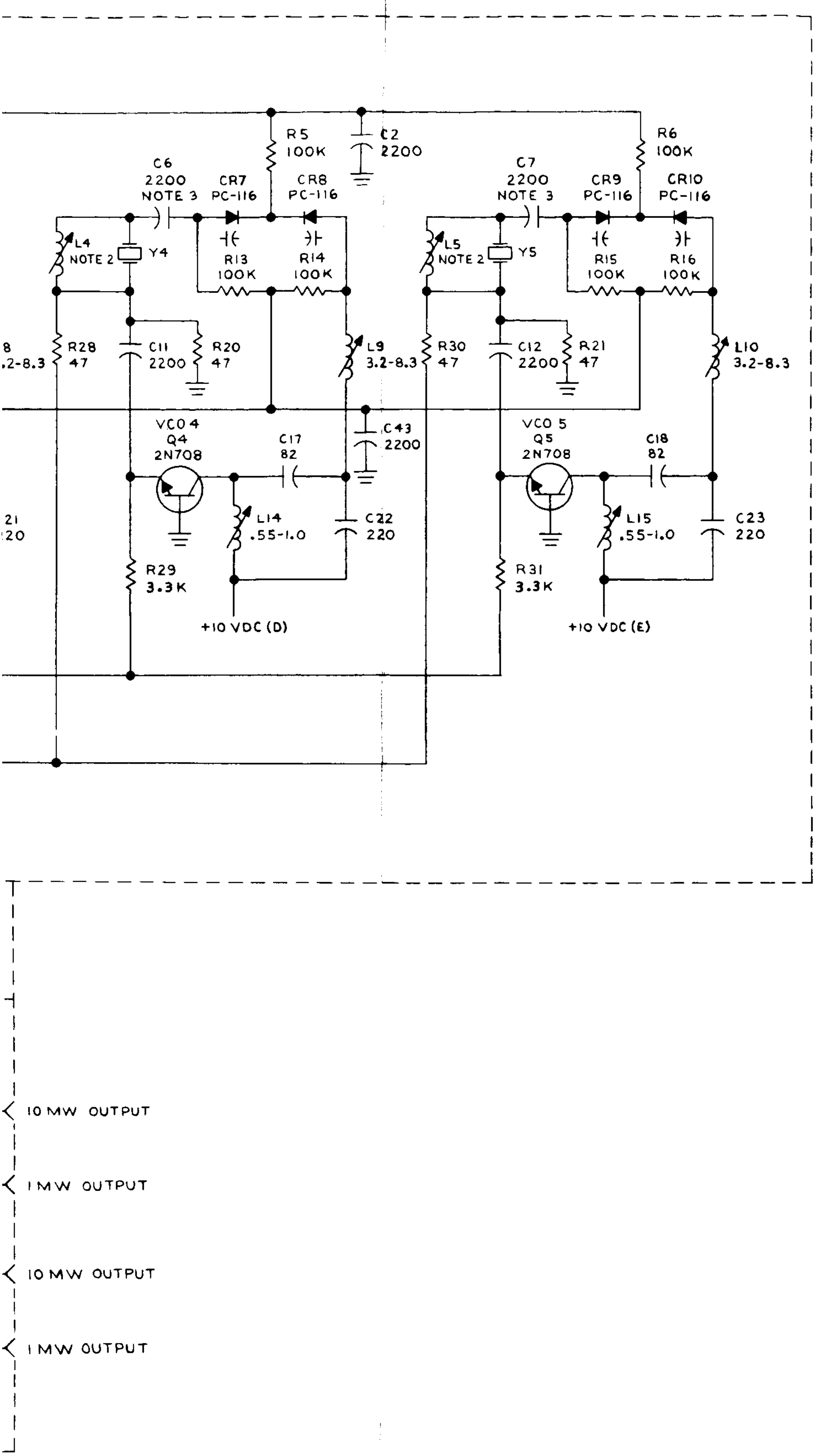
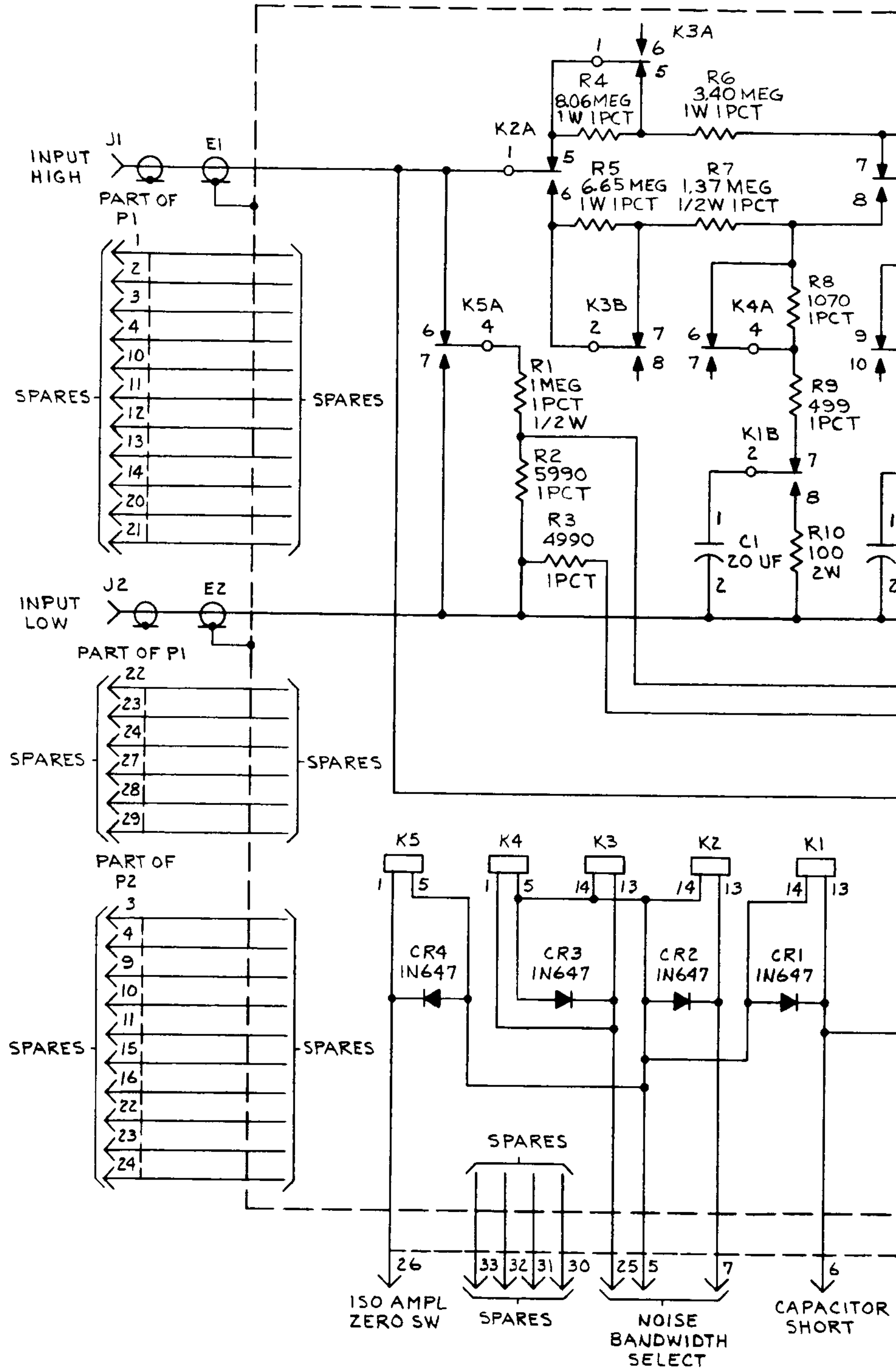

R2 100K
R3 100K
R4 100K
C3 2200 NOTE 3
C4 2200 NOTE 3
C5 2200 NOTE 3
CR1 PC-116
CR2 PC-116
CR3 PC-116
CR4 PC-116
CR5 PC-116
CR6 PC-116
L1 NOTE 2
Y1
L2 NOTE 2
Y2
L3 NOTE 2
Y3
R7 100K
R8 100K
R9 100K
R10 100K
R11 100K
R12 100K
R22 47
C8 2200
R17 47
L6 3.2-8.3
R24 47
C9 2200
R18 47
L7 3.2-8.3
R26 47
C10 2200
R19 47
VCO 1 Q1 2N708
C14 82
VCO 2 Q2 2N708
C15 82
VCO 3 Q3 2N708
C16 82
L11 .55-1.0
C19 220
L12 .55-1.0
C20 220
L13 .55-1.0
R23 3.3K
R25 3.3K
R27 3.3K
+10 VDC (A)
+10 VDC (B)
+10 VDC (C)
-15 VDC (F)
L18 3.3
L19 3.3
L20 3.3
L21 3.3
L22 3.3
C44 1200
C45 1200
C46 1200
C47 1200
C48 1200
C49 1200
R32 15K
R47 470
R37 3.3K
Q8 2N708
C32 2200
R39 33
L23 .55-1.0
C26 330
L24 .55-1.0
C31 110
C41 2200
R41 470
R40 220
C27 110
Q7 2N708
C30 150
C25 2200
Q6 2N708
R35 1000
Q9 2N708
C33 2200
R42 33
R33 3.3K
R34 220
C28 2200
R36 470 NOTE 3
R38 3.3K
R44 470
R43 220
-15 VDC (G)

Figure 6-25. 5-



Channel VCO (1A6A1 and 1A9A1), Schematic Diagram (63-25280E)

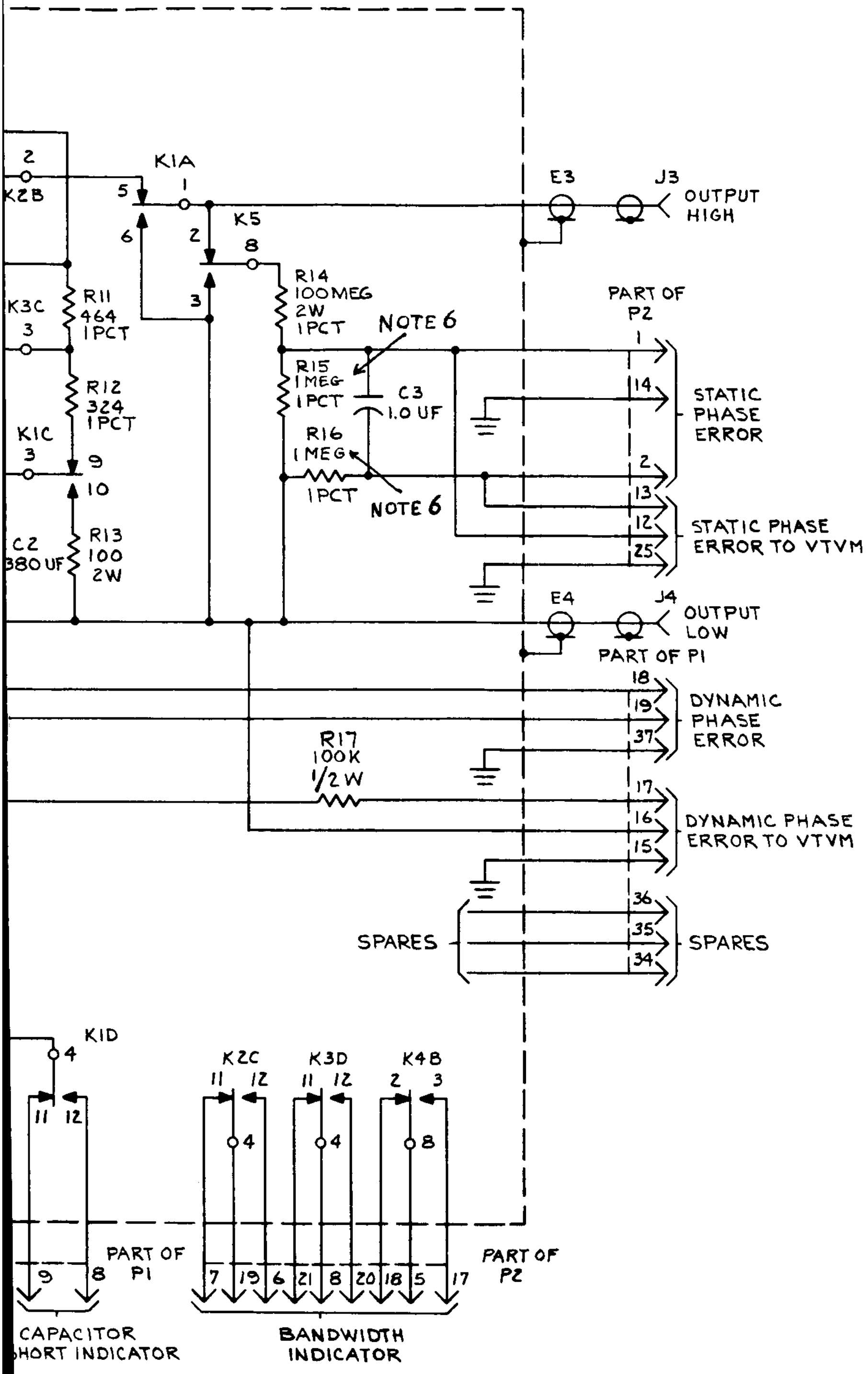


3. ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4
ALL CAPACITORS ARE IN UUF.
ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIAT
IGNATIONS WITH UNIT NUMBER AND ASSEMB

1 FOR ASSEMBLY SEE DRAWING D9330513 (M

Figure 6-26.



ATT.

D. PREFIX THE DES-
Y DESIGNATION.

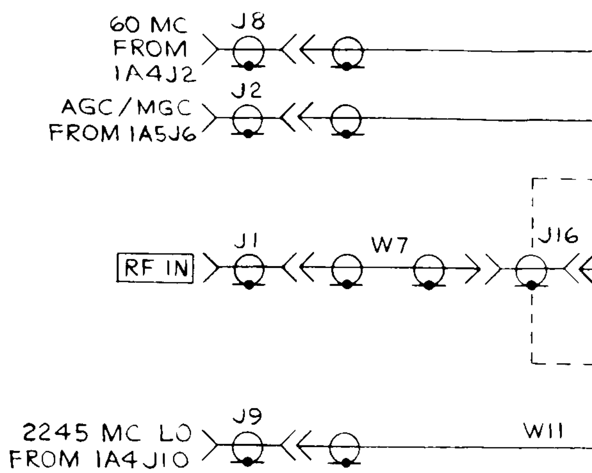
TOROLA NO.

6. RESISTORS R15 AND R16 WERE CHANGED FROM 100K TO 1MEG TO USE IN THIS ASSEMBLY.

5. BANDWIDTH RELAY LOGIC:
   5 CPS BANDWIDTH = K3 AND K4 ENERGIZED
   12 CPS BANDWIDTH = NO RELAYS ENERGIZED
   48 CPS BANDWIDTH = K2, K3 AND K4 ENERGIZED
   152 CPS BANDWIDTH = K2 ENERGIZED

4. ALL RELAYS SHOWN IN DE-ENGERIZED STATE.

Loop Filter (1A6A2), Schematic Diagram (63-23863D)

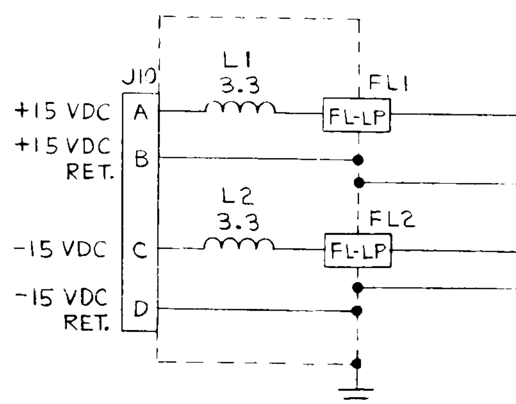


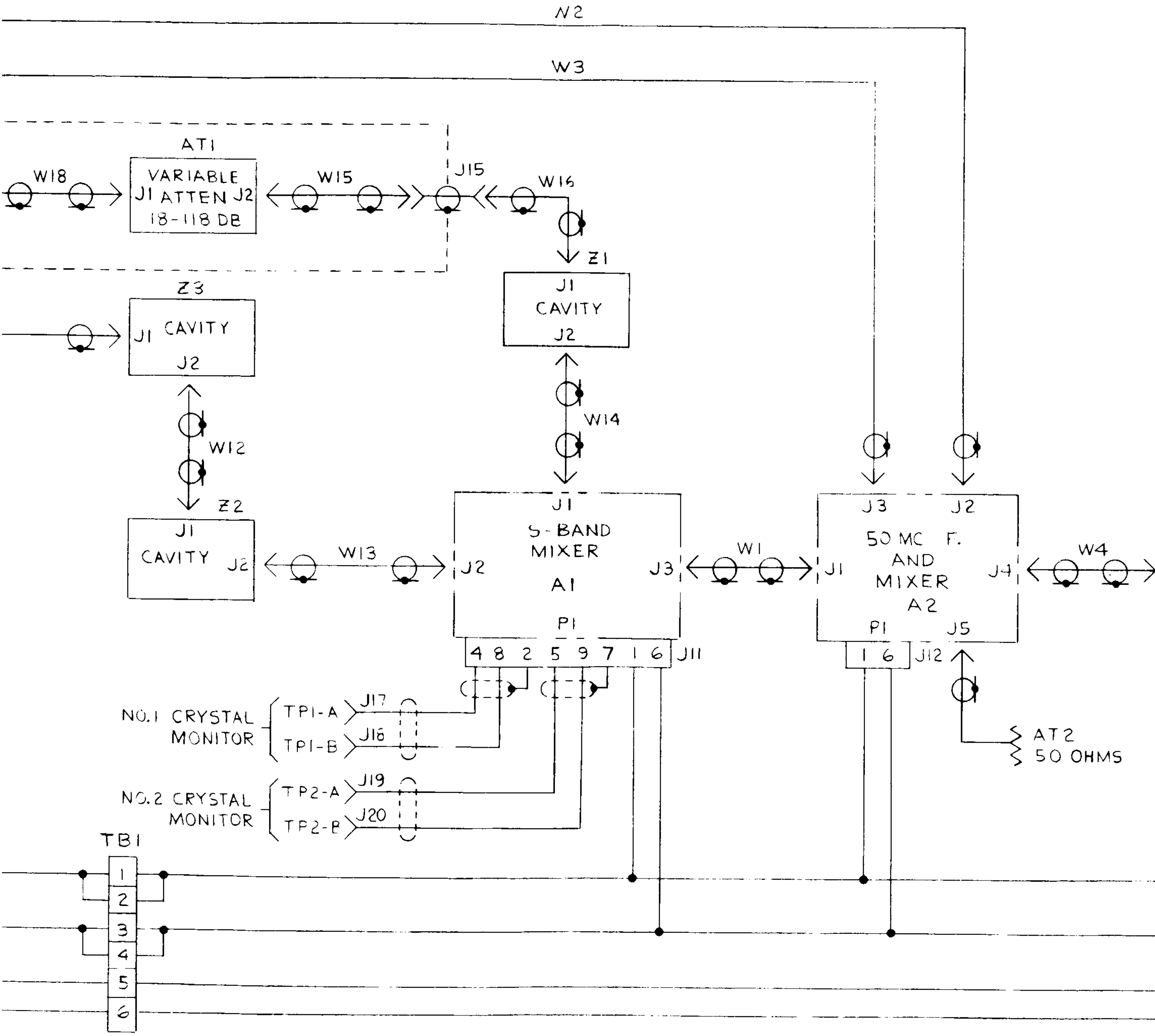
NOTES

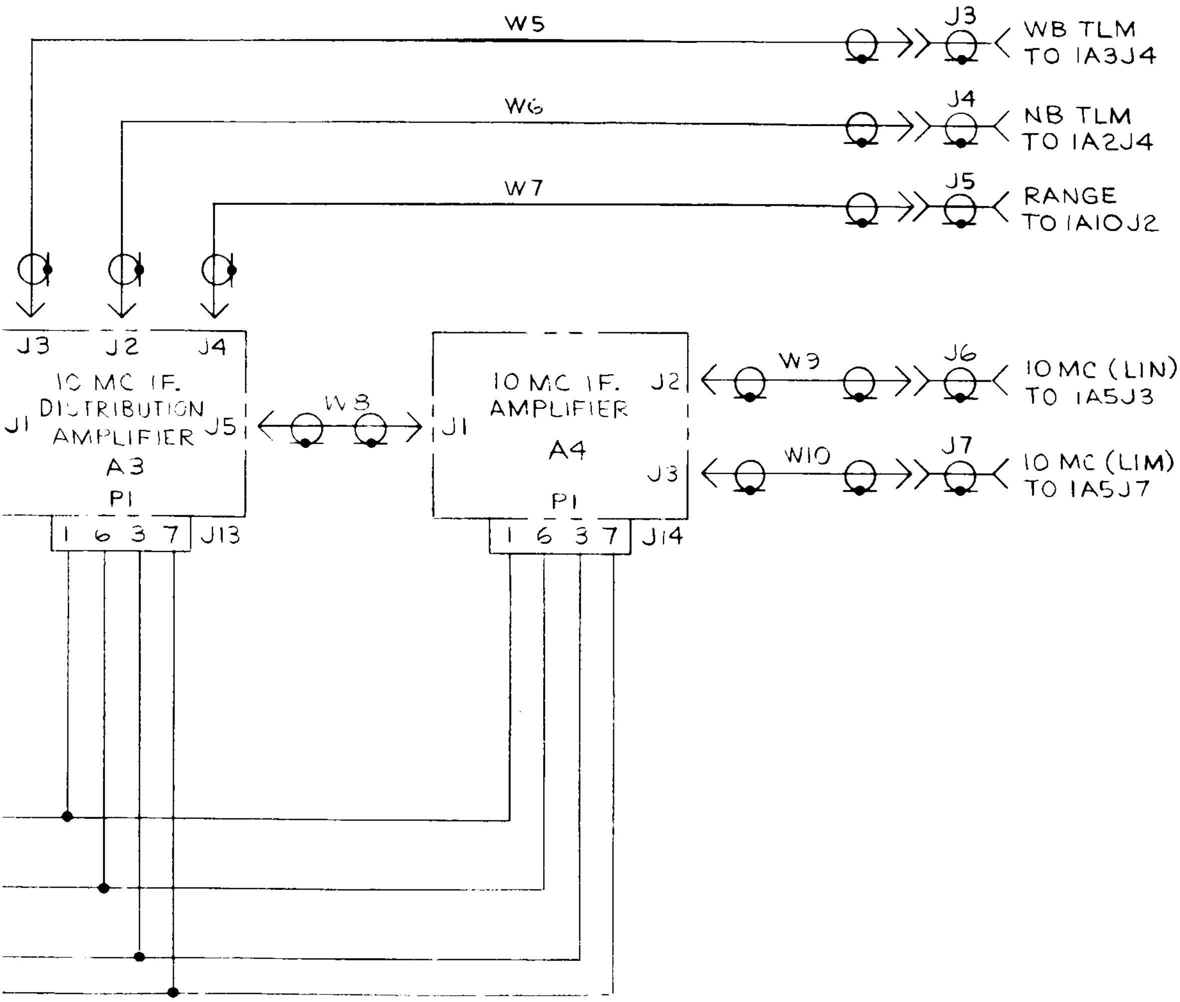
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION 1A7.

2. UNLESS OTHERWISE SPECIFIED:
   ALL INDUCTORS ARE IN UH.

3. ▭ INIDCATES FRONT PANEL MARKING.




W2
W3
AT1
W18
VARIABLE
J1 ATTEN J2
18-118 DB
W15
J15
W16
Z1
J1
CAVITY
J2
Z3
J1 CAVITY
J2
W14
W12
Z2
J1
CAVITY J2
W13
J1
S-BAND
MIXER
J2
J3
A1
P1
4 8 2 5 9 7 1 6 J11
W1
J3 J2
50 MC F.
AND
MIXER
J1
J4
A2
P1 J5
1 6 J12
W4
AT2
50 OHMS
NO.1 CRYSTAL
MONITOR
TP1-A
TP1-B
J17
J18
NO.2 CRYSTAL
MONITOR
TP2-A
TP2-B
J19
J20
TB1
1
2
3
4
5
6



igure 6-27. Test Receiver, Part Four (1A7), Schematic Diagram (63-25450E)

4. VALUE SELECTED IN TEST.

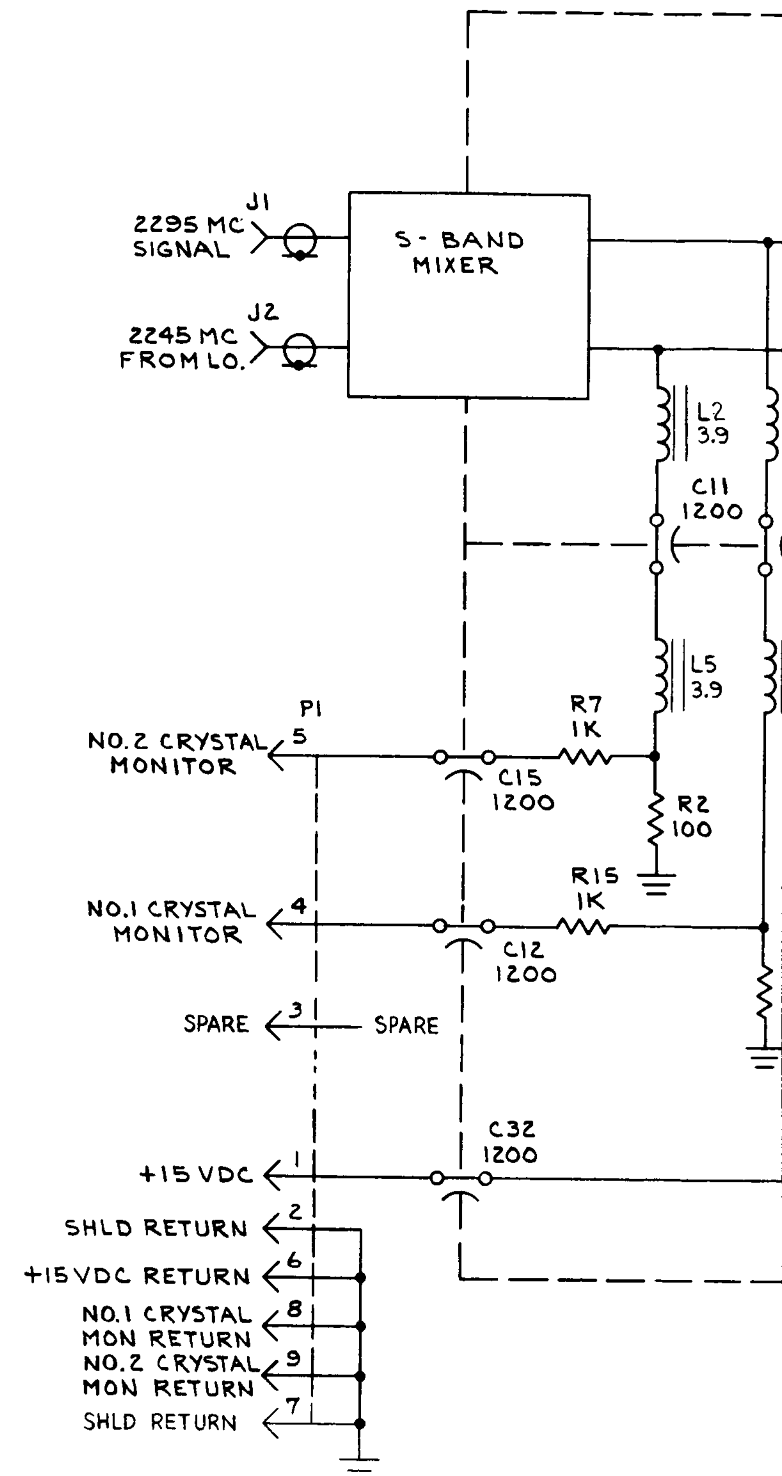
REFERENCE NO.	APPROXIMATE VALUE
R10	390
R26	10K
R25	27K

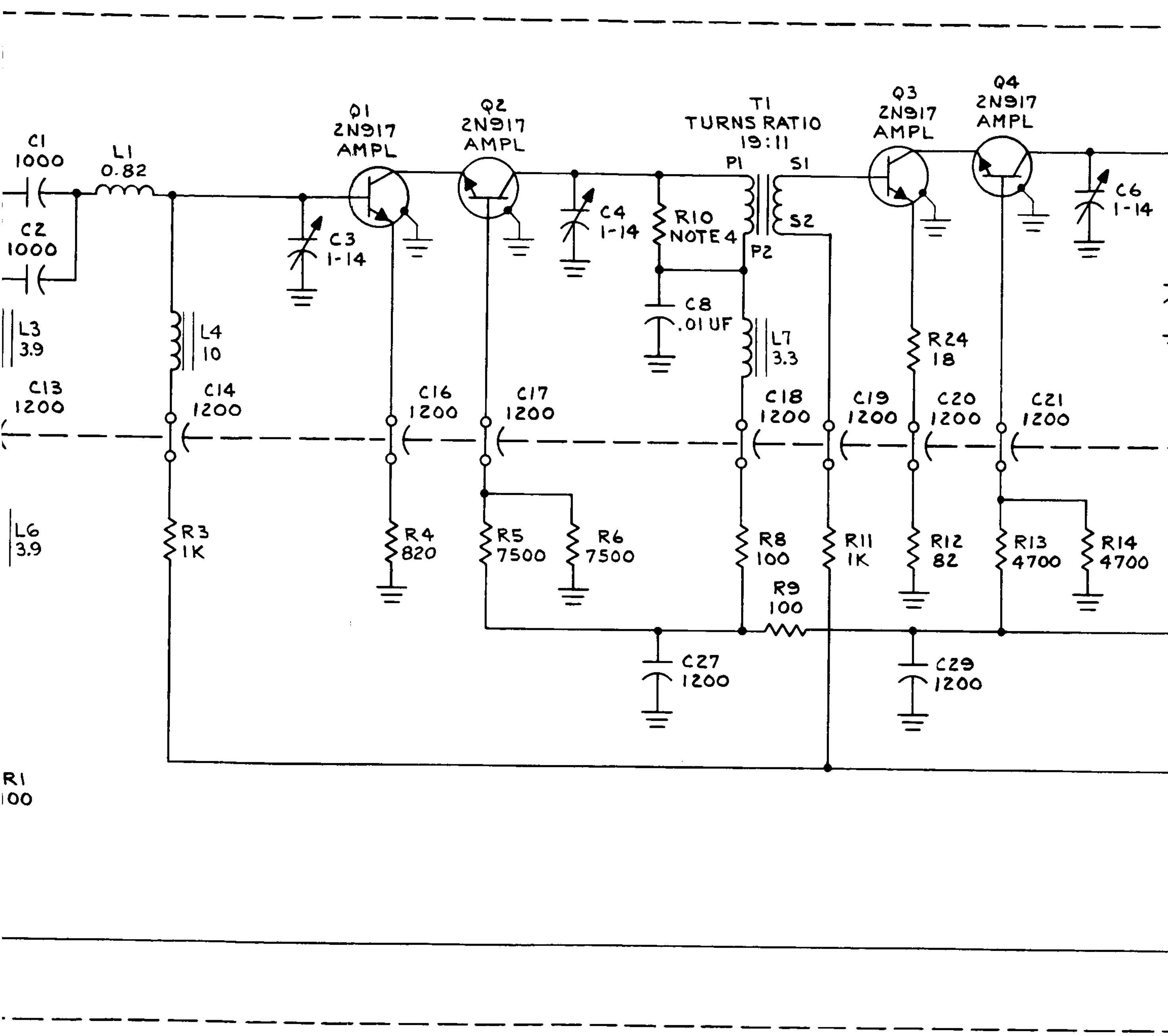
3. ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UUF.
   ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330502 (MOTOROLA NO. 01-23773D).

NOTES: UNLESS OTHERWISE SPECIFIED





C1
1000
C2
1000
L1
0.82
L3
3.9
L4
10
C13
1200
C14
1200
L6
3.9
R3
1K
R1
100
Q1
2N917
AMPL
C3
1-14
Q2
2N917
AMPL
C16
1200
C17
1200
R4
820
R5
7500
R6
7500
C4
1-14
T1
TURNS RATIO
19:11
P1
S1
S2
P2
R10
NOTE 4
C8
.01 UF
L7
3.3
C18
1200
C19
1200
R8
100
R9
100
R11
1K
C27
1200
Q3
2N917
AMPL
R24
18
C20
1200
R12
82
C29
1200
Q4
2N917
AMPL
C6
1-14
C21
1200
R13
4700
R14
4700

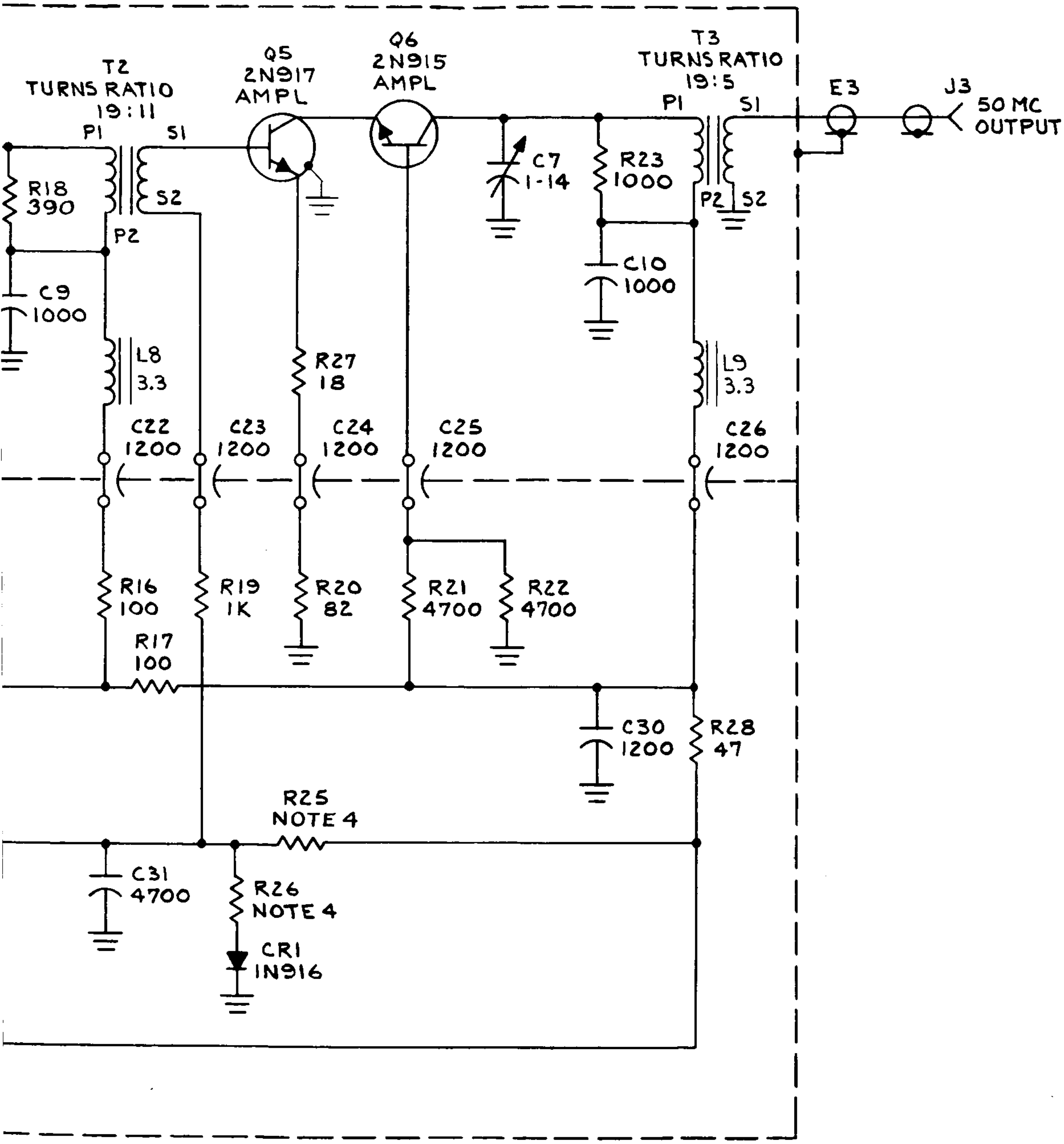


Figure 6-28. Balanced Mixer-Preamplifier (1A7A1), Schematic Diagram (63-23879D)

5. CIRCUIT TO BE SELECTED AT TEST TO OBTAIN 18K NOMINAL VALUE.

4. VALUE TO BE SELECTED IN TEST

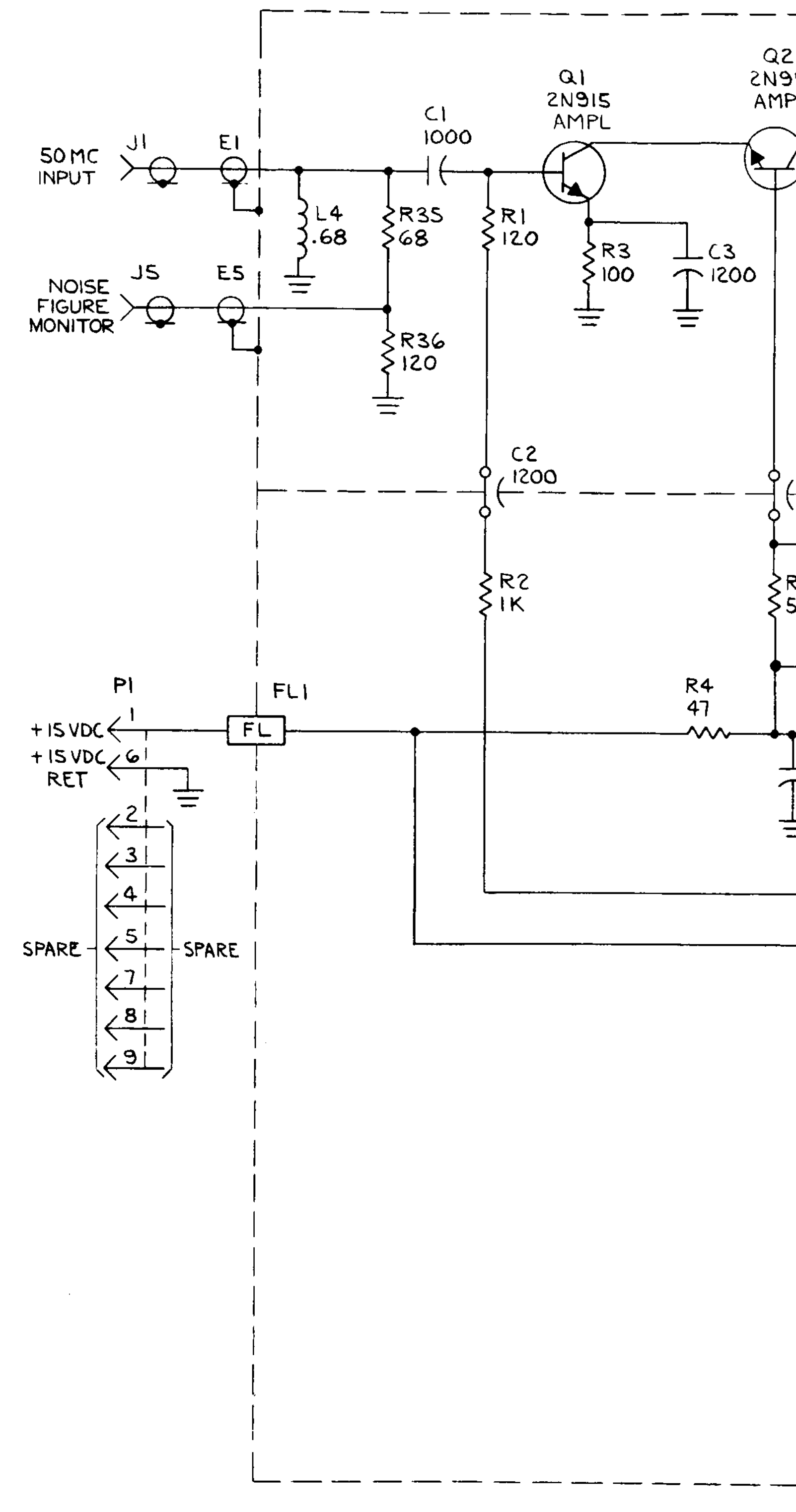
REFERENCE NO.	APPROXIMATE VALUE
R38	1500
R39	1500
R43	3000
C28	270
L5	0.82

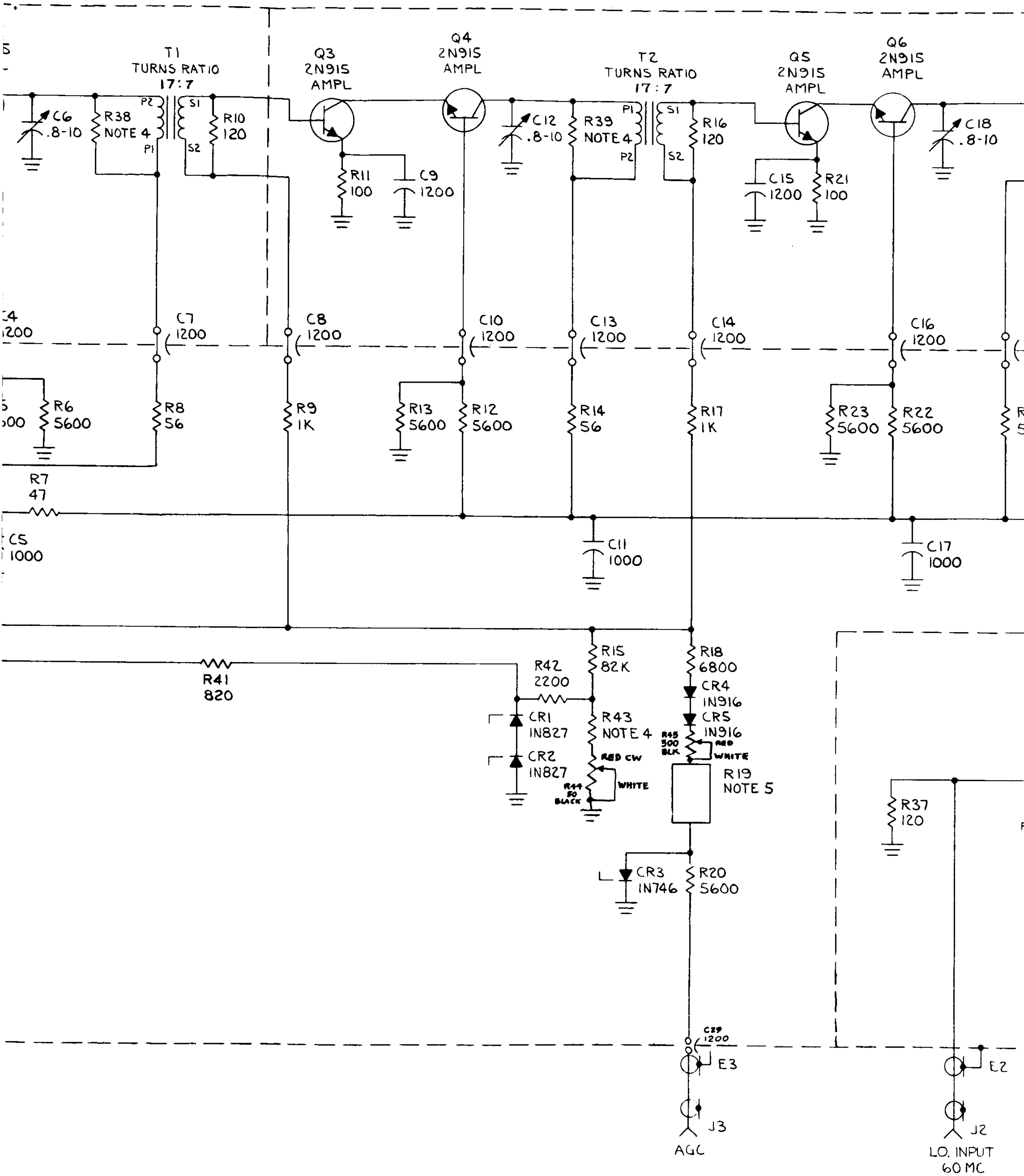
3. ALL RESISTORS ARE IN OHMS, (5PCT, 1/4 WATT.)
ALL CAPACITORS ARE IN UUF
ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

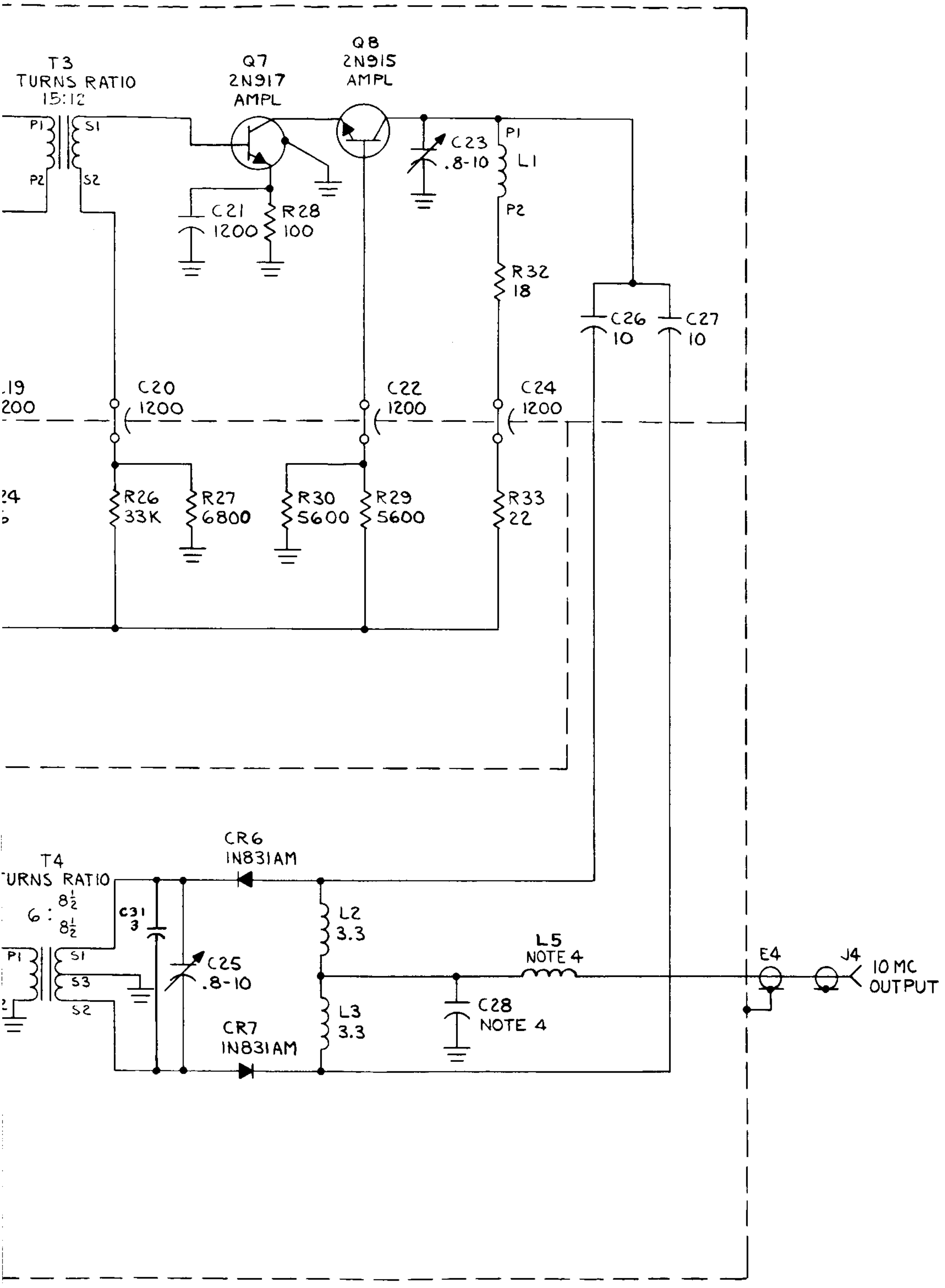
1. FOR ASSEMBLY SEE DRAWING D9330503 (MOTOROLA NO. 01-23774D).

NOTES: UNLESS OTHERWISE SPECIFIED




T1
TURNS RATIO
17:7
C6
.8-10
R38
NOTE 4
P2
P1
S1
S2
R10
120
Q3
2N915
AMPL
R11
100
C9
1200
Q4
2N915
AMPL
C12
.8-10
R39
NOTE 4
T2
TURNS RATIO
17:7
P1
P2
S1
S2
R16
120
Q5
2N915
AMPL
C15
1200
R21
100
Q6
2N915
AMPL
C18
.8-10
1200
C7
1200
C8
1200
C10
1200
C13
1200
C14
1200
C16
1200
R6
5600
R8
56
R9
1K
R13
5600
R12
5600
R14
56
R17
1K
R23
5600
R22
5600
R7
47
C5
1000
C11
1000
C17
1000
R41
820
R42
2200
R15
82K
R18
6800
CR1
IN827
CR2
IN827
R43
NOTE 4
RED CW
WHITE
R44
50
BLACK
CR4
IN916
CR5
IN916
R45
500
BLK
RED
WHITE
R19
NOTE 5
CR3
IN746
R20
5600
R37
120
C29
1200
E3
J3
AGC
E2
J2
LO. INPUT
60 MC

Figure



6-29. 50 MC IF Amplifier and Second Mixer (1A7A2), Schematic Diagram (63-21450C)

3. ALL RESISTORS ARE IN OHMS ±5 PCT, 1/4 WATT.
ALL CAPACITORS ARE IN UF.
ALL INDUCTORS ARE IN UH.

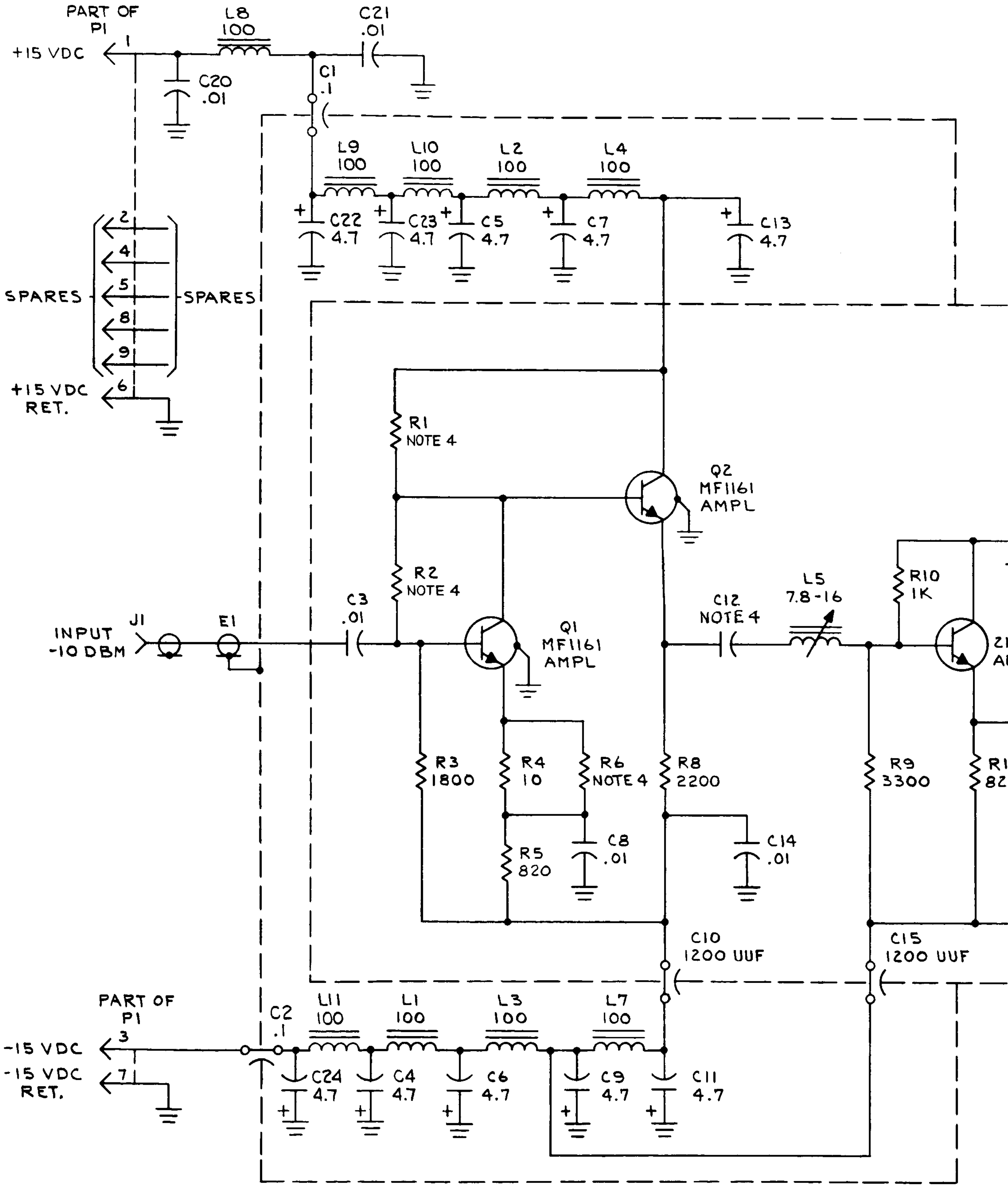
2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330504 (MOTOROLA NO. 01-23775D).

4. VALUE TO BE SELECTED IN TEST.

REFERENCE NO.	APPROXIMATE VALUE
R1	680
R6	15
R2	1500
C12	47
C18	22

NOTES: UNLESS OTHERWISE SPECIFIED


PART OF
P1
+15 VDC
1
L8
100
C21
.01
C20
.01
C1
.1
L9
100
L10
100
L2
100
L4
100
C22
4.7
C23
4.7
C5
4.7
C7
4.7
C13
4.7
2
4
5
8
9
SPARES
SPARES
+15 VDC
RET.
6
R1
NOTE 4
Q2
MF1161
AMPL
R2
NOTE 4
INPUT
-10 DBM
J1
E1
C3
.01
Q1
MF1161
AMPL
C12
NOTE 4
L5
7.8-16
R10
1K
R3
1800
R4
10
R6
NOTE 4
R8
2200
R9
3300
R5
820
C8
.01
C14
.01
C10
1200 UUF
C15
1200 UUF
PART OF
P1
C2
.1
L11
100
L1
100
L3
100
L7
100
-15 VDC
3
-15 VDC
RET.
7
C24
4.7
C4
4.7
C6
4.7
C9
4.7
C11
4.7

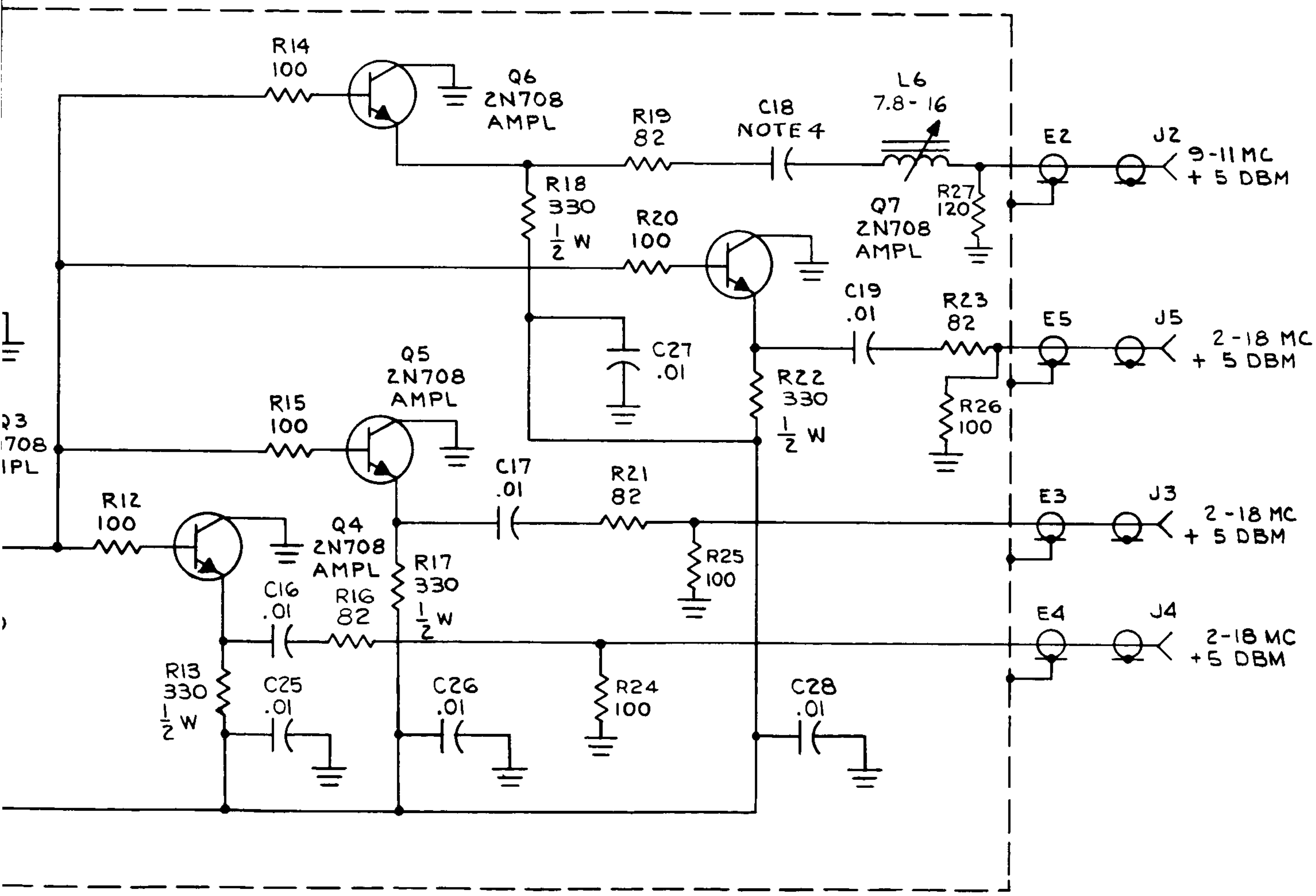


Figure 6-30. 10 MC Distribution Amplifier (1A7A3), Schematic Diagram (63-23886D)

5. VALUE TO BE SELECTED IN TEST

REFERENCE NO.	APPROXIMATE VALUE
R34	100
R32	100
R18	62
R9	1000
R16	110

4. SELECTED IN TEST AS REQUIRED FOR TEMPERATURE COMPENSATION.

REFERENCE NO.	TEMPERATURE COEFFICIENT	NOMINAL VALUE
C27	N5600	10
C37	N5600	10
C38	N5600	10

3. ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4 WATT.

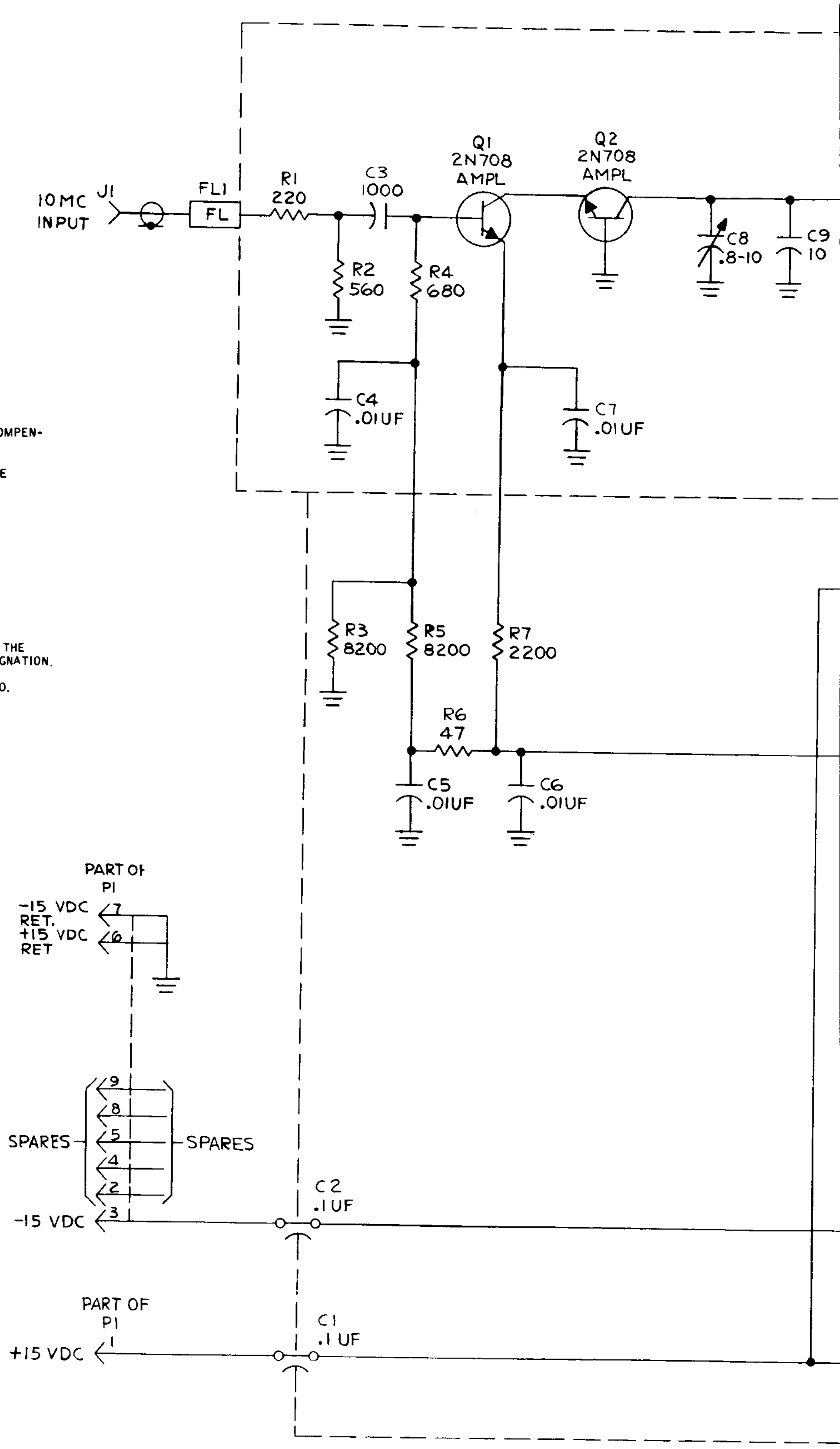
ALL CAPACITORS ARE IN UUF.

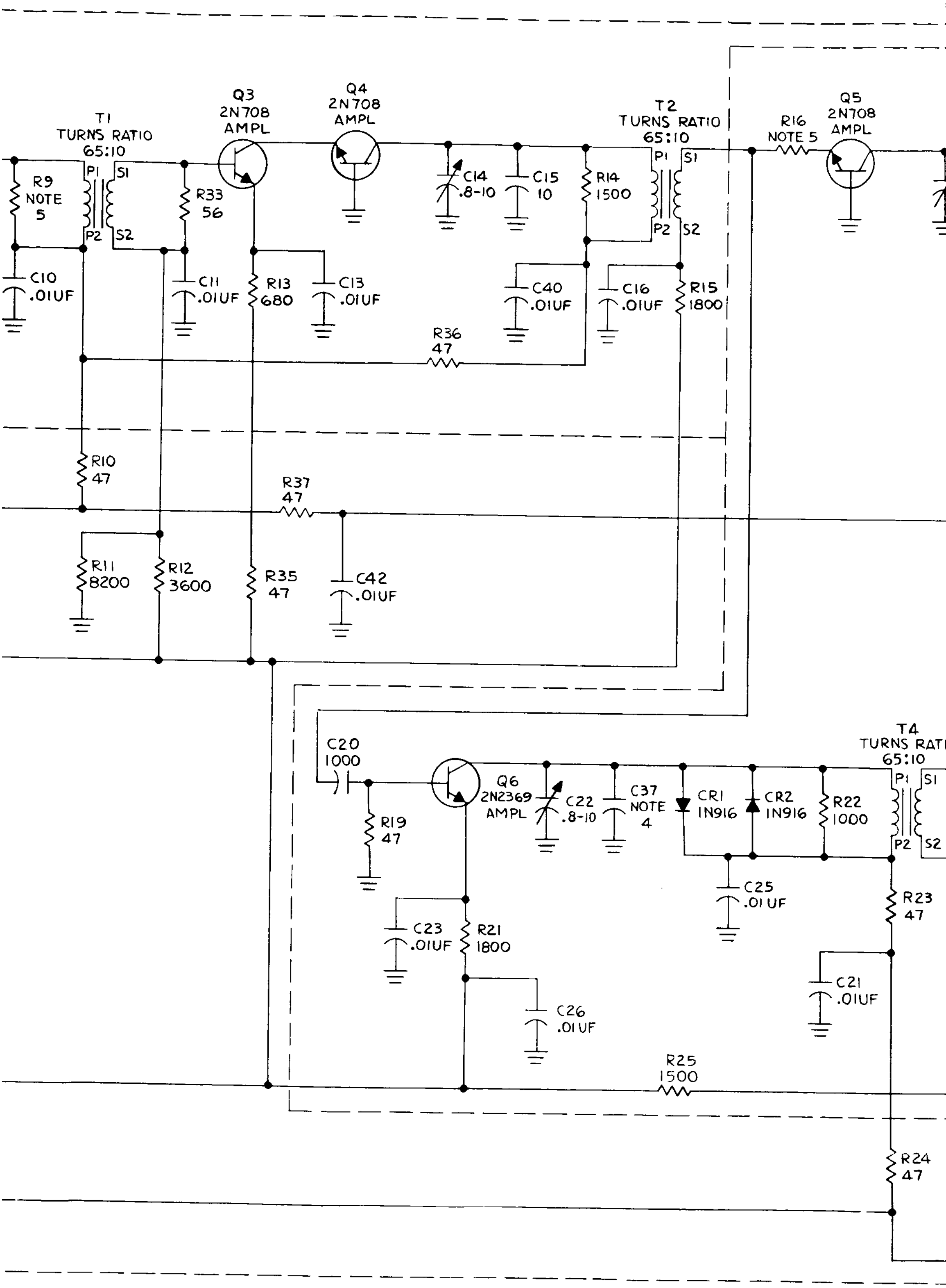
ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330505 (MOTOROLA NO. 01-23776D.

NOTES: UNLESS OTHERWISE SPECIFIED




T1
TURNS RATIO
65:10
P1
S1
P2
S2
R9
NOTE
5
C10
.01UF
Q3
2N708
AMPL
R33
56
C11
.01UF
R13
680
C13
.01UF
Q4
2N708
AMPL
C14
.8-10
C15
10
C40
.01UF
R14
1500
T2
TURNS RATIO
65:10
P1
S1
P2
S2
C16
.01UF
R15
1800
R36
47
R16
NOTE 5
Q5
2N708
AMPL
R10
47
R37
47
R11
8200
R12
3600
R35
47
C42
.01UF
C20
1000
R19
47
Q6
2N2369
AMPL
C22
.8-10
C37
NOTE
4
CR1
1N916
CR2
1N916
R22
1000
T4
TURNS RATI
65:10
P1
S1
P2
S2
C25
.01 UF
C23
.01UF
R21
1800
R23
47
C21
.01UF
C26
.01 UF
R25
1500
R24
47

2

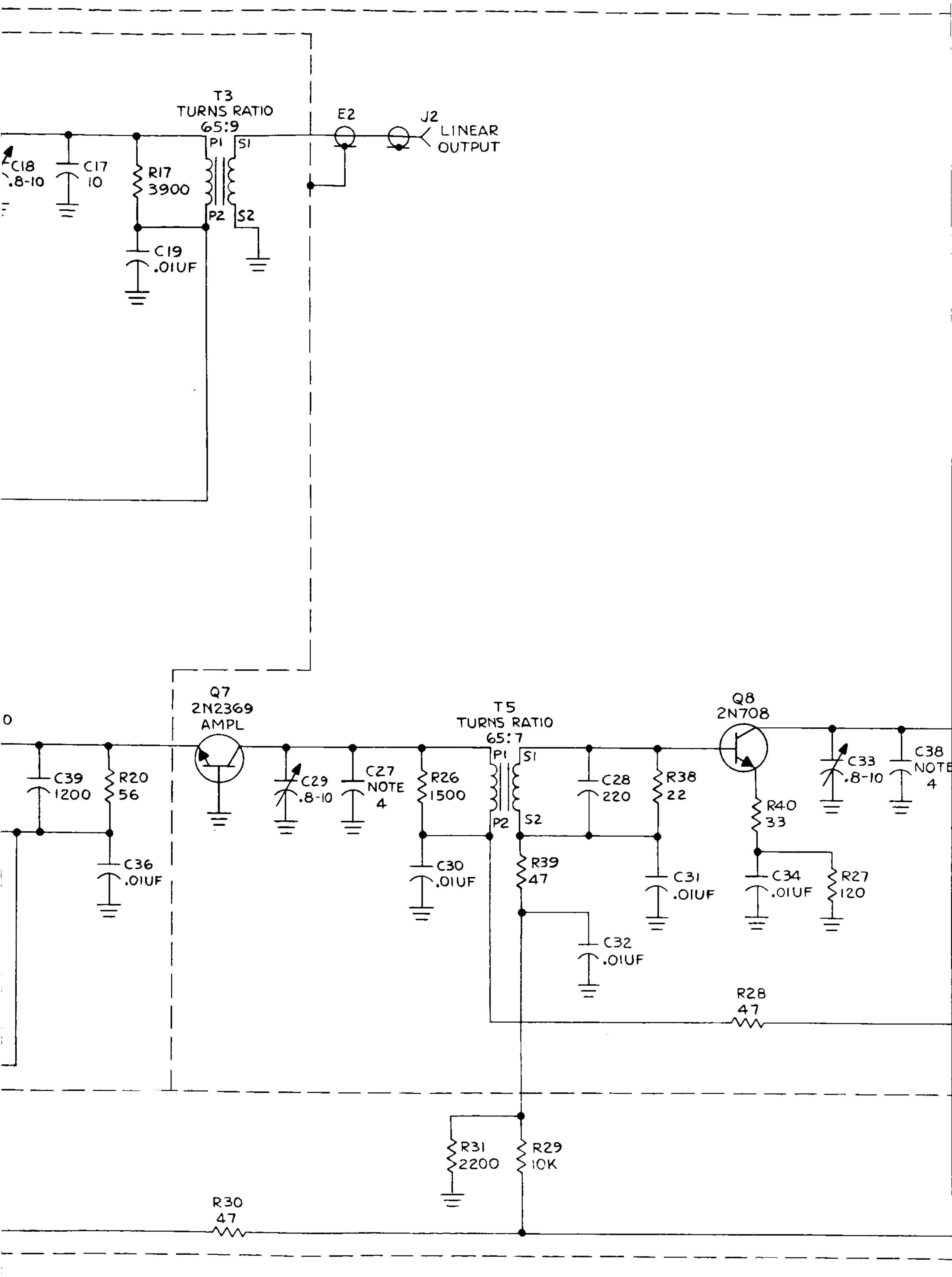
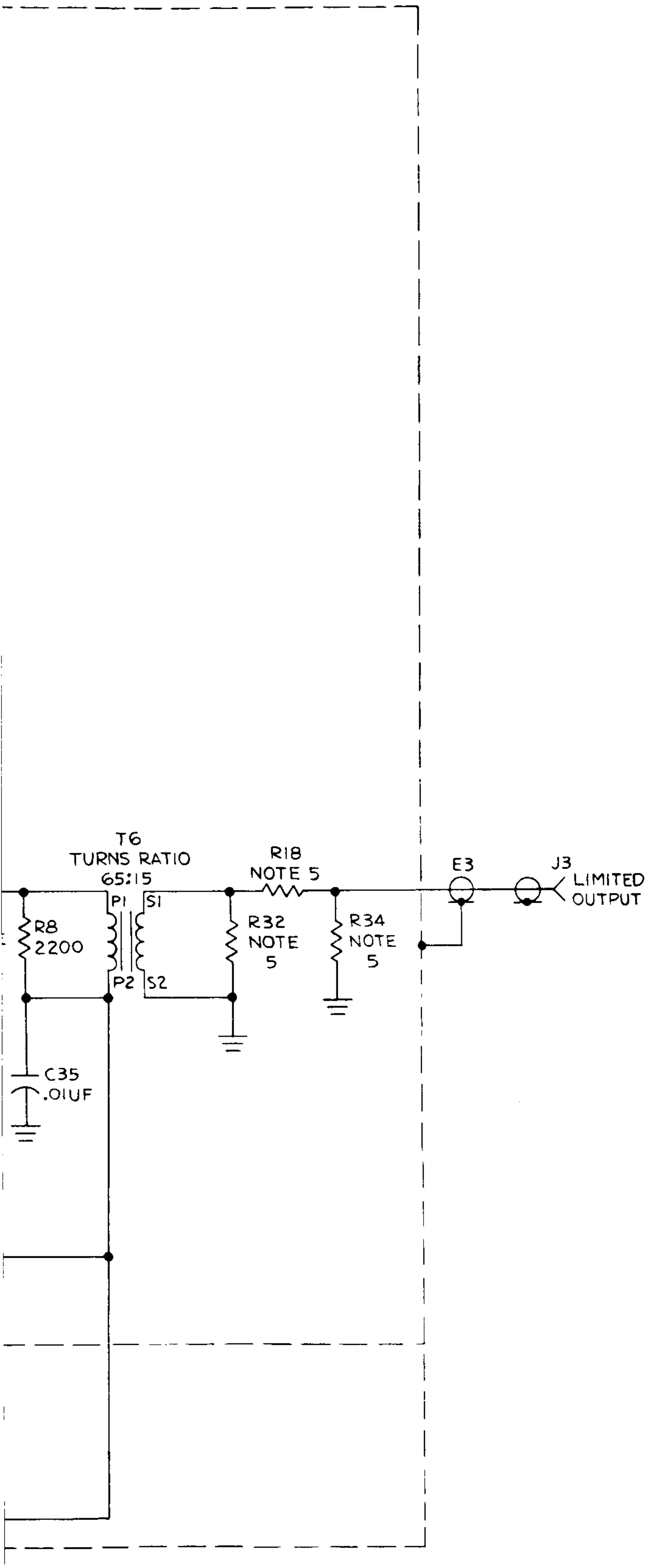


Figure 6-31. 10 MC IF Amplifier (I



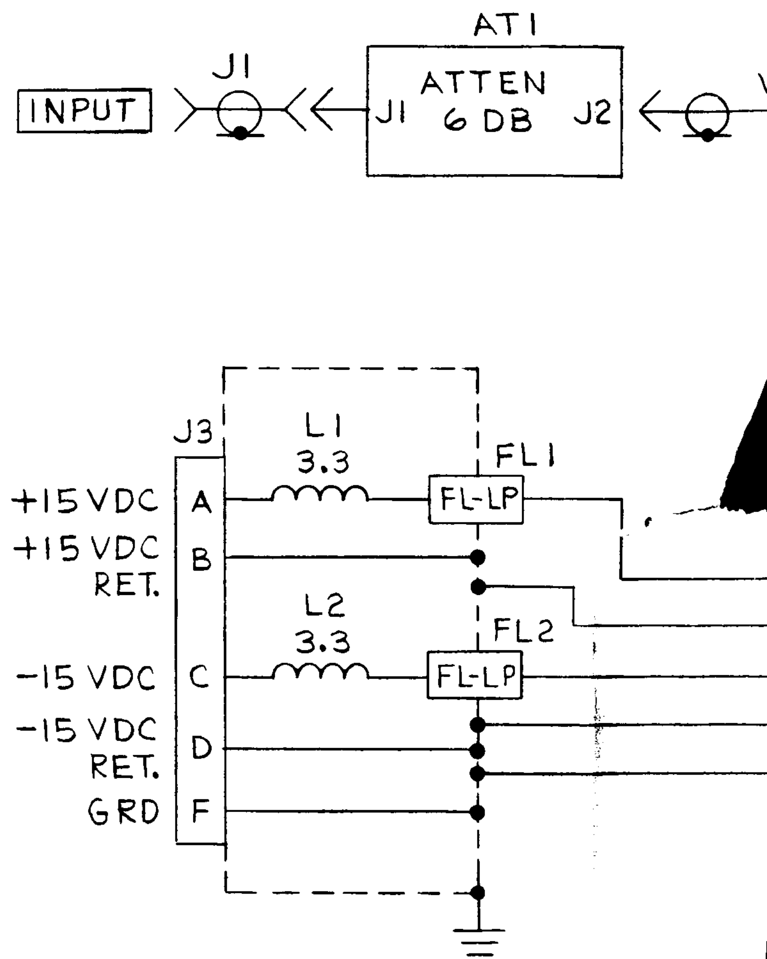
.A7A4), Schematic Diagram (63-21449C)

NOTES

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION 1A8.

2. UNLESS OTHERWISE SPECIFIED:
   A. ALL INDUCTORS ARE IN UH.

3. ▭ INDICATES FRONT PANEL MARKING.



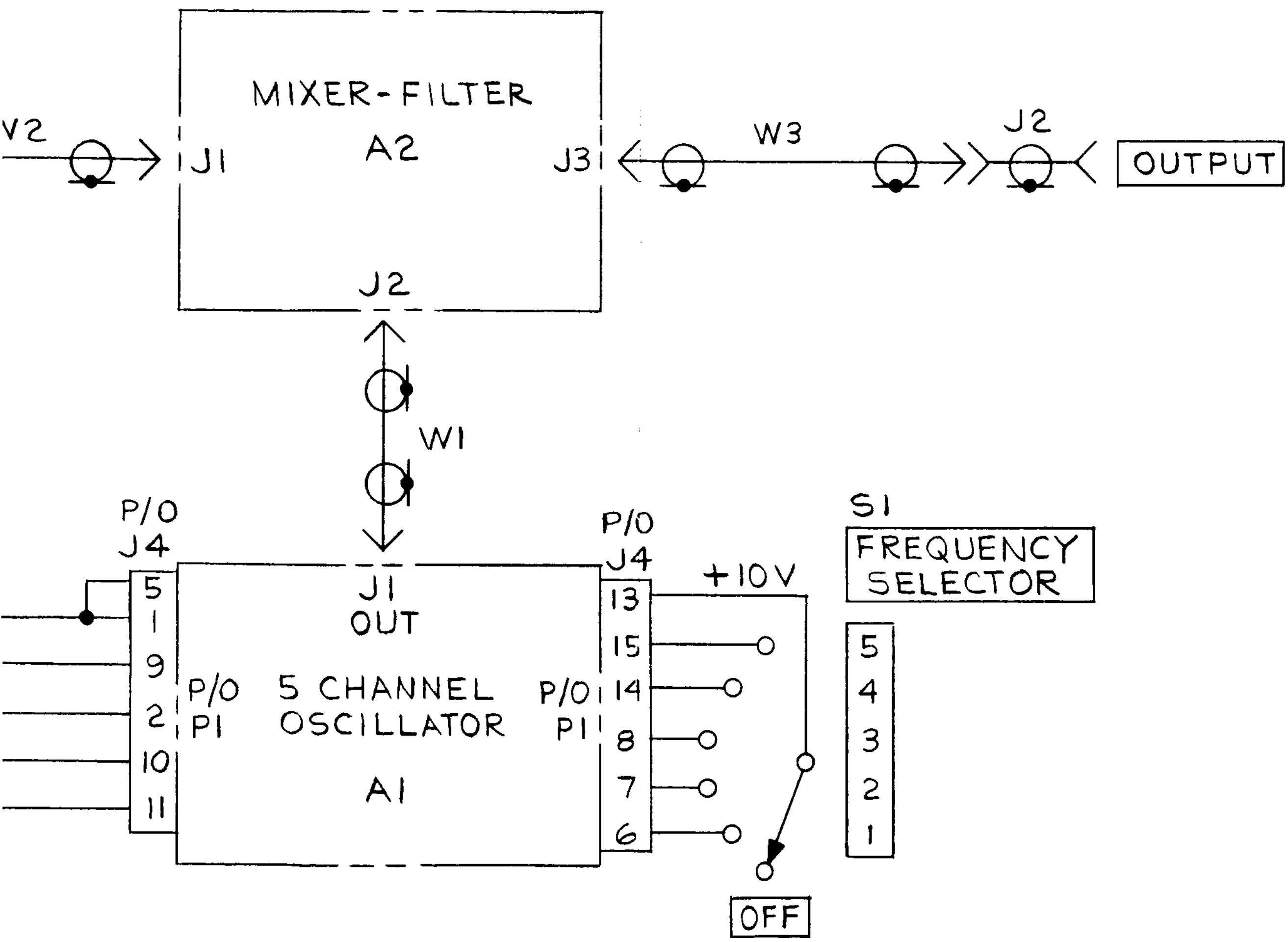


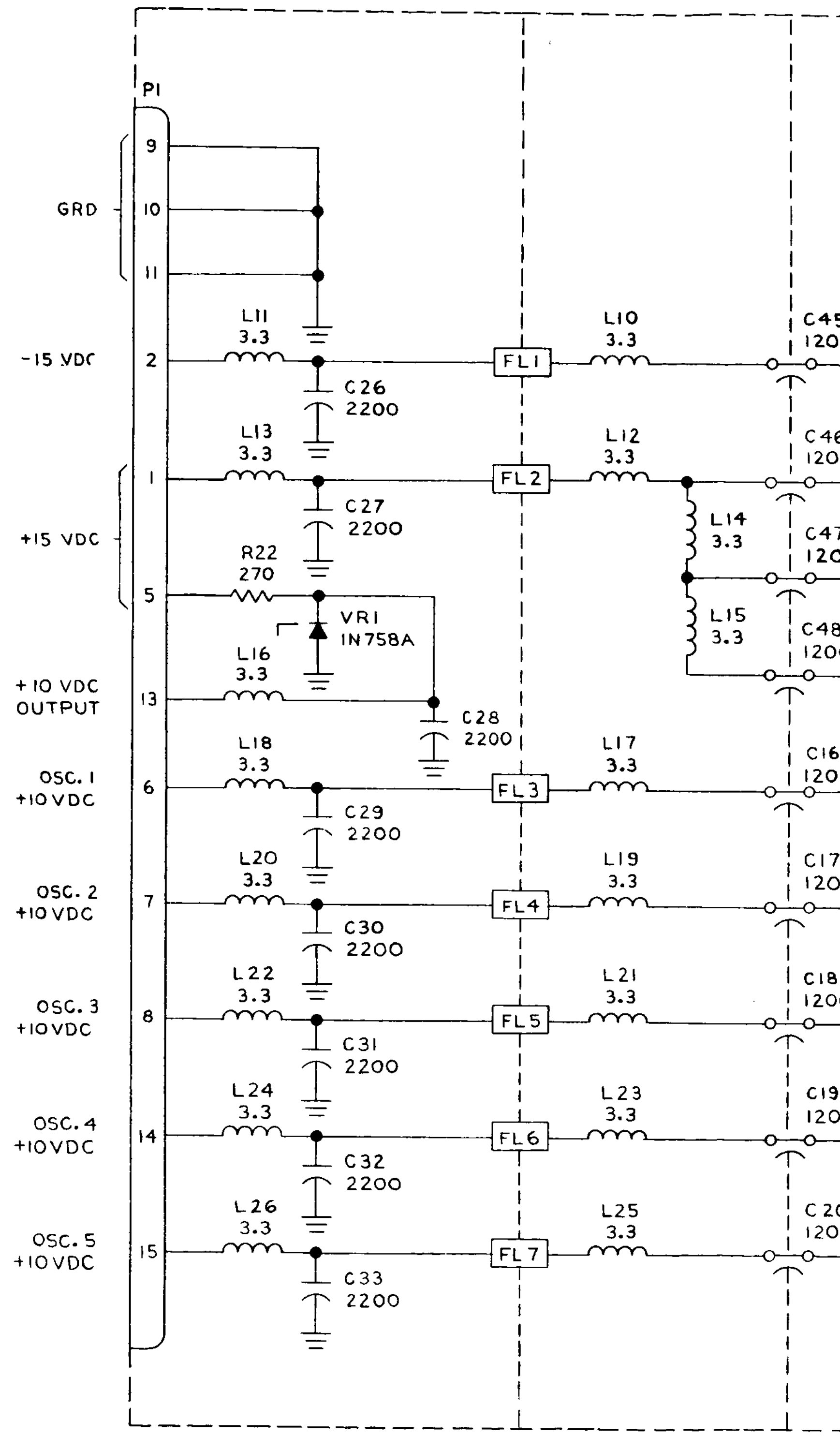
Figure 6-32. Frequency Converter (1A8), Schematic Diagram (63-25451E)

NO.

1. UNLESS OTHERWISE NOTED;
ALL RESISTORS ARE IN OHMS, ± 5 PCT, 1/4 WATT.
ALL CAPACITORS ARE IN UUF.
ALL INDUCTORS ARE IN UH.

2.

REFERENCE DESIGNATION	MODULE PART NO.	CRYSTAL FREQUENCY MC	CRYSTAL PART NO.
1A8A1 Y1	01-25277E01	45.42187	48-26403C23
1A8A1 Y2	01-25277E01	45.47319	48-26403C37
1A8A1 Y3	01-25277E01	45.48052	48-26403C38
1A8A1 Y4	01-25277E01	45.48785	48-26403C39
1A8A1 Y5	01-25277E01	45.49518	48-26403C40



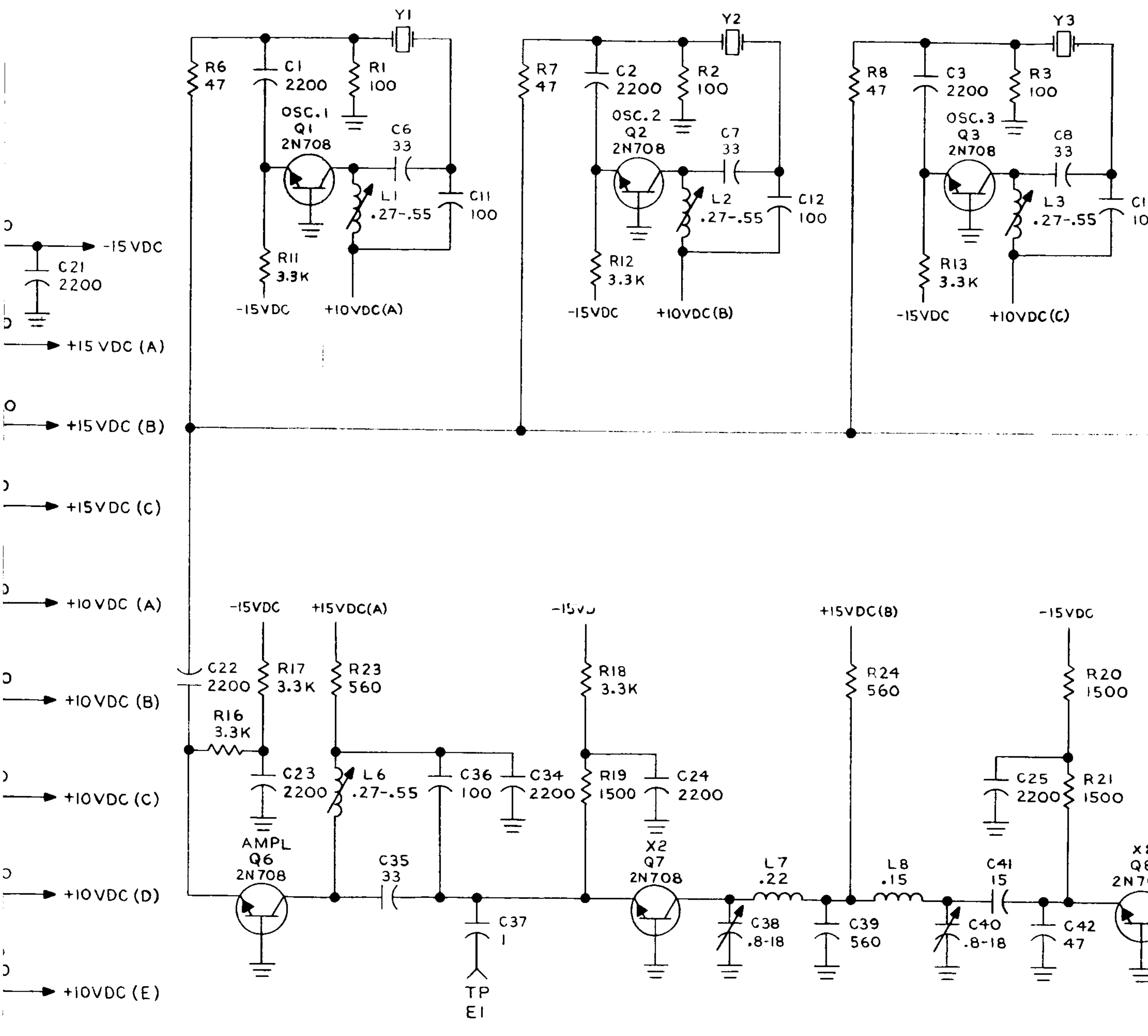
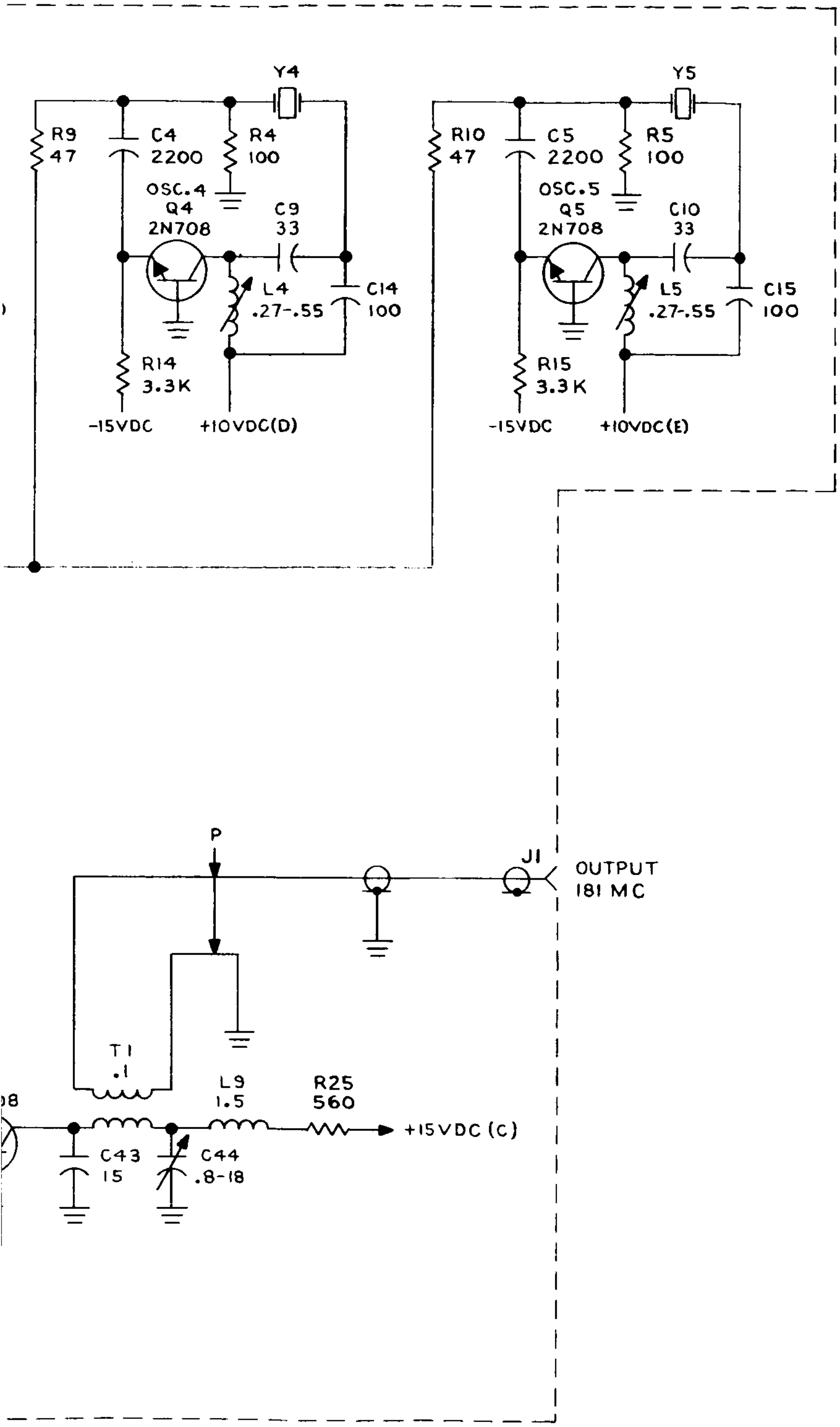


Figure 6-33 . 5-Cha

2



nel Oscillator (1A8A1), Schematic Diagram (63-25281E)

NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

   UNIT AND ASSEMBLY NO. 1A8A2

2. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE IN OHMS ±5 PCT, $\frac{1}{4}$ WATT.

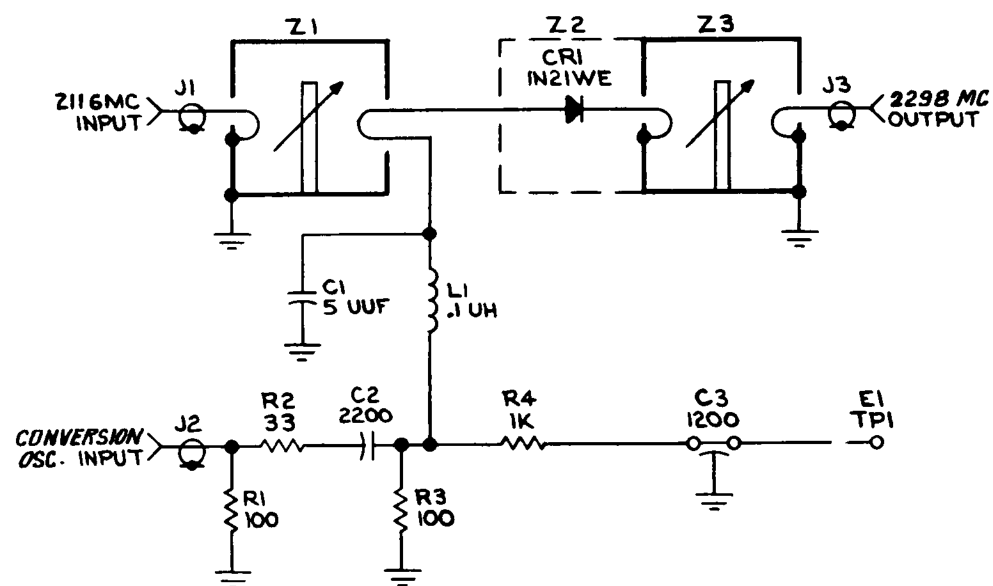
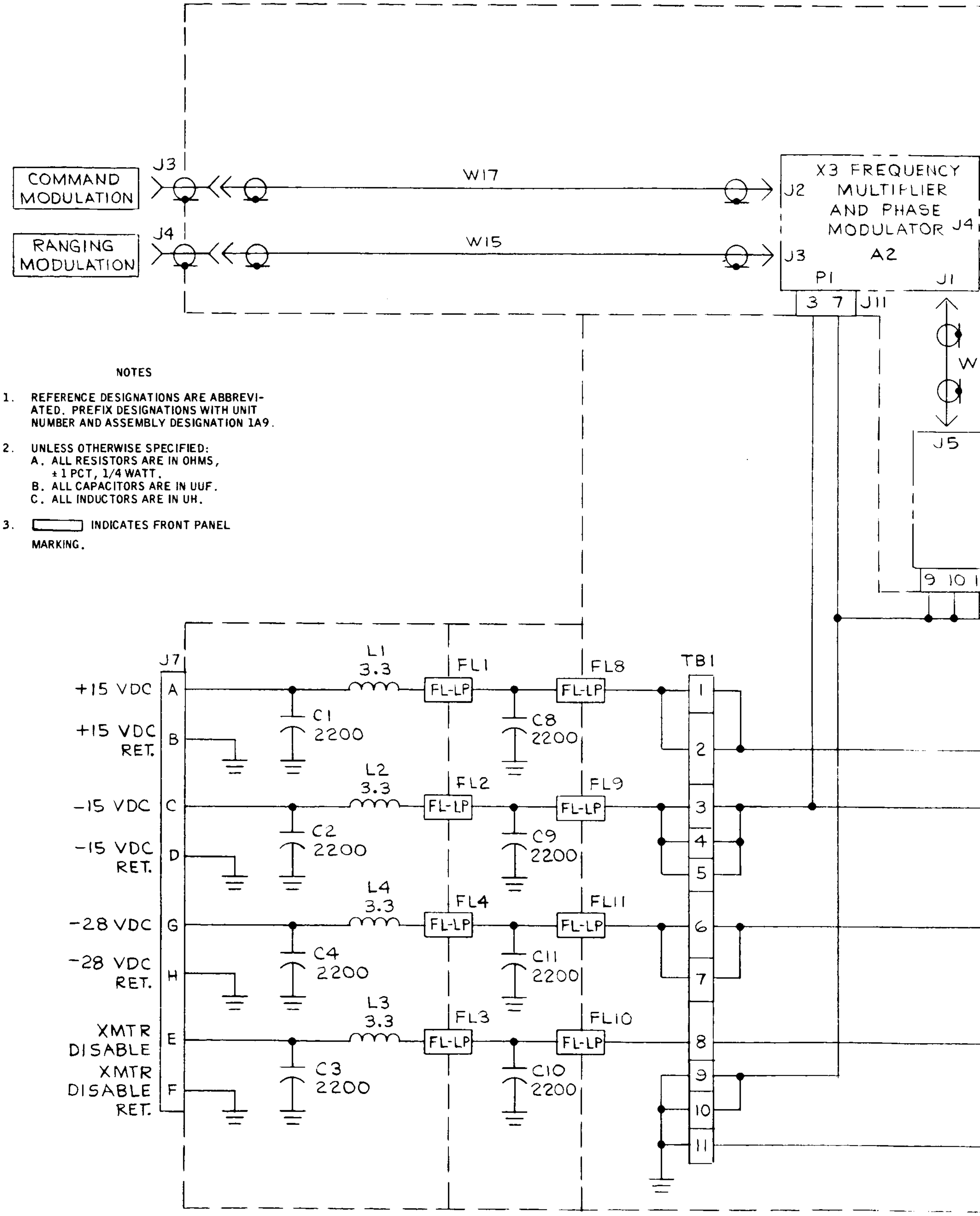


Figure 6-34. Mixer-Filter (1A8A2), Schematic Diagram (63-20348E)

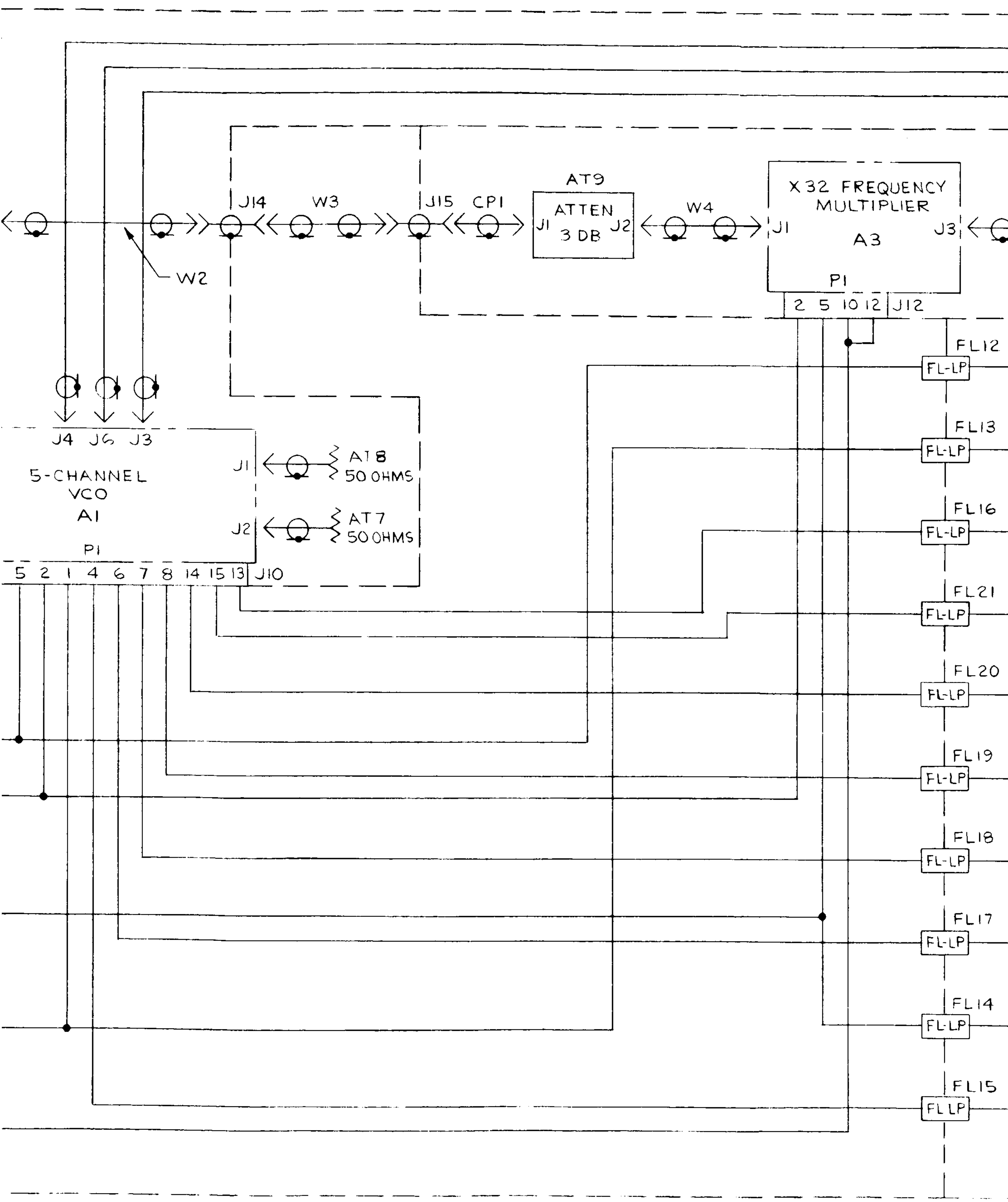


NOTES

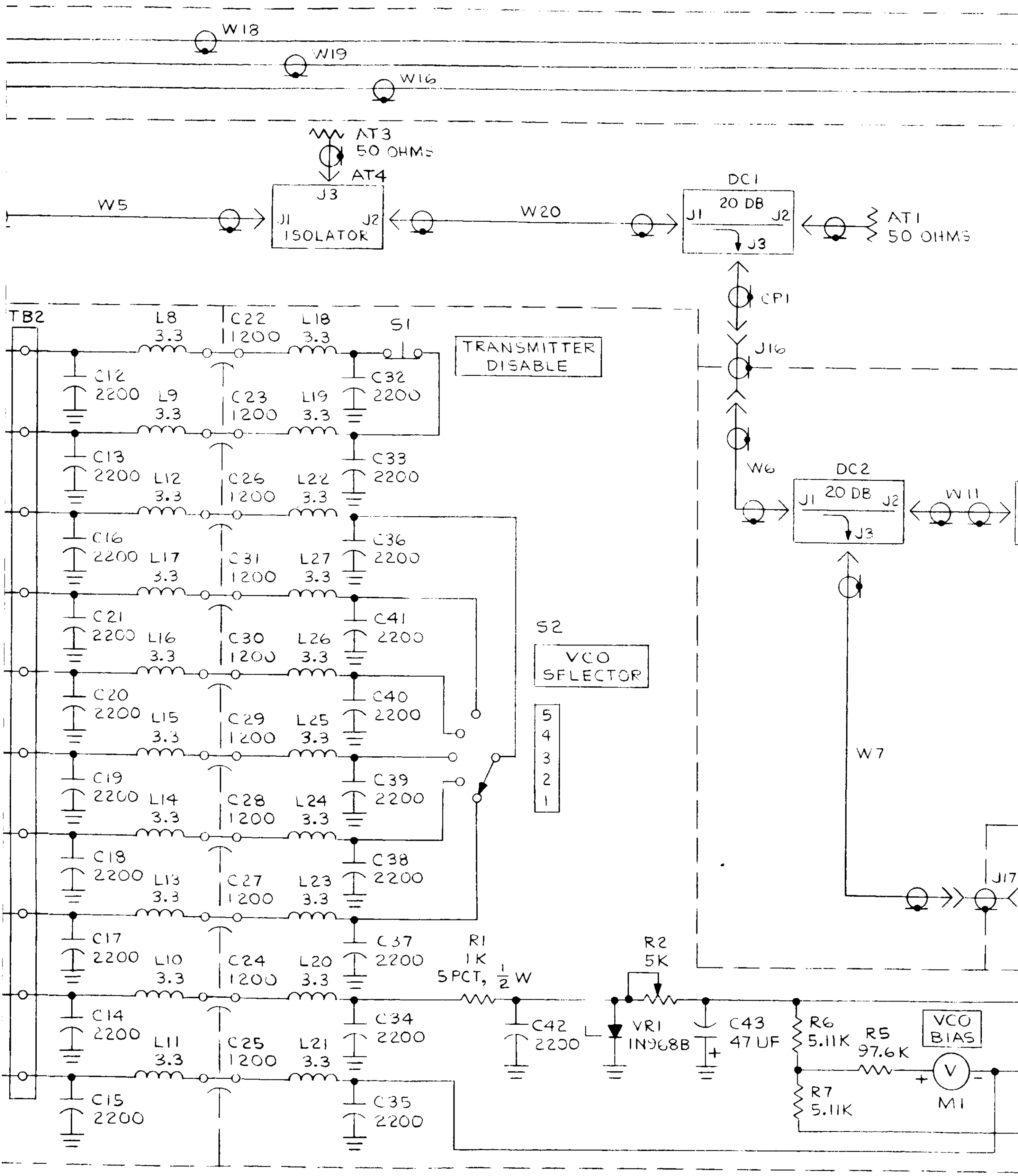
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION 1A9.

2. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS, ±1 PCT, 1/4 WATT.
   B. ALL CAPACITORS ARE IN UUF.
   C. ALL INDUCTORS ARE IN UH.

3. [box symbol] INDICATES FRONT PANEL MARKING.



W2
J14
W3
J15
CP1
AT9
ATTEN
3 DB
J1
J2
W4
X32 FREQUENCY
MULTIPLIER
A3
J1
J3
P1
2 5 10 12
J12
J4 J6 J3
5-CHANNEL
VCO
A1
J1
J2
AT8
50 OHMS
AT7
50 OHMS
P1
5 2 1 4 6 7 8 14 15 13
J10
FL12
FL13
FL16
FL21
FL20
FL19
FL18
FL17
FL14
FL15
FL-LP


W18
W19
W16
AT3
50 OHMS
AT4
J3
W5
J1
J2
ISOLATOR
W20
DC1
20 DB
J1
J2
J3
AT1
50 OHMS
CP1
J16
W6
DC2
20 DB
J1
J2
J3
W11
W7
J17
TB2
L8
3.3
C22
1200
L18
3.3
S1
TRANSMITTER
DISABLE
C12
2200
L9
3.3
C23
1200
L19
3.3
C32
2200
C13
2200
L12
3.3
C26
1200
L22
3.3
C33
2200
C16
2200
L17
3.3
C31
1200
L27
3.3
C36
2200
C21
2200
L16
3.3
C30
1200
L26
3.3
C41
2200
S2
VCO
SELECTOR
5
4
3
2
1
C20
2200
L15
3.3
C29
1200
L25
3.3
C40
2200
C19
2200
L14
3.3
C28
1200
L24
3.3
C39
2200
C18
2200
L13
3.3
C27
1200
L23
3.3
C38
2200
C17
2200
L10
3.3
C24
1200
L20
3.3
C37
2200
R1
1K
5 PCT, 1/2 W
R2
5K
C14
2200
L11
3.3
C25
1200
L21
3.3
C34
2200
C42
2200
VR1
1N968B
C43
47 UF
R6
5.11K
R5
97.6K
VCO
BIAS
V
M1
R7
5.11K
C15
2200
C35
2200

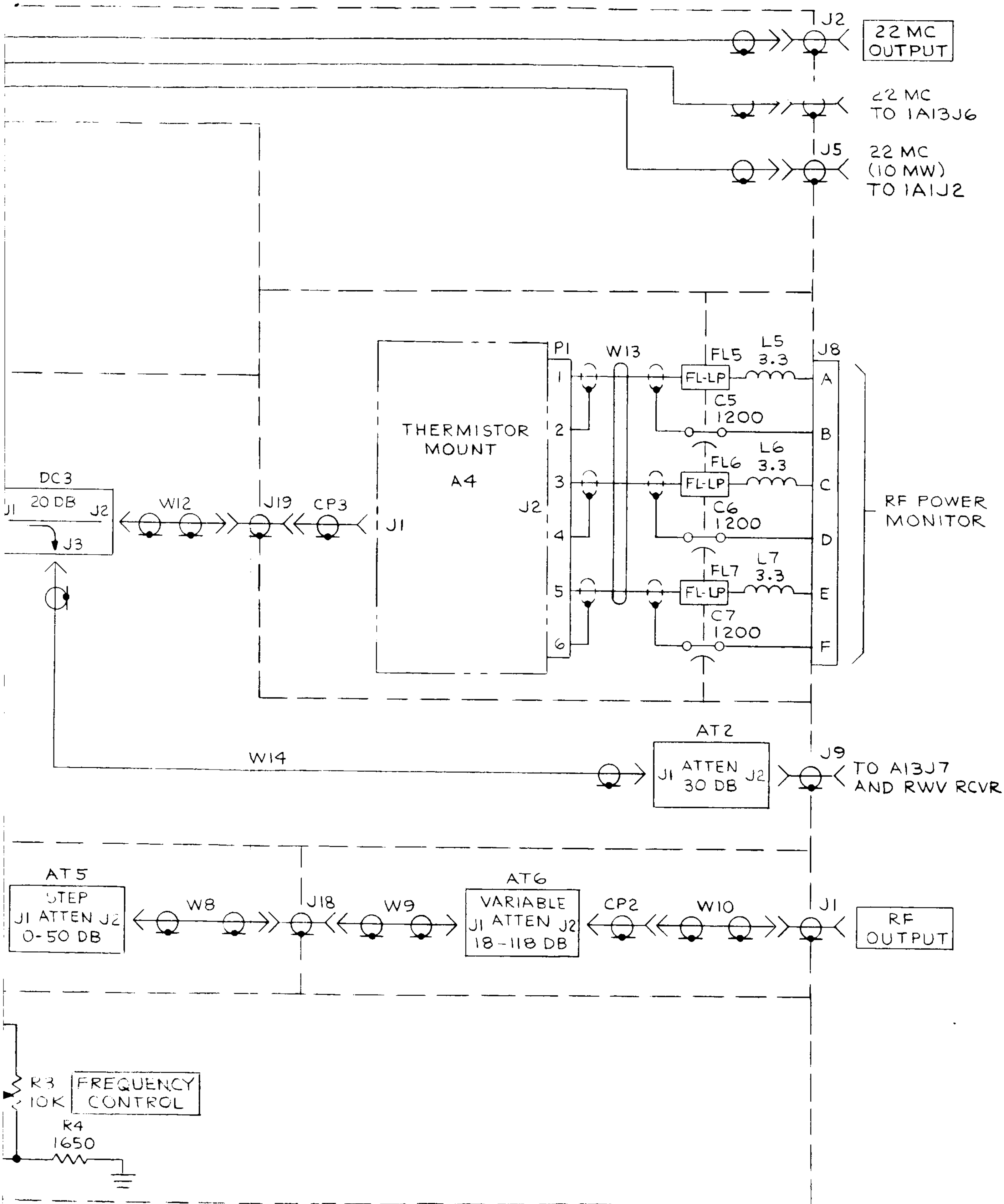


Figure 6-35. Test Transmitter (1A9), Schematic Diagram (63-25452E)

4. VALUE TO BE SELECTED IN TEST.

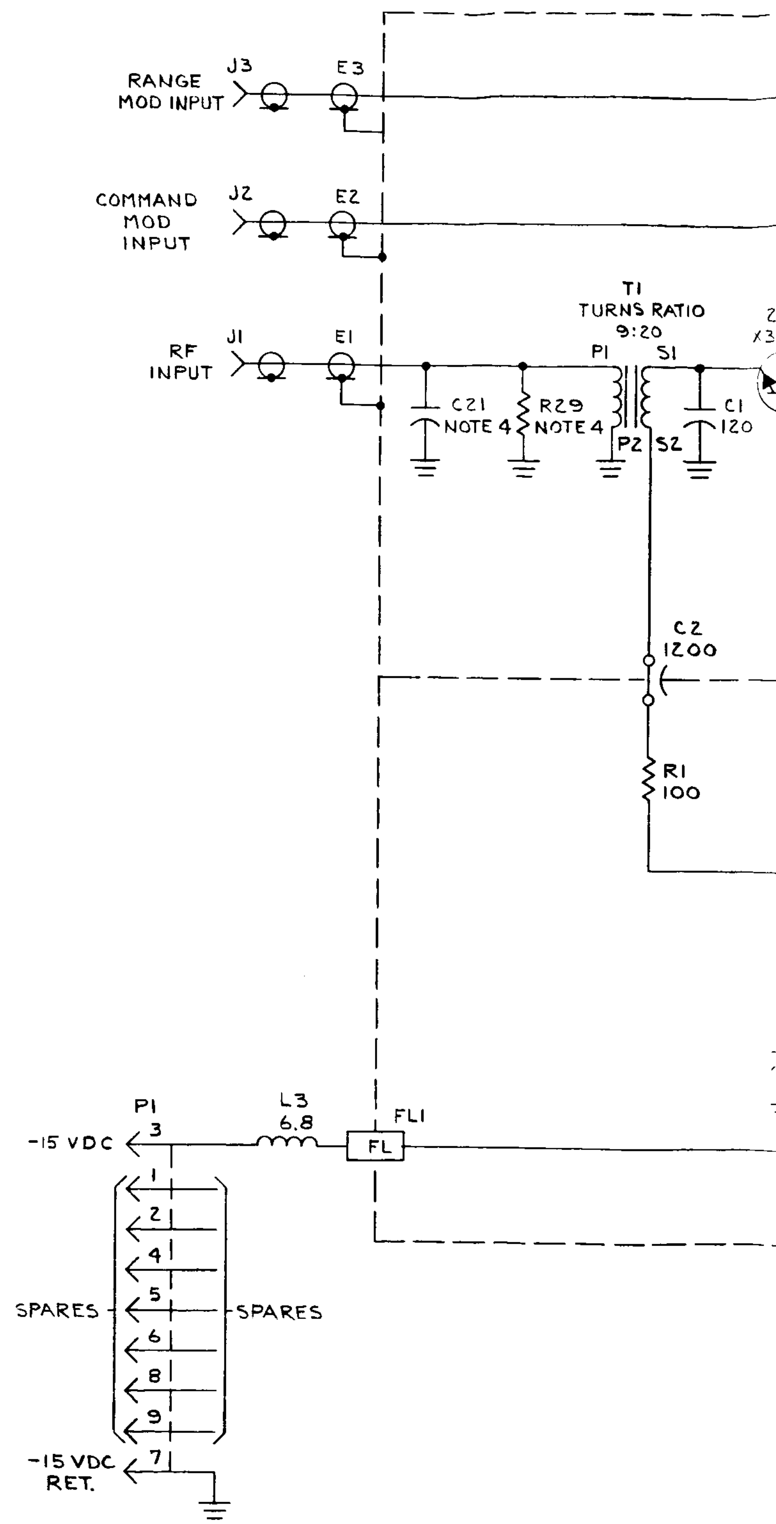
REFERENCE NO.	APPROXIMATE VALUE
R6	3000
R13	390
R29	120
R30	220
C21	120
C22	22
R7	560

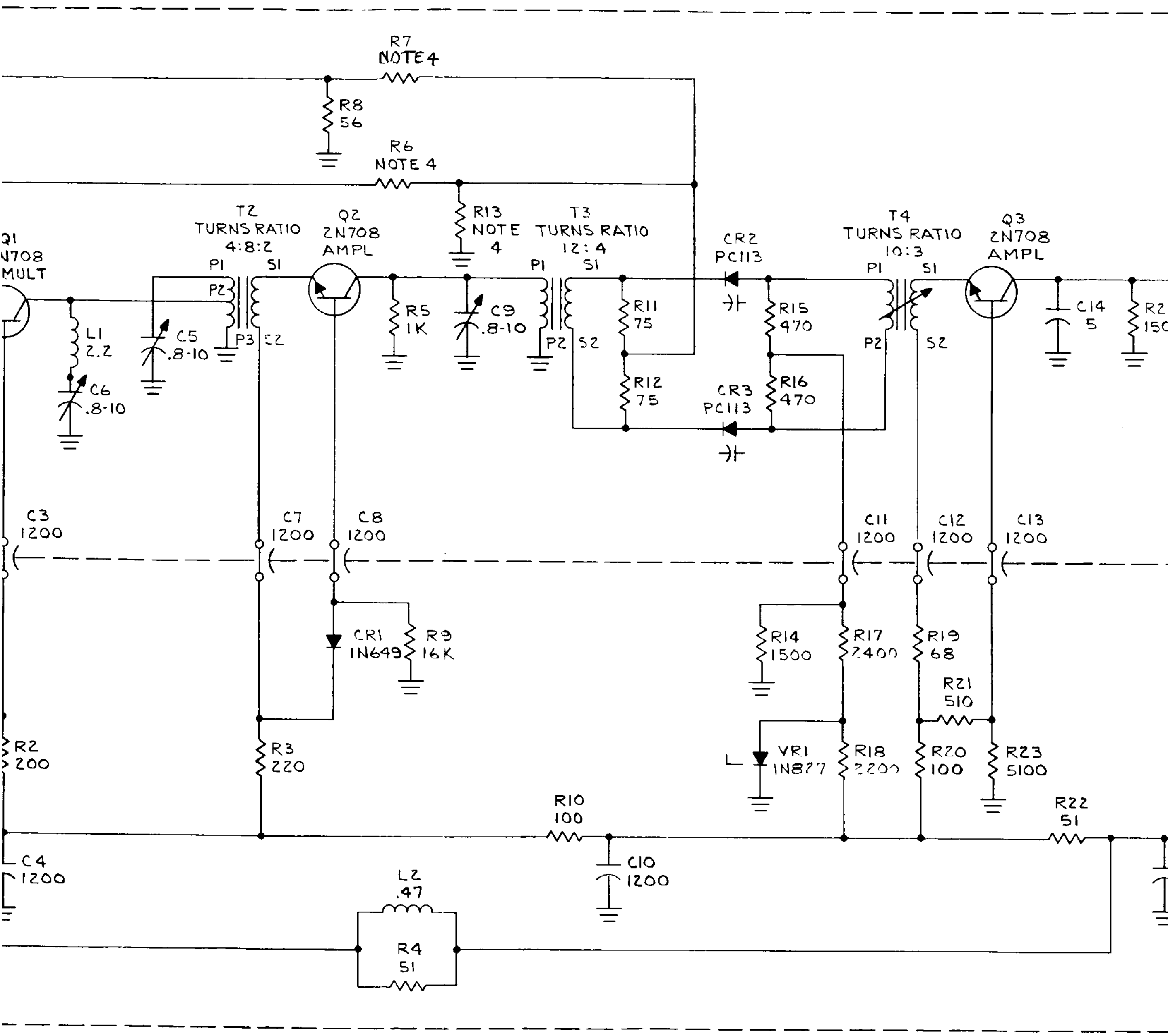
3. ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UUF.
   ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330515 (MOTOROLA NO. 01-23760D).

NOTES: UNLESS OTHERWISE SPECIFIED





R7
NOTE 4
R8
56
R6
NOTE 4
Q1
N708
MULT
T2
TURNS RATIO
4:8:2
P1
S1
P2
P3
S2
Q2
2N708
AMPL
R13
NOTE
4
T3
TURNS RATIO
12:4
P1
S1
P2
S2
CR2
PC113
T4
TURNS RATIO
10:3
P1
S1
P2
S2
Q3
2N708
AMPL
L1
2.2
C6
.8-10
C5
.8-10
R5
1K
C9
.8-10
R11
75
R12
75
R15
470
R16
470
CR3
PC113
C14
5
C3
1200
C7
1200
C8
1200
C11
1200
C12
1200
C13
1200
CR1
1N649
R9
16K
R14
1500
R17
2400
R19
68
R21
510
R2
200
R3
220
VR1
1N827
R18
2200
R20
100
R23
5100
R10
100
R22
51
C4
1200
C10
1200
L2
.47
R4
51

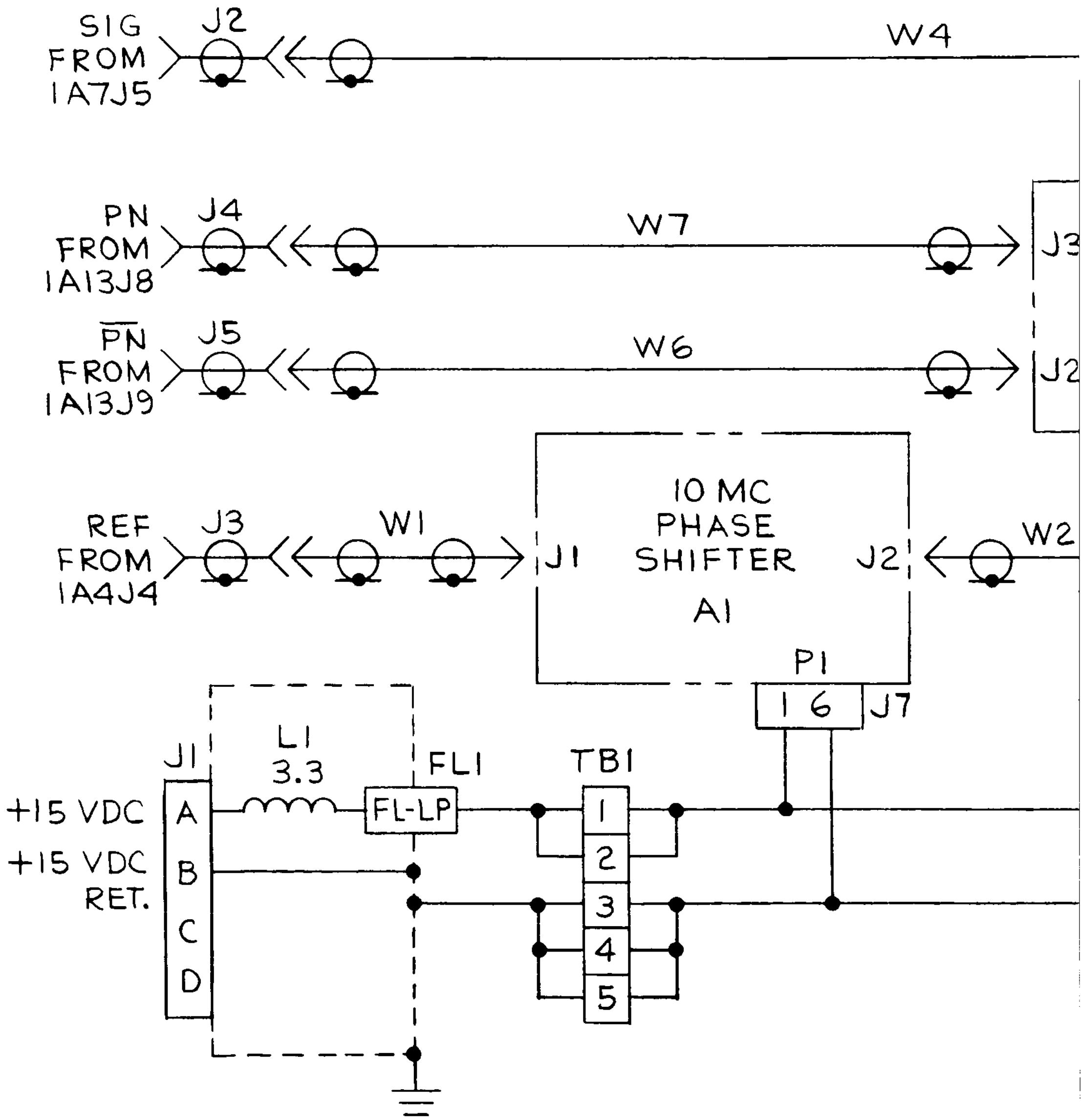
Figure 6-

2

NOTES

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION 1A10.

2. UNLESS OTHERWISE SPECIFIED
   A. ALL INDUCTORS ARE IN UH.



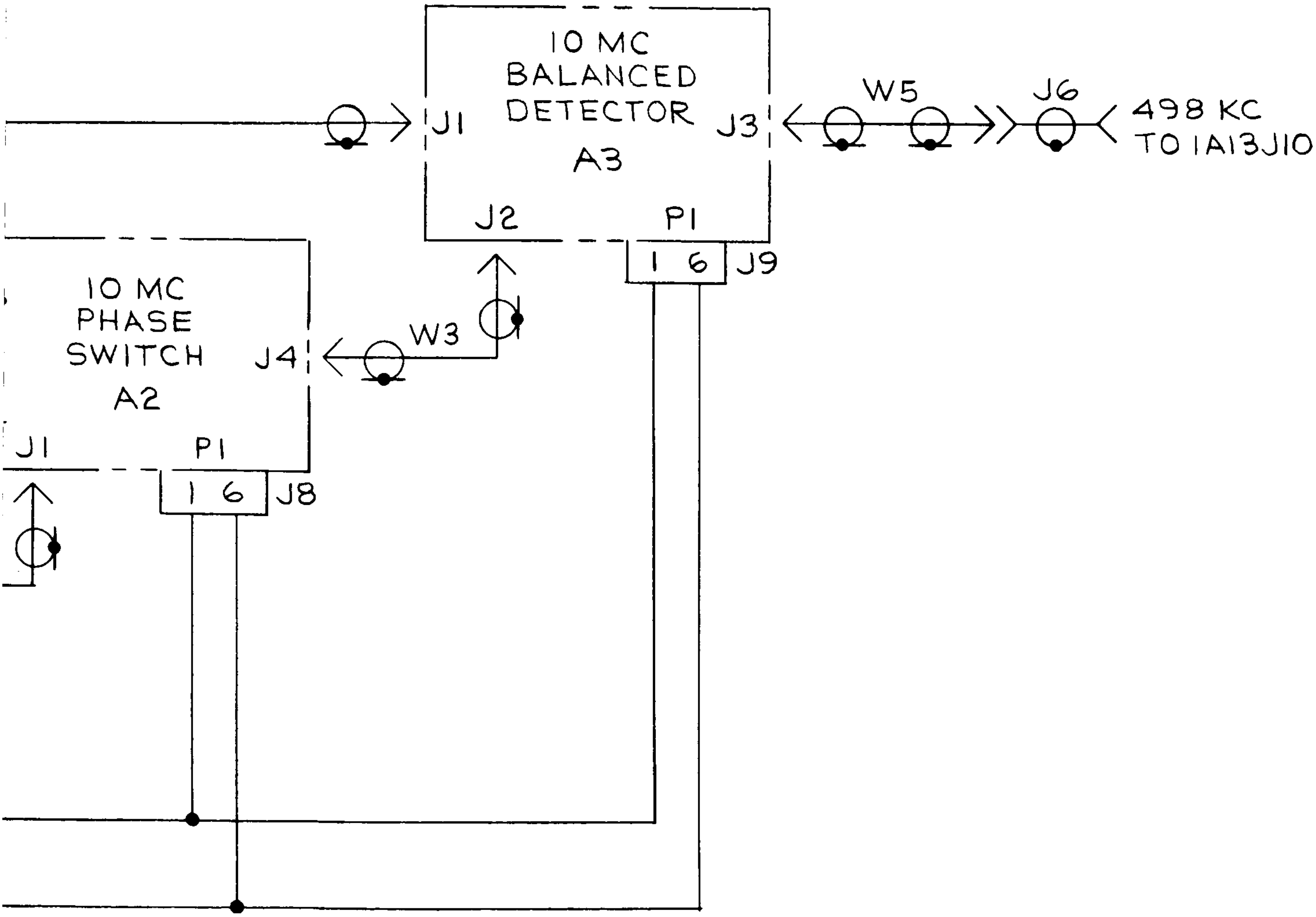
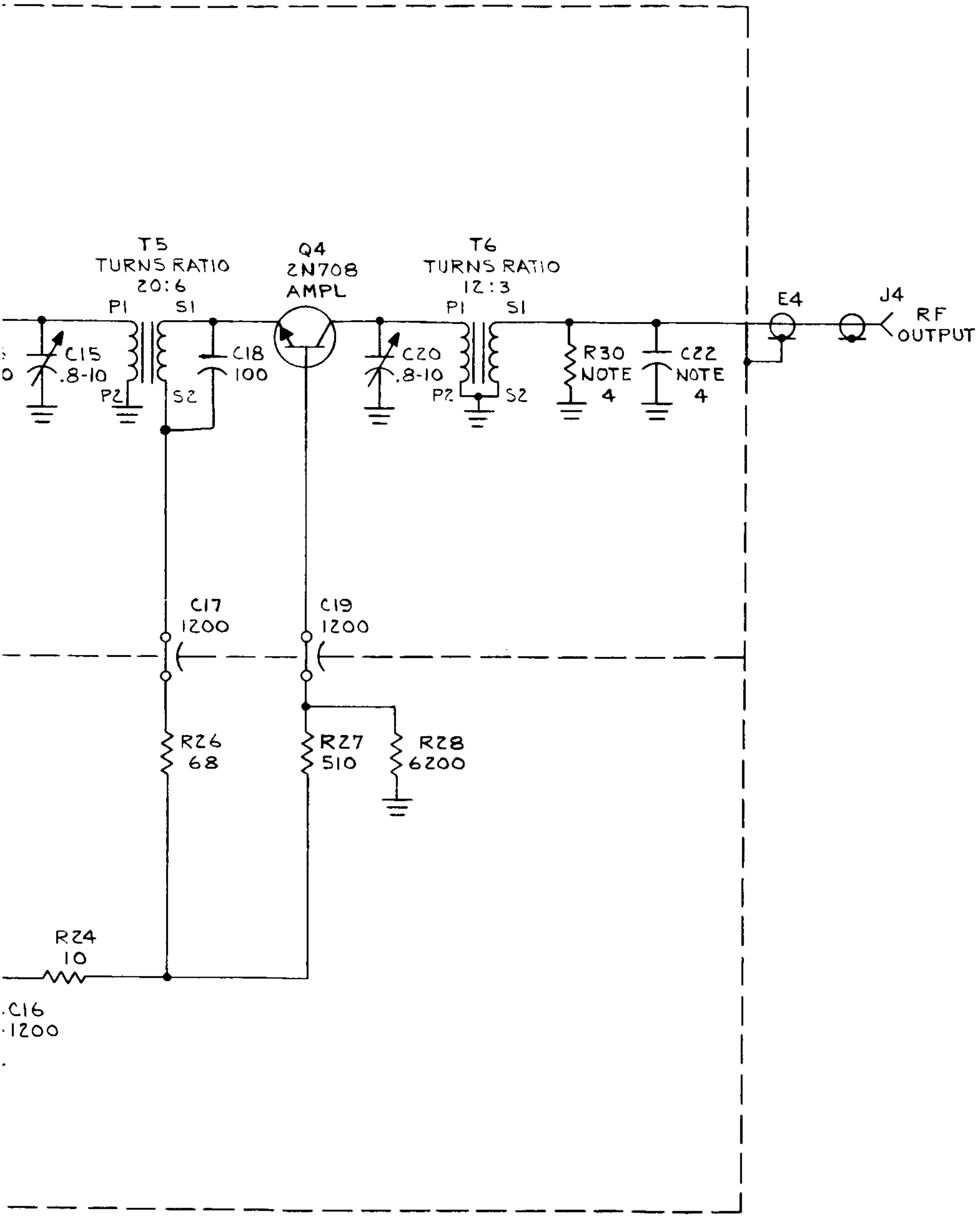


Figure 6-37. Ranging Conversion Unit (1A10), Schematic Diagram (63-25453E)



36. X3 Multiplier and Phase Modulator (1A9A2), Schematic Diagram (63-23862D)

4. VALUE TO BE SELECTED IN TEST.

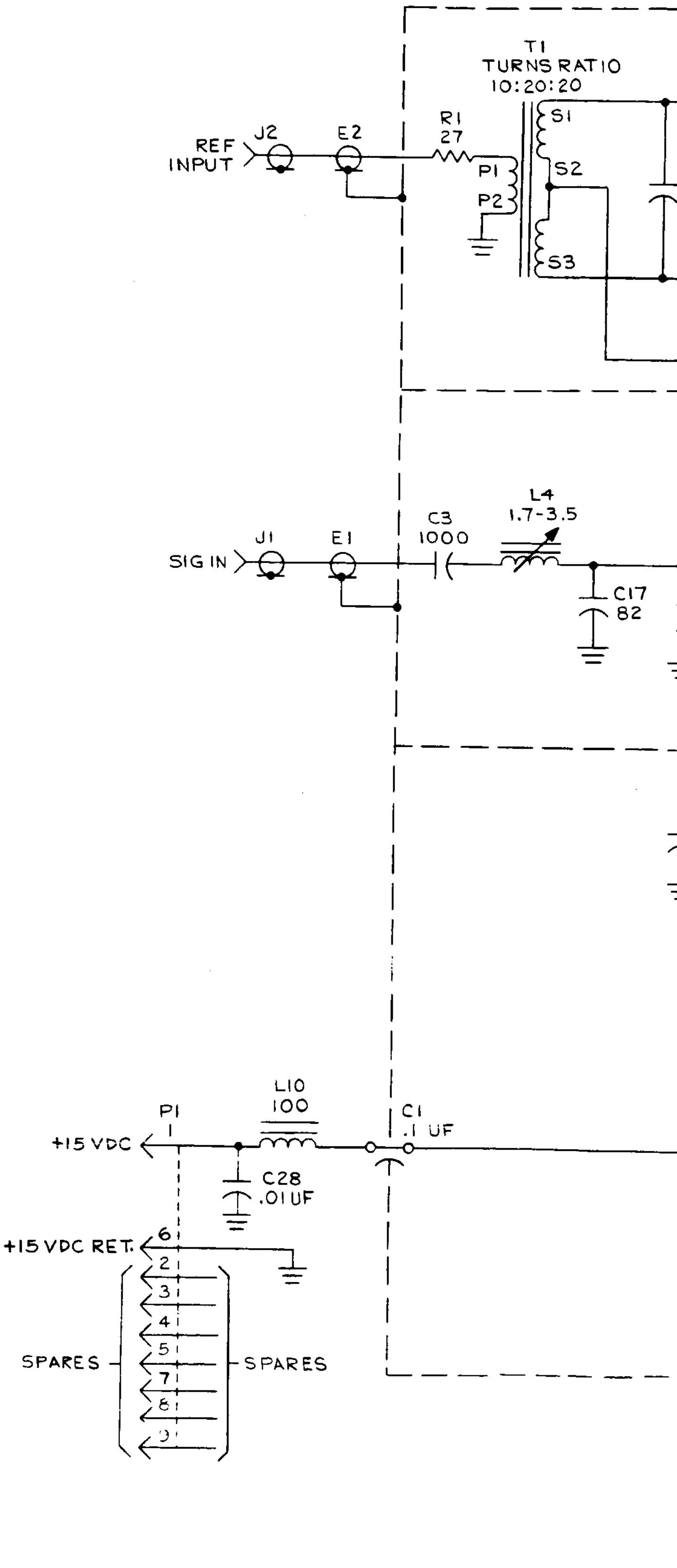
REFERENCE NO.	APPROXIMATE VALUE
R25	47

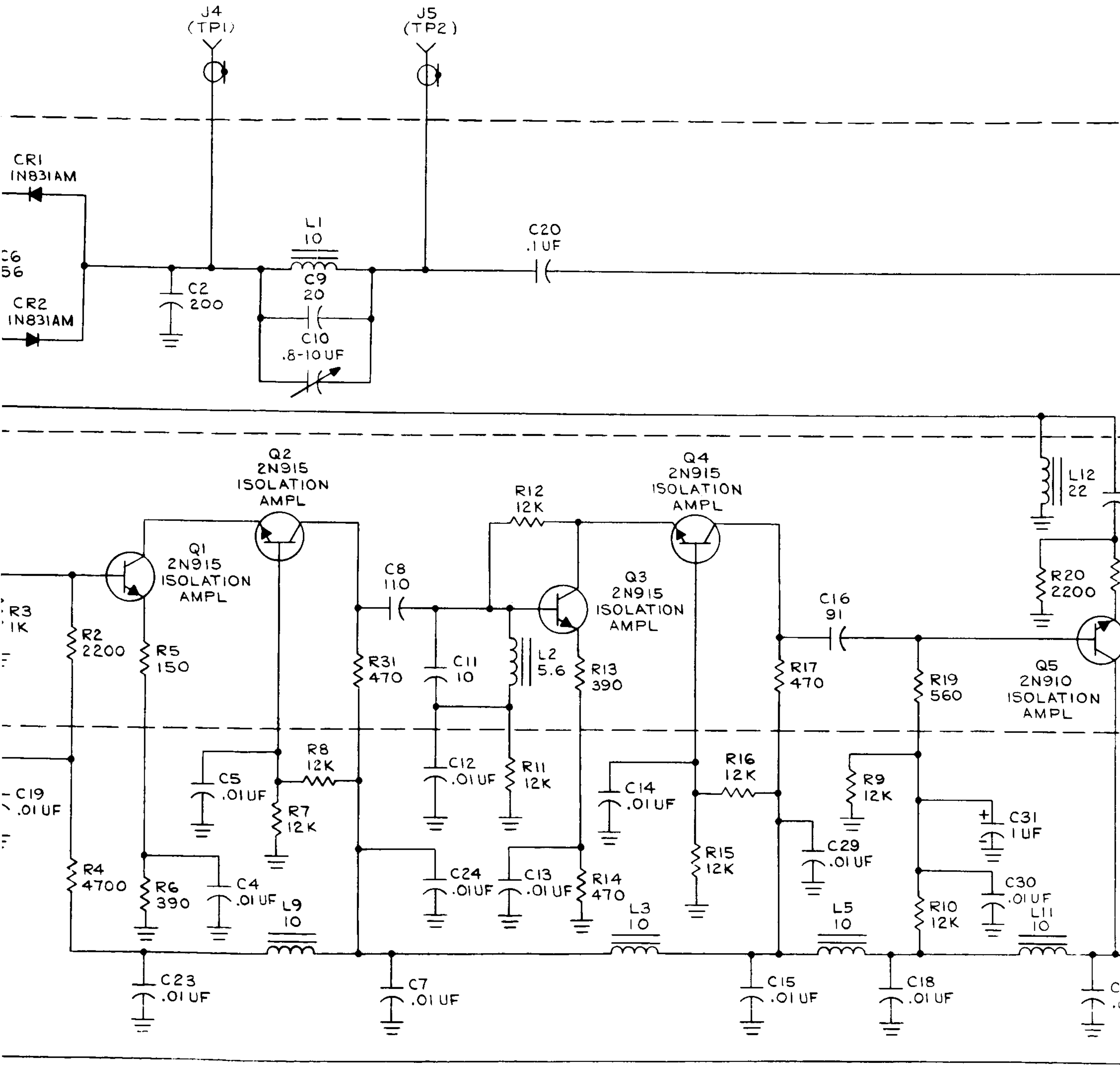
3. ALL RESISTORS ARE IN OHMS ± 5 PCT, 1/4 WATT.
ALL CAPACITORS ARE IN UUF.
ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER AND ASSEMBLY DESIGNATION.

1. FOR ASSEMBLY SEE DRAWING D9330539 (MOTOROLA NO. 01-23845D).

NOTES: UNLESS OTHERWISE SPECIFIED





J4 (TP1)
J5 (TP2)
CR1 1N831AM
CR2 1N831AM
C2 200
L1 10
C9 20
C10 .8-10 UF
C20 .1 UF
Q1 2N915 ISOLATION AMPL
Q2 2N915 ISOLATION AMPL
Q3 2N915 ISOLATION AMPL
Q4 2N915 ISOLATION AMPL
Q5 2N910 ISOLATION AMPL
R2 2200
R3 1K
R4 4700
R5 150
R6 390
R7 12K
R8 12K
R9 12K
R10 12K
R11 12K
R12 12K
R13 390
R14 470
R15 12K
R16 12K
R17 470
R19 560
R20 2200
R31 470
C4 .01 UF
C5 .01 UF
C7 .01 UF
C8 110
C11 10
C12 .01 UF
C13 .01 UF
C14 .01 UF
C15 .01 UF
C16 91
C18 .01 UF
C19 .01 UF
C23 .01 UF
C24 .01 UF
C29 .01 UF
C30 .01 UF
C31 1 UF
L2 5.6
L3 10
L5 10
L9 10
L11 10
L12 22

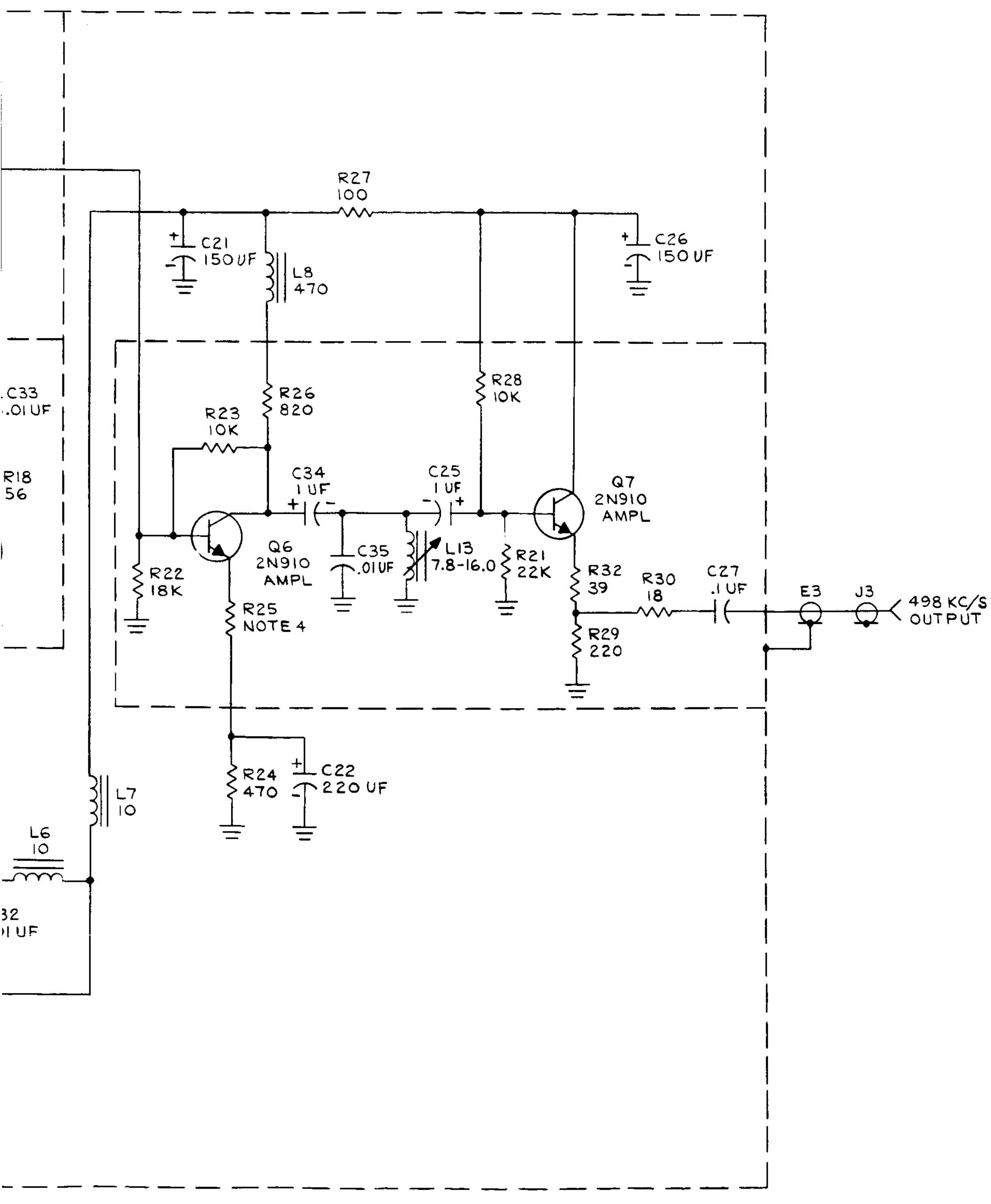
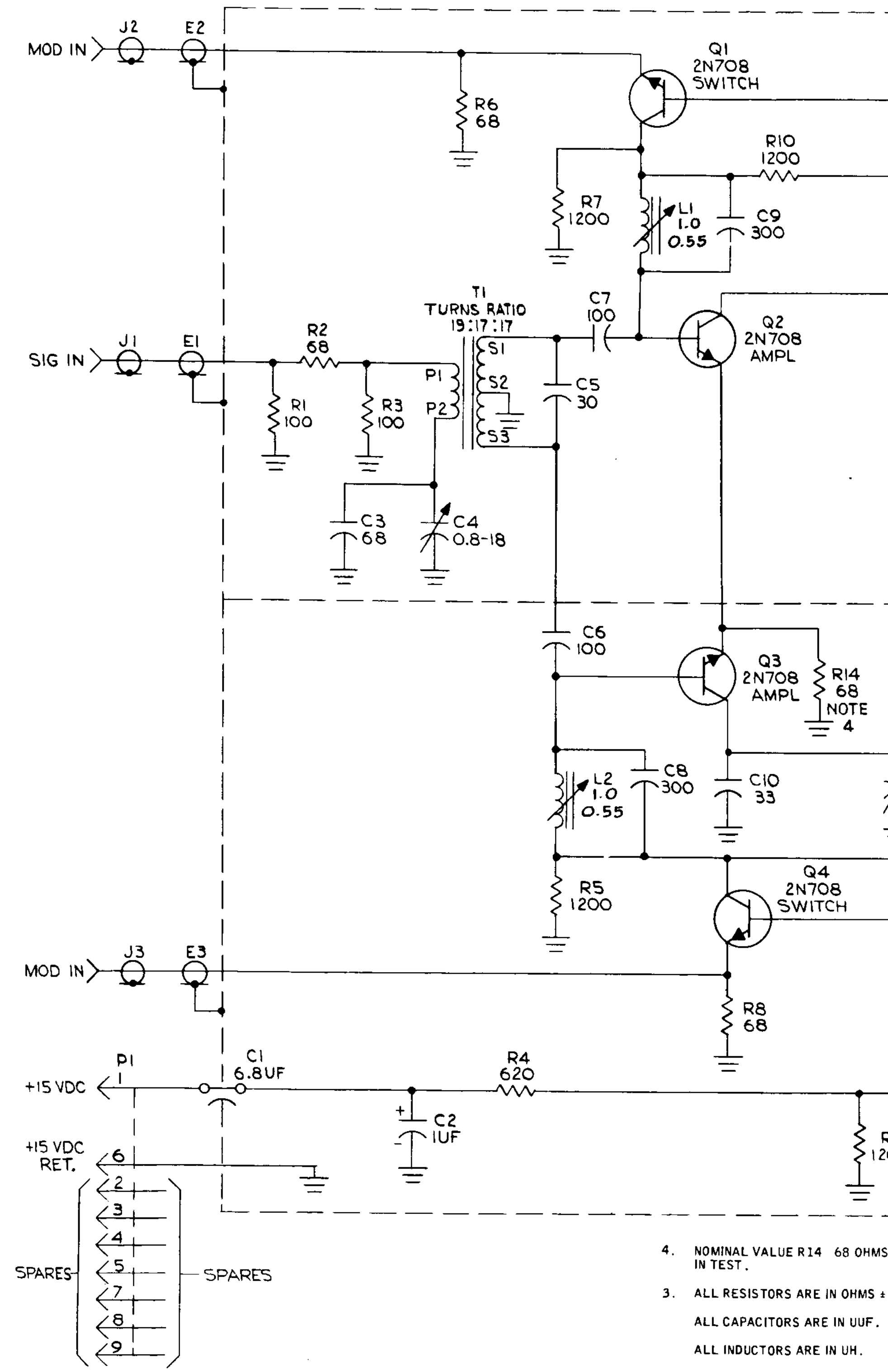


Figure 6-39. 10 MC Balanced Detector (1A10A3), Schematic Diagram (63-23897D)



4. NOMINAL VALUE R14 68 OHMS
IN TEST.

3. ALL RESISTORS ARE IN OHMS ±

ALL CAPACITORS ARE IN UUF.

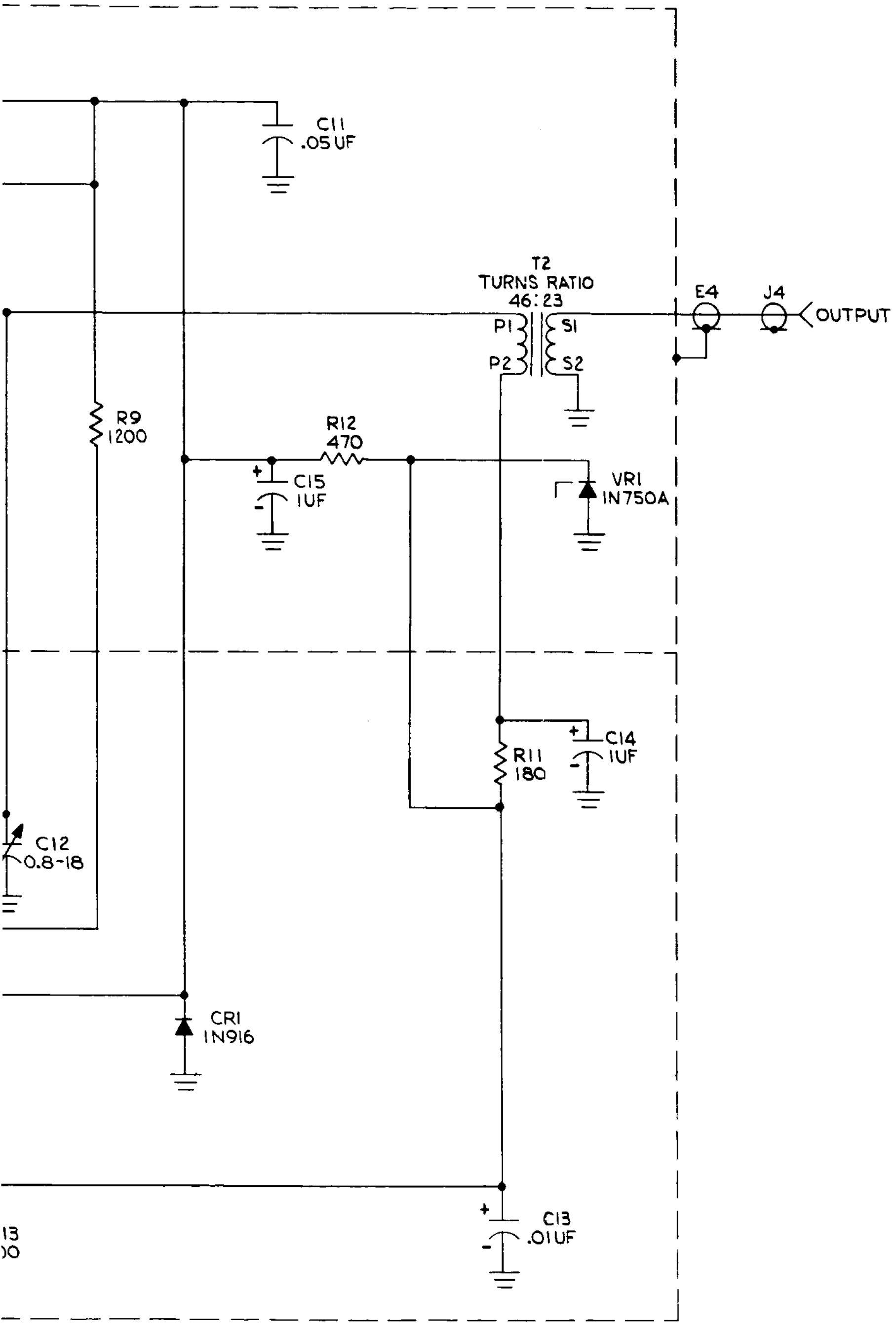
ALL INDUCTORS ARE IN UH.

2. REFERENCE DESIGNATIONS ARE
DESIGNATIONS WITH UNIT NO. A

1. FOR ASSEMBLY SEE DRAWING D
(MOTOROLA NO. 01-23840D).

NOTES: UNLESS OTHER

Figure 6-38. 10



, TRUE VALUE TO BE SELECTED

5 PCT, 1/4 WATT.

ABBREVIATED. PREFIX THE
ND ASSEMBLY DESIGNATION.

9330534

WISE SPECIFIED

MC Phase Switch (1A10A2), Schematic Diagram (63-23895D)