
NASA CONTRACTOR REPORT

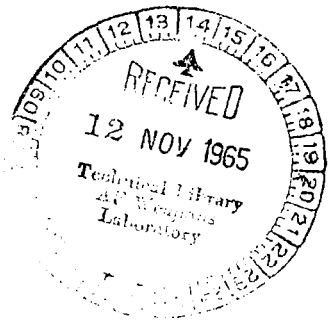

NASA-CR-3

NASA CR-323



# A PHASE LOCKED DUAL CHANNEL SPACECRAFT RECEIVER FOR PHASE AND GROUP PATH MEASUREMENTS

*by R. L. Koehler*




Prepared under Contract No. NAS 2-1759 and Grant No. NsG-329 *by*
STANFORD ELECTRONICS LABORATORIES
Stanford, Calif.
*for*

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • NOVEMBER 1965

# A PHASE LOCKED DUAL CHANNEL SPACECRAFT RECEIVER FOR PHASE AND GROUP PATH MEASUREMENTS

By R. L. Koehler



Prepared under Contract No. NAS 2-1759 and Grant No. NsG-329 by
STANFORD ELECTRONICS LABORATORIES
Stanford, Calif.

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

For sale by the Clearinghouse for Federal Scientific and Technical Information
Springfield, Virginia 22151 – Price $5.00

## ABSTRACT

This report describes a 49.8 and 423.3 Mc phase locked receiver for group and phase path measurement aboard the Pioneer interplanetary spacecraft. A magnetometer aboard the spacecraft imposes a stringent low residual magnetic field requirement on the equipment. The receiver's magnetic field is only 1 gamma ($10^{-5}$ gauss) at 3 feet after exposure to a 25 oersted magnetizing field.

The experiment uses two high power ground based transmitters and a 150 foot parabolic antenna to transmit phase modulated signals to the receiver. Group and phase path measurements will be made as the spacecraft travels to 0.5 AU ($7.5 \times 10^{10}$ m) from earth, and the results telemetered back to earth.

The minimum measureable increment of phase path is 1 wavelength of 49.8 Mc, corresponding to an integrated electron density of $3.75 \times 10^{14}$ electrons/$m^2$ or a volume density of $5 \times 10^3$ electrons/$m^3$ at 0.5 AU. The error in group path is 2 percent of a wavelength of the 8.692 kc modulation frequency, corresponding to an integrated electron density of $4 \times 10^{16}$ electrons/$m^2$ or a volume density of $6 \times 10^5$ electrons/$m^3$ at 0.5 AU.

The receiver will maintain phase lock for 10 hours before skipping a cycle in the 49.8 Mc channel at -130 dbm with 8000°K cosmic noise, and in the 423.3 Mc channel at -137 dbm with 100°K cosmic noise. These levels include the modulation sidebands which use 0.5 of the total signal power. The 49.8 Mc channel has a 3 db noise figure and the 423.3 Mc channel has a 6 to 7 db noise figure; the IF noise bandwidth is 45 kc. It weighs 5.0 lbs without antennas and uses less than 1.5 w power.

This report discusses the receiver performance and a detailed block diagram, followed by schematics with a description of their operation. Reasons for some of the design decisions are included, as well as a discussion of the areas for improvement. The calculated and measured phase lock loop performance are compared. Low residual magnetism construction techniques and other construction details are included.

TABLE OF CONTENTS

LIST OF FIGURES

APPENDIX FIGURES

## LIST OF TABLES

## ACKNOWLEDGMENT

Work on the Stanford/Pioneer receiver was supported by the National Aeronautics and Space Administration. The initial design phase was supported by grant NsG 329. The final design phase and construction of flight equipment was supported by contract NAS 2-1759.

The overall receiver was designed and constructed at Stanford Research Institute (SRI), and the radio frequency modules were designed and constructed at TRW Space Technology Laboratories (STL).

Special thanks go to Roy Long, who headed the project at SRI and capably guided it through many problems, and to Lyle Nelson, who very ably and conscientiously supervised the partial redesign and construction of the radio frequency modules at STL.

Designers of various portions of the receiver at SRI deserve special mention: John Yarborough, Jim Woodbury, Hank Olsen, and Boyd Fair. Bruce Clark supervised the reliability program, and Vel Sanford and Ed Spitzer were responsible for the mechanical design.

At Stanford University, thanks to Professor Owen K. Garriott, who started the development project, Professor Von R. Eshleman, who assumed role as principal investigator for the flight on the Pioneer Spacecraft, and Professor Allen M. Peterson, who helped solve some of the knotty administrative problems and also started me on this project.

I greatly appreciate the work of many people on the receiver throughout the past year. I express gratitude to the many others for their support on problems concerning the overall Pioneer project, such as the spacecraft antenna, the ground antenna and transmitters, trajectories, and the NASA-SU interface.

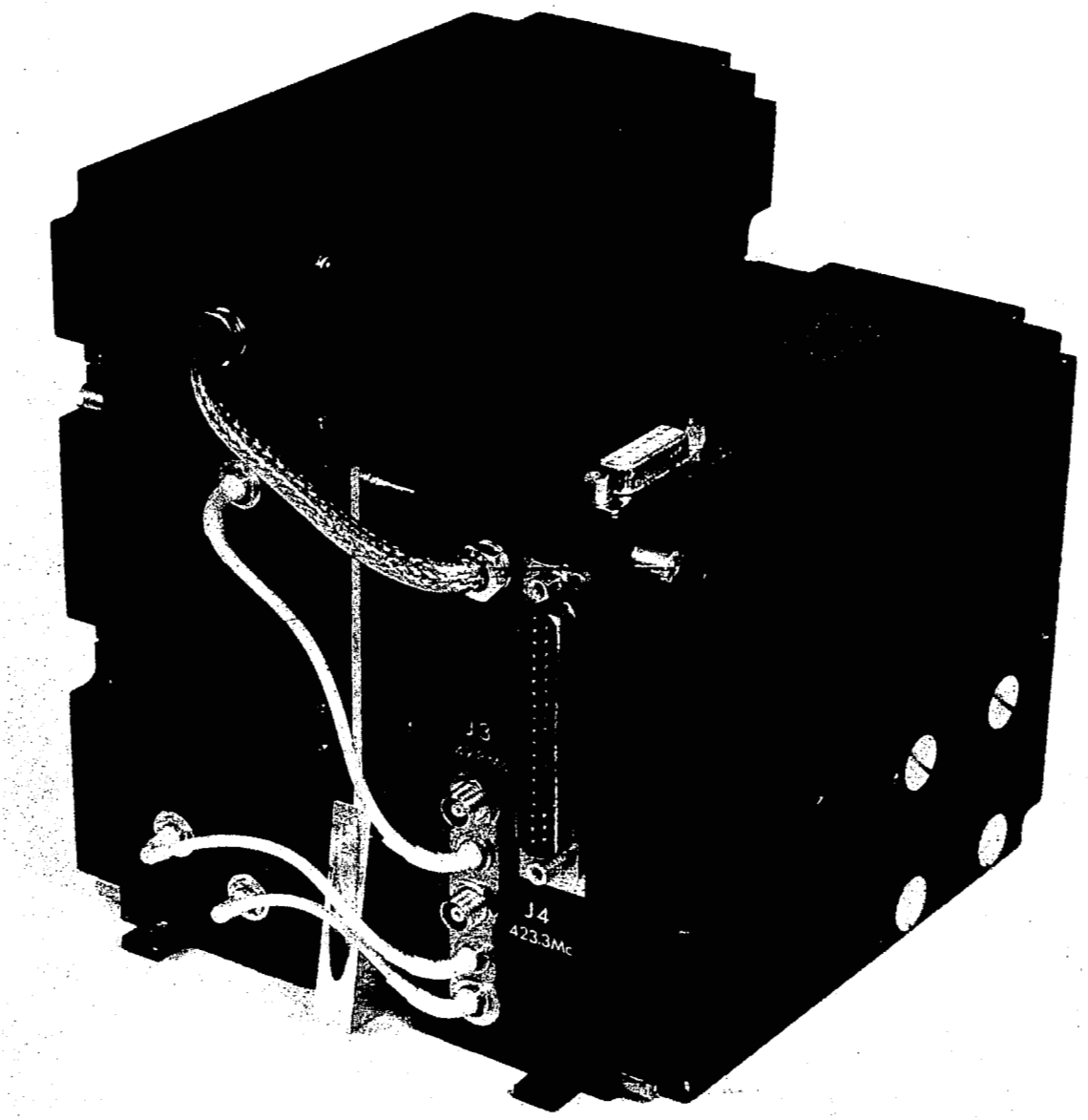



Figure 1.1 - The Dual Channel Stanford/Pioneer Receiver

# I. INTRODUCTION

This report describes the design and construction of a receiver intended for operation as a part of a space probe experiment. The experiment involves the transmission of two modulated, coherent carriers from the ground (at approximately 50 Mc and 425 Mc) and the reception of these signals by the receiver in a space probe. From the relative phase of the received carriers and their sidebands, it is possible to deduce the integrated electron density between the earth and the space probe. This is the major purpose of the experiment.

It can be shown that the phase of a radio wave in passing through an ionized medium, will be advanced by an amount in meters $\Delta P = (40.3/f^2) \int N\, ds$, where $f$ is the wave frequency and the electron density $N$ is integrated along the ray path. It is also true that a wave packet (which may be described by the peak of a modulation envelope) is delayed by the same amount, $\Delta P$ meters. The space probe receiver has been designed to measure the relative phase of the modulation envelopes on the two carrier frequencies and, since the higher frequency is relatively unaffected by the presence of the ionization, this will provide a value for the integrated electron density. In addition, the rate of change of phase of one carrier with respect to the other will be measured, thus very accurately determining the rate change of integrated electron density. The measurements will be transmitted back to earth by the space probe telemetry system.

In the following sections, the specifications and system parameters to which the receiver has been designed will be given. This is followed by a discussion of the entire system and a more detailed description of the individual unit operation. The report concludes with a discussion of possible areas for improvement in future receivers.

## 2. SYSTEM PARAMETERS AND PERFORMANCE

While several system parameters such as weight, size, and VHF noise figure were determined by a combination of the state of the art and the time available for development, most were dictated by the scientific measurements to be performed. An introduction to ionospheric and interplanetary gas density measurements can be found in references 1 and 2. Performance of ground based facilities of the Stanford Center for Radar Astronomy, consisting of VHF and UHF transmitters and a fully steerable 150 foot parabolic antenna, sets the ultimate limit on signal strength available to the receiver.

Figure 2.1 is a simplified, functional block diagram of the receiver. Radio frequency, phase locked loops enable the carrier to be filtered in a 10 to 20 cps noise bandwidth without frequency stability problems. This makes measurement of the normalized frequency difference between carriers (phase path) possible at very low signal levels. Contents of the $\Delta f$ counter are telemetered at regular intervals. Audio phase locked loops are used to provide narrow bandwidth for the modulation frequencies so that group path data will be available at the full range of the space probe telemetry system.

### 2.1 - Electron Density Measurements

Group path measurements

| | |
|---|---|
| Total integrated electron density error | $\pm 4.3 \times 10^{16}$ electrons/$m^2$ ($\pm 6°$ phase error at 8.692 kc) |
| Maximum unambiguous integrated electron density | $1.7 \times 10^{19}$ electrons/$m^2$ (8 cycles of 8.692 kc) |

Phase path measurements

| | |
|---|---|
| Rate of change of integrated electron density error (1 min sampling interval) | $\pm 6 \times 10^{12}$ electrons/$m^2$ -sec ($\pm 1$ cycle of $\Delta f$ in 1 min) |
| Maximum rate of change of integrated electron density, without ambiguity (1 min sampling interval) | $\pm 3.2 \times 10^{15}$ electrons/$m^2$ -sec ($\Delta f = 8.5$ cps) |

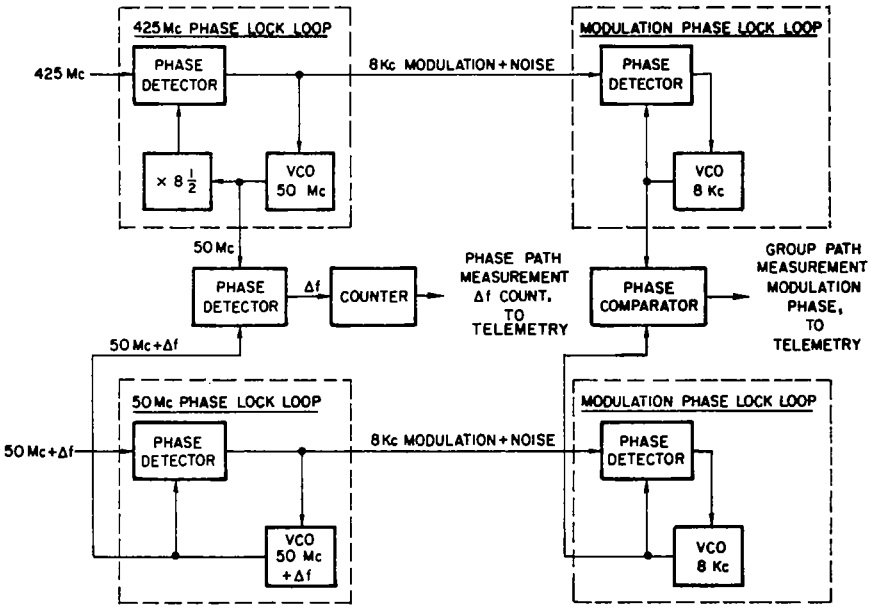



Figure 2.1 - Simplified Diagram of the Receiver
This diagram shows the concept of the phase path and group path measurements. The actual implementation and frequencies are slightly different from those shown.

## 2.2 - Receiver Performance at 0.5 AU ($75 \times 10^6$ km)

| Frequency of operation | 49.80 Mc | 423.30 Mc |
|---|---|---|
| **Receiver operating point at 0.5 AU** | | |
| Total signal power (carrier plus modulation) at bottom of 8 db antenna null; includes 2.5 db fading loss on 49.8 Mc | -125.7 dbm | -134.2 dbm |
| N/A (total noise to total signal power) in 45 kc IF NBW | 12.8 db | 12.5 db |
| Phase lock loop 3 db bandwidth | 21.6 cps | 33.2 cps |
| Signal power margin over threshold (defined as the power which gives 1 cycle loss/10 hr) at 0 v loop stress | 3.5 db | 2.0 db |

## 2.3 - Communication Link Parameters

| | | |
|---|---|---|
| Transmitting antenna | 150 ft. dia paraboloid | |
| Efficiency | 50 percent | |
| Transmission line loss | 1.0 db | |
| Polarization | Circular | |
| Receiving antenna. Both have nulls of 8 db | Quarter wave monopole | Half wave dipole |
| Transmission line loss | 0 db | 0.78 db |
| Polarization | Approximately linear | |
| Transmitter | | |
| Power | 86.0 dbm (400 kw) | 74.8 dbm (30 kw) |
| Modulation | Phase modulation | |
| Fraction of power in carrier | 0.5 | |
| Maximum range desired | 0.5 AU ($75 \times 10^6$ km) | |

## 2.4 - Receiver Performance[1]

| | | |
|---|---|---|
| Receiver system noise temperature, referred to antenna terminals; including cosmic noise, transmission line loss, and image response | 8300°K | 1500°K |
| Cosmic noise temperature | 8000°K | 100°K |

[1] See Appendix A for calculations of receiver performance and expected signal levels.

| | 49.80 Mc | | 423.30 Mc | |
|---|---|---|---|---|
| Receiver noise temperature alone, including image response | 300°K (3 db NF) | | 1200°K (7 db NF) | |
| Input impedance | 50 ohms | | | |
| IF noise bandwidth | 45 kc | | | |
| Receiver threshold sensitivity (defined as the power which gives loss of 1 cycle/10 hr). This is total power (carrier plus side bands)<br>Conditions: System noise temperature is 8300°K at 49.8 Mc; 1500°K at 423.3 Mc. Modulation sidebands use 0.5 of the power. Magnitude of loop stress < 0.1 v at the VCO input. | -129.2 | dbm | -136.2 | dbm |
| Additional signal power required to maintain threshold because of loop stress of magnitude: | | | | |
| 0.5 v at VCO input | 0.5 | db | 1.5 | db |
| 1.0 v at VCO input | 2.3 | db | 3.3 | db |
| **Threshold level parameters** | | | | |
| Loop noise bandwidth, $B_L$ | 24.8 | cps | 50 | cps |
| Loop error 3 db bandwidth | 9.0 | cps | 17.5 | cps |
| Loop 3 db bandwidth | 16.0 | cps | 31.3 | cps |
| Noise to signal ratio in IF noise bandwidth (45 kc) | 16.5 | db | 14.5 | db |
| Carrier amplitude, at amplitude phase detector output, relative to 5 v supply; with or without modulation | -0.14 | v | -0.175 | v |
| **Strong signal parameters** | | | | |
| Loop error 3 db bandwidth | | | | |
| with modulation | 74 | cps | 160 | cps |
| without modulation | 106 | cps | 230 | cps |
| Loop 3 db bandwidth | | | | |
| with modulation | 80 | cps | 180 | cps |
| without modulation | 111 | cps | 250 | cps |
| Carrier amplitude, at amplitude phase detector output, relative to 5 v supply: | | | | |
| with modulation | -1.5 | v | | |
| without modulation | -1.06 | v | | |

| | 49.80 Mc | 423.30 Mc |
|---|---|---|
| Interference level from other channel, for equal input levels | -87.5 db | -47.5 db |

## 2.5 - Receiver Outputs

### 2.5.1 - Group path measurement

Modulation Frequency: 7.192 or 8.192 kc ± 2 cps

Error of modulation phase measurement at receiver threshold

- Receiver alone, without use of calibration command (mean error): ± 6°
- Receiver alone, with use of calibration command (mean error): ± 3°
- Transmitter and receiver, together with use of calibration command (mean error): ± 6°
- Rms variation: 1.6°

Hold-in range at threshold (error increases with modulation phase lock loop stress): ± 50 cps

Output voltage (423.3 Mc channel is reference phase). See Figure 2.2

Linear from 0.20 to 2.80 v for -43° (317°) to 137°

Linear from 2.80 to 0.20 v for 137° to 317°

Output impedance: 1 kc

Output current (positive current flowing out of the output): -50 to +10 μa

The 16.834 kc clock pulse is used by this circuit.

The rounded corners of the triangular shaped output, Figure 2.2, are caused by noise. The averaging circuit used cannot average the output at the corners.

### 2.5.2 - Carrier amplitude and loop stress subcommutator output

The carrier amplitude (amplitude phase detector output) and loop stress are subcommutated alternately. A flip flop alternates with each scientific subcom pulse. In the binary zero state, the carrier amplitude is connected to the subcommutator output. In the binary one state,

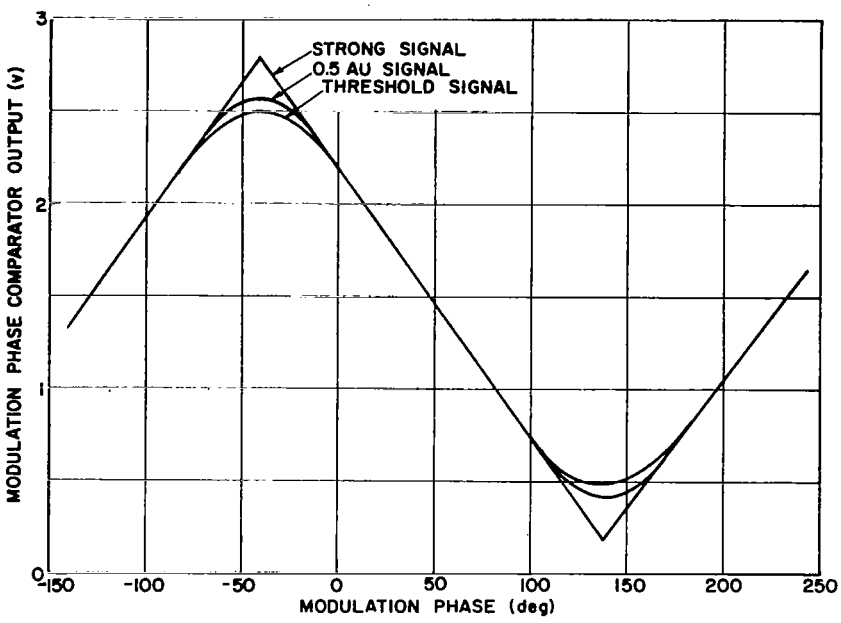



Figure 2.2 - Volts Output vs. Phase Input of the Modulation Phase Comparator

The output is shown for strong signal, signal levels corresponding to operation at 0.5 AU (Section 2.2), and threshold signals (Section 2.4). The reference phase is the 423.3 Mc channel at the receiver input. the loop stress is connected. The reset signal resets the flip flop to the binary zero state. It begins with the engineering subframe pulse and ends one bit time later with the next shift pulse. The 423.3 Mc channel information is connected to one output line, and the 49.8 Mc information is connected to another.

Output levels are with the Thevenin equivalent of the load connected (4.75 v, 465 k).

| | |
|---|---|
| Output impedance | 11 k |
| Carrier amplitude output | 0.2 to 3 v |
| no signal (minimum) | 0.2 v |
| strong signal, no modulation (maximum) | 2.83 v |
| strong signal, with modulation | 1.85 v |
| threshold signal, with or without modulation | |
| 423.3 Mc channel | 0.430 v |
| 49.8 Mc channel | 0.375 v |
| Carrier amplitude 3 db bandwidth | 0.3 cps |
| Loop stress output | 0.2 to 3 v |

| | |
|---|---|
| Zero loop stress (zero loop stress is the loop stress output for no RF signal input) | 1.6 v (nominally) |
| Loop stress scale factor | |
| 423.3 Mc channel | -11 kc/v |
| 49.8 Mc channel | 0.63 kc/v |

2.5.3 - Phase path measurement

$$\Delta f = \left| f_{49.8} - \frac{2}{17} f_{423.3} \right|$$

| | |
|---|---|
| $\Delta f$ phase detector 3 db bandwidth | 80 cps |
| $\Delta f$ counter capacity | 1024 counts (10 bits) |

Output - The contents of the 10 bit $\Delta f$ counter are transferred to the serial shift register with alternate frame rate pulses; the counter is not reset. A flip flop alternates with each frame pulse. Transition to binary zero causes the contents of the counter to be transferred to the shift register. The reset signal (discussed in Section 2.5.2) resets this flip flop to binary zero.

When the word gate is on, the output is shifted out synchronously with each shift pulse. Binary zeros are entered serially into the shift register as the information is shifted out. Thus, only binary zeros are shifted out after the first 10 bits of information have been shifted out.

2.5.4 - Format D output. Sample and Hold

The carrier amplitude of each channel is subcommutated by a sample and hold circuit. The two channels are sampled alternately with each word pulse, and that sampled value is held until the next word pulse. A flip flop alternates state with each word pulse. Transition to binary one causes the 49.8 Mc channel to be sampled. The reset signal (discussed in Section 2.5.2) resets the flip flop to binary zero, without causing a sample to occur.

| | |
|---|---|
| Carrier amplitude 3 db bandwidth | 10 cps |

| | |
|---|---|
| Output level with Thevenin equivalent of load connected to output (4.75 v, 465 k) | |
| No signal (minimum) | 0.2 v |
| Strong signal, no modulation (maximum) | 2.92 v |
| Output impedance | 11 k |
| Sample duration | 0.5 ms |
| Drift for 1 sec hold time | < 2 percent of full scale (.06 v) |
| Time to reach final level, in the positive going direction | < 100 μs |
| Time to reach final level, in the negative going direction | < 300 μs |

Sun Pulse - The sun pulse occurs once each spacecraft revolution (approximately 1 rps). With the bit rate 512 level on, the sun pulse causes the sample and hold output to be 0.2 v for 30 ms, or slightly more than 2 word times at the 512 bps rate. The sun pulse has no effect with the bit rate 512 level off.

## 2.6 - Specifications on the signals received from and sent to the spacecraft

These signals are listed in Table 2.1. Further information about the spacecraft data system is in Appendix B.

## 2.7 - General

| | |
|---|---|
| Power (constant power load) | < 1.50 w |
| Voltage (primary power is isolated from ground) | 20 to 35 v |
| Size | h x w x d<br>6.75 x 6.0 x 6.0 in<br>depth requires approximately one additional inch for mounting feet and connectors |
| Weight (without antennas) | 5.0 lbs |
| Temperature, operating | -15° to +60°C |
| storage | -45° to +85°C |

# Table 2.1 - Signals Received from and Sent to the Spacecraft Data System

| NOMENCLATURE | SIGNAL DESCRIPTION | NO-LOAD CHARACTERISTICS AND TOLERANCES | | | | | IMPEDANCE, OHMS | |
|---|---|---|---|---|---|---|---|---|
| | | AMPLITUDE, (+)VOLTS | | DURATION, MICROSECONDS (50%-50%) | RISE TIME (at generator output), MICROSECONDS (10%-90%) | FALL TIME (at generator output), MICROSECONDS, (90%-10%) | SPACE-CRAFT | INSTRUMENT |
| | | ON | OFF | | | | | |
| Main-Frame Rate Pulse | A pulse at beginning of each frame. | 11 ±2 | 0 ±1 | 10 ±3.5 | ≤ 1 | ≤ 1 | <5 | ≥3.3 K No DC potential shall be introduced on line by instrument. Capacitive load <300 pf. |
| Instrument Sub-Frame rate pulse | A pulse every 16 frames. | 11 ±2 | 0 ±1 | 10 ±3.5 | ≤ 1 | ≤ 1 | <5 | As above |
| Engineering Sub-frame rate pulse | A pulse every 64 frames. | 11 ±2 | 0 ±1 | 10 ±3.5 | ≤ 1 | ≤ 1 | <5 | As above |
| 16.384 kc clock | A pulse train with a 16.384 kc repetition rate. | 11 ±2 | 0 ±1 | $2^{+1.0}_{-0.5}$ | ≤ 1 | ≤ 1 | <5 | As above |
| Word Rate pulse | A pulse generated during the last bit period of each word. Word rate pulse delayed 122 ±10 μs from word gate. | 11 ±2 | 0 ±1 | 10 ±3.5 | ≤ 1 | ≤ 1 | <5 | As above |
| Bit shift pulse | Pulses generated at the bit rate in groups of 6 pulses followed by a missing pulse. Parity is inserted in 7th pulse position. | 11 ±2 | 0 ±1 | 10 ±3.5 | ≤ 1 | ≤ 1 | <5 | As above |
| 16 cps clock | A pulse train with a 16 cps repetition rate. | 11 ±2 | 0 ±1 | 10 ±3.5 | ≤ 1 | ≤ 1 | <5 | As above |
| Word Gate | Gate to each instrument to indicate time of reading out digital data to DTU. Separate line for main frame and sub-frame digital words. | $9^{+1}_{-2}$ | 0 ±1 | Bit rate and word format dependent | Rise Time Constant < 50 | Fall Time Constant < 1000 | <5 | ≥20 K from interface to ground. Capacitive load <300 pf. |
| DTU Operational Status | Continuous states indicating operational conditions of the DTU as follows: Bit Rates - 512, 256, 64, 16, 8 Formats - A, B, C, D Storage - Duty cycle, telemetry Separate line required for each signal. | $9^{+1}_{-2}$ | 0 ±1 | Duration of condition | Rise Time Constant <10 | Fall Time Constant < 3000 | 23 K | ≥48 K in series. ≥100 K from interface to ground. Capacitive load <300 pf. |
| Command Pulse | Pulse upon receipt of a ground command. Separate line for each command. | 10 ±2 | 0 ±1 | 10 ±2 | < 1 | 3 -15 | < 1000 | > 1000 |
| Sun Pulse | A single pulse per spacecraft revolution. | 10.5 ±2 | 0 ±1 | 12.5 ±6 | ≤ 1 | ≤ 1 | <10 | ≥3.3 K No DC potential shall be introduced on line by instrument. Capacitive load <300 pf. |
| Digital Data | Series of pulses synchronized to within 10μs of bit shift pulse. A pulse shall indicate one and no pulse shall indicate zero. | 10 ±1 Across 3.9 K | 0 ±1 Across 3.9 K | 3 -13 | ≤ 1 | ≤ 3 | 3.9 K ±1% | — |
| Analog Data | Normalized analog voltage. One line required for each word. | Normal-ized 0 to +3 | — | Duration of word gate | — | — | Current to instrument will be ≤25 μ amp. | ≤1000 for ±1 bit A/D conversion accuracy |
| Instrument operational status | Bi-level states indicating operational conditions of instruments. Separate line required for each signal. | 8 to 28 | 0 to +1 | Duration of condition | — | — | 47 K | ≤100 K |

NOTE: The capacitive load results from s/c wiring. (Max. 10 ft at 30 pf/ft.)

Vibration

Sinusoidal, swept once through each range at 2 octaves/min, in each of 3 orthogonal axes

| Frequency Range, cps | Test Duration, min. | Acceleration g, 0 to peak |
|---|---|---|
| 10 - 50 | 1.25 | 7.5 |
| 50 - 100 | .5 | 30 |
| 100 - 250 | .625 | 20 |
| 250 - 500 | .5 | 7.5 |
| 500 - 2000 | 1.0 | 21 |

Gaussian random vibration is applied with the "G-peaks" clipped at three times the rms acceleration specified in the schedule. Vibration is applied in each of 3 orthogonal axes.

| Frequency Range, cps | Test Duration, min. | Power spectral density, $g^2$/cps | Acceleration g - rms |
|---|---|---|---|
| 20 - 2000 | 4 each axis | 0.7 | 11.8 |

## 2.8 - Word Assignment for Instrument Outputs

### Δf counter output (digital output)

Line Ea. Format A, word 13; Format B, word 29.

The 10 bit digital output is the contents of a 10 bit counter which counts the cycles difference between the 49.8 Mc carrier and $\frac{2}{17}$ of the 423.3 Mc carrier. To obtain the difference in frequency (Δf), the difference between successive 10 bit outputs is divided by the sampling interval. The counter is not reset by the sampling.

Figure 2.3 shows how the 10 bit word is read out on successive frames. This alternating read-out is continued in consecutive frames. Frame 1 in Figure 2.3 is read out in the first frame following the engineering subframe pulse.

| | | | | | | |
|---|---|---|---|---|---|---|
| FRAME 1 | 1 $2^9$ | 2 $2^8$ | 3 $2^7$ | 4 $2^6$ | 5 $2^5$ | 6 $2^4$ |
| FRAME 2 | 1 $2^3$ | 2 $2^2$ | 3 $2^1$ | 4 $2^0$ | 5 0 | 6 0 |

Figure 2.3 - Binary Digit Designation
The number in the upper left hand corner of each box is the bit sequence number. The number in the center of each box is the weight of a binary one in that position. The last two 0's are always binary zeros.

Modulation phase

Line Eb. Format E (scientific subcom), words 7 and 15.

This analog voltage is the relative phase of the same modulation on the two carriers of 49.8 and 423.3 Mc. The modulation frequency can be 7.692 or 8.692 kc. The output ranges from 0.2 to 2.8 v. Figure 2.2 shows a calibration curve.

49.8 Mc channel carrier amplitude and loop stress

Line Ec. Format E (scientific subcom), word 2.

This analog voltage is alternately the carrier amplitude and the loop stress. The carrier amplitude is the first of the two quantities to be read out after the engineering subframe pulse. A carrier amplitude of 0.2 v represents no RF signal, and 2.85 v represents strong signal with no modulation. A loop stress signal of about 1.6 v represents zero loop stress.

423.3 Mc channel carrier amplitude and loop stress

Line Ed. Format E (scientific subcom), word 11.

This is the same as for the 49.8 Mc channel.

Format D output. Carrier amplitude of the 49.8 and 423.3 Mc channels

Line Ee. Format D, words 4 through 16, and words 20 through 32.

This analog voltage is the carrier amplitude of the 49.8 and the 423.3 Mc channels, alternately. Words 4 and 20 are the 49.8 Mc channel. An output of 0.2 v represents no signal, and 2.92 v represents strong signal with no modulation. At 512 bps, the sun pulse causes the output to be 0.2 v for a duration of two word times, occuring asynchronously with the format.

# 3. RECEIVER SYSTEM

The block diagram, Figure 3.1, page 21, shows the whole receiver system.

## 3.1 - Dual channel phase locked receiver

The RF inputs are 423.3 Mc and 49.8 Mc and are phase modulated. The outputs of the phase locked receiver which will provide scientific information are:

1. The $\Delta f$, which is the normalized frequency difference between the carriers ($\Delta f = \left| f_{49.8} - \frac{2}{17} f_{423.3} \right|$).
2. The demodulated modulation from the loop phase detectors.
3. The carrier amplitude (the output of the amplitude phase detector), which is proportional to the signal to noise ratio, when the limiters are limiting on noise.

Additional outputs are the loop stress which, together with the carrier amplitude, are used to monitor the operation of the receiver.

### 3.1.1 - 423.3 Mc phase locked receiver

The 423.3 Mc channel is a coherent phase lock loop. The VCO-1 is controlled by the output of the loop phase detector; and the loop amplifier, which includes the control network.

The basic frequency in the receiver is 24.9 Mc. The input at 423.3 Mc is 17 x 24.9 Mc. The local oscillator frequency of the first mixer is 448.8 Mc = 18 x 24.9 Mc. The first IF is 24.9 Mc. The second IF is operating at an arbitrarily chosen 7 Mc, instead of some harmonic of 24.9 Mc. The reason for this is to avoid producing 24.9 Mc or its harmonics at high levels, in order to keep these harmonics from leaking into the inputs of the receiver or the first IF, where they could cause self lock.

The 423.3 Mc phase lock loop is coherent, despite the use of the 7 Mc second IF and the 7 Mc reference oscillator. The phase lock loop is coherent with the difference between the VCO-1 and the reference oscillator frequencies: 31.9 - 7.0 = 24.9 Mc.

The third harmonics of the VCO and reference oscillator are generated before mixing to prevent undesired harmonics of 24.9 Mc, especially

the first and second, from being produced. The 74.7 Mc third mixer output is multiplied by 6 to obtain the first mixer local oscillator frequency.

3.1.2 - 49.8 Mc phase locked receiver

The 49.8 Mc channel is phase locked, but not coherent. Like the 423.3 Mc channel, the VCO-2 is controlled by the output of the loop phase detector for the 49.8 Mc channel through the loop amplifier, which includes the control network.

The local oscillator frequency (74.7 Mc) for the first mixer is derived from the 423.3 Mc channel. Hence, the first mixer local oscillator frequency is coherent with the 423.3 Mc carrier and not with the 49.8 Mc carrier. The 74.7 Mc local oscillator could have been generated separately for the 49.8 Mc channel, but instead, it is derived from the 423.3 Mc channel receiver to avoid duplication of circuitry.

3.1.3 - Function of parts of the receiver

Δf comparison

The output frequency of the Δf phase detector is the same as the difference frequency between the normalized carrier frequencies, $\Delta f = \left| f_{49.8} - \frac{2}{17} f_{423.3} \right|$. An increment of frequency has been added to each frequency source in the two channel receiver in the block diagram, Figure 3.1. Each VCO must adjust its frequency increment, ΔVCO-1 or ΔVCO-2, until the output of its corresponding loop phase detector is zero cps. The output of the Δf phase detector is then the difference frequency between the normalized carrier frequencies.

Phase of the modulation out of the loop phase detector

At the output of the loop phase detector of the 423.3 Mc channel, Figure 3.1, the ΔVCO-1 must change in the same direction as the input, Δ423. At the output of the 49.8 Mc channel, the ΔVCO-2 must change in the opposite direction to the input, Δ49.8. To obtain this opposite polarity of ΔVCO frequency, the loop phase detector for the 49.8 Mc channel must operate on the opposite slope of its detection characteristic

curve than the 423.3 Mc channel loop phase detector. This opposite slope causes output of the two loop phase detectors to be of opposite polarity when the RF carriers are of the same relative modulation phase.

Amplitude phase detector

The carrier amplitude (amplitude detector phase output) is detected with a 90° phase shifted reference signal. The phase lock loop holds the output of the loop phase detector near zero volts. This occurs when the reference signal is in quadrature with the input signal. Hence, the 90° phase shifted reference signal is in phase with the signal in the amplitude phase detector.

Thus, the output of the amplitude phase detector is proportional to the amplitude of the phase locked signal at its input. This amplitude is proportional to the signal to noise ratio in the IF noise bandwidth, when the limiters in the IF are limiting on noise. See Appendix A (page A-10) for the equation for A, a more exact expression for the amplitude.

Crystal filter in the first IF

The first IF crystal filter has a noise bandwidth of 45 kc. The two crystal filters in one dual receiver are phase matched within 2° of each other over the middle 21 kc of the passband, and are phase symmetric about the center of the passband within 20°. The amplitude is flat to within 0.25 db over the center 21 kc passband. All this accuracy is to insure that the phase of the modulation will be affected equally by both channels.

3.1.4 - IF Switch

The IF switch is used to establish the output of the modulation phase detector for zero modulation phase shift at the inputs to the receiver. Once this zero phase point is established, the modulation phase detector output vs. modulation phase can be calibrated by changing the modulation phase at the transmitters. Little error is expected, but this will serve as a check.

The IF switch, upon a calibrate command, disconnects the 49.8 Mc channel IF signal from the first mixer. It connects both first IF inputs

to the same signal, the output of the 423.3 Mc first mixer. An internal reset signal switches the IF switch back to normal operation. When the input signal to both channels is the same, there is zero modulation phase shift. This does not compare the modulation phase shift in the RF and first mixer stages, but since the first mixer stages have a bandwidth of 2 to 3 Mc and the RF stages are even wider, they contribute little to the uncertainty in the modulation phase measurement.

3.2 - Modulation phase comparator

The modulation phase comparator, Figure 3.1, measures the relative phase of the detected modulation from the two channels of the receiver and provides a dc output proportional to the relative phase. The phase comparator can measure the phase of signals at either 7.692 or 8.692 kc. The two frequencies allow ambiguities up to 7 or 8 cycles of phase shift to be resolved. The output is 0.2 v for -43° (317°), increasing linearly to 2.8 v for 137°, and then decreasing linearly to 0.2 v for 317°. However, the modulation phase shift out of the receiver is 180° when the inputs to the receiver have 0° modulation phase shift, as explained under "Phase of the modulation out of the loop phase detector" (Section 3.1.3). Therefore, the modulation phase comparator output shifts 180° for modulation at the receiver input, to give 0.2 v for 137° and 2.8 v for 317°. This triangular shaped output was used instead of a linear output for a 360° range in order to obtain an error of less than 1 percent of 1 cycle, even though the spacecraft A-D converter quantizes to only 64 levels.

A broad bandpass filter centered on 8 kc precedes the mixer. The filtered signal (7.692 or 8.692 kc) is mixed with 8.192 kc; the output is 500 cps. The 8.192 kc is 500 cps above the input frequency for the 7.692 kc input, and 500 cps below for the 8.692 kc input. Hence, the phase meter is sensitive to either of the two frequencies without switching.

The 500 cps signal is filtered and amplified, and fed to the phase detector of a phase lock loop. The output of the phase detector goes through a control network and a dc amplifier to a 1 kc VCO. The VCO

output is divided by 2 to provide a symmetrical 500 cps signal for the phase detector, and for phase comparison with the other channel.

The second channel is identical to the first. The 16.384 kc pulses from the spacecraft are crystal controlled, and are expanded into the 8.192 kc square wave by an alternating flip flop. This flip flop output is used for the mixers.

The symmetrical 500 cps signal, from the phase locked flip flop from each channel, is cross correlated in the phase detector which is a digital NAND gate. The phase detector output is filtered to eliminate the 500 cps component and to provide additional filtering for the phase measurement.

### 3.3 - Analog gates and gate selector

The analog gates subcommutate the carrier amplitude and loop stress onto an output line for each channel. There are two identical subcommutation channels. Only the 423.3 Mc channel will be discussed. The loop stress voltage ranges from 3 to 7 v; this is transferred to 3 to 0.2 v respectively and connected to the output via the electronic switch. The carrier amplitude ranges from 5 to 3.5 v which is transferred to 0.2 to 2.85 v respectively and alternately connected to the same output as the loop stress via another electronic switch.

The two electronic switches are selected alternately by a flip flop, which changes state with the scientific subcom pulse. This flip flop is synchronized to the spacecraft subcommutation system via the reset signal (see Section 3.4 for the source of the reset signal).

### 3.4 - Counter register

The counter register accumulates the number of cycles of $\Delta f$, and shifts the count out periodically in serial form under spacecraft control. The $\Delta f$ phase detector output has a frequency response from 0 to 80 cps, with the low pass filter of the counter register connected. Normally, $\Delta f$ will be biased to about 5 cps, to enable detection of positive and negative excursions of $\Delta f$. The Schmitt trigger and following amplifier shape the sinusoidal-like $\Delta f$ phase detector output to drive

the input of the 10 bit binary counter.

The 10 bits of the counter will not fit into one 6 bit spacecraft word. Therefore, part of it must be sent in one word, and the rest in the next word. The contents of the counter are non-destructively shifted in parallel into the 10 bit serial shift register once every two words. We have one word per frame. The frame rate pulse occurs at the beginning of each frame, and is divided by two in a flip flop. Transition of this flip flop to the zero state transfers the contents of the counter to the shift register.

The time to shift out of the serial shift register is defined by the word gate from the spacecraft. Shift pulses are always present. The word gate selects the group of 6 shift pulses in an AND gate. These pulses are amplified and drive the serial shift register and its output pulse amplifier. There is an output pulse for binary one and no pulse for binary zero. The first word out of the shift register is the 6 highest order bits, highest order bit first. The second word is the 4 lowest order bits, highest order bit first, followed by two binary zeros.

A reset pulse is initiated by the engineering frame pulse from the spacecraft (occuring once every 64 frame pulses) and terminated one bit time later by the next bit pulse. The reset is used to synchronize the order of the words out of the shift register with spacecraft telemetry format. The reset pulse is also used for telemetry format synchronization in the sample and hold circuit, and in the analog gates and gate selector.

## 3.5 - Sample and hold

The sample and hold circuit, Figure 3.1, samples the carrier amplitude alternately from the 423.3 Mc channel and the 49.8 Mc channel. The "hold" function is necessary because the conversion rate of the spacecraft 6 bit A-D converter can be as slow as 8 bps. The circuit is used to measure the carrier amplitude (actually, signal to noise ratio) versus spacecraft rotation for one rotation of the spacecraft (approximately 1 second). It is also used to obtain the instantaneous carrier amplitude versus time for a measurement involving occultation by the

moon.

Each carrier amplitude signal is filtered by a 10 cps low pass filter. Each filter output is connected to an electronic switch. Either one switch or the other is turned on for 0.5 msec during which time the storage capacitor is charged to the same value as the input. This value is held until the alternate switch is turned on. The low input current hold amplifier, with a gain of one, follows the storage capacitor. A level transfer circuit shifts the amplifier's output voltage from a 5 v base line, going negative to 3.5 v, to an 0.2 v base line, going positive to 3 v. This level transfer circuit has a gain of about two.

The switches are operated by the NANDing of a flip flop output, which determines which switch will be operated; and a one shot output, which determines the 0.5 msec sample time. The word rate pulse triggers the one shot and changes the state of the flip flop. The reset input to the flip flop maintains synchronization with the spacecraft telemetry format.

The sun pulse occurs once each spacecraft rotation, and defines the angular position of the spacecraft. The 30 msec one shot, triggered by the sun pulse, is two words long at the 512 bps rate. Hence, the clamp will clamp the output to zero for at least one whole word, marking the angular position of the spacecraft. The sun pulse is ANDed with the 512 bps state so that at other bit rates, the sun pulse clamp will be inoperative.

## 3.6 - Power Converter

The power converter, Figure 3.1, converts the nominally 28 v input to the supply voltages required by the system: 12, 5, 2.5 and -3 v. The 28 v input is electrically isolated from ground and from the output supplies in order to eliminate the magnetic field due to ground currents. The blocking oscillator power converter is a constant power type, over a supplied input voltage range of 24 to 33 v. The output voltage change of the blocking oscillator portion of the converter is about 100 mv for a 9 v change in input. This voltage change is sufficiently low for the

2.5 and -3 v supplies. A post regulator for the 12 and 5 v supplies gives an output voltage change of<0.5 mv for the 9 v change in input.

The 28 v input passes first through a high frequency filter (for blocking oscillator frequencies greater than 1 Mc), and then to an active current limiter. The turn on and other transient current surges are limited to less than 250 ma by the current limiter. A low pass filter provides instantaneous peak power to the blocking oscillator and keeps the blocking oscillator transients from the 28 v supply.

The blocking oscillator portion of the converter is controlled by a feedback loop. The output voltage is compared with a zener reference; the difference is amplified and used to control the blocking oscillator base current.

The converter transformer provides 2.5 v and -3 v for direct use, and 13.3 v for the post regulator. The post regulator for the 12 v compares the 12 v with a zener, and the difference is amplified and applied to the series regulator. An additional input from the 13.3 v supply into the summing point further reduces the effect of input transients.

The 5 v is dropped from the 12 v through a zener diode.

A more complete description of the blocking oscillator converter (without the current limiter or series regulator) can be found in Reference 3.

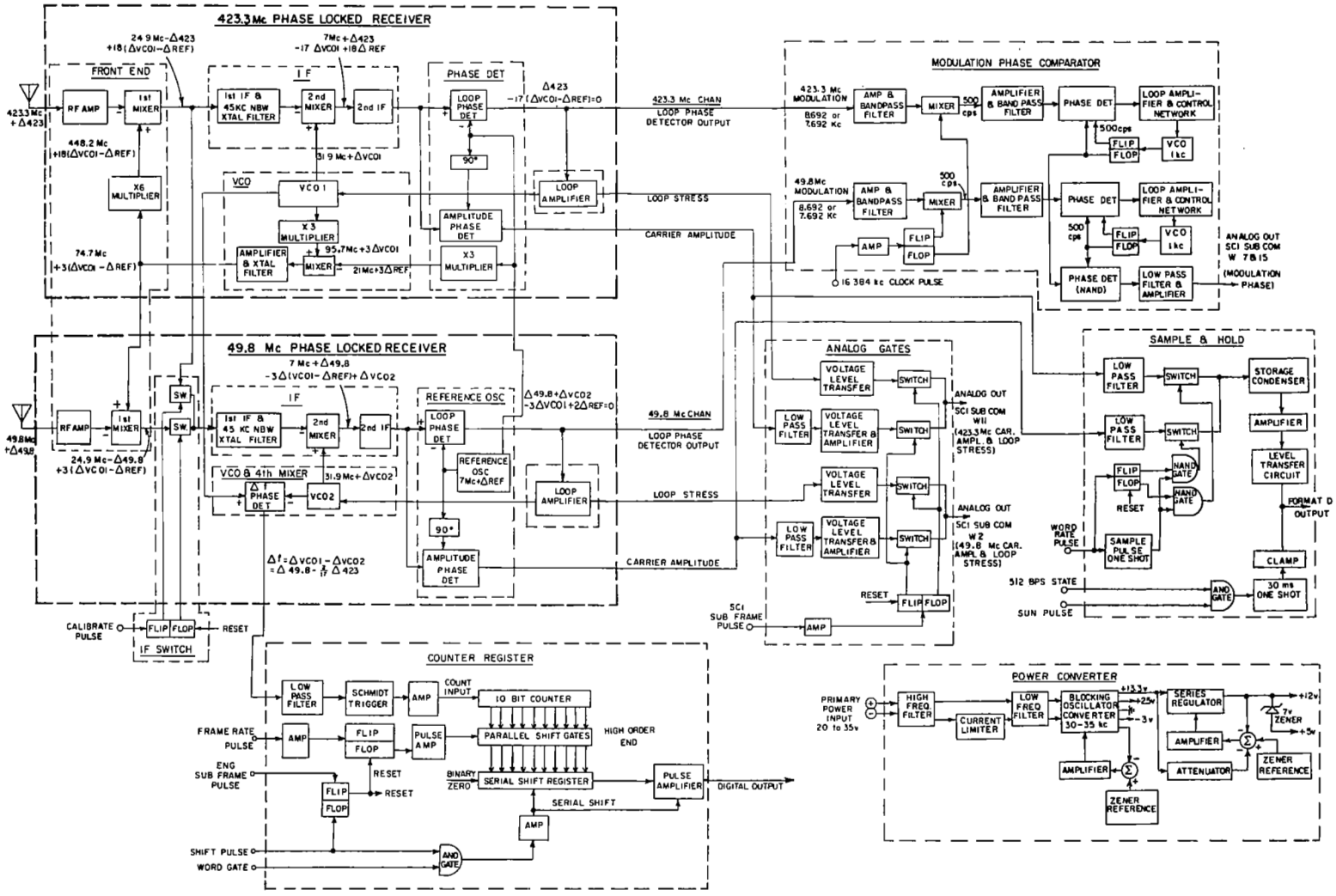



Figure 3.1 - Block Diagram of the Whole Dual Channel Receiver

# 4. CIRCUIT DESCRIPTION AND SPECIFICATION FOR EACH SUBASSEMBLY

This section contains the specifications and circuit description of each subassembly. Schematics, pictorial diagrams and photographs of the various units are located at the end of the section beginning on page 57.

Figures 4.2, 4.3, 4.4, and 4.5 are photographs which show the location of subassemblies in the receiver. Table 4.1 lists pin connections for all external connectors. The frame A wiring diagram is Figure 4.6 and frame B wiring diagram is Figure 4.7.

The radio frequency modules were designed and constructed at TRW Space Technology Laboratories (STL) and are described in Sections 4.1 through 4.6. The overall receiver design and the data processing and support subassemblies were designed and constructed at Stanford Research Institute (SRI). These subassemblies are described in Sections 4.7 through 4.13.

## 4.1 - Front End

Figure 4.8 is a pictorial diagram of the front end and Figure 4.9 is a schematic.

Specifications

| | |
|---|---|
| 423.3 Mc front end gain | 18 db (> 17 db) |
| Input and output impedance | 50 ohms |
| 423.3 Mc noise figure | < 5 db |
| 423.3 Mc noise figure, corrected for image | < 6.5 db |
| 423.3 Mc 3 db bandwidth | 2.3 Mc (< 2.6 Mc) |
| 423.3 Mc image response | -4 db |
| 423.3 Mc channel 448.2 Mc local osc. level | |
| At antenna input | -22 db |
| At IF output | -19 db |
| Interference in 423.3 Mc channel due to 49.8 Mc channel | -66 db |

| | | |
|---|---|---|
| 49.8 Mc front end gain | | 26 db (> 20 db) |
| Input and output impedance | | 50 ohms |
| 49.8 Mc noise figure | | 3.4 db (< 3.5 db) |
| 49.8 Mc 3 db bandwidth | | 2.3 Mc (< 3.0 Mc) |
| 49.8 Mc image response | | -30 db |
| 49.8 Mc channel 74.7 Mc local osc. level | | |
| At antenna input | | -52 dbm |
| At first mixer output | | -36 dbm |
| Interference in 49.8 Mc channel due to 423.3 Mc channel | | -72 db |
| 74.7 Mc input level (nominal)(P13A) | | -10 dbm |
| | 74.7 Mc | 448.2 Mc |
| 448.2 Mc X6 multiplier 50 ohm output level (junction of C603 and C616) vs. 74.7 Mc input level: | 0 dbm | - .8 dbm (-3 dbm ± 2 db) |
| | - 5 dbm | -1.0 dbm (-4 dbm ± 3 db) |
| | -10 dbm | -1.25 dbm (-6 dbm ± 4 db) |
| | -15 dbm | -2.8 dbm (-10 dbm ± 6 db) |
| Maximum first mixer output (24.9 Mc) level for measurements | | -27 dbm |
| Power | 12 v | 10.6 ma |
| | 5 v | 0.23 ma |

Front end circuit description

At the top of Figure 4.9 is the 423.3 Mc channel RF amplifier (Q602). This amplifier is a grounded base stage with neutralization which allows higher gain. The transistor, an RCA 2N2857, was the lowest noise figure silicon transistor available at the time of design. The lowest noise figure 2N2857's were selected for use in this stage.

The 423.3 Mc signal from the collector of the RF amplifier feeds the base of the mixer stage, Q603, a Fairchild S7201 (2N918 with a non-magnetic hat). The local oscillator frequency of 448.2 Mc is fed through a filter and 50 ohm matching network (T604 and C616) to the emitter of the mixer. The local oscillator signal level is about -2 dbm at the 50 ohm input to the matching network, the junction of T604 and C616. The collector of the mixer is tuned to 24.9 Mc, the first IF frequency. All the adjustments are tuned for maximum output from the mixer, then

C602 is adjusted for best noise figure.

In the middle of the schematic are 4 transistors which form an X6 multiplier, for multiplying from 74.7 Mc to 448.2 Mc. Q609 is a grounded base amplifier, used for isolation and amplification. T612 and T611 are tuned to 74.7 Mc. Q605 is a tripler; its collector (C625) is tuned to 224.1 Mc. Q604 is an amplifier and Q601 is a doubler with its collector (C606) tuned to 448.2 Mc. T601 is tapped at 50 ohms to provide output through C603 to the matching network, T604 and C616.

The tuning range of the capacitors and inductors in the X6 multiplier is broad enough so that a stage intended to be an amplifier, may be tuned as a doubler, etc. Each stage must, therefore, be observed with a sampling scope or at several frequencies with a receiver to insure that it is performing its intended function.

The RF amplifier and mixer stages for the 49.8 Mc input are shown at the bottom of Figure 4.9. The RF stage, Q606, a grounded emitter stage, is run mismatched for stability instead of neutralized, primarily to make its gain comparable to that of the 423.3 Mc RF stage. The comparable gain was desired to minimize cross talk between channels. The base input (L604) and collector output (T613) are tuned to 49.8 Mc. The RF amplifier is an RCA 2N2857, selected from those left after the best had been chosen for the 423.3 Mc channel. This transistor provides a better noise figure than the S7201 (non-magentic hat version of the 2N918), and is far better than is necessary for the 8000°K cosmic noise.

The mixer, Q607, is fed with a 49.8 Mc signal at the base and with the 74.7 Mc local oscillator signal at the emitter. The collector load of the mixer (T614) is tuned to 24.9 Mc.

A separate amplifier, Q608, provides the additional gain necessary for the 74.7 Mc local oscillator signal while reducing the amount of 49.8 and modulated 74.7 Mc signal going up the X6 multiplier chain.

All adjustments associated with the 49.8 Mc channel are made for maximum output at 24.9 Mc. L604 is then adjusted for best noise figure.

## 4.2 - IF Amplifier

Figure 4.10 is a pictorial diagram of the IF amplifier, and Figure

4.11 is a schematic. The receiver uses two identical IF amplifiers consisting of an amplifier at 24.9 Mc; a mixer which converts the signal to 7 Mc and, finally, a 7 Mc amplifier. There are limiters on four stages of the IF amplifier.

Specifications

| | |
|---|---|
| First IF amplifier center frequency | 24.9 Mc ± 1 kc |
| First IF gain | 54 db (> 50 db) |
| First IF input impedance (E704) | 50 ohms |
| First output impedance (point "A" T705) | 50 ohms |
| First IF 3 db bandwidth (with crystal filter) | 45 kc |
| First IF bandpass ripple | ± 0.3 db |
| First IF crystal filter characteristics | |
| Center frequency | 24.9 Mc ± 1 kc |
| Phase match of matched pairs over the center 22 kc of the bandpass | ± 2° |
| Phase symmetry about the center frequency over the center 22 kc of the bandpass | ± 20° |
| Noise bandwidth | 45 kc |
| Ripple, center 22 kc bandwidth | ± 0.2 db |
| 3 db bandwidth | 40 kc |
| First IF 3 db bandwidth without crystal filter | 1.4 Mc |
| Maximum output of first IF which is safely below limiting level (for gain measurements) | -30 dbm |
| Second mixer input center frequency | 24.9 Mc |
| Second mixer input impedance (point "A" T706) | 50 ohms |
| Second mixer local oscillator frequency | 31.9 Mc |
| Local oscillator input impedance | 50 ohms |
| Local oscillator input level (approx.) | -3 dbm |
| Second mixer output frequency | 7.0 Mc |

| | | |
|---|---|---|
| Gain of second IF amplifier, including mixer gain | | 87 db (> 80 db) |
| Second IF center frequency | | 7.0 Mc |
| Second IF output level, with limiting (E708) | | 6 v pp |
| Second IF output impedance (E708) | | will drive 1 k load |
| Second IF 3 db bandwidth | | 180 kc (< 400 kc) |
| Second IF output test point output impedance (E706) | | 50 ohms |
| Maximum output level of second IF output test point which is safely below limiting level (used for gain measurements) | | -10 dbm |
| Power | 12 v | 11.6 ma |
| | 5 v | 0.2 ma |

IF Amplifier Circuit Description

The upper half of Figure 4.11 is the first IF amplifier. This amplifier has three transistor stages, with a stage gain of about 18 db. The stages are mismatched by the resistor shunted across the collector inductors to make tuning easier and insure stability. The crystal filter determines the bandwidth of the first IF and of the whole receiver. The input and output impedance of the crystal filter is 500 ohms resistive, and is matched to the amplifiers with transformers T702 and T703. Capacitor C710 is used to adjust for minimum ripple in the passband.

The last stage of the first IF has diodes across the collector tuned circuit to provide the first stage of limiting. Input and output impedances of the first IF amplifier are at 50 ohms to facilitate measurements.

The lower half of the schematic is the second mixer, Q704, and second IF. The signal input at 24.9 Mc is through a 50 ohm impedance matching transformer to the base of the mixer. The local oscillator signal of 31.9 Mc is injected into the emitter. A tuned network, C728 and T707, matches the emitter to the 50 ohm local oscillator input, E709. The local oscillator input level is about -3 dbm. The collector of the second mixer is limited with diodes across the tuned circuit.

The next three stages with individual gain of about 24 db make up the 7.0 Mc second IF amplifier. The stages of this amplifier are mismatched by a resistor shunted across each collector inductor to make alignment easier and the first two stages have diode limiters. The output stage power amplifier, Q707, is adjusted to 6 v pp open circuit at E708 on a limiting signal by selection of emitter resistor, R727.

The output stage can drive its load (an emitter follower in the following module) with almost no drop in output. Because the load is capacitive, the output transformer, T711, is retuned for maximum output after the receiver has been assembled. The extra winding, E706, (TP701) is a 50 ohm output for adjustment and measurement.

## 4.3 - Reference Oscillator

The reference oscillator module includes the 7 Mc reference oscillator and buffer amplifier, and the loop and amplitude phase detectors for the 49.8 Mc channel. Figure 4.12 is the pictorial diagram and Figure 4.13 is the schematic.

Specifications

| | |
|---|---|
| 7 Mc oscillator frequency at 25°C | 7.00000 Mc $\pm$ 10 cps |
| 7 Mc buffer amplifier output level (P20A) | 7 dbm |
| 7 Mc buffer amplifier output impedance | 50 ohms |
| 7 Mc variation with temp. -20° to 55°C | less than $\pm$ 300 cps |
| Signal input level (7 Mc) (P18B) | 6 v pp |
| Signal input impedance | > 1 k |
| Amplitude phase detector output (E906) (locked to strong signal) | -1.5 v (with reference to the 5 v supply) |
| Amplitude or loop phase detector output (strong signal, unlocked) | 3.0 v pp |
| Amplitude or loop phase detector unbalance (noise only for signal) | magnitude < 25 mv dc |
| Amplitude or loop phase detector output impedance | approx. 1 k |
| Amplitude phase detector 3 db bandwidth | 16 kc |

| | | |
|---|---|---|
| Loop phase detector 3 db bandwidth | | 32 kc |
| 7 Mc reference oscillator signal level at base of Q901 | | 1.5 v pp |
| Power | 12 v | 15.3 ma |
| | 5 v | 0.35 ma |

Reference Oscillator Circuit Description

The 7 Mc crystal oscillator is shown in the lower right hand corner of Figure 4.13. The transistor oscillator, Q905, has positive feedback from the collector to the base via transformer T903. The 7 Mc crystal, Y901, which is in series with the emitter, allows the stage to have gain only near the series resonant frequency of the crystal. The diode, CR904, rectifies some of the oscillator output to provide negative dc feedback to control the amplitude of oscillation. When the oscillator amplitude exceeds 5 v zero to peak at the diode, diode current will begin to flow, thus taking current away from the emitter of the transistor. Oscillator stability is quite good and the output exhibits a frequency shift of only about 15 cps with a 1 v change in either power supply.

The buffer amplifier, Q904, provides the 7 Mc reference signal for the 423.3 Mc channel phase detector module and isolates the crystal oscillator and the phase detector driver inputs, Q901 and Q903, from the load.

The 7 Mc input signal from the second IF output, drives the emitter follower Q902. The emitter follower load is a toroidal transformer, T901, with trifilar windings to insure equal, in phase signals to both phase detectors. The relatively large 5 ma dc emitter current is necessary to provide enough driving power to the 1 k resistors in the phase detectors.

The loop phase detector is at the top of the schematic, and includes T905. T905 is driven by transistor Q901, with a dc collector current of about 4 ma. This relatively high power is required to drive the two 1 k resistors (R910 and R911) in the transformer secondary, and the relatively low Q of the transformer. The transformer is low Q to minimize the effect of temperature on phase shift through it. The secondary of the transformer is bifilar wound to obtain equal signals on both sides

of the center tap.

The phase detector is simply a half wave switch, which connects the junction of the diodes CR901 and CR905 (signal input) to the transformer center tap, wires Nos. 4 and 5. For the half cycle that the switch is conducting, the input signal is averaged through the RC network formed by R910 and R911 in parallel and C915. During the non-conducting half cycle, the RC network is not driven. The output, E905, is biased to 5 v by connecting the T901 signal winding return to the 5 v supply.

The amplitude phase detector which is driven by Q903 and T902 is identical to the loop phase detector with the exception of a 90° phase shift network between the oscillator signal and the base of Q903. The phase shift network consists of the 200 ohm load R901, phase shift elements C904 and L902, and compensation, C903, to make the network resistive. The phase shift network has a Q of 1, is low impedance (200 ohms), and hence, is quite phase stable. The output terminal is E906.

The phase detector diodes, CR902 and CR903, are connected to make the sign of the amplitude output negative with respect to the 5 v supply.

## 4.4 - Phase Detector

The phase detector module contains the 423.3 Mc channel phase detectors which are almost identical to those for the 49.8 Mc channel. It also contains a frequency tripler to produce 21 Mc from the 7 Mc reference oscillator signal. Figure 4.14 is the pictorial diagram and Figure 4.15 is the schematic.

Specifications

| | |
|---|---|
| 21 Mc buffer amplifier output level (P15B) | -0.8 dbm (> -8 dbm) |
| 21 Mc buffer amplifier output impedance | 50 ohms |
| 7 Mc reference oscillator input level (P20B) | -6 dbm |
| 7 Mc reference oscillator input impedance | 50 ohms |

| | | |
|---|---|---|
| Signal input level (7 Mc)(P12B) | | 6 v pp |
| Signal input impedance | | > 1 k |
| Amplitude phase detector output (E906) (locked to strong signal) | | -1.5 v (with reference to the 5 v supply) |
| Amplitude or loop phase detector output (strong signal, unlocked) | | 3.0 v pp |
| Amplitude or loop phase detector output (noise only for signal) | | magnitude < 25 mv |
| Amplitude or loop phase detector output impedance | | approx. 1 k |
| Amplitude phase detector 3 db bandwidth | | 16 kc |
| Loop phase detector 3 db bandwidth | | 32 kc |
| 7 Mc reference oscillator signal level at the base of Q901 | | 1.5 v pp |
| Power | 12 v | 13.5 ma |
| | 5 v | 0.12 ma |

Phase Detector Circuit Description

The 7 Mc reference oscillator signal is transformed from 50 ohms to 200 ohms by T907. The secondary of this transformer is returned to 5 v dc to provide base bias for the driver and tripler transistors. Signal level at the transistor bases is about 1.5 v pp.

Q904 is a tripler, with its collector tuned to 21 Mc. The 21 Mc signal is coupled to the output, E908, through a double tuned circuit which provides additional attenuation to the undesired harmonics of 7 Mc.

The amplitude and loop phase detectors are almost identical to those in the reference oscillator module. The only difference is that the diodes in the amplitude phase detector (CR902 and CR903) are reversed in polarity in this module. The need for this is explained in Section 3.1.3.

## 4.5 - Voltage Controlled Oscillator (VCO)

Figure 4.16 is the pictorial diagram of the VCO and Figure 4.17 is the schematic. This module includes a voltage controlled oscillator at 31.9 Mc with its buffer amplifier, and the third mixer which produces

74.7 Mc by mixing the third harmonics of 31.9 Mc and 7 Mc.

Specifications

| | | |
|---|---|---|
| VCO frequency at 5 v input | 31.90000 Mc ± 100 cps at 25°C | |
| VCO frequency variation over the temperature range -20° to +55°C | less than $^{+400}_{-300}$ cps | |
| VCO gain | 950 ± 100 cps/volt | |
| VCO input range (P805) | 5.0 ± 3.0 v | |
| VCO buffer amplifier output level (P14B, P19A) | 1.0 dbm (> -1 dbm) | |
| VCO buffer amplifier output impedance | 50 ohms | |
| 74.7 Mc output level (P13B) | -10 dbm | |
| 74.7 Mc output level for reduced 21 Mc input of -16 dbm | -15 dbm | |
| 74.7 Mc output impedance | 50 ohms | |
| 21.0 Mc input level (P15A) | -6 dbm | |
| 21.0 Mc input impedance | 50 ohms | |
| Power | 12 v | 6.4 ma |
| | 5 v | 0.15 ma |

VCO Circuit Description

The voltage controlled oscillator, Q804, is a grounded base amplifier connected as an oscillator. The collector transformer (T808) output is coupled through the crystal and a series tuned circuit to the emitter. Q804 is a Fairchild S7200 which is a 2N915 with a non-magnetic hat.

The VCO collector circuit consists of T808, a powdered iron toroid for minimum temperature coefficient, capacitor C830, variable capacitor C833, and negative temperature coefficient capacitor (N1500) C842 for temperature compensation. The variable capacitor is tuned for maximum output in the center (31.9 Mc) of the band.

The VCO oscillation frequency is determined primarily by the elements between the collector transformer T808 and the emitter of transistor Q804 with crystal Y801 being the dominant element.

L808, L804, CV801, CV802, and C827 form a series resonant circuit, which has an effect on the VCO frequency by its phase shift. L808 is the

center frequency adjustment, and CV801 and CV802 are voltage controlled capacitors (reverse biased diodes) which provide dc control of the VCO frequency. C827 is a negative temperature coefficient capacitor (N750).

Auto-transformer, T807, transforms the crystal impedance to change VCO gain and it moves the position of the crystal impedance pole. By this means, the phase vs. frequency characteristic of the crystal can compensate for the non-linear voltage controlled capacitors thus giving a linear frequency vs. control voltage characteristic.

The buffer amplifier consists of Q805 and collector tuned circuit T809 and C839. The amplifier stage is neutralized with C843 allowing higher power gain and minimizing the effect of external signals entering the buffer amplifier on the VCO.

The rest of the circuitry in the module generates 74.7 Mc from the VCO and the external 21 Mc. Q803 is a tripler, with its collector tuned to 95.7 Mc. The collector transformer (T806) output is coupled through a double tuned circuit to the base of the mixer, Q802 (called the third mixer). The double tuned circuit reduces the undesired harmonics, especially the first and second, from the tripler.

The external 21 Mc signal is fed into the emitter of the mixer at a -6 dbm level. The collector of the mixer is tuned to the difference frequency 74.7 Mc.

The mixer output is filtered first through the double tuned circuit which includes T804 and T803, and then through the crystal filter FL803. This filtering reduces potentially troublesome, undesired mixer products. The crystal filter has a 6 kc 3 db bandwidth. Its 500 ohm input and output impedances are matched with T803 and T802. These two transformers are initially adjusted for maximum gain, then slightly readjusted for minimum ripple in the passband.

The signal presented to the base of output amplifier Q801 is about 300 mv rms (high impedance measurement). The stage is neutralized to obtain higher power gain and provides an output of about -10 dbm at 50 ohms.

## 4.6 - Voltage Controlled Oscillator (VCO) and Fourth Mixer

Figure 4.18 is a pictorial diagram and Figure 4.19 is the VCO and fourth mixer schematic. The VCO and its buffer amplifier are identical to those in the VCO module. The fourth mixer is a phase detector which compares the VCO frequency in this module with the frequency of the oscillator in the VCO module.

### Specifications

| | | |
|---|---|---|
| VCO frequency at 5 v input | 31.90000 Mc ± 100 cps at 25°C | |
| VCO frequency variation in the temperature range -20° to +55°C | less than $^{+400}_{-300}$ cps | |
| VCO gain | 950 ± 100 cps/volt | |
| VCO input range (E505) | 5 ± 3.0 v | |
| VCO buffer amplifier output level (P17B) | 1.0 dbm (> -1 dbm) | |
| VCO buffer amplifier output impedance | 50 ohms | |
| Δf (fourth mixer) output level (E507) | 3 v pp | |
| Δf output impedance | 50 k | |
| Δf 3 db bandwidth (without additional filtering) | 350 cps | |
| Δf input frequency (P19B) | 31.90000 Mc | |
| Δf input level | 230 mv rms | |
| Δf input impedance | 900 ohms | |
| Coupling through the phase detector | -60 db | |
| Power | 12 v | 4.5 ma |
| | 5 v | 0.13 ma |

### VCO and Fourth Mixer Circuit Description

Operation of the VCO (Q504) and its buffer amplifier (Q505) is the same as described for the VCO module in Section 4.5.

The buffer amplifier output from T509 drives the base of the phase detector amplifier, Q503, which is tuned to 31.9 Mc by selection of C512. The phase detector amplifier, in addition to gain, provides some isolation between the two VCO's and between the two second mixers (in the IF modules). R515 swamps out amplitude variations due to change of collector resistance or transformer Q with temperature and reduces the

sensitivity of the tuning peak to temperature. The amplified signal appears at the secondary of T502. This secondary is part of the phase detector.

The signal from the other VCO buffer amplifier (in the VCO module) is applied to the base of phase detector amplifier Q502. This amplifier is tuned by selection of C505, and provides isolation as well as amplification. The collector resistor, R514, makes the output less sensitive to temperature.

The signal from T502 and the signal from the upper half of the secondary of T501 are added and peak detected by diode CR501 and capacitor C508. The signal from T502 and the signal from the lower half of the secondary of T501, are added and peak detected by diode CR502 and capacitor C509. The diodes are polarized to give a positive voltage (relative to the 5 v supply) across C508, and a negative voltage across C509. The difference between these two peak detected voltages is obtained from the summing resistors R506 and R507.

The voltage across C508 is the most positive when the voltage across T502 and the upper half of T501 are in phase. Because of the phase reversal of the bottom half of T501, the sum of voltages across T502 and the bottom half of T501 is at a minimum. Therefore, the voltage across C509 is least negative, and the output of the summing resistors is positive. When the output of T502 shifts phase by half a cycle, the situation is reversed and the output of the summing resistors is negative.

## 4.7 - Loop Difference Amplifier

The loop difference amplifier is a feed back amplifier which provides dc gain and includes the lag-lead network for the phase lock loop. Figures 4.20 and 4.21 are pictures of the amplifiers and Figure 4.22 is the schematic.

Specifications

| | |
|---|---|
| DC gain | approx. 20 |
| DC offset at output (with input connected to the 5 v supply) | magnitude < 100 mv (relative to 5 v supply) |

| | | |
|---|---|---|
| Frequency of zero in response | | |
| for 423.3 Mc channel | | 8.1 cps |
| for 49.8 Mc channel | | 4.1 cps |
| Gain at 1 kc | | |
| for 423.3 Mc channel | | $9.4 \times 10^{-3}$ |
| for 49.8 Mc channel | | 0.113 |
| Input impedance (approx.) | | 25 k |
| Output impedance | | |
| at 1 kc | | 20 ohms |
| at dc | | 400 ohms |
| Amplifier open loop $g_m$ | | 75 mmho |
| Power | 12 v | 0.70 ma |
| | 5 v (no input signal) | 0.01 ma |

Loop Difference Amplifier Circuit Description

This amplifier is two cascaded difference amplifiers. The summing point for the feedback is the base of Q201. The output is fed back to the summing point through feedback elements R209, R206, C202 and C206. The input is connected to the summing point through R203.

$$\text{The dc gain} = \frac{R209}{R203}$$

$$\text{The frequency of zero in response} = \frac{1}{2\pi} \frac{1}{\frac{C202}{2}\left(R206 - \frac{1}{g_m \text{ of amplifier}}\right)}$$

$$\text{The gain at 1 kc} = \frac{R206 - \frac{1}{g_m \text{ of amplifier}}}{R203}$$

C202 and C206 are identical tantalums connected back to back to make a non-polar capacitor. See Appendix A.5 for the expressions used in selecting feedback component values.

The amplifier is designed to limit at $5 \pm 2$ v to prevent turning the VCO off with too large an input excursion, and to insure that the nominal 74.7 Mc signal is within the crystal filter passband (in the VCO module). The divider, R212 and R213, prevents the output from being less than 3 v. Current through emitter resistor of the output

stage, R211, is just enough to provide 7 v output with Q204 full on and Q203 off. Diodes CR203 and CR204 prevent voltage saturation of the input and the output stages when overdriven, and help to keep the output from exceeding 7 v.

One of the two diodes, CR201 and CR202, temperature compensates the base emitter diode of the output stage to keep the output stage operating point constant. The other diode temperature compensates the effect of base emitter diode of the input stage on the operating point of the output stage.

The input stage transistors are matched for base-emitter voltage within 5 mv over a temperature range of -20° to +60°C and within 10 percent for $h_{FE}$. The base current of Q202 will cause the same voltage drop across R208 as the base current of Q201 will across R203. The input stage is run at relatively low current (75 μa in each transistor) to minimize the effect of changes in base current. This current is large enough to drive the second stage even if the second stage transistors had an $h_{FE}$ of only 14.

The lag-lead network R210 and C203 is added for stability as is bypass capacitor C201. C204 is added across the output so that no load operation and operation when driving the 10 nf VCO capacitor will not be very different in terms of frequency breakpoints in the open loop response.

Loop stress is defined as the voltage at the input to the VCO, which is the output of the loop difference amplifier. The loop stress voltage which goes to the analog gate and gate selector for subcommutation is decoupled from the amplifier output by the low pass filter R214 and C205.

## 4.8 - IF Switch

The IF switch is a broad band, single pole, double throw switch, operating at a 50 ohm impedance level. The switch is controlled by a flip flop and an amplifier. Figure 4.23 is a picture of the switch portion and Figure 4.24 is the overall schematic. The flip flop portion is part of the circuit board in Figure 4.29.

Specifications

| | | |
|---|---|---|
| Switch closed insertion loss | | < 5 db |
| Switch open insertion loss | | > 70 db |
| Input impedance level | | |
| Switch closed | | 100 ohms |
| Switch open | | > 1 k |
| Control signal for switch | | |
| On | | 3 v at 1.7 ma |
| Off | | 0 v |
| Calibrate signal | | 10.5 v, 10 μs pulse |
| Reset signal | | 2 v, > 15 μs |
| Power | 5 v | 1.8 ma |

IF Switch Circuit Description

The circuit consists of two parts: the switch portion, which is in the upper half of the schematic, Figure 4.24; and the control portion, which is in the lower half of the schematic.

The switch is made of two identical sections, the right and the left halves. Normally, the switch control voltage at E221 is 0 v and at E222 is 3 v. In this state, the two series diodes, CR201 and CR202, are conducting 1.6 ma, their total series resistance is reduced to about 50 ohms and the left hand switch is conducting. The base of the shunt transistor, Q205, is biased to 0 v so it is not conducting. Coupling through the base collector capacity is bypassed by capacitor C203 to keep the signal off the control lead.

The right hand side of the switch is open. The series diodes, CR203 and CR204, are biased to zero volts and have an impedance of 2 to 3 pf each. The shunt transistor is biased on and looks like approximately 20 ohms. Bypassing and decoupling of the control leads reduces coupling around the switch through the control leads. Inductors L204 and L201 are added to provide a dc path to facilitate testing. The TI SM6316 transistor is a 2N2432 with a non-magnetic hat. This chopper type transistor has some reverse $h_{FE}$ and a lower saturation resistance than the Fairchild SP9458.

When the control voltage is reversed, the switch control voltage

at E221 is 3 v and at E222 is 0 v; the left hand switch changes from on to off, and the right hand switch changes from off to on.

The control flip flop is made up of Q202 and Q203. The calibrate pulse is amplified and coupled to the flip flop via trigger transistor Q201. The -3 v bias on the base of this transistor makes it less sensitive to noise. Resistor R201 limits the input pulse current and protects the trigger transistor. The flip flop is reset by the reset pulse at the base of Q204. The reset pulse is generated in the counter register.

The flip flop drives a saturating amplifier whose emitter resistor is, therefore, connected to either one side or the other of the switch control. The amplifier is necessary both to conserve current, and to drive the 10 nf bypass capacitors on the switch control lines.

## 4.9 - Modulation Phase Comparator

The modulation phase comparator measures the relative phase of two audio signals, either 7.692 or 8.692 kc. It consists of two phase locked loops for filters, and a phase to voltage converter. Figure 4.26 is the phase lock loop schematic, of which two are used; Figure 4.25 is a photo of the printed circuit. Figure 4.28 is the phase detector schematic and Figure 4.27 is a photo of the printed circuit.

Specifications

| | |
|---|---|
| Input frequency (E114) | 7.692 or 8.692 kc $\pm$ 2 cps |
| Input voltage level | 0.4 to 3 v pp |
| Input impedance | 50 k |
| Design level of spectral density of input noise, $N_o$, (one sided) | $3.1 \times 10^{-5}$ v/cps |
| Design signal level | 0.4 v pp |
| Loop noise bandwidth at design signal level, $B_L$, (at input to the synchronous detectors) | 67 cps |
| Loop 3 db bandwidth at design signal level | 42 cps |
| Phase detector filter 3 db bandwidth | 0.06 cps |

| | | |
|---|---|---|
| Rms phase error vs. signal level with design level noise present | | |
| 3 v pp signal level | | 0.17° rms |
| 1 v pp signal input level | | 0.5° rms |
| 0.4 v pp signal level | | 1.1° rms |
| Phase error vs. temperature -20° to +60°C | | < 3° |
| Output voltage (423.3 Mc channel is reference phase)(E112) | | |
| | | Linear from 0.2 to 2.8 v for 317° to 137°<br>Linear from 2.8 to 0.2 v for 137° to 317° |
| Output impedance | | 1 k |
| Output current (positive current is out of the output) | | -40 to +10 μa |
| 16.384 kc clock (input) | | 11 v, 2 μs pulses |
| Power | 12 v | 1.25 ma |
| | 5 v | 0.15 ma |
| | -3 v | 0.18 ma |

Modulation Phase Comparator - Section I. Circuit Description

The 10 to 1 voltage divider at the input R139 and R140 (Figure 4.26) provides a decoupled, relatively low impedance (10 k) loop phase detector output for the GSE (test) connector.

The input signal is filtered by an 8 kc center frequency band pass filter. The filter is made up of a high pass filter, R101 and C101, and a low pass filter R103 and C102, with the isolating emitter follower, Q101, in between. Both filters have 3 db points at 8 kc.

The modulation frequencies, 7.692 kc and 8.692 kc, were chosen to be, respectively, 500 cps below and above the mixer frequency, 8.192 kc. Thus, the output of the chopper type mixer, Q102, is 500 cps when either modulation frequency is present.

The 500 cps band pass filter following the mixer consists of a cascaded low pass and high pass filter. The mixer output drives the emitter follower, Q103, which drives the low pass filter R108 and C103. The low pass filter drives the emitter follower Q104 which drives the high pass filter C104 and R110.

The center frequency of the 500 cps filter for the 100A (49.8 Mc channel) board is 707 cps, which causes a phase shift of 19.6°. The center frequency of the 500 cps filter for the 100B (423.3 Mc channel) board is 328 cps, which causes a phase shift of -23.5°. The 49.8 Mc channel thus has a phase shift of +43° relative to the 423.3 Mc channel. This phase shift is added to move the 180° calibrate phase from the receiver output away from the 2.8 v corner of the triangular shaped phase detector output, for these corners become rounded in the presence of noise. Rounding begins about 30° from the corners at the design level of signal and noise.

The 500 cps filter output is amplified about 20 times by a feedback amplifier. The overall gain from input (E114) to output of the amplifier (emitter of Q107) is 2. The amplifier has a high pass 3 db point of about 320 cps, as determined by R114 and C105. It is made up of amplifiers Q105, Q106 and output emitter follower Q107. The feedback loop, R112 and R118, also determines the dc operating point of Q107.

The loop phase detector consists of the two synchronous detectors, Q109 and Q110. These chopper transistors are inverted to reduce their offset voltage and have a minimum reverse $h_{FE}$ of 4. They operate as half wave detectors 180° out of phase with each other by virtue of being switched from opposite sides of the 500 cps flip flop. The outputs drive opposite sides of the difference amplifier, Q112 and Q113. Between each detector and the input to the difference amplifier is a lag-lead network which controls the bandwidth of the phase lock loop. R124, R126 and C111 comprise one lag-lead network and R127, R129 and C112 comprise the other. Since the reverse voltage developed across C111 and C112 is considerably less than 0.1 v, ordinary polar tantalum capacitors are used.

The difference amplifier controls the frequency of an astable multivibrator (the VCO) by changing the voltage applied to the base resistors. Resistor R137 is selected to make the VCO operate at exactly 1 kc.

The 1 kc VCO signal then drives the 500 cps flip flop. The flip flop output swings between 0 v and about 10 v, and is dc coupled to the

synchronous detectors. The flip flop output is exactly symmetrical; therefore, the transitions of the flip flop correspond exactly to the 90° and 270° phase points of the input to the phase lock loop (assuming zero phase error). This phase relationship makes the phase detector relatively simple.

Modulation Phase Comparator - Section II. Circuit Description

Figure 4.28 is the schematic diagram. The phase detector is a NAND gate, made up of Q104 and Q105. The signal from the 500 cps flip flop in each of the two phase lock loop channels is ac coupled to one of the NAND gate inputs. The ac coupling allows the phase detector to operate at ground level. As the phase changes, the NAND gate conduction time will vary between being continuously on (0 v output) to being on half the time (3 v output). The voltage divider R114 and R115 provides a 6 v source, which averages to 3 v when conducted to ground half the time by the NAND gate.

A low output impedance is provided for the NAND gate output by NPN emitter follower Q106. Q107 acts as a constant current source for the emitter follower. The .06 cps low pass filter, R117 and C108, removes 500 cps pulsations from the NAND gate output, and filters out most of the rms phase error due to noise from the phase lock loops.

PNP emitter follower Q108 provides approximately a 1 k output impedance and its base-emitter voltage nearly cancels that of the previous NPN emitter follower Q106. The output emitter follower can only supply current flowing into the emitter follower. This is the correct polarity for the spacecraft load. Base resistor R119 and collector resistor R122 are current limiting resistors to protect Q108 and C108 if the output should be connected to an incorrect voltage.

The 8.192 kc square wave for the 8 kc converter is derived from the flip flop, Q102 and Q103. This flip flop converts the spacecraft pulse train into a signal for the two 8 kc mixers which are driven from opposite sides of the flip flop.

A 16.384 kc, 11 v, 2 μs pulse from the spacecraft drives the flip flop trigger amplifier. To improve noise immunity, the amplifier is biased to 5 v, which the input signal must overcome before causing it

to trigger. The series base resistor, R101, limits base current.

## 4.10 - Analog Gates and Gate Selector

The carrier amplitude (amplitude phase detector output) and the loop stress (VCO control voltage) from each channel are subcommutated onto one subcom output for each channel. The subcommutated voltages are translated from a 5 v reference to a normalized 0 to 3 v output. The state of the subcommutator alternates with the scientific subframe rate pulse. The reset pulse maintains subcommutator synchronization with the spacecraft data format.

Figure 4.29 is a photo of the printed circuit and Figure 4.30 is the schematic.

### Specifications

49.8 Mc channel carrier amplitude and loop stress are subcommutated onto one output (scientific subcom word no. 2)

423.3 Mc channel carrier amplitude and loop stress are subcommutated onto one output (scientific subcom word no. 11)

| | |
|---|---|
| Carrier amplitude input | 5 v to 3.5 v |
| Corresponding subcom output (with Thevenin equivalent = 4.75 v, 465 k of output load connected) | 0.2 v to 2.85 v |
| Loop stress input | 7 v to 3 v |
| Corresponding subcom output (with output load Thevenin equivalent = 4.75 v, 465 k) | 0.2 v to 3 v |
| Subcom output impedance | 11 k |
| Scientific subframe rate pulse input (subcommutate pulse) | 11 v, 10 μs |
| Reset pulse | 2 v, > 15 μs |

### Analog Gates and Gate Selector Circuit Description

The gates are on the left of the schematic, Figure 4.30. The gates at the top and at the bottom of the schematic are identical.

A simplified diagram of a single gate is shown in Figure 4.1, with the gate on. The base emitter voltages of the NPN Q1, and PNP Q2 emitter followers approximately cancel, so the emitter voltage of Q2 is nearly the same as the input. Since 99 percent of the emitter current of Q2

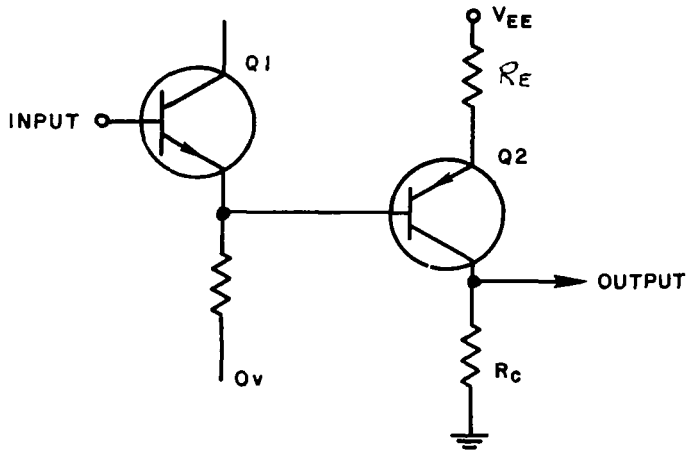



Figure 4.1 - Simplified Schematic of a Single Gate

comes out of its collector, the voltage gain of the gate is $R_C/R_E$. The output is 0 v when the input = $V_{EE}$ and increases positively, as the input increases negatively from $V_{EE}$. Transmission through the gate is inhibited if the voltage at the bottom of the emitter resistor of Q1 is made more positive than $V_{EE}$.

The loop stress gate and the carrier amplitude gate share a common output collector resistor. Since only one of these two gates is on at a time, the subcommutated output is taken at this resistor.

The loop stress gate has a gain factor of 0.75, and a $V_{EE}$ of 7 v. The output is 0 v for an input of 7 v and the output is 3 v for an input of 3 v. The amplitude phase detector gate has a gain factor of 1.75, and a $V_{EE}$ of 5 v. The output is 0 v for an input of 5 v and is 2.85 v for an input of 3.5 v. A 0.3 cps 3 db point low pass filter (R201 and C203, R202 and C202) averages out variations in the carrier amplitude signal. The variations occur because nulls in the antenna pattern amplitude modulate the signal as the spacecraft rotates at 1 cps.

The gates are controlled by the flip flop, Q209 and Q210. It has an output of either 0 v or 10 v, and drives the emitter resistor of the

first emitter follower of the gates. The two gates which share the same output are connected to opposite sides of the flip flop. The scientific subframe pulse drives the count input of the flip flop through amplifier Q211. The base of amplifier Q211 is biased at -3 v to prevent triggering on noise. R218 limits the input pulse current and the amplifier output is only 6 v to prevent exceeding the 5 v base-emitter reverse voltage rating of the flip flop transistors.

The reset amplifier, Q212, requires a 2 v pulse. The reset pulse occurs simultaneously with each fourth scientific subframe rate pulse, and lasts longer than the subframe rate pulse to insure resetting. The carrier amplitude is connected through the gates to the subcom output after the reset pulse.

## 4.11 - Counter Register

The schematics of the counter register are shown in Figures 4.33 and 4.35. Photographs of the printed circuit boards are presented in Figure 4.32, and Figures 4.31 and 4.34 are related schematics.

The counter register accumulates cycles of $\Delta f$ from the $\Delta f$ phase detector in a 10 bit counter. The counter contents are non destructively parallel shifted into a serial shift register every alternate frame rate pulse. By command of the word gate, once each frame, six bits are serially shifted out of the shift register. Synchronism of the parallel shift with the spacecraft format is accomplished by the engineering subframe pulse (which occurs once every 64 frames).

Specifications

| | |
|---|---|
| $\Delta f$ input amplitude (E309) | 5 v $\pm$ 2.5 v |
| $\Delta f$ trigger levels | 5 v $\pm$ 0.4 v |
| $\Delta f$ input impedance | 0.047 μf in parallel with 500 k |
| $\Delta f$ input 3 db bandwidth (with the 50 k source impedance of the $\Delta f$ phase detector) | 70 cps |
| Engineering sub-frame pulse input | 11 v, 10 μs |
| Frame rate pulse input | 11 v, 10 μs |
| Shift pulse input | 11 v, 10 μs |

| | |
|---|---|
| Word gate input | 10 v on<br>0 v off |
| Digital output | 10 v, 10 μs pulse for binary one<br>0 v for binary zero |

Order of output - During the first word gate after the engineering sub-frame pulse, the higher order six bits of the counter are shifted out, highest order bit first. During the second word gate after the engineering sub-frame pulse, the lower order four bits are shifted out, highest order bit first, followed by two dummy zeros. This pattern repeats with successive word gates.

Counter Register Circuit Description

Most of the counter register is made of Texas Instrument, SNR51, integrated circuits in order to save weight. The SNR51 circuits were employed because they used less power than other integrated circuits available at the time.

As shown in Figure 4.35, the Δf input is first filtered with capacitor C304. Combined with the 50 k source impedance, this capacitor makes a low pass filter having a 3 db bandwidth of 70 cps. The emitter coupled, Schmitt trigger has an 0.8 v hysteresis which is centered on 5 v. Emitter follower, Q305, provides additional power for the positive going output to drive the input of the $\frac{1}{2}$N301H ($\frac{1}{2}$SNR514), a single transistor amplifier which is used to drive the first SNR510 flip flop in the counter chain.

Five circuit boards (A through E) constitute the 10 bit counter and 10 bit serial shift register with each board containing a two bit counter and two bit serial shift register. One flip flop directly drives the clock pulse input of the following stage. The counter is a single stage shift register with its output crossed and fed back into itself. The preset input of the counter flip flop is grounded to prevent amplification of $I_{co}$ in the preset transistor, and to prevent extraneous conducting paths to the preset input from causing false triggering.

The serial shift register also consists of SNR510 flip flops. A negative step on the clock pulse input shifts the contents one place to the right. The input of the left most shift register, Figure 4.35, is

connected to binary zero. As bits are shifted to the right, zeros take their place and, after 10 shifts, the serial shift register contains all zeros.

With the serial shift register in the "all zero" condition, the parallel shift of binary ones from the counter is possible without having to provide a parallel shift for binary zeros. If the counter flip flop is in a one state at Q = 2 v, $\overline{Q}$ = 0 v, a parallel shift pulse into the parallel shift gate ($\frac{1}{2}$SNR514) sets the serial shift register to binary one (Q = 0 v, $\overline{Q}$ = 2 v). Note the definition of binary one in the counter is opposite to its definition in the serial shift register.

The shift pulses are a continuous, uniformly spaced, string with every seventh pulse missing (see Figure B - 2). The word gate brackets the group of 6 bit pulses which are to be used to serially shift the contents out to the spacecraft. The gated shift pulses are obtained by ANDing the shift pulses with the word gate. The AND gate is made up of Q303 and Q302, which are connected in series. Shift pulses cannot get through when the word gate is at 0 v, but can get through with the word gate at 10 v. The emitter of the shift pulse AND gate transistor, Q303, is biased to 2.5 v to prevent noise up to about 5 v on the shift pulse input from getting through, and to prevent a signal of up to 2.5 v on the word gate input from letting shift pulses through. The negative pulse developed by the AND gate is ac coupled to the non-inverting power amplifier, N301G, (SNR517) which in turn drives the serial shift line of the serial shift register with negative going pulses (2 v to 0 v).

The output of the 10 bit serial shift register drives input resistor R318 of the output pulse amplifier, Q306 and Q307. The capacitor, C309, is driven from the serial shift pulse line. When a binary zero is shifted out, the input to R318 is at 2 v, which reverse biases diode CR303 and prevents the negative going shift pulse from passing through. For a binary one, the input to R318 is 0 v, which biases the diode to 0 v. Now the negative going shift pulse is conducted through the diode and turns off amplifier Q306. The collector output of Q306 is power amplified by emitter follower Q307 to provide a short rise time. At the end of the shift pulse, Q306 is turned on.

The collector of Q306 is connected to the output through diode CR404, which provides a short fall time. The pulse generator output is ac coupled to the digital output terminal to prevent damage to the output circuitry should the digital output be shorted or connected to a dc voltage.

The parallel shift pulse occurs with alternate frame rate pulses. The frame rate pulse is amplified by N301H ($\frac{1}{2}$ SNR514) which drives the clock pulse input of counter N302F (SNR510). The counter output is differentiated by C310 and R320, and power amplified by the pulse amplifier N303F (SNR517). The N303F pulse amplifier drives the parallel shift line with a negative going pulse (2 v to 0 v).

The reset pulse circuit is made from the two halves of N301F (SN514A), connected as a flip flop, with dc inputs on both sides. The engineering sub frame pulse sets the flip flop so the reset output is at 2 v. One bit time later, the shift pulse resets the flip flop so the reset output is at 0 v. There is no shift pulse when the engineering sub frame rate pulse occurs.

The three external pulses drive the SN514A inputs through voltage dividers, which reduce the pulses to the voltage level required, limit the input current, and raise the input threshold from 0.6 v to about 2.5 v.

## 4.12 - Sample and Hold

Figure 4.36 is a photo and Figure 4.37 is a schematic of the sample and hold circuit.

The two amplitude phase detector outputs provide the two inputs to the sample and hold circuit. Each input is sampled alternately at the word pulse time, and the instantaneous amplitude held (up to 1 second) to give the spacecraft analog to digital converter time to convert. The sun pulse causes the sample and hold output to be 0 v for 30 ms (= 2 word times), when the spacecraft is operating at 512 bps. The sun pulse marks the time when the spacecraft is at a known angular position relative to the sun.

Specifications

| | |
|---|---|
| Input voltage level | 5 v to 3.5 v |
| Input 3 db bandwidth, with 1 k source impedance of the amplitude phase detector output | 10 cps |
| Input impedance | 15 μf |
| Output voltage level (with 4.75 v 4.65 k Thevenin equivalent output load) | 0.2 v to 2.9 v, corresponding to an input of 5 v to 3.5 v respectively |
| Hold voltage drift rate | < 0.07 v/sec |
| Output impedance | 11 k |
| Hold amplifier gain | 1.00 |
| Level transfer circuit gain | 1.87 |
| Word rate pulse | 11 v, 10 μs |
| Reset input | 0 v to 2 v pulse, > 15 μs |

The reset pulse causes the 423.3 Mc channel amplitude phase detector to be sampled if the word pulse occurs simultaneously.

| | |
|---|---|
| Sun pulse input | 10 v, 10 μs |
| Bit rate 512 level input | 9 v when on<br>0 v when off |
| Effect of sun pulse, with bit rate 512 input on. This effect is inhibited with the bit rate 512 input off. | Output voltage clamped to 0.2 v for 30 ms after the sun pulse |

Sample and Hold Circuit Description

The word rate pulse is amplified by Q202, which triggers the 0.5 ms one shot and the flip flop. The input to this trigger amplifier is biased to -3 v, to provide about 4 v of noise immunity. Resistor R204 is connected in series with the trigger transistor base to limit current.

The 0.5 ms one shot, Q204 and Q206, is standard, with the addition of negative bias on the quiescently off transistor, Q204. This bias eliminates the effect of 0.2 v pulses which feed through from the trigger input to the base of Q204, via the base-collector capacities.

Amplifier Q201 resets the flip flop when the reset pulse changes

from 0 v to 2 v. This resetting keeps the subcommutator flip flop in synchronism with the spacecraft data format. The reset pulse is long enough (> 1.9 ms) to overcome the effect of the simultaneous word rate pulse. The first word after the reset will be from the 423.3 Mc channel.

The flip flop is triggered simultaneously with the 0.5 ms one shot and its outputs are individually NANDed with the one shot output in the NAND gates Q207 and Q208. The flip flop output to the selected NAND gate is 0 v, and to the unselected NAND gate is 3.5 v. The one shot input to the NAND gates goes from 3.5 v to 0 v for 0.5 ms which allows the selected NAND gate output to go positive for 0.5 ms. This positive output makes the sample gate transistor Q209 or Q210 conduct. The sample gate transistor has a reverse $h_{FE}$ of about 3, so that current can flow either way through it.

In less than 0.3 ms, the 0.1 μf capacitor, C208, (mylar for low soakage) is brought to within 10 mv of the input. The offset is 10 mv or less because of the sample gate transistor reverse $h_{FE}$. The 15 μf input capacitors, C206 and C207, provide an instantaneous source of charge for the hold capacitor while lowering the 3 db bandwidth to 10 cps (the input has a 1 k source impedance).

The gate transistors are connected in the forward (high $h_{FE}$) direction to make the hold capacitor (C208) voltage go negative. Hence, the hold capacitor voltage can go negative more quickly than it can go positive. Due to inversion by the transfer circuit, Q222, the output goes positive more quickly than it goes negative. The A-D converter required that for inputs > 1.5 v (half scale), its input must exceed 1.5 v less than 120 μs after the word rate pulse. For inputs < 1.5 v, the input can take as long as 1 ms to become less than 1.5 v.

The hold amplifier is a unity feed back amplifier made up of two cascaded difference amplifiers. The first stage has low input current (< 3 na) to keep from discharging the hold capacitor too quickly. The hold capacitor is as large as practicable to minimize the effect of the input current. The input stage consists of emitter followers, Q214 and Q215, driving the difference amplifier, Q216 and Q217. The emitter follower has the 44 M emitter resistor to decrease the transient response

time, although this increases the input current. Q214 and Q215 are a matched pair as are Q216 and Q217. They are matched within 5 mv for base-emitter voltage over a temperature range from -20° to +60°C, matched for $h_{FE}$ within 10 percent and are high $h_{FE}$ units (> 150 at 0.1 ma). The difference amplifier is run at only 2 μa per transistor to further reduce input current.

One of the two diodes CR205 and CR206 temperature compensates for the base-emitter diode of the second stage, Q219 and Q220. The other diode compensates for the effect that the base-emitter diodes of the first stage have on the operating point of the second stage.

The output of the second stage is connected through emitter follower Q222 to the feedback point of the input stage, the base of Q215. Thus, the voltage at the base of Q215 is the same (within 10 mv) as the hold capacitor voltage (base of Q214). The voltage across emitter resistor R241 is the same as on the hold capacitor. All the current through R241 goes into the emitter of Q222, and 99 percent comes out of the collector of Q222. The emitter voltage of Q222 is, therefore, transferred to its collector resistor with a gain of R242/R241 and is the Format D output voltage.

The sun pulse and the 512 bps state are ANDed in the gate made up of Q211 and Q212. With the 512 bps state below about 5 v, the current through R222 due to the sun pulse gets shunted through Q211 to ground. With the 512 bps state above 5 v, the current will go through Q212 and trigger the 30 ms one shot. R203 in series with the base of Q211 insures the input impedance will be greater than the 48 k required for this line, and protects Q211 from accidental excessive base current. Bypass capacitor C205 provides an instantaneous low source impedance for the base of Q211. R221 helps to discharge the diode OR gate output in the spacecraft, which drives the sun pulse line but has no return to ground. CR203 and CR204 prevent the 5 v base-emitter reverse breakdown voltage from being exceeded.

The 30 ms one shot is standard, except that negative bias is supplied to the normally off transistor, Q213, to keep the 0.2 v pulses fed through the gate from having any effect. The timing capacitor C209

is mylar to enhance temperature stability. The sun pulse clamp, Q221, clamps the Format D output to about 0.2 v for the duration of the 30 ms one shot pulse. R202 protects the clamp transistor should the output be inadvertently connected to an improper voltage.

## 4.13 - Power Converter

The power converter provides four voltages for the receiver from the nominally 28 v supply. It is a regulated blocking oscillator, followed by a series regulator for two of the voltages. It also provides dc isolation between primary and secondary power. Figure 4.38 is a photograph and the schematic is shown in Figure 4.39.

Specifications

| | |
|---|---|
| Output voltages | 12 v, 5 v, 2.5 v, -3 v |
| 12 v output current | 78 ma |
| 12 v output noise voltage | 8 mv pp[1] + 120 mv pp<br>0.1 μs converter spikes |
| 12 v output change for a shift in input from 24 to 33 v | < 0.5 mv |
| 5 v output current | 4.5 ma |
| 5 v output noise voltage | 40 mv pp[1] + 150 mv pp<br>0.1 μs converter spikes |
| 5 v output change for a shift in input from 24 to 33 v | < 0.5 mv |
| 2.5 v output current | 22 ma |
| 2.5 v output noise voltage | 7 mv pp + 150 mv pp<br>0.1 μs converter spikes |
| 2.5 v output change for a shift in input from 24 to 33 v | 100 mv |
| -3 v output current | 0.2 ma |
| -3 v output noise output | 3 mv pp + 110 mv pp<br>0.1 μs converter spikes |

[1] All but 1 mv of this noise is caused by the receiver load and is predominantly 7 Mc.

| | |
|---|---|
| -3 v output change for a shift in input from 24 to 33 v | 100 mv |
| Input voltage, required | 23 to 34 v |
| Input voltage, typical | 16 to 55 v. Loses regulation below 16 v, but nothing is damaged |
| Input power (for the load currents indicated) | 1.4 w, independent of input voltage |
| Efficiency | 73.3 percent |
| Turn on surge | 250 ma for 10 ms |
| Noise voltage developed across primary supply (28 v), 13 ohms source impedance | 10 mv pp |
| Converter operating frequency | 30 to 35 kc |

Input transient pulses: The converter can survive spikes added to the supply voltage which give a peak input voltage of 50 v, 10 ms wide, at 10 cps.

| | |
|---|---|
| Weight | 0.15 lbs |

Power Converter Circuit Description

The principle parts of the power converter are the current limiter, the input filter, the regulated blocking oscillator converter and the output series regulator.

The current limiter consists of Q404, its 3.3 ohm emitter resistor made up of R405, R406 and R407, and diodes CR405 and CR406. In the current limiting state, the emitter resistor voltage drop (at $I_E$ = 250 ma) equals the voltage drop across one of the diodes (about 0.7 v). Transistor Q404 is held out of saturation by negative feedback through the diodes to its base. The other diode compensates for the base-emitter diode. The current limiting transistor saturates for currents less than 250 ma.

Before the converter is running, the current limiter base current is supplied from the voltage at the collector of Q404 through the non-active 2.6 v transformer winding, diode CR407, and base current limiting resistor R408. After the converter is running and the current limiter transistor is saturated; base current is provided by the 2.6 v supply from the converter. This scheme uses less power than a resistor from the +28 v line to the base of Q404.

The main $\pi$ input filter, consisting of C401, L401 and C404, is designed to keep the blocking oscillator transients from the 28 v line. C404 provides the instantaneous current pulses required by the blocking oscillator. In addition, a filter consisting of a 10 nf capacitor (mounted in frame B) and a ferrite shielding bead is installed in each side of the 28 v line to reduce a damped 8 Mc converter spike to 5 to 10 mv (across a 13 ohm source). The converter spike is due to leakage inductance when the blocking oscillator transistor turns off.

The blocking oscillator consists of Q403 and T401. The feedback winding to the base comes out at terminals 9 and 10. During the transistor on portion of the cycle, current builds up in the transformer and collector of the transistor. When the collector current exceeds $h_{FE}$ x (base current), the transistor turns off. During the transistor off portion of the cycle, the flux in the transformer causes current to flow through all the diodes connected to the transformer. This is a form of the switching regulator. The 2N3037 is used for the blocking oscillator because of its high collector-base voltage rating (120 v), low saturation voltage (0.35 v), and high frequency response (fall time $< 0.2$ $\mu$s). The blocking oscillator regulator output voltages are controlled by adjustment of the average blocking oscillator base current. The control winding (terminals 8 and 10) provides the voltage that is regulated. All the other output voltages are related to the voltage in the control winding by their turns ratio.

The control voltage (approximately 10 v across C403) is matched with the voltage drops across the diode CR403, zener diode CR402, and the base emitter diodes of Q402 and Q401. Any difference in voltage between these diode voltages and the control voltage causes amplifier Q402, Q401 to conduct either more or less current through the collector of Q401. This collector current is the average base current for the blocking oscillator. Q401 looks like an emitter follower, but is actually a common emitter stage. Note also that the emitter of Q401 is more negative than its collector.

Q402 is an emitter follower to increase the $h_{FE}$ of the combination Q402 and Q401. R419 and C413 are a lag-lead network for stability. The

control voltage filter capacitor is relatively small to minimize response time. R403 provides some current load (about 2 ma) for the reference supply and R404 reduces the effect of the spike due to leakage inductance. Both were selected in the design to make the output voltage as constant as possible with input voltage change. Diode CR401 prevents Q401 from saturating in reverse connection during turn on. This saturated transistor would clamp the base and the emitter of the blocking oscillator together through the transformer windings 9 and 10, and keep the blocking oscillator from starting.

The receiver VCO is very sensitive to low frequency (0 to 50 cps) noise on the 5 and 12 v lines. Voltage steps of only 0.8 mv cause the same response as a phase step of .5 radian. Larger signals cause loss of lock. The blocking oscillator regulator reduces a 9 v step (from 24 to 33 v) at the primary power input, to about 100 mv at the input to the series regulator. The series regulator further reduces this 100 mv to much better than 0.5 mv.

The 5 v is derived from the 12 v supply through a 7 v zener diode. The effect of a step on the 5 and 12 v power supply lines of the VCO are opposite and roughly equal. The two supplies change together through the zener diode so that the effect of power supply changes on the VCO, approximately cancel.

With a loop voltage gain of over 1000 a change at the series regulator input is reduced by a factor of about 100 at the output. The major cause of this relatively poor performance is that the change signal appears in the feedback loop at the base of Q405 due to the finite collector impedance of Q407. The addition of R420, which provides a signal of opposite phase, and is selected to give minimum output response to a step, improves performance by a factor of 3 to 10. The difference amplifiers, Q407 and Q408, are matched for base-emitter voltage to within 5 mv over -20° to +60°C.

The temperature compensated, voltage, reference diode, CR411, is bypassed by C410 to reduce the several millivolt zener noise. R411 is a starting resistor, without which the output of the series regulator would remain at 0 v. The high loop gain of the regulator results in a

low output impedance, which reduces the shunting effect of R411 to a negligible value. R411 also conducts part of the load current, reducing the load on Q406.

R416 prevents accidental shorts of the 5 v or 12 v supplies from burning out Q405 or the base-emitter junction of Q406. Similar protection could have been achieved by connecting the collectors of Q405 and Q406 together, but then the input to the series regulator would have to be 0.6 v larger to take care of the additional base-emitter drop of Q405. This would have used more power. Q406 is a 2N2907A in a non-magnetic hat. It was selected for its 600 ma current rating for use as the series regulator at 85 ma.

LIST OF MAIN SCHEMATICS



SPECIAL TRANSISTOR EQUIVALENCE TABLE

| Non-magnetic hat version | Standard version | Manufacturer |
|---|---|---|
| S7200 | 2N915 | Fairchild |
| S7201 | 2N918 | Fairchild |
| SP9458-2 | 2N2483 | Fairchild |
| SM6316 | 2N2432 | TI |
| SM6415 | 2N2861 | TI |
| SM3577 | 2N2907A | Motorola |

The printed circuits are labeled: "Wiring Side. Components are as seen through wiring side." The components side of these circuits are foamed. So the circuits are shown from the wiring side, with the components superimposed to show their location for circuit tracing. Since the printed circuits are identical on both sides, this was achieved by printing photographs of the components side backwards.

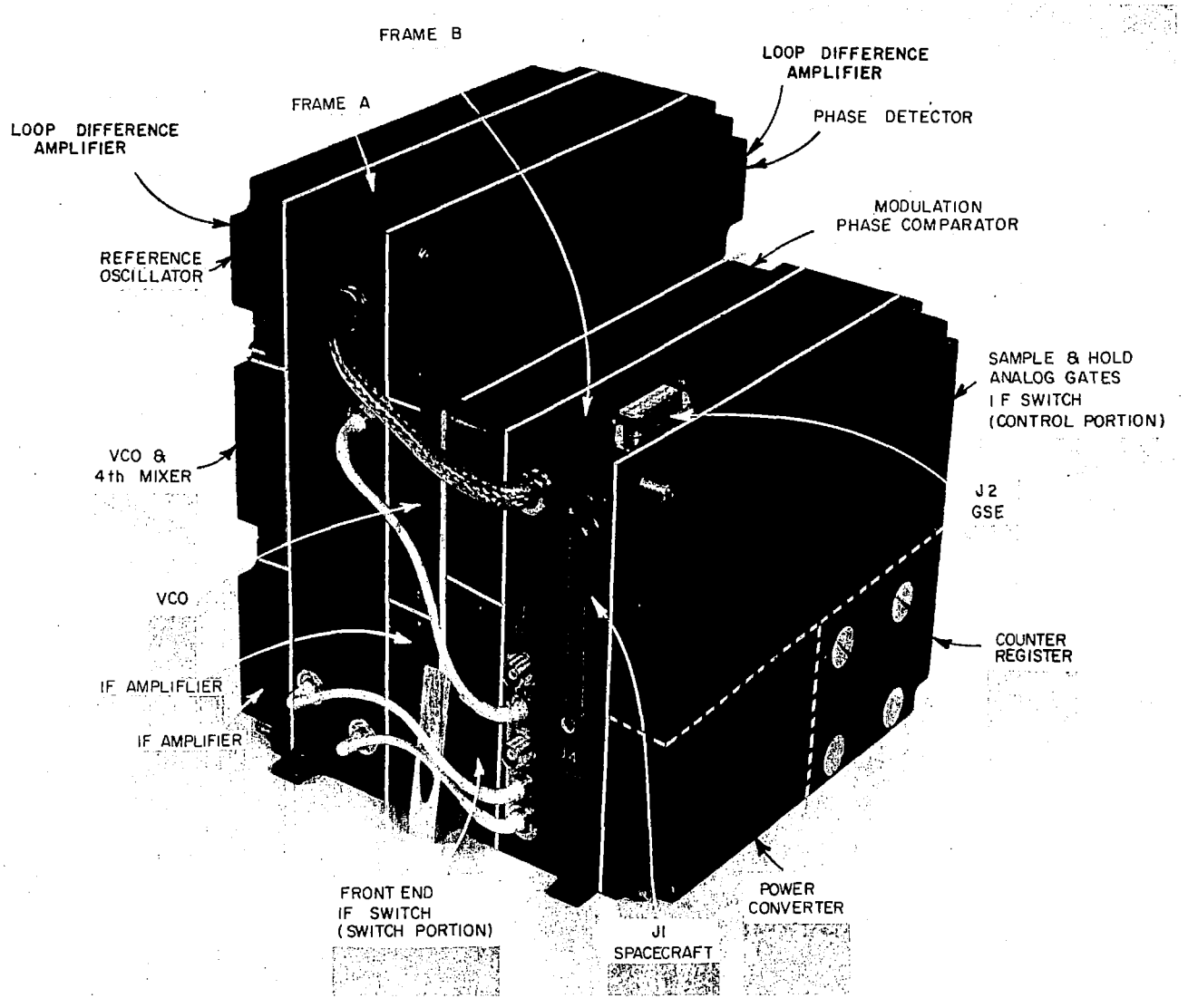



Figure 4.2 - Location of the Subassemblies in the Receiver

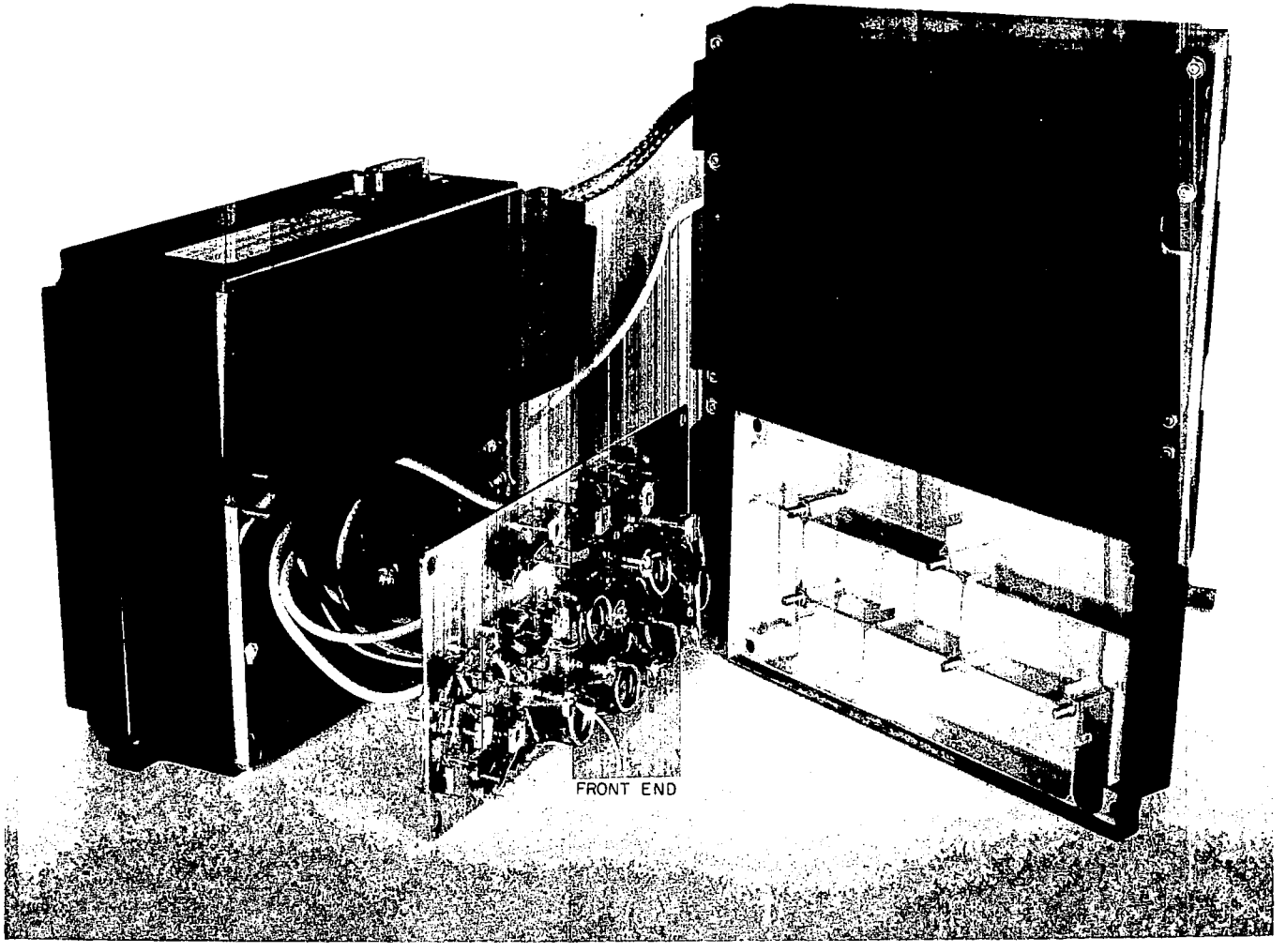



Figure 4.3 - The Front End with the Cover Off
This welded connection circuitry and shielding covers is typical of all the STL modules.

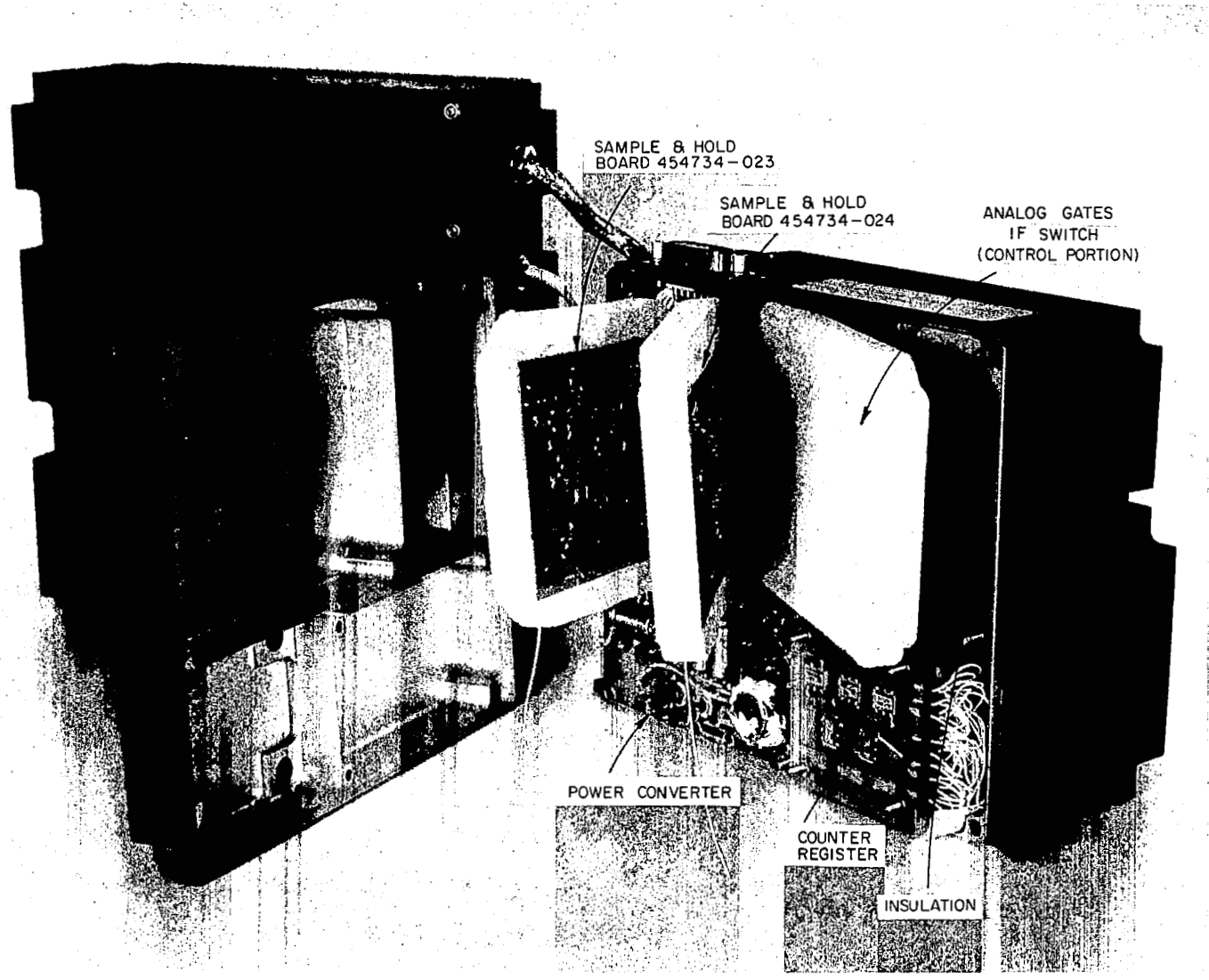



Figure 4.4 - Location of the Subassemblies under the Large Cover of Frame B

...semblies under the Small Covers of Frame B

SPACECRAFT CONNECTOR J 1

| PIN NO. | FUNCTION | CONNECTS TO |
|---|---|---|
| 1 | +28 v dc spacecraft power in | Power converter |
| 2 | Return 1 | Power converter |
| 3 | Chassis ground | |
| 4 | Chassis ground | |
| 5 | Frame rate pulse | Counter register |
| 6 | Eng. sub frame rate pulse | Counter register |
| 7 | Chassis ground | |
| 8 | Shift pulse | Counter register |
| 9 | Word rate pulse | Sample and hold |
| 10 | Chassis ground | |
| 11 | Return 29, 30 | Ground |
| 12 | Chassis ground | |
| 13 | Return 32 | Ground |
| 14 | Chassis ground | |
| 15 | Format D analog output | Sample and hold |
| 16 | Sci. subcom analog out (words E7 and E15)(Modulation phase) | Mod. phase comp. II |
| 17 | Analog out sci. subcom word 2 (49.8 Mc carrier ampl. and loop stress) | Analog gates |
| 18 | Chassis ground | |
| 19 | Digital output (counter out) | Counter register |
| 20 | Sun pulse | Sample and hold |
| 21 | Return 20 | Ground |
| 22 | 16.384 kc clock pulse | Mod. phase comp. II |
| 23 | Return 22 | Ground |
| 24 | Return 5, 6, 8, 9, 25 | Ground |
| 25 | Sci. sub frame rate pulse | Analog gates |
| 26 | Word gate | Counter register |
| 27 | Return 26 | Ground |
| 28 | Chassis ground | |
| 29 | 512 bps state | Sample and hold |
| 30 | Format D state | No connection |
| 31 | Chassis ground | |
| 32 | Calibrate pulse | IF switch |
| 33 | Chassis ground | |
| 34 | Return 15, 16, 17, 35 | Ground |
| 35 | Analog out sci. subcom word 11 (423.3 Mc carrier ampl. and loop stress) | Analog gates |
| 36 | Chassis Ground | |
| 37 | Return 19 | Ground |

Note: All Returns, except Return 1, are connected to Chassis Ground.

Table 4.1 - Pin Connections for the External Connectors

GSE CONNECTOR J 2

| PIN NO. | FUNCTION | CONNECTS TO |
|---|---|---|
| 1 | +12 v | Power Converter |
| 2 | +2.5 v | Power Converter |
| 3 | Chassis ground | |
| 4 | Analog out sci. subcom word 2 (49.8 Mc carrier ampl. and loop stress) | Analog gates |
| 5 | Format D analog output | Sample and hold |
| 6 | 423.3 Mc loop phase det. x 1/10 | Mod. phase det. I (100B) |
| 7 | Word gate | J 1; counter register |
| 8 | Eng. sub frame rate pulse | J 1; counter register |
| 9 | +5 v | Power converter |
| 10 | -3 v | Power converter |
| 11 | Analog out sci. subcom word 11 (423.3 Mc carrier ampl. and loop stress) | Analog gates |
| 12 | Sci. subcom analog out (words E7 and E15)(Modulation phase) | Mod. phase comp. II |
| 13 | 49.8 Mc loop phase det. x 1/10 | Mod. phase det. I (100A) |
| 14 | Digital output (counter out) | Counter register |
| 15 | Shift pulse | J 1; counter register |

J 3 ANTENNA CONNECTOR

| FUNCTION | CONNECTS TO |
|---|---|
| 49.8 Mc antenna input | Front end |

J 4 ANTENNA CONNECTOR

| FUNCTION | CONNECTS TO |
|---|---|
| 423.3 Mc antenna input | Front end |

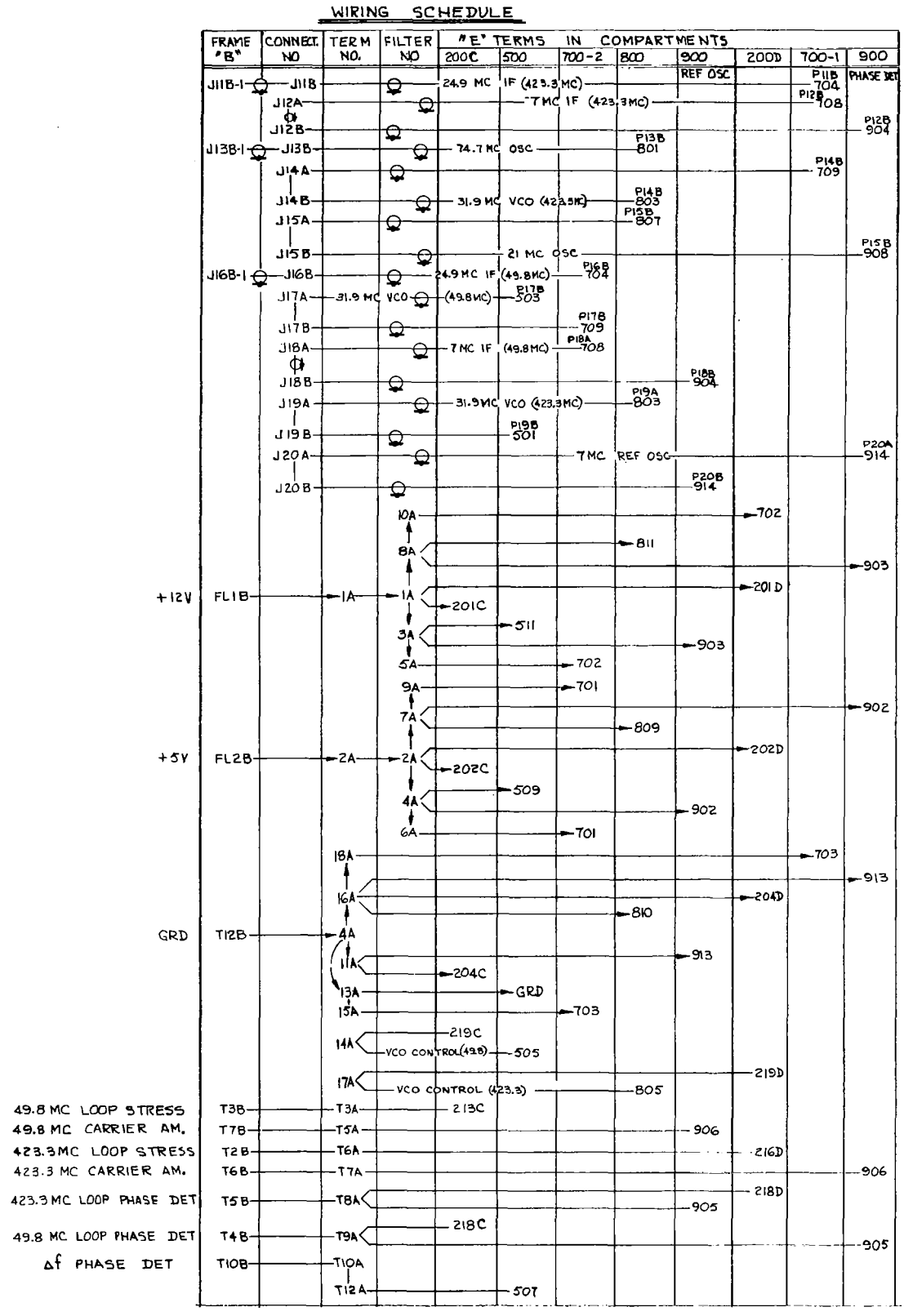
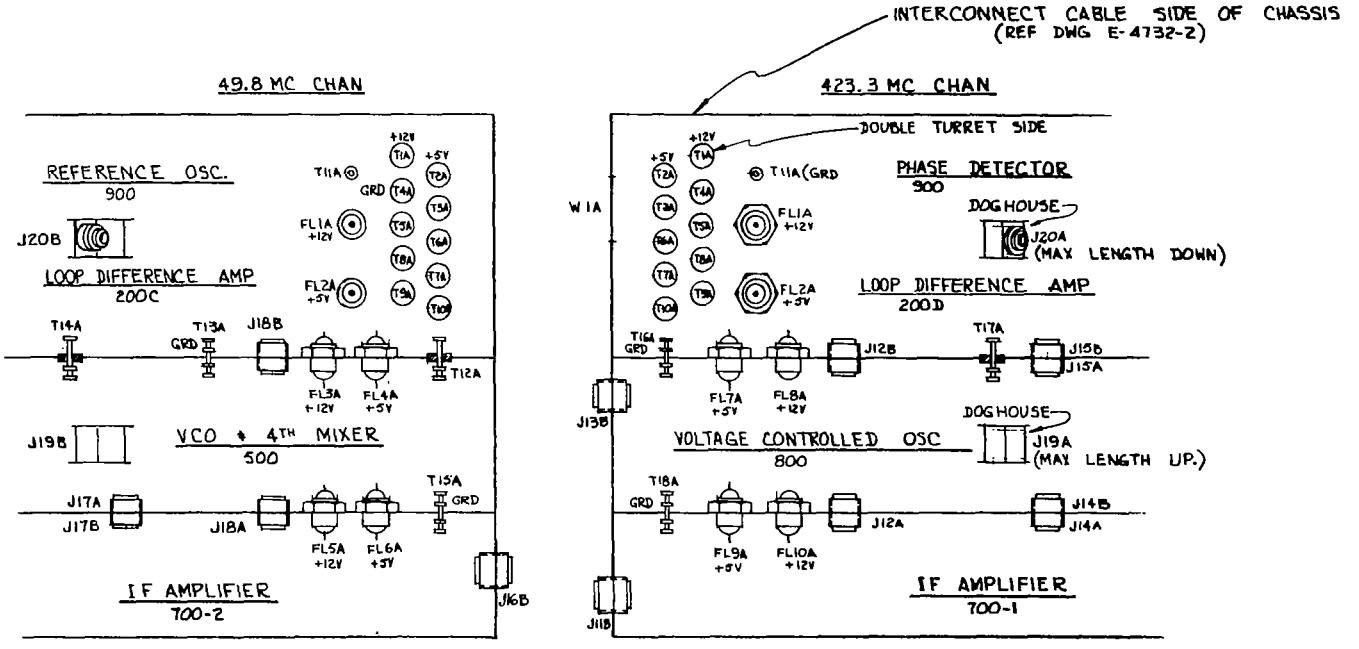



Figure 4.6 - Frame A Wiring Diagram




PHYSICAL LOCATION OF WIRING COMPONENTS
(NO SCALE)

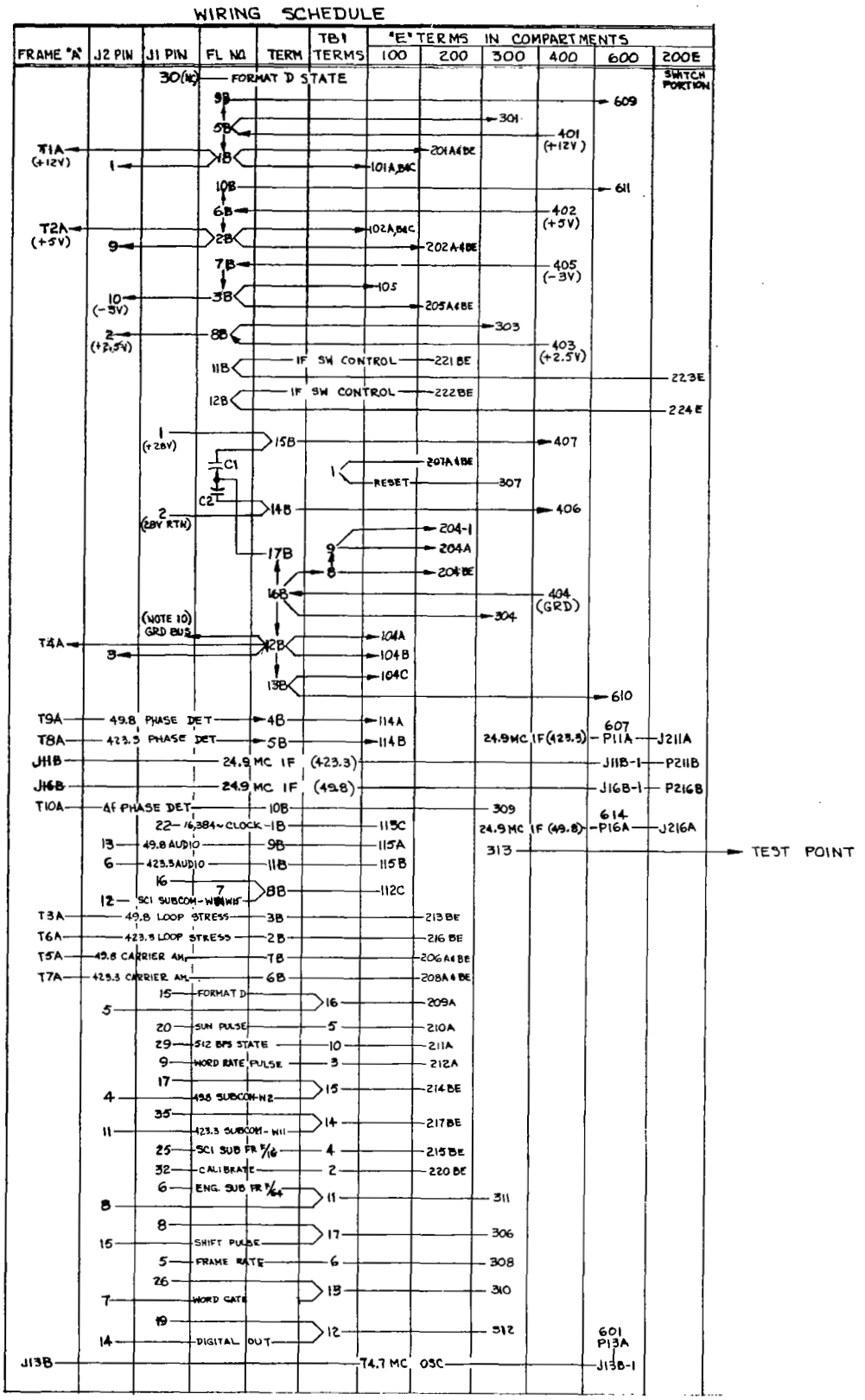
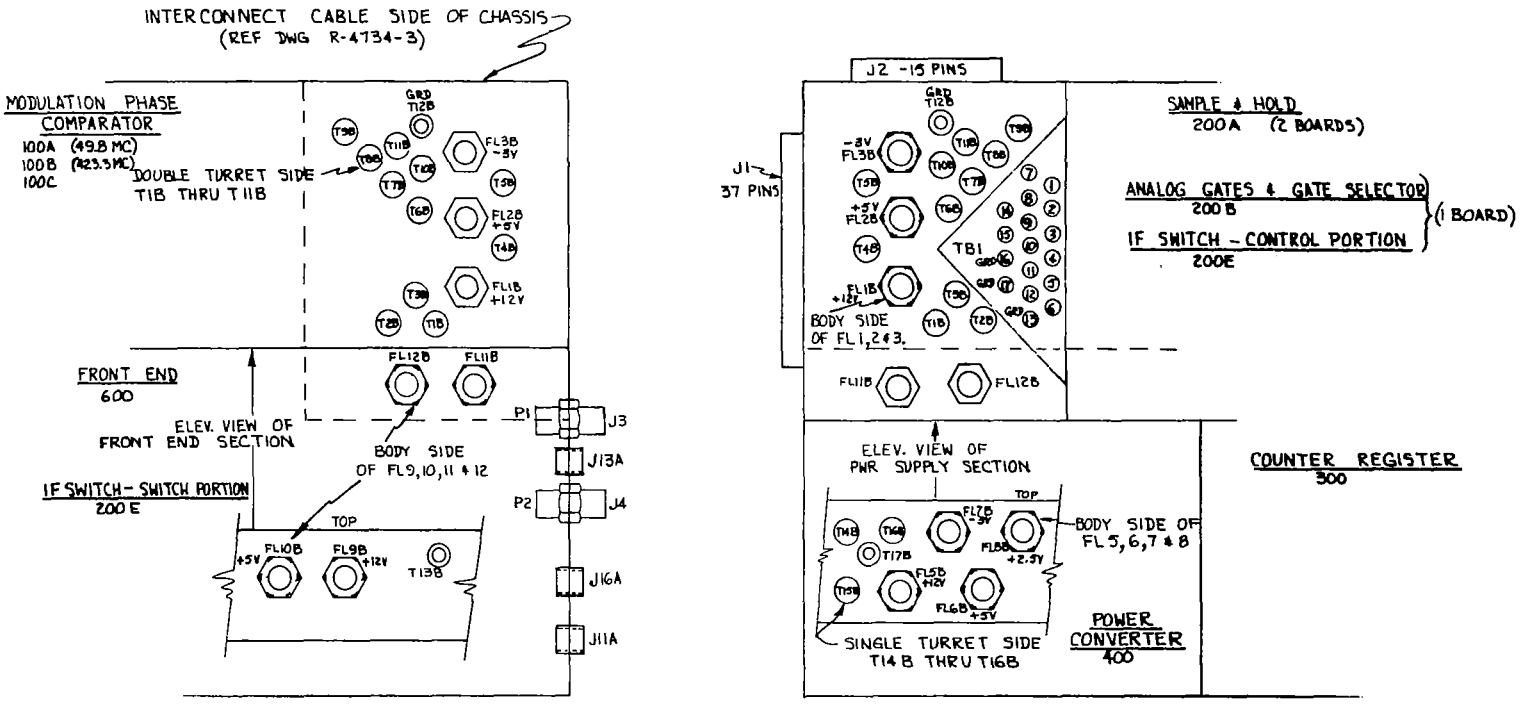



Figure 4.7 - Frame B Wiring Diagram




PHYSICAL LOCATION OF WIRING COMPONENTS
(NO SCALE)

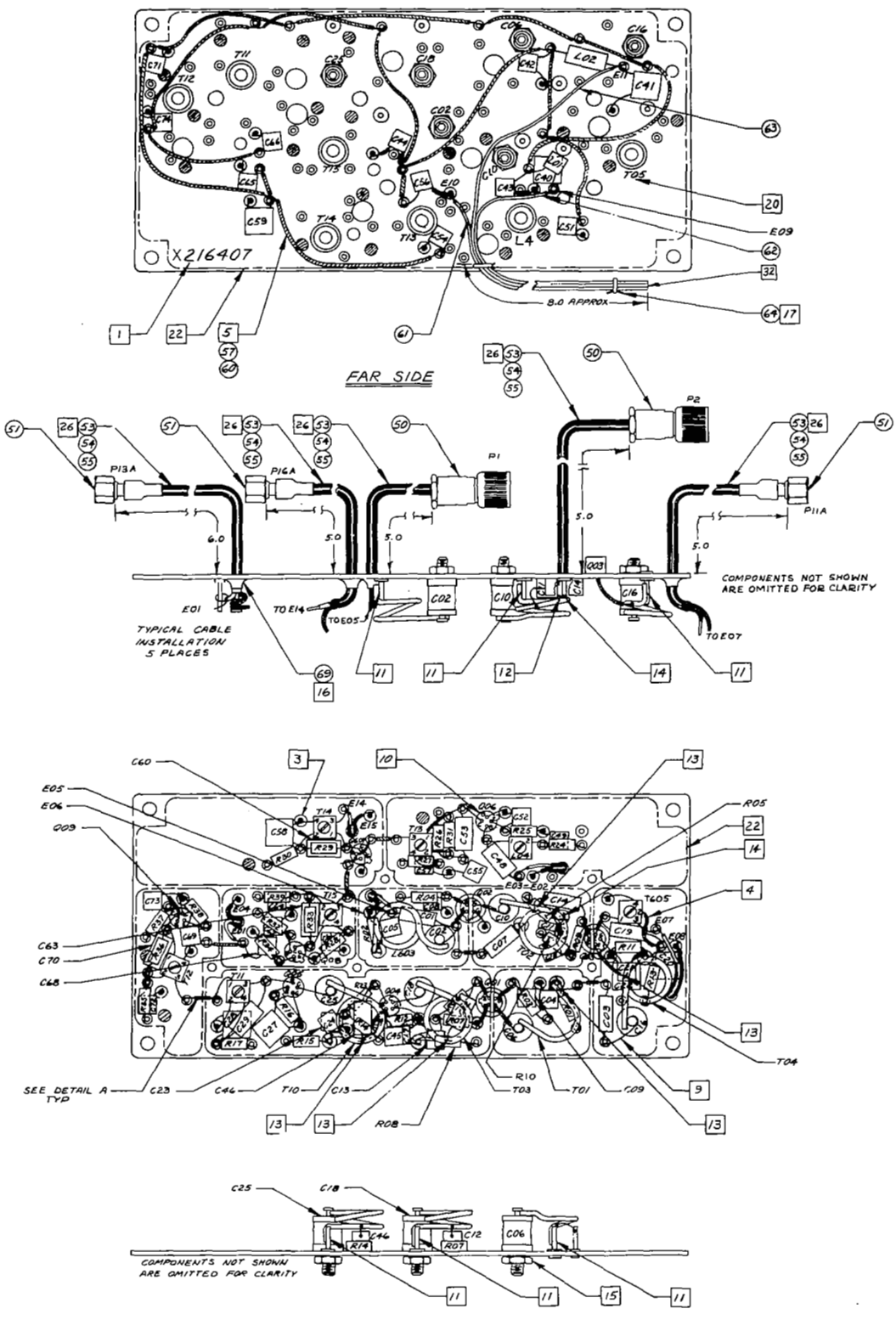



Figure 4.8 - Pictorial Diagram of the Front End

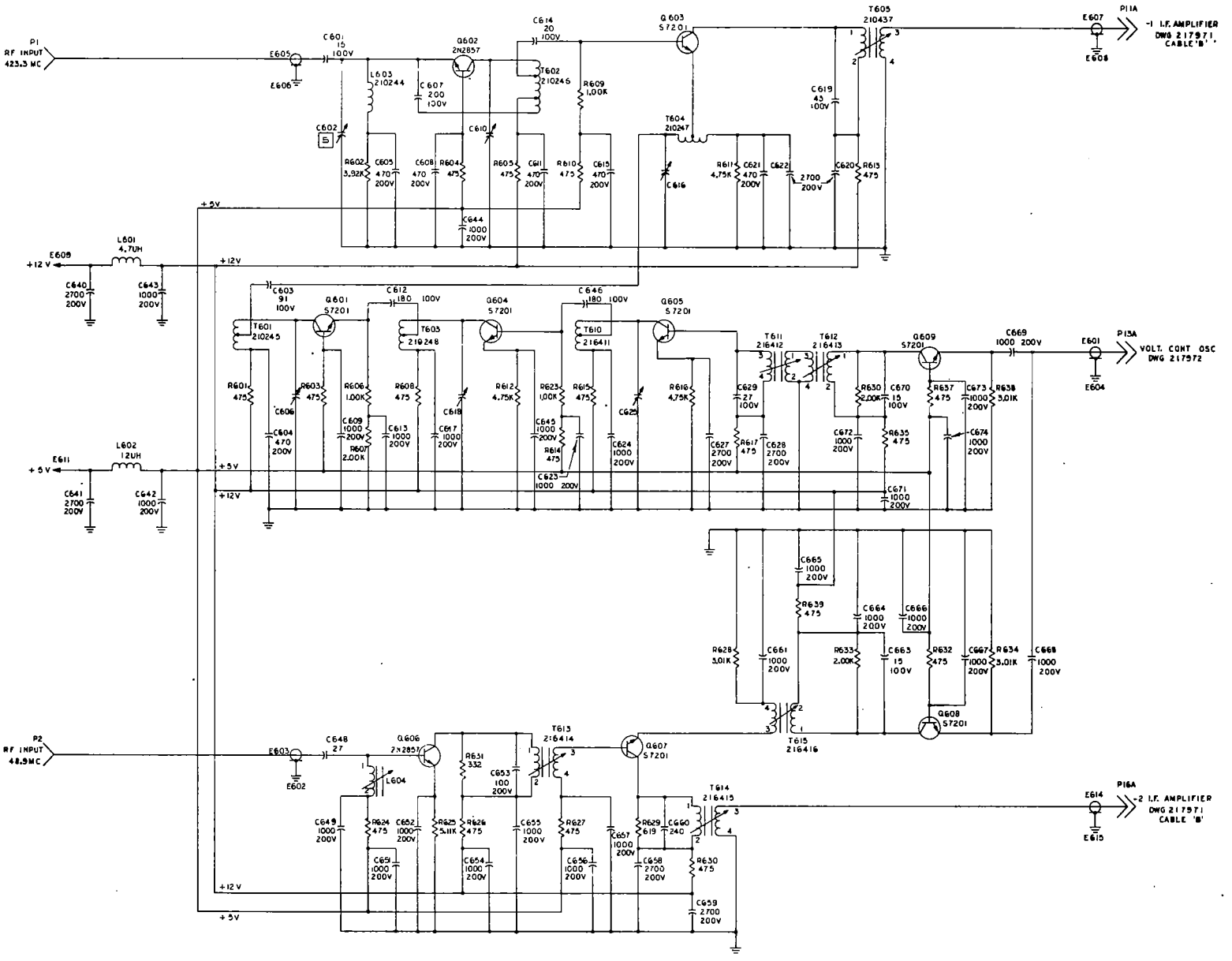



Figure 4.9 Front End

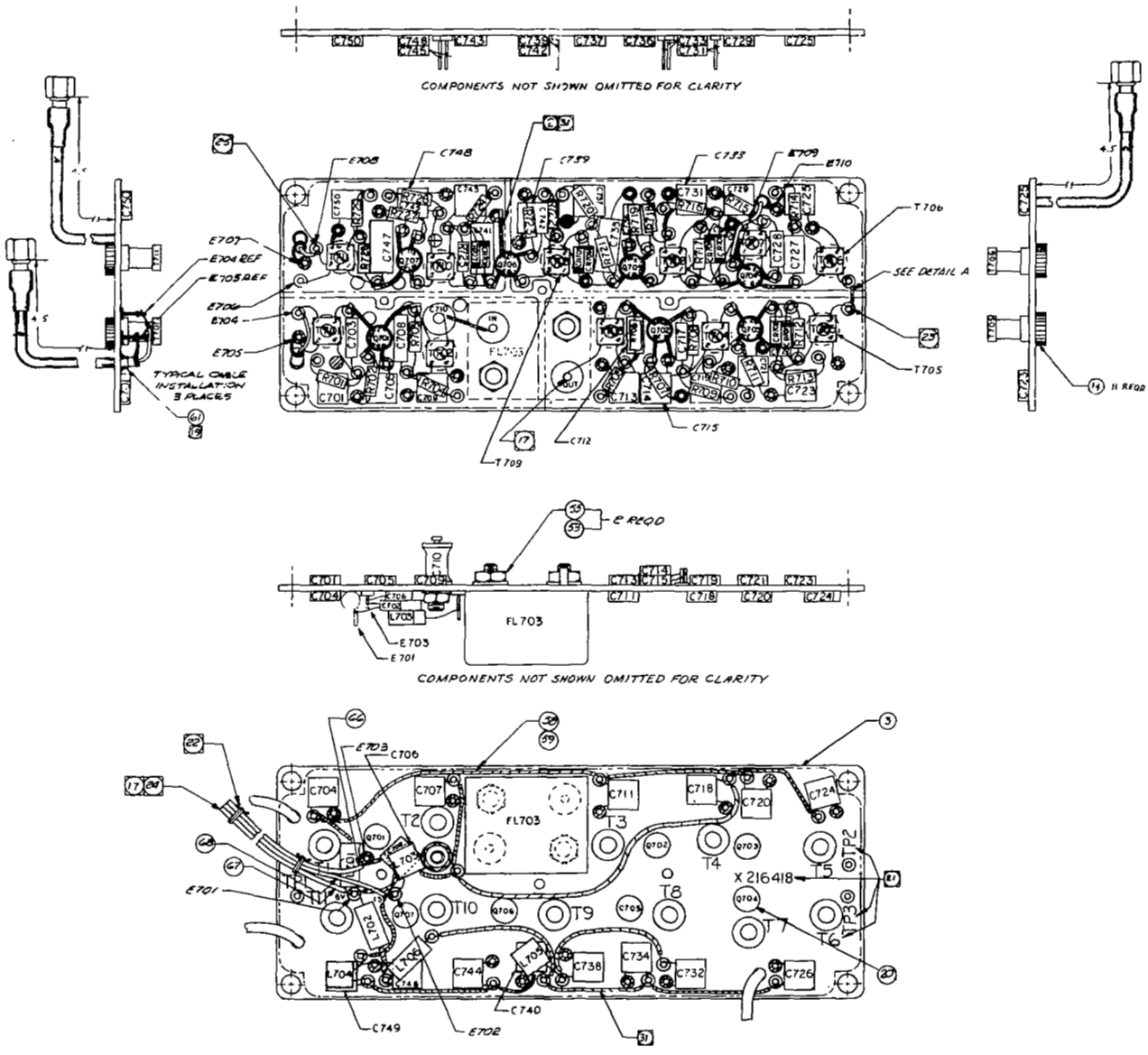



Figure 4.10 - Pictorial Diagram of the IF Amplifier

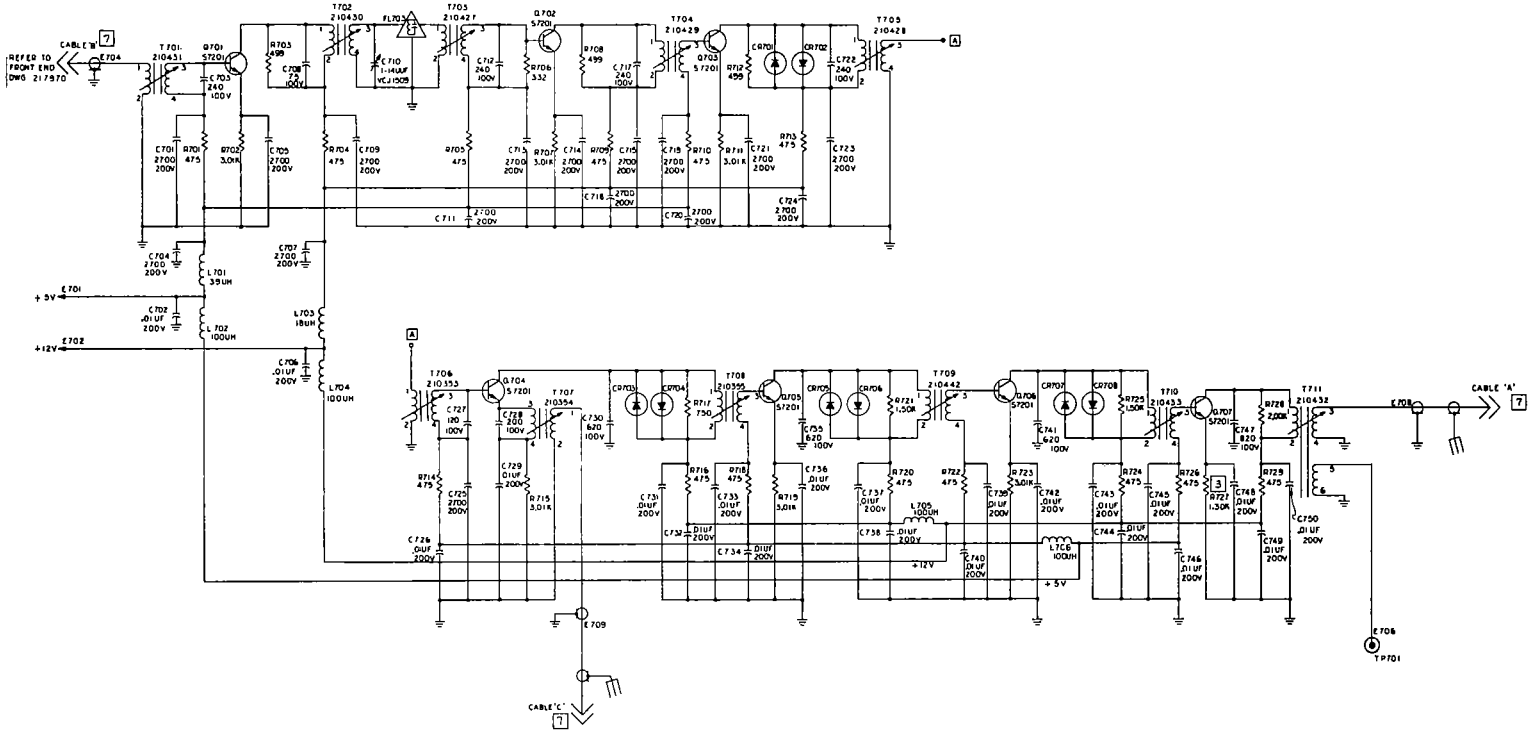



Figure 4.11 I.F. Amplifier

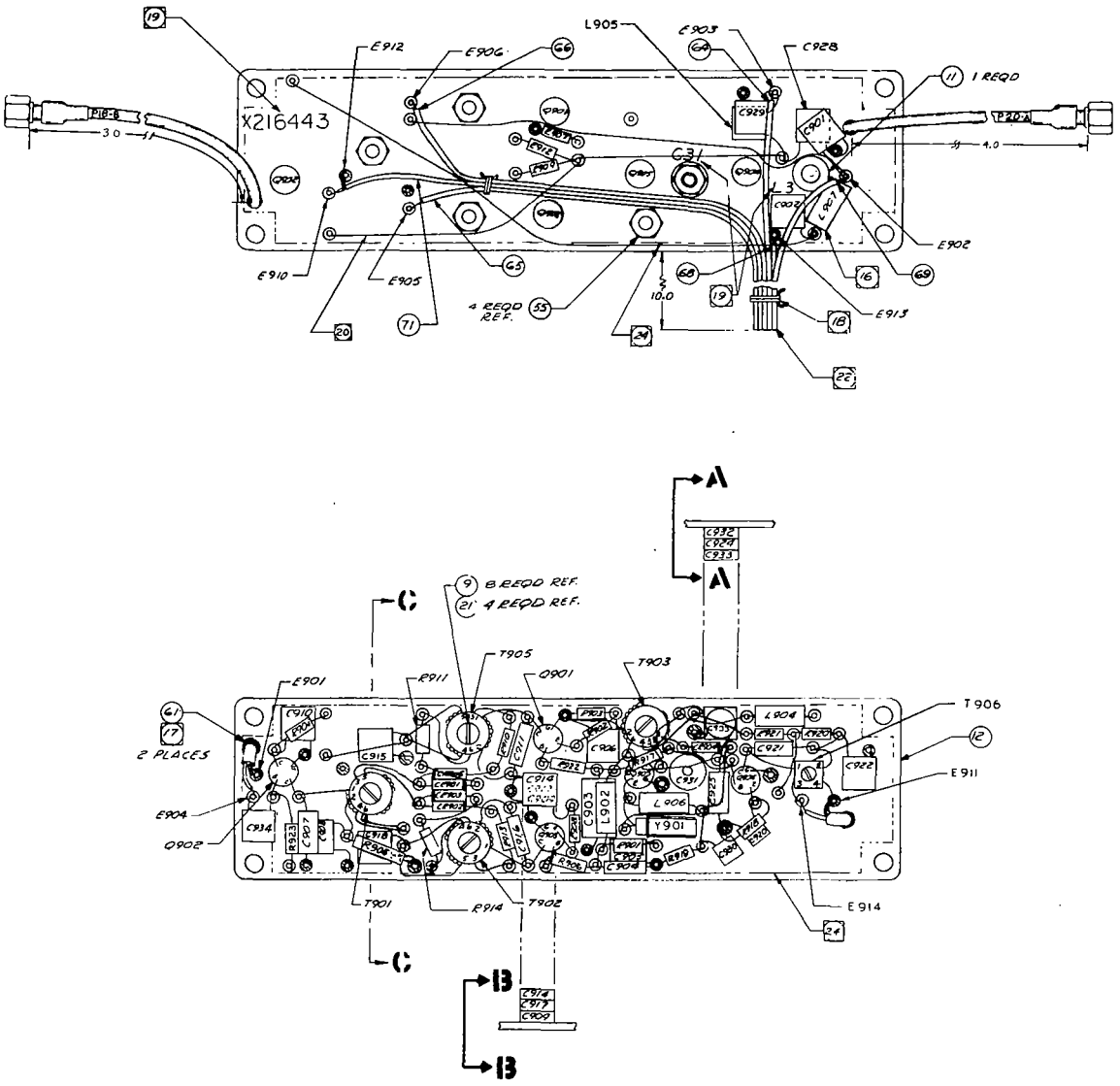



Figure 4.12 - Pictorial Diagram of the Reference Oscillator

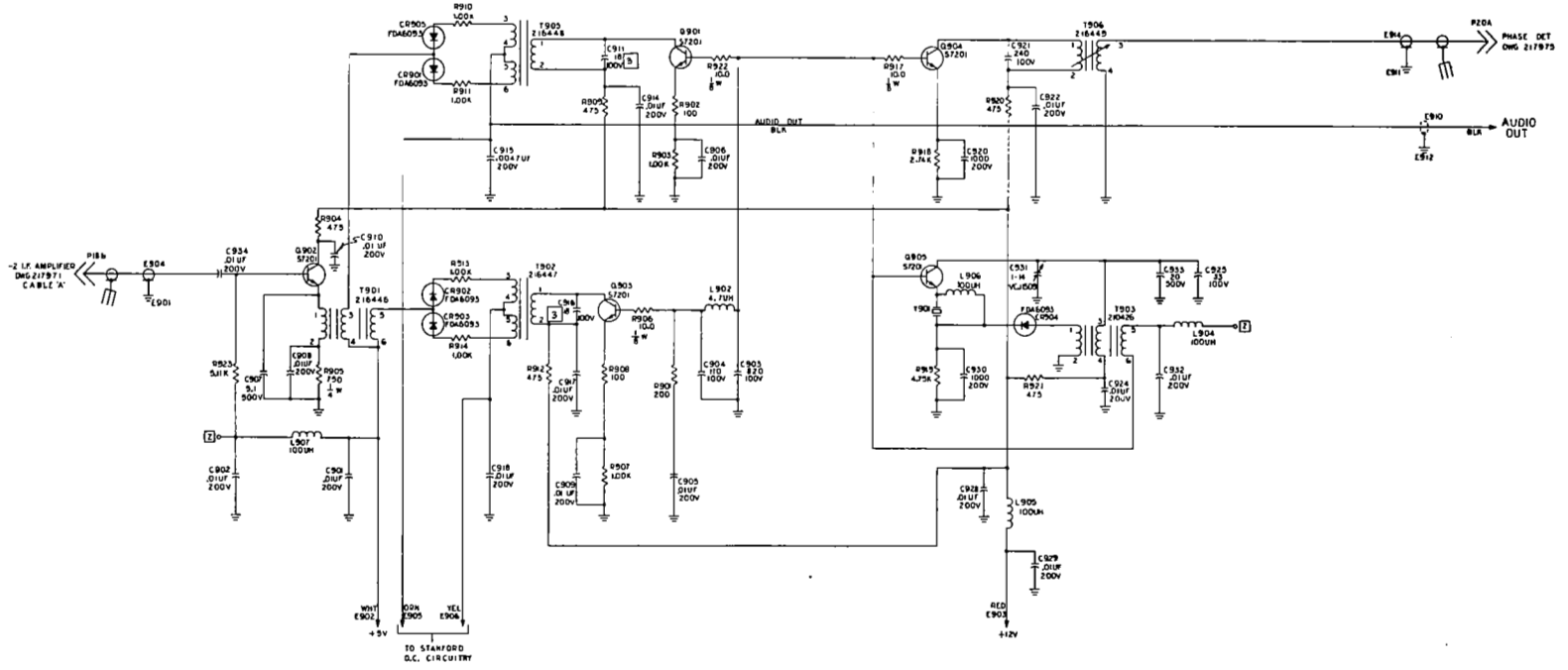



Figure 4.13 Reference Oscillator

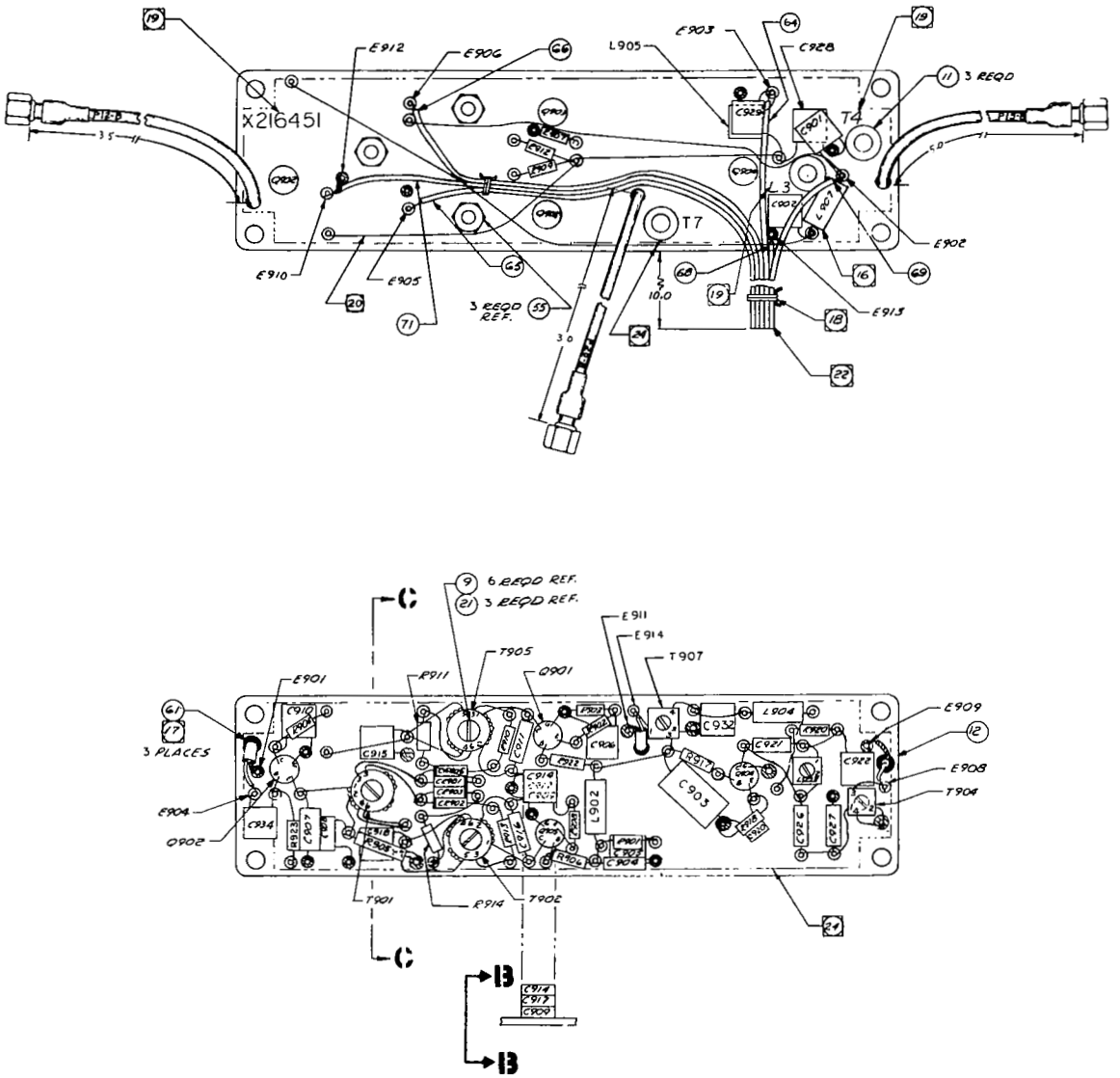



Figure 4.14 - Pictorial Diagram of the Phase Detector

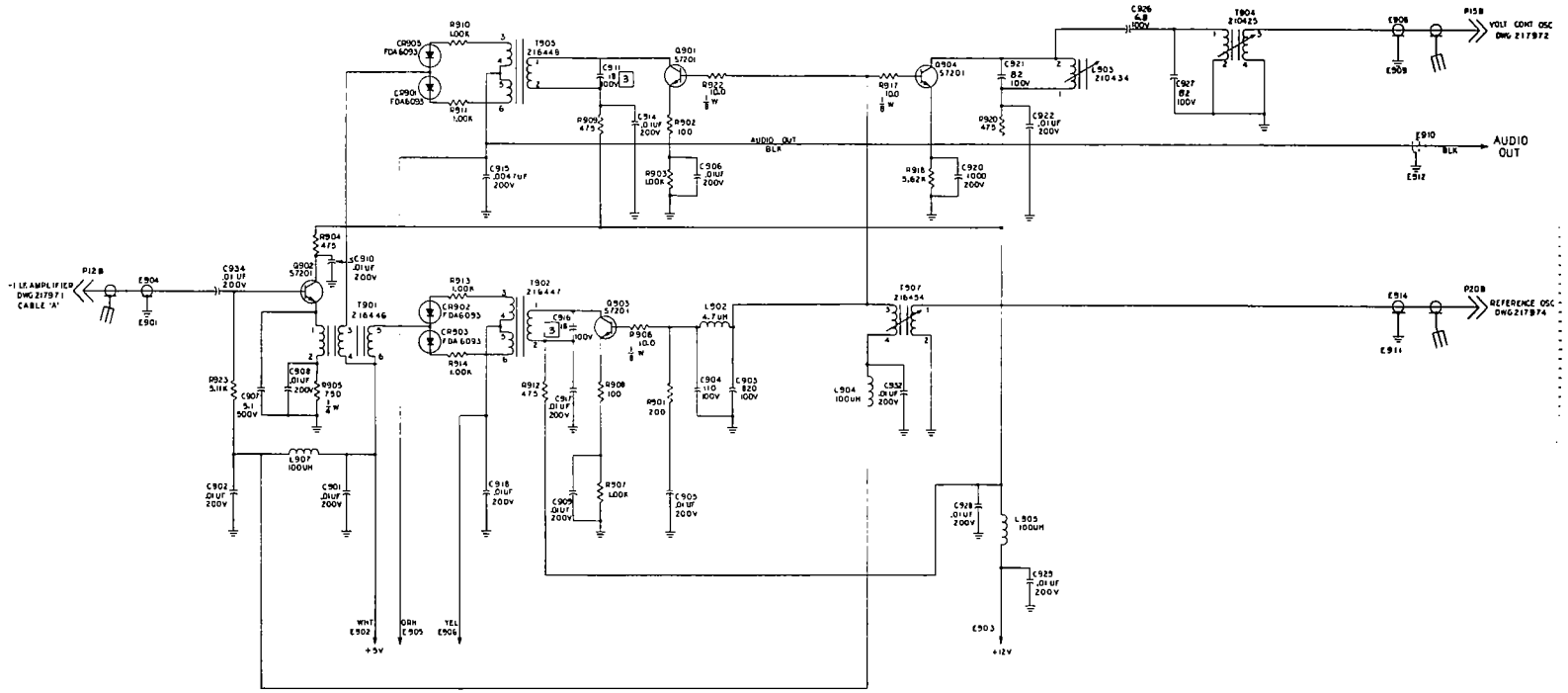



Figure 4.15 Phase Detector

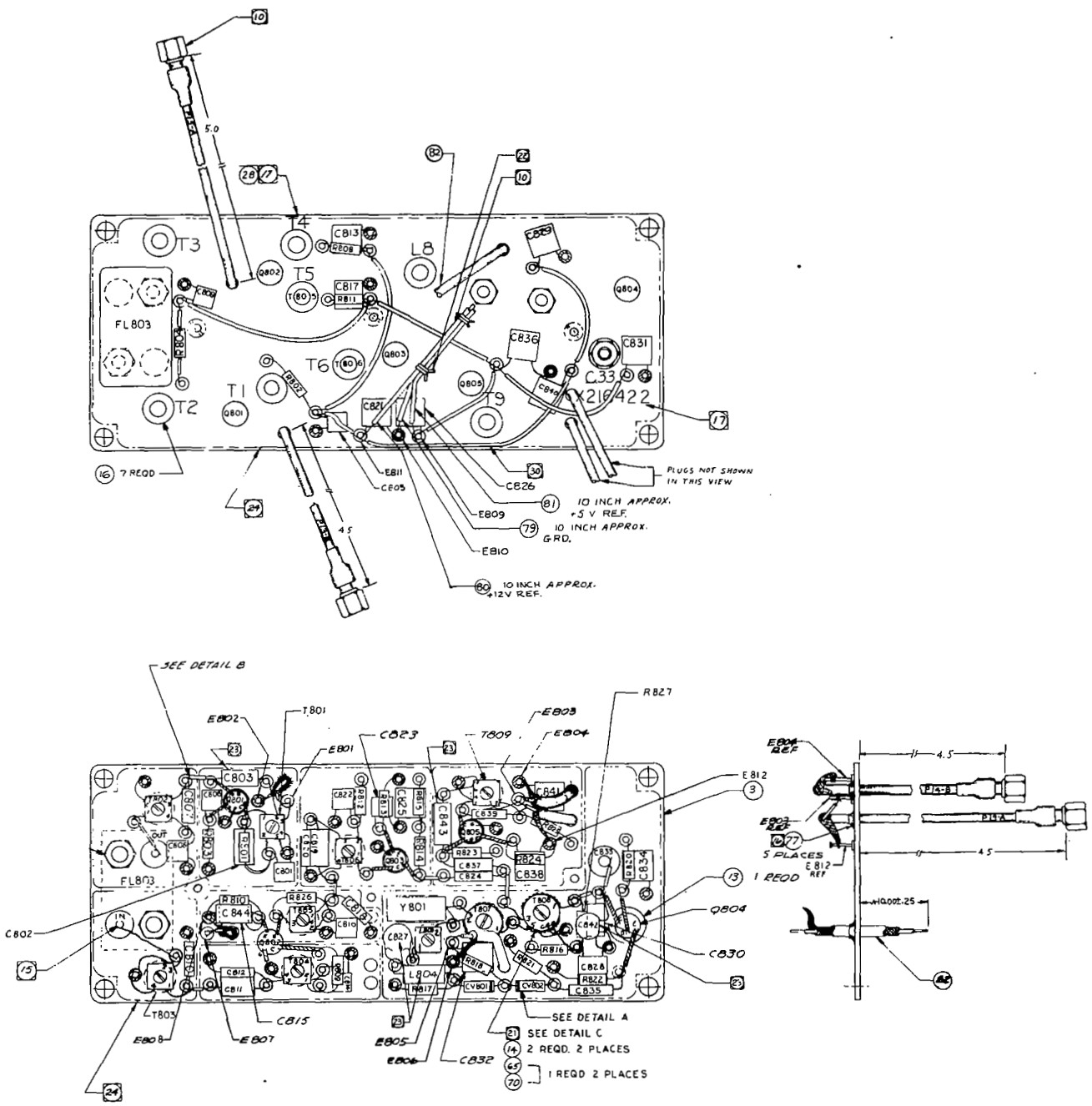



Figure 4.16 - Pictorial Diagram of the Voltage Controlled Oscillator

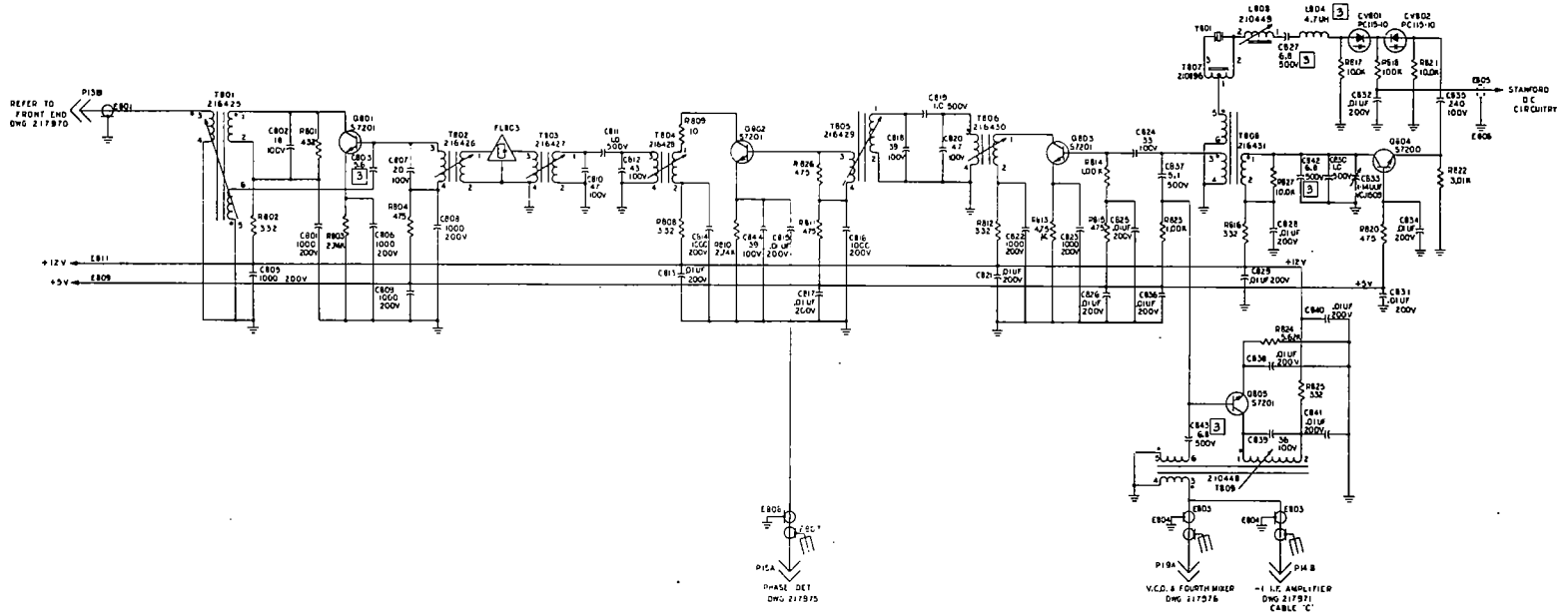



Figure 4.17 Voltage Controlled Oscillator

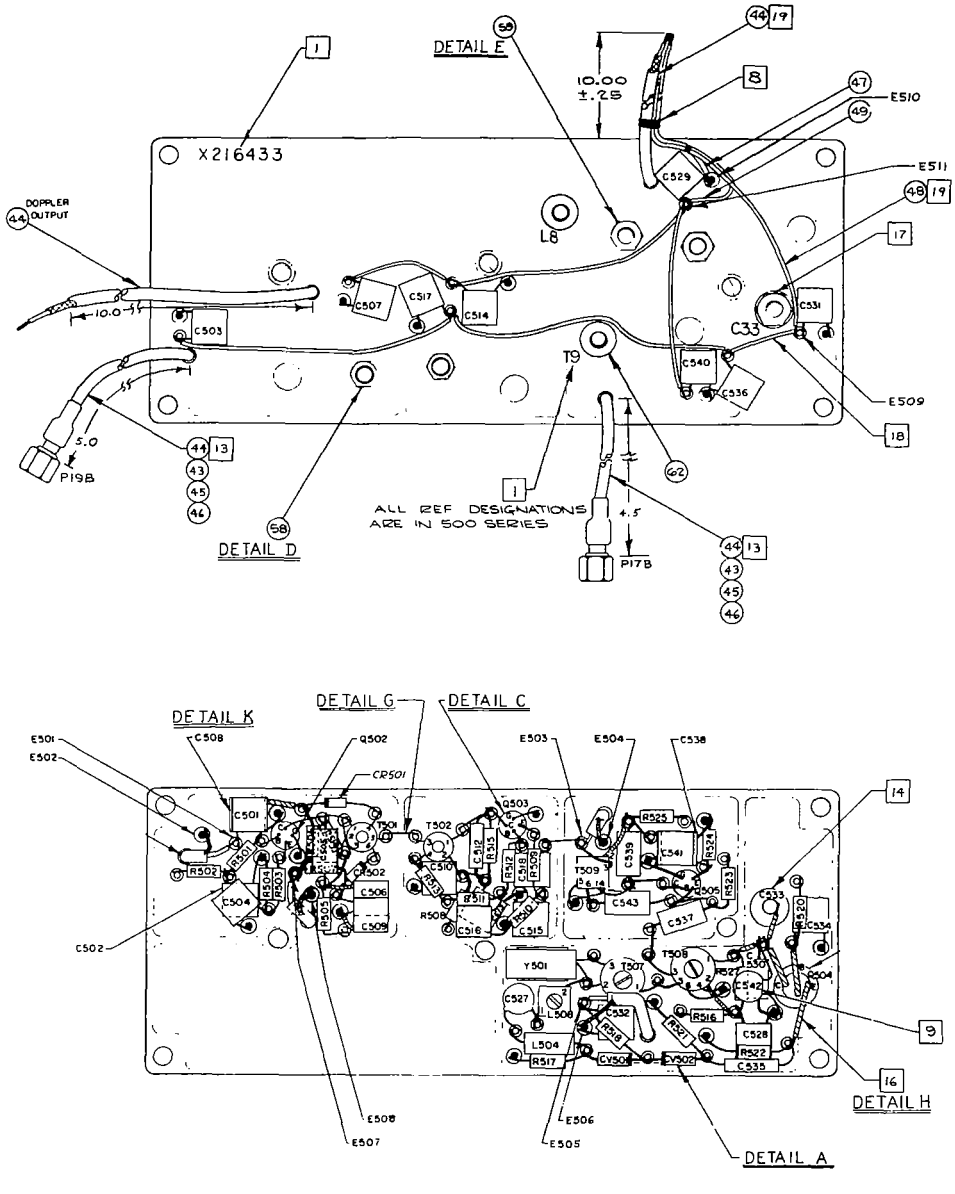



Figure 4.18 - Pictorial Diagram of the VCO and Fourth Mixer

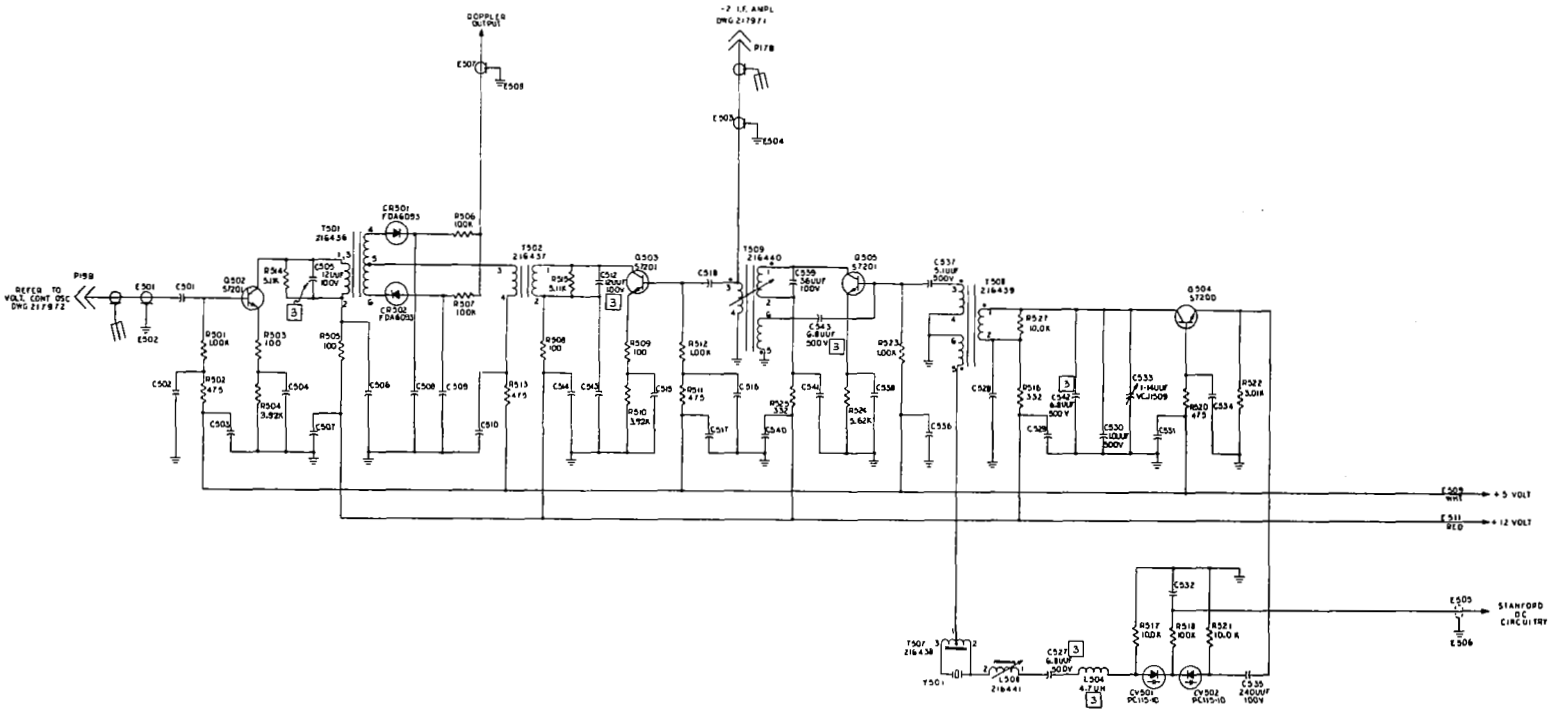



Figure 4.19 VCO and Fourth Mixer

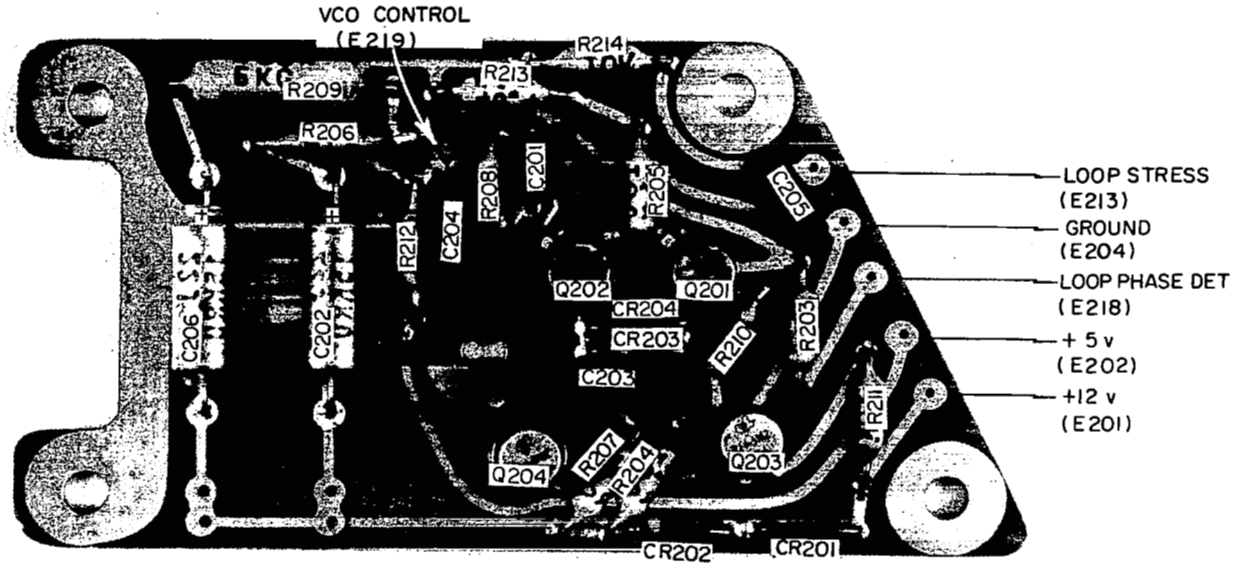



Figure 4.20 - Printed Circuit of the Loop Difference Amplifier for the 49.8 Mc channel - Wiring Side
Components are as seen through the wiring side.

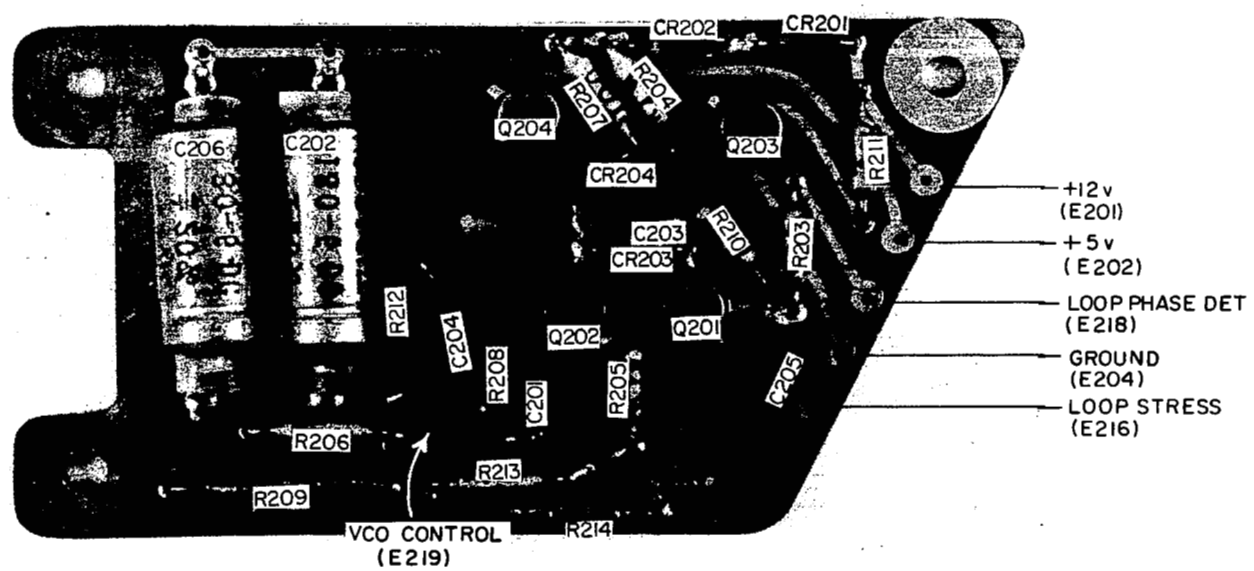
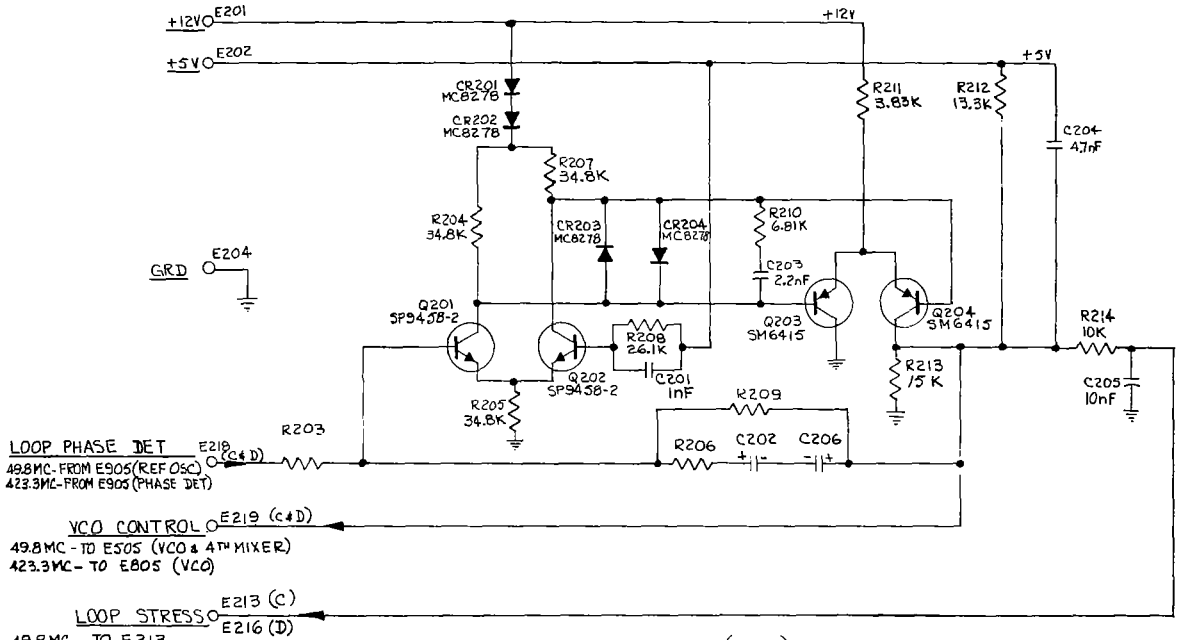



Figure 4.21 - Printed Circuit of the Loop Difference Amplifier for the 423.3 Mc channel - Wiring Side
Components are as seen through the wiring side.




FOR 49.8 MC LOOP: (200C)
C202 & C206 = 22 μF @ 15V
R203 = 31.6K; R206 = 3.48K, R209 = 619K

FOR 423.3 MC LOOP: (200D)
C202 & C206 = 180 μF @ 6V
R203 = 23.7K, R206 = 261Ω, R209 = 464K

NOTE: 1. ALL COMPONENT NUMBERS IN 49.8 MC LOOP DIFFERENCE AMPLIFIER CIRCUIT HAVE SUFFIX "C"; i.e. R206C, CR204C, ETC.
2. ALL COMPONENT NUMBERS IN 423.3 MC LOOP DIFFERENCE AMPLIFIER HAVE SUFFIX "D", i.e. R206D, CR204D, ETC.
3. Q TYPE SP9458-2 ≈ 2N2483; SM6415 ≈ 2N2861.
4. DC GAIN = 20.
5. Q201 & Q202 ARE MATCHED PAIR
6. CIRCUITRY ON THIS DWG MOUNTED ON TWO BOARDS, BOTH S.R.I. #454734-009.

Figure 4.22 Loop Difference Amplifier

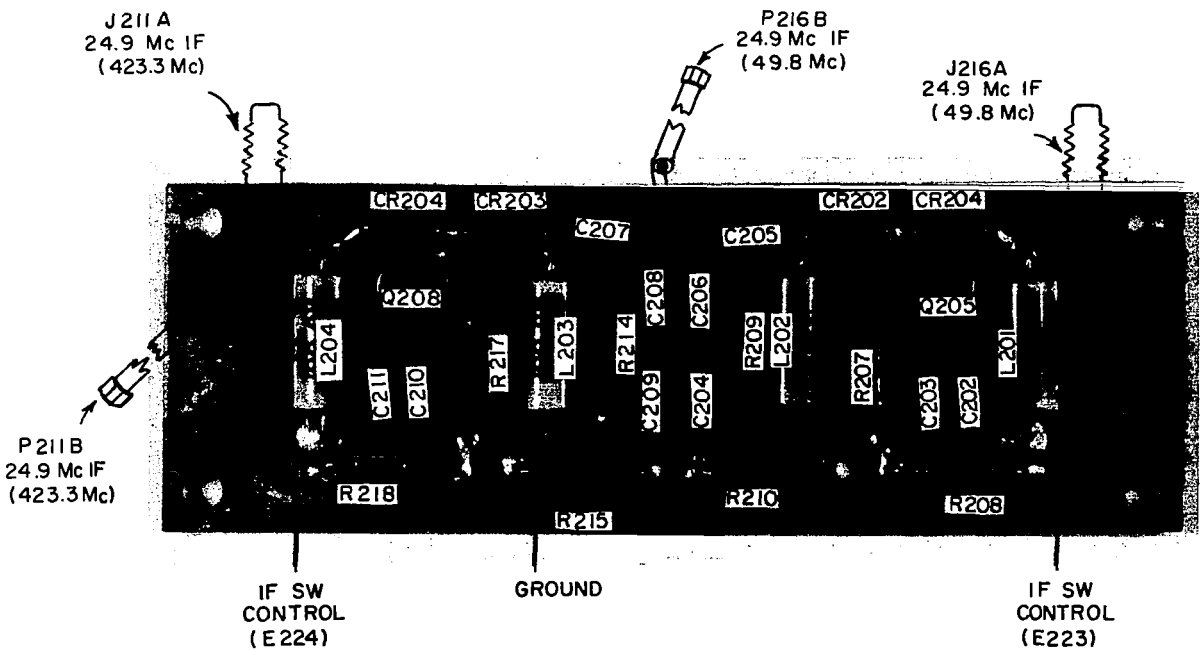



Figure 4.23 - Printed Circuit of the Switch Portion of the IF Switch - Wiring Side
Components are as seen through the wiring side. The control portion of the IF switch is part of the printed circuit in Figure 4.29, page 88.

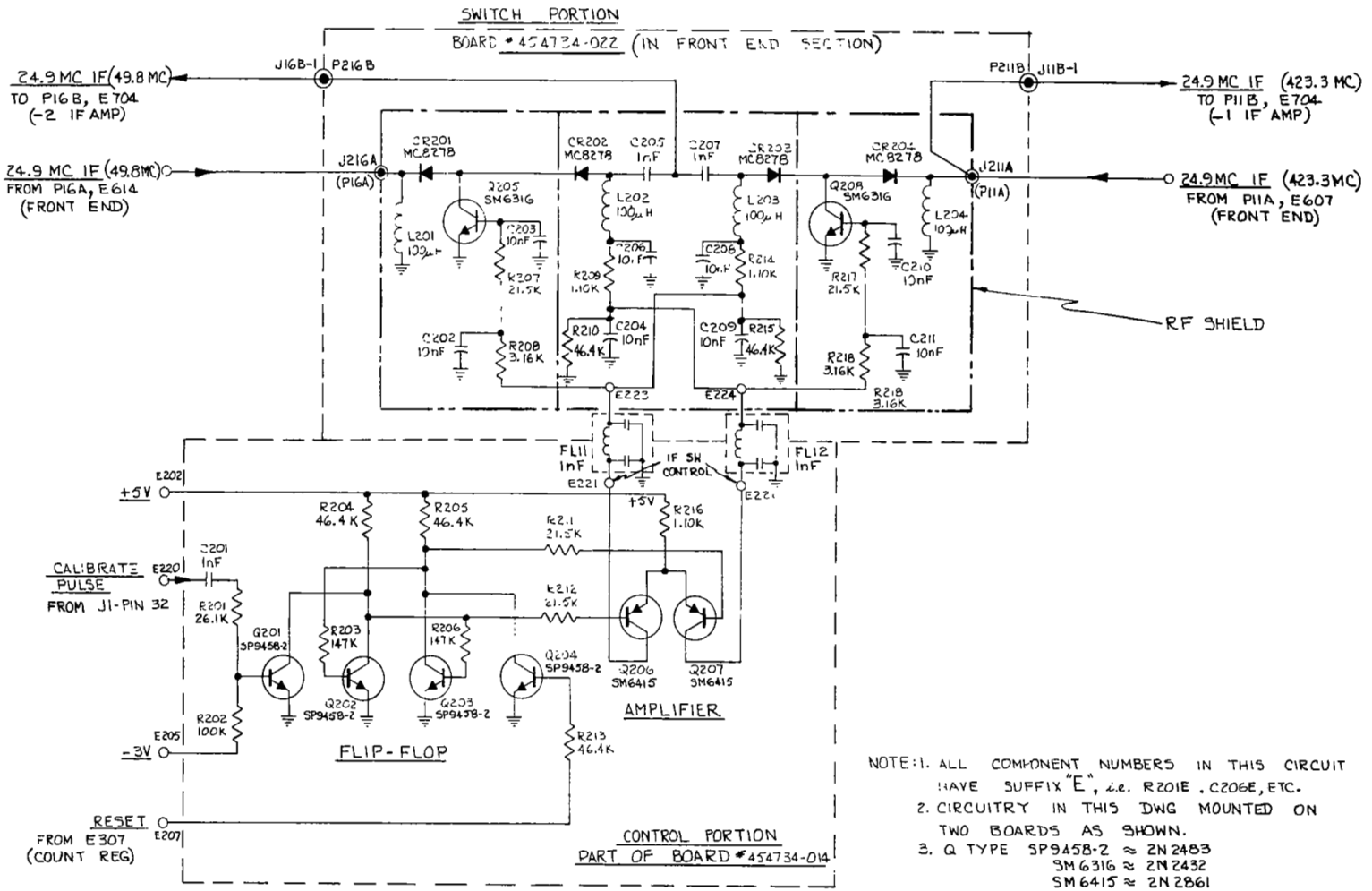



**Figure 4.24 IF Switch**

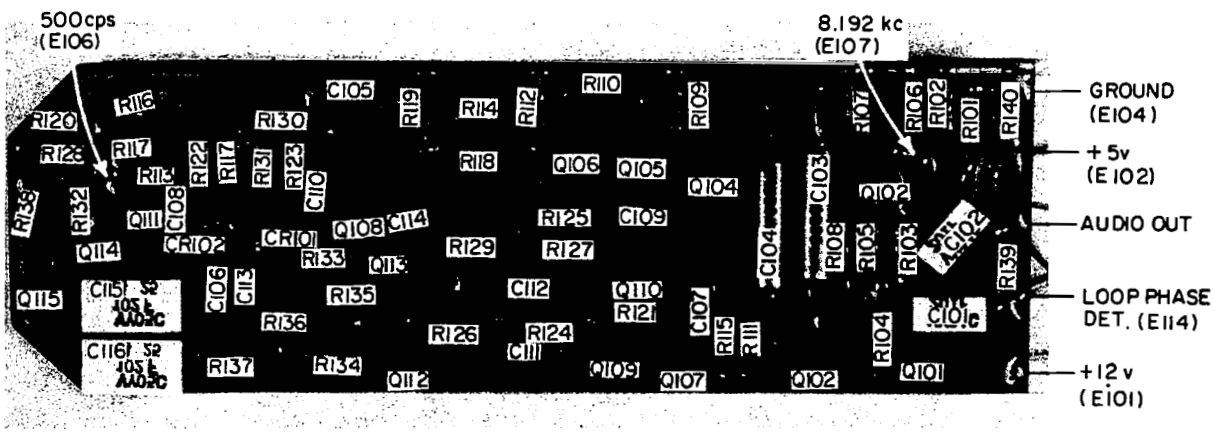
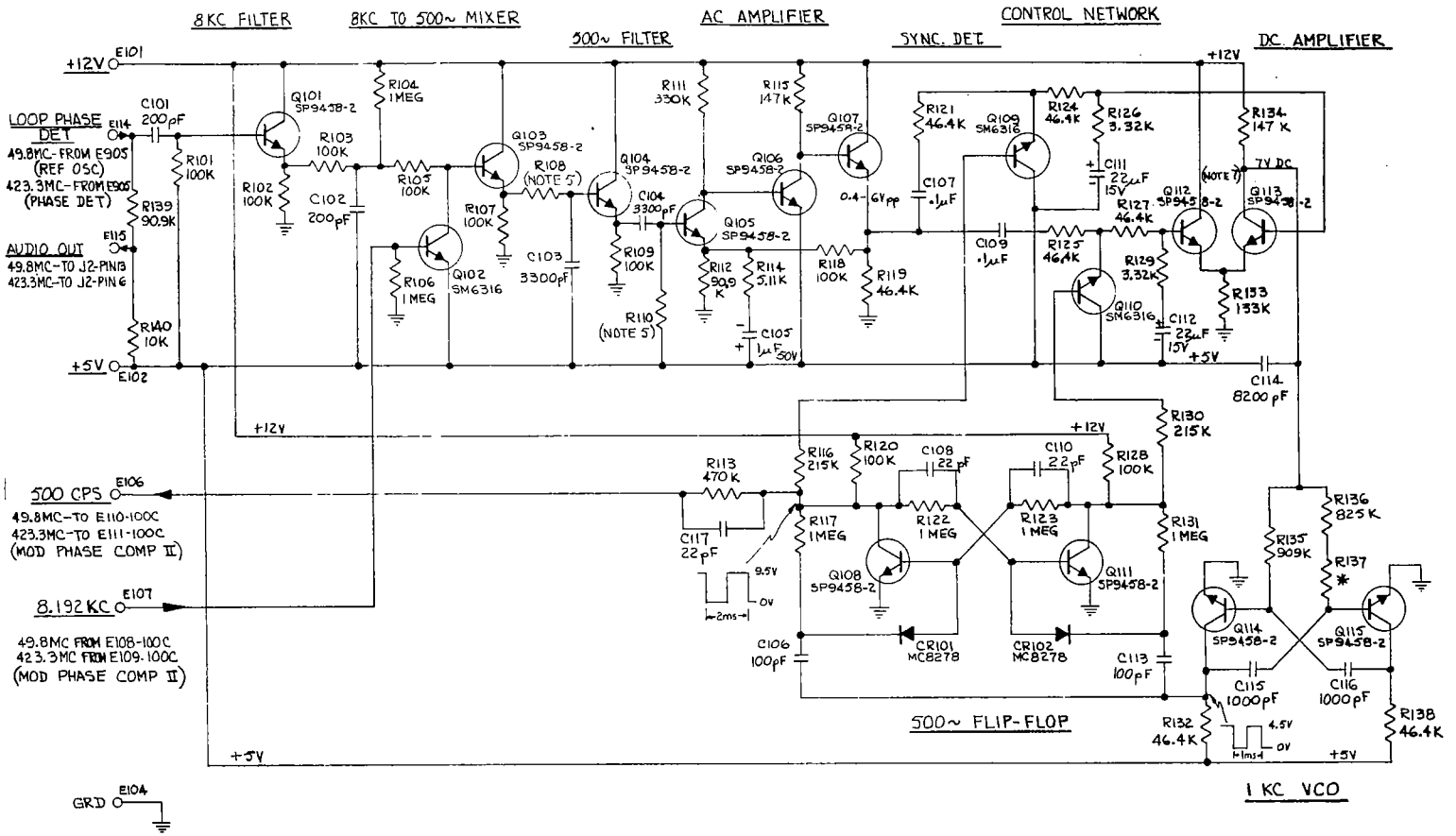



Figure 4.25 - Printed Circuit of the Modulation Phase Comparator, Section I - Wiring Side
Components are as seen through the wiring side.




NOTE: 1. ALL COMPONENT NUMBERS IN ONE CIRCUIT (49.8MC - CHANNEL 'A') HAVE SUFFIX "A", i.e. R106A, CR101A, ETC.

2. ALL COMPONENT NUMBERS IN AN IDENTICAL CIRCUIT (423.3MC - CHANNEL 'B') HAVE SUFFIX "B", i.e. R106B, CR101B, ETC.

3. * SELECT R137 AT ASSEMBLY.

4. CIRCUITRY ON THIS DWG IS MOUNTED ON TWO BOARDS, BOTH SRI #454734-021.

5. R108A & R110A ARE 68.1K ; R108B & R110B ARE 147K.

6. Q TYPE SM6316 ≈ 2N2432 ; Q TYPE SP9458-2 ≈ 2N2483.

7. Q112 & Q113 ARE MATCHED PAIR.

**Figure 4.26 Modulation Phase Comparator Section I**

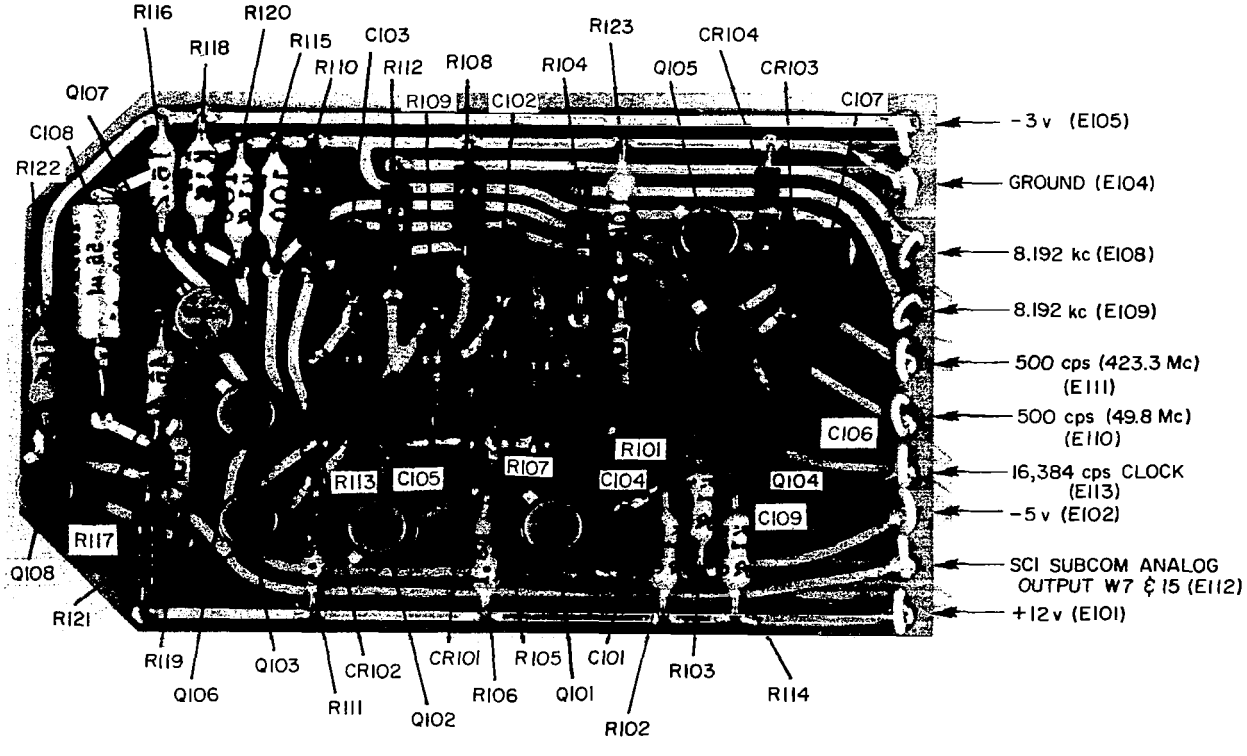
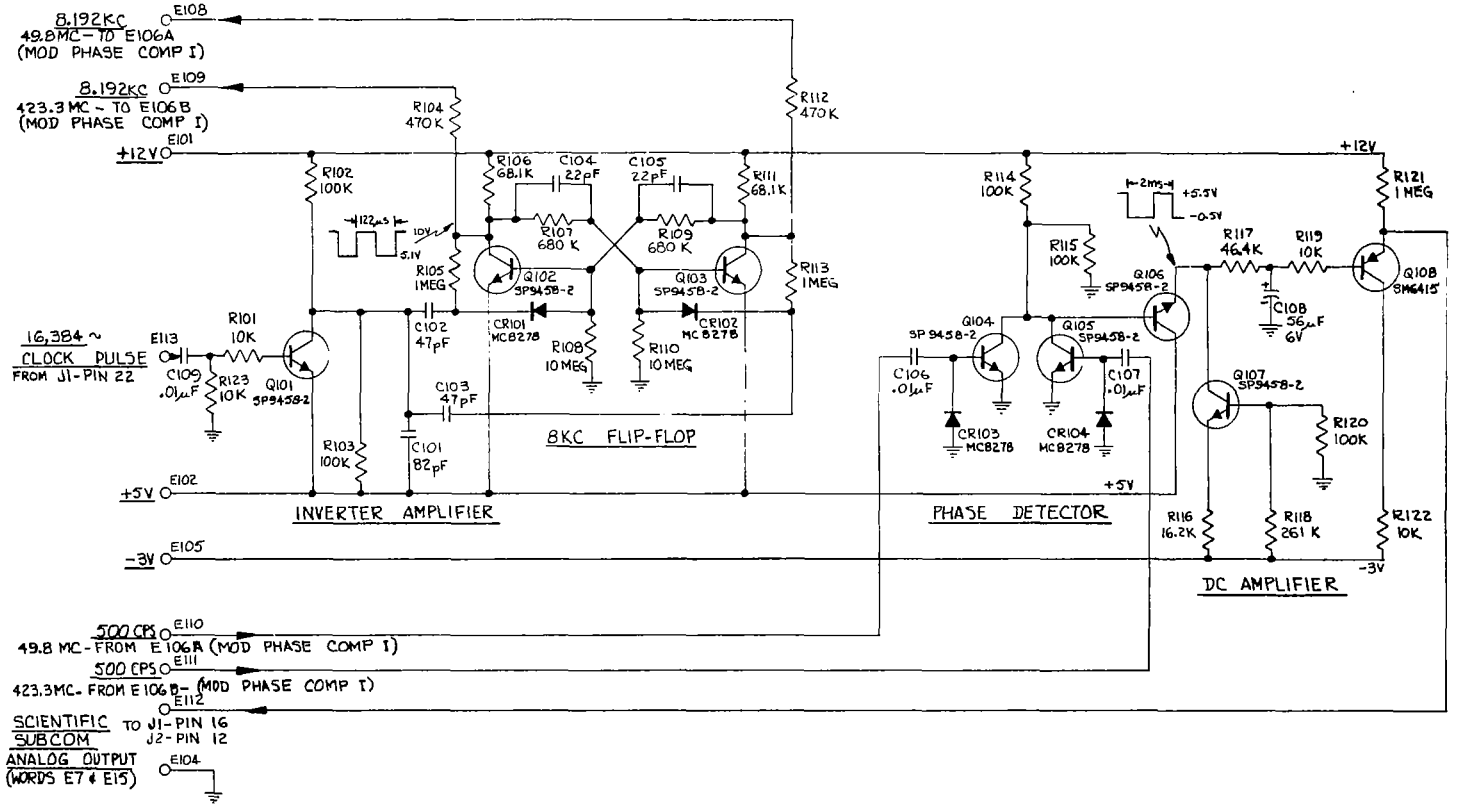



Figure 4.27 - Printed Circuit of the Modulation Phase Comparator, Section II - Wiring Side
Components are as seen through the wiring side.




NOTE: 1. ALL COMPONENT NUMBERS IN THIS CIRCUIT HAVE SUFFIX "C", i.e. R106C, CR104C, ETC.
2. CIRCUITRY ON THIS DWG IS MOUNTED ON BOARD SRI #45-4734-020.
3. Q TYPE SP9458-2 ≈ 2N2483
SM6415 ≈ 2N2861

Figure 4.28 Modulation Phase Comparator Section II

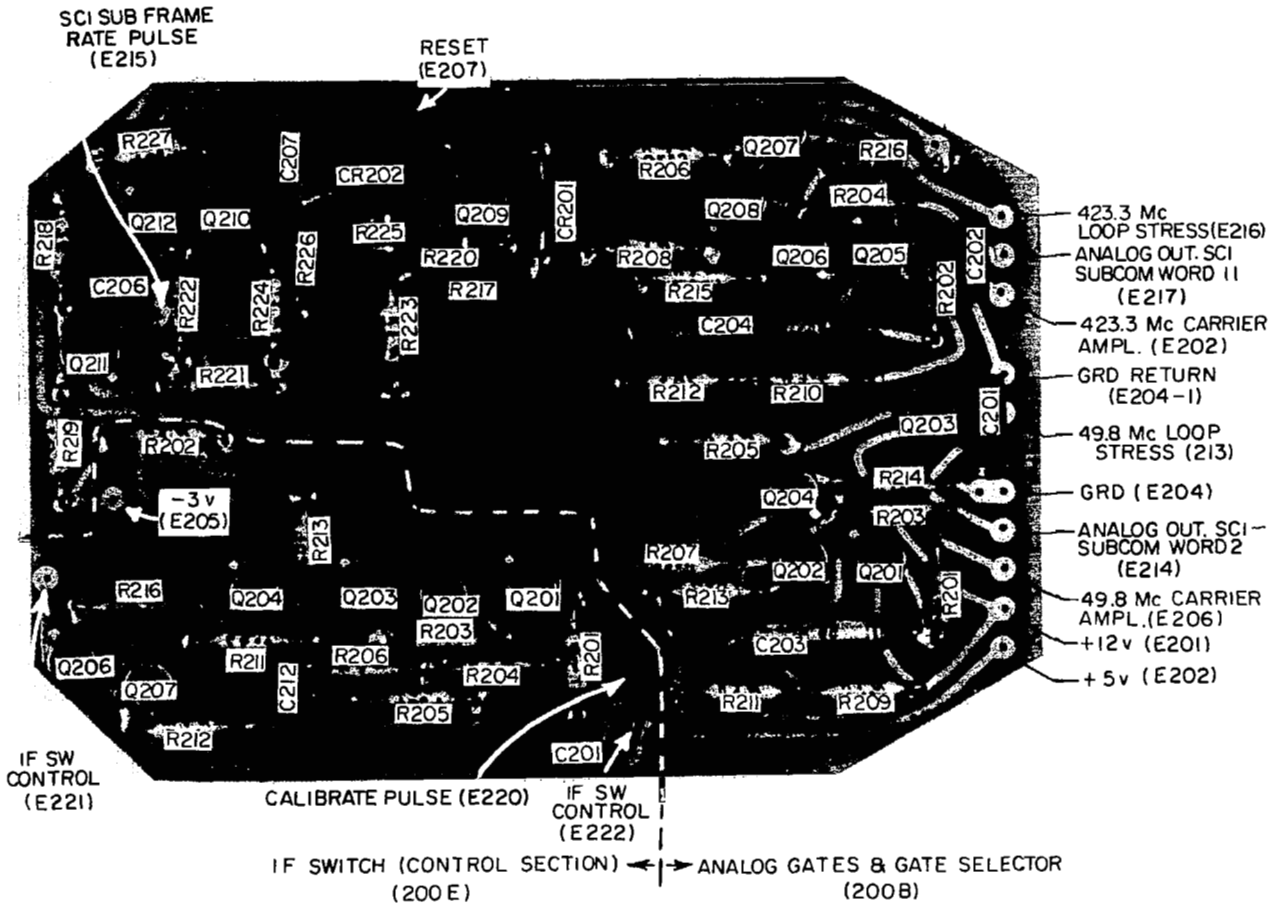
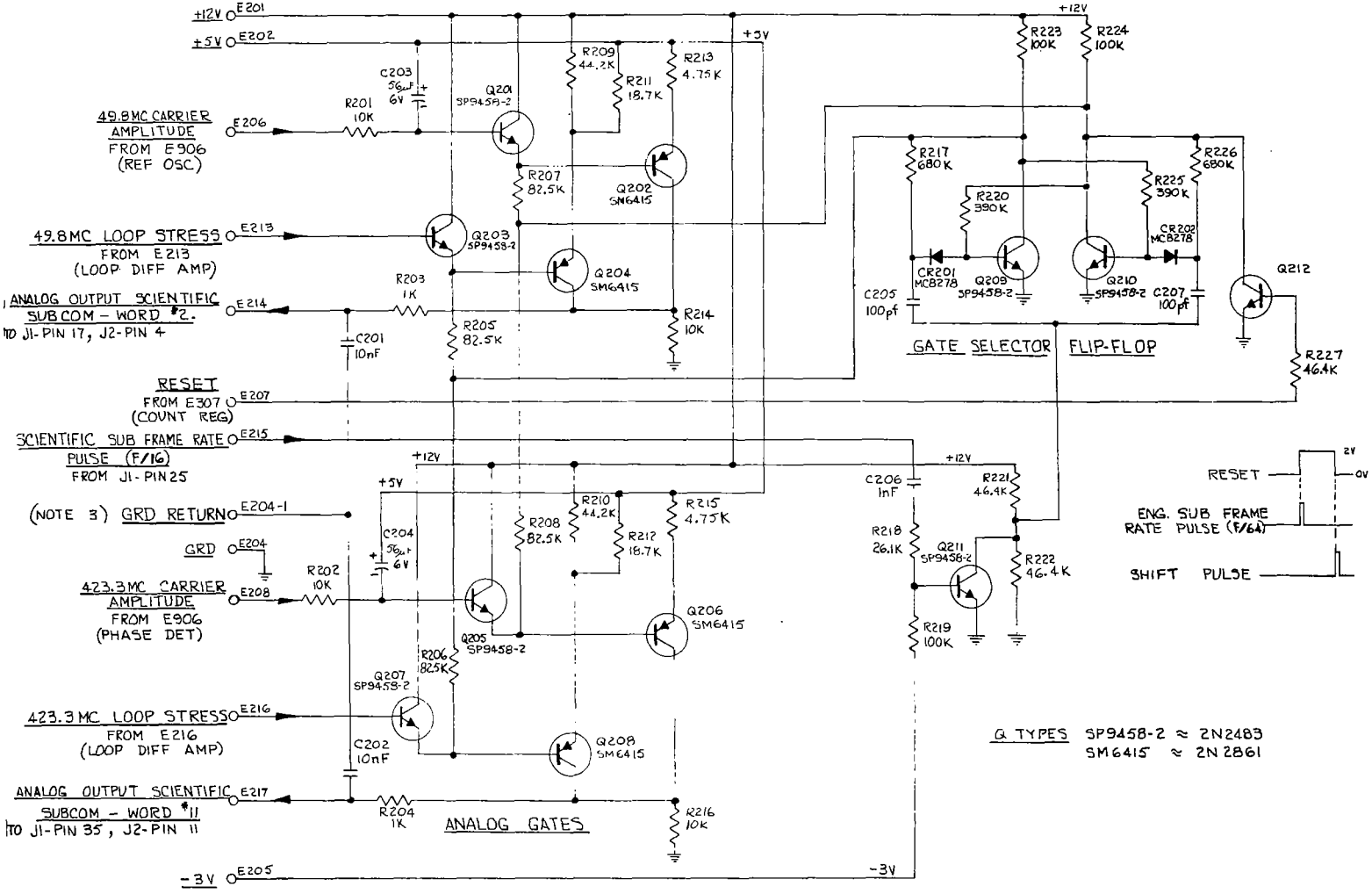
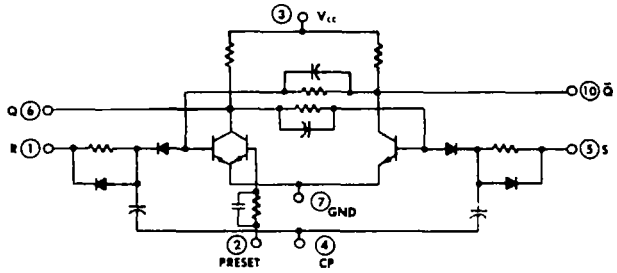



Figure 4.29 - Printed Circuit of the Analog Gates and Gate Selector, and the Control Portion of the IF Switch - Wiring Side Components are as seen through the wiring side.

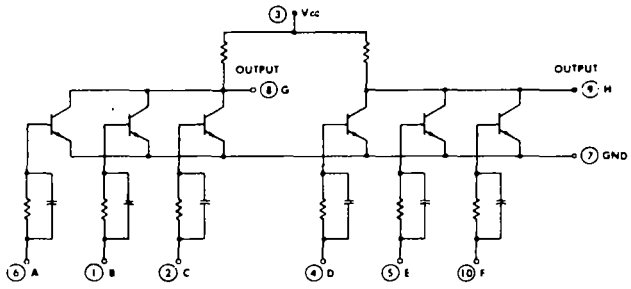


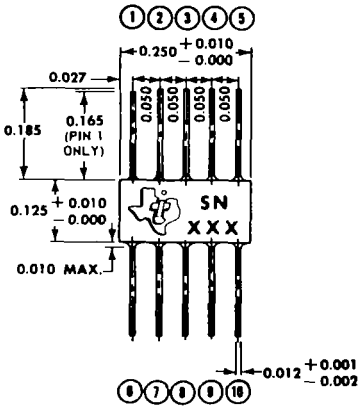

NOTE: 1. ALL COMPONENT NUMBERS IN THIS CIRCUIT HAVE SUFFIX "B", i.e. R201B, C206B, ETC.
2. CIRCUITRY ON THIS DWG AND PART OF CIRCUITRY ON DWG C-4734-200E-1 ARE MOUNTED ON S.R.I. #4734-014 BOARD.
3. GRD RETURN TERM E204-1 CONNECTS TO TB1-9.

Figure 4.30 Analog Gates and Gate Selector

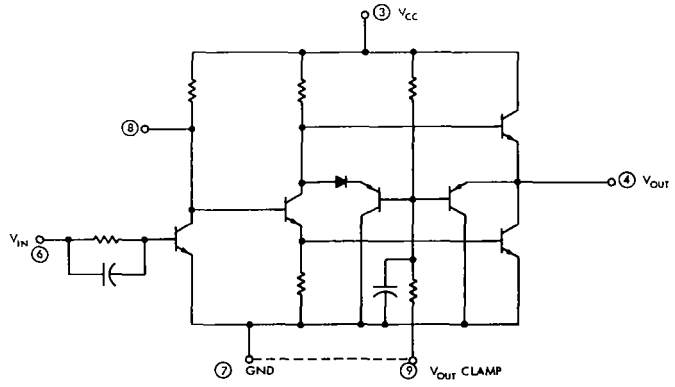



SNR510 Flip Flop




SNR514 Two NOR/NAND




SNR517 Clock Driver

Figure 4.31 - The Three TI SNR51 Series Integrated Circuits used in the Counter Register

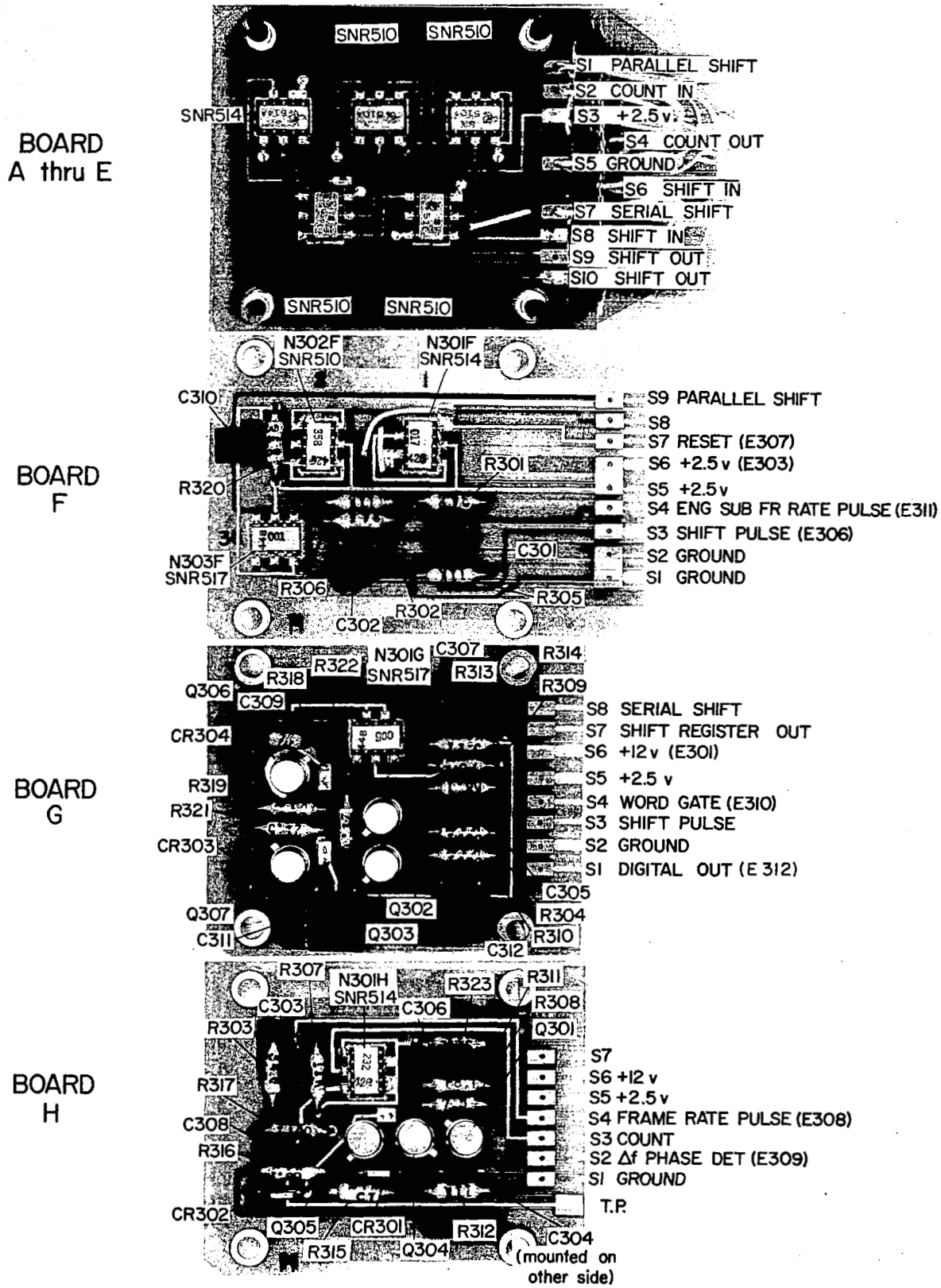
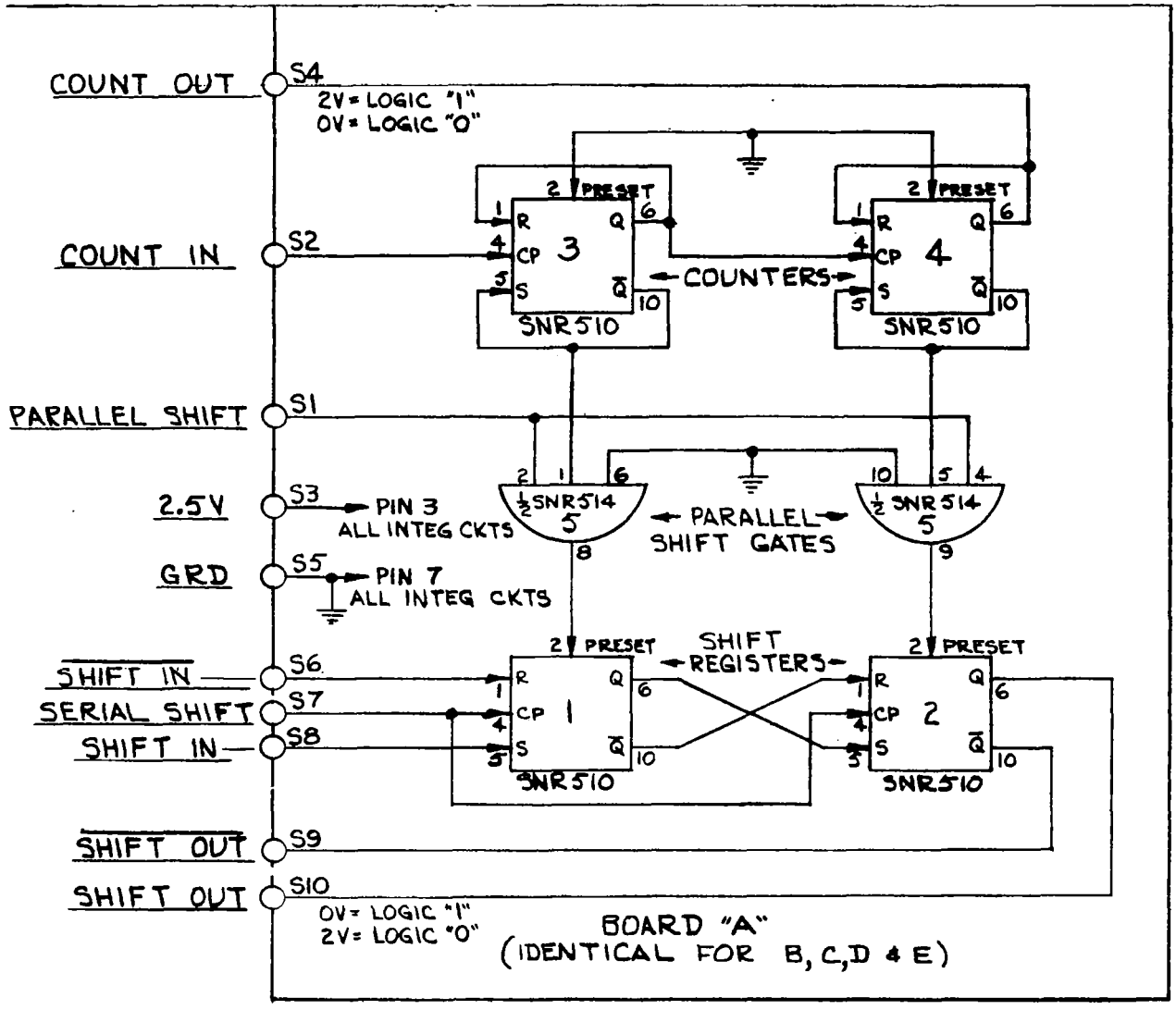
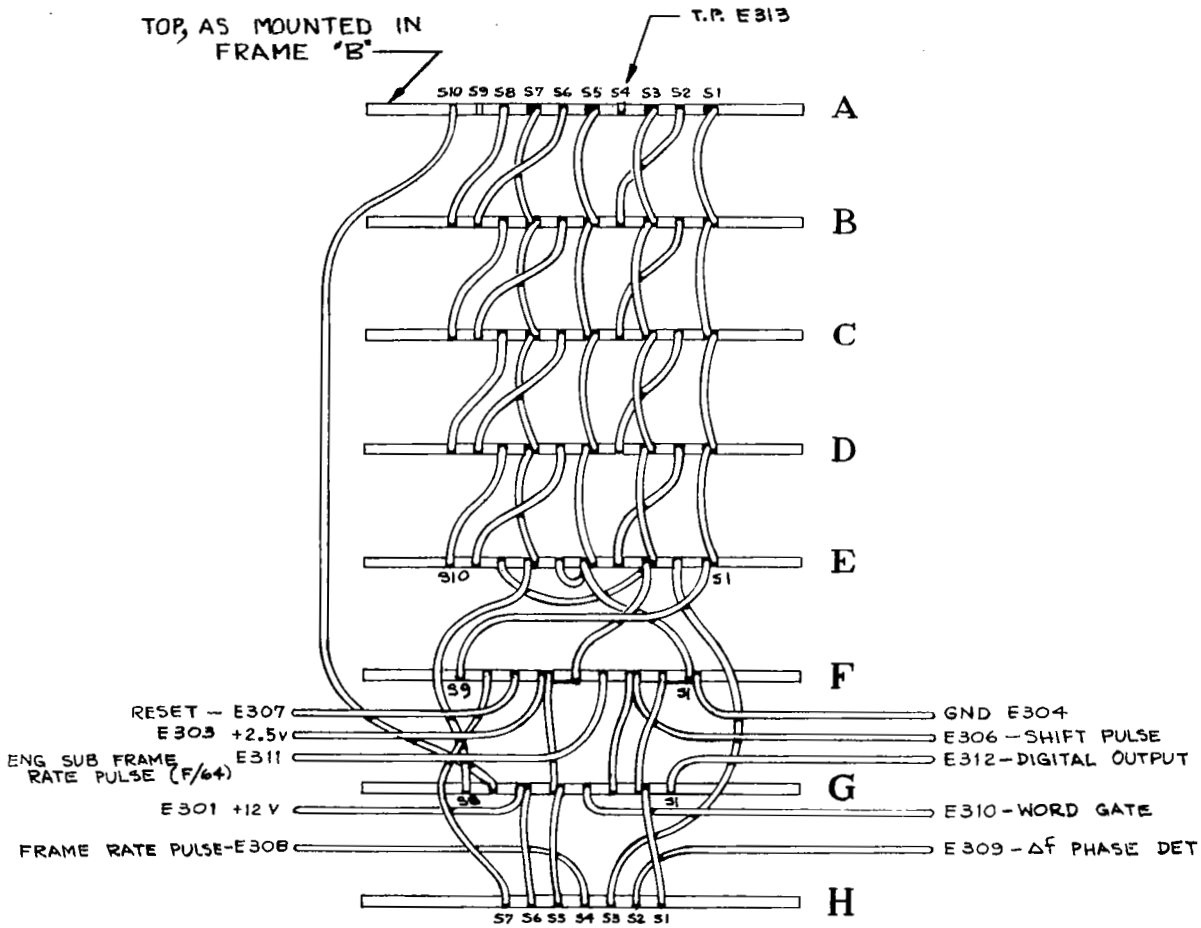



Figure 4.32 - The Four Types of Printed Circuits Boards used in the Counter Register



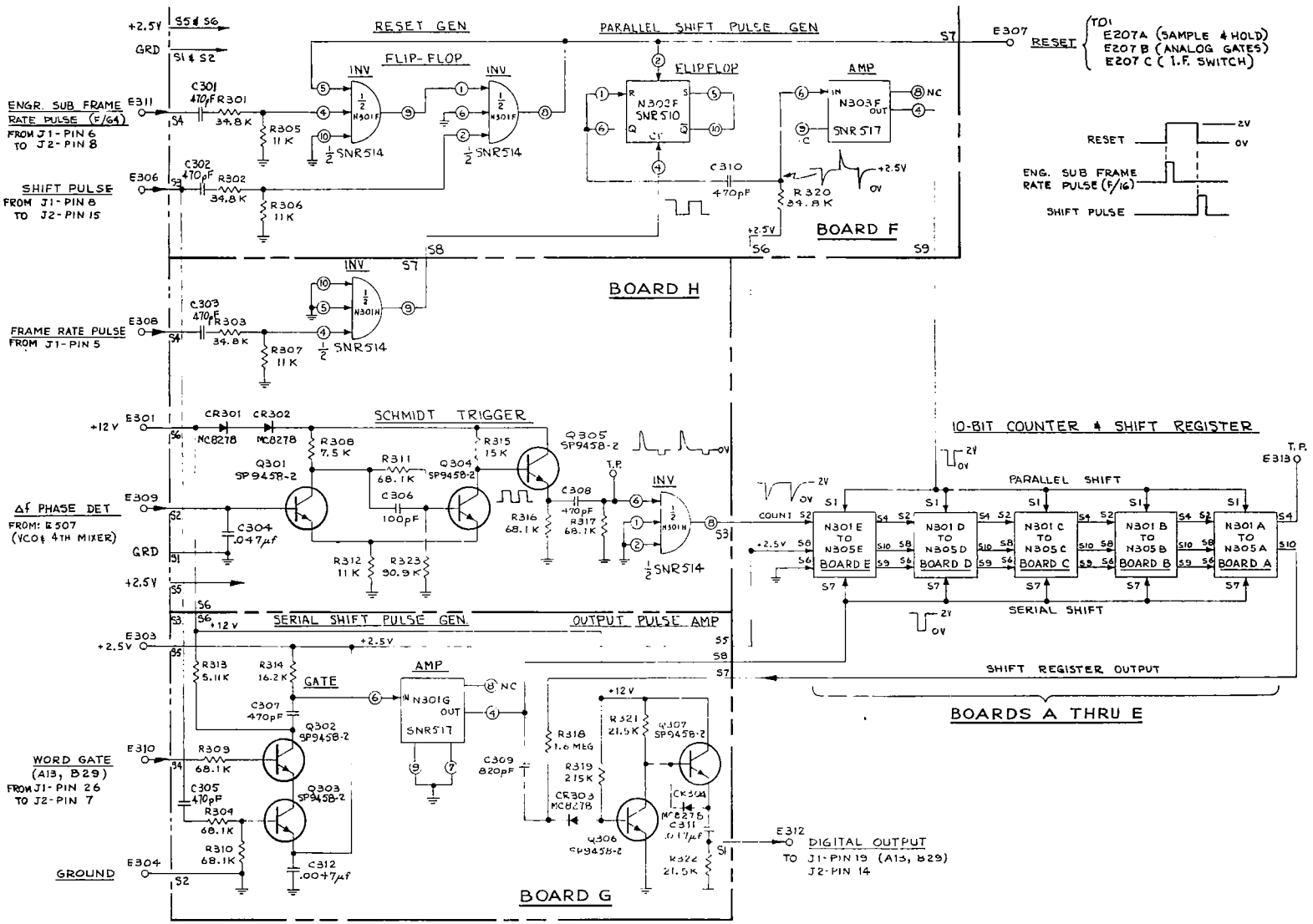

NOTE: INTEGRATED CIRCUITS FROM TEXAS INST. CO.

Figure 4.33 - Counter Register Boards A-E




END VIEW OF BOARDS, SHOWING INTERCONNECTING WIRING

Figure 4.34 - Counter Register Boards Interconnection Diagram




NOTE:

1.) ON ALL T.I. INTEGRATED CIRCUITS (SNR UNITS) PIN 3 = +2.5V AND PIN 7 = GROUND.

2.) SEE DWG. Nº C-4734-300-5 FOR INTERCONNECTING WIRING, AND WIRING TABLE.

3.) Q TYPE SP9458-2 ≈ 2N2483

Figure 4.35 Counter Register

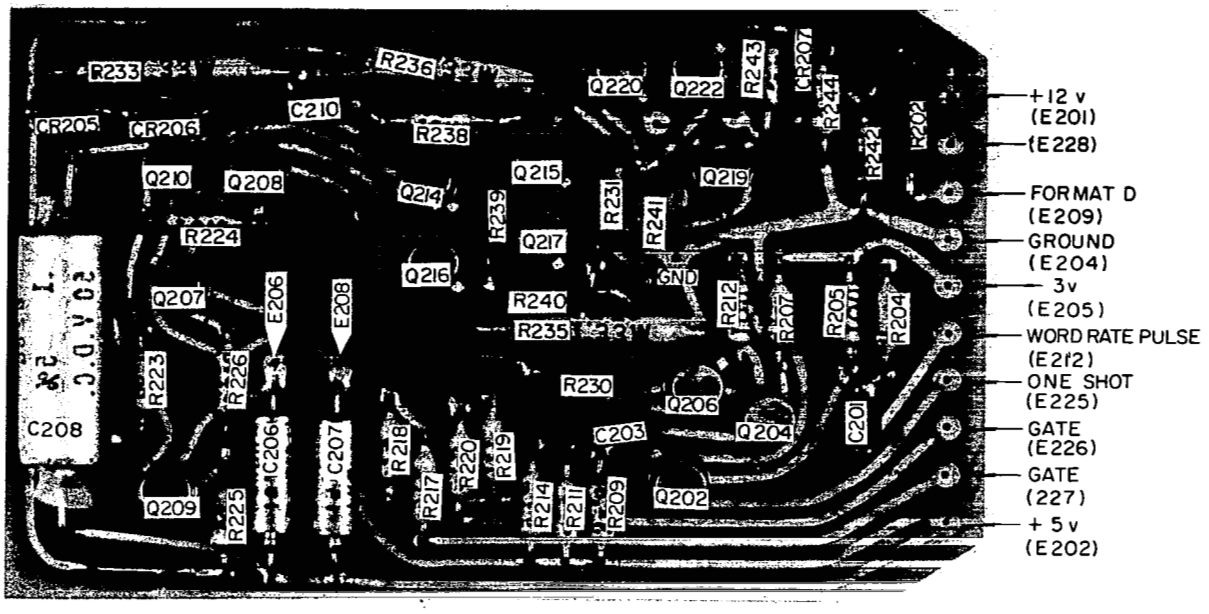
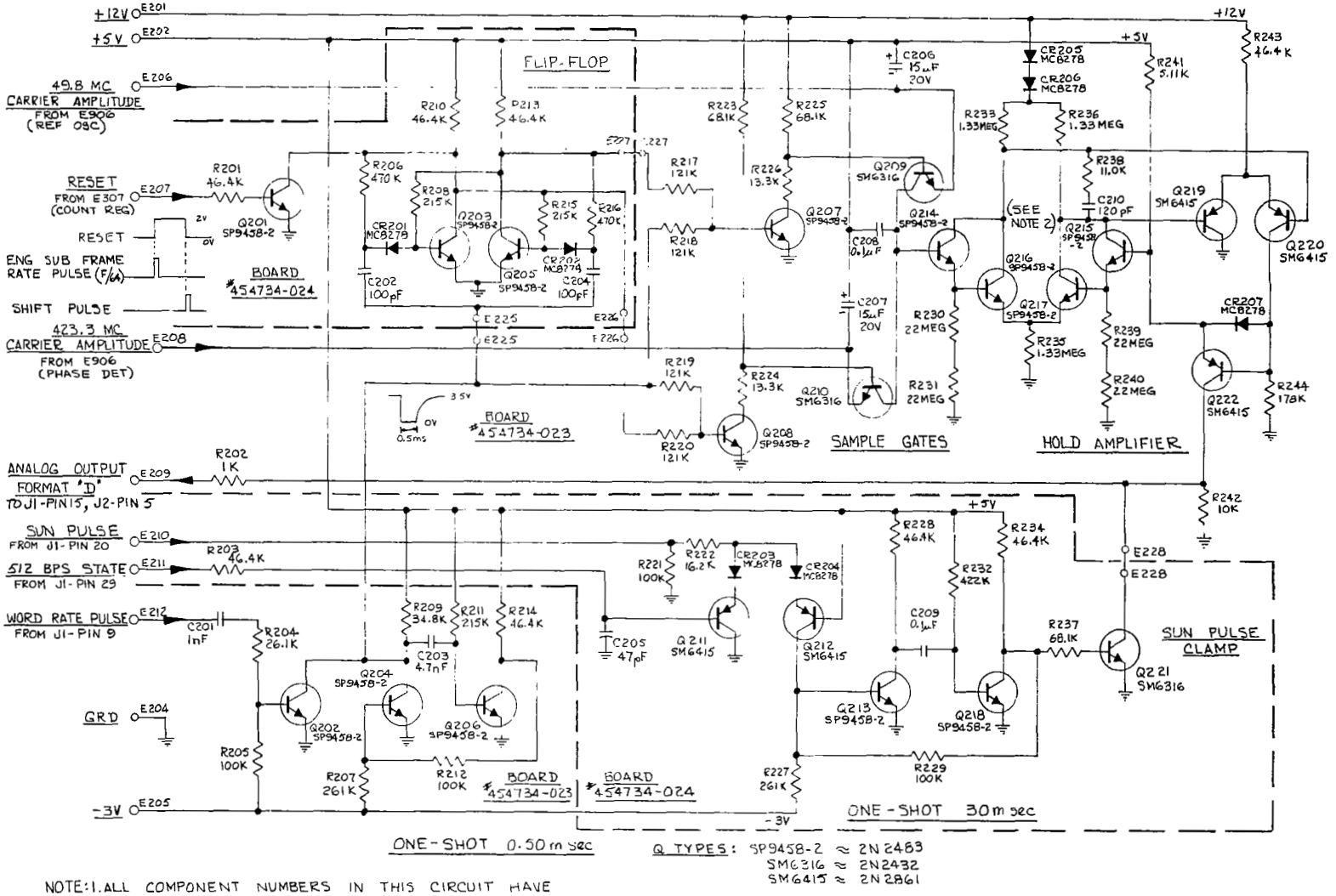



Figure 4.36 - Printed Circuits of the Sample and Hold - Wiring Side
Components are as seen through the wiring side.




NOTE: 1. ALL COMPONENT NUMBERS IN THIS CIRCUIT HAVE SUFFIX "A", i.e. R210A, C206A, ETC.
2. Q214 & Q215 ARE MATCHED PAIR.
Q216 & Q217 ARE MATCHED PAIR.
3. CIRCUITRY ON THIS DWG MOUNTED ON TWO BOARDS, SHOWN BY DOTTED LINES & CONNECTED BY E225, E226, E227 & E228. BOARD NOS. ARE SR1 #454734-023 & #454734-024.

Figure 4.37 Sample and Hold Circuit

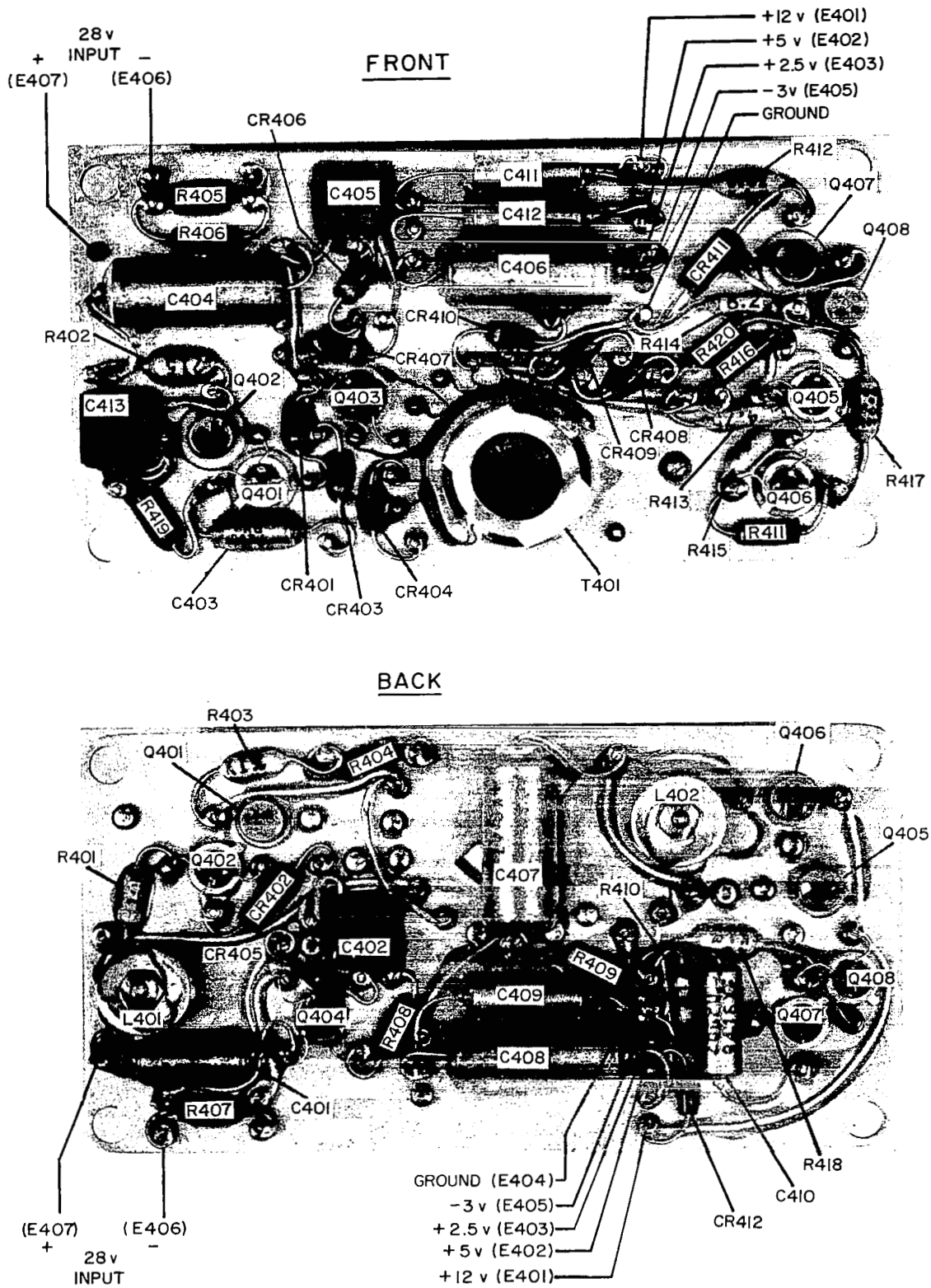
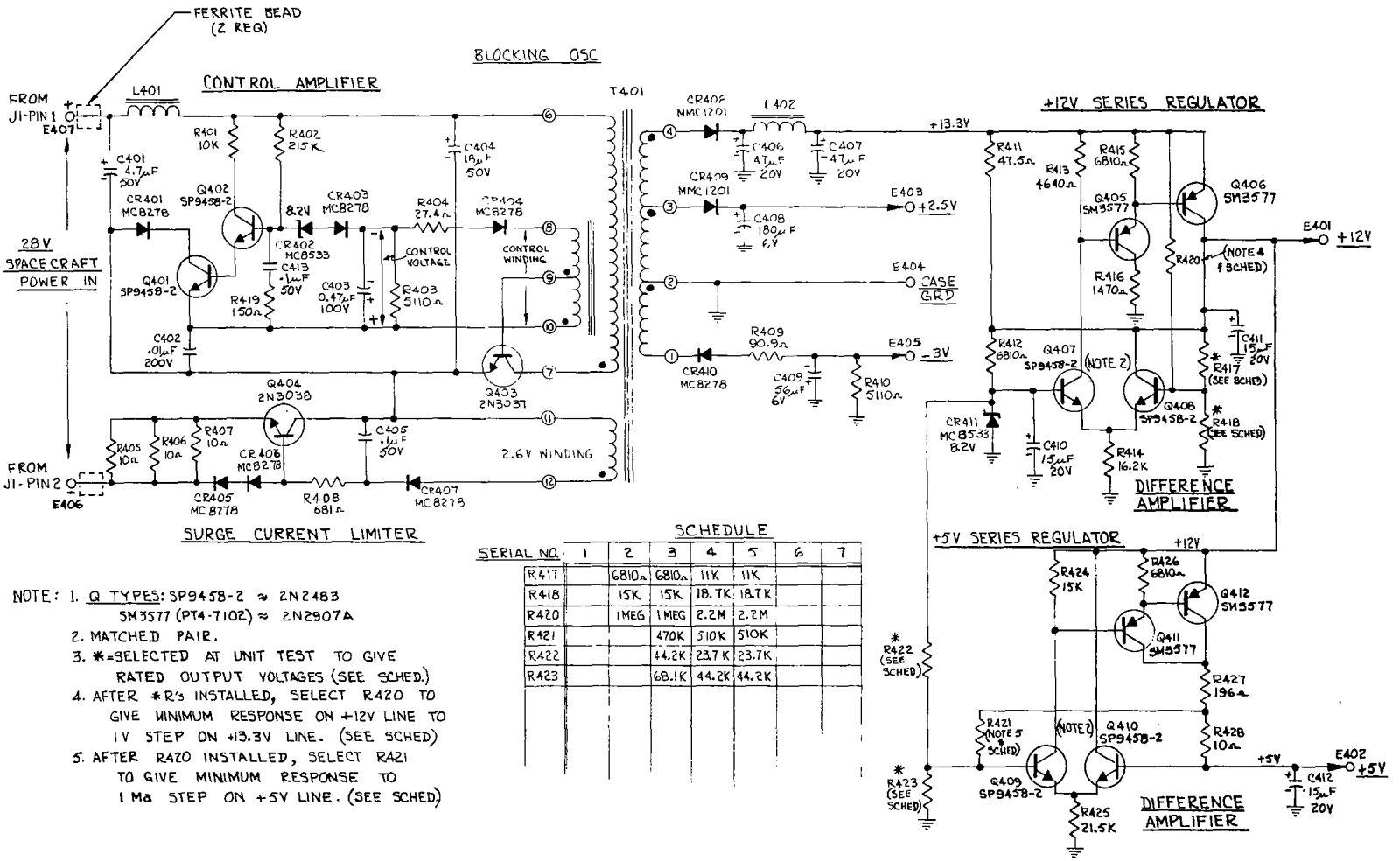



Figure 4.38 - Power Converter




SCHEDULE

| SERIAL NO. | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| R417 | | 6810Ω | 6810Ω | 11K | 11K | | |
| R418 | | 15K | 15K | 18.7K | 18.7K | | |
| R420 | | 1MEG | 1MEG | 2.2M | 2.2M | | |
| R421 | | | 470K | 510K | 510K | | |
| R422 | | | 44.2K | 23.7K | 23.7K | | |
| R423 | | | 68.1K | 44.2K | 44.2K | | |

NOTE: 1. Q TYPES: SP9458-2 ≈ 2N2483
SM3577 (PT4-7102) ≈ 2N2907A
2. MATCHED PAIR.
3. *=SELECTED AT UNIT TEST TO GIVE RATED OUTPUT VOLTAGES (SEE SCHED.)
4. AFTER *R's INSTALLED, SELECT R420 TO GIVE MINIMUM RESPONSE ON +12V LINE TO 1V STEP ON +13.3V LINE. (SEE SCHED)
5. AFTER R420 INSTALLED, SELECT R421 TO GIVE MINIMUM RESPONSE TO 1 Ma STEP ON +5V LINE. (SEE SCHED)

Figure 4.39 Power Converter

# 5. AREAS FOR IMPROVEMENT

The receiver in its present form works very well; indeed it was trouble-free even during the preliminary integration tests. If a redesign were contemplated, to meet new scientific or spacecraft requirements, there are a few minor areas that could be improved. These points, which have been found and explored as time would permit since the design freeze, are discussed in this section.

## 5.1 - 7 Mc Reference Oscillator

The 7 Mc IF signal of the 49.8 Mc channel phase modulates the 7 Mc reference oscillator through the phase detector. The magnitude of this modulation is multiplied by 18 in the local oscillator multiplier chain for the 423.3 Mc channel. When noise is the predominant component of the 49.8 Mc channel IF signal, the strong signal loop phase detector output of the 423.3 Mc channel has noise added to it. This noise has a 1/f spectral characteristic above 100 cps with the amplitude at 100 cps equal to the amplitude for noise alone in the 423.3 Mc channel.

This additional noise does not have any affect on the minimum lock level of the 423.3 Mc channel, probably because the noise modulation of the 423.3 Mc carrier is about 10 db below the carrier, independent of the carrier level. The presence of this modulation is undesirable, however, because the output of the 423.3 Mc channel is noisy when it should be clean.

This noise modulation can be considerably reduced by putting the buffer amplifier between the oscillator and both phase detector amplifiers. The change from the present configuration is shown in the block diagram, Figure 5.1. This change would require that the physical location of the reference oscillator and the buffer amplifier be interchanged, for the circuit oscillates when merely rewired without relocation. In addition, the buffer amplifier would have to be redesigned to give the same output whether or not the external load was connected. A voltage limiting buffer amplifier would fulfill this requirement.

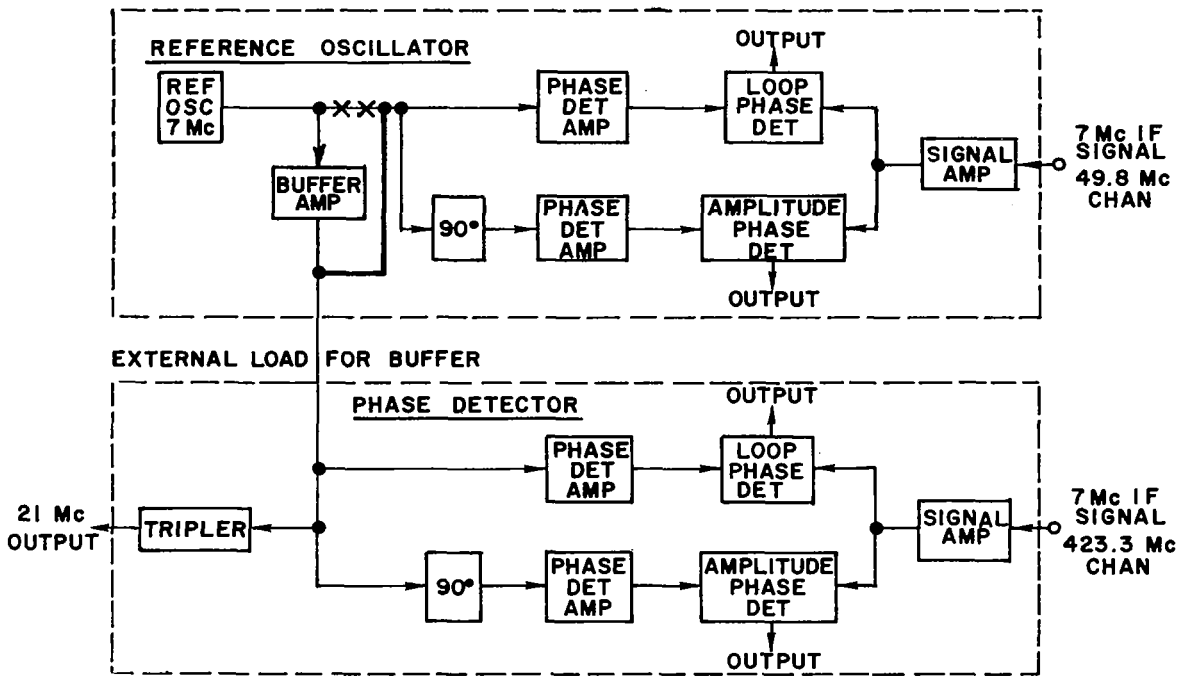



Figure 5.1 - Change Proposed in the Reference Oscillator Module
The change from the present system is indicated by the addition of the heavy line and the elimination of the x-ed out line.

A note on voltage limiting: The STL adjustable coil forms, as used in the output of the buffer amplifier, have relatively low L. Hence C is large ($X_C$ = 32 ohms at 7 Mc). Q $\approx$ 40 for the L, or the effective shunt resistance of the 7 Mc tuned circuit is $X_C$ Q = (32)(40) = 1280 ohms. Hence a 1 ma current can develop only 1.28 v. A larger L is necessary to make voltage limiting possible without excessive (> 2 ma) amplifier dc current.

## 5.2 - 31.9 Mc VCO

The VCO is extremely sensitive to power supply voltage changes; approximately 1300 cps/v for the 5 and 700 cps/v for the 12 v supply. For comparison, the VCO control input has a sensitivity of 950 cps/v. A voltage step of 0.8 mv on the 5 v supply causes a step of phase error of 0.5 radian at the 423.3 Mc channel loop phase detector output.

This problem was solved in the present receiver by the use of an

extremely stable power supply. A decrease of the VCO's sensitivity to power supply voltage changes would be the next logical step.

This could be accomplished by providing a local zener regulated 5 v supply for the VCO transistor and could bias one end of the Varicaps (see Figure 5.2). The control end of the Varicaps would then be at ground level as would the loop phase detector and the loop amplifier outputs. Thus, the VCO would be independent of steps on the common 5 v supply. The location of the VCO control voltage around ground level reduces the voltage level transfer circuit for the loop stress to a simple divider.

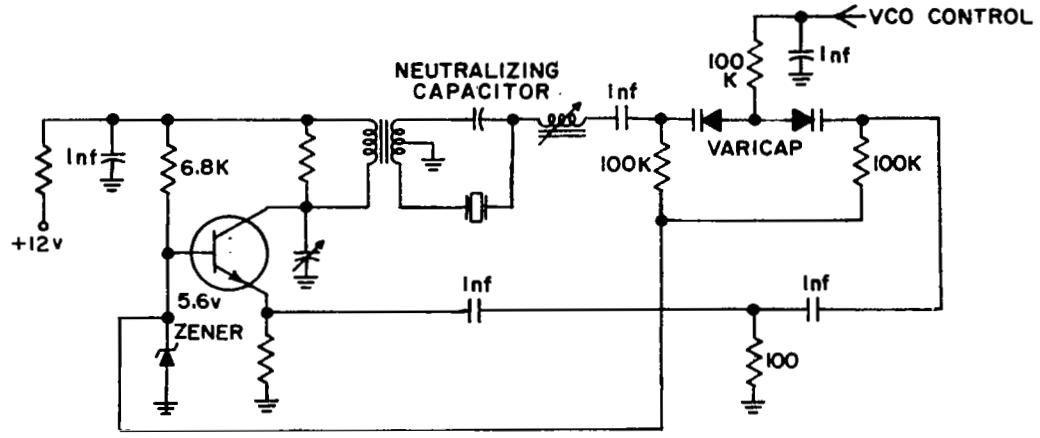



Figure 5.2 - Proposed 31.9 Mc VCO Circuit
Temperature compensation is not shown.

Loading of the VCO collector circuit should be increased so that small changes in tuning due to collector voltage changes have a smaller effect on the phase of the collector signal, and hence on the frequency of the VCO.

The autoformer (T807) could be removed if the crystal holder capacity were controlled by a neutralizing type capacitor, and the impedance level were modified by changing the Varicap size. Replacement of the autoformer with capacitors might very well make the VCO more stable with temperature and easier to adjust.

## 5.3 - Phase Detector Driver Amplifiers

The phase detector drivers (Q901, Q903 in Figures 4.13 and 4.15) draw approximately 5 ma per stage. The collector swing is less than the maximum available and an increase in the collector load impedance would allow this current to be reduced. Secondly, the 470 ohm collector decoupling resistor has a voltage drop of 2.5 v and could be replaced by a choke, thus saving 12.5 mw per phase detector driver or a total of 50 mw secondary power for the 4 phase detectors used in the receiver.

## 5.4 - Δf Phase Detector

This circuit causes cross coupling between channels of about -60 db. The cross coupling path is between the second mixers via the VCO connection through the Δf phase detector in the VCO and fourth mixer module (Figure 4.19). The VCO's do not pull each other.

While the circuit works satisfactorily, a decrease in cross coupling might be obtained by capacity neutralization of the Δf phase detector amplifiers, Q502 and Q503 in Figure 4.19. Less advisable is the insertion of an attenuator between the VCO signal and the base of the Δf phase detector amplifier.

## 5.5 - Front End

The image response of the 423.3 Mc channel is -4 db. If the image response were decreased, the noise figure would be decreased by as much as 1.4 db. A decrease in image response between the RF stage and the first mixer would be more effective in decreasing noise figure than a decrease in the image response before the RF stage.

The interference in the 423.3 Mc channel from the 49.8 Mc channel is about -66 db and about -72 db in the opposite direction. Since the noise temperature (including cosmic noise) of the 49.8 Mc channel is 7.5 db larger than for the 423.3 Mc channel, the 49.8 Mc signal will be about 10 db larger than the 423.3 Mc signal. Hence, in actual operation the interference in the 423.3 Mc channel from the 49.8 Mc channel will be -56 db.

Though this amount of cross talk is sufficiently low, conservative engineering practice makes improvement desirable. A -70 db cross coupling at 24.9 Mc exists between the collector circuits of the two first mixers, which is equal in both directions. The 26 db gain of the 49.8 Mc channel vs. the 18 db gain of the 423.3 Mc channel could account for the difference in cross coupling referred to the RF input. If increased decoupling of the power supply leads does not help, division of the front end into two separate modules should.

## 5.6 - Ferrite Tuning Slugs

Indiana General Q-3 ferrite, used for the tuning slugs in all the STL adjustable inductors decreases in $\mu_o$ below room temperature. Q-3 has a $\mu_o = 16$. Siemans ferrite tuning slugs made of U17 or 20K12 ferrite change very little in $\mu_o$ over -65° to +100°C. U17 has a $\mu_o = 10$ and a frequency range of 10 to 220 Mc. 20K12 has a $\mu_o = 24$ and a frequency range of 3 to 40 Mc. The adjustable inductors could use tuning slugs made of these ferrites. Siemans tuning slugs come in a range of sizes, but with millimeter threads. This is no problem, however, since the STL inductor forms are custom made.

## 5.7 - IF Switch

If the cross coupling between channels were decreased in the front end, the IF switch cross coupling would dominate. Part of this cross coupling path is through magnetic coupling of the 100 μh inductors. These can be changed to a 39 μh choke, which is self resonant at the IF switch operating frequency of 24.9 Mc. Alternatively, they could be replaced with toroidal inductors which would have less mutual coupling.

The best location for the IF switch is in the front end, instead of its present location. There is sufficient empty space in the present front end and the layout would require less cables, one less unit, and two less inductors (L201 and L204 in Figure 4.24) and would probably have less cross coupling.

## 5.8 - Sample and Hold

If the analog to digital (A-D) converter in the spacecraft quantized more quickly, i.e., fast with respect to the 10 cycle bandwidth of the sample and hold data, the sample and hold circuit would not be necessary. The A-D converter in the spacecraft originally ran at 1024 bps (16 ms conversion time), independent of the bit rate being transmitted by the spacecraft. During development, however, six gates were eliminated to "simplify the spacecraft," resulting in the converter running at the prevailing spacecraft data system rate (as slow as 64 bps for our use, or about 100 ms conversion time).

An alternative would be to use an individual A-D converter with conversion time sufficiently short to be able to dispense with the sample and hold circuit. This converter could be used for all the experiment's analog data. This alternative is even more attractive in view of the fact that the Jet Propulsion Laboratory had mysterious offset voltages with analog data wires running to a central A-D converter in Mariner II (Venus probe). As a consequence, they have changed to a voltage to time interval converter in each experiment in later spacecraft and all signals are transmitted through dc isolated pulse transformers on twisted pairs.

While the sample and hold circuit works well for the present experiment, it depends on high impedance (44 M) and high $h_{FE}$ at low $I_C$ (0.1 μa). The block diagram of an improved circuit is shown in Figure 5.3. In this circuit, the voltage stored is that necessary to make the output equal to the input. Dc offset in the sample driver, sample switch or hold amplifier are of no importance.

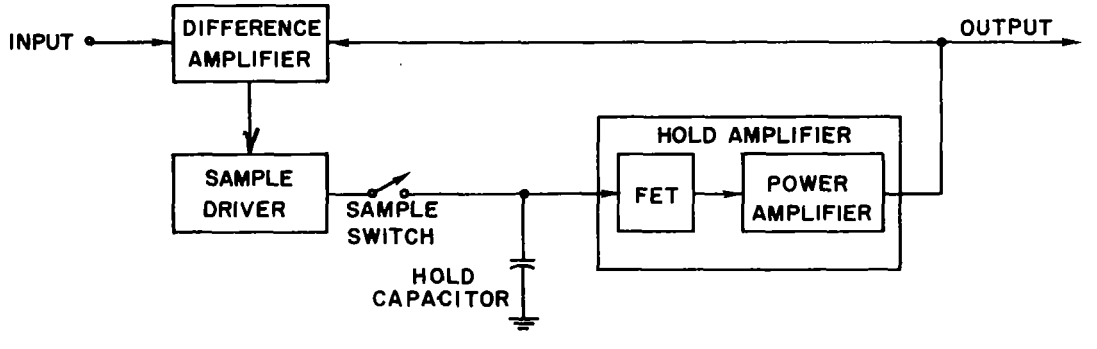



Figure 5.3 - Proposed Sample and Hold Circuit

The actual circuit is described in Reference 4. The circuit described samples 0 to 6 v in 1 μs and holds for 1 sec, all to an accuracy of 0.1 percent.

## 5.9 - TI SNR51 Integrated Circuits

The integrated circuit capacitors are reverse biased diodes. These capacitors will conduct if they are forward biased causing pulses to come out of inputs, in some cases. The capacitors also increase in capacity, as the voltage across them is decreased.

All or many of the components are insulated from the basic silicon slice by reverse biased diodes. The basic silicon slice is connected to ground. Hence, each point in the circuit is clamped to ground through a reverse biased diode.

The designer of the integrated circuits at TI said that the units work best when they are connected to other SNR51 units. This is why in some places an extra amplifier using one half of an SNR514is used.

He was very hesitant to say anything about ripple counters (the type used in the counter register). The SNR510 flip flops are susceptible to overdrive (clock pulse larger than the resistor gate level), so that if the flip flop driving a clock input had a larger signal than the flip flop being driven (which gates itself), it might not count. The use of a common clock signal for all the flip flops, which could be made smaller than the smallest gate input, or clamping all the signals with external diodes was strongly suggested. To obtain a counter with a common clock, a maximal length shift register, or a gated counter could be used.

The ripple counter used in the counter register does not work over the rated temperature range (-40° to +80°C) at a supply voltage of 6 v. However, it does work at the supply voltage of 2.5 v. It is suspected that the reverse biased diodes connected between all points and ground clip the negative going signal of the R-C gate thus, if both gates are overdriven, both R-C gate outputs become equal, and the flip flop can remain in its original stage. At lower supply voltages, the differences between the flip flop outputs, which are due to unequal collector resis-

tors (± 20 percent tolerance) and loads, are smaller than the 0.6 v required to overcome the grounded reverse biased diodes. In addition, there is a fraction of the clock pulse signal lost across the R-C gate capacitors which would absorb some of the overdrive.

## 5.10 - Loop Difference Amplifier

The output of the loop difference amplifier is current limited at ± 2 v relative to the 5 v supply. This is to keep from losing the 74.7 Mc signal by driving it beyond the 6 kc 3 db bandwidth of the 74.7 Mc crystal filter. The VCO has a nominal sensitivity of 950 cps/v which is multiplied by three in the derivation of the 74.7 Mc signal.

When the output of the amplifier nears its limit, it has insufficient dynamic current to drive the feedback network. The dynamic current required equals the current through the input resistor (R203, Figure 4.22) for the ± 1.5 v input signal. When the amplifier limits, the input signal feeds forward through the feedback network to the VCO control input causing a false lock condition due both to modulation of the VCO at the beat frequency and to phase shift throughout the phase lock loop. The false lock prevents the output of the loop difference amplifier from getting any nearer the ± 2 v limit. See Reference 5 for a derivation of the false lock condition. The current of the output stage was increased from 200 to 600 μa, but the output can still only be driven to about ± 1.5 v before dynamic current limiting begins.

A method of obtaining an output closer to the ± 2 v limit would be to provide a larger voltage output swing but to voltage limit the output with back to back 2 v zener diodes (or equivalent) across the feedback network (across R209). In this case, the diodes between the collectors of the first stage could be eliminated. Other methods would be to use a complementary pair emitter follower output or a 74.7 Mc crystal filter having a wider 3 db bandwidth, say 10 or 12 kc.

## 5.11 - Power Converter Transistor

The 2N3037 was selected for the blocking oscillator in the power converter, Q403, Figure 4.39, for its singular set of characteristics.

These are:

| Parameter | Value | Reason for selection |
|---|---|---|
| $V_{BE}$ | 120 v max | High, to survive the blocking oscillator leakage inductance transient |
| Fall time | 200 ns max | Short, for low dissipation |
| $V_{CE}$ (saturated) | 0.35 v max at 150 ma | Low, for low dissipation |
| $I_C$ | 500 ma | High, for the peak current |
| Power | 1 w | High, to survive abuse |
| Material | Silicon | Longer life |

There is the possibility that this transistor may burn out when the power converter output is disconnected or shorted. This was the best transistor available at the time, but a stronger transistor should be more reliable. If such a transistor is found, it could also be used to replace the 2N3038 used for Q404.

## 5.12 - Measurement of Δf without an Offset Frequency

A more sophisticated technique of counting the Δf is to use an up-down counter, and a Δf detector which also tells whether the Δf is positive or negative frequency. Positive frequency can make the counter count up, and negative frequency can make the counter count down.

With the new up-down counter scheme, a frequency bias will not have to be added at the ground based transmitters to determine the sign of the carrier frequency difference (Δf). Also, in the presently used scheme, a phase noise pulse larger than the hystersis of the level detector (about 0.6 radian) will cause an extra count. With the up-down counter, a phase noise pulse will not cause an unwanted count unless the phase lock loop skips a cycle. The up-down counter scheme, outlined in Figure 5.4, could be made from TI integrated circuits.

Figure 5.5 shows the position of the Δf vector which rotates about the origin. The projection of the vector on the level detector axis is the output of the level detector phase detector. The projection of the vector on the gate axis is the output of the gate phase detector. When

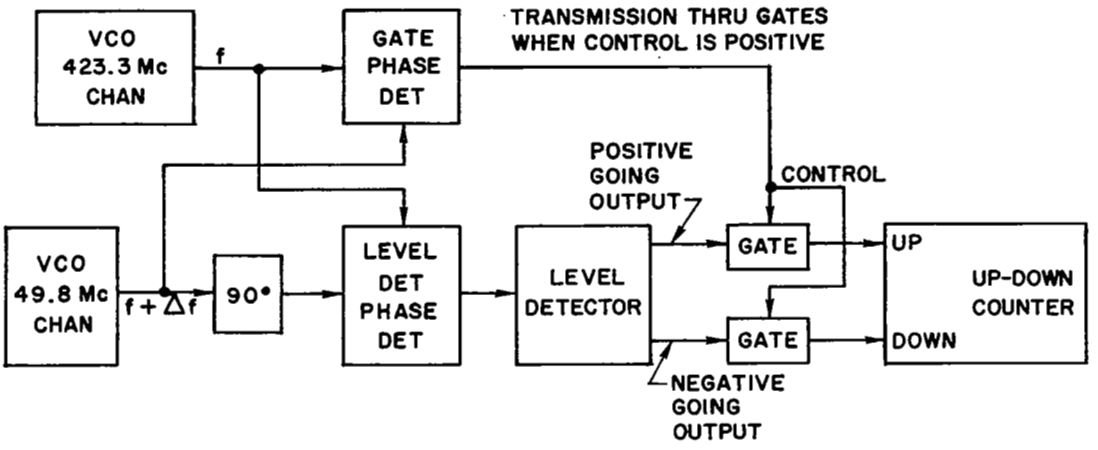
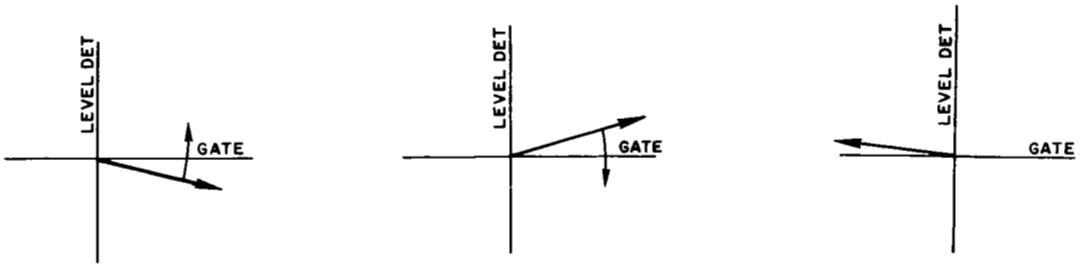



Figure 5.4 - Proposed Δf Phase Detector with an Up-Down Counter




a) Δf Vector for positive frequency

b) Δf Vector for negative frequency

c) Δf Vector passing through negative gate axis

Figure 5.5 - The Δf Vector for Several Conditions.

the vector rotates in the positive direction (counter-clockwise) through the positive gate axis, Figure 5.5a, the projection on the level detector axis goes from negative to positive, which produces a positive going output from the level detector. The projection of the vector on the gate axis is positive, so the positive going output goes through the gate and is added in the counter.

When the vector is rotating in the negative direction through the positive gate axis, Figure 5.5b, the projection on the level detector axis goes from positive to negative, which produces a negative going output from the level detector. The projection of the vector on the gate axis is positive, so the negative going output goes through the gate and is subtracted in the counter.

When the vector crosses through the negative gate axis, Figure 5.5c, the control to the gates is negative, and the output of the level detector does not go through the gates. Thus the level detector goes through the opposite transition than it did when the vector was going through the positive gate axis but this output is inhibited from being counted.

## 5.13 - Modulation Phase Measurement

The modulation phase measurement can be somewhat improved or it can be replaced by a radically different technique.

Slight modifications to the present scheme would be to combine the low and high pass sections of the 8 kc filter, Figure 4.26, into a single filter and to eliminate the emitter follower between sections. The same thing could be done for the 500 cps filter. In fact, the spectral density of the noise goes up only about 1.5 db if these filters are eliminated altogether, but the rms noise at the synchronous detector is larger. If the filters are eliminated, only a synchronous detector is necessary, i.e., no 8 kc to 500 cps mixer is needed, but the signal feeding the synchronous detector must be the "exclusive or" product of the 500 cps flip flop and the 8 kc flip flop.

The ac amplifier could be modified to provide a higher voltage output, thus the amplifier could have more gain without saturating. A higher gain dc amplifier might be desirable to provide a lower static phase error, especially at low signal levels. Some other form of VCO might be more stable. The noise bandwidth of the phase lock loop might be reduced. The dc amplifier following the phase detector (Figure 4.28) could be a difference amplifier feedback type, using 3 or 4 transistors.

The present scheme is sensitive to the noise centered around both input frequencies, 7.692 and 8.692 kc. Some method might be devised that would be sensitive to the noise only around the frequency to which it is locked.

A radical departure from the method presently used to determine the phase of the modulation would be to make the comparison before the IF crystal filter. The bandwidth is wide here, allowing high frequency

or high frequency content signals to be compared. In addition, the phase slope is very small, which would eliminate the need for the IF switch to calibrate the relative phase through the two channels.

A technique for accomplishing comparison of the incoming modulation with the expected modulation by the use of wideband modulation was developed at Jet Propulsion Laboratory; see References 6 and 7. The technique is to correlate the incoming signal with a local model of the expected signal. When they match, the correlator output is maximum. While this could be used with sinusoidal signals, JPL has developed a digital signal which is orthogonal to itself in auto correlation everywhere except over $\pm$ 1 bit length. Over these two bit lengths, it has a triangular auto correlation function.

This digital code is called a pseudo random code. Of the many digital codes available which have this type of orthogonality, there is one, the maximal length shift register code, which is generated with simple logical operations and a serial shift register. A code length equal to $2^n - 1$ characters is possible for an n bit serial shift register.

The use of the pseudo random code for measurement of group delay will allow high resolution by using a short bit length, and will resolve ambiguity by use of a code longer than any possible group delay. The bit length probably will be limited by the 100 to 200 kc bandwidth of the 400 kw VHF (20 to 55 Mc) transmitter.

A bonus with this scheme is that the IF crystal filter can be narrowed down to something like a 2 kc bandwidth from the present 45 kc. This will reduce the rms noise at the phase detector, although the power spectral density will remain the same. The narrowing of the IF crystal is permissable because the modulation is used before the IF crystal filter.

APPENDIX A

RECEIVER PHASE LOCK LOOP PERFORMANCE

A.1 - Anticipated Received Signal Level at the Receiver

The Stanford receiver is a limiting receiver which has about 30 db excess gain over that needed to limit on noise alone. Therefore, only signal-to-noise ratios are important, not absolute signal levels. The basic equation for received signal levels in the line of sight situation is:

$$P_R = \frac{P_T G_T A_R}{4\pi R^2} \qquad (1)$$

$P_R$ = received power at the input to the receiver (watts)

$P_T$ = transmitted power (watts)

$G_T$ = power gain of the transmitting antenna over isotropic

$A_R$ = area of the receiving antenna ($m^2$)

$R$ = distance between transmitting and receiving antennas (m)

For this experiment, there is a 150 foot parabolic antenna on the ground and the equivalent of a dipole antenna on the spacecraft. The power gain of a parabola is:

$$G_T = \frac{4\pi A_T}{\lambda^2} = \frac{4\pi\ (\pi r_T^{\ 2})}{\lambda^2}$$

$A_T$ = area of trnsmitting antenna ($m^2$)

$r_T$ = radius of $A_T$ (m)

$\lambda$ = wavelength of transmitted frequency (m)

The area of a dipole, which has a power gain of $G_R = 1.64$, is:

$$A_R = \frac{G_R \lambda^2}{4\pi} = \frac{1.64\ \lambda^2}{4\pi}$$

Inserting the expressions for $G_T$ and $A_R$ into eq. (1)

$$P_R = \frac{P_T \left[\frac{4\pi(\pi r_T^2)}{\lambda^2}\right] \left[\frac{1.64\ \lambda^2}{4\pi}\right]}{4\pi R^2} = P_T \frac{0.41\ r_T^2}{R^2}$$

Converting this to db form:

$$P_R\ (\text{dbm}) = P_T\ (\text{dbm}) - 20 \log R + 20 \log r_T - 3.87 \qquad (2)$$

The actual value of $P_R$ is less than calculated by eq. (2) due to the following factors:

1 db transmitting transmission line loss

3 db transmitting antenna aperture efficiency

3 db loss because circular polarization is transmitted and linear polarization is received. Circular polarization is required for one experiment goal of the experiment and to insure that Faraday fading does not adversely affect the received signal level.

---

7 db total additional reduction in $P_R$

Substitute the following values and the 7 db additional reduction of $P_R$ into eq. (2):

$P_T$ (423.3 Mc) = 30 kw = 74.77 dbm

$P_T$ (49.8 Mc) = 400 kw = 86.0 dbm

$r_T$ = 22.9 m for the Stanford 150 foot dish

$$P_R\ (423.3\ \text{Mc}) = (86\ \text{dbm} - 20 \log R + 27.2 - 3.87) - 7$$
$$= 102.3 - 20 \log R \quad (\text{dbm})$$

$P_R$ (423.3 Mc) (received power by a dipole) vs. range is plotted in Figure A.1.

$$P_R\ (49.8\ \text{Mc}) = (74.77\ \text{dbm} - 20 \log R + 27.2 - 3.87) - 7$$
$$= 91.1 - 20 \log R \quad (\text{dbm})$$

$P_R$ (49.8 Mc) (received power by a dipole) vs. range is plotted in Figure A.2. This is total received power. The carrier is modulated for the group path experiment, and half the power goes into the sidebands

while half remains in the carrier. That is, the carrier power is 3 db lower than the total received power, $P_R$. This reduction of carrier power is taken into account by the expressions for the phase lock loop performance, Section A.4.

## A.2 - Equivalent Input Noise Temperature of the Two Receiver Channels

Input noise due to the receiving system:

$$\text{Noise Figure} = NF = \frac{T_{out}}{T_{ref}} = \frac{T_{ref} + T_A}{T_{ref}}$$

$$T_A = T_{ref} (NF - 1)$$

$$T_{ant} = \frac{T_A}{G_{lead\text{-}in}} = \frac{T_{ref} (NF - 1)}{G_{lead\text{-}in}}$$

$T_{out}$ = amplifier output temperature, referred to amplifier input (°K)

$T_{ref}$ = temperature of reference source = 293°K for noise figure measurements

$T_A$ = temperature added to amplifier input by the amplifier (°K)

$T_{ant}$ = temperature referred to antenna terminals, without cosmic noise added (°K)

$G_{lead\text{-}in}$ = gain in the antenna coax (< 1)

### Input noise due to cosmic noise

Cosmic noise, expressed in terms of temperature, was obtained by numerically integrating sky maps of cosmic noise (Reference 8) and scaling to frequency using -23.2 db/decade as the scaling factor (Reference 9). At 423.3 Mc the cosmic noise is about 100°K and is much below the receiver noise.

At 49.8 Mc a 250 Mc sky map in galactic coordinates was integrated, frequency scaled, and weighted by the gain pattern of a dipole parallel to the galactic axis. For comparison, several lower frequency sky maps were frequency scaled and integrated with no weighting; then 2 db (the maximum gain of a dipole) was added. The temperatures obtained by the two methods for 49.8 Mc were 7150°K and 8100°K respectively. At 49.8 Mc, 8000°K of cosmic noise is used in the calculations.

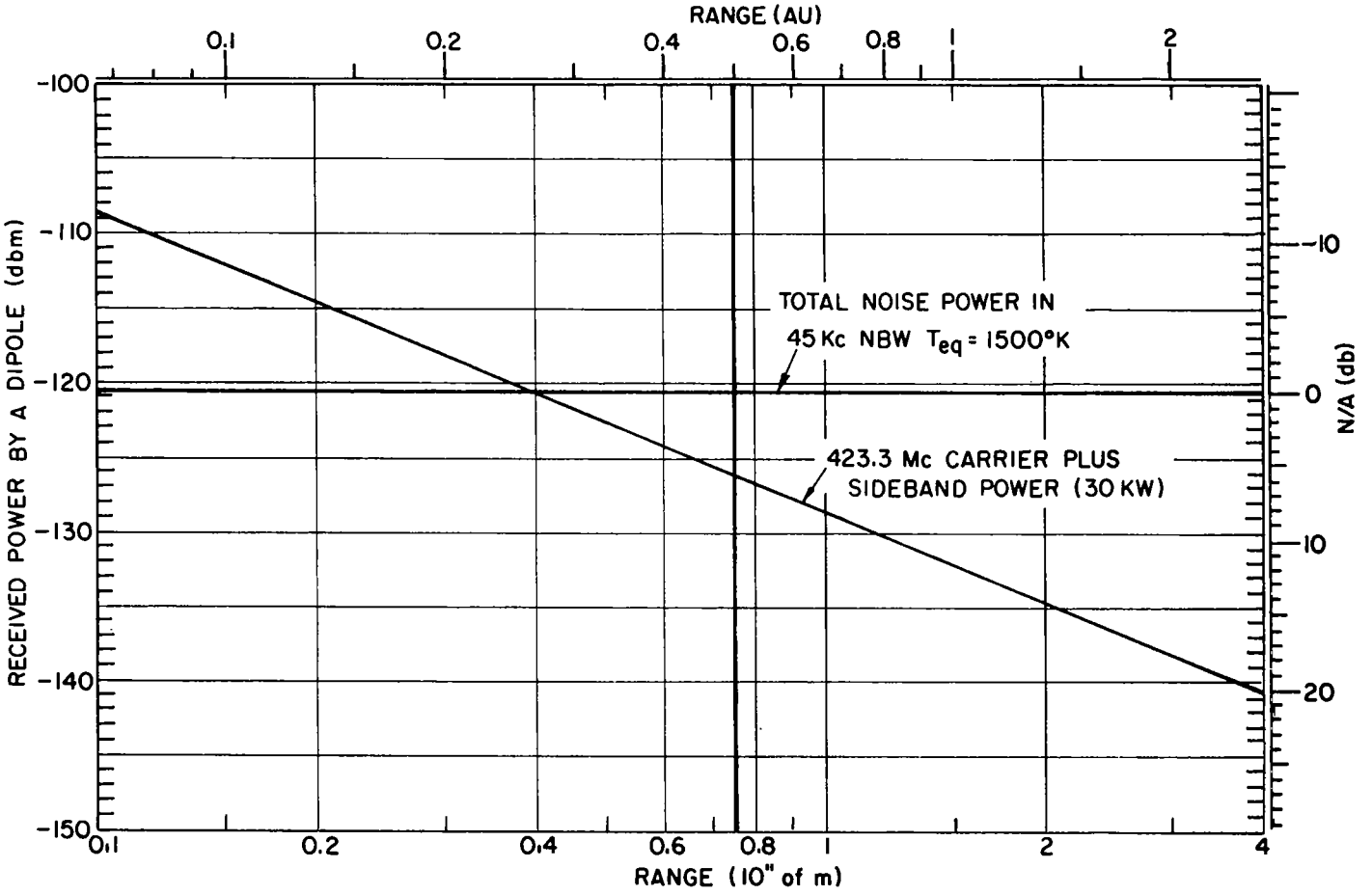



Figure A.1 - 423.3 Mc Power Received by a Dipole at the Spacecraft vs. Range
The right hand scale is the total noise power to carrier plus sideband power in the IF noise bandwidth of 45 kc.

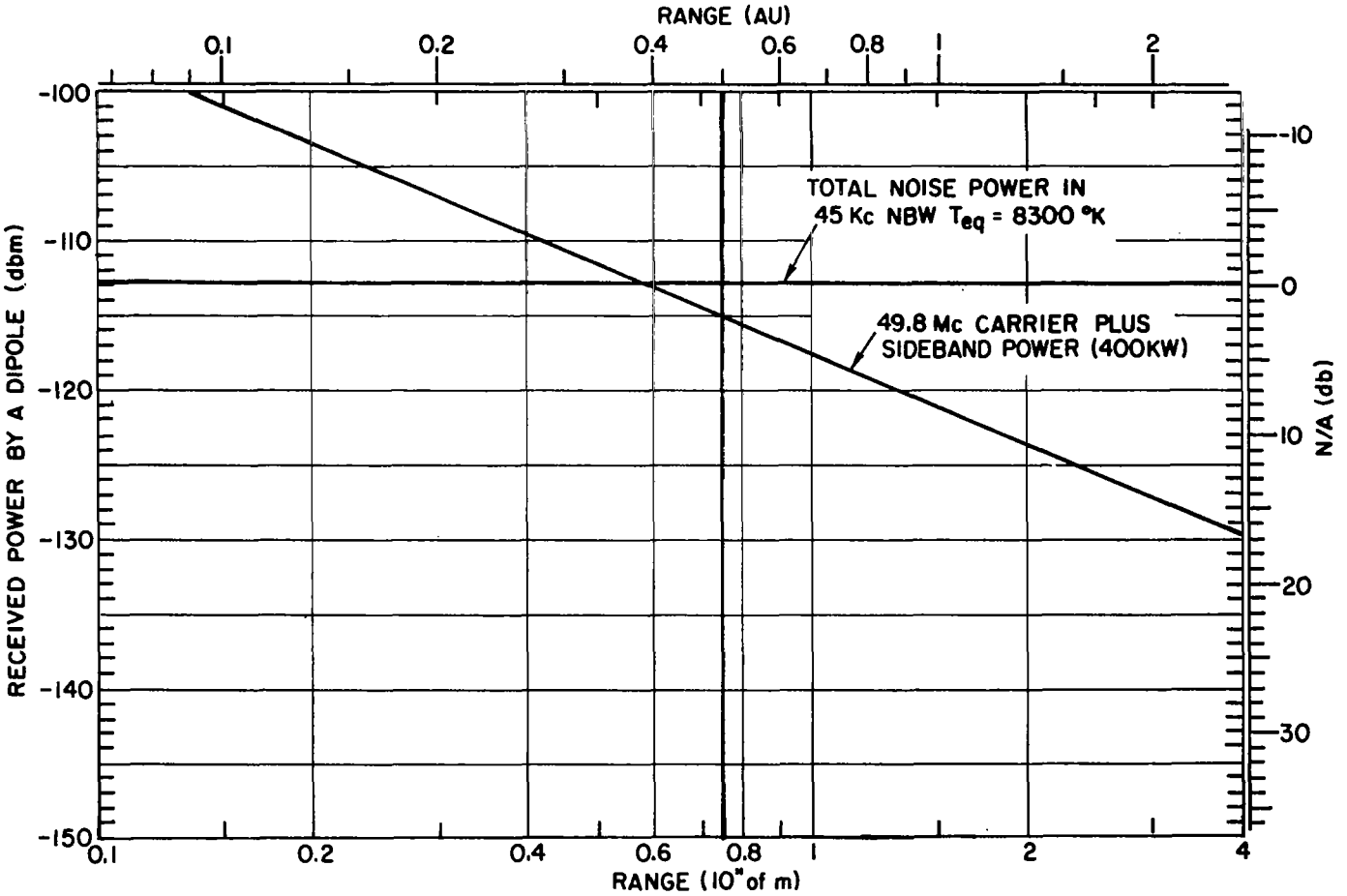



Figure A.2 - 49.8 Mc Power Received by a Dipole at the Spacecraft vs. Range
The right hand scale is the total noise power to carrier plus sideband power in the IF noise bandwidth of 45 kc.

Total input noise

$$T_{eq} = T_{ant} + T_{cosmic} = \frac{T_{ref}\,(NF-1)}{G_{lead\text{-}in}} + T_{cosmic} \qquad (3)$$

$T_{eq}$ = total equivalent noise temperature at the antenna terminals

$T_{cosmic}$ = cosmic noise temperature, discussed above

Total noise power in same noise bandwidth as seen by the limiters in the receiver

$$N_o = K\,T_{eq} \quad \text{(watts/cps)}$$

$$P_N = N_o\,NBW = K\,T_{eq}\,NBW \quad \text{(watts)}$$

$P_N$ stated in dbm form is:

$$P_N = 10 \log K + 30 + 10 \log T_{eq} + 10 \log NBW \text{ (dbm)} \qquad (4)$$

$P_N$ = total noise power referred to antenna terminals (watts/cps)

$K$ = Boltzmann's constant = $1.38 \times 10^{-23}$ (joules/°K)

$N_o$ = power spectral density (one sided, i.e. positive frequencies only) ( watts/cycle)

NBW = equivalent rectangular bandwidth which passes as much noise as an actual filter. The NBW as seen by the limiters in the receiver is 45,000 cps (cps).

Total noise power in 423.3 Mc channel

NF = 7 db = 5.0

$T_{cosmic}$ = 100°K

$G_{lead\text{-}in}$ = (6 ft) (-0.13 db/ft at 423.3 Mc) = -0.78 db = 0.84

Inserting these values into eq. (3):

$$T_{eq} = \frac{(293)(5-1)}{0.84} + 100 = 1500°K$$

Inserting values into eq. (4):

$$P_N \text{ (423.3 Mc)} = 10 \log (1.38 \times 10^{-23}) + 30 + 10 \log (1.5 \times 10^{3}) + 10 \log (4.5 \times 10^{4})$$

$$= -228.6 + 30 + 31.76 + 46.53 = -120.3 \text{ dbm}$$

$P_N$ (423.3 Mc) of -120.3 dbm is plotted on the $P_R$ (received power by a dipole) vs. range graph for 423.3 Mc, Figure A.1.

Total noise power in 49.8 Mc channel

NF = 3 db = 2

$T_{cosmic} = 8000°K$

$G_{lead\text{-}in} = 1$

Inserting these values into eq. (3):

$$T_{eq} = \frac{(293)\ (2\text{-}1)}{1} + 8000 = 8293°K$$

Inserting values into eq. (4):

$$P_N\ (49.8\ Mc) = 10 \log\ (1.38 \times 10^{-23}) + 30 + 10 \log\ (8.293 \times 10^3) + 10 \log\ (4.5 \times 10^4)$$

$$= -228.6 + 30 + 39.19 + 46.53 = -112.9\ dbm$$

$P_N$(49.8 Mc) of -112.9 dbm is plotted on the $P_R$ (received power by a dipole) vs. range graph for 49.8 Mc, Figure A.2.

The cosmic noise at 49.8 Mc is 14 db larger than the receiver noise. Attenuation of the signal from the antenna will not appreciably change the signal to noise ratio, unless the cosmic noise is less than 3 db greater than the receiver noise.

## A.3 - Total Noise to Total Signal Ratio (N/A) at the Limiter Output

The performance calculations for the phase lock loop are in terms of the total noise to total signal (carrier and sidebands) ratio at the input to the limiter and not in terms of absolute signal levels at the receiver input. The noise to signal ratio is given on the right hand scale of the plots of $P_R$ (power received by a dipole) vs. range, Figures A.1 and A.2.

Selection of the maximum N/A at which the receiver will operate

First the N/A for a dipole at the maximum range (0.5 AU) is read off the graphs, Figure A.1, for 423.3 Mc and Figure A.2 for 49.8 Mc. The spacecraft antenna pattern has nulls in it of 8 db below a dipole, which amplitude modulate the received signal as the spacecraft rotates at 1 rps. At the nulls, the N/A is increased by the amount that the

gain of the null is below the gain of a dipole. The N/A is increased because the signal is reduced by the null, but the cosmic noise is more isotropic, hence is affected little by the directional nulls; the receiver noise is not affected by the nulls at all.

At 49.8 Mc there can be fading on one of the characteristic transmission modes through the ionosphere of up to 3 db. The N/A at 49.8 Mc is increased 3 db by this fading.

Some margin in N/A is added to allow the signal to decrease or the noise to increase from these calculated values, and still have the receiver work. At 423.3 Mc, the signal can decrease, and the noise can increase due to an increase in receiver noise figure. At 49.8 Mc, the signal can decrease, but the receiver noise figure would have to increase from 3 to 11 db to increase the N/A, which is very unlikely. More margin is, therefore, required at 423.3 Mc than at 49.8 Mc.

| | 423.3 Mc | 49.8 Mc | |
|---|---|---|---|
| N/A for a dipole at 0.5 AU range | 5.8 | 2.2 | db |
| N/A for antenna nulls | 8 | 8 | db |
| N/A for ionospheric fading | 0 | 3 | db |
| N/A for margin | 10 | 6 | db |
| Design level of N/A for a mean time of 10 hr for skipping 1 cycle in the phase lock loop | 23.8 | 19.2 | db |

The design level N/A above is what it should be with what is now known. However, after the design freeze, the noise figure in the 423.3 Mc channel was found to be higher than planned, a 1 db difference involved in an approximation was lost, the fading on the 49.8 Mc channel is less severe than originally supposed, and less margin was included. As a consequence, the design level N/A used in the present receiver is 21 db for the 49.8 Mc channel and 18 db for the 423.3 Mc channel.

## A.4 - The Phase Lock Loop

The linearized phase lock loop is shown in Figure A.3.

The equations for the performance and parameters of the phase lock loop are:

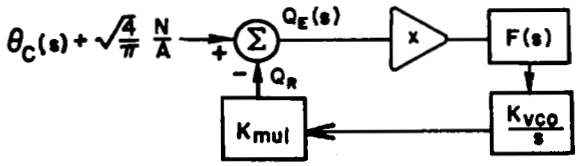



Figure A.3 - Linearized Phase Lock Loop

Laplace or Fourier transform of output phase vs. input phase

$$\frac{\theta_R}{\theta_C} = \frac{x(\sqrt{2}\ B_o s + B_o^2)}{s^2 + x(\sqrt{2}\ B_o s + B_o^2)}$$

Laplace or Fourier transform of error phase vs. input phase

$$\frac{\theta_E}{\theta_C} = \frac{s^2}{s^2 + x(\sqrt{2}\ B_o s + B_o^2)}$$

Ratio of amplitude of the carrier to its design level vs. noise power to signal power, $(N/A)^2$

$$x^2 = (A/A_1)^2 = \frac{1 + \frac{4}{\pi}\left(\frac{N_1}{A_1}\right)^2}{1 + \frac{4}{\pi}\left(\frac{N}{A}\right)^2}$$

Rms phase noise in the loop

$$\sigma_N^2 = N_o\ B_L = \left(\frac{4}{\pi A^2}\frac{N^2}{\frac{P_{car}}{P_{tot}}}\frac{1}{\Delta f}\right)\left(B_o\ \frac{2x+1}{4\sqrt{2}}\right) \quad (rad^2)$$

Noise bandwidth in the phase lock loop

$$B_L = B_o\ \frac{2x+1}{4\sqrt{2}} \quad (cps)$$

One sided power spectral density in the loop or before the phase detector. This expression is close enough for $N/A > 3$ db

$$N_o = \frac{4}{\pi}\frac{N^2}{A^2}\frac{1}{\frac{P_{car}}{P_{tot}}}\frac{1}{\Delta f} \quad (rad^2/cps)$$

Mean time to loss of lock

$$T = \frac{\pi}{4 B_L} e^{2/\sigma_N^2} \quad \text{(sec)}$$

3 db bandwidth of the output phase, $\Theta_R$

$$f_{R\ 3\ db} = \frac{B_o}{2\pi} \sqrt{x(x+1) + \sqrt{[x(x+1)]^2 + x^2}} \quad \text{(cps)}$$

3 db bandwidth of the loop error phase, ($\Theta_E$ decreases with decreasing freq.)

$$f_{E\ 3\ db} = \frac{B_o}{2\pi} \sqrt{x(x-1) + \sqrt{[x(x-1)]^2 + x^2}} \quad \text{(cps)}$$

Amplitude of the carrier at the phase detector output

$$A = \sqrt{\frac{L^2 \frac{P_{car}}{P_{tot}}}{[1 + \frac{4}{\pi} (\frac{N}{A})^2]}} \quad \text{(v, 0 - pk)}$$

Loop parameter (undamped resonant frequency at design level)

$B_o$ ($\frac{rad}{sec}$), solved from expression for $\sigma_n^2$, once $\sigma_n^2$ is decided upon. $x = 1$ at design level.

$(N/A)^2$ = noise to signal power ratio in the IF noise bandwidth, $\Delta f$

$(N_1/A_1)^2$ = design level of $(N/A)^2$

$A_1$ = design level of A, i.e., A for $(N/A)^2 = (N_1/A_1)^2$ (v)

$\frac{P_{car}}{P_{tot}}$ = fraction of total signal power in the carrier

L = limiting output amplitude (0 - pk) out of the phase detector (v)

$\Delta f$ = IF noise bandwidth (cps)

Selection of the loop parameters

First, the maximum N/A at which the receiver is desired to operate is determined from the anticipated signal and noise levels. This is the design level $N_1/A_1$, because the performance should be optimum at

the most difficult operating point. The design level N/A was determined in Section A.3 to be 18 db for the 423.3 Mc channel and 21 db for the 49.8 Mc channel.

Second, the mean time to skip 1 cycle is decided upon. One day's operation, or about 10 hours, was chosen for the Stanford receiver. Then $\sigma_N^2$ is determined from the equation for T. $\sigma_N^2$ is a logarithmic function of $B_L$, so the exact value of $B_L$ does not affect $\sigma_N^2$ very much. For $B_L$ = 100 and T = 36000 sec (10 hr), $\sigma_N^2$ is -8.7 db.

With $N_1/A_1$ and T decided upon, everything else is determined by the equations. Table A.1 shows the calculated performance vs. N/A for the 423.3 Mc channel with design level $N_1/A_1$ = 18 db. Table A.2 shows the same thing for the 49.8 Mc channel with design level $N_1/A_1$ = 21 db.

Derivation of the phase lock loop equations

$\theta_R/\theta_C$, $\sigma_N$ came from Jaffe and Rechtin (Reference 10). $\theta_E/\theta_C$ was easily derived from Jaffe and Rechtin. $x = A/A_1$ came from Jaffe and Rechtin with a slight correction from Davenport (Reference 11) (Jaffe and Rechtin made an approximation $4/\pi \approx 1$). The quantities $N_o$ and $A_o$ in Jaffe and Rechtin have been changed to $N_1$ and $A_1$ to allow $N_o$ to be used for one sided power spectral density.

$B_L$, $N_o$ are an identification of the parts of $\sigma_N$, divided up in the same way as by Viterbi (Reference 12). Viterbi shows (p. 1738) that a synchronous detector is sensitive to all the signal, but to only half the noise. This is not the case for a non synchronous detector. The one sided noise power density in the IF, when folded about the synchronous detector frequency is doubled in density. But the phase detector is sensitive to only half the noise, so the one sided noise power density is the same at the output of the phase detector as at the input.

T came from Viterbi, and is the exact solution for a first order phase lock loop with zero dc phase error. The exact solution for the second order loop is too difficult to be of interest for the present problem and it is felt that the first order loop solution is a reasonable guide for the performance of the second order loop.

Table A.1 - 423.3 Mc Calculated Phase Lock Loop Performance

phase lock loop performance vs n/a (total noise to total signal power in if)

limit n/a design level = 18 db
design n/a level = 18 db
limit sigma (loop n/a) level = -8.7 db
b (loop parameter) = 71.2 rad/sec
if noise bandwidth = 45000. cps
maximum amplitude phase detector output = 1.500
fraction of total power in carrier = .50

| n/a db | margin db | amplitude v | out f3db cps | err f3db cps | nbw cps | sigma db | sigma rad | time min |
|---|---|---|---|---|---|---|---|---|
| strong carrier | | 1.500 | 212.4 | 196.4 | 333.8 | | | |
| strong signal | | 1.060 | 152.5 | 136.6 | 239.7 | | | |
| 0 | 18 | .703 | 103.8 | 87.9 | 163.2 | -20.3 | .096 | |
| 1 | 17 | .657 | 97.5 | 81.6 | 153.3 | -19.6 | .104 | |
| 2 | 16 | .610 | 91.1 | 75.3 | 143.3 | -18.9 | .113 | |
| 3 | 15 | .563 | 84.7 | 68.9 | 133.3 | -18.2 | .122 | |
| 4 | 14 | .517 | 78.5 | 62.6 | 123.4 | -17.5 | .132 | |
| 5 | 13 | .473 | 72.4 | 56.6 | 113.9 | -16.9 | .142 | |
| 6 | 12 | .430 | 66.6 | 50.8 | 104.7 | -16.2 | .153 | |
| 7 | 11 | .390 | 61.1 | 45.4 | 96.1 | -15.6 | .165 | |
| 8 | 10 | .352 | 55.9 | 40.4 | 88.1 | -15.0 | .177 | .581e 24 |
| 9 | 9 | .318 | 51.2 | 35.7 | 80.7 | -14.4 | .190 | .140e 21 |
| 10 | 8 | .286 | 46.8 | 31.5 | 73.8 | -13.7 | .204 | .105e 18 |
| 11 | 7 | .257 | 42.8 | 27.7 | 67.6 | -13.1 | .219 | .205e 15 |
| 12 | 6 | .230 | 39.1 | 24.3 | 61.9 | -12.5 | .235 | .909e 12 |
| 13 | 5 | .206 | 35.8 | 21.2 | 56.7 | -11.9 | .253 | .808e 10 |
| 14 | 4 | .184 | 32.7 | 18.6 | 52.1 | -11.3 | .272 | .131e 09 |
| 15 | 3 | .165 | 30.0 | 16.3 | 47.9 | -10.6 | .292 | .361e 07 |
| 16 | 2 | .147 | 27.5 | 14.4 | 44.1 | -10.0 | .315 | 157597.39 |
| 17 | 1 | .131 | 25.3 | 12.7 | 40.8 | -9.3 | .340 | 10267.71 |
| 18 | 0 | .117 | 23.3 | 11.3 | 37.7 | -8.7 | .367 | 953.26 |
| 19 | -1 | .104 | 21.5 | 10.1 | 35.0 | -8.0 | .397 | 120.91 |
| 20 | -2 | .093 | 19.8 | 9.1 | 32.6 | -7.3 | .429 | 20.19 |
| 21 | -3 | .083 | 18.3 | 8.2 | 30.4 | -6.6 | .465 | 4.29 |
| 22 | -4 | .074 | 16.9 | 7.5 | 28.5 | -5.9 | .505 | 1.13 |
| 23 | -5 | .066 | 15.7 | 6.8 | 26.8 | -5.1 | .550 | .36 |
| 24 | -6 | .059 | 14.6 | 6.3 | 25.2 | -4.4 | .599 | .13 |
| 25 | -7 | .052 | 13.6 | 5.8 | 23.8 | -3.6 | .653 | .05 |
| 26 | -8 | .047 | 12.6 | 5.3 | 22.6 | -2.9 | .714 | .02 |
| 27 | -9 | .041 | 11.8 | 5.0 | 21.5 | -2.1 | .782 | .01 |
| 28 | -10 | .037 | 11.0 | 4.6 | 20.6 | -1.3 | .857 | .00 |
| 29 | -11 | .033 | 10.2 | 4.3 | 19.7 | -.5 | .941 | .00 |
| 30 | -12 | .029 | 9.6 | 4.0 | 18.9 | .3 | 1.035 | .00 |

Table A.2 - 49.8 Mc Calculated Phase Lock Loop Performance

phase lock loop performance vs n/a (total noise to total signal power in if)

limit n/a design level = 21 db
design n/a level = 21 db
limit sigma (loop n/a) level = -8.7 db
b (loop parameter) = 35.6 rad/sec
if noise bandwidth = 45000. cps
maximum amplitude phase detector output = 1.500
fraction of total power in carrier = .50

| n/a db | margin db | amplitude v | out f3db cps | err f3db cps | nbw cps | sigma db | sigma rad | time min |
|---|---|---|---|---|---|---|---|---|
| strong carrier | | 1.500 | 148.3 | 140.3 | 233.0 | | | |
| strong signal | | 1.060 | 106.0 | 98.0 | 166.6 | | | |
| 0 | 21 | .703 | 71.6 | 63.6 | 112.6 | -21.9 | .079 | |
| 1 | 20 | .657 | 67.2 | 59.2 | 105.6 | -21.2 | .086 | |
| 2 | 19 | .610 | 62.7 | 54.7 | 98.5 | -20.5 | .094 | |
| 3 | 18 | .563 | 58.2 | 50.2 | 91.5 | -19.8 | .101 | |
| 4 | 17 | .517 | 53.8 | 45.8 | 84.5 | -19.2 | .109 | |
| 5 | 16 | .473 | 49.5 | 41.5 | 77.8 | -18.5 | .118 | |
| 6 | 15 | .430 | 45.4 | 37.4 | 71.3 | -17.9 | .126 | |
| 7 | 14 | .390 | 41.5 | 33.6 | 65.3 | -17.3 | .136 | |
| 8 | 13 | .352 | 37.9 | 30.0 | 59.6 | -16.7 | .145 | |
| 9 | 12 | .318 | 34.5 | 26.6 | 54.3 | -16.1 | .156 | |
| 10 | 11 | .286 | 31.4 | 23.6 | 49.5 | -15.5 | .167 | |
| 11 | 10 | .257 | 28.6 | 20.8 | 45.1 | -14.9 | .179 | .289e 24 |
| 12 | 9 | .230 | 26.1 | 18.3 | 41.1 | -14.3 | .192 | .109e 21 |
| 13 | 8 | .206 | 23.7 | 16.1 | 37.5 | -13.7 | .205 | .112e 18 |
| 14 | 7 | .184 | 21.6 | 14.0 | 34.2 | -13.1 | .220 | .273e 15 |
| 15 | 6 | .165 | 19.7 | 12.3 | 31.2 | -12.5 | .236 | .139e 13 |
| 16 | 5 | .147 | 18.0 | 10.7 | 28.6 | -11.9 | .253 | .137e 11 |
| 17 | 4 | .131 | 16.4 | 9.3 | 26.2 | -11.2 | .272 | .238e 09 |
| 18 | 3 | .117 | 15.1 | 8.2 | 24.0 | -10.6 | .293 | .684e 07 |
| 19 | 2 | .104 | 13.8 | 7.2 | 22.1 | -10.0 | .315 | 306156.21 |
| 20 | 1 | .093 | 12.7 | 6.3 | 20.4 | -9.3 | .340 | 20283.98 |
| 21 | 0 | .083 | 11.6 | 5.6 | 18.9 | -8.7 | .367 | 1902.01 |
| 22 | -1 | .074 | 10.7 | 5.0 | 17.5 | -8.0 | .396 | 242.58 |
| 23 | -2 | .066 | 9.9 | 4.5 | 16.3 | -7.3 | .429 | 40.62 |
| 24 | -3 | .059 | 9.1 | 4.1 | 15.2 | -6.6 | .465 | 8.65 |
| 25 | -4 | .052 | 8.5 | 3.7 | 14.2 | -5.9 | .505 | 2.28 |
| 26 | -5 | .047 | 7.8 | 3.4 | 13.4 | -5.1 | .549 | .72 |
| 27 | -6 | .041 | 7.3 | 3.1 | 12.6 | -4.4 | .599 | .27 |
| 28 | -7 | .037 | 6.8 | 2.9 | 11.9 | -3.6 | .653 | .11 |
| 29 | -8 | .033 | 6.3 | 2.7 | 11.3 | -2.9 | .714 | .05 |
| 30 | -9 | .029 | 5.9 | 2.5 | 10.8 | -2.1 | .781 | .03 |

$f_{R\ 3\ db}$ , $f_{E\ 3\ db}$ are solutions to the equations $\left|\theta_R/\theta_C\right|^2 = 0.5$ and $\left|\theta_E/\theta_C\right|^2 = 0.5$ respectively, which are quadratic in $\omega^2$.

## A.5 - Loop Difference Amplifier Parameters

A difference amplifier with appropriate elements in its feedback loop is used for the phase lock loop control network, F(s). The amplifier is in Figure A.4, which identifies the feedback elements.

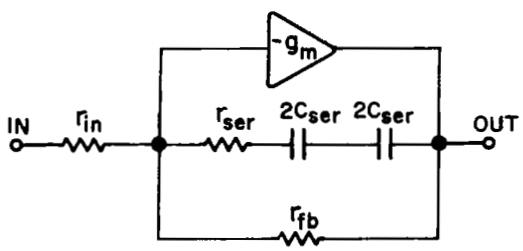



Figure A.4 - Loop Difference Amplifier used for Control Network F(s)

The equations for the feedback elements are:

$r_{in}$ = input resistor, value chosen.

$$r_{ser} = \frac{\sqrt{2}\ B_o}{A_1 K}\ r_{in} + \frac{1}{g_m} \quad \text{(ohms)}$$

$$r_{fb} = K_{dc}\ r_{in} \quad \text{(ohms)}$$

$$(2)(C_{ser}) = 2\left(\frac{A_1\ K}{B_o^{\,2}\ r_{in}}\right) \quad \text{(farad)}$$

$$\text{hold in} = \frac{K_{mul}\ K_{vco}}{A_1\ K_{dc}} \quad \text{(cps)}$$

$$K = K_{vco}\ K_{mul} \quad \left(\frac{\text{rad/sec}}{\text{volt}}\right)$$

$K_{vco}$ = gain of the VCO $\left(\frac{\text{rad/sec}}{\text{volt}}\right)$

$K_{mul}$ = the frequency multiplication following the VCO

$K_{dc}$ = closed loop dc gain of difference amplifier

$g_m$ = open loop transconductance of difference amplifier

Selection of the loop difference amplifier parameters

$B_o$ and $A_1$ are determined from Section A.4. $K_{vco}$, $K_{mul}$, and $g_m$ are determined by the receiver configuration and the design of the loop difference amplifier.

The impedance level should be as small as possible with the following constraints:

1. It should not load the 1 k output impedance of the loop phase detector,
2. It should not require too much signal power from the difference amplifier, and
3. The capacitors in the feedback loop must be an available size.

The impedance level was established somewhat arbitrarily by setting $r_{in} = 25$ k.

$K_{dc}$ should be as large as possible to minimize the dc phase error. Yet, it must be small enough that the loop amplifier will not saturate due to dc offset in the first stage of the loop amplifier and dc offset from the loop phase detector. $K_{dc}$ is chosen to be 20, which gives a 0.5 v loop amplifier output (relative to the 5 v supply), or 25 percent of its 2 v maximum output, for an input dc offset of 25 mv (the maximum expected).

Table A.3 shows the 423.3 Mc channel loop difference amplifier parameters. Values are shown for design levels of $N_1/A_1$ from 3 to 30 db. Table A.4 shows the 49.8 Mc loop difference amplifier parameters.

Derivation of the loop difference amplifier parameters

The node equations were written for the feedback amplifier. Negligible quantities were determined by inserting actual values for the amplifier and typical values for the feedback elements. After simplification, the elements of the amplifier transfer function were identified with the control network, F(s). The zero, the high frequency gain, and the dc gain of the amplifier transfer function and F(s) were made equal.

# Table A.3

423.30 mc channel loop amplifier parameters vs design level n/a (total noise to total signal power in if)

limit sigma level = -8.7 db
time to loss of 1 cycle approx = 10 hrs
if noise bandwidth = 45000. cps
maximum amplitude phase detector output = 1.500 v
fraction of total power in carrier = .50
loop gain without amplifier = 96132. rad/sec-volt
amplifier dc gain = 20.0
vco gain = 900.0 cps/v
vco x multiplier gain = 15300. cps/v

| n/a db | amplitude v | hold in cps | b rad/sec | nbw cps | out f3db cps | err f3db cps | rin kohm | rser kohm | rfb kohm | 2(cser) microf |
|---|---|---|---|---|---|---|---|---|---|---|
| 3 | .563 | 30600. | 2252.4 | 1194.6 | 737.8 | 358.4 | 21.361 | 1.268 | 427.225 | 1.000 |
| 4 | .517 | 30600. | 1789.2 | 948.9 | 586.0 | 284.7 | 31.090 | 1.593 | 621.802 | 1.000 |
| 5 | .473 | 30600. | 1421.2 | 753.7 | 465.5 | 226.1 | 20.469 | .917 | 409.389 | 2.200 |
| 6 | .430 | 30600. | 1128.9 | 598.7 | 369.8 | 179.6 | 29.524 | 1.151 | 590.485 | 2.200 |
| 7 | .390 | 30600. | 896.7 | 475.5 | 293.7 | 142.7 | 19.860 | .684 | 397.210 | 4.700 |
| 8 | .352 | 30600. | 712.2 | 377.7 | 233.3 | 113.3 | 28.452 | .858 | 569.059 | 4.700 |
| 9 | .318 | 30600. | 565.7 | 300.0 | 185.3 | 90.0 | 40.656 | 1.076 | 813.127 | 4.700 |
| 10 | .286 | 30600. | 449.4 | 238.3 | 147.2 | 71.5 | 18.163 | .432 | 363.263 | 15.000 |
| 11 | .257 | 30600. | 356.9 | 189.3 | 116.9 | 56.8 | 25.850 | .541 | 517.009 | 15.000 |
| 12 | .230 | 30600. | 283.5 | 150.3 | 92.8 | 45.1 | 25.048 | .466 | 500.962 | 22.000 |
| 13 | .206 | 30600. | 225.2 | 119.4 | 73.7 | 35.8 | 35.554 | .584 | 711.089 | 22.000 |
| 14 | .184 | 30600. | 178.9 | 94.8 | 58.6 | 28.4 | 19.807 | .295 | 396.147 | 56.000 |
| 15 | .165 | 30600. | 142.1 | 75.3 | 46.5 | 22.6 | 28.056 | .368 | 561.326 | 55.000 |
| 16 | .147 | 30600. | 112.8 | 59.8 | 36.9 | 17.9 | 39.743 | .460 | 794.877 | 56.000 |
| 17 | .131 | 30600. | 89.6 | 47.5 | 29.3 | 14.2 | 26.250 | .276 | 525.016 | 120.000 |
| 18 | .117 | 30600. | 71.2 | 37.7 | 23.3 | 11.3 | 24.759 | .233 | 495.190 | 180.000 |
| 19 | .104 | 30600. | 56.5 | 30.0 | 18.5 | 9.0 | 35.018 | .291 | 700.360 | 180.000 |
| 20 | .093 | 28551. | 44.9 | 23.8 | 14.7 | 7.1 | 27.007 | .204 | 540.154 | 330.000 |
| 21 | .083 | 25555. | 35.6 | 18.9 | 11.6 | 5.6 | 38.180 | .253 | 763.600 | 330.000 |
| 22 | .074 | 22791. | 28.3 | 15.0 | 9.2 | 4.5 | 53.965 | .315 | 1079.303 | 330.000 |
| 23 | .066 | 20323. | 22.5 | 11.9 | 7.3 | 3.5 | 76.266 | .393 | 1525.329 | 330.000 |
| 24 | .059 | 18120. | 17.8 | 9.4 | 5.8 | 2.8 | 107.772 | .492 | 2155.454 | 330.000 |
| 25 | .052 | 16154. | 14.2 | 7.5 | 4.6 | 2.2 | 152.281 | .616 | 3045.636 | 330.000 |
| 26 | .047 | 14401. | 11.2 | 5.9 | 3.6 | 1.7 | 215.158 | .772 | 4303.171 | 330.000 |
| 27 | .041 | 12838. | 8.9 | 4.7 | 2.9 | 1.4 | 303.981 | .968 | 6079.623 | 330.000 |
| 28 | .037 | 11443. | 7.1 | 3.7 | 2.3 | 1.1 | 429.453 | 1.216 | 8589.078 | 330.000 |
| 29 | .033 | 10200. | 5.6 | 3.0 | 1.8 | .9 | 606.697 | 1.527 | 12133.947 | 330.000 |
| 30 | .029 | 9092. | 4.4 | 2.3 | 1.4 | .7 | 857.069 | 1.920 | 17141.395 | 330.000 |

# Table A.4

49.80 mc channel loop amplifier parameters vs design level n/a (total noise to total signal power in if)

limit sigma level = -8.7 db
time to loss of 1 cycle approx = 10 hrs
if noise bandwidth = 45000. cps
maximum amplitude phase detector output = 1.500 v
fraction of total power in carrier = .50
loop gain without amplifier = 5654. rad/sec-volt
amplifier dc gain = 20.0
vco gain = 900.0 cps/v
vco x multiplier gain = 900. cps/v

| n/a db | amplitude v | hold in cps | b rad/sec | nbw cps | out f3db cps | err f3db cps | rin kohm | rser kohm | rfb kohm | 2(cser) microf |
|---|---|---|---|---|---|---|---|---|---|---|
| 3 | .563 | 1800. | 2252.4 | 1194.6 | 737.8 | 358.4 | 2.673 | 2.684 | 53.469 | .470 |
| 4 | .517 | 1800. | 1789.2 | 948.9 | 586.0 | 284.7 | 3.891 | 3.376 | 77.822 | .470 |
| 5 | .473 | 1800. | 1421.2 | 753.7 | 465.5 | 226.1 | 5.636 | 4.247 | 112.723 | .470 |
| 6 | .430 | 1800. | 1128.9 | 598.7 | 369.8 | 179.6 | 8.129 | 5.343 | 162.586 | .470 |
| 7 | .390 | 1800. | 896.7 | 475.5 | 293.7 | 142.7 | 11.682 | 6.723 | 233.653 | .470 |
| 8 | .352 | 1800. | 712.2 | 377.7 | 233.3 | 113.3 | 16.737 | 8.460 | 334.740 | .470 |
| 9 | .318 | 1800. | 565.7 | 300.0 | 185.3 | 90.0 | 23.915 | 10.647 | 478.310 | .470 |
| 10 | .286 | 1800. | 449.4 | 238.3 | 147.2 | 71.5 | 34.098 | 13.401 | 681.970 | .470 |
| 11 | .257 | 1800. | 356.9 | 189.3 | 116.9 | 56.8 | 22.809 | 7.935 | 456.184 | 1.000 |
| 12 | .230 | 1800. | 283.5 | 150.3 | 92.8 | 45.1 | 32.415 | 9.986 | 648.304 | 1.000 |
| 13 | .206 | 1800. | 225.2 | 119.4 | 73.7 | 35.8 | 20.914 | 5.720 | 418.288 | 2.200 |
| 14 | .184 | 1800. | 178.9 | 94.8 | 58.6 | 28.4 | 29.658 | 7.197 | 593.162 | 2.200 |
| 15 | .165 | 1800. | 142.1 | 75.3 | 46.5 | 22.6 | 19.671 | 4.247 | 393.420 | 4.700 |
| 16 | .147 | 1800. | 112.8 | 59.8 | 36.9 | 17.9 | 27.855 | 5.343 | 557.110 | 4.700 |
| 17 | .131 | 1800. | 89.6 | 47.5 | 29.3 | 14.2 | 39.425 | 6.723 | 788.510 | 4.700 |
| 18 | .117 | 1800. | 71.2 | 37.7 | 23.3 | 11.3 | 17.477 | 2.660 | 349.545 | 15.000 |
| 19 | .104 | 1800. | 56.5 | 30.0 | 18.5 | 9.0 | 24.718 | 3.345 | 494.372 | 15.000 |
| 20 | .093 | 1685. | 44.9 | 23.8 | 14.7 | 7.1 | 23.830 | 2.873 | 476.606 | 22.000 |
| 21 | .083 | 1503. | 35.6 | 18.9 | 11.6 | 5.6 | 33.688 | 3.614 | 673.765 | 22.000 |
| 22 | .074 | 1340. | 28.3 | 15.0 | 9.2 | 4.5 | 18.706 | 1.794 | 374.128 | 56.000 |
| 23 | .066 | 1195. | 22.5 | 11.9 | 7.3 | 3.5 | 26.436 | 2.255 | 528.738 | 56.000 |
| 24 | .059 | 1065. | 17.8 | 9.4 | 5.8 | 2.8 | 37.358 | 2.835 | 747.163 | 56.000 |
| 25 | .052 | 950. | 14.2 | 7.5 | 4.6 | 2.2 | 24.633 | 1.671 | 492.676 | 120.000 |
| 26 | .047 | 847. | 11.2 | 5.9 | 3.6 | 1.7 | 23.203 | 1.405 | 464.067 | 180.000 |
| 27 | .041 | 755. | 8.9 | 4.7 | 2.9 | 1.4 | 32.782 | 1.765 | 655.645 | 180.000 |
| 28 | .037 | 673. | 7.1 | 3.7 | 2.3 | 1.1 | 25.261 | 1.216 | 505.239 | 330.000 |
| 29 | .033 | 600. | 5.6 | 3.0 | 1.8 | .9 | 35.688 | 1.527 | 713.761 | 330.000 |
| 30 | .029 | 534. | 4.4 | 2.3 | 1.4 | .7 | 50.415 | 1.920 | 1008.317 | 330.000 |

## A.6 - Comparison of Measured and Calculated Phase Lock Loop Performance

Figure A.5 shows the carrier amplitude vs. RF carrier input. The most important feature of this Figure is the level of the carrier amplitude (vertical scale) at which 1 cycle per minute is skipped in the phase lock loop. For zero (or 0.1 v) loop stress, the measured level is 3 db higher than the calculated level for the 423.3 Mc channel. The measured level is 4.5 db higher than calculated for the 49.8 Mc channel. As expected, an even higher carrier amplitude is required if there is loop stress. It is reasonable to expect the loop stress to be as large as 0.5 v.

The horizontal displacement between measured and calculated curves is probably due to error in the input amplitude, or error in the measurement of noise figure.

The RF carrier input is the carrier level alone. If the carrier is being modulated with 50 percent of the total power in the sidebands, the total power would have to be 3 db larger than that indicated for carrier alone. Also, the carrier amplitude would be asymptotic to 1.06 v instead of 1.5 v.

Figure A.6 allows comparison of the measured and calculated phase error 3 db bandwidth. The most significant feature is that the measured phase error bandwidth for the 49.8 Mc channel is 30 percent narrower than calculated, yet it performs worse than calculated for the 423.3 Mc channel in terms of the level at which it loses 1 cycle per minute.

The loop error 3 db bandwidth was measured because it only required measurement of the output of the loop phase detector. Measurement of the phase lock loop output would be the next step in the investigation of the discrepancies, but it requires development of additional circuitry. The loop error 3 db bandwidth is a function of the carrier amplitude only, so its performance is the same whether or not the approximately 8 kc modulation is present. Modulation was not present for these measurements.

## A.7 - Selection of Transmitter Frequencies

The frequencies of the two transmitted signals should be separated

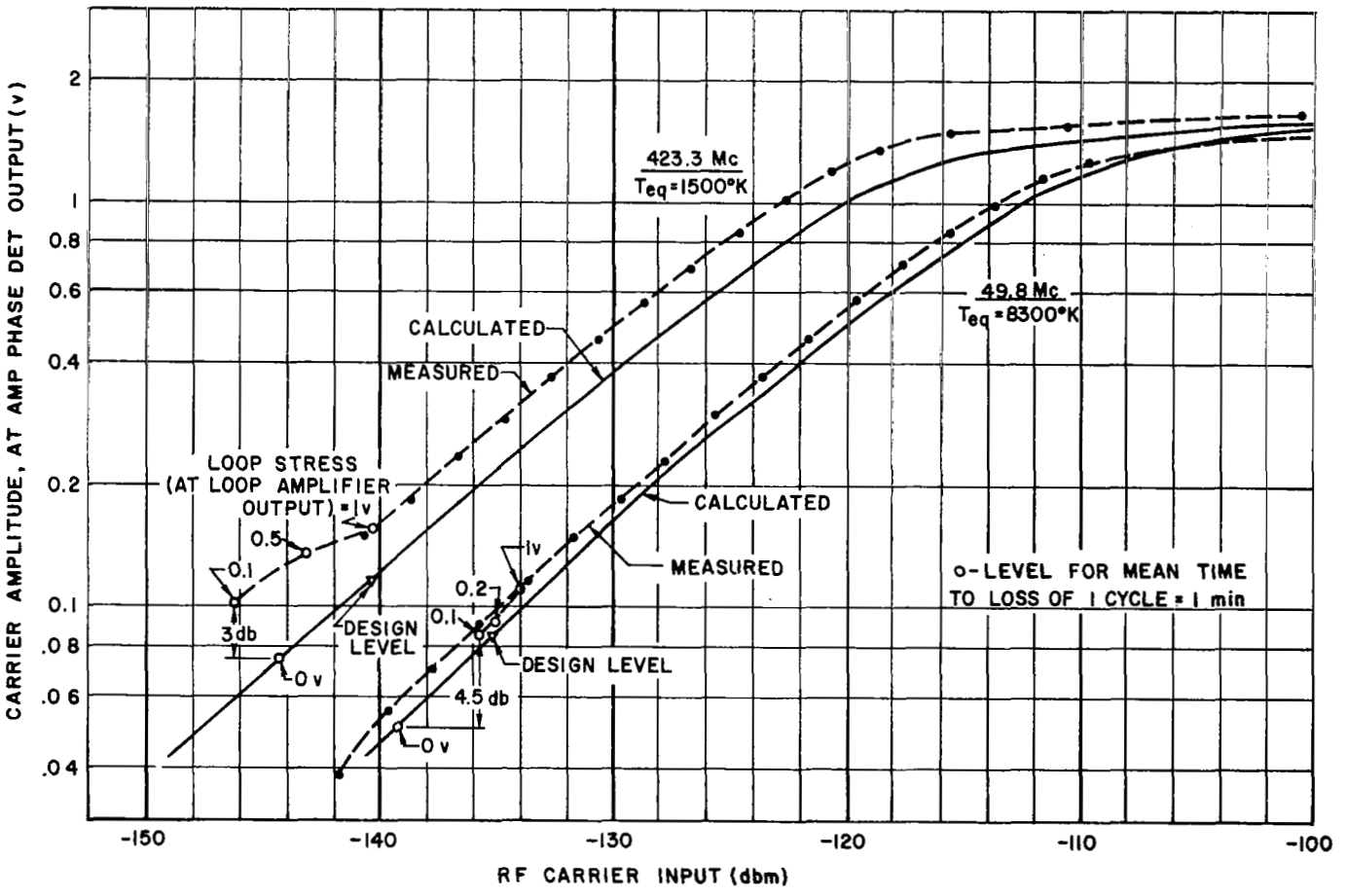



Figure A.5 - Carrier Amplitude vs. RF Carrier Input
The level at which loss of lock occurs is shown as a function of loop stress.

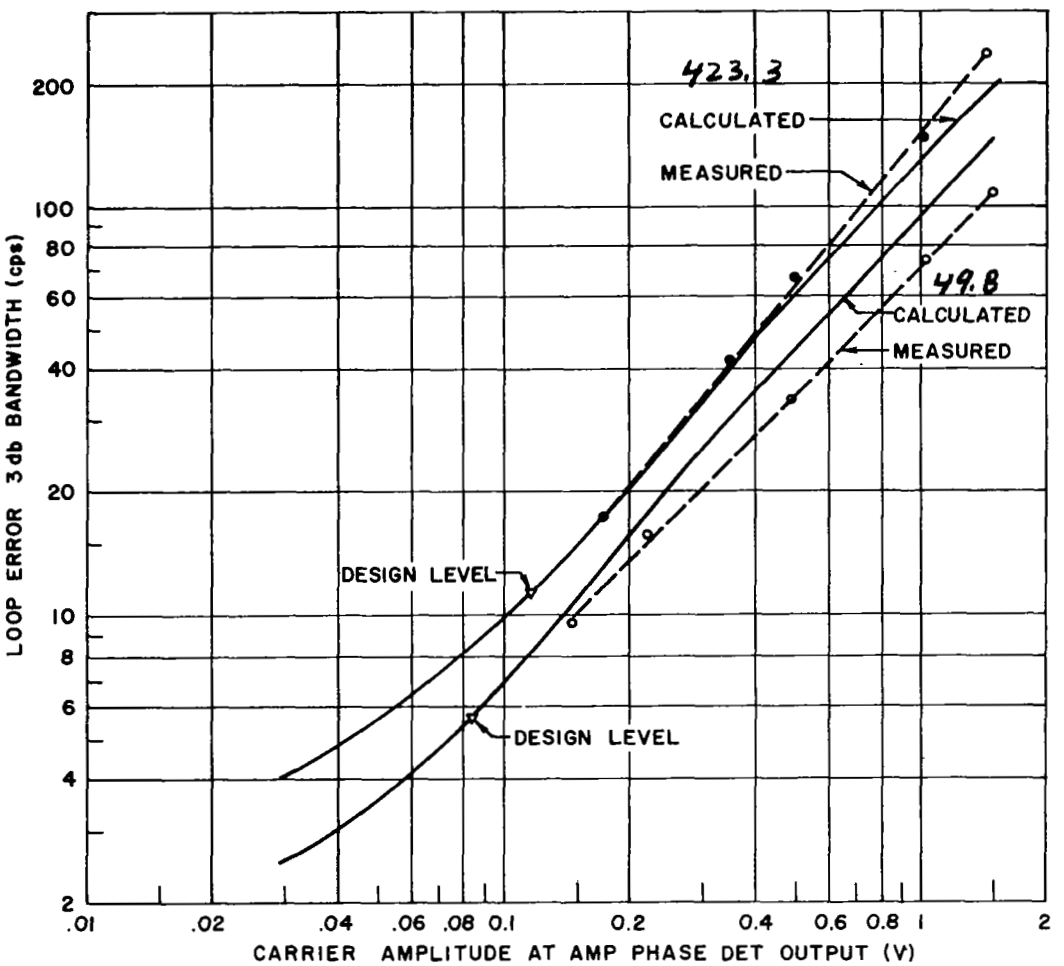



Figure A.6 - Phase Error 3 db Bandwidth vs. Carrier Amplitude

by at least a factor of 2 and related by some rational number. The lower frequency should be low enough to be affected by the interplanetary electrons, but not so low that the approximation to the refractive index of the earth's ionosphere is not valid. Other considerations were that the lower frequency antenna on the spacecraft should be as small as possible; and that certain high power transmitters were available.

The lower frequency was chosen to be 49.8 Mc because it was in the center of an authorized government band, 49.6 to 50.0 Mc, in which the 400 kw transmitter is licensed by ARDC as a space radar. The higher frequency was chosen to be 17/2 times the lower, or 423.3 Mc, because it allows easy multiplication (by 2's and 3's) to obtain the local oscillator frequency in the receiver, and was the first of several possible frequencies to be authorized.

A.8 - Selection of the Modulation Frequencies

For adequate resolution of group path, a high modulation frequency should be used. The signal to noise ratio at the loop phase detector should not be lower than -20 to -30 db for satisfactory phase detector and phase lock loop operation. This requirement is satisfied at the maximum range by limiting the IF bandwidth, which in turn limits the modulation frequency. The phase can be controlled only over the center two thirds of a crystal filter's 3 db bandwidth. A 40 kc 3 db bandwidth filter just about gives -20 db signal to noise ratio at the phase detector. The maximum modulation frequency with this filter is about 12 kc.

Two modulation frequencies are used to resolve multiple cycle ambiguities up to about 8 cycles of 8.692 kc. The two modulation frequencies, 7.692 and 8.692 kc, are located symmetrically about 8.192 kc, a clock frequency available from the spacecraft. This symmetrical location about the clock frequency allows the phase of either modulation frequency to be measured without switching in the receiver.

At the 0.5 AU range, an error of 2 percent of one cycle corresponds to an electron density of $0.6 \times 10^6$ electrons/$m^3$; and 8 cycles of

8.692 kc corresponds to an electron density of $230 \times 10^6$ electrons/$m^3$. A density of $10 \times 10^6$ electrons/$m^3$ is anticipated.

APPENDIX B

DATA SYSTEM

## B.1 - Spacecraft Data Handling and Signals

### Telemetry Word

A telemetry word in the data handling sub-system consists of 6 binary bits and one odd parity bit for error detection except for a limited number of words in which the parity bit has been omitted. Spacecraft generated words will be transmitted with the most significant bit first.

### Bit Rates

The data handling sub-system will be capable of processing scientific and engineering data (including the parity bit) at the following rates:

512 bits per second
256 bits per second
64 bits per second
16 bits per second
8 bits per second

### Frame

The data handling sub-system will assemble information from the instruments into frames composed of a series of 32 digital words.

### Format and Word Assignments

The words in a frame are assigned in several formats. The first word in a frame is numbered 1. The formats were organized for specific purposes and are selected by ground command for particular spacecraft operational modes.

### Format A, Format B

These are the two main formats for scientific information. Scientific information is in digital form. See Figure B.1 for the layout of the format.

### Format C

Primarily for spacecraft analog or digital engineering information,

| | | | |
|---|---|---|---|
| 1<br>FRAME SYNC. | 2<br>MODE IDENT. | 3<br>SCIENTIFIC SUBCOMM. | 4 |
| 5 | 6 | 7 | 8 |
| 9 | 10 | 11 | 12 |
| 13 | 14 | 15 | 16 |
| 17<br>FRAME SYNC. COMPLIMENT | 18<br>SUBCOMM. IDENT. | 19<br>ENGINEERING SUBCOMM. | 20 |
| 21 | 22 | 23 | 24 |
| 25 | 26 | 27 | 28 |
| 29 | 30 | 31 | 32 |

Figure B.1 - Form of the Main Frame Format for Formats A, B, and D The words which are the same in these three formats are specified, and the words which are different are only numbered.

and usually subcommutated into word No. 19 of Format A, B or D; this format is 64 words long.

Format D

This format is used infrequently and when used, then only for a short time. All the blank words in Figure B.1 are analog words connected to one line, called Format D, provided to the Stanford experiment. When this format is used, the information is simultaneously transmitted, and stored in a 68 frame memory. Storage stops when the memory is filled, and the data system then reverts to transmitting at 16 bps in Format B.

Format E

This format is 16 words long and is used for analog and digital scientific information and is subcommutated into word No. 3 of formats A, B, and D.

The various signals are described in Table 2.1. The relative timing of some of the signals is shown in Figure B.2.

B.2 - Division of Subcommutation

The Stanford experiment is assigned 4 analog words in the 16 word scientific subcom, nearly evenly spaced in time. There are 5 analog quantities to put on these 4 analog words. One is data: the modulation phase. The other 4 are operational information: carrier amplitude and loop stress for both channels. The subcommutator control is a simple one stage counter if the operational information is subcommutated onto just 2 scientific subcom words. The subcommutation is arranged to give information alternately about each channel, approximately evenly spaced in time, in this order: 49.8 Mc carrier amplitude (word No. 2), 423.3 Mc carrier amplitude (word No.11), 49.8 Mc loop stress (word No. 2), 423.3 Mc loop stress (word No. 11), repeat. Both carrier amplitude and loop stress can be used to indicate loss of lock.

Words No. 7 and 15 in the scientific subcom are left for the modulation phase, and are evenly spaced in time. The sampling rate is much higher than needed for the slowly varying modulation phase.

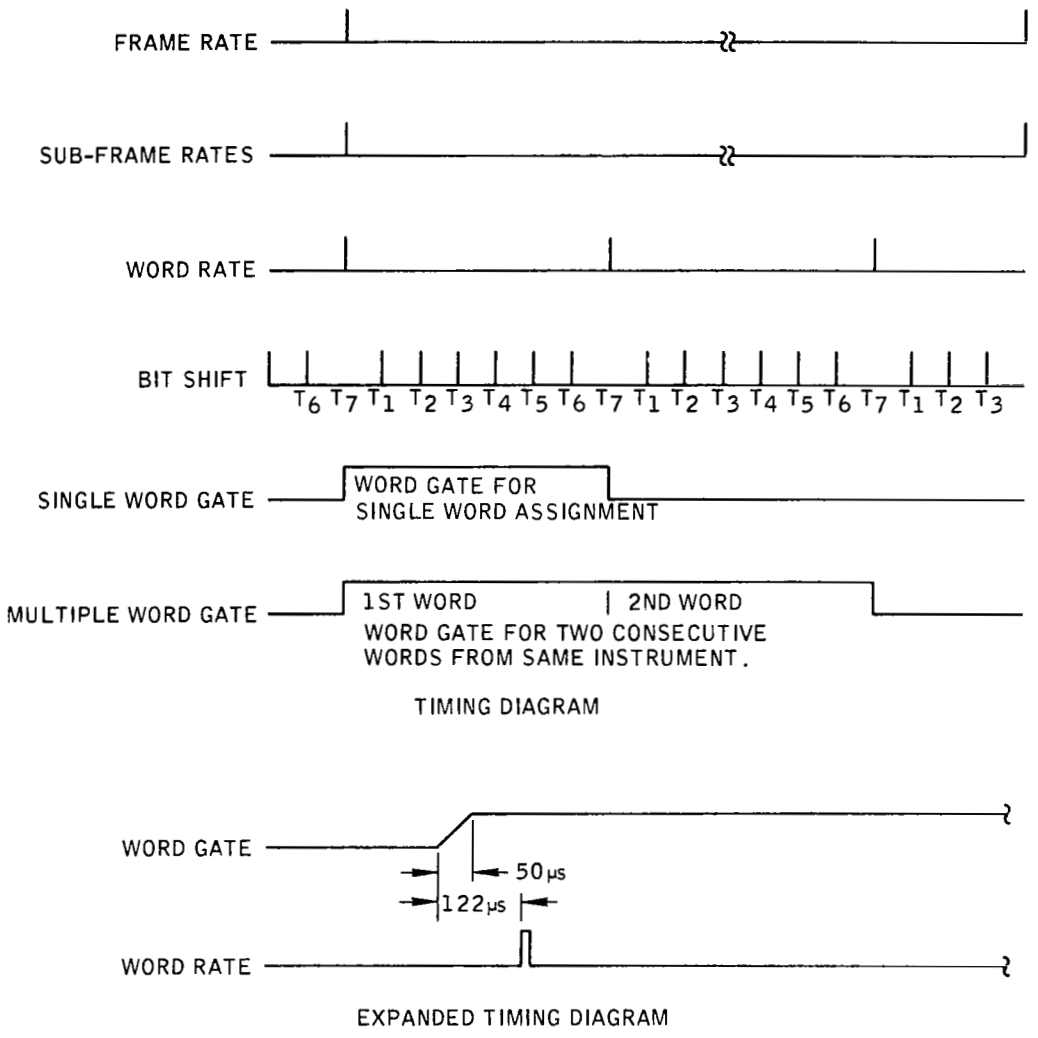



Figure B.2 - Timing Signal Relationships

# APPENDIX C

## NON-MAGNETIC COMPONENTS

The presence of a sensitive magnetometer aboard the spacecraft made it necessary to reduce the magnetic field of everything aboard the spacecraft. Individual experiments are required to have a magnetic field less than 2 gamma, 0 -pk, (1 gamma = $10^{-5}$ gauss or $10^{-9}$ webers per $m^2$) at a distance of 3 ft after exposure to a magnetizing field of 25 oersted ($2 \times 10^3$ amp-turn per m). The magnetic field of a magnetic dipole is proportional to $r^{-3}$.

The magnetic field of the completed Stanford receiver was 1 gamma measured under the above conditions.

A Hewlett Packard 428B clip-on dc ammeter with its 3529A magnetometer probe was used to measure the retentivity (retained B field) of all prospective components. All components used in production were also measured, because the manufacturer sometimes changes the materials without warning. They are also checked because special non-magnetic components look just like their magnetic counter parts, and the manufacturer sometimes accidentally substitutes the magnetic component.

The magnetometer is sensitive to changes of 1 gamma and indicates 100 gamma full scale on the most sensitive range. The probe is mounted in a horizontal plane, and rotated until its axis is normal to the local B field. Cars passing by, machines operating in the area, watches, and pockets full of keys cause the reading to fluctuate. Operation in a small cubicle made of transformer iron considerably reduced the fluctuations. Components were demagnetized first, to remove any previous strong magnetization, then tumbled in a magentizing field of 25 oersted. The peak to peak retentivity of the component was measured at a distance of 3 inches between the center of the component and the magnetometer probe. Standardization of the magnetizing field and measurement distance made comparison possible. An arbitrary limit of 12 - 14 gamma pp, below which components were acceptable was set. Above this limit, the non-availability of a substitute and the quantity used determined

acceptability.

Kovar (29 percent nickel, 54 percent iron), which is used in metal-to-glass seals for its equal thermal expansion, was the major offender. It is also used for the leads of many components because it can be both welded and soldered. Its shape dramatically affects its retentivity. Long thin needle shapes, like wire leads, are the most retentive shape as would be expected. Alloy 180 (nickel-copper) was substituted for the nickel-iron wire usually used in the welded modules.

Where possible, ferrite cores were used instead of the more magnetic powdered iron. These magnetic components were selected from a group for those with minimum magnetism. Ferrite, however, is more temperature sensitive than powdered iron.

TO-18 transistors were made with non-magnetic nickel-silver hats at the transistor factory on a special order (TI, Fairchild, and Motorola). However, the transistor leads are still kovar, and had to be clipped to their maximum usable length (0.12 in) before magnetic testing. Micro Semiconductor made diodes with special non-magnetic leads welded to the very short kovar ribbon which makes the hermetic seal to the glass. As a favor, and with the prospect of business with the other experimenters, Kemet made 200 of each size tantalum capacitor that was needed, substituting non-magnetic Alloy 180 for the normally used kovar leads. The 200 units were necessary to be able to statistically measure their reliability within a reasonable time.

Goodall specially manufactured hermetically sealed mylar capacitors which used copper cases and copper leads. Their standard hermetically sealed line is magnetic. Small mica capacitors, type MCM, which would fit into the space designed for the magnetic Corning glass capacitors, were made by General Instrument. JFD designed a special trimmer capacitor which is non-magnetic and has satisfactory temperature characteristics. Their standard model used invar (nickel and iron). Crystals from Hughes for frequency control and for filters were put in a hermetic aluminum can by Monitor.

Items which are non-magnetic without a special order are metal film resistors (Electra), carbon composition resistors (Allen-Bradley,

but with solder coated leads instead of tin dipped), high reliability ceramic capacitors (Aerovox), and feed-through capacitors (Erie: Filtercon).

Minimum magnetic construction practices

Transistor leads were trimmed to 0.10 in and mounted flat (with a little space) on the printed circuit board. The leads were not bent over thus minimizing the lead length. Where longer transistor leads were necessary, an Alloy 180 wire, flattened at the weld, was welded to the lead.

Components with magnetic parts were placed so the magnetic pieces were not lined up to give a long thin shape. The TI integrated circuits have kovar cases. Five TI circuits in a stack have about the same magnetic field as a single circuit, probably because the stack resembles a sphere.

APPENDIX D

PAINTS, ADHESIVES, AND FOAMS

Cat-a-lac top coat flat black 463-1-8 (2 parts), and Cat-a-lac reducer TL-26 (cleaner)(Finch Paint and Chemical Company)

This material is used on the outside of the receiver to obtain an emmisivity of greater than 0.72, so that all the packages in the spacecraft will be nearly the same temperature.

828 Epoxy (Shell) and Hardener EM308 (Thiokol), equal parts by weight

This is used to bond components to the chassis. This flexible bonding material allows flexure of the board (or chassis) without breaking the bond. Rigid adhesives shear from the board or from the component when the board is flexed. The flexibility of this material is a function of the amount of hardener added.

Polyurethane coat PTU (Emerson and Cuming)

The printed circuit boards are coated on both sides with this alcohol soluble polyurethane coating for protection from moisture, and from the catalyst (a secondary amine) used in the polyurethane foam. If the catalyst for the foam is not thoroughly mixed with the resin, it reacts with the copper of the printed circuits to form a highly conductive green substance.

Eccofoam FP and catalyst 12-2 rigid polyurethane foam (Emerson and Cuming)

The printed circuit boards are supported in this 2 pound/cu ft foam. The foam is formed over the components side of the printed circuit in a mold at room temperature. It is left undisturbed for at least 2 hours to keep it from collapsing. The next day, the foam is cut to size with a band saw. This foam will dissolve in acetone, or soften in ethyl alcohol.

Silastic RTV 891 adhesive (Dow Corning)

This material is squirted into the apertures of pot cores, but not filling the whole void inside, to secure the leads and the bobbin.

Q27A Max cement enamel (Communication Products Company)

Used by STL to hold the windings of the coils in place.

Eccobond 55 and catalyst no. 9 (Emerson and Cuming)

Used to secure stainless steel studs in the magnesium covers and frames.

## BIBLIOGRAPHY


1. Eshleman, V. R., P. B. Gallagher, and R. C. Barthle, "Radar Methods of Measuring the Cislunar Electron Density," J. Geophys. Res., 65, 1960, p. 3079-3086

2. Lawrence, R. S., C. G. Little, and J. J. A. Chivers, "A Survey of Ionospheric Effects upon Earth-Space Radio Propagation," Proc. IEEE, 52, no. 1, Jan. 1964, pp. 4-27

3. Bamberg, P., "Gleichspannungswandler mit Geregelter Ausgangsspanung" ("A Direct Voltage Converter with Adjustable Output Voltage"), Electronische Rundschau, no. 6, 1963, pp. 289-292[1]

4. Harris, P. E., and B. E. Simmons, "DC Accuracy in a Fast Boxcar Circuit via a Comparator," IEEE Transactions on Electronic Computers, EC-13, no. 3, June 1964, pp. 285-288

5. Develet, Jean A., Jr., The Influence of Time Delay on Second Order Phase Lock Loop Acquisition Range, Space Technology Laboratories Report, Sept. 1962

6. Baumert, L., M. Easterling, S. W. Golumb, and A. Viterbi, Coding Theory and Its Application to Communications Systems, Jet Propulsion Laboratory Technical Report, no. 32-67, March 1961

7. "Transponder Ranging System," JPL Space Programs Summary, no. 37-14, pp. 75-98

8. Ko, H. C., "The Distribution of Cosmic Radio Background Radiation," Proc. IRE, 46, no.1, Jan. 1958, pp. 208-215

9. Reference Data for Radio Engineers, 4th ed., ITT, p. 746

10. Jaffe, R., and E. Rechtin, "Design and Performance of Phase Lock Circuits Capable of Near Optimum Performance Over a Wide Range of Input Signal and Noise Levels," IRE Transactions-Information Theory, March 1955, pp. 66-76

11. Davenport, W. B., Jr., "Signal to Noise Ratios in Band-pass Limiters," Journal of Applied Physics, 24, no. 6, June 1953, pp. 720-727

12. Viterbi, A. J., "Phase Locked Loop Dynamics in the Presence of Noise by Fokker-Planck Techniques," Proc. IEEE, 51, no. 12, Dec. 1963, pp. 1737-1753


---

[1] R. Long at the Stanford Research Institute has an English translation.