TECHNICAL ADVISEMENT MEMORANDUM NO. 106-11

GEOS A TELEMETRY SUBSYSTEM RELIABILITY ASSESSMENT

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Prepared by

Winifred C. Graham
Charles E. Bloomquist

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TECHNICAL ADVISEMENT MEMORANDUM NO. 106-11

To: Program Manager, Geodetic Satellite Physics and Astronomy
           Programs, Office of Space Science and Applications,
           NASA Headquarters

From: PRC GEOS Reliability Assessment Team

Subject: GEOS A Telemetry Subsystem Reliability Assessment

1.   Introduction

        PRC has completed an analysis of the GEOS A telemetry
subsystem. Details of this analysis, as well as the results and con-
clusions, are discussed below. Briefly, two tasks were accomplished:
(1) an engineering analysis was performed, including a failure mode
and effect analysis, and (2) the subsystem was modeled, using infor-
mation generated in the first task, and effectiveness figure-of-merit
numerics were calculated.

2.   Functional Description

        Since the experiments do not use telemetry for transmitting
experiment results, the telemetry data are composed solely of opera-
tional information on the spacecraft equipment. These data consist of
commutated PAM data, memory readout, and the time marker. The
commutated data and related hardware will be discussed first.

        There are two commutators, but they are not redundant, since
they do not handle the same data. The commutation rate is 0.63 sec-
onds per channel, or approximately 24 seconds per frame. A common
group of circuits provides timing and control to both commutators (see
Exhibit 1). The timing and control signals are derived from a 1,628-cps
tuning fork oscillator.

        The commutator switches, as discussed below, are set up to pro-
vide 35 data channels, but 38 channels per commutator are actually
transmitted. This is accomplished by "holding" the channel following

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channel 35 for 4 channel times. These 4 channels are designated numbers 36, 37, 38, and 1, and their +0.25 volt input is read continuously during this period on both commutators.

Essentially, a two-level gating scheme is employed in each commutator (see Exhibit 2). The A1 through A7 terms commutate seven channels simultaneously in each of the five "switch boxes." The outputs of the switch boxes are further commutated by the B1 through B5 terms to provide the output.

Associated with the commutators are subcommutators and telltale (TT) registers. There are two subcommutators, each consisting of eight subcommutated channels transmitted as channel 18 of each of the main commutators. A common group of circuits provides timing and control to both subcommutators. Both of these subcommutators contain channels assigned to the optical beacon and its power supply. Channel 8 on each subcommutator (optical system current and optical battery voltage) is transmitted when a flash sequence is not occurring. When a sequence occurs, signals from memory activate the timing and control circuitry, causing the other optical system information assigned to the subcommutators to be telemetered.

The telltale registers are 15-bit words, with each bit representing the "off/on" status of a command or some other binary function. Commutator 1 has two telltale registers read in as channels 17 and 29. Commutator 2 has one telltale register read in as channel 17. A common group of circuits provides timing and control for all three telltale registers. These circuits are, in turn, under the control of other encoder timing and control circuits.

Either main commutator can be stopped by ground command so that any channel can be continuously read out. In addition, each of the commutators modulates a subcarrier oscillator (SCO), and each SCO phase modulates the transmitter.

The other two outputs of the telemetry system (memory readout and time marker) will now be discussed. A signal from memory transfers a relay which causes data from commutator 2 to be replaced by
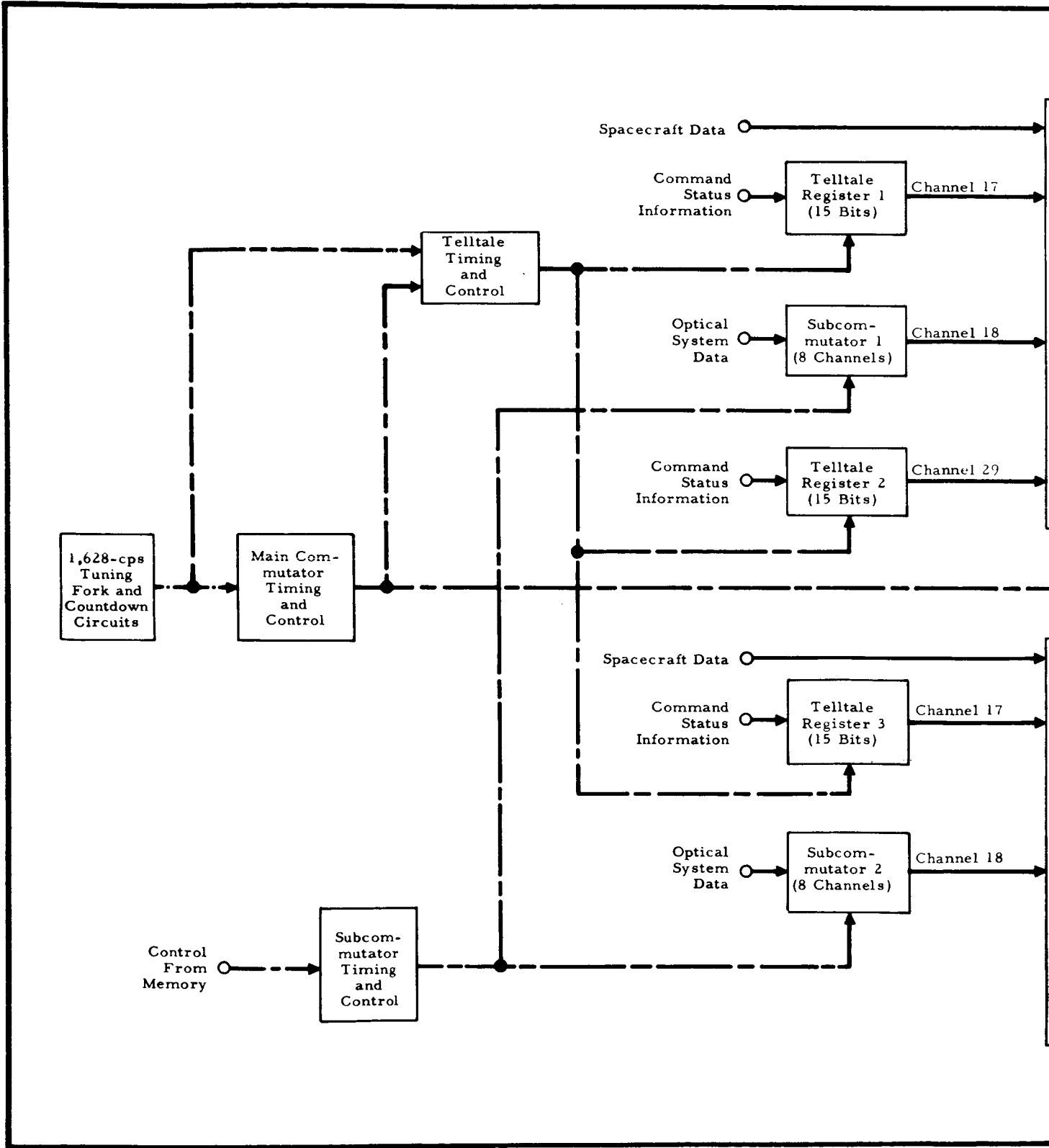
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Spacecraft Data

Command Status Information → Telltale Register 1 (15 Bits) → Channel 17

Telltale Timing and Control

Optical System Data → Subcommutator 1 (8 Channels) → Channel 18

Command Status Information → Telltale Register 2 (15 Bits) → Channel 29

1,628-cps Tuning Fork and Countdown Circuits

Main Commutator Timing and Control

Spacecraft Data

Command Status Information → Telltale Register 3 (15 Bits) → Channel 17

Optical System Data → Subcommutator 2 (8 Channels) → Channel 18

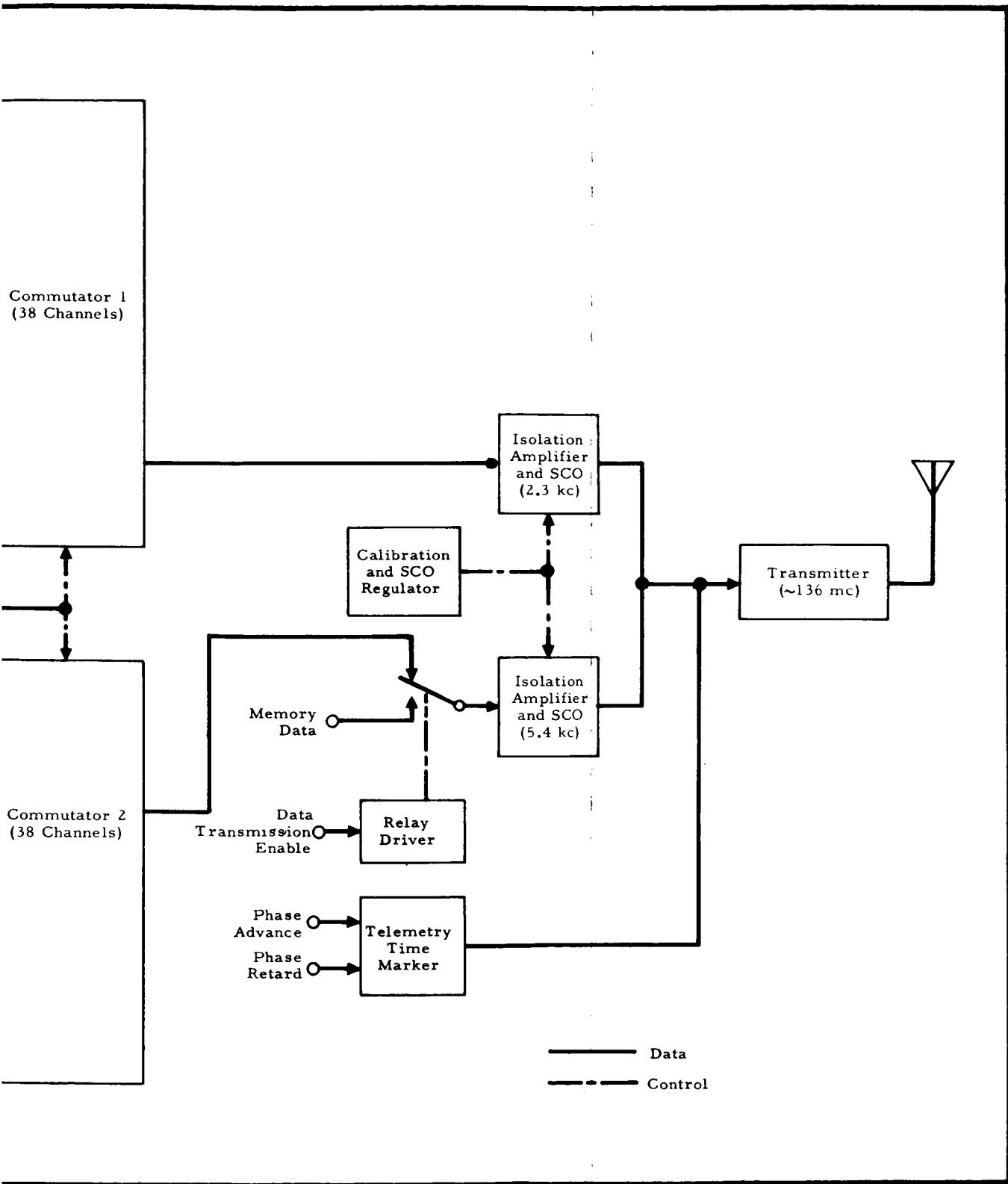Control From Memory → Subcommutator Timing and Control

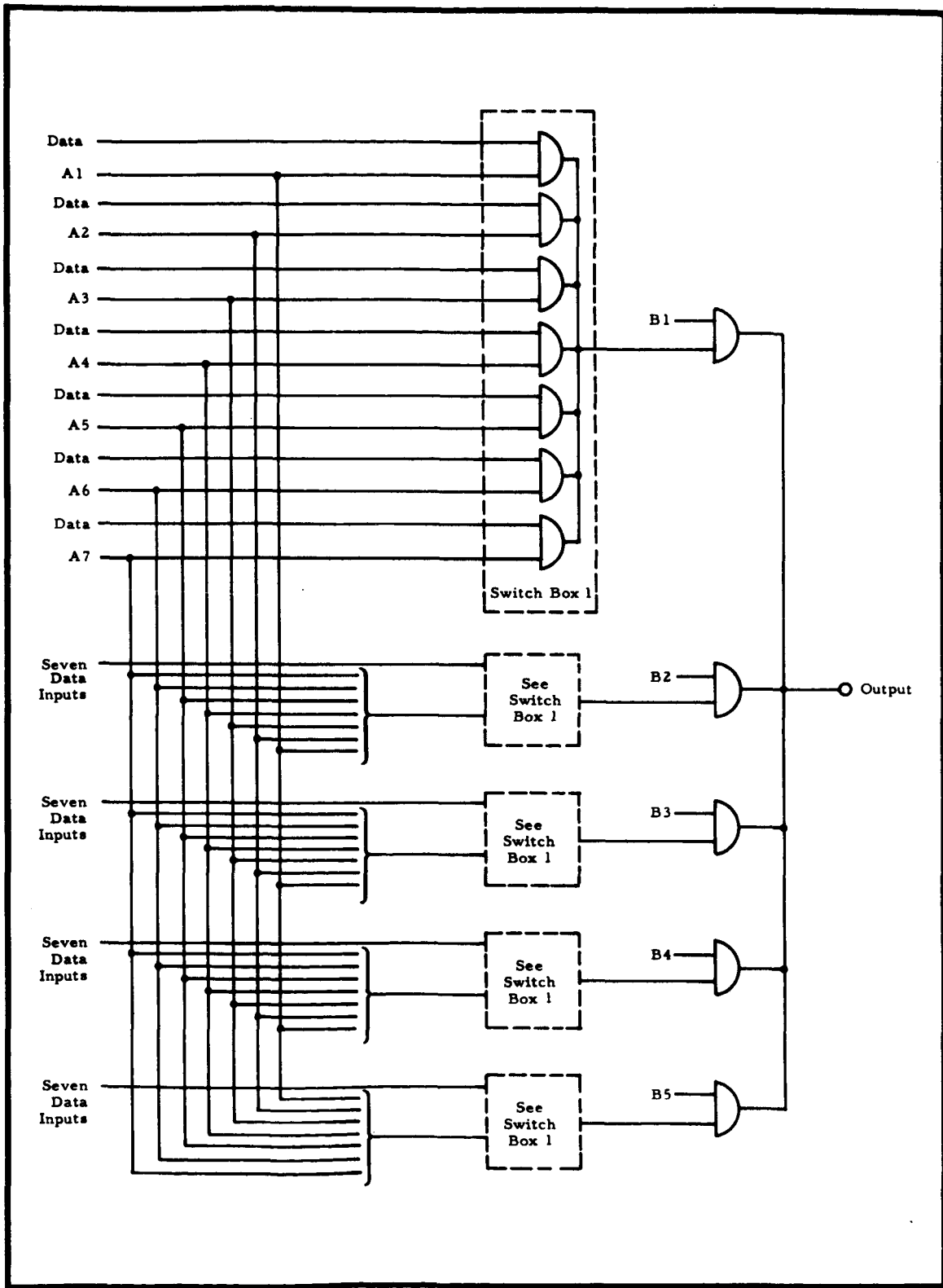EXHIBIT 1 - FUNCTIONA

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2

BLOCK DIAGRAM

EXHIBIT 2 - LOGICAL REPRESENTATION OF COMMUTATOR

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memory readout data at the input of the SCO. When readout is complete, the relay transfers back. The time marker circuits cause the phase advance and phase retard signals from the spacecraft clock to modulate the transmitter directly.

The normal operational plan for the telemetry subsystem calls for operation with only the transmitter and time marker on. The remainder of the unit (commutated data and memory readout) will be turned on only when the spacecraft is over a ground station assigned to receive these data.

3. Engineering Analysis

The appendix to this TAM contains the failure mode and effect analysis. The analysis revealed 20 failure states, ranging in severity from loss of the entire subsystem (due to loss of the transmitter) to loss of one TT bit. These failure states (none of which were unexpected in a subsystem of this type) are summarized in Exhibit 3.

An important aspect of failures in a telemetry system is that certain types of failure states may occur and not be recognized from the telemetry data. Attention was given to this potential problem, and a discussion of it appears in Reference 1. Of the 20 possible failure states in the GEOS telemetry subsystem, it was felt that very few were of this type. State 15 (the loss of one TT bit) would be the most difficult to identify via diagnosis of other spacecraft data and/or the response of the spacecraft to commands.

4. Telemetry Model

Making use of the preceding sections, the telemetry subsystem may be thought of as providing 128 discrete "outputs" which are either present or absent, depending on the state of the subsystem. The 128 outputs consist of the memory readout, the time marker, 45 telltale bits (utilizing 3 main commutated channels), 16 subcommutated channels (utilizing 2 main commutated channels), and, finally, 65 "other" main commutated channels. The state of the subsystem is a function of its failed and unfailed components.

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EXHIBIT 3 - FAILURE STATES

Failure State	Loss
1	All telemetry
2	Both commutators
3	60 channels (30 from each commutator)
4	56 channels (28 from each commutator)
5	Commutator 2 and memory readout
6	One commutator
7	Both subcommutators
8	One subcommutator
9	All telltale registers
10	One telltale register
11	Seven commutated channels
12	One commutated channel
13	One subcommutated channel
14	Five telltale bits
15	One telltale bit
16	Flash intensity information
17	Memory readout
18	Time marker
19	Sync
20	Temperature indications

Assume that the presence of all 128 outputs yields a value of unity for the subsystem. Further, assume that each output contributes a proportion, V_i, of this value independent of any other output and that the value of any particular subsystem state is the sum of the values associated with each output. Under these conditions, if P_i is the probability of output i being present, considered independently, it can be shown that the telemetry subsystem figure of merit is given by

$$\sum_{i=1}^{128} P_i V_i \,.\tag{1}$$

Exhibit 4 explicitly defines all 128 outputs, as well as tabulating the probability and relative value of each. Derivation of the probability and value terms of Exhibit 4 is undertaken in the following two subsections.

a. Derivation of Output Probabilities, P_i

The probability of any particular output being present, at time t, is assumed to be given by an expression of the form

$$P_i = \exp(-\lambda_i t)\tag{2}$$

where
i = particular output
λ_i = total failure rate of all parts required to achieve output i
t = operating time (uniformly assumed to be 8,760 hours)

The λ_i are derived by consulting Exhibit 5, which indicates generally the portions of the telemetry subsystem required for each output and which is cross-referenced to the appendix (via the item numbers). The appendix gives a comprehensive tabulation of the telemetry component

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EXHIBIT 4 - TELEMETRY MODEL TERMS

Output, i	Probability, P_i	Value, V_i	Output Definition
1	0.855	31	Memory readout
2	0.825	2	Time marker
3-32	0.246	1/9	Telltale bits from commutator 1 (30)
33-47	0.244	1/9	Telltale bits from commutator 2 (15)
48-52	0.323	1/4	Subcommutated channels from commutator 1 with flash intensity information (5)
53-55	0.340	1/4	Subcommutated channels from commutator 1 without flash intensity information (3)
56-63	0.336	1/4	Subcommutated channels from commutator 2 (8)
64-71	0.377	58/65	Commutated channels from commutator 1 with temperature information (8)
72-95	0.408	58/65	Other commutated channels from commutator 1 (24)
96-100	0.373	58/65	Commutated channels from commutator 2 with temperature information (5)
101-128	0.404	58/65	Other commutated channels from commutator 2 (28)

$$\sum_{i=1}^{128} P_i V_i = 0.54$$

EXHIBIT 5 - TELEMETRY EQUIPMENT REQUIRED FOR AVAILABILITY OF VARIOUS OUTPUTS

Output/Telemetry Equipment Required	Item Number[1]
A. Memory Readout (Output 1)	
1. Transmitter	60
2. Isolation amplifier	63
3. Subcarrier oscillator (SCO)	65
4. Calibration and SCO regulator	61
5. Relay module	66, 67
B. Time Marker (Output 2)	
1. Transmitter	60
2. Time marker generator	68
C. One Telltale Bit (Outputs 3-47)	
1. Timing and control	1-19
2. Commutator	1/35 of 20; 1/5 of 21 and 23; 22, 24
3. Telltale register	46, 47; 1/15 of 48, 1/3 of 49
4. Isolation amplifier	62
5. Subcarrier oscillator (SCO)	64
6. Calibration and SCO regulator	61
7. Transmitter	60
8. Relay module[2]	66, 67
9. Trigger circuits	58, 59 (worst case)
D. One Subcommutated Channel (Outputs 48-63)	
1. Timing and control	1-3, 5-19, 33, 34
2. Commutator	1/35 of 20; 1/5 of 21 and 23; 22, 24
3. Subcommutator	37, 1/8 of 38
4. Isolation amplifier	62

EXHIBIT 5 (Continued)

Output/Telemetry Equipment Required | Item Number[1]

		Output/Telemetry Equipment Required	Item Number[1]
	5.	Subcarrier oscillator (SCO)	64
	6.	Calibration and SCO regulator	61
	7.	Transmitter	60
	8.	Relay module[3]	66, 67
	9.	Flash intensity circuits[4]	39, 43
	10.	Attenuators	Assume two R's per channel

E. One Commutated Channel (Outputs 64-128)

	1.	Timing and control	1-3, 5-19
	2.	Commutator	1/35 of 20; 1/5 of 21 and 23; 22, 24
	3.	Isolation amplifier	62
	4.	Subcarrier oscillator (SCO)	64
	5.	Calibration and SCO regulator	61
	6.	Transmitter	60
	7.	Relay module[5]	66, 67
	8.	Thermistor regulator[6]	69
	9.	Attenuators	Assume two R's per channel

Notes: (1) See appendix.
(2) Outputs 33-47 only.
(3) Outputs 56-63 only.
(4) Outputs 48-52 only.
(5) Outputs 96-128 only.
(6) Outputs 96-100 and 64-71 only.

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parts. Component part failure rates are as given previously in Reference 2. The numerical results for the probability of each output being present are tabulated in Exhibit 4.

b. Derivation of Output Relative Values, V_i

In order to derive a rational assignment of relative values to each state, assume first that each main commutated channel has a value of unity. Then, since the 16 subcommutated channels utilize 2 main commutated channels, assign a value of 1/8 to each subcommutated channel. The 45 telltale bits utilize 3 main commutated channels, and, hence, each bit may be assigned a value of 1/15. The memory readout essentially replaces one commutator when it is in service; thus, assign it a value of 35. There is no direct relationship between the time marker and a main commutated channel, but a value of 2 is judged to be reasonable in the present context. If these values are normalized to total unity, the V_i shown in Exhibit 4 are the result.

If the operation of Equation (1) is performed using the data of Exhibit 4, the telemetry subsystem figure of merit is found to be approximately 0.54. A cursory examination of Exhibit 4 indicates that the memory readout alone contributes nearly half of the subsystem figure of merit. Since the probability associated with this output is relatively high, reducing the relative value of the memory readout will reduce the telemetry subsystem figure of merit, and vice versa.

5. Results

The design and implementation of the telemetry subsystem are considered by PRC to be good. Since telemetry is not used to transmit experiment results on GEOS, it is felt that the nonredundant design is adequate.

The telemetry subsystem figure of merit of 0.54 (indicating roughly that the subsystem is expected to be 54-percent available at the end of one year) is judged to be not unreasonable in view of the generally pessimistic assumptions used throughout the GEOS subsystem assessments. The figure of merit is highly dependent on the relative values assigned to the individual outputs.

6. <u>Summary</u>

a. The design and implementation of the GEOS telemetry subsystem are good.

b. The expected proportion of telemetry subsystem capability available at the end of one year is approximately 54 percent.

REFERENCES

1. Operational Reliability Assessment of the GEOS A Spacecraft, Technical Advisement Memorandum No. 106-10 (PRC D-1056), 29 October 1965.

2. Component Part Failure Rate Assignments for Reliability Assessment of the GEOS Satellite, Technical Advisement Memorandum No. 106-6 (PRC D-1027), 8 June 1965.

APPENDIX

FAILURE MODE AND EFFECT ANALYSIS

Item Number	Drawing Number	Circuit	Failure Mode	Q	D	DZ
1	7211-4821	Tuning fork oscillator	Any	3	3	1
2	7211-4821	Three-stage ripple counter	Any	3	2	
3	7211-4821	Five-stage ripple counter and amplifier	Any	2		
4	7211-4821	÷ 3, OR gate, TT reset amplifier	Any		4	
5	7211-4941	Sync one-shot	Any	2	5	
6	7211-4941	Synchronizable multivibrator	Any	2	8	
7	7211-4941	Flip-flop	Any	2	2	
8	7211-4941	Duty cycle circuits	Any	4	4	
9	7211-4941	Reset generator	True	1-1/2	4-1/2	
10	7211-4941	Reset generator	False	1-1/2	4-1/2	
11	7211-4941	Frame marker generator	Any	5	20	
12	7210-4911	Step one-shot	Any	2	3	1
13	7210-4911	B counter input circuit	Any	2	2	1
14	7210-4911	B counter	True	5	11-1/2	1/2
15	7210-4911	B counter	False	5	11-1/2	1/2
16	7210-4821	A counter input circuit	Any	2	2	1
17	7210-4821	A counter	True	8	17	1/2
18	7210-4821	A counter	False	8	17	1/2
19	7210-4821	Dead time circuit	Any	2		

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Parts Count				Failure State	Comments
R1	C1	C2	Other		
9	1	6	1 tuning fork	2	
6	3	1	2 IC	2	
5	3		5 IC	2	
5			3 IC	9	
6	2			2	
11	5			2	
8	4			2	
10	1			2	
5-1/2	1	1/2		2	Assumes failure holds timing circuits reset
5-1/2	1	1/2		19	Indeterminate
26	10			2	Worst-case assumption
5	2			2	
6	1			2	
10-1/2	2-1/2			2	If counter fails so that either no outputs are true or more than one output is true, all encoded data are lost; if counter fails so that only one output is true, then its data groups will be continuously telemetered
10-1/2	2-1/2			4	(See above comment)
6	1			2	
16	4			2	If counter fails so that either no outputs are true or more than one output is true, all encoded data are lost; if counter fails so that only one output is true, then one channel from each data group will be continuously telemetered
16	4			3	(See above comment)
2	1			2	

Item Number	Drawing Number	Circuit	Failure Mode	Q	D	D2
20	7210-4761	Commutator 1 (five data groups of seven channels each)		35 (O)	35 (O)	
21	7210-4761	Commutator 1 (five data groups of seven channels each)		35 (S)		
22	7210-4761	Commutator 1 (five data groups of seven channels each)		5 (S)	5 (O)	
23	7210-4761	Commutator 1 (five data groups of seven channels each)		5 (O)		
24	7210-4761	Commutator 1 (five data groups of seven channels each)			45 (S), 5 (O)	
25	7210-4761	Commutator 2		35 (O)	35 (S)	
26	7210-4761	Commutator 2		35 (S)		
27	7210-4761	Commutator 2		5 (S)	5 (O)	
28	7210-4761	Commutator 2		5 (O)		
29	7210-4761	Commutator 2			45 (S), 5 (O)	
30	7210-4741	Attenuators, commutator				
31	7210-4711	Attenuators, commutator				
32	7210-4731	Attenuators, commutator				
33	7211-4741	Subcommutator regulator	Any	2	1	2
34	7211-4741	Subcommutator control	Any			
35	7211-4741	Attenuators, subcommutator 1				
36	7211-4741	Attenuators, subcommutator 2				
37	7211-4721	Subcommutator 1		16 (S)	9	
38	7211-4721	Subcommutator 1		16 (O)		
39	7211-4761	Light intensity detectors		2	2	
40	7211-4761	Light intensity detectors		1	2	
41	7211-4761	Light intensity detectors		1	2	
42	7211-4761	Light intensity detectors		1	2	

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Parts Count				Failure State	Comments
R1	C1	C2	Other		
				12	Open input
				11	Superimposed data
				6a	Superimposed data
				11	
5	5			2	Worst-case assumption
				12	Open input
				11	Superimposed data
				6b	Superimposed data
				11	
5	5			2	Worst-case assumption
39				12	Worst-case assumption
46				12	Worst-case assumption
54				12	Worst-case assumption
3		1		7	
			5 IC	7	
6				13a	Worst-case assumption
15				13b	Worst-case assumption
16			2 IC	8a	
			2 IC	13a	
10	1	1		16a	Lose flash intensity indication 1 and flash control pulse
6	1	1		16c	Lose flash intensity indication 2
6	1	1		16c	Lose flash intensity indication 3
6	1	1		16c	Lose flash intensity indication 4

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Item Number	Drawing Number	Circuit	Failure Mode	Q	D	DZ
43	7211-4761	Light intensity detectors		3	1	
44	7211-4721	Subcommutator 2		16 (S)	9	
45	7211-4721	Subcommutator 2		16 (O)		
46	7210-5221	Telltale register 1	Any			
47	7210-5221	Telltale register 1	True			
48	7210-5221	Telltale register 1	False			
49	7210-5221	Telltale register 1	False			
50	7210-5221	Telltale register 2	Any			
51	7210-5221	Telltale register 2	True			
52	7210-5221	Telltale register 2	False			
53	7210-5221	Telltale register 2	False			
54	7210-5221	Telltale register 3	Any			
55	7210-5221	Telltale register 3	True			
56	7210-5221	Telltale register 3	False			
57	7210-5221	Telltale register 3	False			
58	7210-4851	Trigger circuits, register	Any	2	1	2
59	7210-4851	Trigger circuits (5 circuits)	Any	10	10	
60	7211-4501	Transmitter	Any	9	7	1
61	N/A	± Calibration and SCO regulator	Any	3		
62	7211-4641	Isolation amplifier 1	Any	1		
63	7211-4641	Isolation amplifier 2	Any	1		
64	N/A	Subcarrier oscillator 1	Any	5	3	
65	N/A	Subcarrier oscillator 2	Any	5	3	
66	7211-4621	Relay module	True	1/2	1/2	
67	7211-4621	Relay module	False	1/2	1/2	
68	7211-4871	Time marker generator	Any	6		1
69	7207-4981	Thermistor regulator	Any	9	5	

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| Parts Count | | | | Failure | |
R1	C1	C2	Other	State	Comments
11		3		16b	Lose all flash intensity indications
16			2 IC	8b	
			2 IC	13b	
3			11 IC	10a	
			20/2 IC	10a	
29			15/2 IC	15a	
			5/2 IC	14a	
3			11 IC	10b	
			20/2 IC	10b	
29			15/2 IC	15b	
			5/2 IC	14b	
3			11 IC	10c	
			20/2 IC	10c	
29			15/2 IC	15c	
			5/2 IC	14c	
3		2		19	Indeterminate
25	15			19	Indeterminate
35	69	2	1 IC, 19 inductors, 1 crystal	1	
10		2		1	Assumed parts count
7	5			6a	
7	5			5	
8	2	2	1 inductor	6a	Assumed parts count
8	2	2	1 inductor	5	Assumed parts count
1			1/2 relay	6b	
1			1/2 relay	17	
15	1	2	1 inductor	18	
32		4		20	Worst-case assumption