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# FINAL REPORT

describing

# DESIGN AND DEVELOPMENT OF A 10 NANOSECOND SEMICONDUCTOR SWITCH

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IN ACCORDANCE WITH CONTRACT NAS8-11611

FOR

GEORGE C. MARSHALL SPACE FLIGHT CENTER

NASA

HUNTSVILLE, ALABAMA

## TABLE OF CONTENTS

I. INTRODUCTION

II. DEVICE DESIGN

A. DESIGN GOALS

B. EPITAXIAL STARTING MATERIAL

C. SURFACE GEOMETRY

D. DIFFUSED REGIONS

E. PACKAGE DESIGN

III. FABRICATION PROCESS

A. STARTING MATERIAL

B. SURFACE PREPARATION

C. DIFFUSIONS

1. SILICON DIOXIDE LAYERS

2. BASE AREA

3. $P^+$ DIFFUSION

4. EMITTER DIFFUSION

D. ALUMINUM EVAPORATION

E. PHOTO RESIST

1. MASKS

2. OXIDE AND ALUMINUM ETCH

F. SURFACE PASSIVATION

G. ASSEMBLY

IV. TEST METHODS AND TRANSISTOR EVALUATION

A. INTRODUCTION

B. SWITCHING CIRCUITS

1. CIRCUIT DESIGN CONSIDERATIONS

2. CIRCUIT #1 AND CIRCUIT #2

3. CIRCUIT #3

4. CIRCUIT #4

C. CHARACTERISTICS

1. POWER DISSIPATION

2. PARAMETERS

D. VHF APPLICATIONS

E. FINAL PRODUCTION UNITS

V. PERSONNEL

# I. INTRODUCTION

## I. INTRODUCTION

The scope of work of this contract involved the design, development, fabrication and delivery of five (5) prototype and fifty (50) production semiconductor switches capable of extending the speed of high level switching transistors into the low nanosecond range.

Completion of this contract was accomplished in three (3) phases, which were as follows:

Phase I consisted of the essential study and the preparation of a complete design of the units.

Phase II consisted of the fabrication and delivery of five (5) prototype units which were submitted, evaluated and approved by NASA.

Phase III consisted of the fabrication and delivery of fifty (50) production models in conformity with the objective specification DCN 1-4-40-0158.

This report will be devoted to an overall appraisal of the work done under this contract. The principal areas which are to be discussed include:

1. Device Design.
2. Fabrication Processes.
3. Circuit Design and Typical Test Results.
4. Test Results of Fifty (50) Production Units.

A section devoted to other possible applications of this device is also included.

## II. DEVICE DESIGN

## II. DEVICE DESIGN

A. Design Goals: Criteria applicable to the semiconductor switches fabricated herein are as follows:

1. Mechanical Specifications:
   a. Hermetically sealed.
   b. Materials: silicon semiconductor crystal.
   c. Stud-mounted isolated collector, with double-ended case.

2. Environmental Specifications:
   a. Temperature cycling: $-65^{o}C$ to $+200^{o}C$ 5 cycles.
   b. Moisture resistance: 10 cycles
   c. Centrifugal: 1,000 g.
   d. Storage life: plus $200^{o}C$, 1000 hrs.
   e. Shock: 500 g.
   f. Vibration: 20 g, 100 cps to 2000 cps.

3. Electrical Specifications:
   a. Collector-Emitter Breakdown Voltage $BV_{CEO(SUS)} = 50$ volts min.
   b. Collector Cutoff Current $V_{CE} = 50V$, $T_J = 20^{o}C$, $I_{CES} = 1$ mA max. $I_C = 0$

      Collector Cutoff Current $V_{CE} = 50V$, $T_J = 200^{o}C$, $I_{CES} = 10$ mA max. $V_{BE} = 0$
   c. Emitter Cutoff Current $V_{EB} = 7V$, $T_J = 200^{o}C$, $I_{EBO} = 1$ mA max, $I_C = 0$
   d. DC Current Gain $I_C = 10A$, $V_{CE} = 4V$, $h_{FE} = 10$ min
   e. Saturation Resistance $R_{CE(SAT)} = 0.1$ ohms max.
   f. Base to Emitter Voltage $I_C = 10A$, $V_{CE} = 4V$, $V_{BE(SAT)} = 2.0V$ max, $I_B = 1A$.

g. Turn On Time ($T_D \neq T_R$) $I_C$ = 10A, $I_B$ = 1A

$T_{on}$ = 5 n sec max

h. Turn Off Time ($T_S \neq T_F$) $V_{BE}$ = -5V

$T_{off}$ = 5 n sec max $V_{CE}$ = 50V

(assuming unsaturated condition)

4. Thermal Characteristics:

a. Collector Power Dissipation: $P_C$ = 25 watts max.

(See Derating Curve, Section II E)

b. Thermal Resistance: $\theta_{JC}$ = 4.0°C/Watt max.

c. Junction Temperature Range: -65°C to 200°C

B. Epitaxial Starting Material:

The starting material for this device consisted of an "N" type epitaxial layer on an "$N^{+}$" substrate. The prime reason for employing the epitaxial collector design is that it afforded the best compromise among the device parameters of collector breakdown, capacitance and series resistance.

Because of the predominant role of collector design on the device parameters of (1) collector-base breakdown, (2) collector saturation voltage, and (3) collector-base junction capacitance, it was necessary to take all three (3) parameters into consideration when selecting the epitaxial layer resistivity and thickness. Parameters (1) and (3) improve with increasing resistivity and thickness while (2) is degraded. Based on these considerations, calculations were made and the following initial specifications for epitaxial layer resistivity and thickness were set:

Layer Resistivity -- 3.0Ω cm ±20%

Layer Thickness -- .85 mil ±15%

After several preliminary runs the values of layer resistivity and thickness were increased to the following values:

Layer Resistivity -- 3.2Ω cm ±20%

Layer Thickness -- 1.0 mils ±10%

The objectives of this material change were to reduce $C_{ob}$ and increase $BV_{CEO}$ (sustained) thereby increasing device switching speed and creating a safety margin to protect the device against catastrophic secondary breakdown during the switching cycle.

C. Surface Geometry:

The interdigitated structure shown in Figure 1 was selected because of its inherent high emitter periphery to emitter area ratio. This type of design would enhance the beta linearity, $V_{CE\ SAT}$, $f(t)$, and power handling capabilities of the device.

To achieve this basic goal several areas of the device construction were improved upon. These improvements were:

1. Optimized length, width and taper of finger design.
2. Tightened spacing throughout the design geometry.
3. Minimized area of contact pads.

To increase finger length while reducing the finger width it was necessary to increase the aluminum contact thickness and add a $P^+$ base contact region in order to maintain negligible voltage drops along the fingers.

The total base contacting area is 50 $mils^2$ and the emitter contacting area is approximately 100 $mils^2$.

The conductivity to the ends of the base fingers was insured by the $P^+$ diffusion. This design scheme also appears

to minimize the inherent heating effects normally noted at the emitter base junction around the tip of the base fingers, i.e., close to the emitter lead.

Generally, all fingers and contact areas were tapered and rounded to eliminate hot spots and/or leakage paths. Equal spacing of all geometries at all points was another consideration.

The resulting design is as follows:

| | | |
|---|---|---|
| Base Area | -- | 2175 $mil^2$ |
| Emitter Area | -- | 1000 $mil^2$ |
| Emitter Periphery | -- | 1000 $\neq$ mil |
| Base Periphery | -- | 175 mil |
| Chip Size | -- | 60 mil X 80 mil |

Other areas of design criterion include circular alignment keys on each device chip and a 5 mil wide scribing path, free of oxide and aluminum.

D. <u>Diffused Regions:</u>

<u>Base Region</u>:

Several requirements had to be taken into consideration in determining the concentration levels and the depth of the base region. The $BV_{EBO}$ requirement of 7 volts limited the base surface concentration to a maximum value of approximately 7 X $10^{18}$ atoms/cc.

The $BV_{CBO}$ requirement imposed limitations on the base width-impurity gradient relationship working within these limitations; the base region was designed to yield a high gain, high $f_T$ structure. Base surface concentration and base depth of 5 X $10^{18}$

atoms/cc and 3.0 microns, respectively, was employed for these units. A base width of 1.0 micron is the design center.

Emitter Region:

Conditions for the emitter diffusion had essentially been determined by the base design criteria. The depth of the diffusion required was 2.0 microns to meet the requirement of 1.0 micron base width. A high concentration was required ($\sim 10^{21}$ atoms/cc) to achieve the necessary injection efficiency into the highly doped base region which is needed for high gain.

Simultaneously with the emitter diffusion an $N^{+}$ band was diffused into the surface of the epitaxial collector layer in an area adjacent to and completely surrounding the base diffused junction. This band has two (2) functions. It serves to prevent channelling across the surface of the device from the base junction to the edge of the die. Secondly, it has been observed that such a band improves the gettering effects normally observed during phosphorus diffusion by virtue of its proximity to the collector- base junction.

$P^{+}$ Diffusion:

The primary purpose of this additional diffusion step has been discussed under surface geometry design. There are two (2) positive aspects of design for this diffusion. The primary requirement is to achieve a highly doped conducting layer within the base diffused region in order to optimize the device parameters of $r_b^{1}$, $V_{BE(SAT)}$, $V_{CE(SAT)}$ and beta linearity. Another important function of the $P^{+}$ layer is to provide protection

against the occurrence of a surface inversion layer over the more lightly doped base region. From a negative viewpoint this region must be very carefully defined with respect to both lateral dimensions and penetration.

E. Package Design:

The original contract called for a 7/8" double-ended stud design package capable of sustaining the 100 watts power dissipation of the transistor. The thermal resistance of the device in this package was to have a maximum value of 1.75°C/Watt. The essentials of this package design are illustrated in Figure 2 .

Since the beginning of the contract there have been two (2) revisions made in package design. The first was from the 7/8" to an 11/16" double-ended stud. This change was mutually agreed upon by NASA and Bendix personnel for the following reasons:

1. A smaller device for the NASA application was desirable.
2. Bendix had already been using the 11/16" diameter package for other devices and consequently, equipment and techniques required for device assembly were readily available.

Because of the size reduction, the thermal characteristics for the device were reduced. The collector power dissipation was lowered from 100 watts to 50 watts and the thermal resistance was increased from 1.75°C/Watt to 3.5°C/Watt. Drawings of the redesigned 11/16" stud assembly are shown in Figure 3.

The second revision, replaced the 11/16" diameter stud by a 7/16" diameter stud. This change took place during the early

## III. FABRICATION PROCESS

### A. Starting Material

Material was ordered and received from three (3) vendors, Texas Instruments, Monsanto and General Micro Electronics, and was then evaluted. Devices which have been made from each of the vendor's material had been acceptable; however, differences in yield, distribution, and parameters did exist consistent with the control surface topograph of the respective vendor's epitaxial material.

Since that time Bendix purchased and installed an Ecco epitaxial reactor system. A photograph of this system is included in this report as Figure 6. The epitaxial material obtained from this system had surface topography as good as material purchased from outside vendors. Hence, several of the latter devices processed under this contract were fabricated on our own epitaxial material.

A summary of the material used for the various lots is given in Table 1. The overall range of resistivity and thickness utilized during the course of this contract was 2.6 to 3.4 ohms cm and 0.67 to 1.03 mils, respectively.

### B. Surface Preparation

Prior to the initial thermal oxidation step, the epitaxial wafers were thoroughly cleaned. This operation consists of the following rather universal steps:

1. A trichloroethylene rinse to remove organic contaminants.

2. A hydrofluoric acid (HF) rinse to remove oxide films.

3. Chemical treatment to remove ion impurities and to provide a light protective oxide layer.

C. Diffusions (Refer to Table 1)

1. Silicon Dioxide Layers

(a) Initial Oxide:

The initial oxide layer at 1050°C in a dual cycle oxygen atmosphere (thickness of this layer is 7000 to 8000 Å). The first cycle was a wet $O_2$ atmosphere which was followed by a dry $O_2$ atmosphere (2nd cycle). Both cycles are performed in the same furnace without removing the slices by using a three way stopcock. The purpose of the dry cycle is to densify the oxide grown during the wet cycle. This procedure reduced the pinholes per unit area to approximately (zero). This area is discussed in a subsequent section of this report.

(b) Base Diffusion Oxide:

During the base diffusion cycle an oxide layer is regrown over the base region to provide masking for subsequent diffusions. All diffusions were performed at 1200°C in an oxygen atmosphere. The thickness of the oxide obtained will depend upon the time and conditions (wet and/or dry $O_2$) of the diffusion.

The initial lots processed under this contract underwent a three (3) hour base diffusion consisting of a 1/2 hour wet $O_2$ cycle followed by a 2-1/2 hour dry $O_2$ cycle. The oxide thickness was approximately 6000 $A^o$. As the processing continued the base diffusion time was decreased and consequently, the thickness of oxide grown decreased. The following chart lists the various diffusions, times, and conditions and the corresponding oxide grown for each case:

| Total Time (Min) | Cycle Time (Min.) | | Oxide Thickness ($A^o$) |
|---|---|---|---|
| | Wet | Dry | |
| 150 | 30 | 120 | 6000 |
| 120 | 30 | 90 | 5600 |
| 90 | 15 | 75 | 4400 |
| 75 | 15 | 60 | 4100 |
| 60 | 15 | 45 | 3800 |
| 60 | 0 | 60 | 2500 |

(c) Post $P^+$ Deposition Oxide:

Two (2) types of oxides have been utilized after the $P^+$ deposition, the thermal oxide and the pyrolytic oxide. The thermal oxide was grown at 1000°C and the pyrolytic oxide was deposited at approximately 725°C. A lay-out drawing of the pyrolytic oxide system is shown in Figure 7.

tolerances and geometry quality acceptance criterion. Mask imperfections such as flaws, pinholes, (spots) and peripheral defects are clearly defined by the specification "Mask Acceptance" IN-156.

A thorough vendor evaluation was conducted at the beginning of this contract with the emphasis on capability in mask construction and mask inspection. On the basis of vendor evaluation and the quotes received, the decision was made to contract with the Qualitron Corp., Danbury, Conn.

There were three (3) shipments of masks received by Bendix. The first shipment received was inspected and conditionally accepted to construct devices for initial evaluation. This set of masks failed to meet the spot and peripheral defect specifications and some of the dimensions were questionable. One (1) set of masks from this shipment was returned for vendor evaluation.

A second shipment of masks were received and inspected by Bendix in early October. Those masks were rejected due to excessive peripheral defects, spots and smears. The vendor was notified and re-evaluated his handling and packaging of masks.

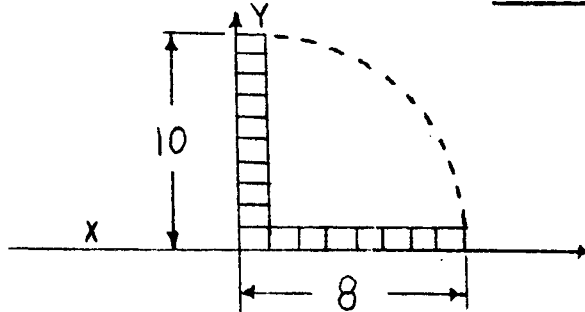
The third shipment of masks were received in November, which were inspected and accepted. Table 2, shows a comparison of the three (3) shipments of masks with respect to defects.

| THE BENDIX CORPORATION<br>BENDIX SEMICONDUCTOR DIVISION<br>HOLMDEL, N.J. | PROCESS SPECIFICATION<br>MASK ACCEPTANCE | Number - IN - 156<br>Pg. (1) of (2) Pgs. |
|---|---|---|

A. GENERAL NOTES:

1. All dimensions ± .05 mil (50 millionths of an inch) exception noted

2. The active mask area to be a circle of 1.25" dia.




X dir ± 8 (.080") patterns
Y dir ± 10 (.060") patterns

3. The inspection area referred to in the specification to a circle of 1" dia. All patterns which fall within (better than 1/2 of the pattern is considered within) this circumference are covered by the following inspection criterion:

$\frac{1000}{80} \approx 12$ Xdir ± 6 Patterns inspected

$\frac{1000}{60} \approx 16$ Ydir ± 8 Patterns inspected

Approximately $150 {}^{+10}_{-0}$ patterns will be in the inspection area.

4. The cumulative tolerance of the total array of 12 patterns in the X direction and 16 patterns in the Y direction shall not exceed ± .050 mils. Registration (true position) from mask to mask to be within ±.100 mils.

5. Asterisks (*) Radius dimensions and centers are nominal however the parallelism of the registered patterns must be maintained, i.e. spacing between registered patterns ± .100 mils.

6. Breaks in the periphery of a pattern either into or out of the pattern are allowed if they protrude no further than the specification allows, i.e. .0001". However sharp spikes will be considered as grounds for rejection.

7. Grid work not critical - Dimensional accuracy ± .0002. No spec on breaks and/or pin holes.

8. True position of alignment dot centers to device centers must be ±.050 mils, dimensional tolerance of dot ± .0001".

9. The allowable number of defective patterns within the 1" dia. inspection circle (≈ 150 patterns) not to exceed (7) seven ≈ 5%.

(cont'd page 2)

APPROVALS: R. REBER DATE: 5-8-64

| | | |
|---|---|---|
| Prepared by: | RLReber | 5-13-64 |
| Product Manager: | [illegible] | 5-14-64 |
| Industrial Engineer: | [illegible] | 5-14-64 |
| Q.C. Manager: | [illegible] | 5/18/64 |
| Authorized: | [illegible] | MAY 1 1964 |

ENGINEERING CHANGE RECORD

| E.C. | DATE | CHECKED | E.C. | DATE | CHECKED |
|---|---|---|---|---|---|
| 3104 | 5-13-64 | RLR | | | |
| 3104A | 5-21-64 | RLR | | | |
| | | | | | |
| | | | | | |

9. (continued) Defects defined as discrepancies in geometry and/or dimensions, spots and pin holes (see individual mask specifications), lines, scratches, etc.

10. The allowable number of defective glass plates shall not exceed 5% in any one shipment.

11. Border of glass tile to be opaque.

12. Mask tool # and Issue letter on all masks and original art work.

13. The glass plates to be cut 2" ± 1/16 sq. with pattern (grid lines) parallel to the cut edges and the active mask area centered to within ±0.1".

SPECIFIC SPECIFICATIONS:

1. Base Mask. Geometry rejection criterion.
   a. Pin holes in the opaque (base area) greater than 0.080 mils dia. not allowed.
   b. Opaque spots greater than 0.10 mils in the clear area within 0.001" of the base are not allowed.

2. $P^+$ Geometry rejection criterion.
   a. Pin holes in the opaque ($P^+$ area) which are greater than 0.20 mils dia. are not allowed.
   b. Opaque spots greater than 0.10 mils dia. in the clear area are not allowed. Clear area defined to be all clear area within 0.002" outside $P^+$ geometry.

3. Emitter. Geometry, rejection criterion
   a. Pin holes in the opaque (emitter area) greater than 0.080 mils dia. not allowed.
   b. Opaque spots greater than 0.10 mils dia. in the clear area are not allowed. Clear area defined to be all clear area within .0005" inside guard ring.
   c. Guard ring dimensional tolerance ± .0001". Pinhole spec does not apply to guard ring.

4. Contact Cut: Geometry rejection criterion
   a. Pinholes in opaque (Contact Cut Areas) greater than 0.20 mils dia. not allowed.
   b. Opaque spots greater than 0.10 mils ida. in the clear area are not allowed. Clear area defined to be all clear area within 0.0015" outside contact geometry.

5. Al Contact Cut. Geometry rejection criterion
   a. Pin holes in opaque (area to be etched) greater than 0.10 mils dia. not allowed. Opaque area defined to all opaque area within 0.0015" outside al contact geometry.
   b. Opaque spots greater than 0.20 mils dia. in the clear areas are not allowed.

2. Oxide and Aluminum Etch:

The present system utilizing Kodak KPR-KPL at high spinning speeds appeared to offer advantages in etch resistance, adhesion and definition. Micro-filtration of all chemicals and minimum handling of wafers in process resulted in cleaner reproductions and enhanced yield. The Micro-Mechanics alignment and exposure system had the alignment tolerance and exposure conditions deemed necessary. Development was accomplished in standard Kodak chemical baths. Etching of the wafers was done in an ammonium fluoride - HF etch.

Coating and alignment (exposure) operations were in absolute filter dust boxes while all other operations were in 0.5 micron dust boxes.

Photo-micrographs of the geometric reproductions are shown in Figures 8 and 9.

Etching of thick aluminum layers was accomplished by using KTFR (Kodak Thin Film Resist) and a phosphoric - nitric - $H_2O$ etch. The adhesion and etch resistances of the KTFR ideally suited it for this operation. There have been two (2) techniques evaluated for this operation.

The first technique used was photoresist followed by complete etching of the aluminum. However, due to the thickness gradient of the deposited aluminum , the etching resulted in undercutting of the contacts on the thinner side and bridging of contacts on the thicker side. This problem led to the conception of the second technique which was used for fabrication of the final devices.

After the aluminum is deposited the wafer is photoresisted using the KTFR system. The wafer is then placed in the aluminum etch solution for a time long enough to remove approximately 30% of the aluminum. The photoresist is then removed and the wafer is re-photoresisted using KTFR. It is again placed in the etch solution where the remaining aluminum is removed. This method has drastically reduced undercutting and eliminated bridging. Figure 10 shows the comparison between the two (2) methods of etching aluminum.

Resist removal is accomplished in hot sulphuric acid solutions and/or in commercially available resist strippers.

### F. Surface Passivation

The use of thermal oxides in planar processing can be improved through densification and/or combination with pyrolytic technology. A good gauge of oxide quality is the number of pinholes/unit area. In order to test the various oxide techniques, a chlorine etch system was designed and constructed. Thus, any flaw or imperfection in the oxide will permit etching of the silicon subsurface by gaseous chlorine.

The use of a thermally grown dry oxide for the subsequent lots processed has proven quite successful. However, the pyrolytic oxide was advantageously employed as the final device layer. The process was carried out at a lower temperature, and therefore, junction travel was minimized. In addition, the silicon dioxide layer formed by the pyrolytic process does not require silicon surface atoms but is provided totally by the thermal cracking of an organo silane compound.

vendors (National Beryllia and Mitronics) who had supplied Bendix with 11/16" packages. However, none of the packages received were acceptable. There were two (2) problems with all packages received: (1) the beryllia pad would crack from the heat of die mounting and/or (2) the metallized patterns would blister causing poor wetting of the die to the pad and in turn thermal resistance problems. With no acceptable 11/16" packages being acquired NASA and Bendix personnel agreed to further reduce the package size to 7/16". These changes are more thoroughly discussed in Section II E.

The die mounting operation was performed in a dry box using eutectic mounting techniques. Results indicated little or no degradation of electrical characteristics and uniform, low thermal resistance measurements.

Initially, wire was used to bond to the emitter and base contacts. This bonding was of the thermo-compression type. However, this method of bonding (10 mil wire to emitter) was introducing pressure across the fingers of the device which tended to degrade emitter-base characteristics.

Experiments were then conducted using a flat ribbon (10 X 4 mil). This method proved very feasible and was used for both the prototype and final devices. Two, 2 mil wires were used to bond to the base pads. Bonding experiments produced bonds which withstood an axial pull great enough to break the wire.

The doming of units was accomplished by the resistance weld method in a dry box.

# IV. TEST METHODS AND TRANSISTOR EVALUATION

## IV. TEST METHODS AND TRANSISTOR EVALUATION

### A. Introduction

The function of the Applications Department was to evaluate the transistor static and dynamic characteristics, design and build any special test circuits necessary for evaluation, and to assist Development Engineering in transistor design.

Switching circuits were developed and constructed to evaluate the switching capability of the transistor. A total of four (4) switching circuits were designed, with each successive circuit containing an improvement.

Device characteristics were tested according to the NASA specification.

Transistors were evaluated as development-lots were made available. Parameter deviations from specification were noted. Development Engineering made appropriate changes in design or processing to have the parameter satisfy the specification.

The transistors were also evaluated in high frequency power amplifier circuits to estimate their potential as high frequency power amplifier transistors.

### B. Switching Circuits

#### 1. Circuit Design Considerations

The design considerations for the applicable switching circuit are of utmost importance to realistically measure the actual switching time of the device. The following criteria were established for circuit design:

a. Demonstrate the switching capability of the device.

b. Adjustments minimized during testing of a large number of units.

c. The unit under test should be plugged into a socket, no soldering should be required.

d. Parasitic reactances must be avoided. All leads should be as short as possible.

e. Reproducibility of the circuit.

f. One circuit should be used to measure "on" and "off" time.

2. Circuit #1 and Circuit #2

Initially, two (2) test circuits were designed to evaluate the transistor switching characteristics. Circuit #1 (Figures #13 and #14) was the resulting design for "$t_{on}$" evaluation, and Circuit #2 (Figure #15) for "$t_{off}$" evaluation. Separate circuits for "$t_{on}$" and "$t_{off}$" were designed to obtain optimum switching characteristics for each parameter.

A Baker clamp was utilized in the circuit (Figures #13 and #15) to minimize storage time. The main purpose of this feedback clamping technique was to keep the collector-base junction from becoming forward biased when the on-drive pulse was applied to the input. Diodes $D_1$ and $D_2$ formed the Baker clamp, and kept the transistor out of saturation. The voltage drop across the diodes is such that the collector junction can never become forward biased and any base driving current in excess of that required to bring the transistor to the edge of saturation is simply channelled

around the base through the upper diode.

The use of a Baker clamp slightly complicates the design because the device specifications must be such as to keep the transistor out of saturation for worst case conditions. The storage time problems are now transferred to the diode which must have a much faster recovery time than the transistor if the Baker clamp method is to be of value.

Figure 14 shows the original "$t_{on}$" Circuit No. 1 with the diodes removed. The "$t_{on}$" was also measured in this circuit. The switching time was slightly better than that measured in circuit Figure #13.

The diodes initially used in the clamp circuit were specified as having 4 or 5 nanosecond recovery times. Faster diodes were not available from stock at the time of the circuit design. The diodes tended to increase the collector turn-off time. Future circuits must have faster diodes.

Care was taken during physical layout of the circuit to minimize parasitics. All leads to the external bias supply were bypassed with suitable capacitors to keep circuit lead inductance to a minimum.

At the time of development of Circuits #1 and #2, a satisfactory transistor socket was not available, and the transistor under test had to be soldered into the circuit. An investigation into the design of a socket suitable for this application was undertaken. The socket had to provide short lead lengths from the circuitry to the transistor pin

connections, and shielding between input and output for isolation. Utilization of a test socket would enable testing of devices to be conducted in a more efficient manner.

The current transformer, $T_1$, in each of the circuits was used to monitor the base current. In this manner, the diode clamping action was observed and the required base current was determined from this observation.

In the turn-off circuit (Circuit #2), reverse bias was applied to the transistor base terminal through a 5 ohm resistor.

Test Circuits #1 and #2 provided valuable data and design insight for redesign and improvement of the test circuits.

3. Circuit #3

A third test circuit was constructed which incorporated many new features not present in the original two circuits.

The main reasons for redesign of the test circuits were:

a. Eliminate the necessity of two test circuits, (one for "$t_{on}$" evaluation and another for "$t_{off}$").

b. To provide a more efficient method of placing the transistor in the circuit (a socket was used).

c. To allow observation of the fastest switching time possible.

d. Further reduction of parasitic effects.

Parasitic inductance and capacitance were minimized by careful location of parts in the circuit. The circuit parts were carefully selected and high frequency non-inductive resistors were used. All circuit lead lengths were minimized. Insertion inductance, resistance, and capacitance due to the current transformers were eliminated by monitoring the base and collector current with a voltage probe. The current probes used in Circuits #1, #2, and #3 were not used in Circuit #4.

Circuit #4 contained the same type transistor socket as the one used in Circuit #3.

Due to the pulse generator impedance of 50Ω, the input of switching Circuit #4 had to have an impedance of about 50Ω. The generator incorporated a charge line, and mismatch of generator to circuit would cause reflections. Matching was accomplished by resistor $R_3$ in series with a resistance having a value

$$\left[ R_7 \quad \beta\left(@\frac{I_C}{I_B} = 10\right)\right] ;$$

i.e., resistor $R_3$ in series with resistor $R_7$ times the forced $\beta$ of the transistor in the conducting state.

To isolate direct current from the pulse generator, during the absence of the "on" pulse, a blocking network of $R_1$, $R_2$, and $C_1$ was placed at the input of the circuit. The resistors $R_1$ and $R_2$ were 1KΩ resistors and served two purposes. The first was to present a high shunt impedance to the generator and eliminate a mismatch between generator

and the 50Ω circuit input-impedance; the second purpose was to provide a discharge path for capacitor $C_1$.

A clamping network consisting of $R_4$, $D_1$ and $C_2$ limited the load current flowing through $R_7$ to 10 amperes maximum.

The reverse bias network consisted of resistors $R_5$ and $R_6$, capacitor $C_3$, and inductor $L_1$. After the input pulse is removed, the capacitor $C_3$ acts like a 5V battery, sweeping the stored charge out of the base-emitter region. Capacitor $C_3$ helps achieve a faster collector turn off time. During the initial part of the turn-off time the inductor $L_1$ acts like a current source.

The input drive was obtained by placing a non-inductive 50Ω resistor across the pulse generator. The generator voltage was adjusted for a current of 1.0 amperes. The resulting generatory voltage was 50V. The generator, with pulse amplitude unchanged, was then connected to the switching circuit input.

In order to experimentally determine the operation of all the circuits described the BIG LEAF transistor was used. The switching time for Circuit #3 was better than that obtained in Circuits #1 and #2. Table #3 presents actual switching time data of individual devices in Circuits #3 and #4. This data demonstrates that the switching capability of the transistor element is in the 5 nSec. range but the circuit effect adds to the time.

Because of circuit limitations, a device design must have switching speeds of 1 nSec. to achieve 5 nSec. circuit switching time.

## C. Characteristics

### 1. Power Dissipation

Transistor collector power dissipation was determined for transistors in the TO-61 (11/16" stud) and the TO-60 (7/16" stud) isolated packages. It was felt that for large production quantities the maximum thermal resistance from junction to case for these two package types should be as follows:

TO-61: $\theta_{JC} = 3.5^{\circ}C/W$

TO-60: $\theta_{JC} = 4^{\circ}C/W$

These values were based on power dissipation tests performed in a temperature controlled environment. Table 4 presents the catastrophic failures versus power dissipation of ten TO-61's and ten TO-60's. The case of each transistor was kept at a temperature given by the thermal resistance junction to case and $T_J = 200^{\circ}C$ according to the formula

$$T_J = T_c + P_c\,\theta_{JC}$$

$$T_c = T_J - P_c\,\theta_{JC}$$

for TO-61: $T_c = 200^{\circ}C - P_c\ 3.5^{\circ}C/W$

for TO-60: $T_c = 200^{\circ}C - P_c\ 4^{\circ}C/W$

Figure #20 shows the power derating curves for the TO-61 and TO-60 packages based on test results of Table 4.

### 2. Parameters

Device testing was performed with appropriate test equipment. All measurements were made at $T_J = 25^{\circ}C$ unless otherwise stated. The test methods used are given in the Appendix.

As a summary, key parameters are plotted in Figure 21 through Figure 24 as a function of fabrication lots. Additional typical data is presented in Test Report Number 1. $h_{fe}$ versus $I_C$ at 50 Mc is shown in Figure 25 for a typical transistor of the final production units. The different production lots show an overall improvement of $h_{FE}$ with other parameters changing but still within specifications. High $h_{FE}$ at $I_C = 10A$ is essential to improve the switching time.

D. VHF Applications

Some transistors of the final production units were evaluated in high frequency power amplifiers to show their potential capability for this application. Measurements were made using the following circuits:

50 Mc Class A: Figure 26

50 Mc Class B: Figure 27

100 Mc Class B: Figure 28

Typical performance data is included with each amplifier circuit diagram. Additional data is plotted in Figure 29 through Figure 31 for operation in the 50 Mc Class B amplifier. The results show that the developed transistor is not only a good switch but also a good linear amplifying device.

## E. Final Production Units

The fifty (50) final production units were evaluated to specification. The data for all required parameters is presented in Test Report No. 2 through Test Report No. 4. All parameters are well within the required specification with exception of $V_{CEO}$ and switching time. All units meet the required $V_{CEO}$ of 50V. The switching time exceeds the 5 nSec. limit; however the time in excess of 5 nSec can be attributed to designing and testing in a fast switching circuit rather than to the capability of the transistor element. A continued circuit design effort and elimination of circuit parasitic reactances could possibly demonstrate the actual device switching capability.

# V. PERSONNEL

## V. PERSONNEL

### A. Project Manager

Mr. Albert Schrob served as project manager through Phase I of this contract. At that time, Mr. Schrob's position was that of Development Engineering Manager and he reported directly to Mr. Hy Newman, Chief Engineer of the Bendix Semiconductor Division. During the course of the program Mr. Schrob transferred to the Eclipse Pioneer Division of Bendix.

Mr. Charles F. Carroll replaced Mr. Schrob as Development Engineering Manager and served as project manager throughout the completion of this contract.

### B. Key Technical Personnel

The following key personnel have performed the work required for the design and development of subject semiconductor switch contract. Resumes of experience and eductional backgrounds are included.

BALTHASAR, PETER

| | |
|---|---|
| Realgymnasium Stuttgart, Germany 1951 | B.S. (Abitur) |
| Dipl. Eng. Technical University of Stuttgart, Germany 1957 | M.S.E.E. |
| Rutgers University | Graduate Work |

Mr. Balthasar is Manager, Applications Engineering Department, Bendix Semiconductor Division, and is responsible for testing and evaluating semiconductor products, electrical test specifications, development of transistor applications and field engineering. He joined the Bendix Corporation in 1959 as an applications engineer.

BRYAN, WILLIAM SCOTT

| | |
|---|---|
| U.S.A.F. Technical School | Basic & Advanced Tacan Maintenance |
| Monmouth College | Electrical Engineering 1960-1963 & Present |

Since joining Bendix in 1963 Mr. Bryan has assumed responsibility for supervision over photo-resist and evaporation operations related to processing of silicon planar epitaxial transistors and integrated circuits. He has written several papers describing improved photo-resist techniques.

CARROLL, CHARLES F.

| | |
|---|---|
| Carnegie Institute of Technology | B.S. Ch. E. 1953 |
| Carnegie Institute of Technology | Post Graduate Work 1956-1958 |

Mr. Carroll is manager of Development Engineering. Prior to joining Bendix, Mr. Carroll was employed by the Molecular Electronics Division of Westinghouse as a senior Design Engineer. He was with Westinghouse from 1959 and worked primarily in the fields of silicon power transistor development and silicon integrated circuitry. He has several patent disclosures in these fields. From 1956 to 1959 he was associated with the Gulf Research Development Company as a project engineer in the Refinery Processes Section. Mr. Carroll served as a Signal Corps officer in the U.S. Army from 1953 until 1956.

EHRENBERG, NATHAN S.

Cooper Union B.S.E.E. 1934

Mr. Ehrenberg is Pilot Line Manager for silicon planar devices. He has performed developmental work on the Bendix silicon high frequency varactor diode program. He was previously associated with the Amperex Electronic Division of North American-Phillips Corporation as Production Manager for germanium diodes. He was associated with Clevite Semiconductor as Manager of Materials Production on silicon and germanium materials. He was also Product Engineer for Western Electric Company and worked on their silicon carbide varistor and quartz crystal devices programs.

HENRY, PETER

Lafayette College 1952 B.S. Biology

Monmouth College 1961 B.S. Chemistry

Mr. Henry is responsible for metallization, dicing, and assembly techniques used for this contract. Since joining Bendix in 1957 he has done development work on germanium power transistors primarily in the areas of surface studies and assembly. More recently he has been concerned with evaporation and assembly of silicon planar power transistors. Prior to joining Bendix he was employed in chemical research work for the Celanese Corp.

HOLLANDER, SIEGFRIED

| | |
|---|---|
| 1st U.S. Army Signal School | Basic Radio Technology 1957 |
| 7th U.S. Army Signal School | High Frequency AM-FM Transceiver 1960<br>Radiological Equipment 1961 |
| Monmouth Technical Institute | Transistor Circuitry 1964 |

Mr. Hollander has been employed by Bendix Semiconductor Division since 1962 as an Applications Technician. His experience includes evaluation and application of various silicon transistor devices. Prior to joining Bendix, Mr. Hollander served in the U.S. Army as communication N.C.O. His work included Third Echelon AM-FM Transceiver And Communication Equipment Repair.

MAKRIS, GEORGE

| | | |
|---|---|---|
| Monmouth College | Physics | 1960--Present |

Mr. Makris is presently attending Monmouth College evening classes working towards completion of requirements for a B.S. in Physics. Since joining Bendix in 1962, he has been engaged in the development and processing of planar epitaxial silicon transistors and integrated circuits. With respect to this contract, Mr. Makris' duties have involved primarily the diffusion and surface passivation of wafers.

NEWMAN, HYMAN

| | |
|---|---|
| Newark College of Engineering | B.S.E.E. 1959 |
| Newark College of Engineering | M.S.E.E. 1962 |

Mr. Newman is Chief Engineer, and is responsibile for the Research and Development Department, Applications Engineering Department, and Mechanical Engineering Department, testing and evaluating semiconductor products, electrical test specifications, development of transistor applications and field engineering. He joined the Bendix Corporation in 1957 as an engineer in charge of testing and evaluation of silicon power rectifiers, determination of ratings and specifications, and correlation of special transistor circuit information. From 1952 to 1957, Mr. Newman worked as an electronics instructor with the Department of the Army Signal School and as a research and development engineering assistant with the responsibility for the evaluation of telephone carrier communication equipment.

WILSON, STANLEY

| | |
|---|---|
| Monmouth College | B.S.E.E. 1963 |
| Newark College of Engineering | Graduate Studies |

Mr. Wilson has been employed by Bendix Semiconductor Division since 1963 as an Applications Engineer. During his employment with Bendix he has worked on various silicon transistor high frequency-high power applications, transistor evaluation, and circuits to extend the range of evaluation of transistor parameters.

WORCHEL, GERALD

| | |
|---|---|
| RCA Institute, NYC | Advanced Electronics 1961 |
| Polytechnic Inst. of Brooklyn | Electrical Engineering and Physics |

Mr. Worchel is responsible for the processing of wafers for this contract. Since joining Bendix in 1964 he has been responsible for diffusion and wet processing studies for advanced devices and integrated circuits. From 1961 to 1964 he was employed by Bell Telephone Laboratories. His work there consisted of the design and development of integrated circuits and ultra high frequency, low power semiconductor devices. While there he was instrumental in the development of a glass isolated integrated logic circuit, a 10 gigacycle switching transistor and a computer diode with a recovery time of less than $10^{-10}$ seconds.

The following engineering personnel have left the employ of the Bendix Semiconductor Division:

R. Reber

C. Rivera

A. Schrob

# APPENDIX

APPENDIX: TESTS

| SYMBOL | CIRCUIT OR EQUIPMENT | MIL STD.-750-METHOD |
|---|---|---|
| $C_{ib}$ | Boonton Electronics RF Admittance Bridge Model 33A-S5 | |
| $C_{ob}$ | Boonton Electronics RF Admittance Bridge Model 33A-S5 | |
| $h_{FE}$ | Baird Atomic -- NC-1 $t_w$ = 300 Sec<br>d = 2% | |
| $h_{fe}$ | General Radio 1607-A Bridge<br>$t_w$ = 300 $\mu$ Sec, d = 2% | |
| $I_{CES}$ | Figure A-1 | 3041 |
| $I_{EBO}$ | Figure A-2 | 3026 |
| $R_{CE(SAT)}$ | Tektronix 575 Scope | |
| $t_{on}$ | Circuit #4 Figure 19 | |
| $t_{off}$ | Circuit #4 Figure 19 | |
| $V_{BE(SAT)}$ | Tektronix 575 Scope | |
| $V_{CBO}$ | Tektronix 575 Scope | |
| $V_{CEO(SUS)}$ | Figure A-3 | |
| $V_{EBO}$ | Tektronix 575 Scope | |
| $\theta_{JC}$ | Bendix TR1-A | |

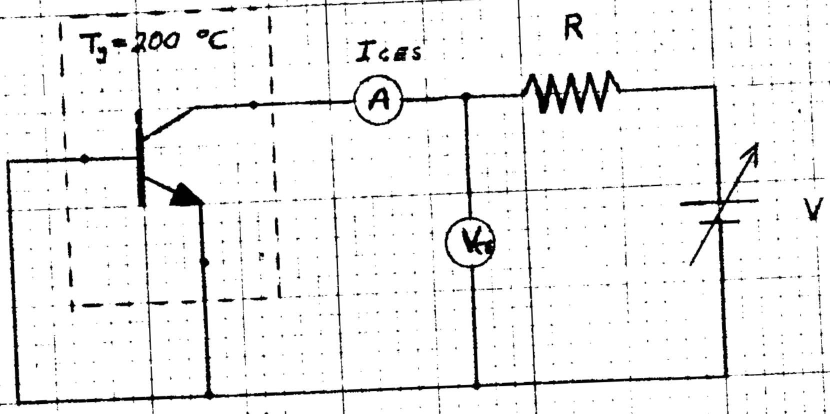



FIGURE A-1 ICES @ TJ = 200 °C TEST CIRCUIT

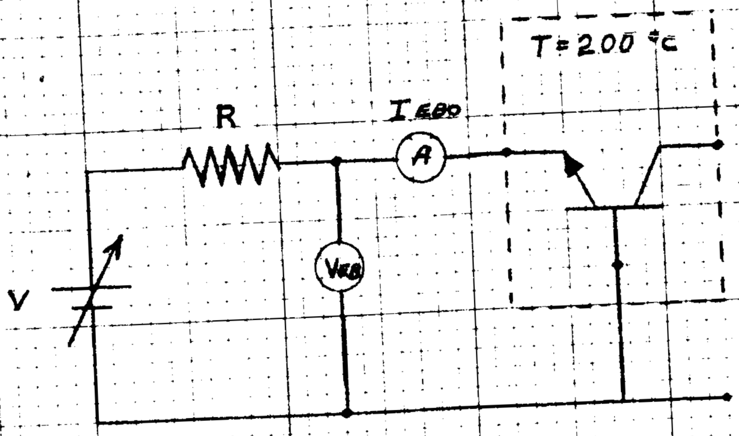



FIGURE A-2 IEBO @ TJ = 200 °C TEST CIRCUIT

10 X 10 PER INCH MADE IN U.S.A.

10 X 10 PER INCH
EUGENE DIETZGEN CO.
MADE IN U. S. A.

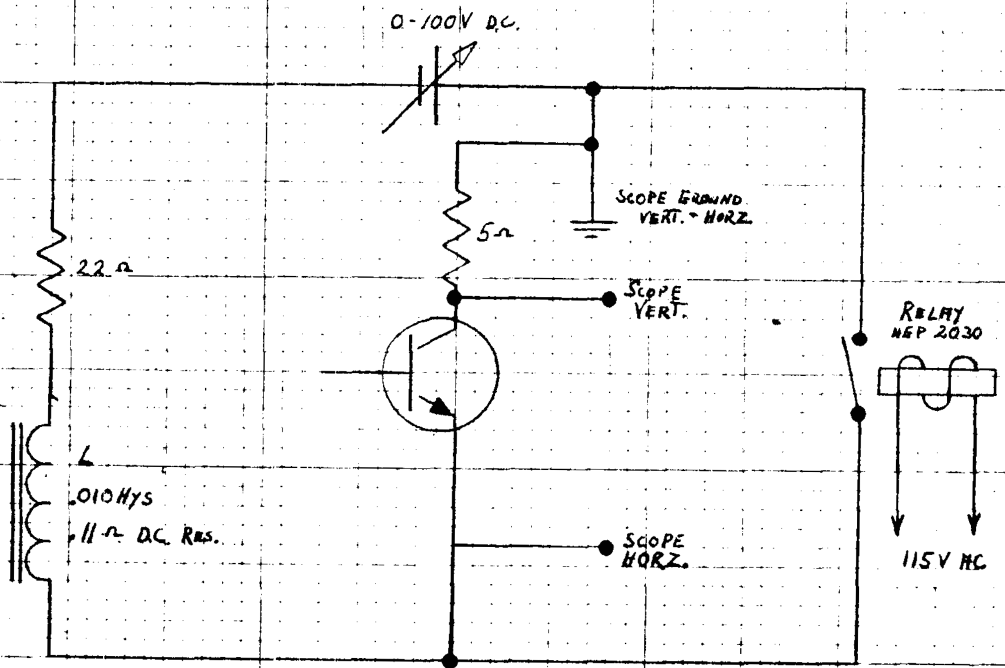



FIGURE A-3 $V_{CEO}(sus)$ TEST CIRCUIT

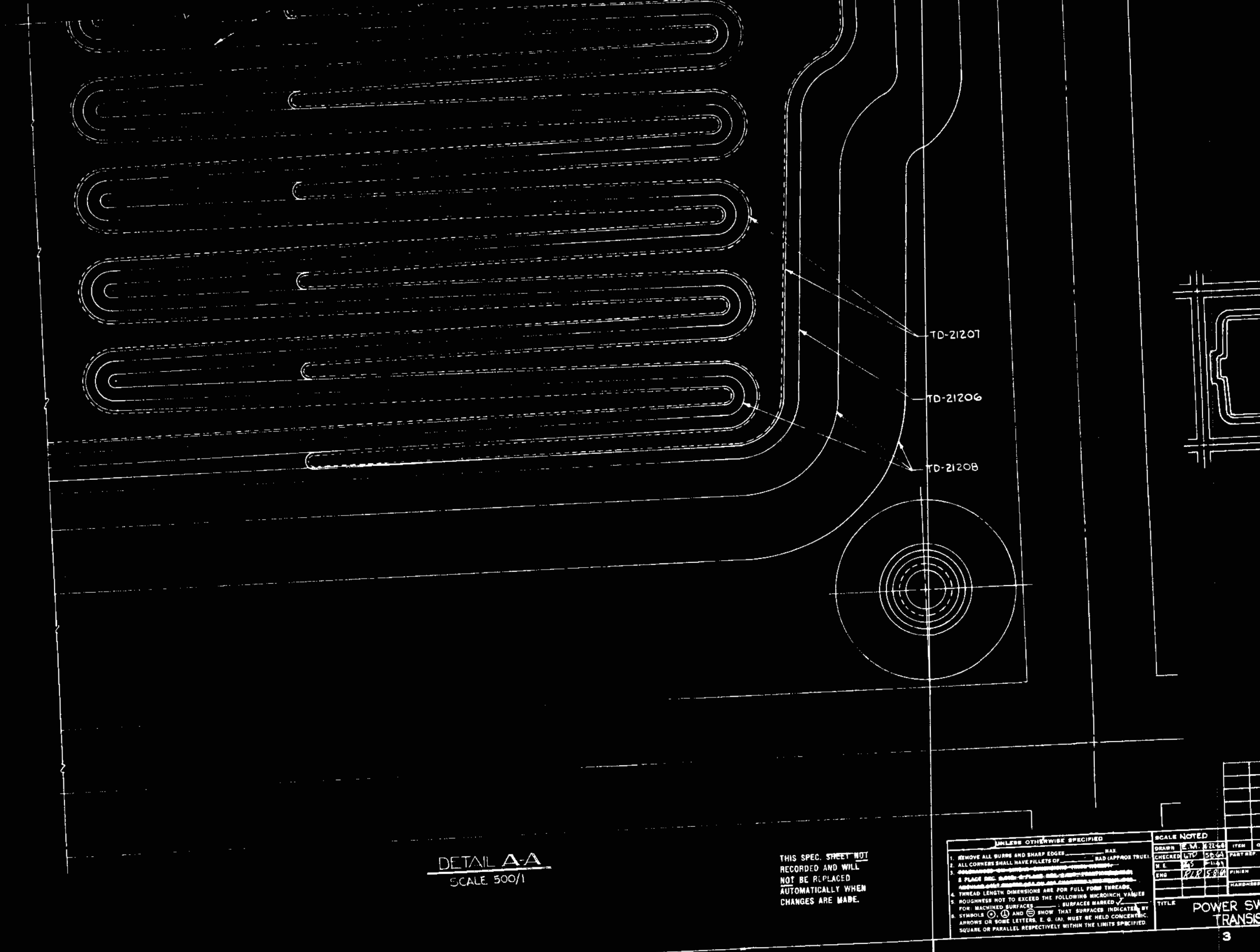
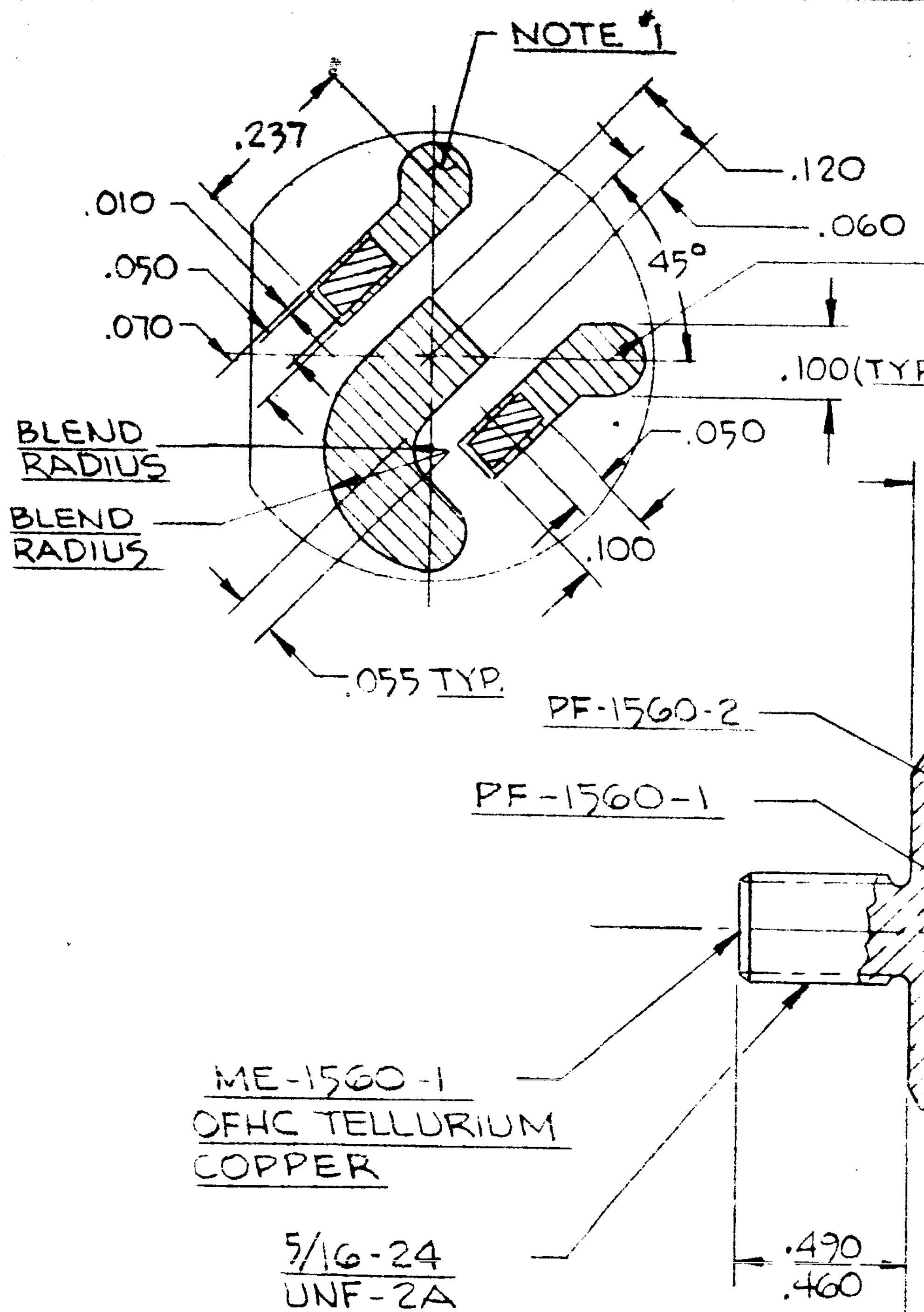



FIGURE 1 -



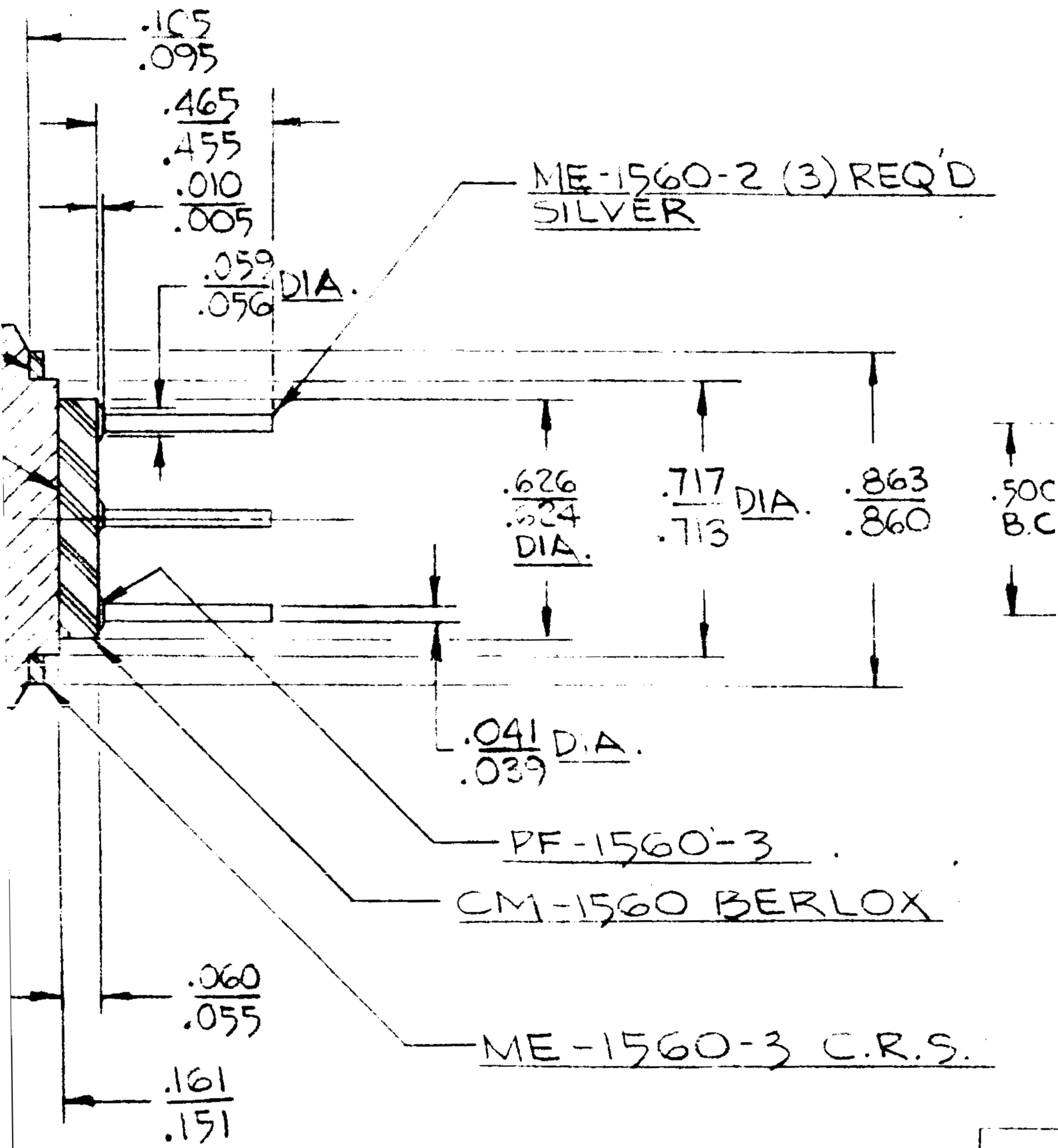

NOTES:

1-METALLIZED AREA .0002 GOLD MININUM

2-FINISH ON STUD TO BE A MININUM OF .0001 GOLD.

FIG. 2

TANGENT RADIUS (TYP)




SC

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A-1560

| 15274 | NBC S.O.# |
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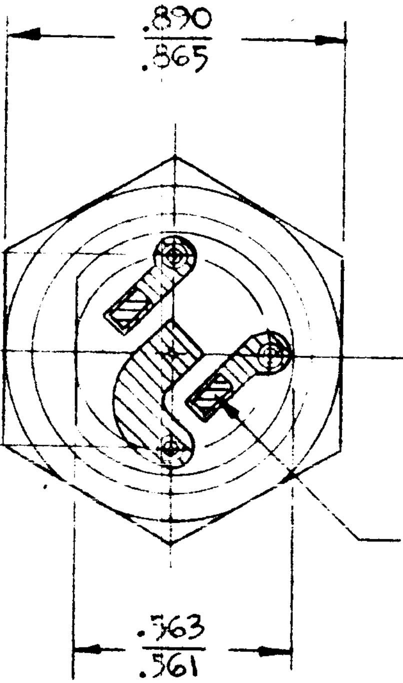
| BENDIX | CUST. |
| ES116 | CUST. DWG. |
| | |




PF-1560-4 AND
ME 1560-4 (PAD)
2 REQ. BRAZED
AS SHOWN

NATIONAL BERYLLIA CORP.

SCALE 2:1

HEX. NAIL HEAD ASS'Y OUTLINE

DRAWING NO. A-1560

ES-119

3

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NOTE:

1. WELD RING MUST BE VACUUM TIGHT, LEAK RATE MUST NOT EXCEED $1\times10^{-8}$ CC/SEC.
2. UNTHREADED PORTION of STUD TO HAVE A DIAM. of .225/.220
3. THIS PART AS RECEIVED MUST PASS HYDROGEN EMBRITTLEMENT TEST AS OUTLINED IN ASTM B152-52
4. STUD MUST WITHSTAND 60 IN-LBS APPLIED RADIALLY AFTER ONE HOUR SOAK @ 450°C.
5. SHADED AREA SHALL BE .0002 MIN. GOLD PLATED ON .0005 TO .0010 MOLY MANGANESE METALLIZED ON Be O
6. .015 THICK SILVER 99.9% PURE BRAZED AS SHOWN.
7. ASSEMBLY SHALL WITHSTAND 500°C IN $N^2$ FOR 5(FIVE) MINUTES WITHOUT EVIDENCE OF BLISTERING, PEELING, CRACKING OR DISCOLORATION.

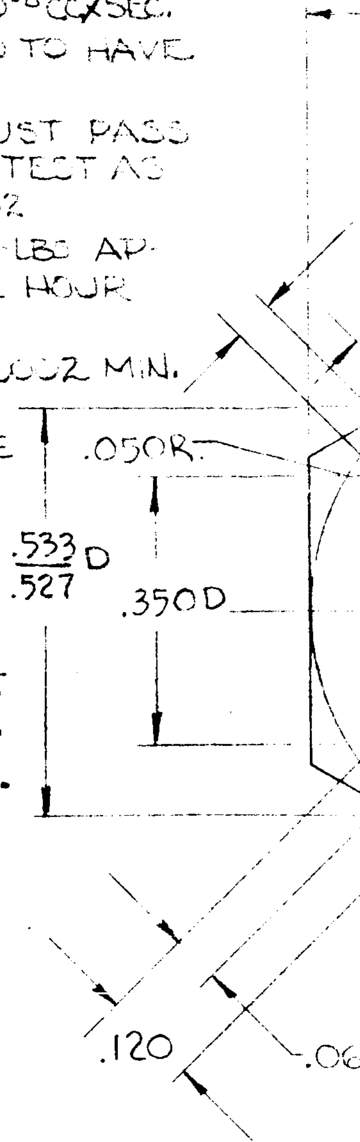
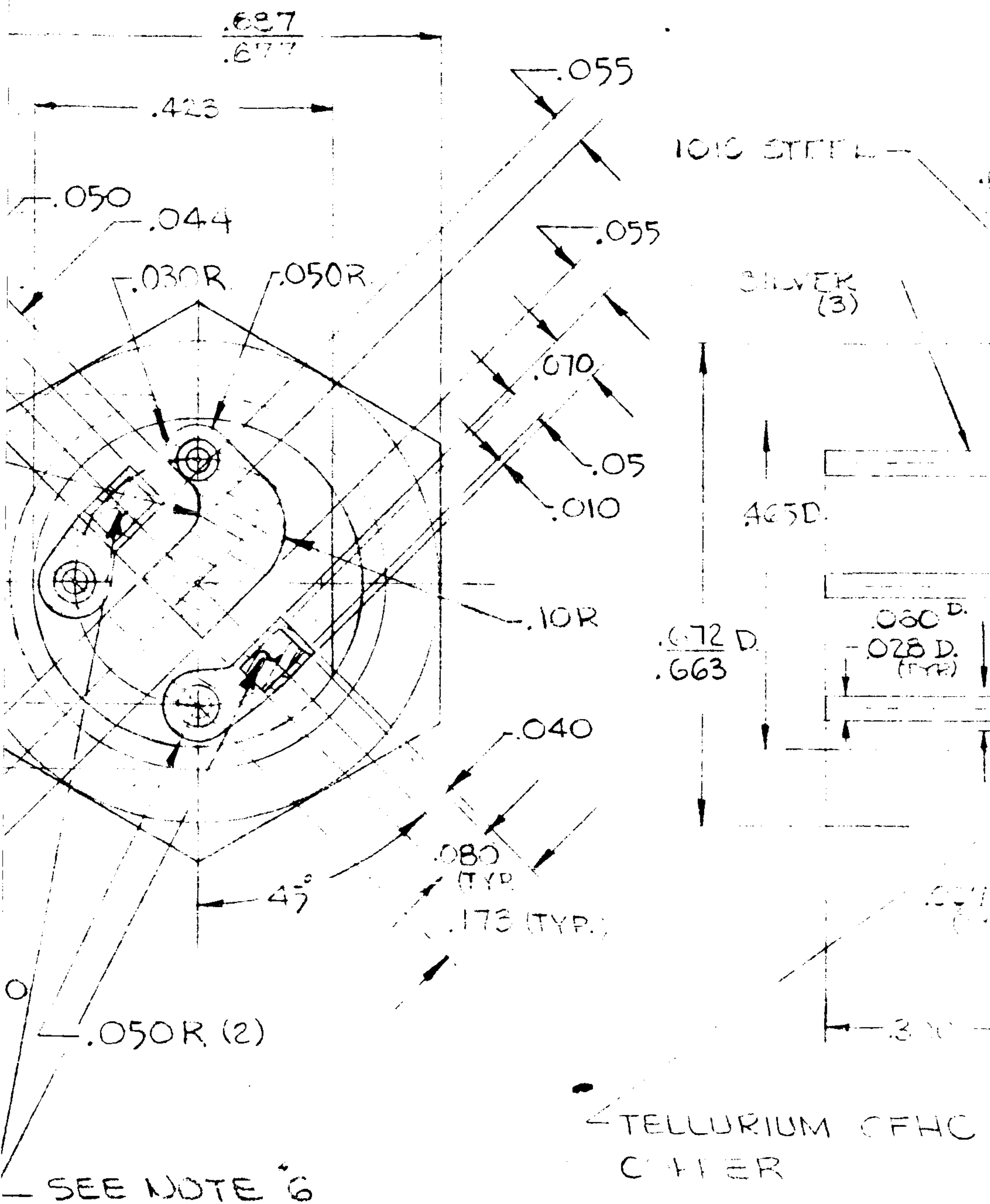



FIG. 3




| UNLESS OTHERWISE SPECIFIED |
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| 1. REMOVE ALL BURRS AND SHARP EDGES ______ MAX. |
| 2. ALL CORNERS SHALL HAVE FILLETS OF ______ RAD (APPROX TRUE). |
| 3. TOLERANCES ON LINEAR DIMENSIONS (INCL HOLES): 2 PLACE DEC. ±.010; 3 PLACE DEC. ±.005; FRACTIONS ±.015; ANGULAR ±½° EXCEPT ±5° ON 45° CHAMFERS LESS THAN .040 |
| 4. THREAD LENGTH DIMENSIONS ARE FOR FULL FORM THREADS. |
| 5. ROUGHNESS NOT TO EXCEED THE FOLLOWING MICROINCH VALUES FOR: MACHINED SURFACES ______ ; SURFACES MARKED √ ______ . |
| 6. SYMBOLS ⊙, ⊥ AND ⊜ SHOW THAT SURFACES INDICATED BY ARROWS OR SOME LETTERS, E. G. (A), MUST BE HELD CONCENTRIC, SQUARE OR PARALLEL RESPECTIVELY WITHIN THE LIMITS SPECIFIED. |

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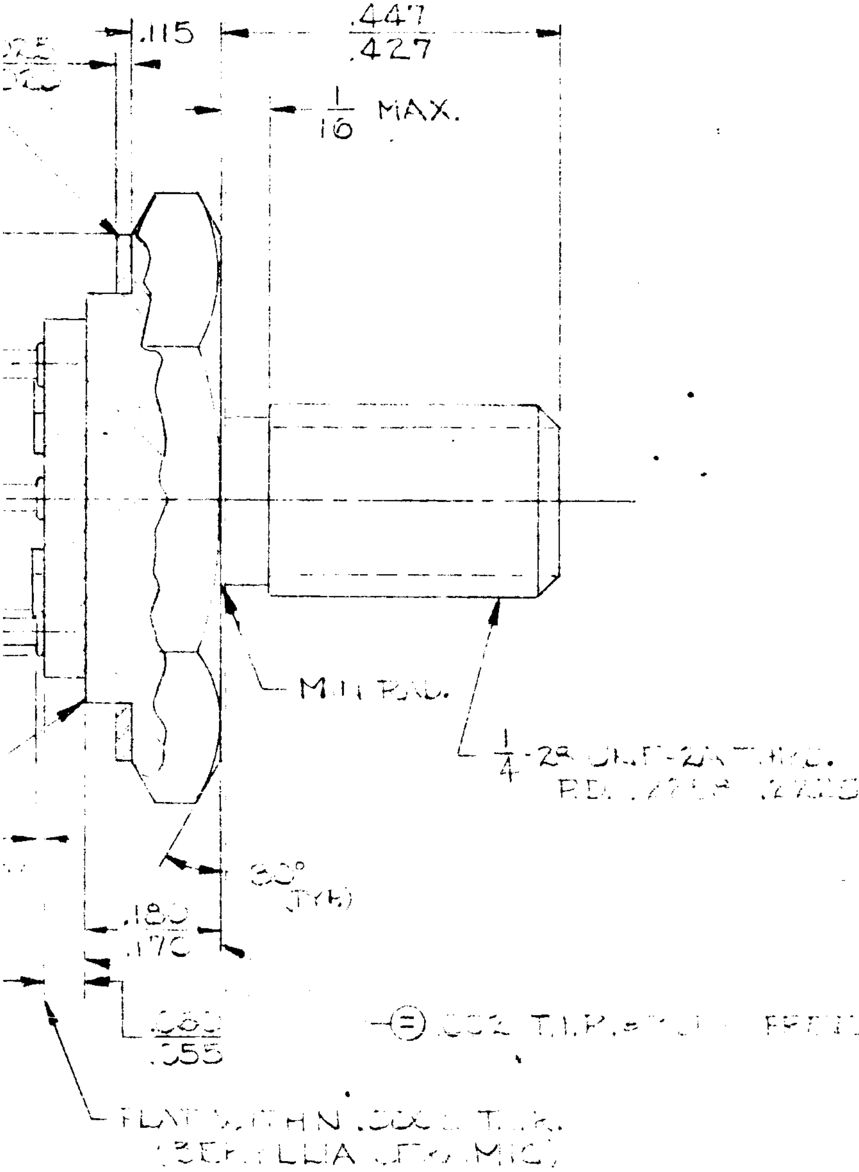


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2. STUD MUST WITHSTAND 25 IN.LBS. APPLIED RADI
3. PLATING AS OUTLINED IN FP-6, FP-6A & FP-32, FP
4. SHADED AREA SHALL BE .0002 MIN. GOLD PLATED O

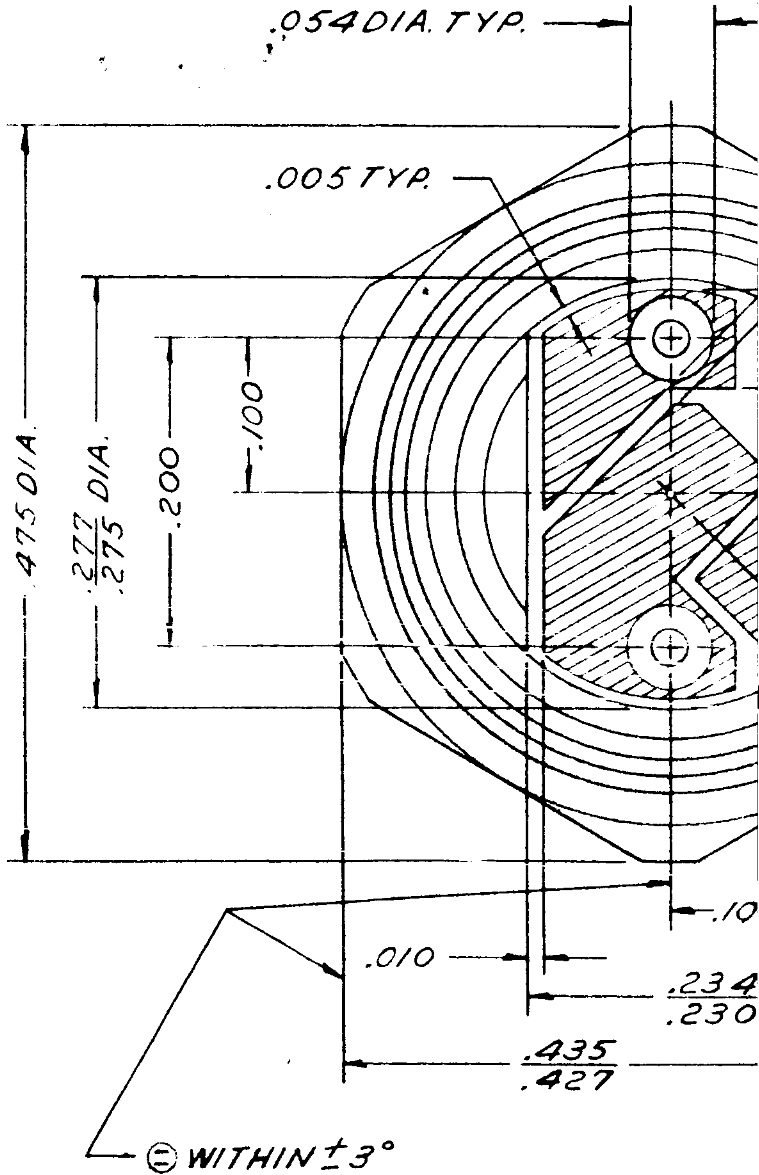
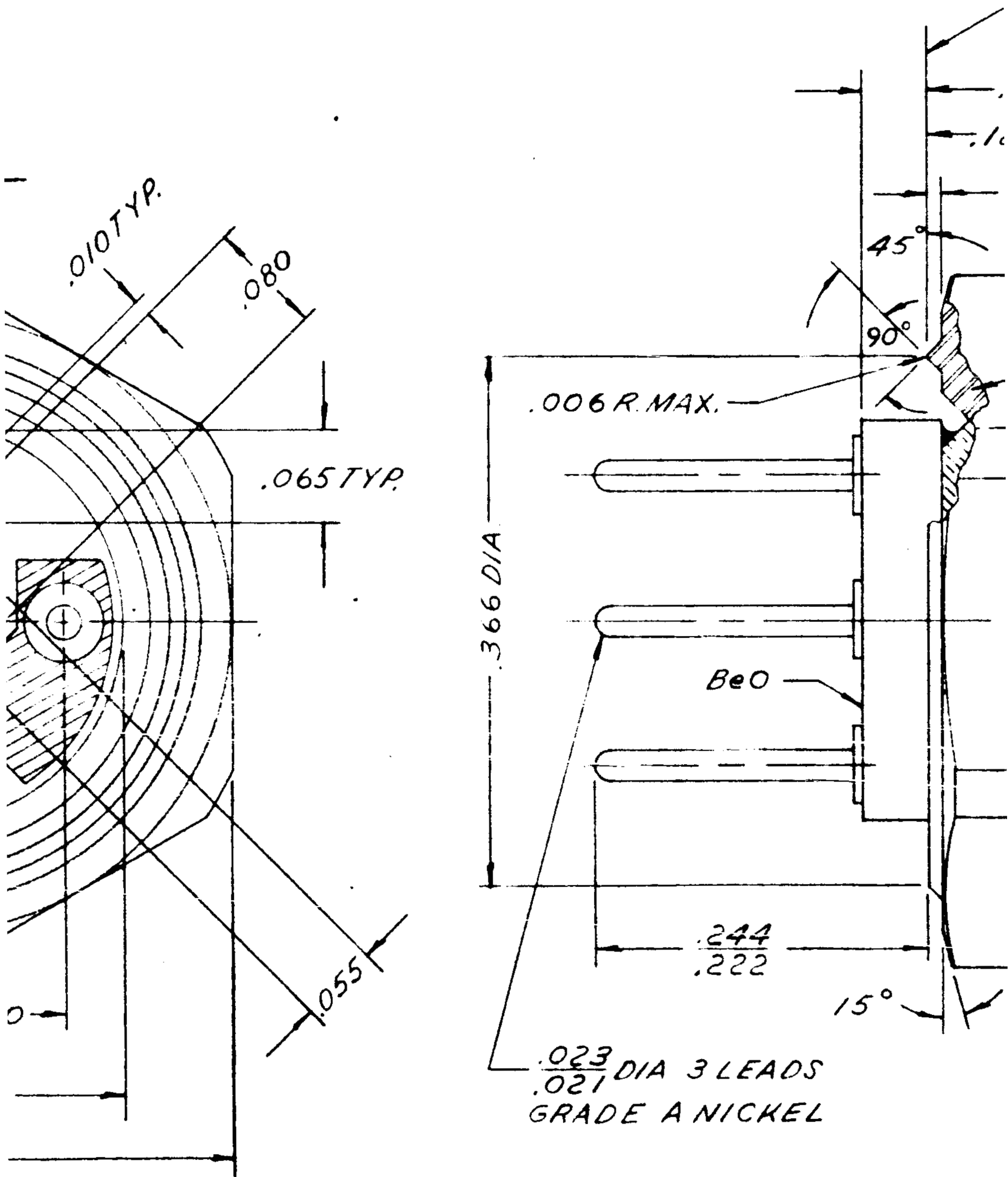



FIG. 4

T NOT EXCEED 1X10⁻⁶ CC/SEC.
ALLY AFTER ONE HOUR SOAK @ 450°C
-32A
N .0005 TO .0010 MOLY MANGANESE METALLIZED ON




| UNLESS OTHERWISE SPECIFIED |
|---|
| 1. REMOVE ALL BURRS AND SHARP EDGES ________ MAX. |
| 2. ALL CORNERS SHALL HAVE FILLETS OF ________ RAD (APPROX TRUE). |
| 3. TOLERANCES ON LINEAR DIMENSIONS (INCL HOLES): 2 PLACE DEC. ±.010; 3 PLACE DEC. ±.005; FRACTIONS ±.015; ANGULAR ±½° EXCEPT ±5° ON 45° CHAMFERS LESS THAN .040 |
| 4. THREAD LENGTH DIMENSIONS ARE FOR FULL FORM THREADS. |
| 5. ROUGHNESS NOT TO EXCEED THE FOLLOWING MICROINCH VALUES FOR: MACHINED SURFACES ______ : SURFACES MARKED √ ______ . |
| 6. SYMBOLS ⊙, ⊥ AND ⊜ SHOW THAT SURFACES INDICATED BY ARROWS OR SOME LETTERS, E. G. (A), MUST BE HELD CONCENTRIC, SQUARE OR PARALLEL RESPECTIVELY WITHIN THE LIMITS SPECIFIED. |

| SCALE | 8:1 | |
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| CHECKED | WIP | 7/12 |
| M. E. | | |
| ENG. | | |
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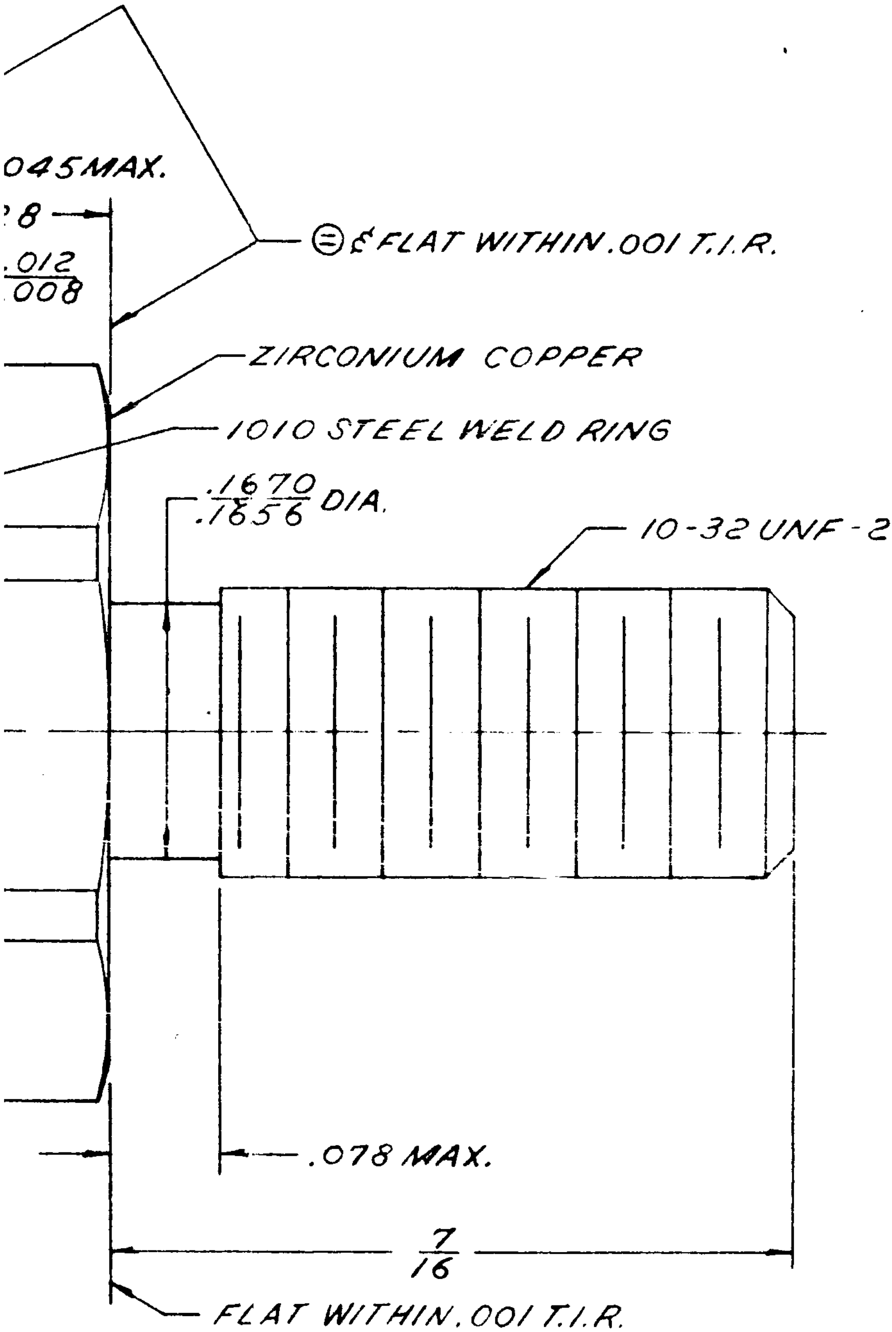


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NOTES:
1. USE NO SULFUR BEARING LUBRICANT IN FABRICAT
2. ALL SEALS SHALL MEET THE REQUIREMENTS O
3. PLATE AS PER FP-6, FP-6A & FP-32, FP-32A

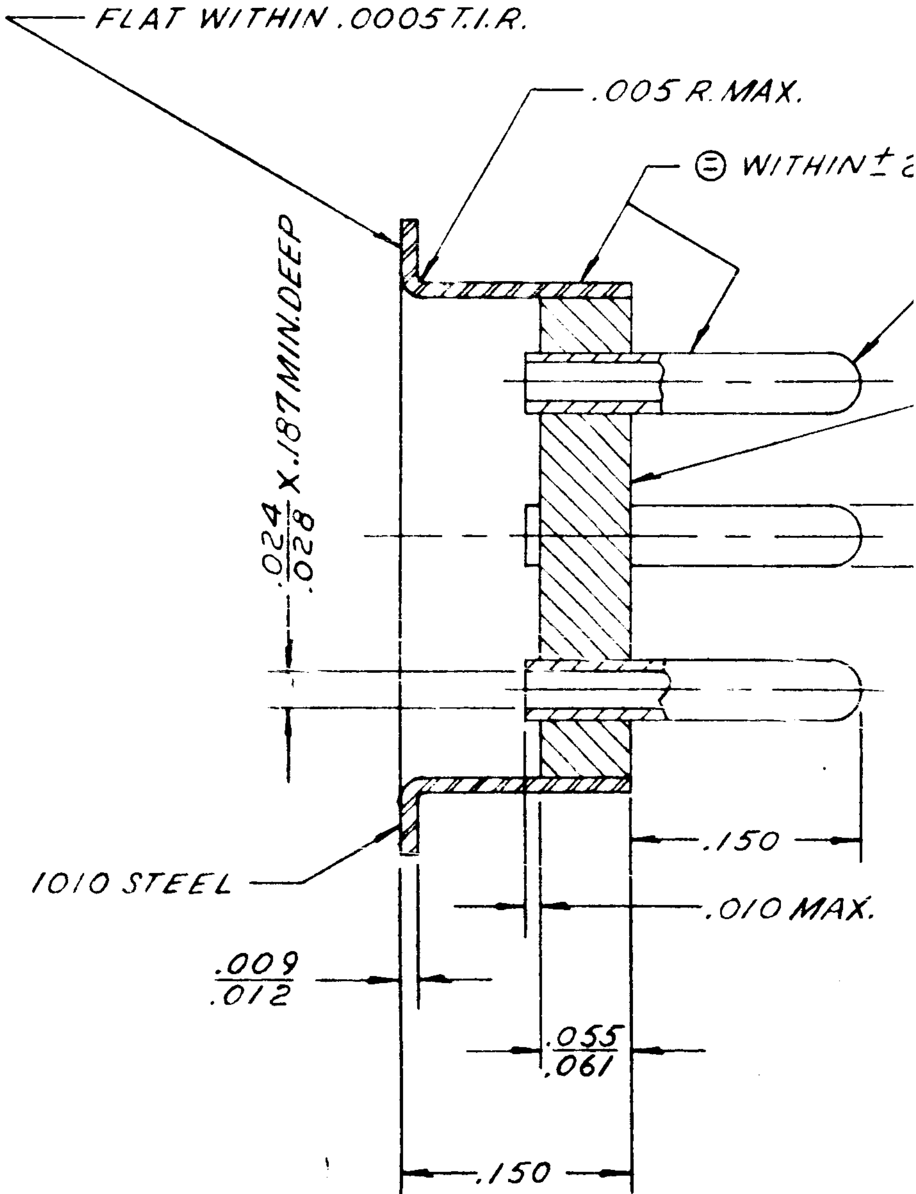


FIG. 5

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TION
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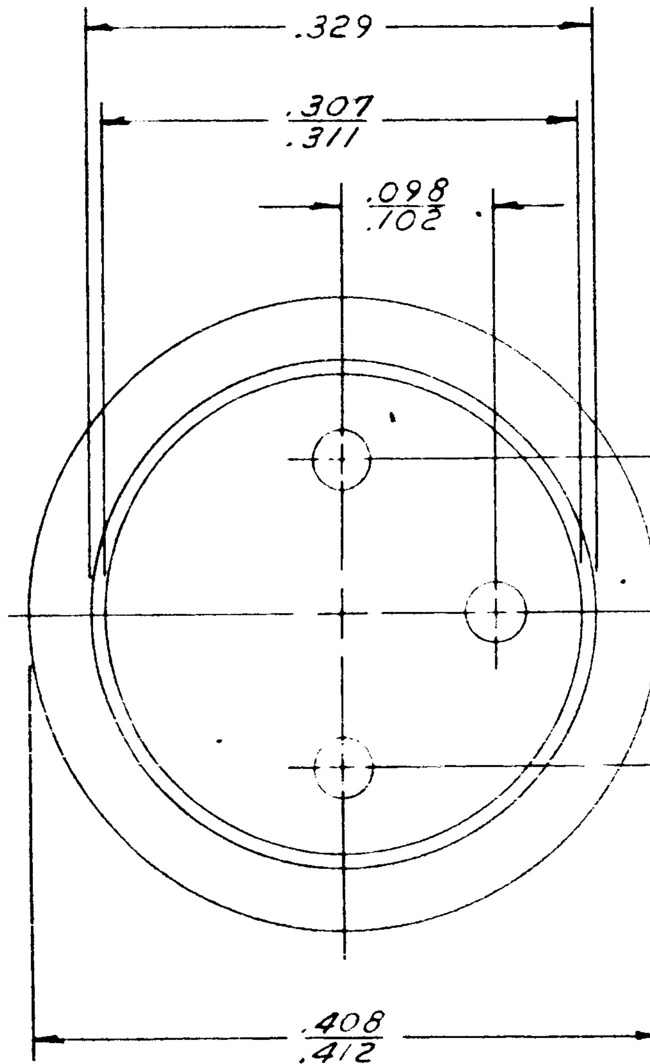
GRADE A NICKEL

ALUMINA

.038
.042




| UNLESS OTHERWISE SPECIFIED |
|---|
| 1. REMOVE ALL BURRS AND SHARP EDGES ______ MAX. |
| 2. ALL CORNERS SHALL HAVE FILLETS OF ______ RAD (APPROX TRUE). |
| 3. TOLERANCES ON LINEAR DIMENSIONS (INCL HOLES): 2 PLACE DEC. ±.010; 3 PLACE DEC. ±.005; FRACTIONS ±.015; ANGULAR ±½° EXCEPT ±5° ON 45° CHAMFERS LESS THAN .040 |
| 4. THREAD LENGTH DIMENSIONS ARE FOR FULL FORM THREADS. |
| 5. ROUGHNESS NOT TO EXCEED THE FOLLOWING MICROINCH VALUES FOR: MACHINED SURFACES ______ : SURFACES MARKED √ ______ . |
| 6. SYMBOLS ⊙, ⊥ AND ⊜ SHOW THAT SURFACES INDICATED BY ARROWS OR SOME LETTERS, E. G. (A), MUST BE HELD CONCENTRIC, SQUARE OR PARALLEL RESPECTIVELY WITHIN THE LIMITS SPECIFIED. |

| SCALE | 8. |
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| DRAWN | GLr |
| CHECKED | WP |
| M. E. | |
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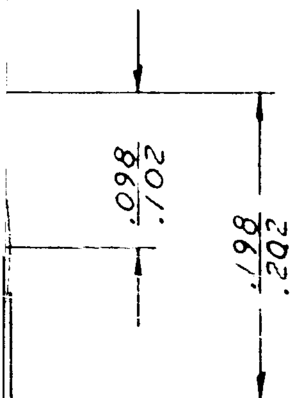


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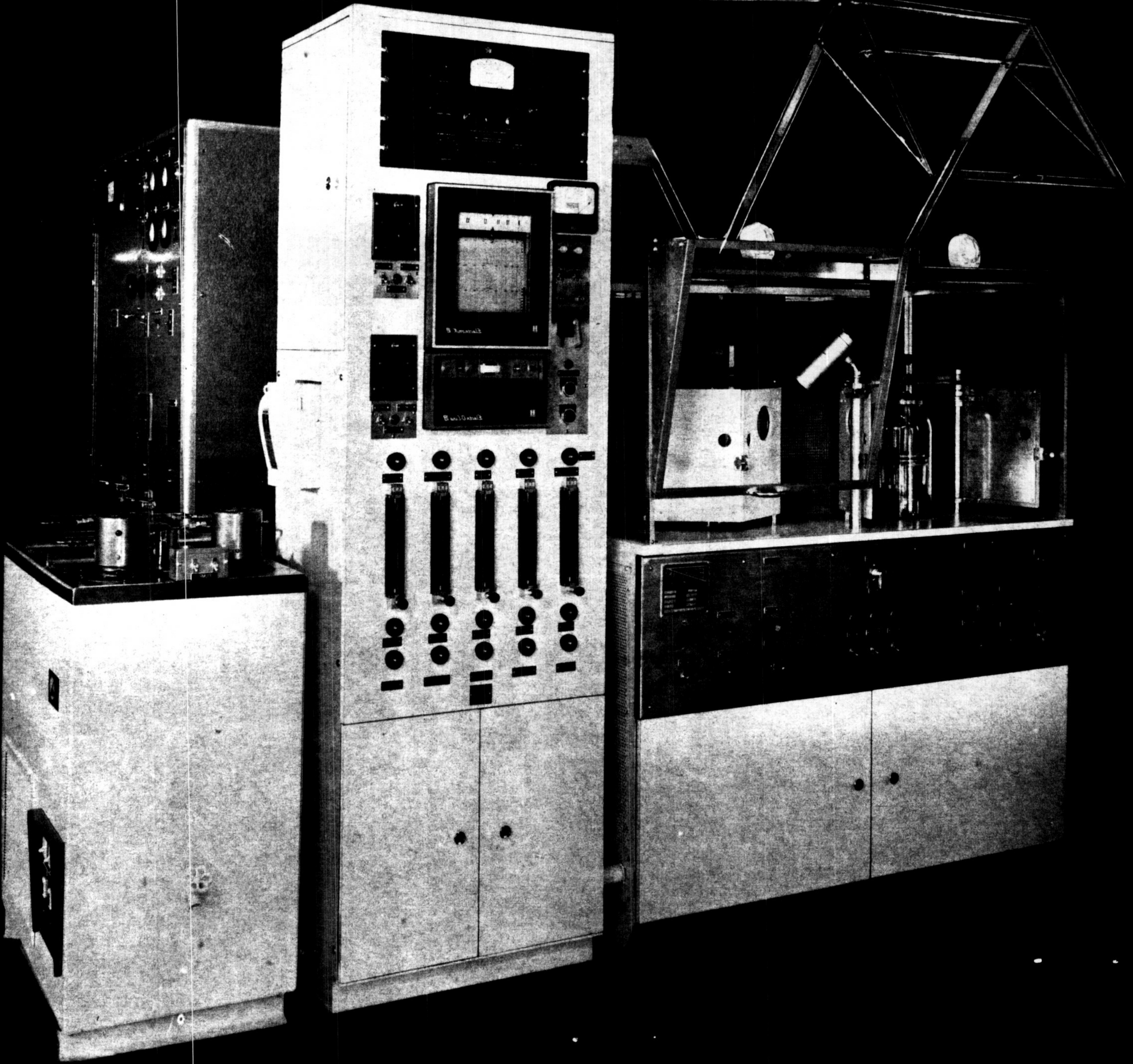


FIGURE 6 -- NEWLY INSTALLED EPITAXIAL SYSTEM

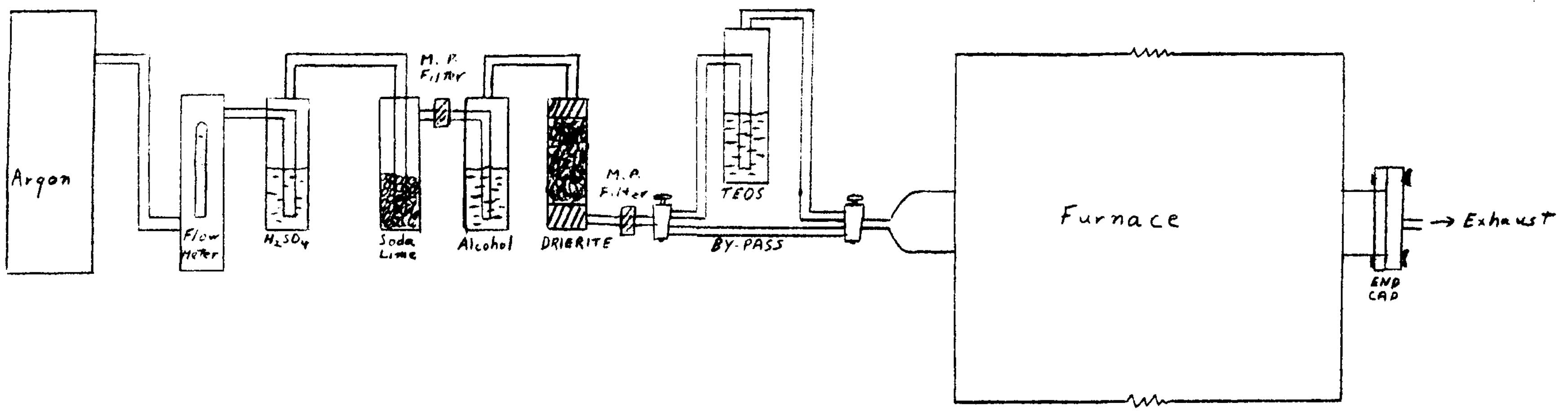



Figure 2. PYROLYTIC OXIDE FURNACE

2/3/65

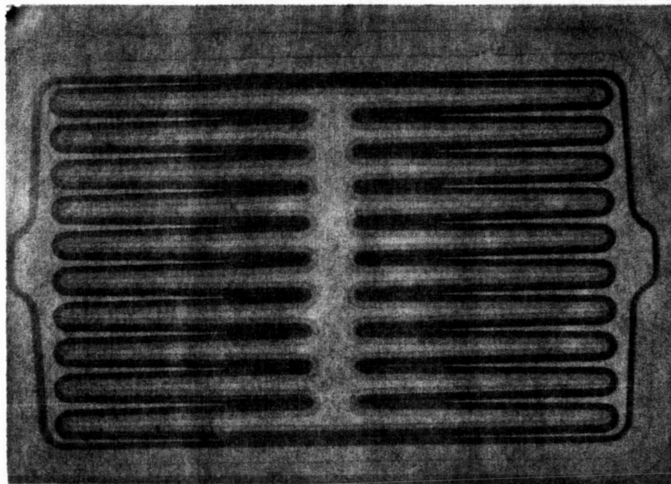


FIGURE 8. The above photo-micrograph is a 60X magnification of the new goemetry through the contact opening stage. Emitter and Contact cut operations have been performed.

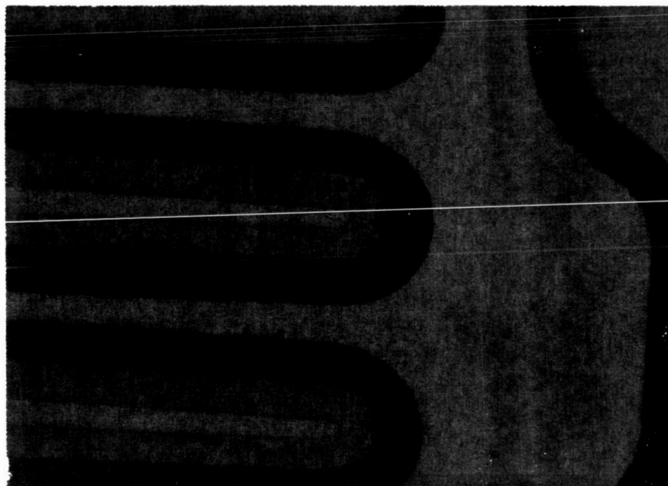


FIGURE 9. A 480X magnification of finger edge on Figure I geometry. The tightest line spacing is 0.1 mil.

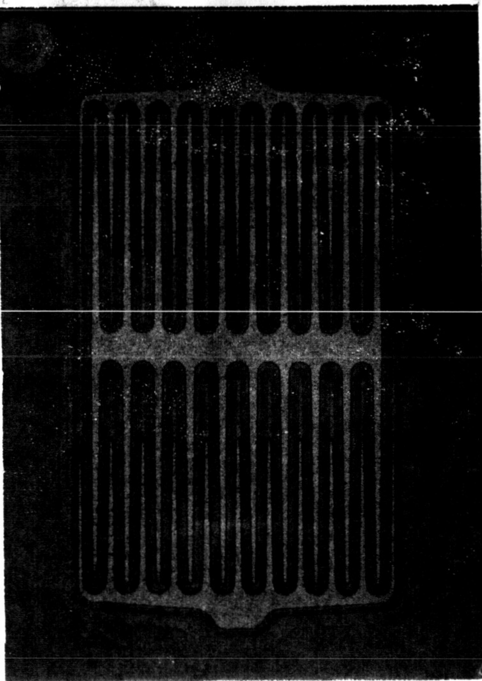


Fig. 10A -- 30,000 $A^{o}$ of Aluminum KTFR, Etch off half of aluminum, remove resist and re-KTFR, etch remaining aluminum at 60X

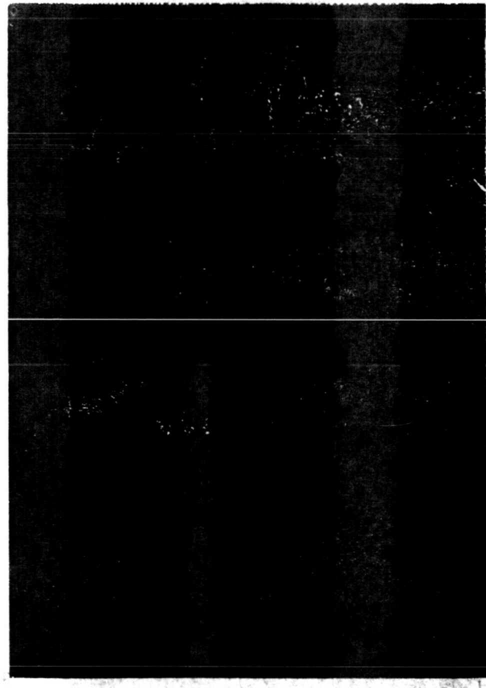


Fig. 10B -- 30,000 $A^{o}$ of Aluminum KTFR, etch off half of aluminum, remove resist and re-KTFR, etch remaining aluminum at 400X

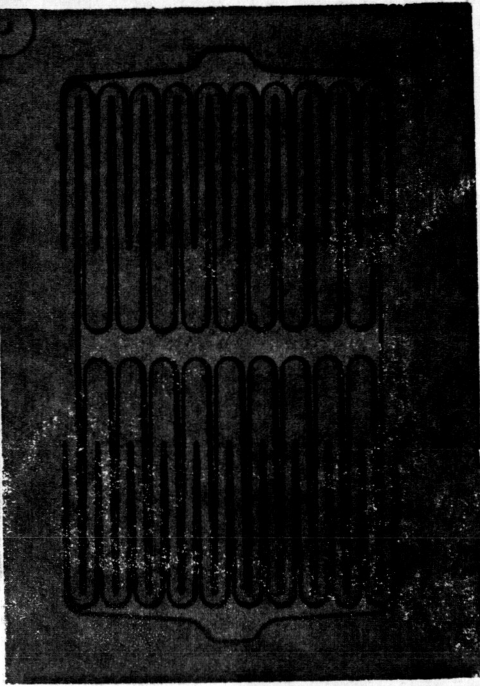


Fig. 10C -- 50,000 $A^{o}$ of Aluminum Two 25,000 $A^{o}$ aluminum depositions and two subsequent etches at 60X

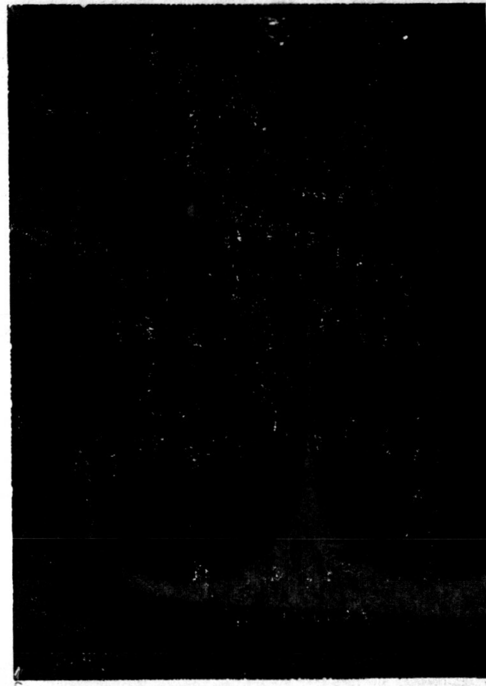


Fig. 10D -- 50,000 $A^{o}$ of Aluminum Two 25,000 $A^{o}$ aluminum depositions and two subsequent etches at 300X

DOUBLE SHOT ALUMINUM

HEAVY ALUMINUM METALLIZATION EXPERIMENTS

FIGURE 10

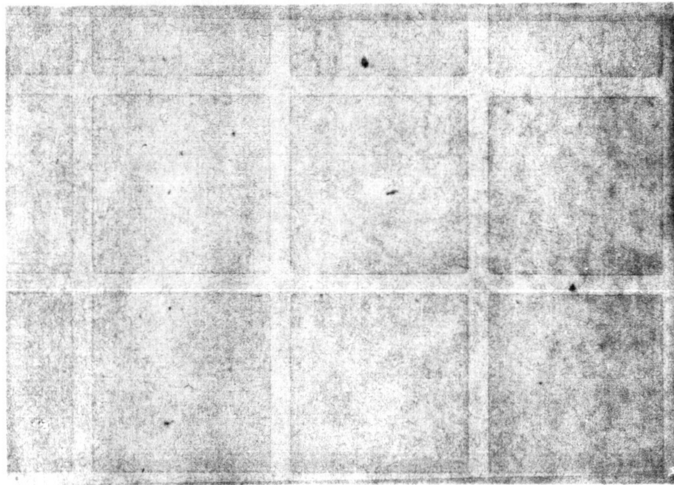


FIGURE 11A

"BEFORE"

SI $O_2$ MASKED WITH KTFR AND ETCHED WITH BUFFERED HF

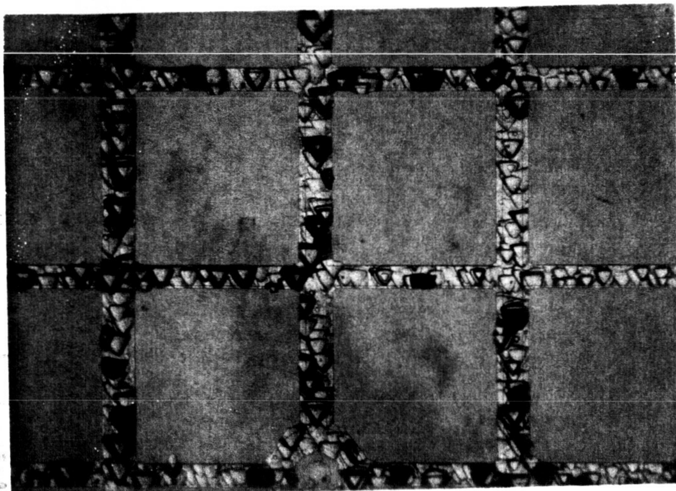


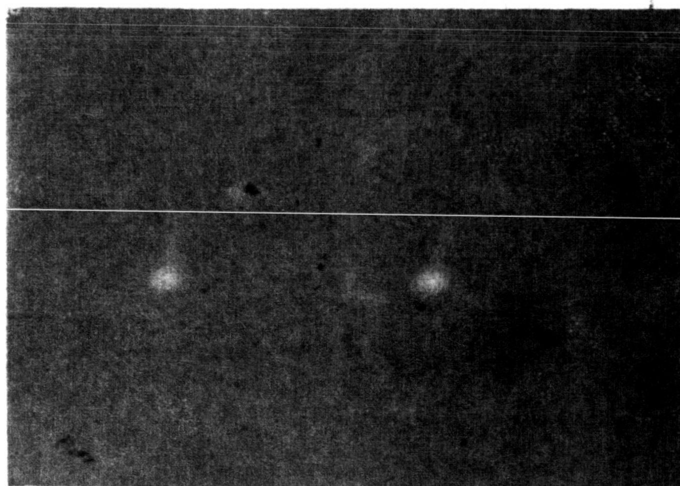
FIGURE 11B

"AFTER"

SAME SAMPLE AS 3A AFTER ADDITIONAL CHLORINE ETCH

FIGURE 11

12a. Pyrolytic oxide deposited in old system. Dark spots represent pinholes. 200X



12b. Pyrolytic oxide deposited in new system. Dark spots represent pinholes. 200X

FIGURE 12

Chlorine Etch Test of Pyrolytic Oxide

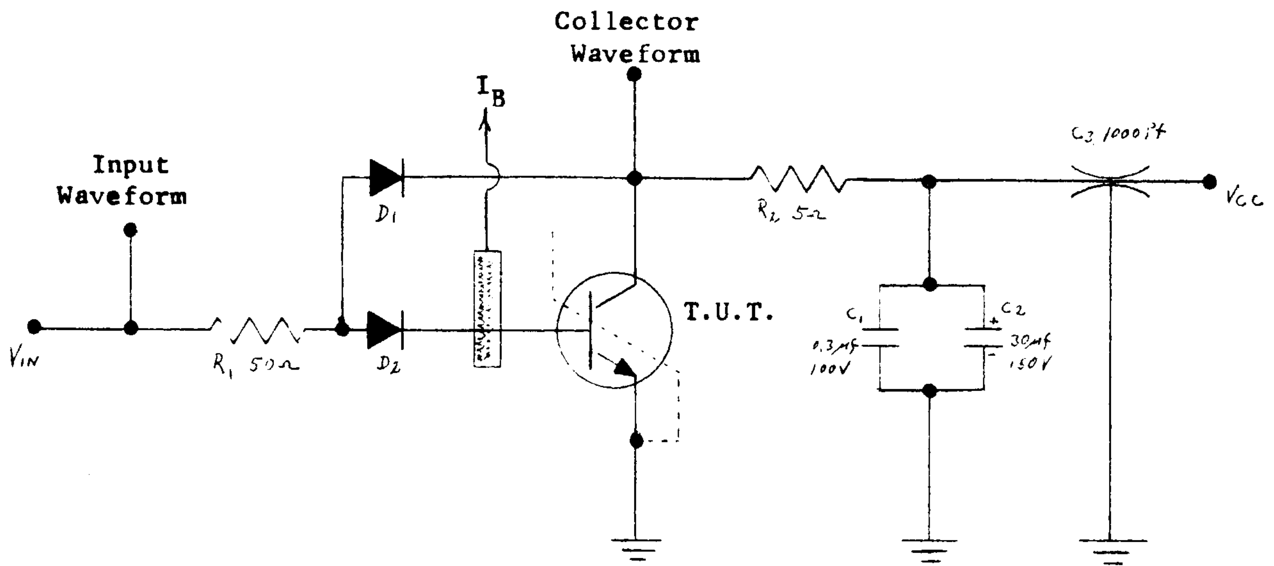



**FIGURE 13** **CIRCUIT NO . 1 ORIGINAL "$t_{on}$" TEST CIRCUIT**

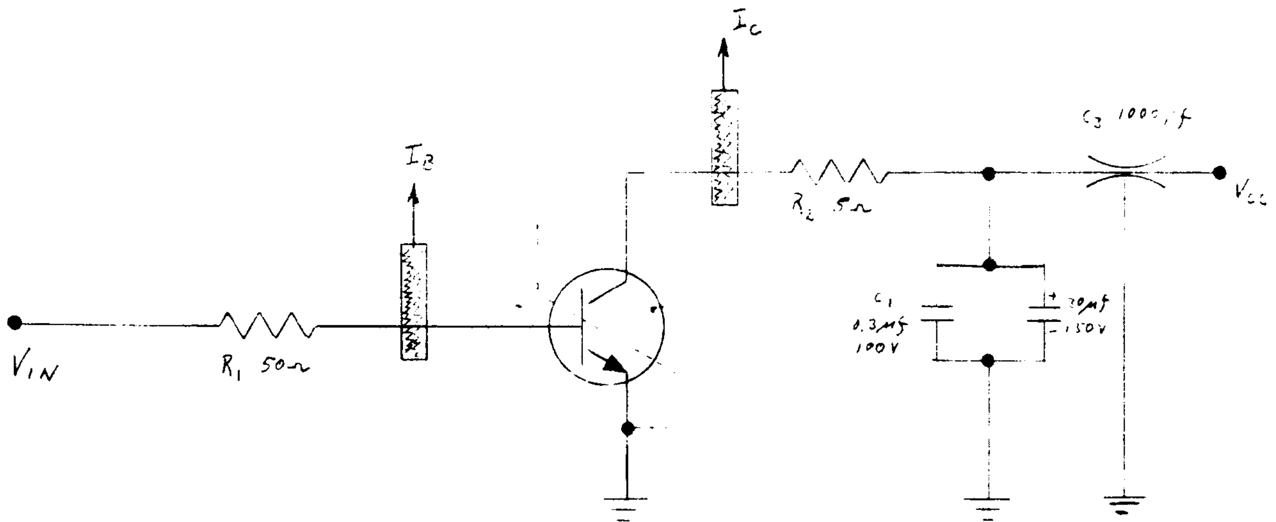



**FIGURE 14** **CIRCUIT NO. 1. ORIGINAL "$t_{on}$" TEST CIRCUIT WITH $D_1$ AND $D_2$ REMOVED**

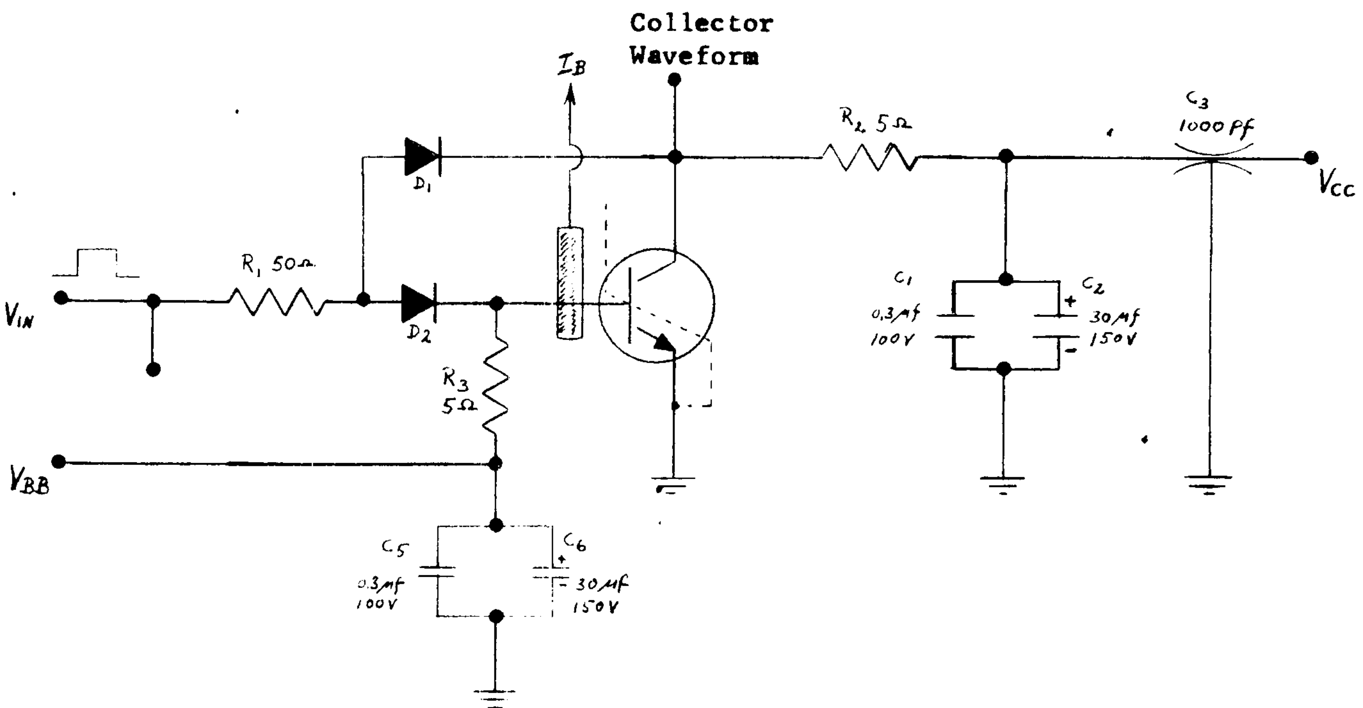



FIGURE 15 CIRCUIT NO. 2, ORIGINAL "$t_{off}$" TEST CIRCUIT

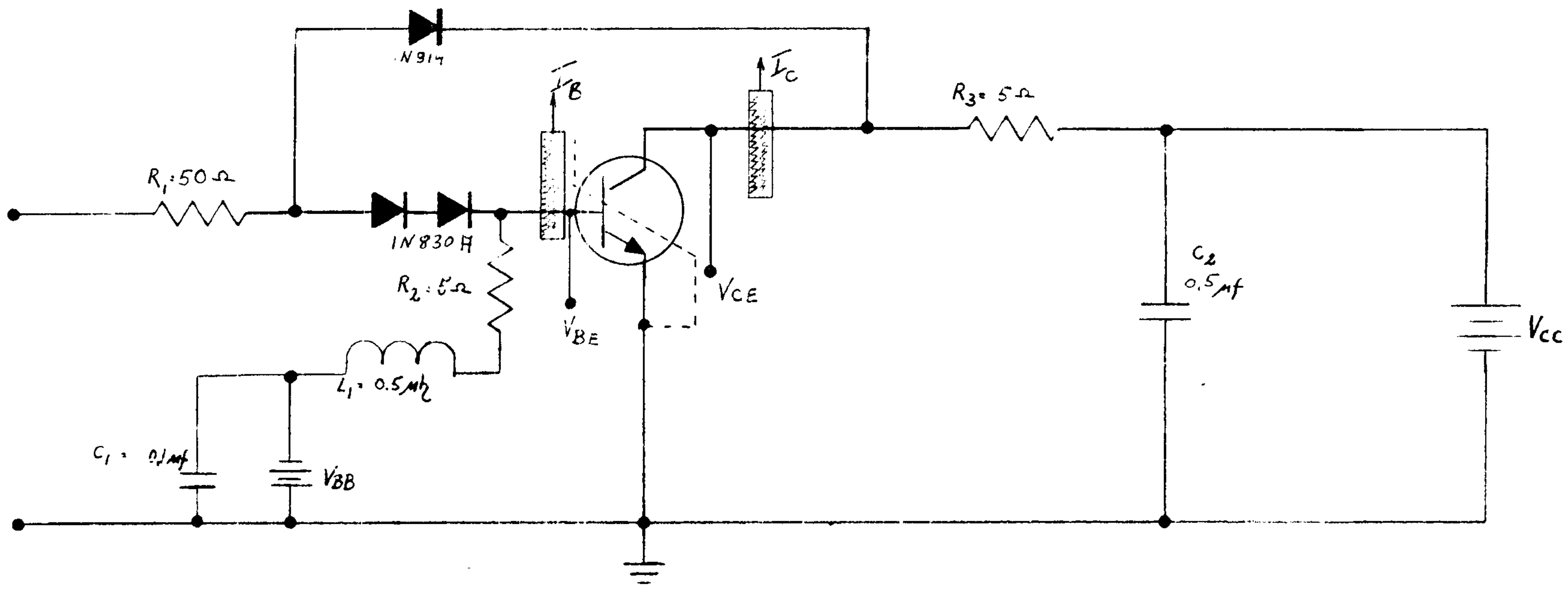



FIGURE 16 SWITCHING CIRCUIT NO. 3 ($t_{on}$ & $t_{off}$)

NASA SWITCHING CIRCUIT No 3 PHOTOGRAPH

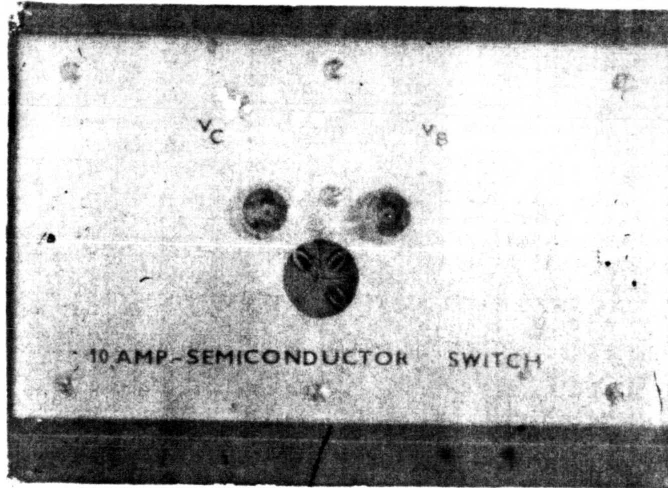
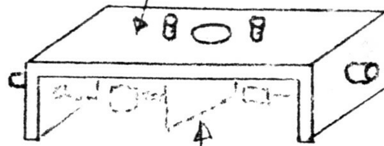



FIGURE 17
TOP VIEW



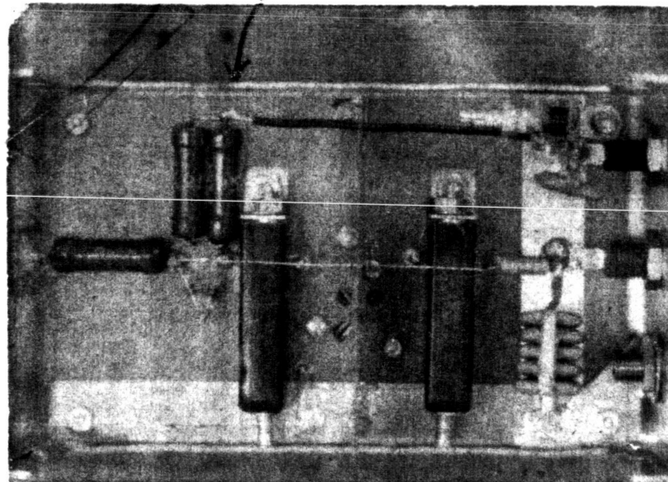
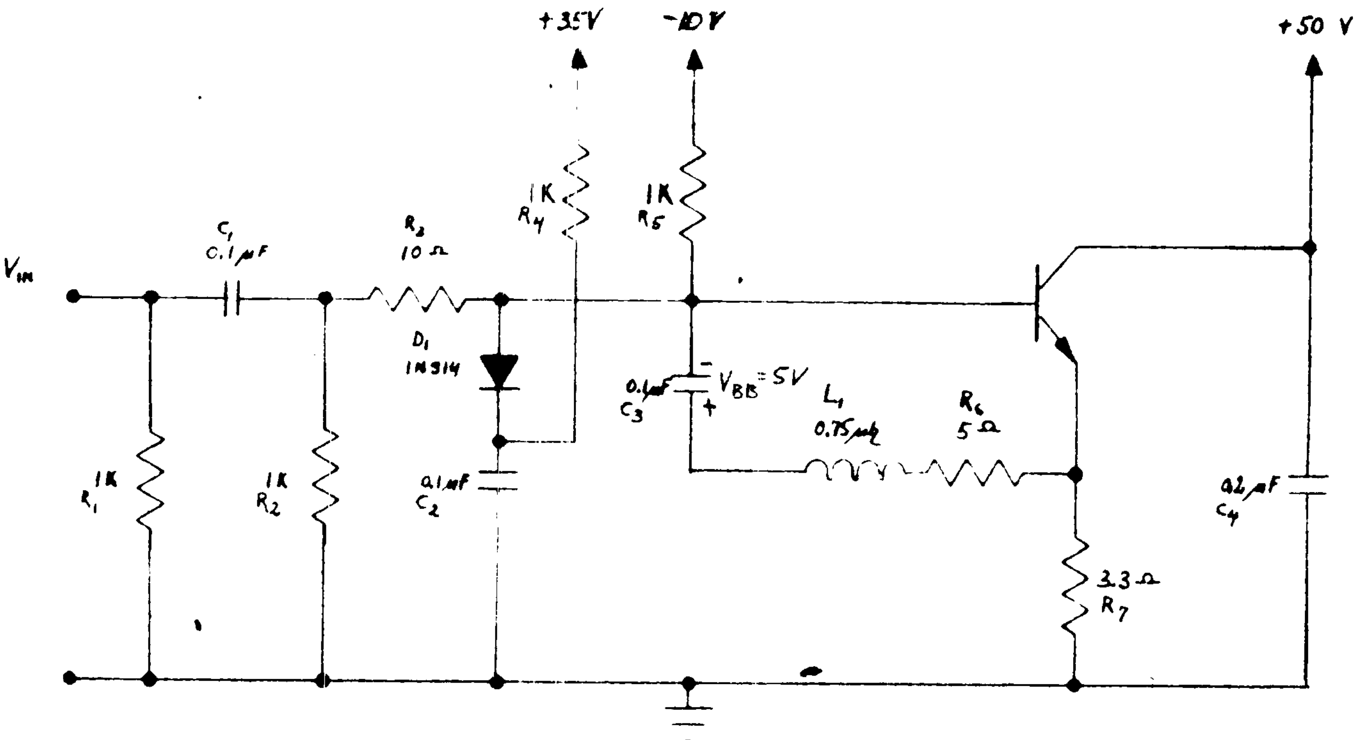


FIGURE 18 BOTTOM VIEW (COVER REMOVED)




COMMON COLLECTOR, SWITCHING CIRCUIT

FIG. 19

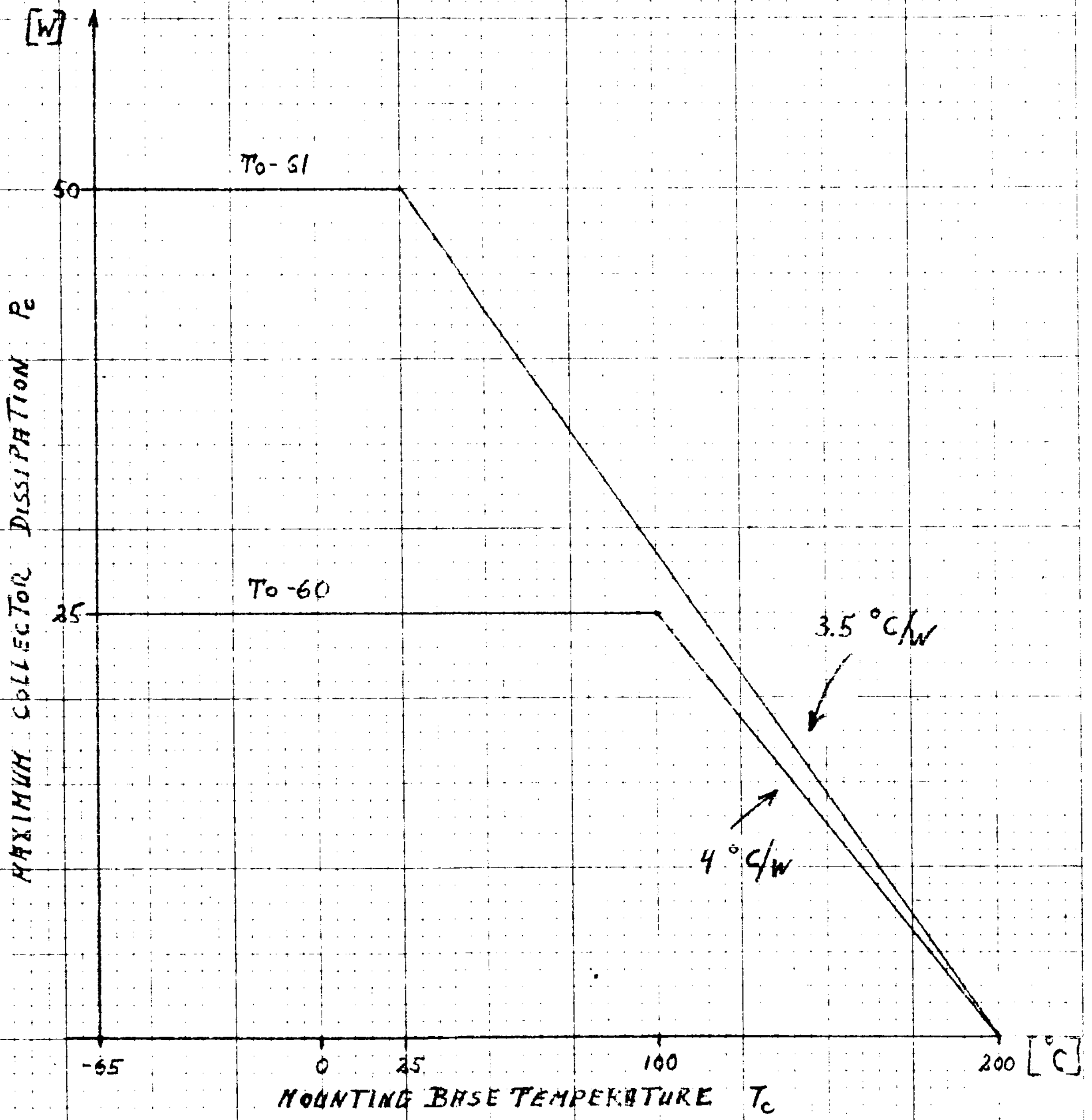



FIGURE 20

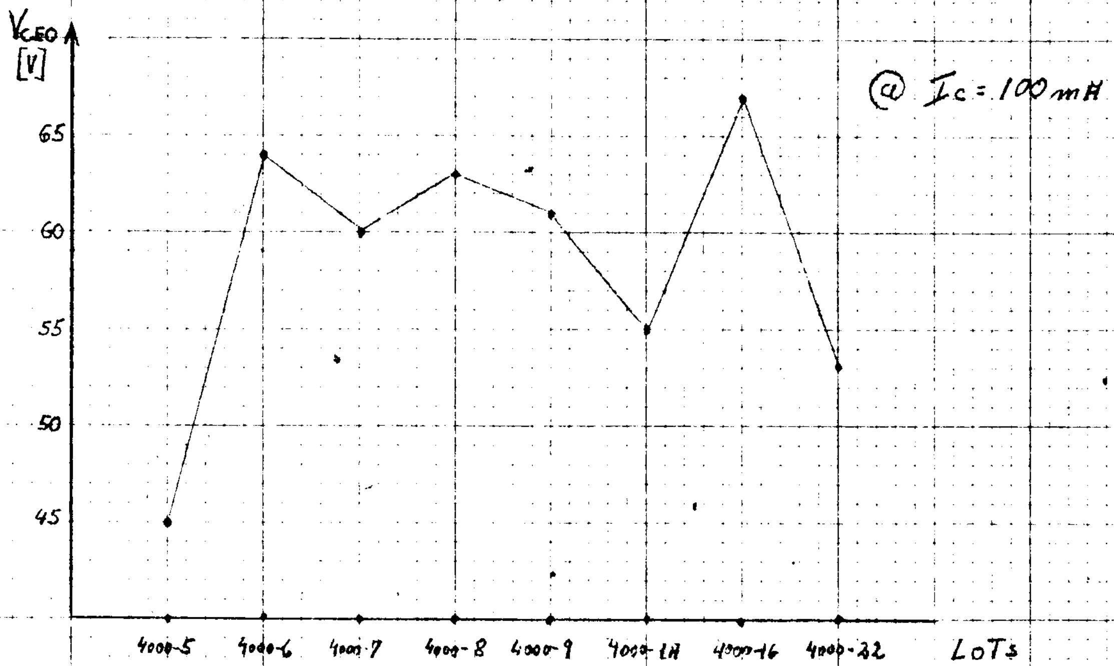



FIGURE 21

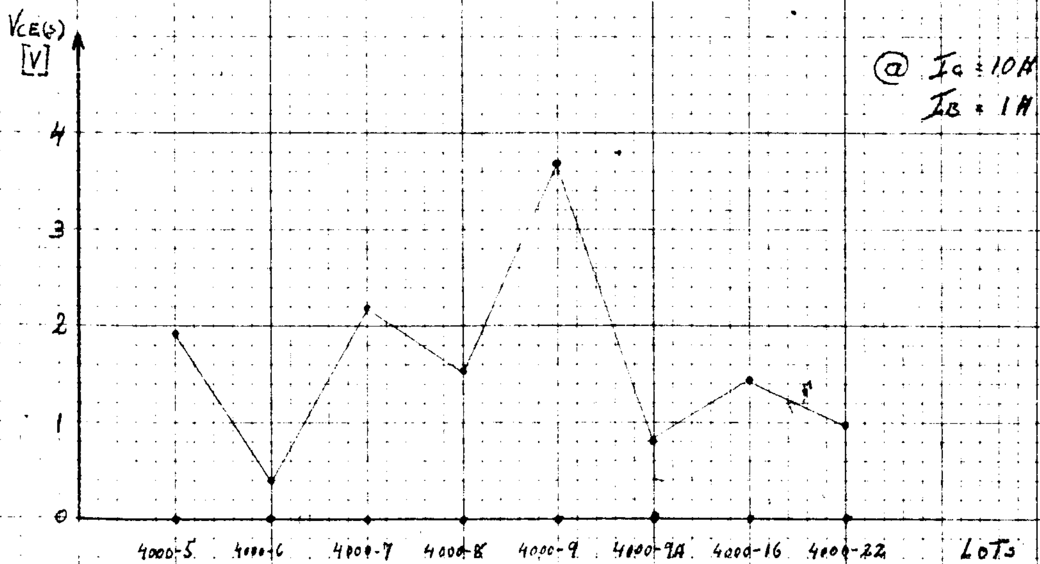



FIGURE 22

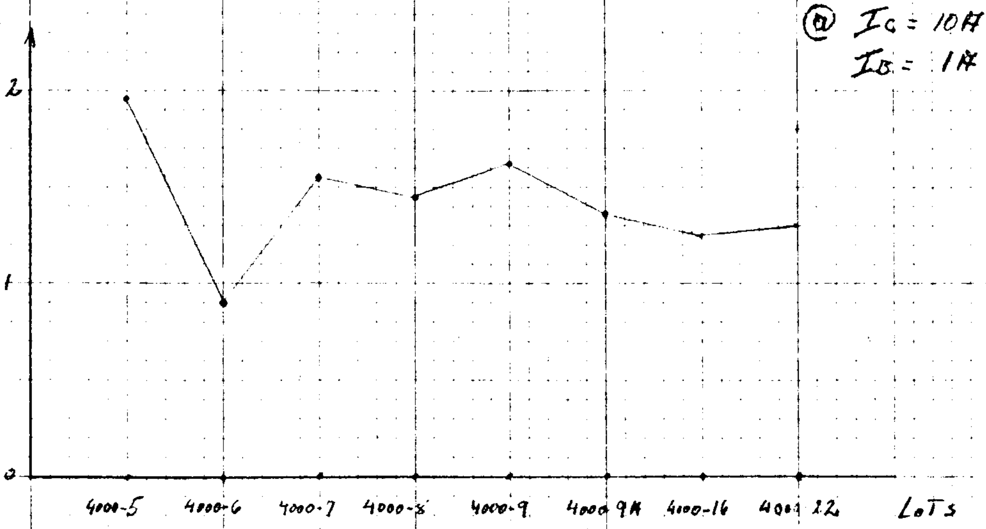



FIGURE 23

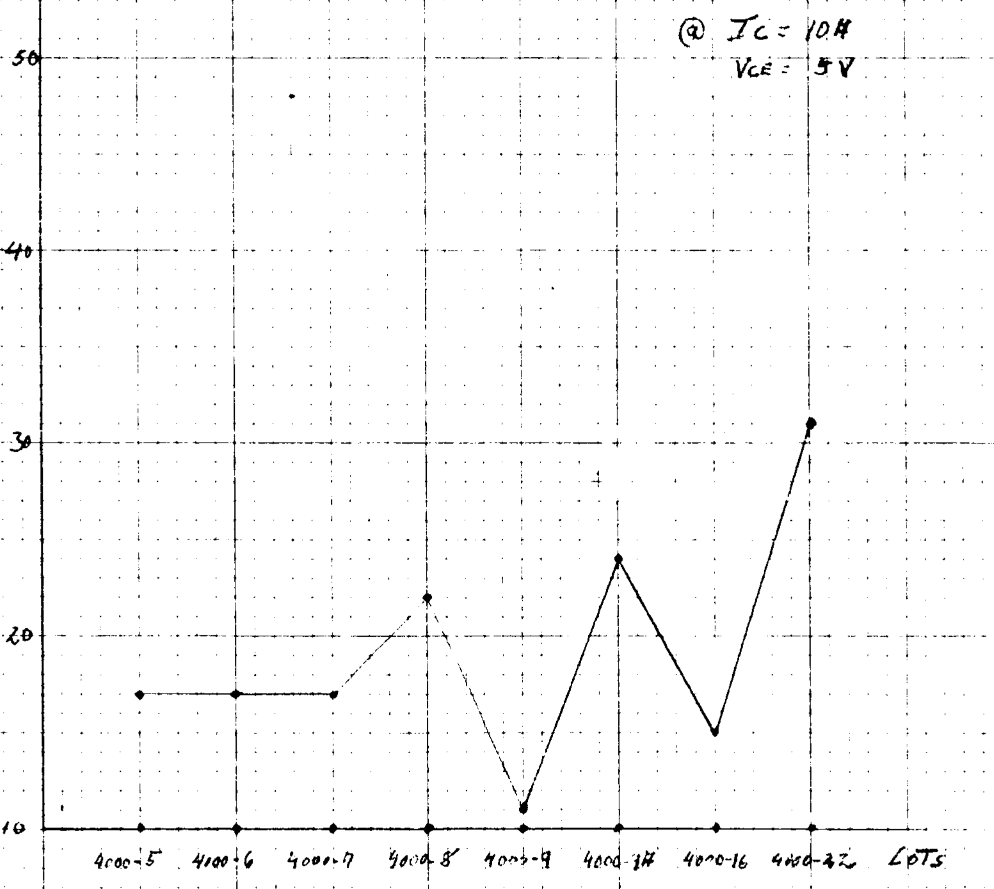



FIGURE 24

10 X 10 PER INCH
MADE IN U. S. A.

10 X 10 PER INCH
MADE IN U. S. A.

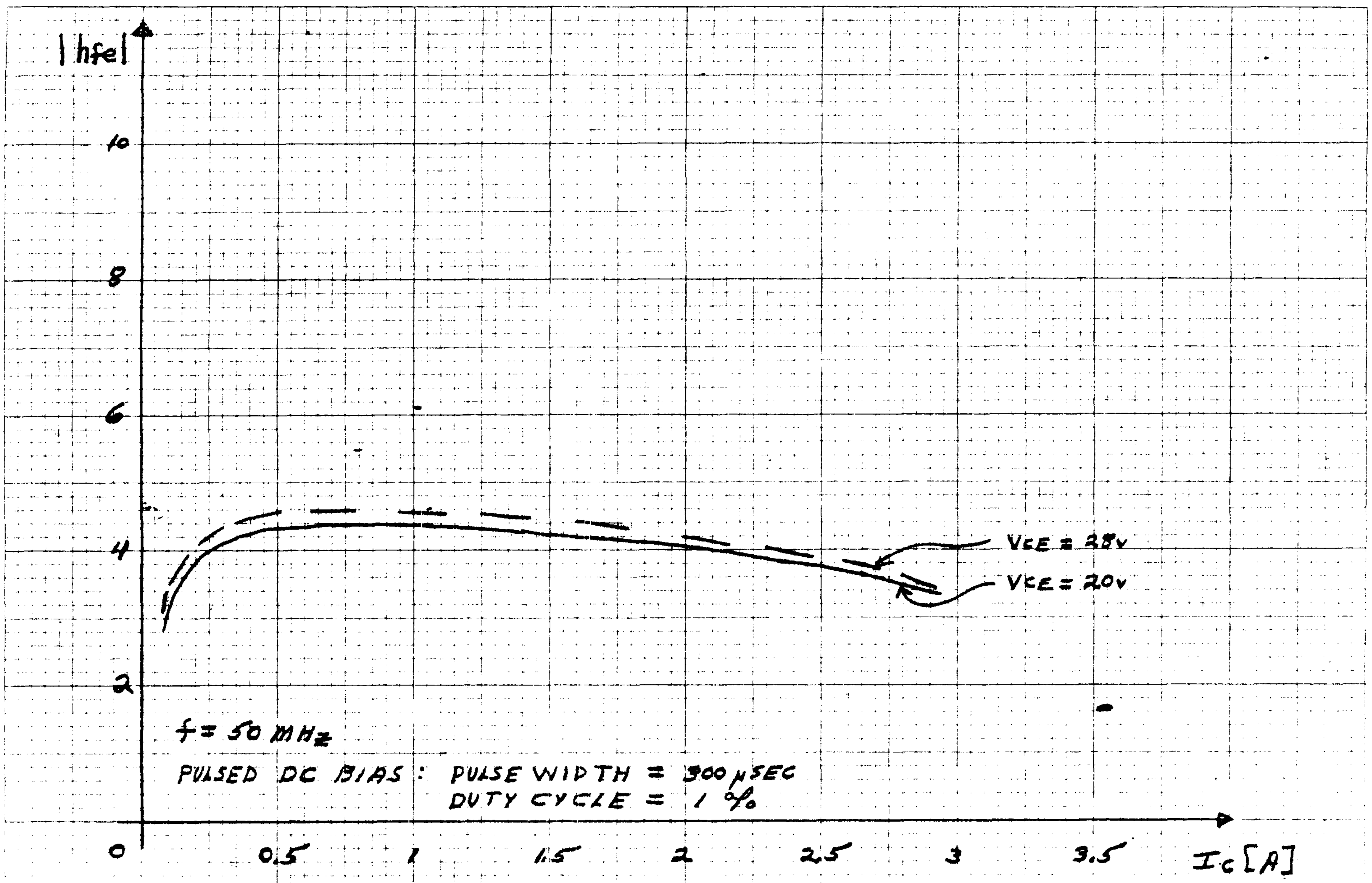
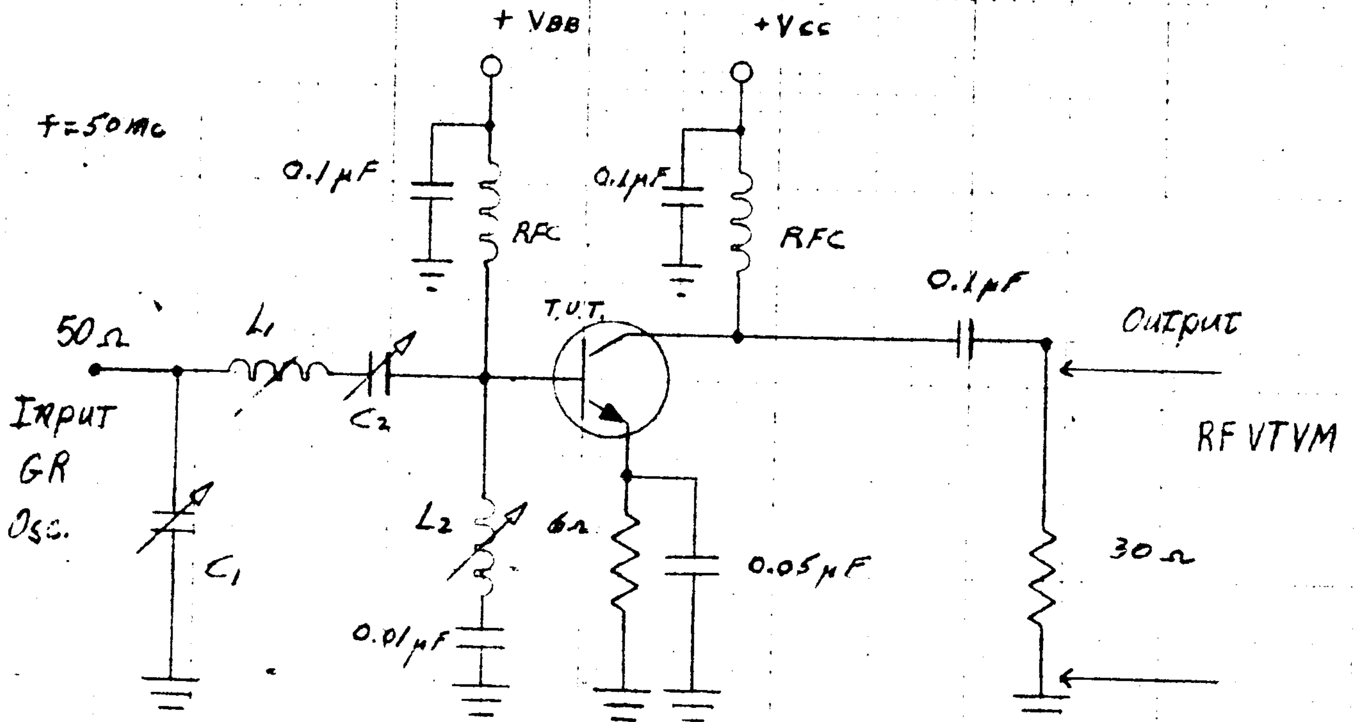



FIGURE 25 |hfe| vs $I_c$ TYPICAL CURVE

# Bendix Class A Power Amplifier




RFC = 7μH

$C_1$ = 170 to 780pF

$C_2$ = 7 to 140 pF

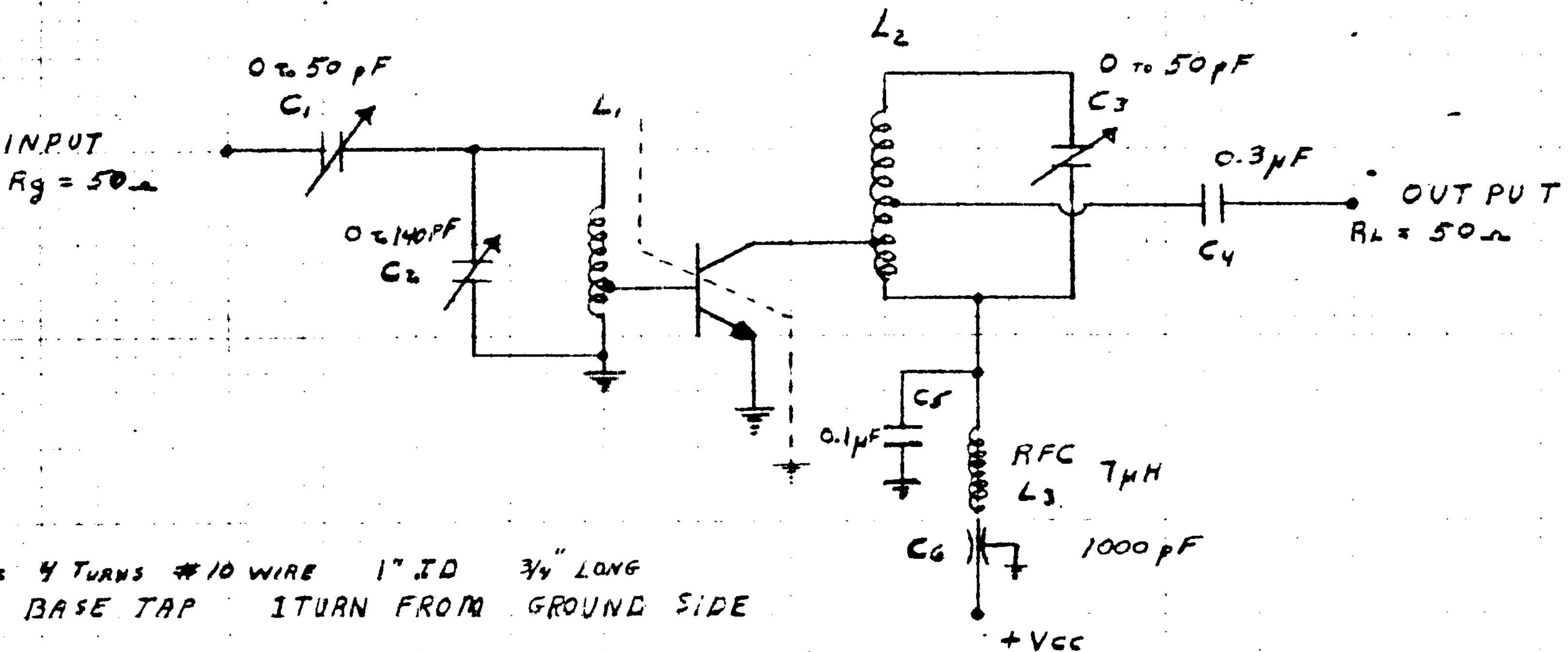
$L_1$ = 6T #16 WIRE COIL FORM OD = 5/16"

$L_2$ ≈ 7T #22 WIRE COIL FORM OD = 5/16"

| TYPICAL CLASS A OPERATION | | |
|---|---|---|
| CIRCUIT CONDITION | EVALUATION DATA | |
| Vcc[V] | 30 | 33 |
| VCE[V] | 26 | 25 |
| Ic[A] | 0.7 | 0.8 |
| PIN[W] | 1 | 1.48 |
| PL[W] | 8 | 10.8 |
| Gp[db] | 9 | 8.65 |
| [illegible] | -- | 41 |

FIGURE 26 CLASS A HIGH FREQ

## 50 Mc CLASS B POWER AMPLIFIER - TEST CIRCUIT




$L_1$ = 4 TURNS #10 WIRE 1" ID 3/4" LONG
BASE TAP 1 TURN FROM GROUND SIDE

$L_2$ = 6 TURNS #10 WIRE 1" ID 1 1/8" LONG
COLLECTOR TAP 1 TURN FROM RFC ($L_3$) SIDE
OUTPUT TAP 1 1/4 TURN FROM RFC ($L_3$) SIDE

FIGURE 27 SCHEMATIC DIAGRAM

4-13-55

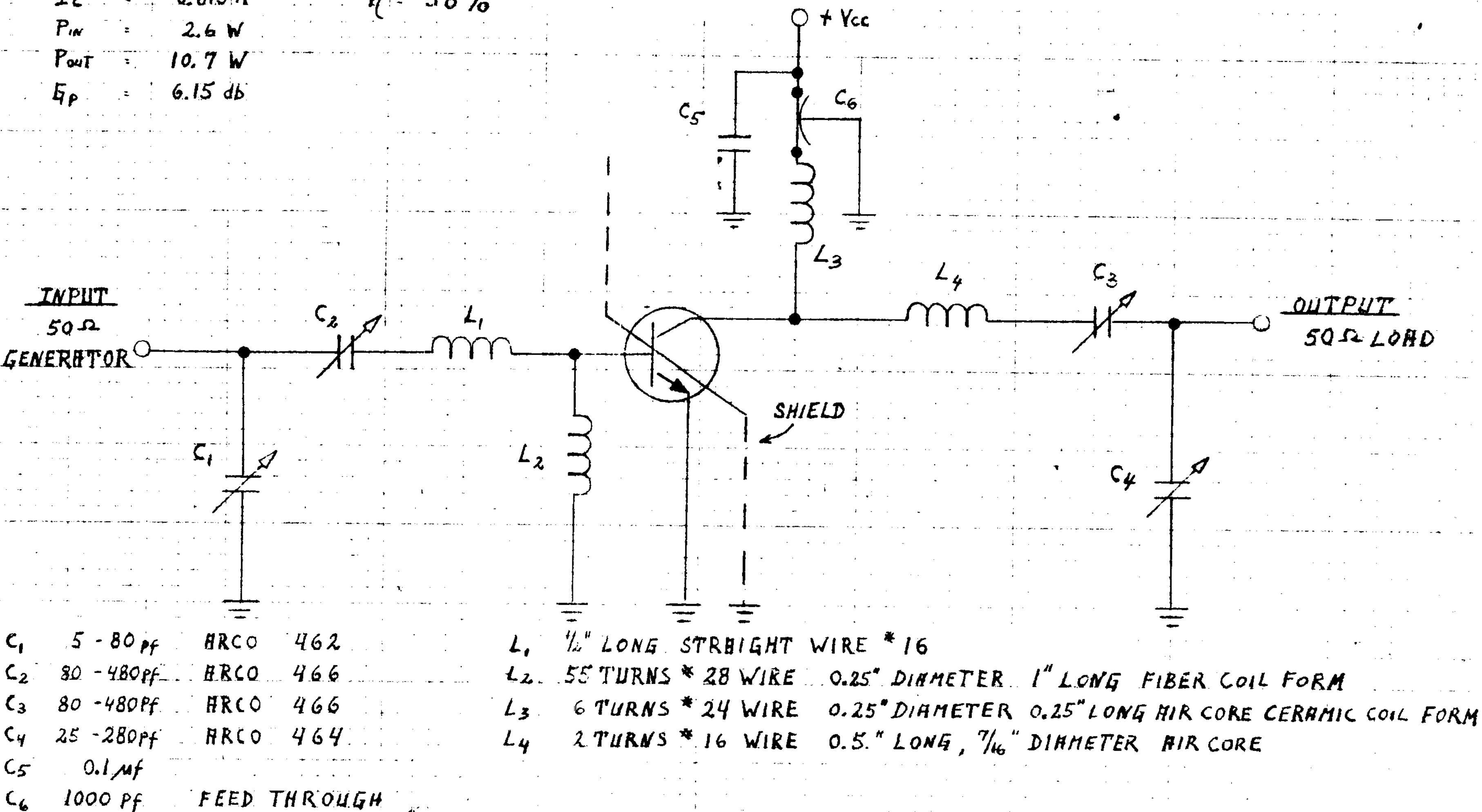
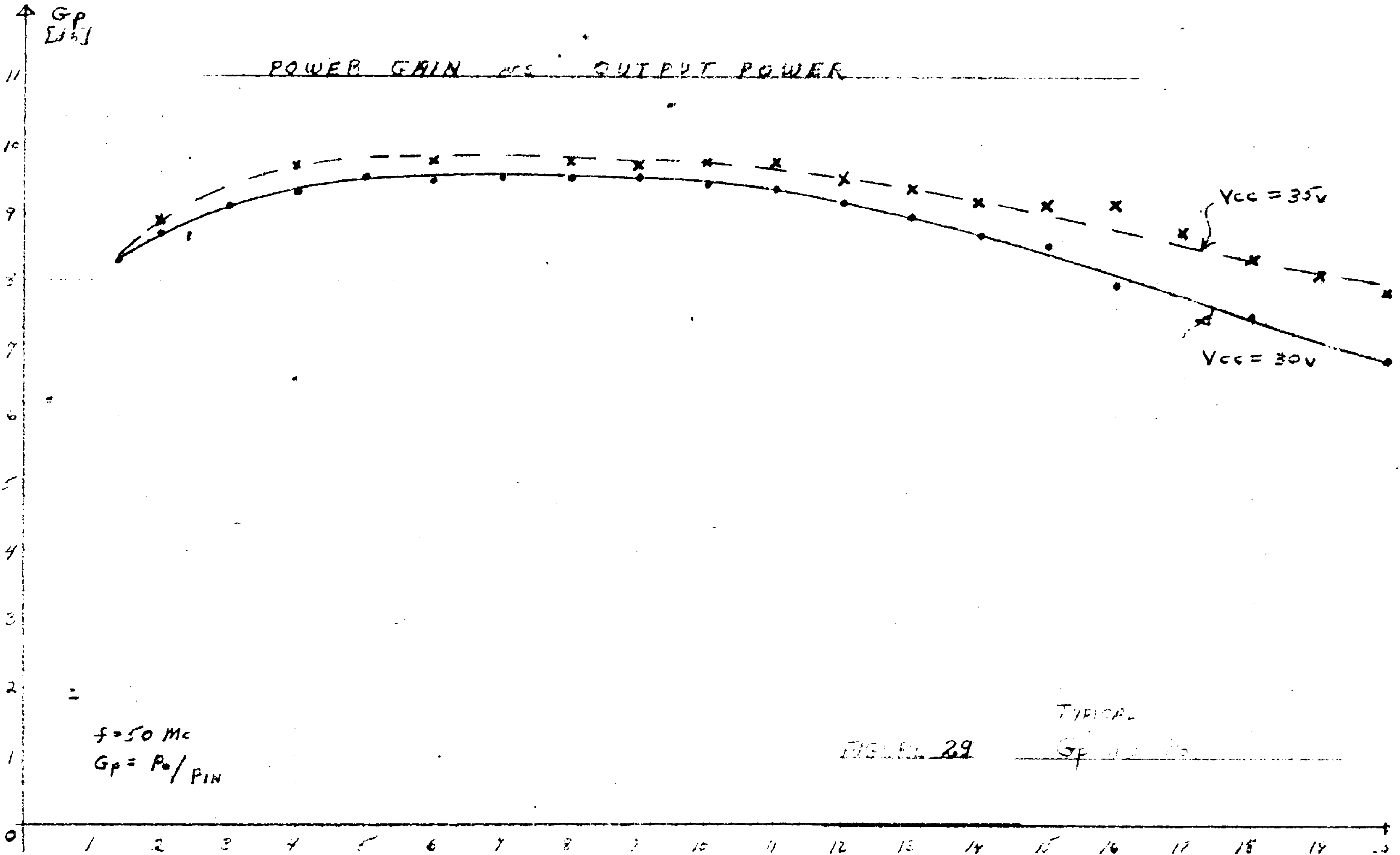



FIGURE 28 SCHEMATIC DIAGRAM – 100 MHz POWER AMPLIFIER



POWER GAIN vs OUTPUT POWER
Gp [db]
Vcc = 35v
Vcc = 30v
f = 50 Mc
Gp = Po/PIN
Po [W]
FIGURE 29
TYPICAL
NASA (REGULAR #5 9000-22 IN 7/16" STUD PKG) 50 mc CLASS A AMPLIFIER

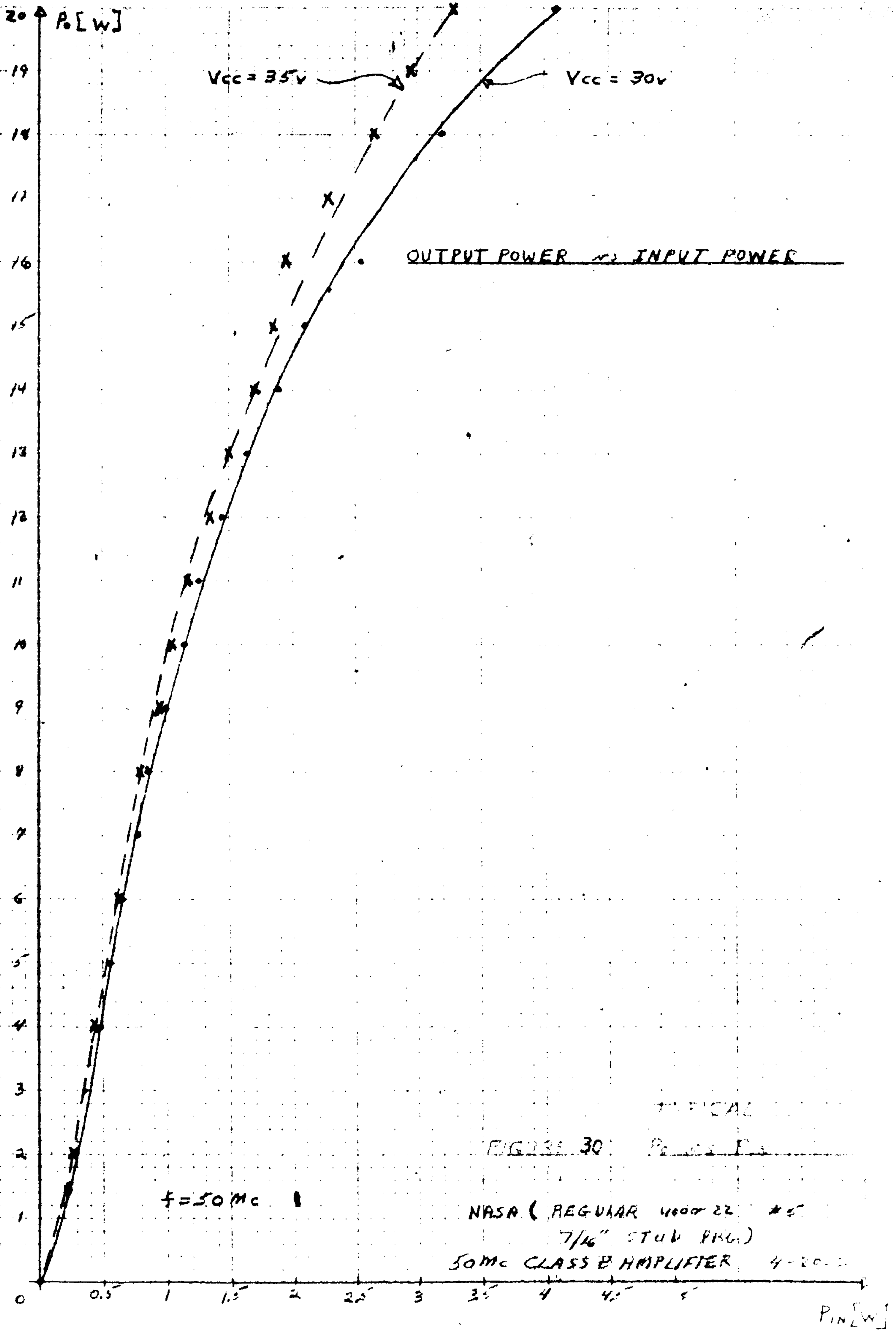



FIGURE 30

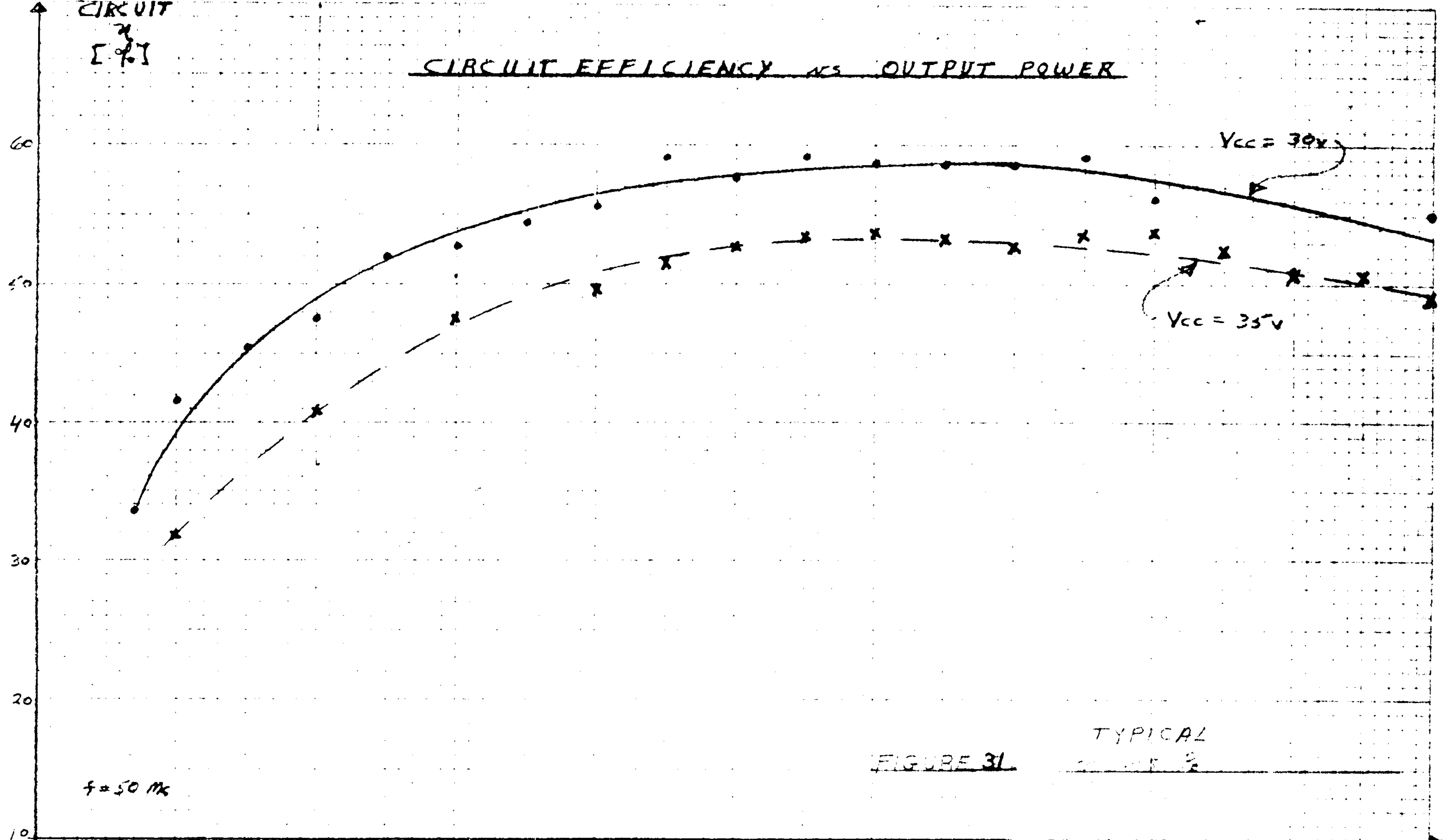



FIGURE 31

# TABLE 1 - LOT PROCESSING

| Process Lot No. | Purpose of Lot | Starting Material $\rho_c$ | Starting Material t (mils) | Starting Material Vendor | Base Diffusion $\rho_s$ | Base Diffusion $X_j$ (μ) | Base Diffusion Oxide Thickness | $p^+$ Diffusion $\rho_s$ | $p^+$ Diffusion $X_j$ (μ) | $p^+$ Diffusion Oxide Thickness | Emitter Diffusion $\rho_s$ | Emitter Diffusion $X_j$ (μ) | Emitter Diffusion $W_B$ (μ) | Final Oxidation Type | Final Oxidation Thickness | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4000-4 | Initial run - new masks | 2.6 | .73 | TI | 231 | 3.6 | 5400Å | 6.56 | 1.8 | — | $p^+$ diffusion penetrated oxide | | | | | |
| 4000-5 | Initial run for evaluation | 2.8 | .71 | TI | 131 | 5.1 | 6200 | 11.3 | 0.9 | 5000Å | 1.68 | 4.2 | 1.5 | Pyrolytic | 5000Å | $p^+$ after emitter |
| 4000-6A | (effect of variation | 3.07 | .67 | Monsanto | 131 | 5.1 | 6200 | 13.1 | 0.9 | 2700 | 2.40 | 2.0 | 2.4 | Thermal | 2700 | $p^+$ after emitter |
| 4000-6B | in base width) | 3.05 | .68 | Monsanto | 131 | 5.1 | 6200 | 13.1 | 0.9 | 2700 | 2.27 | 4.2 | 1.5 | Thermal | 2700 | $p^+$ after emitter |
| 4000-7A | (effect of $p^+$ | 2.8 | .75 | TI | 118 | 4.8 | 5600 | 10.4 | 0.9 | 5000 | 2.31 | 3.6 | 1.5 | Pyrolytic | 5000 | $p^+$ after emitter |
| 4000-7B | diffusion) | 2.8 | .75 | TI | 118 | 4.8 | 5600 | No $p^+$ diffusion | | | 2.31 | 3.6 | 1.5 | Pyrolytic | 5000 | |
| 4000-8 | To do base diffusion after base dep. + $p^+$ deposition | 3.2 | .77 | TI | 544 | 4.5 | 5600 | 37 | 2.3 | 2500 | 2.13 | 3.3 | 1.5 | Pyrolytic | 5000 | |
| 4000-9 | Shallower base depth | 3.0 | .97 | TI | 127 | 3.9 | 5000 | 14.5 | 0.9 | 5000 | 2.04 | 3.3 | 1.0 | Pyrolytic | 5000 | $p^+$ prior to emitter |
| 4000-10 | Shallower base depth. | 3.4 | 1.0 | TI | 116 | 3.6 | 4800 | 15.8 | 1.0 | 2000 | 2.55 | 2.7 | 1.2 | Thermal | 3000 | CB + EB channels |
| 4000-11 | For Proto type units | 3.1 | 1.01 | TI | 362 | 3.6 | 4800 | 14.5 | 0.9 | 2000 | 3.53 | 2.7 | 1.2 | Thermal | 3000 | |
| 4000-12 | For Proto type units | 3.2 | .85 | GME | 181 | 3.6 | 4800 | 15.4 | 0.9 | 2000 | 3.21 | 3.0 | 0.9 | Thermal | 3000 | |
| 4000-13 | For Proto type units | 3.0 | .84 | TI | 289 | 3.6 | 4800 | 15.4 | 0.9 | 2000 | 4.35 | 2.7 | 1.2 | Thermal | 3000 | |
| 4000-14 | For Proto type units | 3.0 | .84 | TI | 229 | 3.6 | 4800 | 12.1 | 1.0 | 5000 | 2.84 | 2.4 | 1.5 | Pyrolytic | 6000 | |
| 4000-15 | Deeper $p^+$ diffusion | 3.03 | .92 | Monsanto | 199 | 3.6 | 4800 | 12.1 | 1.3 | 5000 | 3.27 | 2.4 | 1.5 | Pyrolytic | 6000 | |
| 4000-16 | Evaluate internally grown epitaxial material | 3.0 | .95 | Bendix | 204 | 3.6 | 4600 | 11.7 | 1.0 | 5000 | 3.48 | 2.4 | 1.5 | Pyrolytic | 6000 | |
| 4000-17 | Shallower base depth | 3.1 | .88 | Monsanto | 213 | 3.3 | 4600 | 12.3 | 1.0 | 5000 | 3.30 | 2.1 | 1.3 | Pyrolytic | 6000 | |
| 4000-18 | Narrower Base Width | 3.2 | .85 | GME | 190 | 3.3 | 4600 | 12.3 | 1.0 | 5000 | 3.03 | 2.4 | 1.0 | Pyrolytic | 6000 | |
| 4000-19 | Shallower base depth | 3.1 | 1.01 | TI | 204 | 3.0 | 4400 | 12.3 | 1.0 | 5000 | 2.81 | 2.4 | 1.0 | Pyrolytic | 6000 | |
| 4000-20 | Shallower base depth | 3.1 | 1.02 | TI | 254 | 2.4 | 3600 | 12.7 | 1.0 | 5000 | 5.44 | — | — | — | — | CE punch-thru |
| 4000-21 | Dry $O_2$ base diffusion | 3.0 | .95 | Bendix | 131 | 3.0 | 2500 | 12.3 | 1.0 | 5000 | 3.08 | 2.1 | 1.2 | Pyrolytic | 6000 | |
| 4000-22 | Final Units | 3.0 | .90 | Bendix | 131 | 3.0 | 2500 | 12.3 | 1.0 | 5000 | 3.49 | 2.2 | 1.0 | Pyrolytic | 6000 | |
| 4000-23 | To do $p^+$ diffusion Prior to base diff | 3.0 | .96 | TI | 272 | 2.7 | 2500 | 32.5 | 3.7 | 4000 | 3.62 | 2.0 | 1.0 | Pyrolytic | 6000 | |

| N.A.S.A. TRANSISTOR TO-60 PACKAGE<br>SWITCHING DATA $I_C = 10A$; $I_B = 1A$; $V_{BB} = 5V$<br>FINAL PRODUCTION UNITS | | | | |
|---|---|---|---|---|
| TRANSISTOR No. | CIRCUIT No. 3 | | CIRCUIT No. 4 | |
| | $t_{on}$ (nsec) | $t_{off}$ (nsec) | $t_{on}$ (nsec) | $t_{off}$ (nsec) |
| 1 | 15 | 9 | 7 | 6 |
| 2 | 17 | 11 | 8 | 7 |
| 3 | 15 | 9 | 7 | 6 |
| 4 | 16 | 11 | 8 | 7 |
| 5 | 15 | 11 | 8 | 7 |
| 6 | 16 | 11 | 7 | 7 |
| 7 | 15 | 9 | 7 | 6 |
| 8 | 15 | 11 | 8 | 7 |
| 9 | 17 | 11 | 7 | 7 |
| 10 | 15 | 9 | 7 | 6 |

COMPARISON OF SWITCHING CIRCUITS No. 3 & No. 4

TABLE 3

10 X 10 PER INCH
MADE IN U. S. A.

10 X 10 PER INCH MADE IN U. S. A.

## POWER DISSIPATION TEST

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $P_C$ | [W] | 20 | 25 | 30 | 35 | 40 | 50 | 60 | 70 |
| | $V_{CE}$ | [V] | 5 | 5 | 6 | 7 | 8 | 10 | 12 | 14 |
| | $I_C$ | [A] | 4 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| TO-61 | $T_C$ | [°C] | 130 | 112.5 | 95 | 73 | 60 | 25 | -10 | -45 |
| TO-60 | $T_C$ | [°C] | 120 | 100 | 80 | 60 | 40 | — | — | — |
| | No. OF UNITS HAVING CATASTROPHIC FAILURE | | | | | | | | | |
| TO-61 | 10 UNITS | | 0 | 0 | 0 | 0 | 0 | 0 | 7 | 3 |
| TO-60 | 10 UNITS | | 0 | 0 | 2 | 7 | + | — | — | — |

TABLE 4

| |
|---|
| |
| |
| |
| |
| ENG. FILE |

**THE BENDIX CORPORATION**
BENDIX SEMICONDUCTOR DIVISION
HOLMDEL, N. J.

Test Report No. 4 [illegible]
Date of Test
By

Title TYPICAL VALUES B/LOT COMPARISON

| LOT No. | $V_{CEO}$ | $V_{CE(SAT)}$ | $V_{BE(SAT)}$ | $h_{FE}$ | $f_T$ | Cob | Cebo |
|---|---|---|---|---|---|---|---|
| | $I_C$ 100 mA | $I_C$ 10A | $I_C$ 10A | $I_C$ 10A | $I_C$ 0.4A | f=1 Mc $V_{CB}$= | f=1 Mc $V_{EB}$= |
| | | $I_B$ 1A | $I_B$ 1A | $V_{CE}$ 5V | $V_{CE}$ 30V | 10V | 5V |
| | | | | | f= 100 MC | | |
| | V | V | V | | MC | Pf | Pf |
| 4000-5 | 45 | 1.95 | 1.98 | 17 | 190 | 53.9 | 247 |
| 4800-6 | 64 | 0.4 | 0.9 | 17 | 220 | 44.9 | * |
| 4000-7 | 60 | 2.2 | 1.55 | 17 | 170 | 56 | 296 |
| 1000-8 | 63 | 1.55 | 1.45 | 22 | 165 | 47 | 265 |
| 1000-9 | 61 | 3.7 | 1.62 | 11 | 190 | 47 | 277 |
| 000-9A | 55 | 0.8 | 1.36 | 24 | 180 | 49.5 | 256 |
| 000-16 | 67 | 1.44 | 1.25 | 15 | 160 | * | * |
| 000-22 | 53 | 0.98 | 1.3 | 31 | 220 | 46 | 236 |

* NOT EVALUATED FOR THESE PARAMETERS

| ENG. FILE | |
|---|---|

**THE BENDIX CORPORATION**
BENDIX SEMICONDUCTOR DIVISION
HOLMDEL, N. J.

Test Report No. 3
Date of Test
By GW SH.

Title: FIFTY (50) PRODUCTION UNITS AS PER CONTRACT No. N.A.S. 8-1164

| TEST | $V_{CEO}$ (SUS) | $V_{CE}$ (SAT) | $V_{BE}$ (SAT) | $I_{CES}$ | $I_{CES}$ | $I_{EBO}$ | $h_{FE}$ | $\theta_{J-C}$ | $t_{on}$ | $t_{off}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| CONDITION | $I_C$ 100 mA | $I_C$ 10A, $I_B$ 1A | $I_C$ 10A, $I_B$ 1A | $V_{CE}$ 50V, $T_J$ 20°C | $V_{CE}$ 50V, $T_J$ 200°C | $V_{EB}$ 7V, $T_J$ 200°C | $I_C$ 10A, $V_{CE}$ 4V | | $I_C$ 10A, $I_B$ 1A, CIRCUIT #4 | $I_C$ 10A, $I_B$ 1A |
| LIMITS | MIN. 50 | MAX. 1V | MAX. 2V | MAX. 1mA | MAX. 10mA | MAX. 1mA | MIN. 10 | MAX. 4°C | MAX 5μsec | MAX 5μsec |
| UNITS | V | V | V | μA | μA | μA | — | °C/W | μsec | μsec |
| 21 | 52 | 0.65 | 1.30 | 50 | 73 | 4.6 | 37 | 2.4 | 7 | 7 |
| 22 | 50 | 0.60 | 1.22 | < 2 | 32 | 7.4 | 33 | 2.2 | 7 | 6 |
| 23 | 58 | 0.70 | 1.30 | < 2 | 59 | 15.7 | 42 | 2.4 | 7 | 6 |
| 24 | 51 | 0.72 | 1.26 | < 2 | 26 | 5.8 | 27 | 2.2 | 7 | 6 |
| 25 | 50 | 0.67 | 1.28 | < 2 | 31 | 3.6 | 31 | 2.0 | 7 | 6 |
| 26 | 62 | 0.71 | 1.25 | < 2 | 38 | 7.8 | 20 | 2.1 | 7 | 6 |
| 27 | 62 | 0.88 | 1.20 | < 2 | 26 | 5.4 | 20 | 2.0 | 7 | 7 |
| 28 | 60 | 0.71 | 1.30 | < 2 | 27 | 50 | 21 | 3.1 | 9 | 7 |
| 29 | 58 | 0.76 | 1.25 | < 2 | 33 | 7.5 | 28 | 2.2 | 7 | 7 |
| 30 | 62 | 0.96 | 1.30 | < 2 | 23 | 46 | 20 | 2.4 | 9 | 7 |
| 31 | 59 | 0.77 | 1.20 | < 2 | 48 | 8.5 | 30 | 2.8 | 7 | 6 |
| 32 | 60 | 0.75 | 1.40 | < 2 | 70 | 4.0 | 22 | 2.9 | 9 | 6 |
| 33 | 53 | 0.95 | 1.35 | < 2 | 66 | 11 | 32 | 2.6 | 7 | 7 |
| 34 | 51 | 0.95 | 1.35 | < 2 | 78 | 16 | 26 | 2.4 | 8 | 7 |
| 35 | 50 | 0.90 | 1.35 | < 2 | 67 | 7.7 | 28 | 2.0 | 7 | 7 |
| 36 | 63 | 0.70 | 1.45 | < 2 | 71 | 26.5 | 22 | 2.2 | 7 | 7 |
| 37 | 63 | 0.60 | 1.40 | < 2 | 69 | 14 | 29 | 2.0 | 9 | 7 |
| 38 | 62 | 0.55 | 1.30 | < 2 | 33 | 5 | 28 | 2.5 | 7 | 7 |
| 39 | 57 | 0.55 | 1.30 | 10 | 82 | 7.2 | 28 | 2.0 | 7 | 7 |
| 40 | 51 | 0.60 | 1.35 | < 2 | 32 | 74 | 38 | 3.1 | 7 | 7 |

ENGINEERING COPY

| ENG. FILE |
|---|

**THE BENDIX CORPORATION**

BENDIX SEMICONDUCTOR DIVISION

HOLMDEL, N. J.

Test Report No. 4

Date of Test

By GW-SH

Title FIFTY (50) PRODUCTION UNITS AS PER CONTRACT No. N.A.S. 8 1611

| TEST | $V_{CEO}$ (SUS) | $V_{CE}$ (SAT) | $V_{BE}$ (SAT) | $I_{CES}$ | $I_{CES}$ | $I_{EBO}$ | $h_{FE}$ | $\theta_{J-C}$ | $t_{on}$ | $t_{off}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| CONDITION | $I_C$ 100 mA | $I_C$ 10A, $I_B$ 1A | $I_C$ 10A | $V_{CE}$ 50V, $T_J$ 20°C | $V_{CE}$ 50V, $T_J$ 200°C | $V_{EB}$ 7V, $T_J$ 200°C | $I_C$ 10A, $V_{CE}$ 4V | | $I_C$ 10A, $I_B$ 1A, CIRCUIT #4 | $I_C$ 10A, $I_B$ 1A |
| LIMITS | MIN. 50V | MAX. 1V | MAX. 2V | MAX. 1mA | MAX. 10mA | MAX. 1mA | MIN. 10 | MAX. 4°C | MAX. 5 nsec | MAX. 5 nsec |
| UNITS | V | V | V | μA | μA | μA | | °C/W | n sec | n sec |
| 41 | 53 | 0.90 | 1.22 | 2 | 220 | 9.5 | 30 | 2.5 | 7 | 7 |
| 42 | 52 | 0.70 | 1.35 | 2 | 62 | 14 | 36 | 2.9 | 7 | 7 |
| 43 | 54 | 0.90 | 1.32 | 2 | 54 | 14.5 | 27 | 2.5 | 7 | 6 |
| 44 | 53 | 1.20 | 1.38 | 2 | 42 | 220 | 29 | 2.9 | 7 | 7 |
| 45 | 50 | 0.60 | 1.28 | 20 | 49 | 16 | 38 | 2.3 | 7 | 7 |
| 46 | 51 | 0.70 | 1.35 | 2 | 36 | 11.5 | 38 | 2.5 | 7 | 7 |
| 47 | 52 | 1.00 | 1.32 | 2 | 44 | 23 | 27 | 3.4 | 7 | 7 |
| 48 | 52 | 0.70 | 1.32 | 2 | 85 | 16 | 30 | 2.4 | 7 | 7 |
| 49 | 57 | 1.60 | 1.40 | 2 | 45 | 8.5 | 25 | 3.3 | 9 | 7 |
| 50 | 60 | 0.65 | 1.40 | 2 | 56 | 9.5 | 23 | 2.1 | 9 | 7 |



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