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GENERAL DYNAMICS
ASTRONAUTICS

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COMPUTER AIDS FOR

WORST CASE ELECTRONIC

CIRCUIT DESIGN

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FOREWORD

This report [illegible] work [illegible] case circuit design [illegible] digital computer [illegible].

This study is principally concerned with [illegible] investigations resulting from a presentation [illegible] programmed into the Control Digital [illegible] under contract NAS8-2252.

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SUMMARY

This paper describes several methods of designing switching circuits and optimizing these designs, using a digital computer as a design tool. A method of examining the on-off equation plot of an inverter switching circuit is discussed; and a technique for maximizing the output load current and the fan-out factor for an inverter circuit is also presented.

A tabulation of existing computer programs for transistor resistor logic circuits is given.

In addition, an analysis of a linear circuit is made to determine the parametric changes affecting the d-c bias stability and the manner in which this, in turn, affects the linearity and gain.

Author

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SECTION I

INTRODUCTION

1.1 GENERAL

This report describes work which is being accomplished in the area of worst case and optimized circuit design by the General Dynamics/Astronautics-Centaur flight control group. Particular areas of development are engineering aids to:

a. Predict the optimum design.

b. Find the maximum stress that a circuit may withstand without reduced operability.

These aids are primarily oriented towards new design such that improved devices may be efficiently and carefully utlized by exercising an analog model of the circuits. Mathematical models are primarily based on on-off equations for digital circuits and nodal equations for linear circuits.

All programs produced for circuit evaluation are written in Fortran to be operated on the IBM-7094 computer configuration. These programs are available and other engineering groups are invited to use and add to the library as the need arises.

This report will be revised to include new solutions and methods of analysis switching circuit and analog problems as they occur.

The services and assistance of the scientific data processing logic systems programming group Dept 158-1 are utilized in the programming of the worst case and optimized design solutions.

1.2 PURPOSE

The purpose of this program is to develop a library of computer programs to predict optimum design configurations and evaluate maximum capability of a particular configuration. These programs will provide design assurance essential to high reliability goals of the Centaur program. All programs are designed for flexibility and ease of operation such that an engineer may modify input data and receive stress data in minimum time at minimum cost. The goal is to provide these data at a cost less than that required to manually evaluate the circuit.

1.3 SCOPE

Programs have been developed which evaluate resistor-transistor logic schemes (NOR-LOGIC) without clamping diodes. This type of logic is presently being used in the Centaur upper stage for simplicity and reliability. Programs also exist to evaluate linear circuits with ten nodes. These programs include special-purpose matrix solutions, whose input constants may be varied, and modifications of the IBM-Share library models oriented to the Centaur servo and gyro amplifier configurations.

1.4 UTILIZATION

The designer desiring to utilize these programs will face an indoctrination period to familiarize himself with the techniques and tools available at his disposal. It is expected that the average engineer would become efficient after performing one or two designs by this technique. In addition, new design configurations may be analyzed with minor modification of input parameters. This allows the designer to readily implement new devices, changes, and suggestions with minimum modification design time.

SECTION II

SWITCHING CIRCUITS

2.1 DESIGN CONSIDERATIONS

2.1.1 TRL CIRCUITS. The optimized design of TRL circuits is based on the following considerations.

a. Upper and lower temperature limits.
b. Transistor parameter variations.
c. Component variations.
d. Power supply variations.

2.1.2 CIRCUIT CONFIGURATIONS. The following circuit configurations have been considered for analysis at this time.

a. TRL nor gate.
b. Relay driver.
c. Inverter.
d. Set reset – bistable.

Optimized design circuits can be designed to meet several objectives. A table of possible design objectives together with the constraining condition is shown in Table 2-1. Also shown in Table 2-1 is the circuit variable that can be adjusted to obtain an optimum design. Which design parameter to be optimized is a design choice or is dictated by the design specification.

2.2 DESIGN PROCEDURES

A worst case design can be accomplished by different methods of analysis. Several methods of attack are described below and examples given of each.

2.2.1 ON-OFF EQUATION PLOT. Given the "on" equation and the "off" equation of a simple saturated inverter, the "on" and "off" equations can be plotted on the same coordinate axes. The area enclosed by the "on" equation and the "off" equation and the X axis represents solutions satisfying both "on" and "off" conditions. The resistor tolerances and power supply tolerances are to be included in the "on" and "off" equations. The centroid of the area enclosed by the "on" and "off" curves is the best solution. This solution does not give the maximum fan out for the circuit constraints, but does give the maximum safe operating point. The analysis of the circuit is given in Paragraph 2.2.3.

TABLE 2-1. POSSIBLE DESIGN OBJECTIVES

Circuit	Variables to be Optimized	Variables to be Optimized	Constraints
NOR-RTL	Fan Out – N maximum	R_B, R_K, R_C	V_{BB}, V_{cc}, M I_B, H_{FE}, V_{BEO}
NOR-RTL	Fan In – M maximum	R_B, R_K, R_C	V_{BB}, V_{cc}, I_{D2} H_{FE}, V_{DEO}, N I_L
Inverter	Fan Out – N maximum	R_B, R_K, R_C	V_{BB}, V_{cc}, I_{B2} H_{FE}, V_{DEO}, N I_L
NOR-RTL	Minimizing Switching Time	$R_B R_K R_C C$	V_{BB}, V_{cc}, M, I_{D2}, H_{FE}, V_{BEO} I_L

2.5 EXAMPLE

2.5.1 PROBLEM. Find optimum values of R_1 and R_2. Given a fan out of 1 and base current I_{B2} of Q_2.

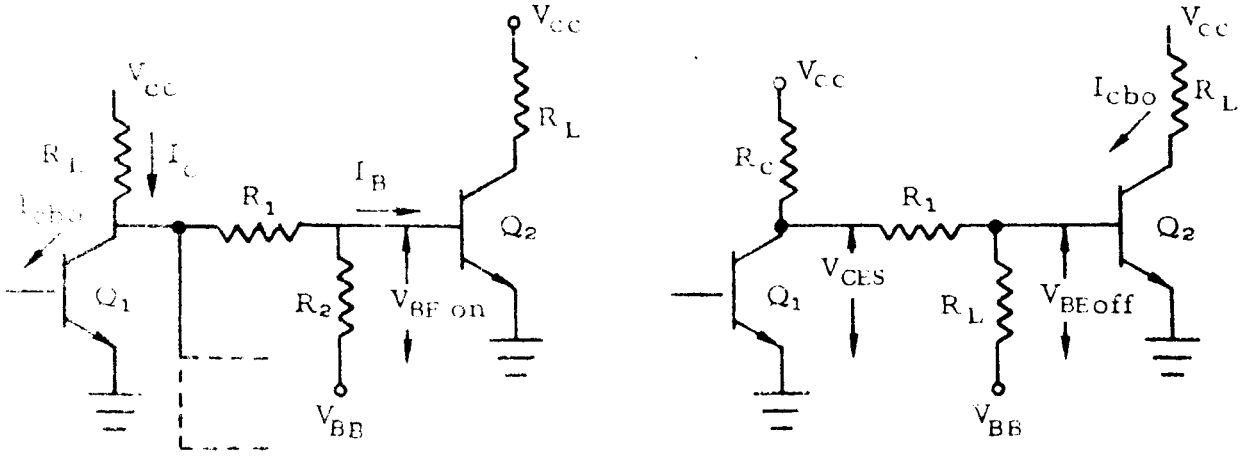

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Figure 2-1. Optimum Values of R_1 and R_2

2.3.1.1 Design Constants

V_{cc} = collector supply voltage

$V_{BE\,on}$ = base to emitter voltage – forward bias of Q2

N = fan out

V_{BEoff} = reverse bias voltage — design option

V_{CES} = saturation voltage Q_1

I_C = base current Q_2

t = resistor tolerance (decimal fraction)

R_c = collector resistance of Q_1

I_{cbo} = collector leakage current at maximum operating temperature.

R_L = Q_2 load

The "on" equation for Q_2 is as follows:

$$\underline{I_B} = \frac{V_{cc} - \overline{V_{BE\,on}} - \overline{I_{cbo}} R_c}{R_c(1+t) + R_1(1+t)} - \frac{\overline{V_{BB}} + \overline{V_{BE\,on}}}{R_2(1-t)} \qquad (2.1)$$

where

$$\overline{I_B} = \frac{\overline{V_{cc}}}{R_c\,(1-t)\,\underline{B}} \quad \text{where B = minimum } H_{FE} \text{ of } Q_2. \qquad (2.2)$$

Subscripts and superscripts indicate a minimum and maximum value respectively. Placing the value of I_B obtained in equation (2.2) in equation (2.1). Setting the resulting equation equal to zero and collecting terms.

$$R_1 V_B(1+t) + R_1 R_2 I_B(1-t^2) + R_2\left[-V_A(1-t) + I_B R_c R_2 (1-t)^2\right] + V_B R_c(1+t) = 0 \qquad (2.3)$$

where

$$V_A = \underline{V_{CC}} - \overline{V_{BE\,on}} - I_{cbo}R_c(1+t),\ V_B = \overline{V_{BB}} + \overline{V_{BE\,on}}$$

where

$$A_1 = V_B(1+t) \tag{2.4}$$

$$B_1 = \underline{I_B}(1-t^2) \tag{2.5}$$

$$C_1 = -V_A(1-t) + I_B R_c R_2 (1-t)^2 \tag{2.6}$$

$$D_1 = V_B R_c (1+t) \tag{2.7}$$

which is an equation of the form

$$A_1 R_1 + B_1 R_1 R_2 + C_1 R_2 + D_1 = 0 \tag{2.8}$$

Solving for R_2

$$R_2 = \frac{-AR_1 + D_1}{C_1 + B_1 R_1} \quad \text{On Equation} \tag{2.9}$$

$$R_2 = \frac{(\overline{V_{BB}} + \overline{V_{BE\,on}})(1+t)\left[R_c + R_1\right]}{(1-t)\left[\overline{V_{BE\,on}} - V_{CC} + I_{cbo}R_c\right] + (1-t)^2 I_B R_1 + I_B(1-t^2)R_c} \tag{2.10}$$

The "off" equation is

$$V_{BE\,off} = \frac{\overline{V_{CES}}\ R_2(1+t) - V_{BB}(1-t)R_1 + \overline{I_{cbo}}\ R_1 R_2 (1-t^2)}{R_1(1-t) + R_2(1+t)} \tag{2.11}$$

Collecting terms and setting equation (2.11) equal to zero

$$R_1\left[\underline{V_{BB}}(1-t) - V_{BE\,off}(1-t)\right] + R_2\left[\overline{V_{CES}}(1+t) - V_{BE\,off}(1+t)\right] + R_1 R_2\left[(1-t^2)I_{cbo}\right] = 0 \tag{2.12}$$

which is an equation of the form

$$A_2 R_1 + B_2 R_1 R_2 + C_2 R_2 = 0$$

where

$$A_2 = (1-t)(-V_{BB} - V_{BE\,off}) \tag{2.13}$$

$$B_2 = (1+t)(\overline{V_{CES}} - V_{BE\,off}) \tag{2.14}$$

$$C_2 = (1-t^2)\, I_{cbo} \tag{2.15}$$

solving for R_2

$$R_2 = \frac{-A_2 R_1}{B_2 R_1 + C_2} \tag{2.16}$$

$$R_2 = \frac{(1-t)(-V_{BB} - V_{BE\,off})}{(1+t)(\overline{V_{CES}} - V_{BE\,off})\, R_1 + (1-t)^2\, I_{cbo}} \tag{2.17}$$

The two resulting expressions for the "on" equation and the "off" equation

$$R_2 = f_1(R_1) \qquad \text{"on" equation} \tag{2.18}$$

$$R_2 = f(R_1) \qquad \text{"off" equation} \tag{2.19}$$

are both expressed as functions of R_1. A graph of $R_2 = f(R_1)$ "ON" $R_2 = f(R_1)$ "OFF" is plotted. Figure 2-2 shows a plot of the "on" and "off" equations. The I_{cbo} term is neglected in these plots

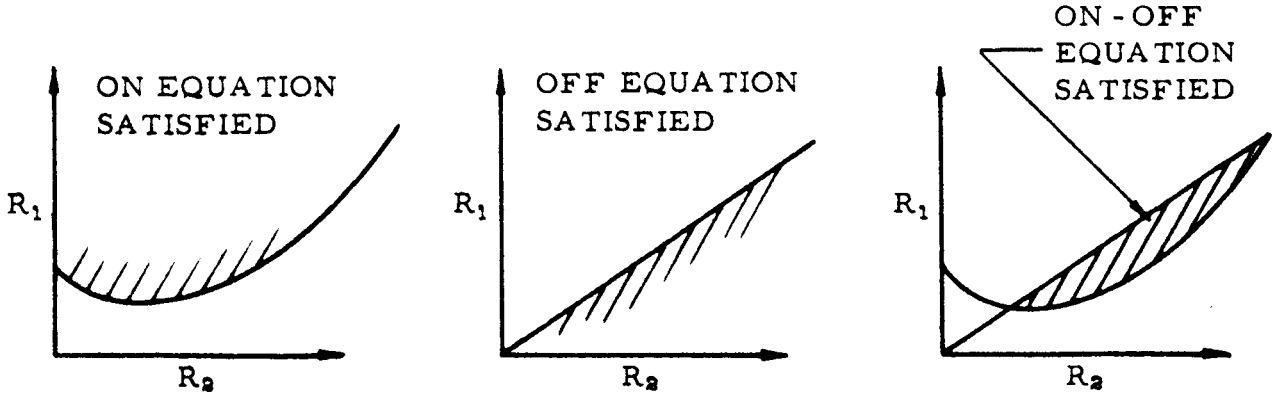

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Figure 2-2. On-Off Equations

The area bounded by the "on" and "off" equations is an acceptable solution satisfying both "on" and "off" conditions.

A computer program exists for obtaining the "ON" and "OFF" equation. The existing program has the I_{cbo} terms set equal to zero since for the types of transistors used, the collector leakage terms made negligible contributions to the V_{BEoff} and I_B terms.

The "on" equation may be modified to include a fan out factor N, where N is the number of stages being supplied a base current of I_B from Q_1. Equation (2.1) becomes

$$\underline{I_B} = \frac{\underline{V_{cc}} - \overline{V_{BEon}} - I_{co}R_c}{N R_c (1+t) + R_1 (1+t)} - \frac{\overline{V_{BB}} + \overline{V_{BEon}}}{R_2 (1-t)} \qquad (2.20)$$

Equation (2.20) does not take into account current hogging which results in differences in R_1 and V_{BEon} between stages of inverters being supplied by Q_1. When current hogging is taken into account, the fan out is reduced to N_o where N_o is given by:

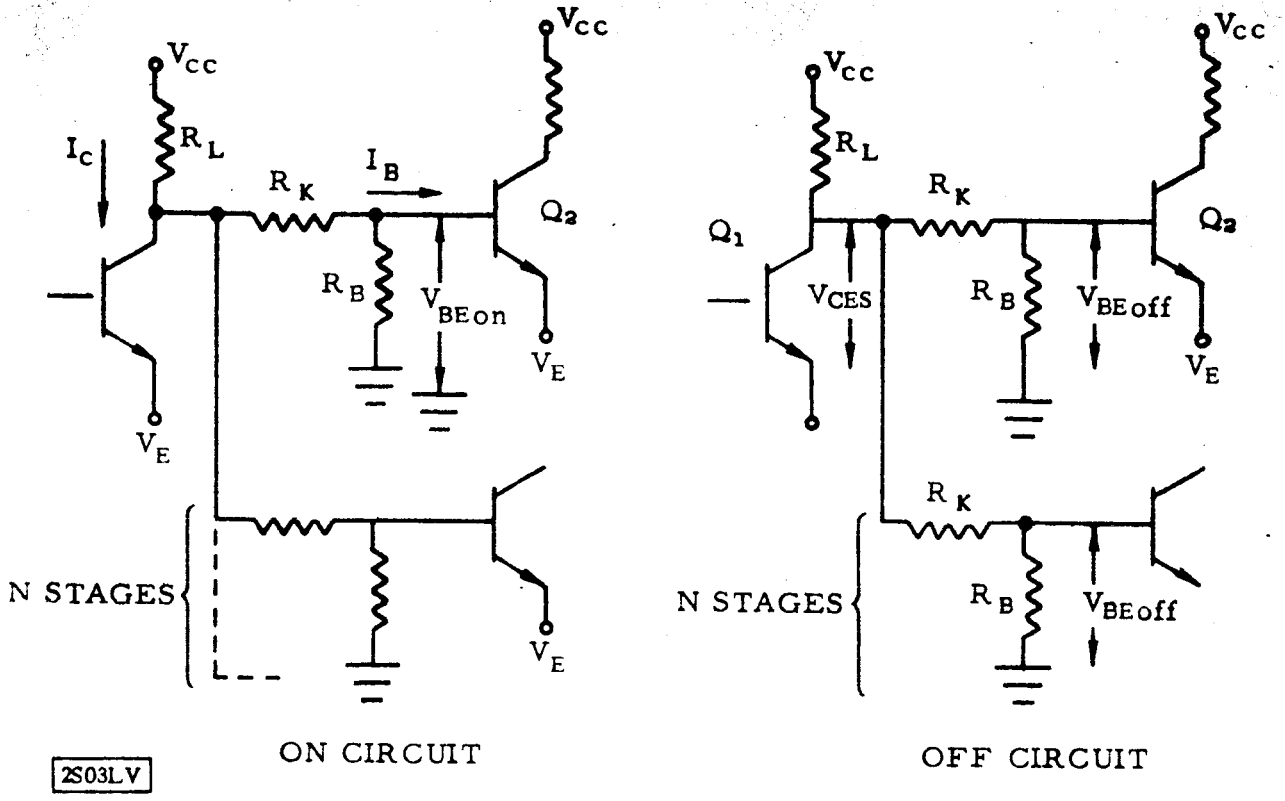
$$N_o = (N-1)\,K + 1 \qquad (2.21)$$

$$K = \frac{\left[\underline{V_{cc}} - I_{cbo}R_L(1+t) - \overline{V_{BEon}}\right]\left[R_1(1-t) + NR_L(1-t)\right]}{\left[\underline{V_{cc}} - \underline{V_{BEon}}\right]\left[R_K(1+t) + NR_L(1+t)\right]} \qquad (2.22)$$

The circuit may be optimized as shown in Table 2-1 by maximizing R_C or N with respect to R_1. The method of attack in optimizing equation (2.1) is to substitute equation (2.2) into (2.1). Find dR_C/dR_1 or dN/dR_1 set resulting equation equal to zero and solve resulting equations for R_1, R_2, and R_C using equation (2.2) as an auxiliary equation. This particular example is not optimized. The following example is optimized for a maximum R_C given a base current I_B, and also for a maximum N_1 given a base current I_B.

2.4 INVERTER CIRCUIT

Consider the inverter circuit shown in Figure 2-3 with back bias provided with an emitter supply voltage V_E instead of the conventional back bias supply V_{BB}. The I_{cbo} terms have been neglected in this case but can be easily inserted into the on off equation if desired. A program has been written to find the minimum collector current I_c for the driver stage Q_1 by finding dR_c/dR_1 and solving for R_1, R_2 and R_C. A second program number of stages of inverters that may be connected to Q_1 each inverter requiring a base current I_B.



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ON CIRCUIT

OFF CIRCUIT

Figure 2-3. Inverter Circuit

V_{cc} = collector supply voltage

N = fan out

V_E = emitter supply voltage

$V_{BE\,off}$ = Reverse bias voltage — design option

V_{ces} = saturation voltage Q_1

I_B = base current Q_2 design constant

t = resistor tolerance - (decimal fraction)

R_L = collector load resistor Q_1

$\overline{V_{BE\,on}} = \overline{V_E} + V_f$

V_f = Base to emitter voltage forward bias of Q_2

From Figure 2-3 the "on" equation can be written as:

$$\frac{V_{CC} - \overline{V_{BE\,on}}}{(1+t)(R_K + NR_L)} - \frac{\overline{V_{BE\,on}}}{R_B(1-t)} = I_B \qquad (2.23)$$

and the "off" equation as:

$$V_{BEO} = \frac{V_O R_B (1-t)}{(1+t) R_K + R_B (1-t)} - \overline{V_E} \qquad (2.24)$$

where

$$V_O = \overline{V_E} + \overline{V_{CES}}$$

solving equation (2.24) for R_B

$$\left[(1+t)\overline{R_K} + R_B(1-t)\right] V_{BEO} - V_O R_B (1-t) + V_E \left[(1+t) R_K + R_B (1-t)\right] = 0 \qquad (2.25)$$

$$V_{BEO}(1+t) R_K + V_{BEO}(1-t) R_B - V_O (1-t) + V_E (1+t) R_K + V_E (1-t) R_B = 0 \qquad (2.26)$$

$$R_B \left[V_{BEO}(1-t) - V_O (1-t) + V_E (1-t)\right] = -R_K \left[V_{BEO}(1+t) + V_E (1+t)\right] \qquad (2.27)$$

$$R_B = R_K \left[- \frac{(1+t)}{(1-t)} \left(\frac{V_{BEO} + V_E}{V_{BEO} - V_O + V_E} \right) \right] \qquad (2.28)$$

$$R_B = R_K \left[- \frac{(1+t)}{(1-t)} \left(\frac{V_{BEO} + V_E}{V_{BEO} - V_E + V_{CES} + V_E} \right) \right] \qquad (2.29)$$

$$R_B = R_K \left[- \frac{(1+t)}{(1-t)} \left(\frac{V_{BEO} + V_E}{V_{BEO} - V_{CES}} \right) \right] \qquad (2.30)$$

$$R_B = R_K C \qquad (2.31)$$

where

$$C = - \frac{1+t}{1-t} \left(\frac{V_{BEO} + V_E}{V_{BEO} - V_{CES}} \right) \qquad (2.32)$$

substituting equation (2.31) into equation (2.23)

$$\frac{V_{cc} - \overline{V_{BEon}}}{(1+t)(R_K + NR_L)} - \frac{\overline{V_{BE\,on}}}{R_K \cdot C\,(1-t)} = I_B \qquad (2.33)$$

$$R_L = R_K^2 \frac{\left[-I_B (1-t^2)\, C\right] + R_K \left[C\,(V_{CC} - V_{BE\,on})\right]}{R_K \left[I_B (1-t^2)\, C N\right] + V_{BE} \cdot N} \qquad (2.34)$$

$$R_L = \frac{C_1 R_K^2 + C_2 R_K}{C_3 R_K + C_4} \qquad (2.35)$$

where

$$C_1 = I_B (1-t^2) \qquad (2.36)$$

$$C_2 = C\,(V_{CC} - \overline{V_{BE\,on}}) - V_{BE\,on} \qquad (2.37)$$

$$C_3 = I_B (1-t^2)\, C \cdot N \qquad (2.38)$$

$$C_4 = V_{BE\,on} N \qquad (2.39)$$

$$\frac{dR_L}{dR_K} = \frac{(C_3 R_K + C_4)(2C_1 R_K + C_2) - \left[C_1 R_K^2 + C_2 R_K\right] C_3}{\left[C_3 R_K + C_4\right]^2} = 0 \qquad (2.40)$$

collecting terms

$$C_1 C_3 R_K^2 + 2C_4 C_1 R_K + C_4 C_2 = 0 \qquad (2.41)$$

and solving the quadratic equation for R_K

$$R_K = \frac{-\overline{V_{BE\,on}} \pm \sqrt{C\,\overline{V_{BE\,on}}\,(V_{CC} - \overline{V_{BE\,on}})}}{I_B (1-t^2)\, C} \qquad (2.42)$$

The positive root of (2.42) is then substituted into equation (2.24) to obtain R_B. R_L is obtained by substituting R_K and R_B into equation (2.23). The computer program is set up to provide print out of solutions for R_K, R_B, and R_L for an N and I_B as variables. If it is desired to obtain dN/R_K equation (2.33) is solved for N instead of dR_K. Equation (2.33) becomes

$$N = \frac{R_K^2 \left[-I_B (1-t^2) C\right] + R_K \left[(V_{CC} - \overline{V_{BEon}}) C - \overline{V_{BEon}}\right]}{R_K \left[I_B (1-t^2) R_L C\right] + \overline{V_{BEon}} R_L} \tag{2.43}$$

$$N = \frac{R_K^2 \left[-I_B)1-t^2) C\right] + R_K \left[V_{CC} - V_{BE}) C - V_{BE}\right]}{R_K \left[I_B (1-t^2) R_L C\right] + V_{BE} R_L} \tag{2.44}$$

where

$$C_1 = -I_B (1-t^2) C \tag{2.45}$$

$$C_2 = (V_{CC} - V_{BE}) C - V_{BE} \tag{2.46}$$

$$C_3 = I_B (1-t^2) R_L C \tag{2.47}$$

$$C_4 = V_{BE} R_L \tag{2.48}$$

$$C = -\frac{(1+t)}{(1-t)} \left(\frac{V_{BE\,Off} + V_L}{V_{BE\,off} - V_{CES}} \right) \tag{2.49}$$

Taking the derivitive of N with respect to R_K

$$\frac{dN}{dR_K} = \frac{(C_3 R_K + C_4)(2C_1 R_K + C_2) - (C_1 R_K^2 + C_2 R_K) C_3}{(C_3 R_K + C_4)^2} \tag{2.50}$$

Setting equation (2.50) equal to zero and collecting terms

$$R_K^2 C_1 C_3 + 2C_4 C_1 R_K + C_4 C_2 = 0 \tag{2.51}$$

Solving equation (2.46) for R_K

$$R_K = \frac{C_4\, C_1 \pm \sqrt{C_4^2\, C_1^2 - C_1\, C_3\, C_4\, C_2}}{C_1\, C_3} \tag{2.52}$$

$$\left[-I_B\,(1-t^2)\,V_{BE}\,R_L\right] \pm \sqrt{V_{BE}^2\,R_L^2\,(1-t^2)\,C^2 + \left[I_B\,(1-t^2)\,R_L C\right]}$$

$$\cdot \sqrt{\left[V_{BE}\,R_L\right]\left[(V_{CC} - V_{BE})\,C - V_{BE}\right]}$$

$$\left[-I_B\,(1-t^2)\,C\right]\quad\left[I_B\,(1-t^2)\,C\,R_L\right] \tag{2.53}$$

$$R_K = -\frac{\overline{V_{BE}} \pm \sqrt{\overline{V_{BE}} \cdot C\,(\underline{V_{CC}} - \overline{V_{BE}})}}{I_B\,(1-t^2)\,C} \tag{2.54}$$

R_B is obtained by substituting equation (2.50) into equation (2.24) and in turn R_B and R_K substituted into equation (2.23) for solution for N. In this case the computer program will provide solutions for R_K, R_B and N given R_L and I_B as variables.

SECTION III

LINEAR CIRCUITS

3.1 CIRCUIT ANALYSIS

The analysis of linear amplifier circuits used in the gyro and servo units is formulated to consider worst case parametric data as indicated previously.

The parametric changes affect the dc biasing stability which in turn affect the maximum linear output and gain. The dc equations show the relative sensitivity of the individual parameters which may be minimized by proper selection of components. The equations were derived by writing the network loop equations for each complete dc circuit, such as for Q_7 and Q_8 or Q_9 and Q_{10} transistor pairs in the 55-40305 gyro signal amplifier.

The solution for the quiescent bias points V_{c8} and V_{e10} permits evaluation of the maximum ac linear (unclipped) output swing, versus parametric data. The equations were formulated for exactness and ease of handling by the Data Processing Groups of GD/A Department 158-1.

3.2 CIRCUIT EVALUATION

The computer solution of the general equation was handled by separate equations for each of the parametric variables as stored inputs.

The equation for V_{c8} (Q_8 collector voltage) of the gyro signal amplifier is shown in Figure 3-1.

3.3 COMPUTER SOLUTION

3.3.1 An example of a solution for the variation of V_{c8} of Figure 3-1 versus transistor common emitter current gains $\left(B_7 \text{ or } B_8 = \frac{a}{1-a}\right)$ is shown by the computer graph of Figure 3-2. Other data are obtained by variation of each parameter in the equation of Figure 3-1 leading to a solution of total effect of all variations on circuit output.

$$V_{c8} =$$

$$V_{cc} - R_{18}\left[\frac{\alpha_8\left|V_{cc} - V_{be7}\left[1+\frac{R_{17}}{R_{24}}(1-\alpha_8)\right] - V_{be8}\right|\left|R_{22}+(1-\alpha_7)R_{23}\right|}{K\,R_{24}} + \frac{V_{be7}}{R_{24}} + S_{Ico7}\right]$$

$$S^* = \text{stability} = 1 + \frac{\alpha_8}{\alpha_7 R_{24}} \left| R_{22} + (1-\alpha_7) R_{23} \right|$$

$$\left(\frac{K + \alpha_7 R_{23} \left| 1 + \frac{R_{17}}{R_{24}} (1-\alpha_8) \right| + \alpha_7 R_{17}}{K} - 1 \right) - \alpha_7 \frac{R_{23}}{R_{24}}$$

$$K = \alpha_7 R_{17} + \left| R_{22} + (1-\alpha_7) R_{23} \right| \left| 1 + \frac{R_{17}}{R_{24}} (1-\alpha_8) \right|$$

* assume $I_{CBO7} = I_{CBO8}$

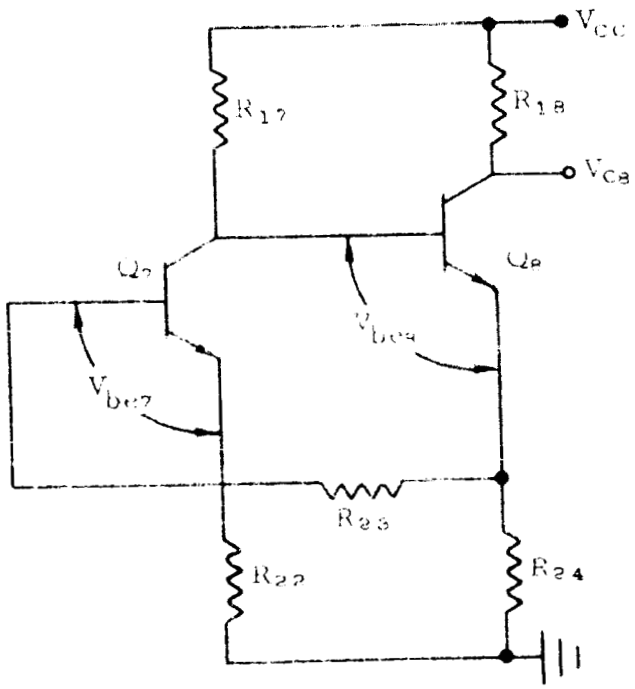

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Figure 3-1. Variation Solution

where:

V_{CC} = dc supply

V_{C7}, V_{C8} = Q_7 or Q_8 Collector Volts

V_{be7} = $0.58 - 2.12 \times 10^{-3} (T-25)$ volts = Q_7 base to emitter volts

V_{be8} = $0.62 - 2.12 \times 10^{-3} (T-25)$ volts = Q_8 base to emitter volts,

α_7, α_8 = Q_7 or Q_8 current gain at T°C (hFB)

I_{cBO_7}, I_{cBO_8} = common base collector leakage current

$$S = \frac{\Delta I_{CS}}{\Delta f(I_{cBO_7}, I_{cBO_8})} = V_{CS} \text{ stability versus } I_{cBO_7} \text{ and } I_{cBO_8}$$

T = Degrees centigrade

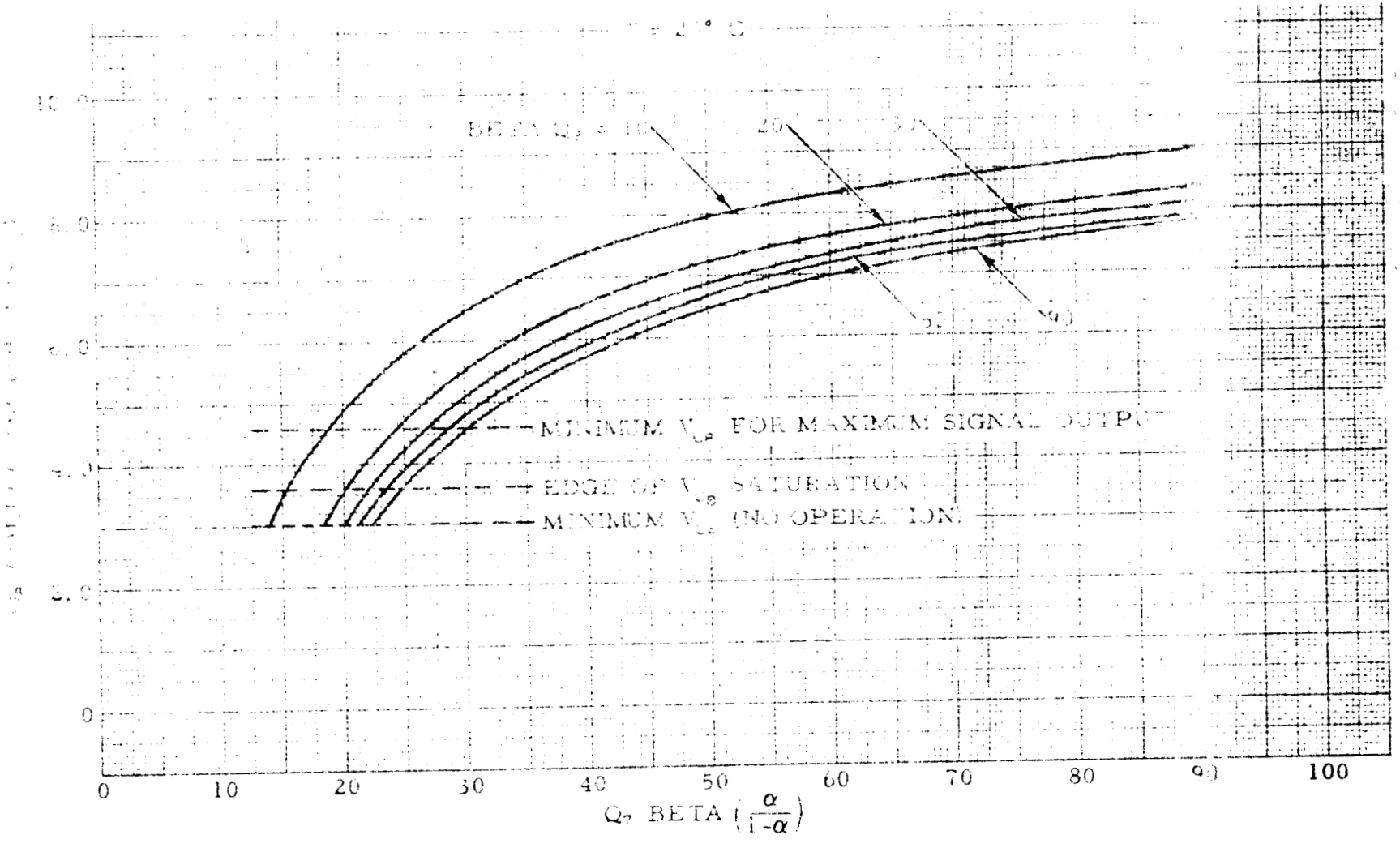

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Figure 3-2. Q_8 Collector Volts Versus Beta Q_7, Q_8

SECTION IV

AVAILABLE PROGRAM FOR SWITCHING CIRCUITS

4.1 CIRCUITRY AVAILABLE

3606	RTL Nor Circuit and RS FLIP-FLOP	Provides maximum fan out for given fan in and load resistor R_L. Provides solutions for N, R_k, and R_B.
3614 A	Inverter Circuit	Provides maximum fan out M and RB and solutions for R_B and R_k given a load resistor R_L .
3614 B	Inverter Circuit	Provides minimum collector current of driver transistor given load and fan out requirements.
3596	RTL Nor Circuit	Provides solutions for R_{Bon} and R_{Boff} given M, N, and load.
3581 A/B	Inverter Circuit	Provides plots of "on" and "off" equation given load current and V_{BEoff}.
3595 A	Unijunction Time Delay Circuit	Provides optimum solution of circuit parameter.
3594 B	Linear Amplifier Circuit	Provides minimum permissible B values over given temperature range.
3261	RTL Nor Circuit	Provides solutions for fan out given 50 different loud resistors.

SECTION V

REFERENCES

1. Switching Transistor Handbook Motorola Inc., 1st edition, 1963.

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3. Switching Circuit Optimization, Solid State Design, D. A. Pierre. Volume 3, Number 10, October 1962.

4. TRL Circuit Design Implemented By Computer, Electronic Design, C. L. Hegedus. 16 March 1964.