A REDUNDANT LOW POWER PCM TELEMETER FOR THE ORBITING SOLAR OBSERVATORY

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Summary

The Orbiting Solar Observatory Satellite developed for NASA under contract NAS 5-976, Prime Contractor, Ball Brothers Research Corp., Boulder, Colorado, requires a PCM telemeter having a very high probability of successful operation for a period of a year, in addition to the usual stringent restrictions on size, weight and power consumption. Consideration of the reliability requirements leads to the conclusion that the desired reliability only can be achieved by the use of redundancy. This paper evaluates the several approaches to redundancy in terms of the system requirements. The use of redundancy, however, is at odds with the other requirements of size, weight, and power, so that careful design using reliable miniature components and a minimum of power dissipating elements is necessary.

This paper describes the development of a PCM telemeter system consisting of a basic timing clock for all satellite functions, analog subcommutators, a digital commutator, an analog-to-digital converter and associated parallel/serial converters and modulators. Long term reliability is obtained by complete component testing, aging and selection, and by the use of redundancy at the basic component level. Both analog and digital circuits are designed using quad-type redundancy.

A new approach to analog circuit redundancy is discussed in detail. Here, as with the digital circuitry, a single transistor is replaced by a quad of transistors. The general concept is that two of the transistors in the quad remain saturated while the other two transistors perform actively. Junction shorts occurring in the active transistors cause the saturated transistors to assume the active role, while suitable feedback stabilizes gain and operating points.

The use of low-power circuitry throughout reduces thermal stress on individual components. The total result of this low power redundant design philosophy, wherein no single failure can cause a system failure, is to produce a system with an extrapolated probability of success of 0.99 for a one-year period.

Introduction

An enormous investment in terms of time, money, and manpower is represented in the launching of a satellite or similar space vehicle. Good economics dictate that the on-board electronic equipment be as reliable as possible since the space environment generally precludes maintenance and repair. Other fundamental characteristics of the ideal space electronic system are that of small size, weight and low power consumption, since booster power and primary electric power usually are limited. This paper discusses the development of a satellite born PCM telemeter in which the design, while emphasizing reliability, has tried to encompass, in some degree, the other characteristics of the ideal system.

Reliability is sought in many ways but the keystone of the reliable system must be the reliable component. It has been demonstrated that components, both active and passive, can be made extremely reliable by carefully controlled manufacturing processes and by stringent screening, aging and testing programs. Furthermore, it has been shown that a direct correlation exists between failure rates and the power dissipated in a component so reliability can be increased further by operating all components at low power levels. The use of simple, straight forward circuit design, utilizing the smallest possible number of components in the lowest power circuitry possible, and the careful culling of components certainly will reduce the number of failures to a minimum. However, such measures cannot offer an absolute certainty of equipment survival; indeed, it is a mathematical certainty that the equipment eventually will fail no matter what precautions are taken. The best that can be achieved is to provide a high probability that the equipment will survive for a stated period. When this stated period is one year, the probability of survival of conventional equipment is relatively small. For example, a system employing 500 transistors that have an average mean time between failure of 10 million hours will have a probability of survival for a

Passive or part redundancy generally is implemented by the parallel series quad configuration shown in Figure (3). The four blocks of the quad could represent individual components or circuits. A short or open circuit in any block is considered a failure of that block. The quad will fail if two series blocks short or the two parallel paths open. If the dotted connection is open there are two combinations of short circuits and four combinations of open circuits that will cause quad failure. If the dotted connection is closed there are four combinations of short circuits and two of open circuits that will cause failure. If the probability of any block failure is small for the desired mission time the probability of quad failure for the dotted connection open will be

$$P_f = 2(P_s)^2 + 4(P_o)^2 \qquad (6)$$

where P_s = probability of a short circuit $P_s \ll 1$
and P_o = probability of an open circuit $P_o \ll 1$

Similarly the probability of quad failure for the dotted connection closed is

$$P_f = 4(P_s)^2 + 2(P_o)^2 \qquad (7)$$

Transistor quad redundancy may be introduced by substituting a transistor and its associated circuitry for each block in the parallel series quad. The quad must be constructed so that at least two failures are required for quad failure. If the relative frequency of effective short or open circuits for the individual transistor blocks is known equation (6) and (7) can be used to determine the preferred quad configuration. Since it often is difficult to predict the relative probability of transistor short or open circuits they will be assumed equal, or

$$P_s = P_o = \frac{P_{f(\text{transistor})}}{2} = \frac{P_{ft}}{2} \qquad (8)$$

where $P_{f(\text{transistor})}$ is the probability of failure of a transistor and its associated circuitry. Thus from equations (6) or (7) the probability of failure of a transistor quad, $P_{f(\text{quad})}$, is

$$P_{f(\text{quad})} = 6\left[\frac{P_{ft}}{2}\right]^2 = \frac{3}{2} P_{ft}^2 \qquad (9)$$

For the assumed 2,000,000 hour mean time to failure for a transistor and its associated components and a 10,000 hour mission time, P_{ft} is

$$P_{ft} = 1 - e^{-tf} = 1 - e^{-\frac{10,000}{2,000,000}} = 1 - e^{-0.005} = 1 - 0.995 = 0.005 \qquad (10)$$

Then from equation (9)

$$P_{f(\text{quad})} = \frac{3}{2} (0.005)^2 = 0.0000375$$

If each transistor in the original 500 transistor system is replaced by a transistor quad, the quad redundant system probability of survival, P_{s4}, is the product of the individual quad survival probabilities or

$$P_{s4} = \left[1 - P_{f(\text{quad})}\right]^{500} = (1-0.0000375)^{500} = (0.9999625)^{500} = 0.981 \qquad (11)$$

Thus the introduction of quad redundancy has increased the predicted probability of success from 0.082 to 0.981. Chart (1) indicates that quad redundancy has greatly exceeded the success probability that can be obtained by assuming a ten times improvement in component failure rate with nonredundant circuitry. To obtain, a similar 0.981 predicted reliability with nonredundant circuitry would require a transistor and its associated components to have a mean time to failure of 267 million hours.

System Design

The Orbiting Solar Observatory Data Handling System is composed of four separate assemblies consisting of two digital multiplexer and encoder assemblies and two analog subcommutator assemblies. The two analog subcommutators operate continually while the digital multiplexer and encoders inputs and outputs are

Transistor and Associated Components Mean time to failure hours	Nonredundant	Circuit Redundant		Quad Redundant
		Two Circuits	Three Circuits	
1,000,000	0.007	0.014	0.020	0.9284
2,000,000	0.082	0.158	0.227	0.9814
20,000,000	0.779	0.951	0.989	0.9998

CHART 1. 10,000 Hour Predicted Reliability for Typical 500 Transistor Function System

connected in parallel with power being applied, via a command link, to only one unit at a time.

Figure 1 illustrates the system functional diagram. A digital frame consists of 32 digital channels, including 30 data channels and two frame synchronizing channels. Twenty-eight data inputs are obtained in the form of an eight bit binary code from the various satellite experiments and are read from storage shift registers. The remaining two digital inputs, representing primarily satellite housekeeping data, are obtained from 94 subcommutated analog voltages, varying from zero to five volts full scale. These voltages are encoded by the analog/digital converter into a like eight bit code and are read from the parallel to serial converter storage register when interrogated by the digital commutator. The output of the digital commutator is applied to modulators where the data is converted into NRZ and Biphase RZ Modulated PCM serial pulse trains for transmission at a rate of 400 bits per second.

System Reliability Prediction

The predicted probability of survival for the digital and analog data handled by the OSO telemeter will be calculated using the simplified method of redundant reliability prediction previously discussed. The same initial conditions, 10,000 hour mission time and 2,000,000 hour mean time to failure for a transistor and its associated components, will be assumed. A reliability prediction block diagram, Figure (2), is used to summarize the results. The reliability predictions for each block in this simplified system diagram are calculated by considering the applicable number of transistors or transistor quads, and the type of redundancy employed.

All data handled by the telemeter is word gated by the 32 channel digital commutator. Two of these channels are used to gate the analog information. The remaining 28 external digital words and two main frame synch words are of primary concern. Therefore all circuits concerned with this digital data are circuit redundant as well as quad redundant. Thus from the reliability prediction block diagram and equation (4) the reliability prediction for the digital data is

$$P_{s(digital)} = 1-(1-0.0066)^2 = 0.99995$$

Therefore the predicted reliability for over 93% of the data exceeds 0.99995.

The analog to digital converters originally were designed using quad redundancy. To meet weight and volume requirements in the digital multiplexer and encoder assemblies a redesign was necessary using some nonredundant transistors. Thus the analog to digital converters are only partially quad redundant and circuit redundancy is used to increase the analog information predicted reliability. Since the digital circuits must survive to obtain a serial PCM output, the predicted reliability for either assembly is

$$P_s = P_{(A/D\ converter)} \times P_{(digital)}$$
$$P_s = 0.7000 \times 0.9934 = 0.6954$$

From equation (4) the predicted reliability for the circuit redundant configuration is

$$P_s = 1-(1-0.3046)^2 = 0.907$$

The analog subcommutators are quad redundant with the exception of the first tier of the analog input switches. However sufficient redundancy is designed into the switch banks so that in the worst case, a single failure can only disable seven other analog inputs. This was felt to be sufficient redundancy, since the analog data is but a small portion of the total information processed. Appropriate allowances are made for this individual channel nonredundancy in the analog commutator reliability prediction. Thus the predicted reliability shown in Figure (2) is for any one analog input. A particularly important data source may be connected to several separate inputs to increase its probability of survival. From the above the reliability prediction for any analog input is

$$P_{s(analog)} = 0.977 \times 0.907 = 0.886$$

Digital Circuit Design

The primary digital design requirements for the OSO telemeter were low power and simplicity of redundant circuit design. To achieve these goals, the digital circuits utilize transistors of alternating conductivity types to minimize passive power dissipating elements. Thus the collector of a PNP transistor is connected directly to the base circuit of an NPN transistor and this NPN may be connected to a succeeding PNP. Power consumption is reduced since a transistor collector need only supply current drive to the base of the succeeding transistor of the opposite conductivity type. Therefore in a logic sequence either all the transistors are conducting or not conducting. The logic is arranged so that the duty cycle of conducting periods is minimized, thereby reducing supply drain since at any time most transistors are in the off state with only leakage currents flowing.

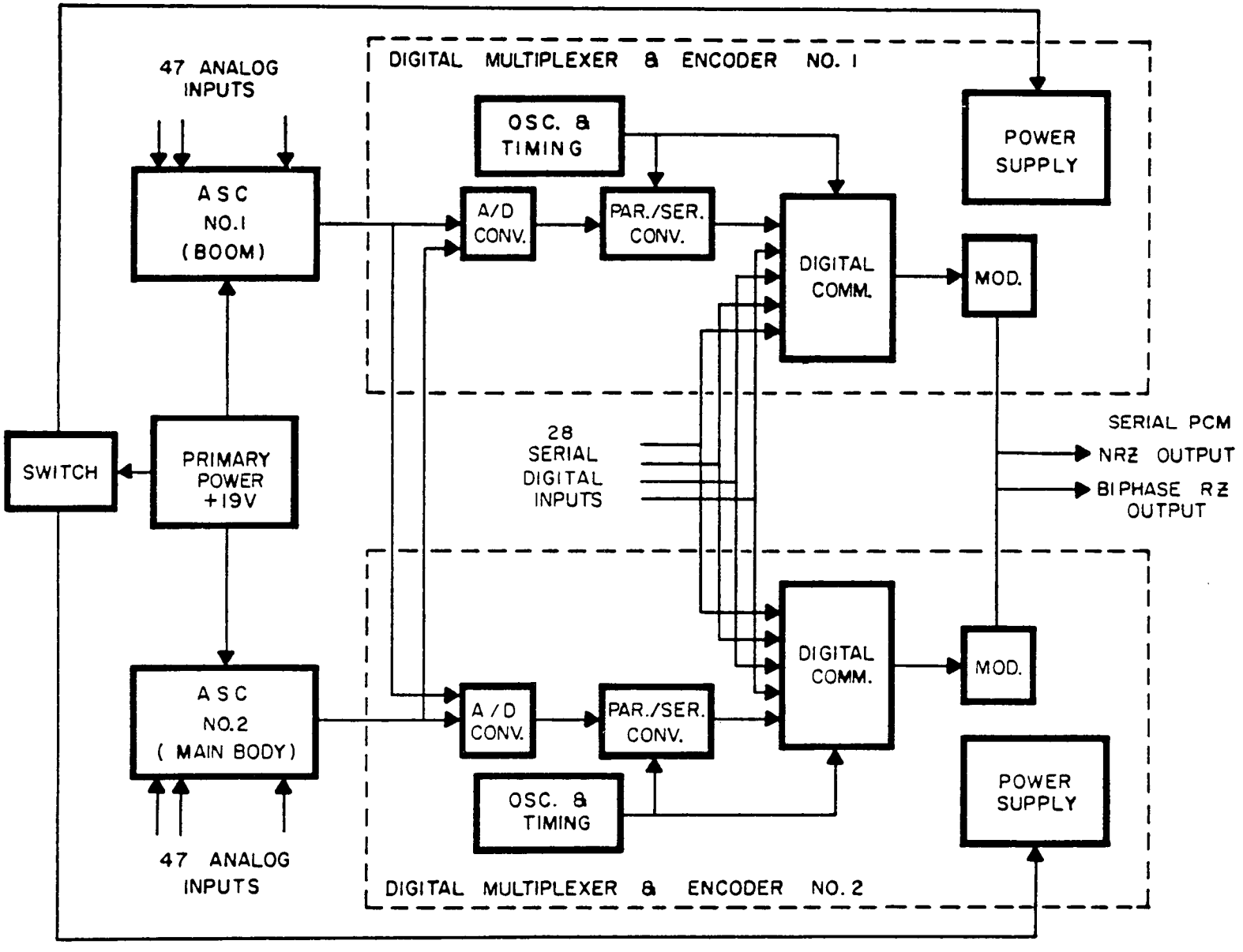
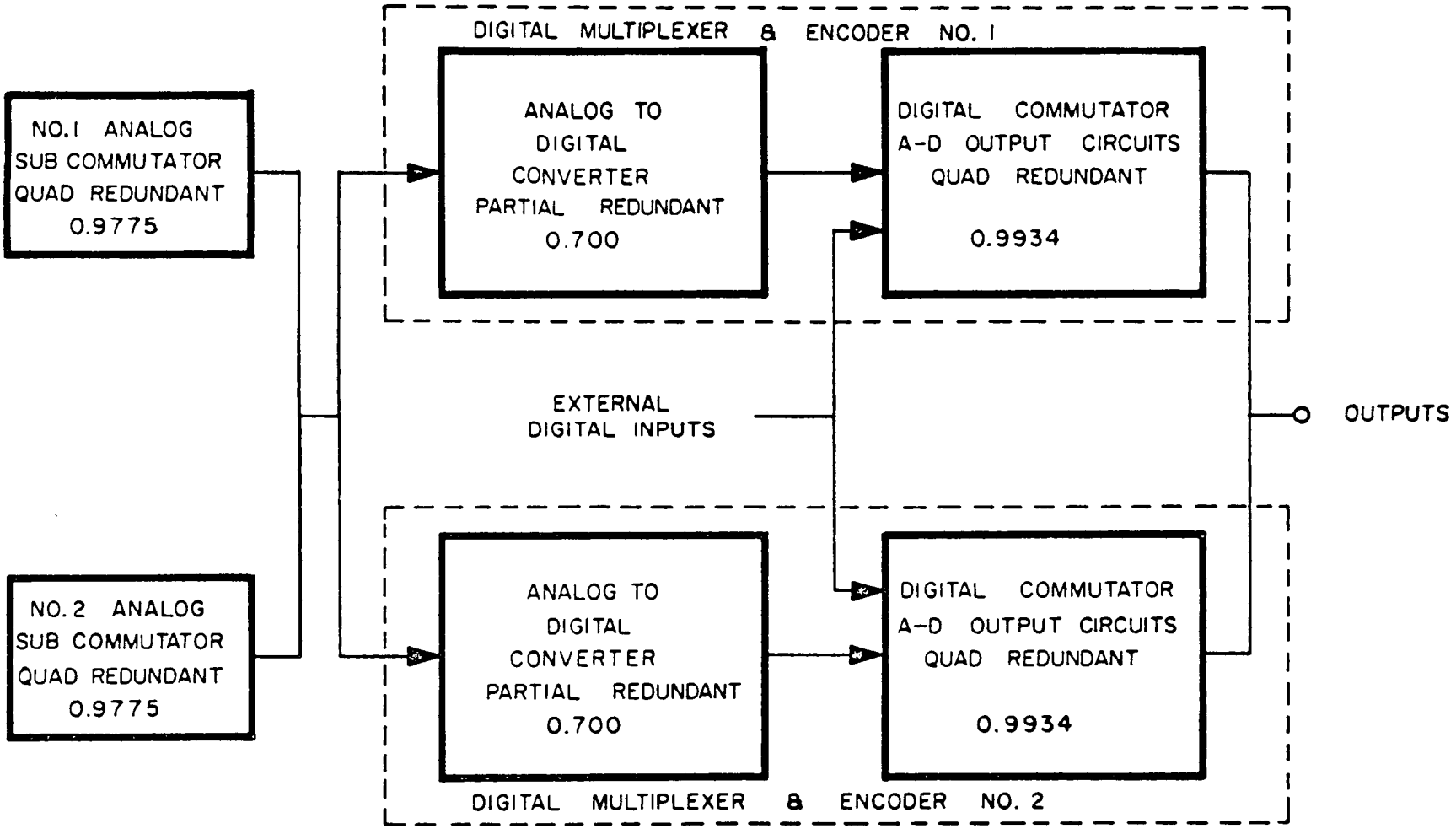


FIGURE 1 OSO-2 TELEMETER SYSTEM FUNCTIONAL DIAGRAM



NO. 1 & NO.2 DIGITAL MULTIPLEXER & ENCODERS CONNECTED IN CIRCUIT REDUNDANT CONFIGURATION

FIGURE 2 RELIABILITY PREDICTION BLOCK DIAGRAM

Low power dissipation is achieved in applications where a low impedance output is required in both logic states by providing a complementary symmetry output. Since the off transistor acts as a collector load for the conducting transistor, the only internal power dissipated is in the base circuit. Since transistor circuitry is essentially current operated it follows that power consumption is also reduced by minimizing the number and magnitude of supply voltages. The relatively high conducting base emitter voltage drop in silicon transistors permits the elimination of turn off bias supplies. Careful selection and testing of components permits design to closer tolerances thereby reducing power consumption. All transistors are specified for high gains at low collector currents.

As a typical example of low power digital circuit design a nonredundant bistable circuit of the type used throughout the OSO telemeter as a flip flop or binary is shown in Figure (4). The basic flip flop is of the symmetrical four transistor complementary high efficiency type containing two NPN and two PNP transistors. Each transistor acts as a collector load for, and to supply base drive current to a transistor of the other type. Thus diagonally opposite transistors are either off or saturated. Besides eliminating unnecessary dissipating elements this flip flop has the advantage of producing an output which approaches the supply voltage values and has a very low impedance in either state. Thus, it is possible to drive either or both NPN and PNP transistors directly from the flip flop output without the need for any additional supply voltages or intervening inverting elements. The usual method of designing low power circuitry uses high value collector resistive elements. The large time constant formed by these resistors and the transistor junction capacitances precludes high speed operation. The complementary flip flop also achieves low power operation but at very low impedance levels, therefore the circuit speed is limited only by the transistor itself. The base capacitors permit relatively large transient current loads during switching, although the quiescent currents are small. The capacitors in the base circuit may be eliminated if a large transient load or high speed operation is not required. The complementary flip flop may be base or collector triggered with either polarity trigger pulses. This trigger versatility further simplifies digital circuit design.

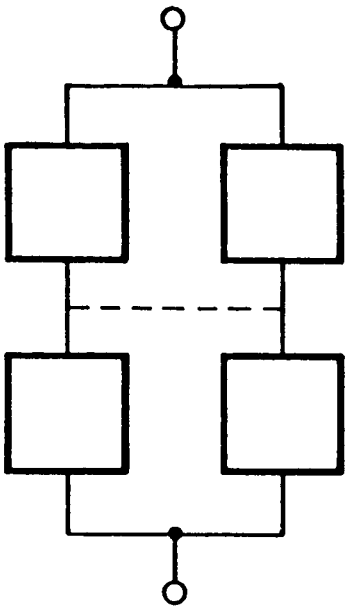
Electronic circuits may be made quad redundant by the direct substitution of quads for each component in the original circuit. Capacitors and diodes are substituted on a quad basis since the failure mode may be either open or short. The carbon composition resistors are only paralleled, however, since these resistors are assumed not to fail by shorting. Transistors may be made quad redundant by the direct substitution of a transistor quad with isolated base circuits. Each transistor in a quad must be capable of supplying the total load requirements.

The complementary flip flop can be made redundant by the direct substitution of the transistor quad shown in Figure (5). Figure (7) shows the redundant flip flop divided into two series redundant halves. The output points A - A' and B - B' are connected for fully redundant operation, however, these points are not permanently connected until just prior to final tests. This technique also is used in all quad redundant circuits to ensure that all components are operating before the final interconnections are made. The operation of this 16 transistor redundant flip flop in the event of component failure may be described as follows. All failures will be considered for one series leg of any quad. Any component or transistor junction open circuit will cause the affected series leg to become inoperative and the load will be absorbed by the noneffected parallel leg. A collector-emitter short will have little effect since the remaining series transistor will not be affected by this short, because its base is independently connected to the low impedance output connection. The base-emitter short effectively will cause the transistor to open circuit and operation will continue on the parallel leg. A collector-base short effectively will open the leg during saturated operation with the load being assumed by the parallel side. The remaining series transistor will ensure the affected leg is open when the quad under consideration should be off. A capacitor short will have little effect since the capacitors are series redundant.

As an example of low power redundant operation a 16 transistor flip flop may be capable of supplying 250 microamperes to a resistive load and several milliamperes to a transient load during a switching time of 250 nanoseconds and still consume less than 250 microwatts from a three volt supply.

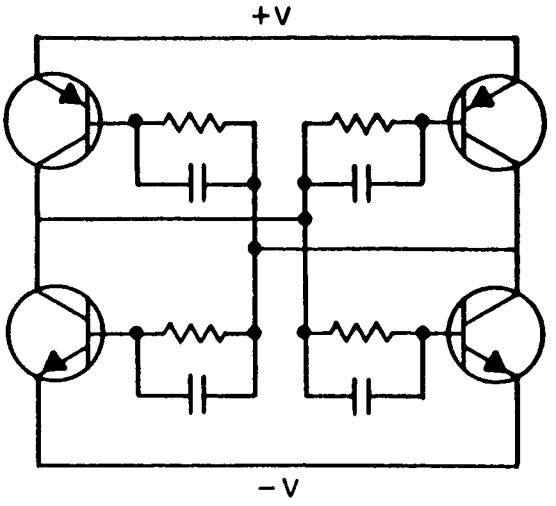
Analog Circuit Redundancy

The normal method of achieving redundancy in analog circuits uses circuits in standby, which are switched into operation when and if the main circuit fails. This method involves a main circuit, one or more standby circuits, a failure detecting circuit and a switching circuit. Failure detection may take many forms; one common method is that of output D-C level detection,



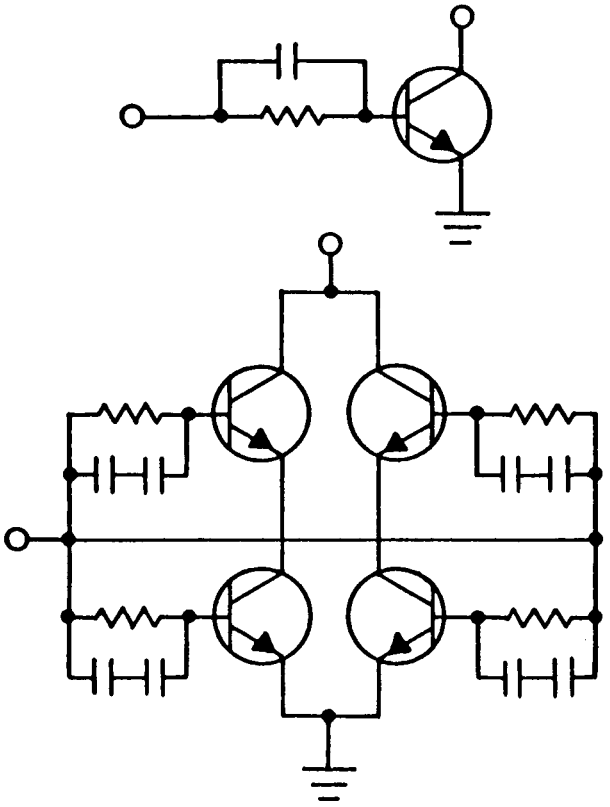
PARALLEL SERIES
QUAD CONFIGURATIONS

FIGURE 3

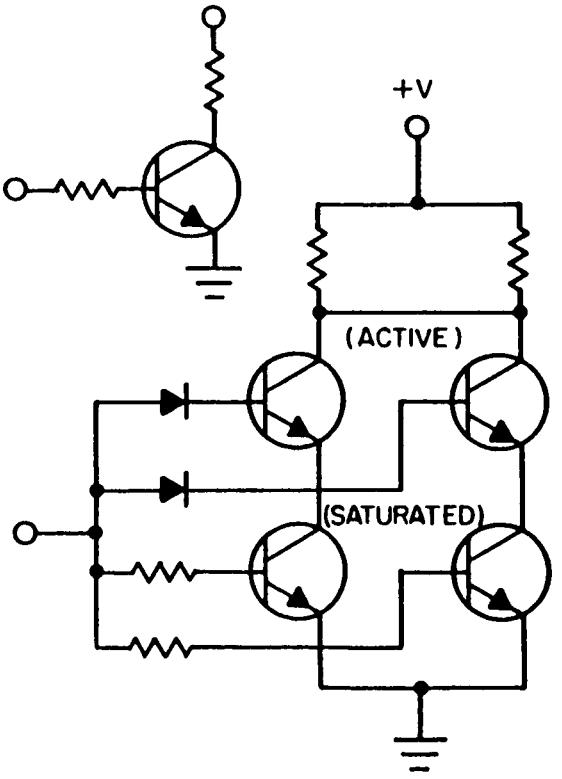


NON-REDUNDANT
FLIP-FLOP

FIGURE 4



DIGITAL REDUNDANT QUAD
FIGURE 5



ANALOG REDUNDANT QUAD
FIGURE 6

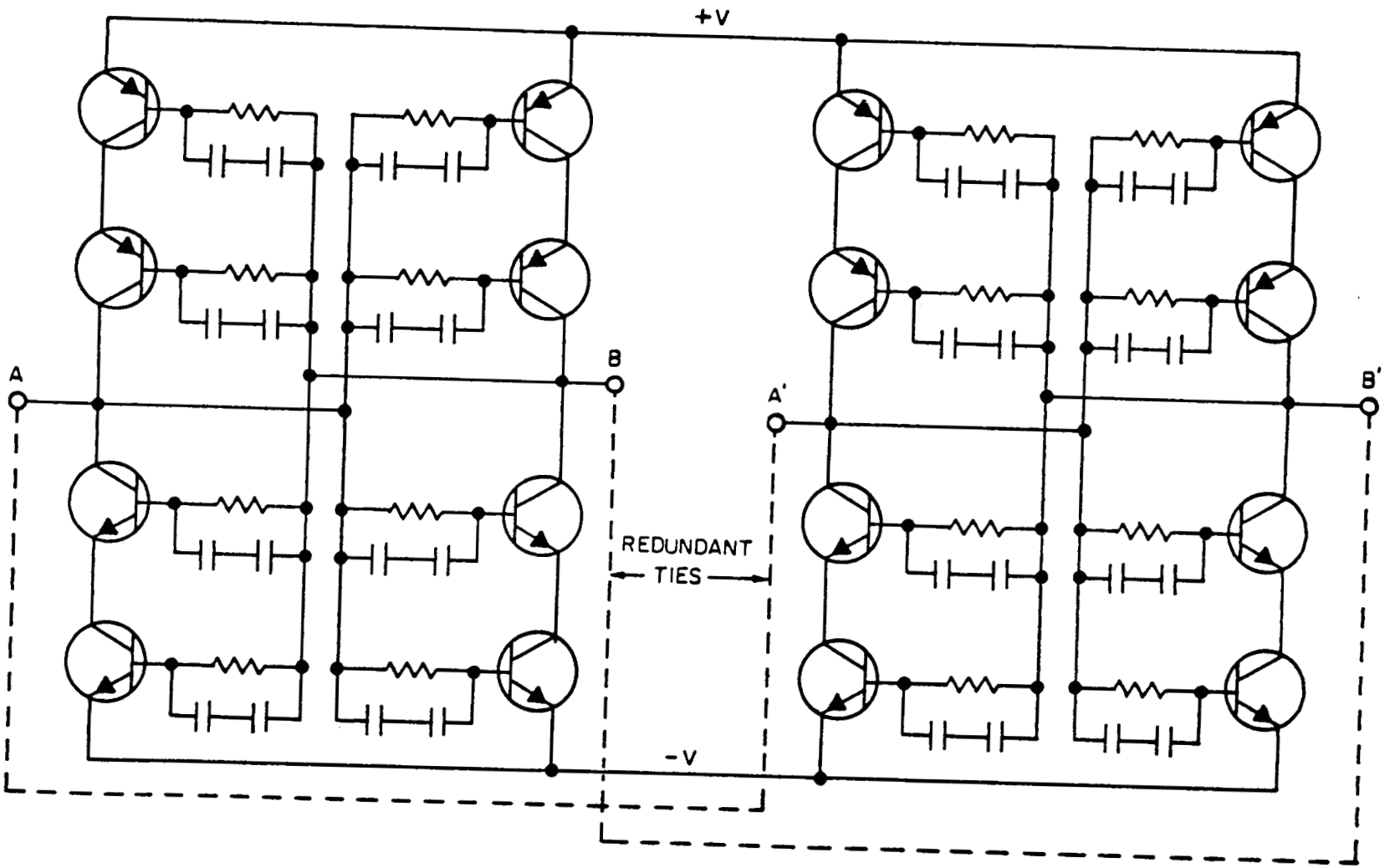


FIGURE 7 REDUNDANT COMPLEMENTARY FLIP – FLOP

where the failure of any component causes the D-C level to behave in a pre-determined manner. A second method of failure sensing is that of carrier detection, where a constant amplitude high frequency carrier is added to the normal signal input. The high frequency carrier is filtered and detected at the circuit output and is used to control a standby circuit switching mechanism. Another analog redundancy technique, primarily confined to amplifiers, is that of majority comparison. A typical system would use three identical amplifiers, with only one amplifier connected to the output load. Logic networks compare all amplifier outputs and only an amplifier having an output which agrees with the majority output is connected to the load. Still another method uses two or more circuits connected in parallel with power switched to "good" units and away from failed units. Failure sensing is done at the ground station and the power switching is accomplished via a command link.

All of the above redundancy techniques have the disadvantage of requiring a more or less complicated failure sensing circuit and a circuit switching device. For this system, a simpler, passive type redundancy was desired. A passive or nonswitching redundancy uses components in such a way that the components or portions of the circuit that have not failed are used and the component or circuit portion that has failed is ignored. A technique of redundant analog circuit design was developed which is quite similar to that of digital circuitry; namely, that a single transistor is replaced by a quad of transistors. The general concept is that the two bottom transistors in the quad are biased to remain normally saturated while the two top transistors perform actively (See Figure (6)). Junction shorts occurring in the active transistors cause the normally saturated transistors to assume the active role. The analog circuit is further divided into right and left halves. Any open failure or any emitter-base shorts will cause the nonaffected half to assume the load. Suitable feedback stabilizes gain and operating points.

The detailed circuit schematic of a quad redundant buffer amplifier is shown in Figure (8). The amplifier specifications are an input impedance of 100 K ± 1%, unity gain ±0.25% and output impedance less than 100 ohms, over all environmental conditions. In addition, voltage gain and input impedance should vary less than 1% as a result of any component failure. The basic circuit is that of a standard operational amplifier having a voltage gain approximately equal to R2/R1 and an input impedance approximately equal to R1. The voltage amplifying transistor quad consists of transistors Q1 through Q4 and the emitter follower quad is Q5 through Q8. As with all redundant analog circuits used in this system, the amplifier is divided into right and left halves. For clarity, the component numbers of the passive elements associated with the right half are primed, while their opposite number in the left half are unprimed.

Transistors having relatively high gains at low current levels have been used; for the N-P-N's, typically h_{fe} = 100 at D-C current levels of 100 microamps. Transistor bias currents, as determined by R6, R6' and R7, R7' are such that the quad transistors Q3, Q4, Q5 and Q6 are saturated. The D-C feedback, as determined by R_2, R2' and R_5, R5' causes Q1, Q2, Q7 and Q8 to operate in the active region. Input, feedback and bias resistors for each amplifier half are so isolated that faults in one half of the amplifier will not at all affect the operation of the other half. This buffer is used to amplify low impedance positive pulses varying from zero to five volts. Input resistors R_1 and R1' convert the input signal to a current, which is applied identically to right and left amplifier halves through the transistor base diodes CR1 and CR1'. A small amount of signal current is shunted through resistors R6 and R6' into the base of the saturated transistors but this shunt current is maintained small and constant. Trimming of the feedback resistors R2 and R2' compensates for this signal loss. Open loop amplifier gain is made large by using specially specified and selected transistors which have high current gains at low collector currents and by utilizing very large value collector load resistors. The large open loop gain causes the closed loop gain to be very nearly equal to the ratio of the feedback resistors, in this case R2 and R2' over R1 and R1' respectively.

The operation of this circuit in the event of a transistor failure may be discussed in general terms as follows:

Collector-Base and Collector-Emitter Short. It will be assumed that these faults occur in transistor quad Q1 through Q4, noting however that the circuit performance is typical of the second quad as well. These particular junction shorts, if sustained in transistors Q3 (or Q4) have relatively little effect on circuit operation since these transistors are already operated in the saturated mode. The open loop gain will tend to increase somewhat since the emitter degeneration normally present on the active amplifying transistor is lessened due to the reduced saturation resistance in Q3 (or Q4). Likewise, the same junction shorts occurring in the active transistors

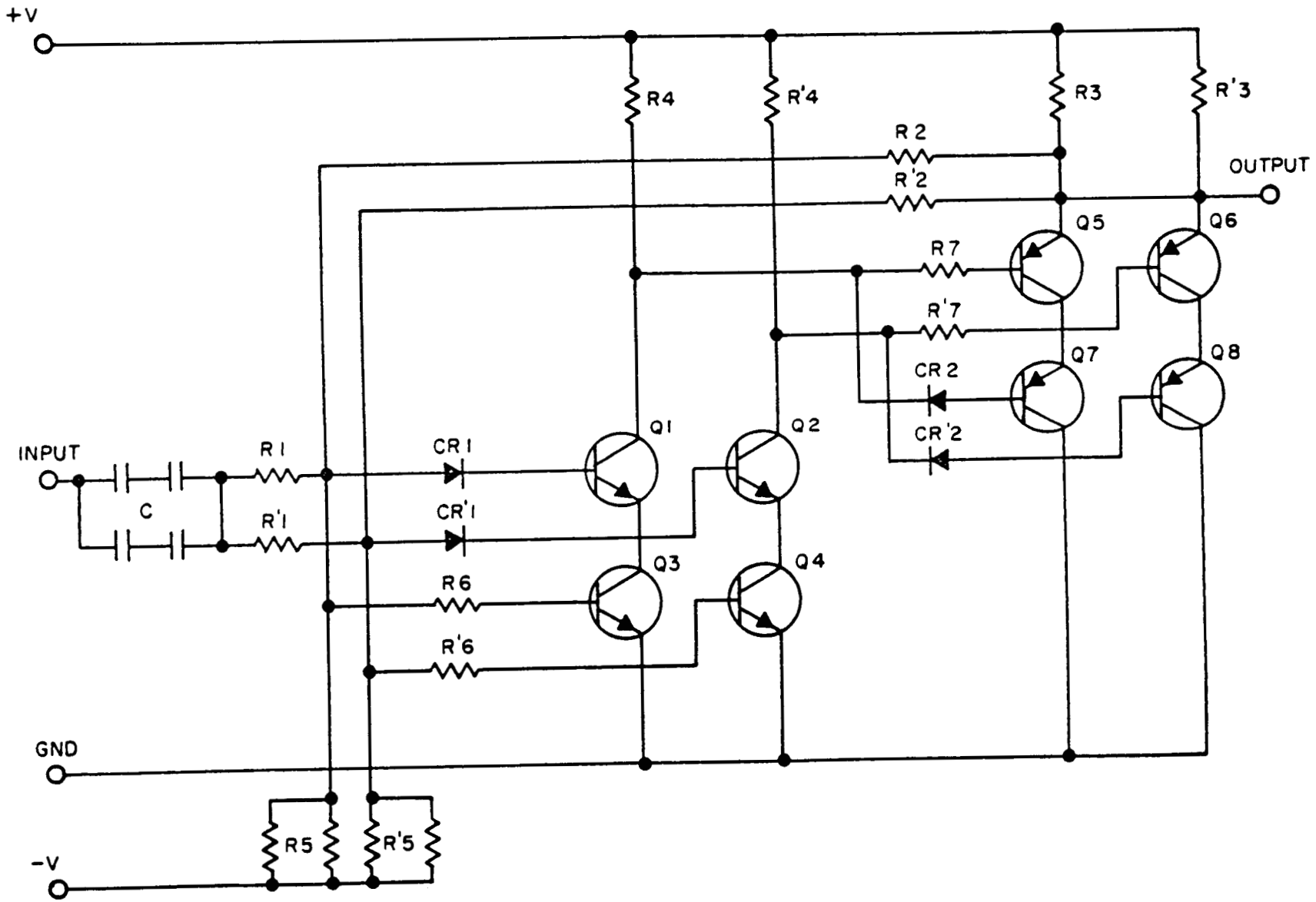


FIGURE 8 REDUNDANT BUFFER AMPLIFIER

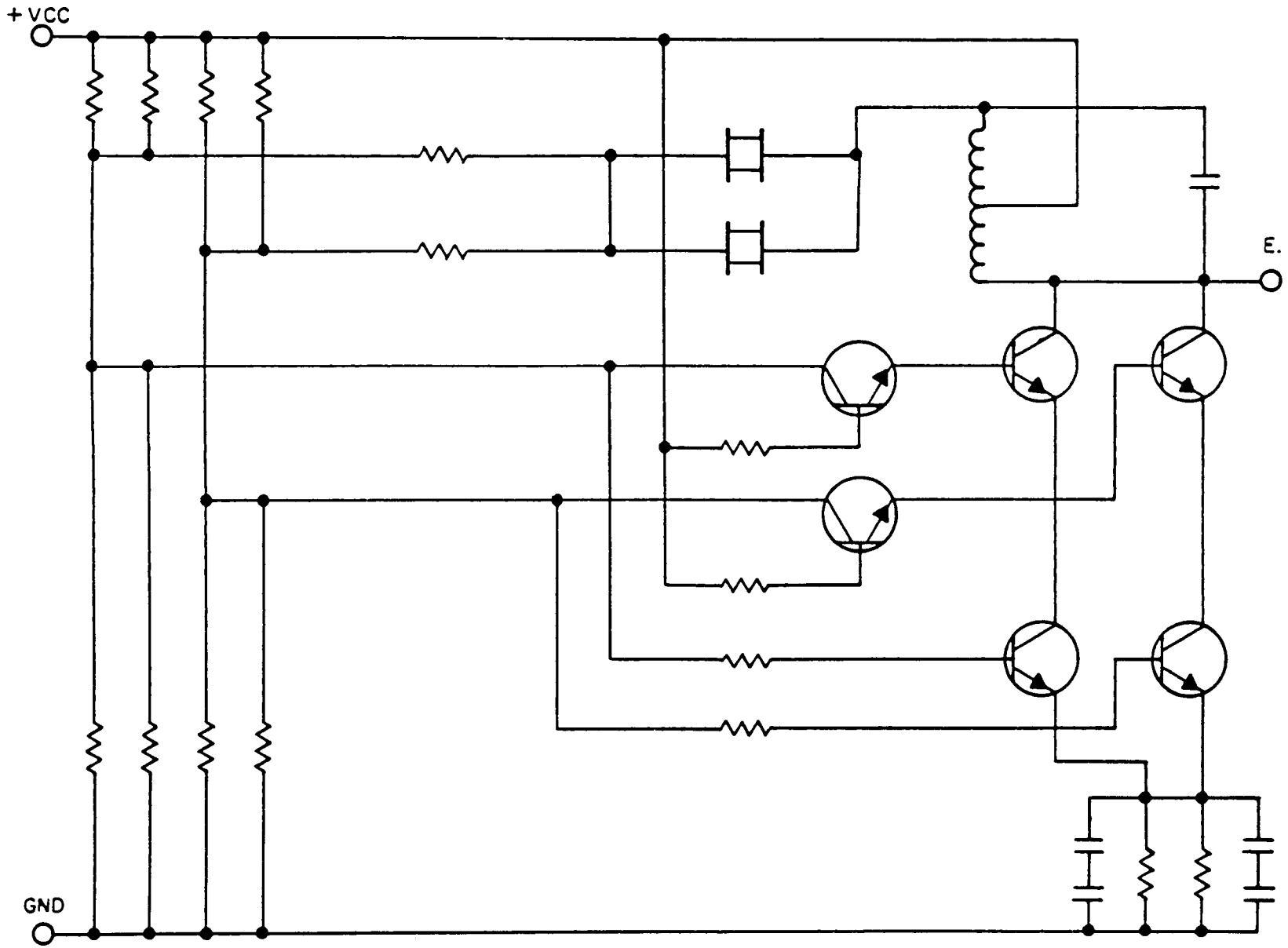


FIGURE 9 REDUNDANT CRYSTAL OSCILLATOR

Q1 (or Q2) effectively short circuits these transistors and the normally saturated transistors are caused by the D-C feedback to assume the active role. Open loop gain tends to be reduced by the base resistors R6 and R6' but this is more than compensated for by the absence of emitter degeneration. The diode in the base circuit of Q1 becomes reversed biased in the presence of these shorts, which helps maintain a stable operating point and also prevents the loss of signal current through the inactive transistor.

Base-Emitter Shorts and Transistor Opens. A short circuit across the base and emitter junction of a transistor effectively will cut it off and make it appear as an open circuit. In this, and in any actual open circuit case, the entire amplifier side becomes inoperative and the load is entirely absorbed by the nonaffected side.

Sufficient latitude is designed into the circuit so that any coupling capacitor or bias resistor may fail without significant degradation of performance. The sole exception is the input resistor R1. An open resistor in this part of the circuit will cause a direct change in gain and input impedance, and therefore, the degree of redundancy obtained will be a function of the number of resistors paralleled.

The major considerations in the buffer amplifier circuit design were accuracy and stability; consequently, very high gain, relatively slow transistors were used. However, a different problem arises when it is desired to amplify narrow pulses at a fast repetition rate. If fast diodes are used in series with the transistor bases to protect against the effects of collector-base shorts, it is possible that the diode will turn off before all the stored charge is removed from the transistor base. This results in relatively slow rise times since the storage charge must be removed by recombination. One solution is to use very slow diodes, but at times it is difficult to match the transistor and diode turn-off times over wide ambient temperature variations. Another method is use saturated transistors in place of the diodes. These transistors are specifically chosen to have high forward gain and very low inverted current gain. Under normal operating conditions the saturated transistor switch can be considered as a small resistance and the storage charge in the amplifying transistors can effectively be removed. In the event of a collector-base short in transistors Q1 or Q2, the saturated switch will then operate in the inverted condition. Because of the low inverted current gain the transistor becomes unsaturated and very little degenerative feedback will be transmitted back to the new active transistor Q3 (or Q4).

The buffer amplifier described is representative of the class of analog quad redundant circuits designed for this PCM system. Other circuits are comparator amplifiers, frame sync amplifiers, crystal oscillator, voltage references, power converters and regulators. The schematic of another passive redundant circuit, a crystal controlled oscillator is shown in Figure (9). Any transistor junction short or open will not cause the frequency to shift by more than one cycle per second or the amplitude to vary by more than 10%.

Fabrication and Testing

It has been stated that high system reliability has been sought by component redundancy, and by a low power design philosophy which results in components operating at a low use-to-rated stress ratio. However, these design techniques do not eliminate the necessity for ensuring the use of high quality components. Therefore, the parts used in the Orbiting Solar Observatory are subjected to rigorous aging and testing.

Each active component destined for system use is serialized uniquely at the time of receipt. The part then is tested and parameters appropriate to its ultimate use are measured. It is then placed in aging racks, where it is aged in circuits closely resembling the actual conditions of use, for periods ranging from one to four months. During, and immediately following the aging process, the component is re-tested and the results are compared to previous test results. Any significant change in parameters causes the component to be rejected.

Besides performing a quality check on all components, this testing procedure provides the actual parameter distribution curves on which circuit design is based. Placing individual, serialized components in specific usage categories makes it possible to design to much tighter tolerances, since the worst case design philosophy is now based on the definite knowledge of the actual worst case. Thus, the final circuit design is based on detailed knowledge of the actual components, rather than on typical production distribution curves. It is therefore possible to design more closely to the end point limits, and consequently, it is possible to attain lower power circuits than would be the case if the full manufacturing range had to be accomodated.

Following the post-aging testing, the components are assembled on printed circuit boards. At the time of assembly all parts are identified according to serial number and circuit location. This record is maintained so that it is possible at any later date to correlate circuit board test results to individual component test results, so as to check against possible damage incurred during the assembly process.

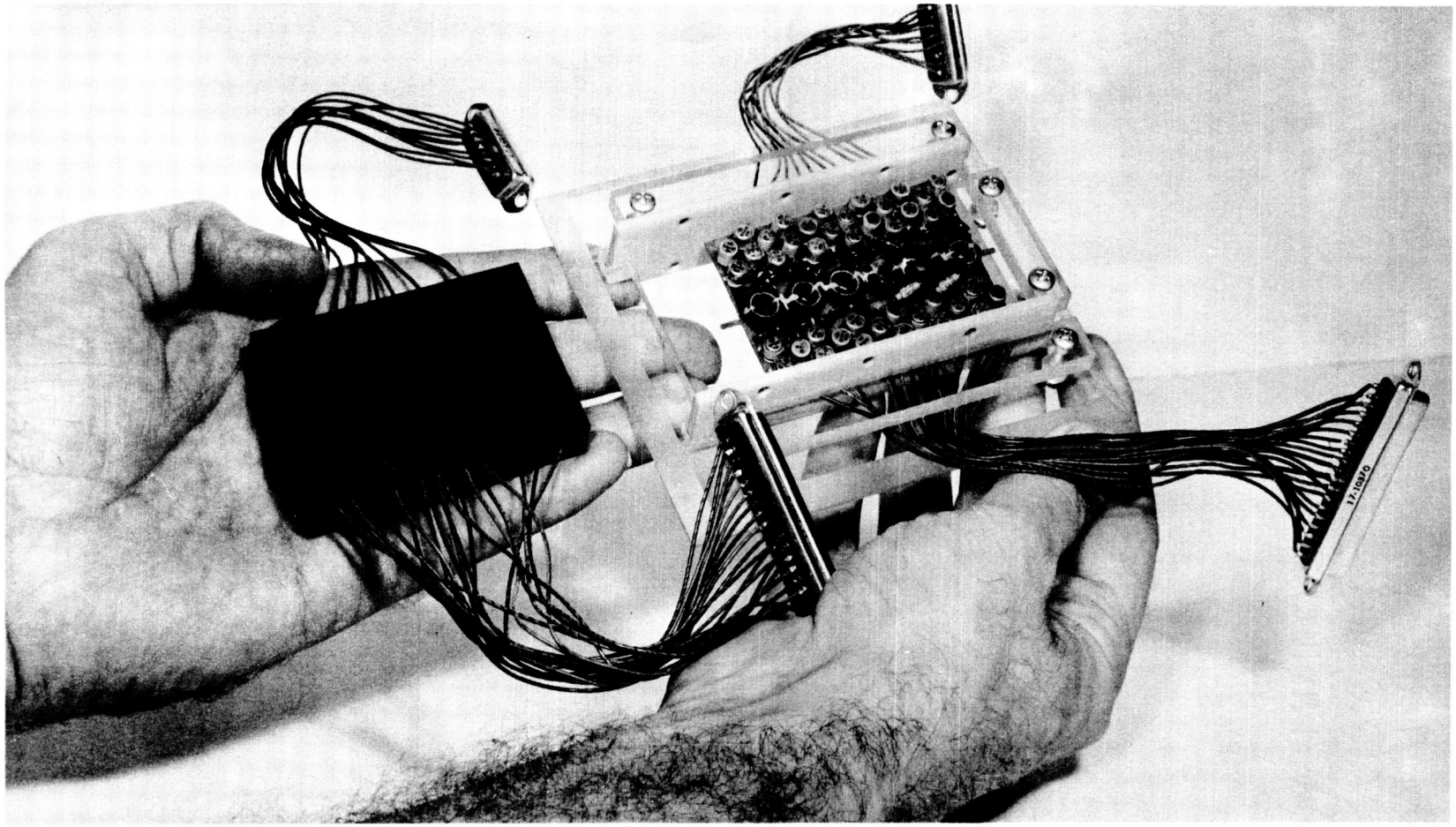
Low power circuit design permits the use of very high density packaging in the printed circuit modules. Figure (10) shows the completed assembly of a typical circuit board, and Figure (11) is the module after encapsulation. Prior to encapsulation the module is subjected to a functional test in which the actual circuit performance is observed. After encapsulation the functional test is repeated. The unique character of component redundant circuits makes mandatory this continuous step-by-step testing during the system assembly process. To derive the full benefits of redundancy it is necessary that the system be shipped with all components functioning. Testing this is difficult because in a fully redundant system it would be almost impossible to perceive that a component has been damaged in assembly without this continuous assembly testing. One testing technique that has worked well is to design circuits in parallel halves with easily removed connectors completing the redundant connection. In this way each parallel half of the redundant circuit may be checked on a "go-no go" basis merely by determining if the circuit operates or not. It is more difficult to check that a member of the series pair within the parallel half of the circuit is still operative. To check this, the module must be probed at the midpoint of the quad leg for proper waveforms during the functional test.

Figure (12) illustrates the final assembly of the encoder and analog subcommutator packages. The encapsulated modules have been stacked and the interconnection wiring has been completed between module pins on top of the assembly. At this time it is still possible to check a good deal of the redundancy since the last connections to be made are those closing the parallel halves. After this test the final connections are made which transforms the telemeter into a completely redundant entity, and thereafter, no single component failure can be identified on the basis of a system test.

Conclusions

Based on generally accepted statistical analysis and component failure rates it is apparent that weapon systems of vital import and space missions of extremely long duration require that some form of redundancy be used to satisfy reliability requirements.

Attainment of reliability through redundancy however is costly. Increases in terms of materials, size, weight, power, and design and testing time are proportional to the degree of redundancy and reliability desired. It may be generalized that the aforementioned system parameters are increased by factors of approximately 2.5 and 5.0 for circuit and quad redundancy, respectively. Certainly redundancy is not an across the board panacea for all electronic ills and it should be used with discretion only after a careful weighing of all considerations. Nevertheless, until a substantial increase in proven component reliability is achieved, redundancy appears to be the best approach to the attainment of high reliability in electronic systems.



FIGURES 10 AND 11 - PRINTED CIRCUIT BOARD AND ENCAPSULATED MODULE

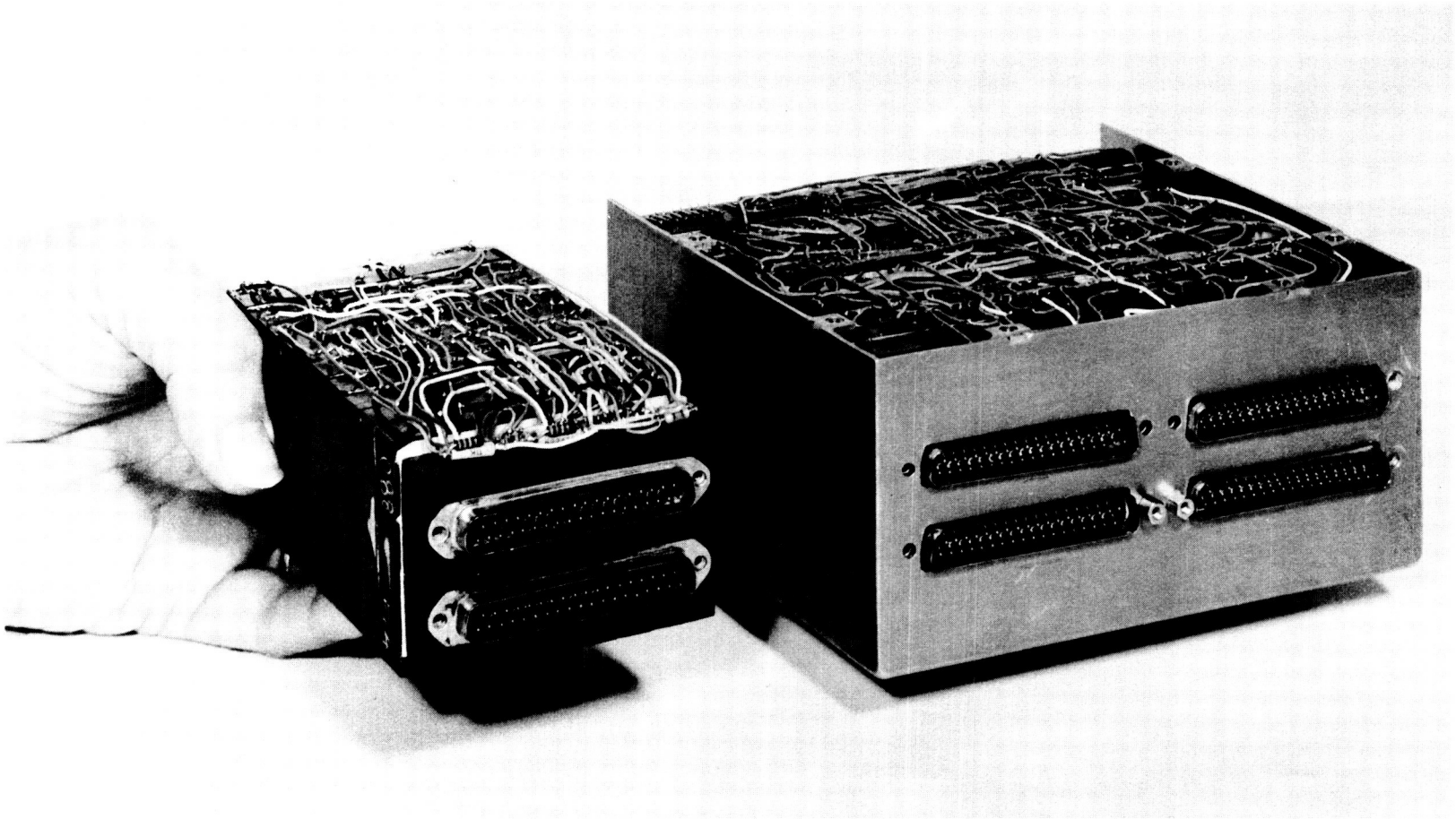


FIGURE 12 - COMPLETED ASSEMBLY, ANALOG COMMUTATOR AND DIGITAL ENCODER

period of one year of 0.65; that is, 1 out of 3 missions will fail.

Certainly, some dramatic action must be taken to increase the reliability of the equipment. This action may consist of the introduction of redundancy. Many forms of redundancy may be used in electronic systems. In general, redundant systems may be classified as active or passive. "Active", or "circuit", or "block" redundancy denotes a system requiring a fault detecting mechanism and a switch which switches out the faulty portion and switches in the redundant portion. Passive redundancy denotes a system in which the reserve elements are connected in such a way that failure of an element does not affect the operation of the system. Quad redundancy is an example of such a system. This type of redundancy generally requires more components than those which employ an active switching redundancy, but active redundant systems have the inherent disadvantage of requiring a complicated failure detector, and in addition have a finite time delay between the sensing of a failure and the replacement of the faulty element.

This paper will explore the predicted reliabilities of various types of electronic systems, including nonredundant, active redundant and passive redundant; and then concentrate on the development of a PCM telemeter for the S-17 Orbiting Solar Observatory satellite using a quad redundant, circuit design approach.

Redundancy Reliability Predictions

The predicted probabilities of survival of part, circuit and nonredundant configurations for a typical transistorized satellite telemeter will be compared to demonstrate their relative reliabilities. For this comparison a basic system consisting of 500 transistors will be assumed, since a nonredundant version of the OSO telemeter would require approximately this number of transistor functions. The probabilities of survival will be calculated for a 10,000 hour, or approximately 400 day, mission. To simplify the calculations these reliability predictions will be based on an assumed combined mean time to failure for a transistor and its associated components. This combination of failure rates is justified on the basis that the failure rate of a typical transistor is usually an order of magnitude greater than the combined failure rate for its associated passive components. An assumed mean time to failure of 2,000,000 hours for a transistor and its associated parts is postulated, based on the quality of parts used, derating, and environmental conditions encountered in the OSO. Since it is difficult to attach a high degree of confidence to any assumed mean time to failure of this order these calculations are intended to show the relative rather than the absolute advantages of various forms of redundancy. For comparison the predicted probability of survival for one half and ten times the assumed mean time to failure will be tabulated in Chart (1).

In calculating the probability of survival for a system containing a large number of components it usually is assumed that the failure distribution of any type of component is exponential. With this assumption the performance of a given component can be characterized by a mean time to failure or a failure rate. If a system contains n components with a failure rate of f per hour it is expected statistically that there will be (n f) failures per hour, or (t n f) failures in t hours. If the failure probability is assumed random and any failure causes system failure the probability of survival, P_s, for the system is

$$P_s = e^{-tnf} \qquad (1)$$

Thus for the previously assumed nonredundant system the predicted probability of survival is

$$P_{s1} = e^{-\frac{10,000 \times 500}{2,000,000}} = e^{-2.5} = 0.0821 \qquad (2)$$

An active, or circuit, redundant system could consist of two or more complete nonredundant telemeters connected such that each system could operate independently. The two digital multiplexer and encoder assemblies shown in Figure (1), are an example of circuit redundancy. The probability of failure, P_f, for two such systems capable of being switched by an assumed nonfailing circuit is the product of their individual failure probabilities. Since for any situation

$$P_s + P_f = 1 \qquad (3)$$

the probability of survival, P_{s2}, is

$$P_{s2} = 1 - P_{f1}^2 \text{ where } P_{f1} = 1 - P_{s1} \qquad (4)$$
$$= 1 - (1 - P_{s1})^2$$
$$= 1 - (1 - 0.0821)^2 = 0.158$$

Similarly for three parallel telemeters where only one is required to survive for successful operation the predicted probability of survival is

$$P_{s3} = 1 - P_f^3 \qquad (5)$$
$$= 1 - (1 - P_{s1})^3 = 0.227$$

It may be noted that this type of redundancy does not increase the chance of mission success materially unless the individual blocks themselves have a very high chance of success.