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ALL-MAGNETIC PCM TELEMETRY: A REVIEW OF THE SYSTEM BREADBOARD

by C. H. Heckler, Jr., and J. A. Baer

Prepared under Contract No. NAS 1-3380 *by*
STANFORD RESEARCH INSTITUTE
Menlo Park, Calif.
for Langley Research Center

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ABSTRACT

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The breadboard design and fabrication techniques used in Phase II have been reviewed and the packaging of the basic magnetic logic circuit has been found to be the major problem. The interrelationships between the circuit performance and the mechanical design have been determined and a planar-circuit mechanical design has been made. A reliability estimate of the probability of success of a five-year mission of 88 percent has been made. A single circuit--the tuning fork oscillator--has been found to make a significant contribution to the system failure rate. The replacement of this circuit with a more reliable one results in an increase to 92 percent for the probability of success. The characteristics of the pressed toroidal stopper cores as well as the factors determining the limit in the possible number of analog channels are also discussed.

Author

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I INTRODUCTION

The feasibility of applying all-magnetic-logic techniques to realize a high-reliability data-handling system has been investigated in three phases. In the first phase[1]* the application of several all-magnetic logic circuits was evaluated in view of the special requirements imposed by a 12-channel PCM Telemetry System. This led to the conception of several new circuits which had characteristics more nearly ideal for this application. Based upon these circuits, a logic design for a 12-channel PCM Telemetry System was completed. In the second phase[2] this basic design was used for a feasibility breadboard. In the construction of this breadboard more extensive problems than had been anticipated were encountered. These problems centered principally around the packaging of the basic circuits. This packaging technique, which had been designed to facilitate circuit modifications, turned out to be near the ideal for the circuits used--when a good circuit assembly was achieved--but difficult to make and more difficult to maintain in a suitably good condition. This resulted in the late completion of the construction of the breadboard and the full testing originally planned was not achieved. In the third phase, the subject of this report, effort was to be directed toward the following:

(1) A review of the breadboard system in order to pinpoint the problem areas

(2) Determination of changes that would result in better overall performance

(3) Determination of the factors influencing the ultimate limitation in the number of analog channels that may be commutated

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*References are listed at the end of the text.

(4) Evaluation of pressed stopper toroids

(5) Additional investigation of the application of redundancy techniques

(6) Making a reliability flow diagram

(7) Investigation of types of oscillators more compatible with the system reliability.

II SUMMARY

During this phase the experience gained in the construction of the Phase II breadboard was used to evaluate the system design and fabrication techniques. The major finding was that the packaging technique for the basic logic circuit was the most severe problem. Interrelations were determined between the circuit and the electrical characteristics of any packaging technique that modify the circuit performance. Using these relationships, an extension of the "tank farm" structure initiated by Langley Research personnel was made. This planar structure permits further simplifications in assembly.

The pressed core samples from Indiana General were tested and found to have their normally measured characteristics (for a fully switched core) very close to the characteristics of the cores cut ultrasonically in Phase II. It was found that characteristics important to proper operation of the basic stopper circuits, however, were significantly different. These differences have been examined in detail. Examination of other toroidal cores of the same material and also of different materials plus a refiring experiment answered in the affirmative the important question of whether the desired partial switched characteristics could be obtained in a pressed core.

A reliability flow diagram was made that disclosed the tuning fork oscillator to be a major contributor to the failure rate figure obtained for the whole system. The probability of success for a five-year mission for this system was found to be 88 percent. Replacing the tuning fork oscillator with a more reliable oscillator--i.e., an RC oscillator--increases the probability for success to 92 percent. Several approaches to redundancy of the semiconductor devices have been examined. Certain approaches were found to be useful due to the small number of semiconductors in the system. On the basis of an hypothesized widespread application of redundancy, it has been estimated that the probability of success for a five-year mission will be increased to 98 percent.

III INVESTIGATIONS

A. Breadboard Design and Fabrication Review

1. Logic Design

The logic design for the 12-channel telemetry system generated in Phase I and modified in Phase II has been reviewed. The experience gained during Phase II was reviewed and served as the starting point for this phase.

One result of this review was the finding that the use of isolated special logic circuits increased fabrication problems. Two such circuits exist in the Phase II design--the digital channel detector circuit and the seventh stage of the weight-current programmer. The logical requirements for these circuits have been examined to determine what alternatives exist.

This examination of the digital-channel-detector logic resulted in the finding that a change in the input circuits of the digital and sync channels will produce several desirable improvements. The special logic circuit to detect the sampling of a digital (and sync) channel is eliminated, the amplifier associated with this circuit is eliminated, the logic is simplified, and there is a simplification in the design of the logic circuits connected to the DCD. The original function of the DCD circuit was to inhibit the repetitive turn-on of the weight-current drivers when a digital or sync channel was being sampled. This was because each of the cores associated with each digital sensor is read out by one of the weight currents and it is necessary to obtain an output from each core only once for each commutation interval. The circuit change on the inputs to these channels provides only one output from each such core and this occurs at the time of the sequential turn-on of the weight-current driver. The requirement to inhibit the repetitive turn-on of the weight currents is no longer necessary and therefore the logic to accomplish this can be eliminated.

A second isolated special logic circuit, the seventh stage of the weight-current programmer, has been examined and a simple logic change has been found to eliminate it. This change merely involves a lengthening of the weight-current programmer to eight stages. In this manner all of the transfer circuits between the programmer and the buffer store are made identical.

The remaining changes relate to the removal of the semiconductor amplifiers that had been added in Phase II as an expedient. The detailed circuit testing necessary to verify the performance achievable with these amplifiers removed has not been made in this phase. Therefore these amplifiers have not been eliminated but are indicated by dashed lines on the logic diagram.* These are the interstage amplifiers inserted between the output of the timing generator and the multipulse drivers L_1 and L_5, and between the super-commutated channel, channel six, and the odd stages of the prime commutated channels and the prime channel programmer.

During the logic review an option was rediscovered in the design of the timing generator. As this has not been included in previous reports it is included here. This option relates to the length of the ring counter when the measurand is to be represented by an odd number of binary digits. The inherent nature of magnetic logic circuits dictates that an even number of stages be used. This may be done, as in the present design, by doubling the number of stages and ORing together the outputs of stages seven stages distant to provide the desired outputs. The other option is to increase the number of bits per channel by one. This may be done by decreasing the number of stages in the ring counter forming the timing generator to one more than required for the binary representation of the measurand. The buffer store is also increased by one stage. This makes an additional bit available for each channel,

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*See Fig. 16.

reduces the length of the ring counter needed (for this system, by six stages), and eliminates the necessity of ORing together outputs of pairs of stages of the ring counter. The availability of this extra bit position makes feasible the inclusion of a check bit for each channel. The logic for generating this check bit may take several forms. One form that is attractive, although it only detects conversion errors in one direction, is relatively simple to implement. This involves energizing the weight-current drivers an eighth time under control of the buffer store. None of the drivers would be turned on at this time by the sequential turn-on logic. A match condition between the weight currents and the measurand should result. Logically a match condition (and also the condition in which the measurand is greater than the weight currents) results in a ONE being set into the buffer store, in this case in the eighth stage of the buffer store. In the event that an error did occur in the digitizing and this error resulted in encoding too large a value in binary form, a mismatch would occur and a ZERO would be set in the store. The logic changes needed to accomplish this would be to increase by one stage the length of both the buffer store and the weight-current programmer, and to change the burst-of-eight generator, L_6, to provide nine pulses.

2. Logic Circuits

The review of the logic circuits was limited to evaluating the data on performance obtained in the previous phases. These data, which related mainly to the basic logic circuit, were variable due to the problems encountered in packaging these circuits, and are therefore subject to interpretation. Further detailed testing of these circuits planned for this phase was not accomplished for two reasons: (1) Important material characteristics of the stopper cores prepared for Langley Research Center by Indiana General differed from those which had been cut ultrasonically and used in Phase II breadboard, and (2) the work on packaging did not reach a sufficiently early conclusion. This effort then was directed at the effect on the circuits due to the logic and packaging changes.

The circuit modification of the input of the digital and sync channels involves a change of the direct current source used to drive the digital sensor input cores to a pulsed current source. By setting all of these input cores only once for each channel commutation, each core is able to be "read out"--i.e., produce an output signal--only once in this interval. This output will occur on the first read-out pulse, and it fully clears the core. The occurrence of subsequent read-out pulses to this core will produce no output as the core is in the fully cleared state. The readout of each input core associated with one of the digital channels is accomplished by one of the seven weight currents (for the lower values of weight current this read current is obtained from the weight-current driver but by a circuit connected in shunt with the weight-current circuit). As each weight-current driver is turned on for the first time, the output of only the core connected to it will produce an output signal. This is the input signal for the BMC of the digital channel. This circuit is shown in Fig. 1. It is of interest to note that by making the polarity of the input signal to the BMC such that the unbalance produced is in the same direction as for the analog channels when the weight current is greater than the measurand, a ZERO will be set in the buffer store when each input core is switched to its clear state. This condition does not produce a repetitive turn-on of the driver as this occurs only for a ONE in the buffer store. Thus it is seen that only one readout pulse can be applied to a core when that pulse produces an output signal.

Reduction of the number of transistors associated with the weight-current drivers was not investigated in this phase. The extra transistors per weight-current driver were included on the breadboard to take care of unexpected losses in the coupling loops between the weight-current drivers and weight-current programmer. This in turn would be determined principally by packaging design.

3. Packaging

A major result of the review conducted in this phase has been to single out circuit fabrication as the problem of paramount importance.

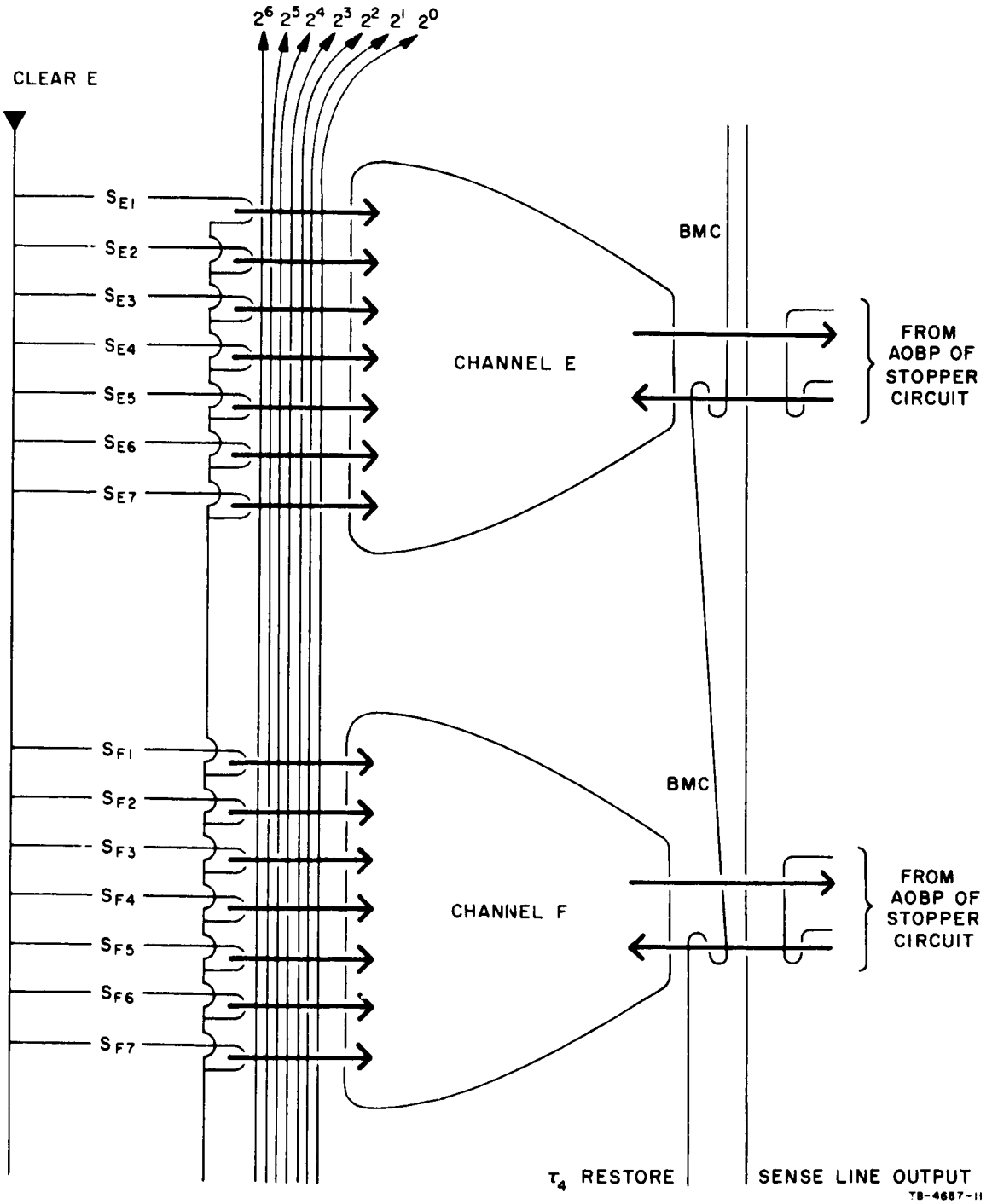


FIG. 1 DIGITAL (and Sync) CHANNEL INPUT CIRCUIT

This is so, due to the strong dependence of the electrical performance of the logic circuits on the electrical characteristics of the mechanical assembly. A second and nearly as significant factor was found to be the production complications induced by the fabrication method. The specific problems encountered in this area were (1) difficulty in obtaining and inability to maintain a low-impedance electrical circuit, (2) production of an excessive number of electrical short circuits due to both the packaging method employed and the large number of solder connections, and (3) the slow and tedious process required for the fabrication of the circuits.

The packaging method used for the assembly of the breadboard in Phase II had been selected in order to achieve low-impedance stopper loops and also to allow (relatively) easy repairs and modifications of the circuits. As discussed in the Phase II report, this produced many complications and did not achieve the desired result. The need for an improved packaging technique has been clearly established. However, before this can be done the limitations imposed on the performance of the circuit by the packaging needed to be more clearly understood.

The starting point in relating the effects on the electrical performance of a given mechanical design was the determination that the impedance of the stopper loop must be low to permit circuit operation at low flux levels. The impedance achieved using the "cavity" was sufficiently low for this purpose when the pressure contact was carefully made. The circuit operation in this structure was adopted as a standard for comparison. At Langley Research Center, an effort was made to obtain an open structure while maintaining a sufficiently low impedance in the stopper loop. This has resulted in the "tank farm" structure where two copper cylinders project from a copper base plate. The stopper loop is completed by solder connections to the tops of these tanks. The impedance of this loop is kept small by making the diameter of the tanks large and the spacing between tanks small. This structure improves the producibility greatly by getting the cores out of the cavity into the open where they are more accessible for wiring. Except for the OBP and AOBP the wiring associated with the stopper cores

is the same as in the cavity structure. The impedance, while somewhat higher than for the cavity structure, is acceptably low.

In magnetic elements where the magnetic path length is long and the flux capacity is small, as in the stopper cores used to date, the position of the windings on a core influence its characteristics. This is due to the effects of the leakage flux that result from this method of excitation. When multiple windings are present on a core, it is important to realize that the net leakage effect is determined by both the excitation current and the reaction currents caused to flow in the secondary windings. For the case where one magnetic element is driven from another through a coupling loop, the impedance of the coupling loop, the characteristics of the load core, and the placement of the excitation windings all combine in a complex manner to determine the reaction current (coupling loop current) and hence the leakage flux. There are guides that are useful in providing an initial assessment of the effects of a contemplated change. Generally leakage flux effects are reduced by physically locating an excitation winding in close proximity to a winding carrying a reaction current. Circuit operation is generally improved by low-impedance coupling loops. The L/R time constant of the coupling loops must be small enough to permit decay of the current during the interpulse period. This illustrates that the limiting lower value of resistance in a coupling loop is determined by the amount of the loop inductance. Leakage flux is also reduced when copper surfaces are contiguous or in close proximity to the surfaces of the magnetic core.

In reviewing the packaging experience together with laboratory tests of Phase II the characteristics required of a new mechanical design were determined. Any new mechanical design must allow the circuit to be more easily and reliably produced. The requirement for complex winding patterns should be eliminated or at least minimized. Connections should be made accessible for forming reliable connections (soldering, brazing). The number of joints should be reduced. Methods for more efficiently handling the cores and use of wiring aids to achieve uniformity and inspectability need to be employed.

To evaluate the producibility of a given mechanical design requires consideration not only of the producibility of the individual circuits but of the complete assembly of circuits comprising the system as well. In this regard, the basic mechanical design must accommodate the necessary circuit variations. This also reflects back on the logic design and requires that special circuits used only once or twice be eliminated unless the alternatives are not satisfactory.

During this phase several different packaging methods were constructed and tested. The considerations listed above are the general results of these tests. From them the factors that needed to be controlled were determined and verified. In particular, the nature of the dependence of circuit operation on the impedance of the flux source loop has been determined, and a more complete understanding of the effects of leakage flux has been obtained. As a result of this increased understanding it is now possible to design a new mechanical structure that will be more producible and reliable.

In the initial investigation of the effect of mechanical design or circuit operation the new pressed S-4 cores (part No. F2271) were used. It was found that the characteristics of these cores are different in important aspects from those obtained ultrasonically.* Before the effects of the mechanical design on circuit operation could be determined, the effects of the difference in core characteristics had to be determined. These differences are discussed in Sec. III-B, below.

A mechanical design has evolved from these tests that is basically an extension of the design originated at Langley Research Center, and provides for improvements in both producibility and reliability. This design is best described as planar, as all cores are situated in one plane. The two stopper cores are positioned on two copper cylinders extending up from a copper base, a few thousandths of an inch higher than the height of the stopper cores. The cylinders are

*See Sec. B-2.

spaced approximately 0.490 inch between center, and the sides of the cylinders are ground flat, forming four surfaces parallel to the plane formed by the two cylinder axes. The cores forming the OBP, the AOBP, the decoupler cores, and the clipper cores are placed between the stopper pair and in the same plane. The flux source cores are placed tangent to one stopper core in the vicinity of the flattened cylinder face. The flux source cores are connected to the stopper pair by means of a flat strip transmission line. This is required to keep the impedance of the flux source loop sufficiently small. The OBP and AOBP are connected into the circuit by "U" shaped conductors that pass down through one core of each balanced pair and up through its mate. Both of these conductors are soldered to the tops of the cylinders and thereby form the stopper loops. The input connections to the circuit are formed by the ends of one of these conductors. The remaining wiring of the circuit may be accomplished by push-through wiring requiring soldering only of the output winding of the AOBP's and the interstage coupling loops between OBP and the input conductors. A sketch of a structure based on the design is shown in Fig. 2.

B. Core Characteristics

The magnetic characteristics of the "stopper" cores are of central importance in the operation of the stopper logic circuit. Specifically, the threshold characteristic and the switching constant determine to a great extent the operating current range of the circuit. For a given core size, the switching constant does not vary much from material to material (as long as we are talking of square-loop ferrites), so the threshold characteristic is our chief concern. The following sections deal with (1) threshold measurements on toroids made from Indiana General Corporation S-4 ferrite material and (2) threshold effects on circuit operation. In addition, abbreviated measurements made on a large number of memory cores of various ferrite materials are discussed.

The breadboard assembly that was developed and fabricated during Phase II of this contract used stopper cores that were cut ultrasonically from a larger toroid. This method of obtaining a toroid having a

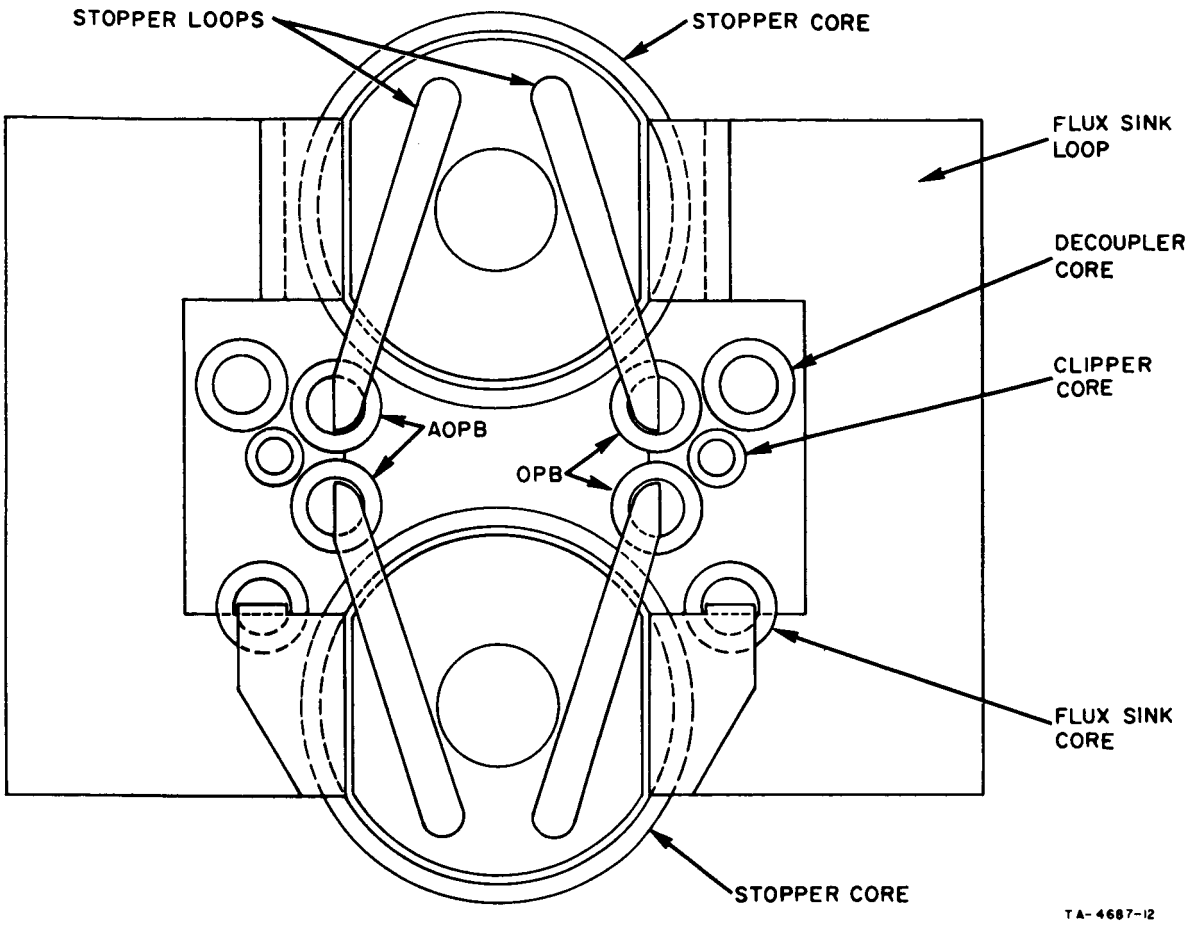


FIG. 2 PLANAR STRUCTURE

high mmf threshold (3 amperes) and a small flux capacity (100 millivolt-microseconds) was satisfactory for the feasibility breadboard. However, for future use of the stopper logic circuit a core made by standard pressing and sintering techniques is desirable. For this reason a pressed core made of S-4 material was secured by Langley Research Center from Indiana General, and it is designated F2271. After initial tests showed these cores to have the same well-cleared threshold and switching constant as the ultrasonically cut cores, stopper logic circuit stages were fabricated both at Langley and at SRI using these new toroids. The circuits so constructed did not function properly, and in particular they could not be driven by a large-amplitude drive current without developing an excessive noise output. Tests on the circuits indicated

that the threshold of the core when partially set was inadequate, and this accounted, in part, for the degradation in performance. Because of this low threshold value a more detailed comparison of type F2271 cores and the ultrasonically cut cores was made and is presented here.

1. Test Procedure

The principal characteristic to be tested is the threshold of the core when it is in a partially set condition--i.e., not in saturation. For the purposes of this report "threshold" is defined as the mmf that switches a specified amount of irreversible flux in the toroid.

We further define three distinct "thresholds": the well-cleared threshold (TH), the partially-switched-state threshold when the threshold value of flux is switched in the set direction (TH_{ps}, partial set) and the partially-switched-state threshold when the threshold value of flux is switched in the clear direction (TH_{pc}, partial clear). The amount of flux that has been partially switched (preset) in the core and the manner in which this is done are specified also.

For the threshold characteristic curves that follow, the pulse sequence used is: (1) saturate the core to its reference condition, the clear state, by applying a large mmf, usually 16 ampere turns, (2) switch specified amount(s) of flux toward the opposite remanent state--i.e., preset the core--and (3) apply the threshold-test pulse. The shape of all pulses is substantially rectangular, having a rise time of approximately 0.2 microseconds, a flat portion of approximately 2.5 microseconds duration, and a fall time of approximately 0.2 microseconds.* The amount of flux that is preset in Step 2 is controlled by varying the amplitude of the preset drive current while maintaining a constant pulse width. The flux begins to switch as soon as the mmf has risen above the threshold (TH) and continues until the current pulse is terminated. The amount of flux switched in Step 3 by the test pulse is specified and is typically 5 or 10 percent of the total core capacity.

*This pulse specification was selected because it gives meaningful data for the stopper logic circuit. If one were primarily interested in material characteristics divorced from this circuit application, another specification would have been appropriate.

The pulses are applied to windings that each have four turns wound tightly around the toroid. The turns in a winding are spaced around the toroid such that each turn is separated from its nearest neighbors by 90°. The three windings for clear, preset, and threshold-test are placed such that the turns on one winding are adjacent to the turns of the other two windings. Care is exercised to maintain the toroid in a strain-free condition.

Three cores for which data are presented are described in Table I, below.

Table I

CORE DIMENSIONS AND FLUX CAPACITY

Core	O.D. (mils)	I.D. (mils)	Height (mils)	$2\Phi_r$ (mV-μs)
Indiana General F2271	330	300	25	100
Ultrasonically Cut from MC 129	330	300	25	90
Indiana General MC 129	375	260	125	1800

2. Core Characteristics--Experimental

Figures 3, 4, and 5 all apply to the ultrasonically cut stopper core, the type used in the feasibility breadboard. Figure 3 shows the threshold values in the set and clear direction as a function of the amount of preset flux. The well-cleared threshold is the value shown for zero preset flux. Note that the threshold values and the preset flux are specified in terms of switched flux in millivolt-microseconds; for this particular core at room temperature this is numerically almost the same as the percent of total flux switched (this is also true for the F2271 core).

In Fig. 3, both 5- and 10-mV-μs thresholds are given. In addition to the magnitude of the various thresholds the shape of the TH_{ps} curve is of particular interest and will be discussed later. The TH_{pc} curves lie below TH, as one expects for a typical ferrite. These TH_{pc} curves are substantially flat for preset values between 30 and 60 mV-μs, which is the region of circuit operation for ZERO transfer. If

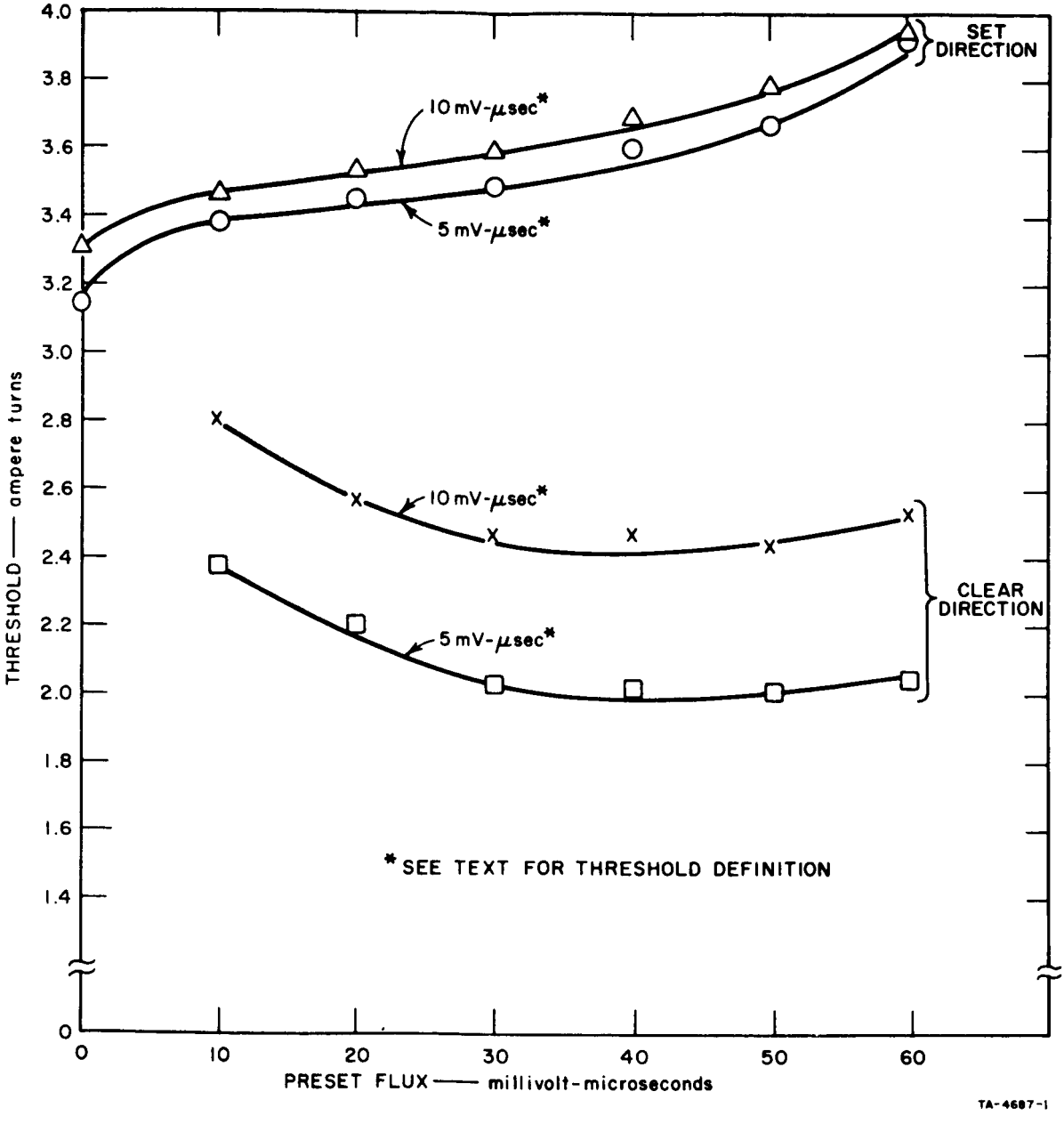


FIG. 3 THRESHOLD CHARACTERISTIC OF ULTRASONICALLY CUT STOPPER CORE AT 32°C

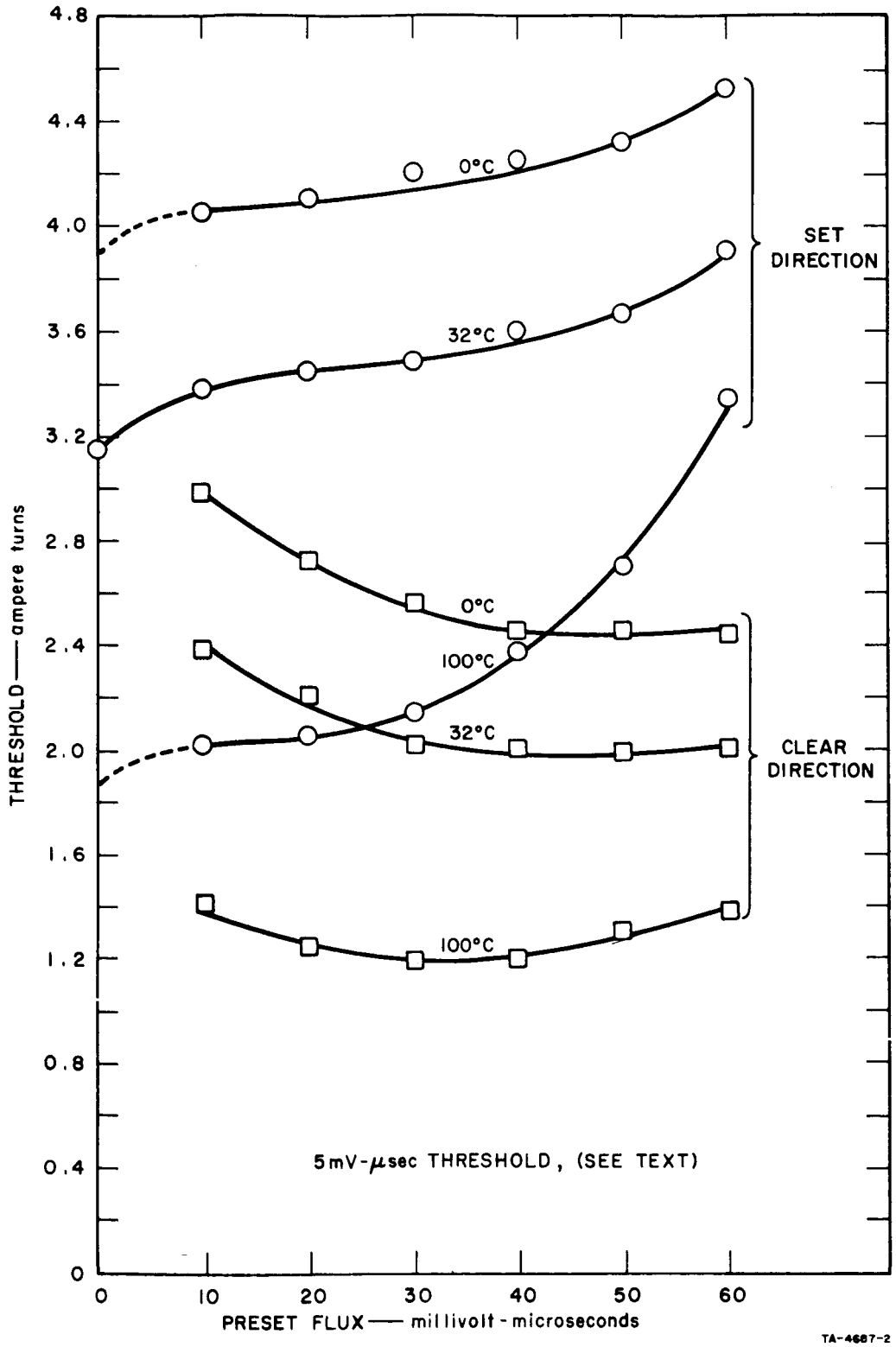


FIG. 4 THRESHOLD CHARACTERISTIC OF ULTRASONICALLY CUT STOPPER CORE AT 0, 32, AND 100°C

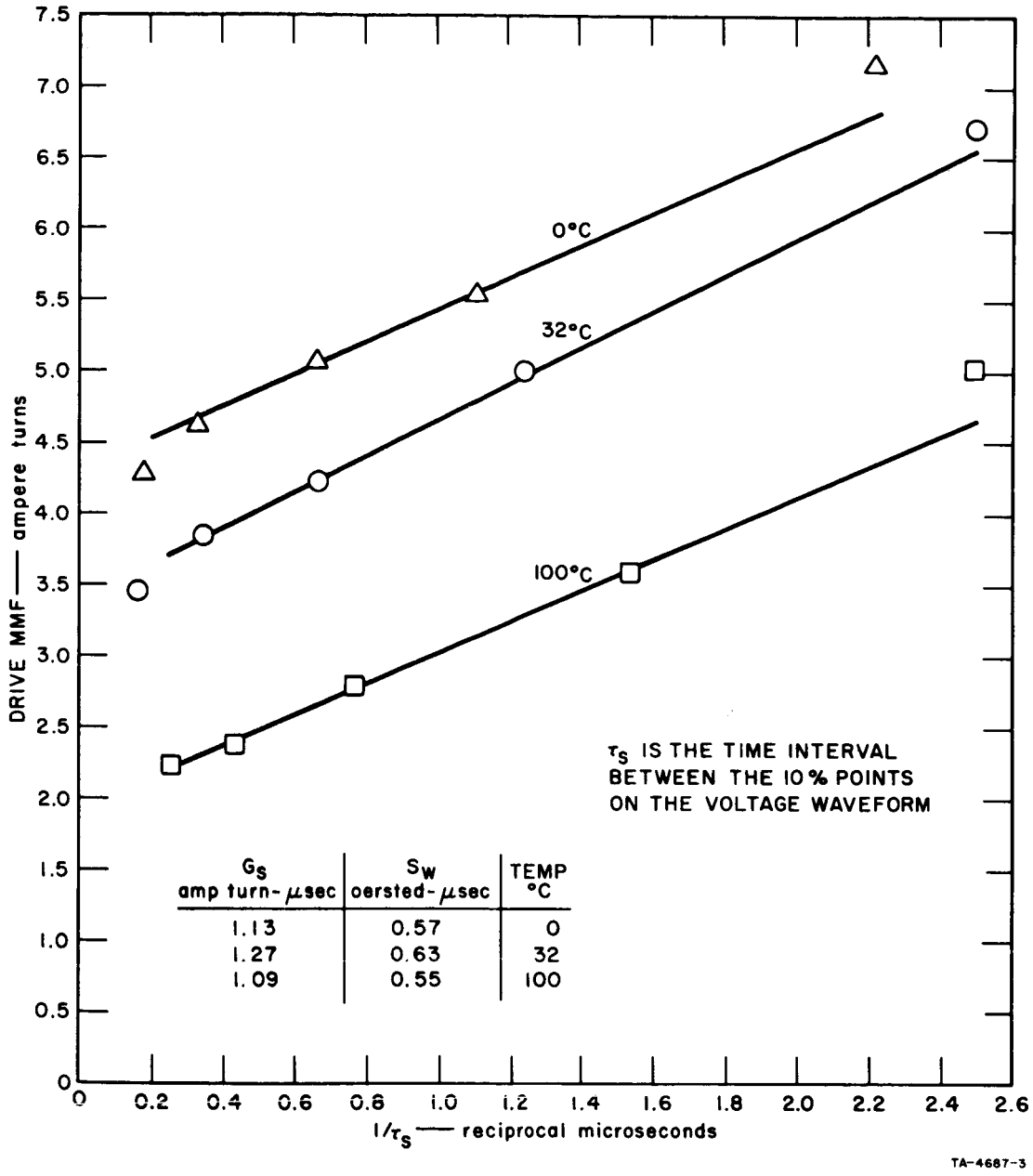


FIG. 5 SWITCHING CHARACTERISTIC OF ULTRASONICALLY CUT STOPPER CORE

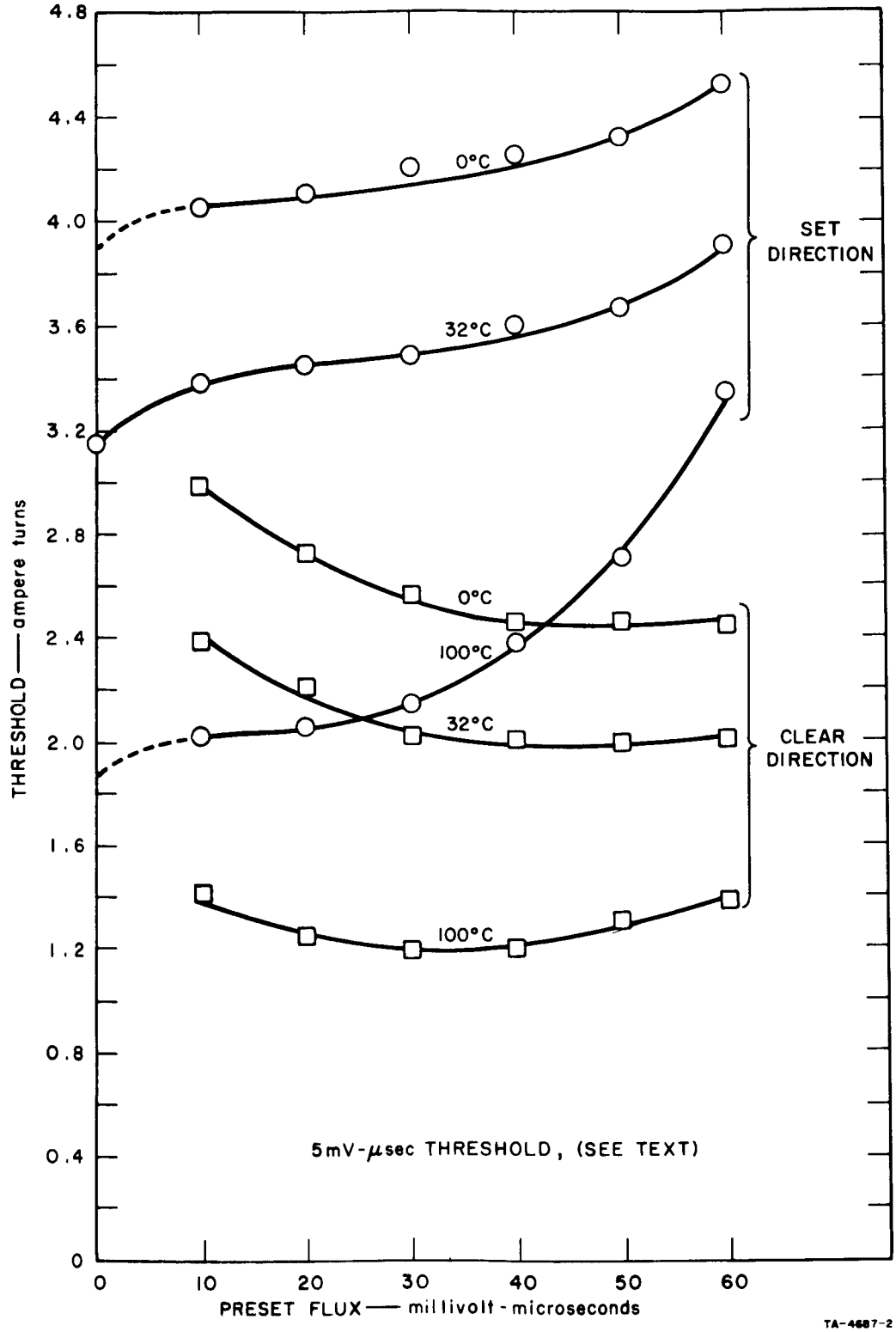


FIG. 4 THRESHOLD CHARACTERISTIC OF ULTRASONICALLY CUT STOPPER CORE AT 0, 32, AND 100°C

the time interval during which flux is preset into the core is decreased, a new family of curves is obtained. With the decreased preset time, both TH_{ps} and TH_{pc} decrease; for example, if the preset time is decreased from the normal 2.5 microseconds to 0.6 microseconds, the 5-mV-μs value for TH_{ps} decreases 10 percent, and TH_{pc} decreases 15 percent.

Figure 4 repeats the 5-mV-μs data presented in Fig. 3 for 32°C temperature and also shows data for 0°C and 100°C. The form of the curves remains unchanged as temperature is varied, but the threshold values decrease as temperature increases. Since the flux capacity of the core varies with temperature this must be borne in mind in analyzing these data. At 100°C the flux capacity has decreased to 70 mV-μs from its 32°C value of 90 mV-μs.

Figure 5 shows the switching characteristic curves for this same core, with temperature as the parameter. These data were taken in the conventional manner. The clear pulse was the same rectangular pulse with a 16-ampere-turn magnitude; however, the width of the set pulse was adjusted to be greater than the switching time to permit the core to completely switch from one remanent state to the other.

Figures 6, 7, and 8 give data for the F2271 toroid taken under the same conditions as for the ultrasonically cut toroid. Comparing the data for the two cores we see that the well-cleared threshold, the switching constant, the threshold defined by extrapolating the switching curve to the ordinate, and the flux capacity (Table I) are all essentially the same for the two cores. Note that these parameters are ones that relate to complete switching of the core rather than partial switching. By comparing only these parameters one would say that these two cores are as alike as one would expect from two cores selected at random from the same production lot. However, the parameters applicable to the cores when in a partially set condition--namely, TH_{ps} and TH_{pc}--show a considerable difference between the two cores. For the ultrasonically cut core, TH_{ps} increases as a function of preset flux while for the pressed core TH_{ps} at first decreases and then increases. Furthermore, for the pressed core the partially set thresholds are both less than

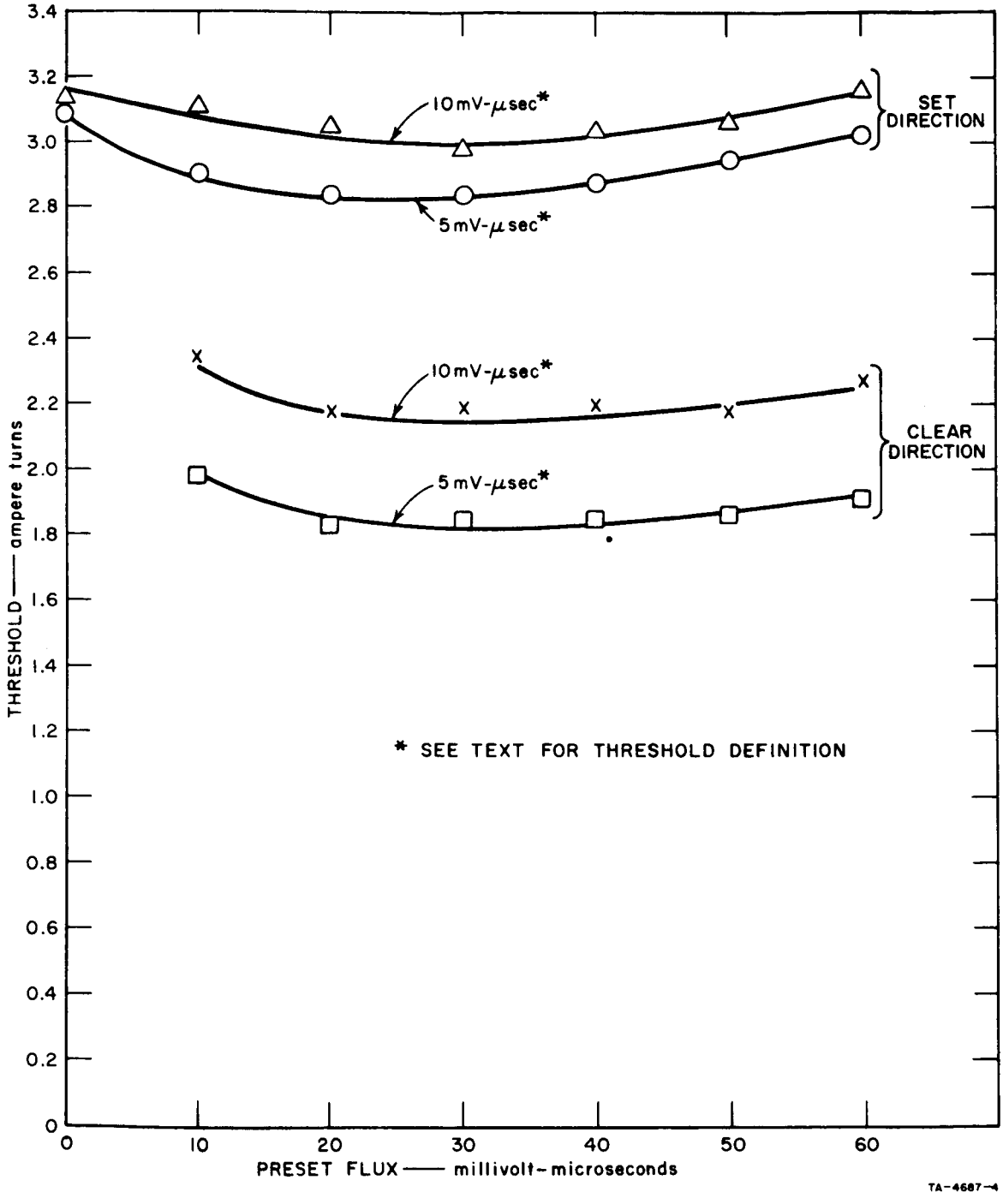


FIG. 6 THRESHOLD CHARACTERISTIC OF PRESSED STOPPER CORE AT 32°C

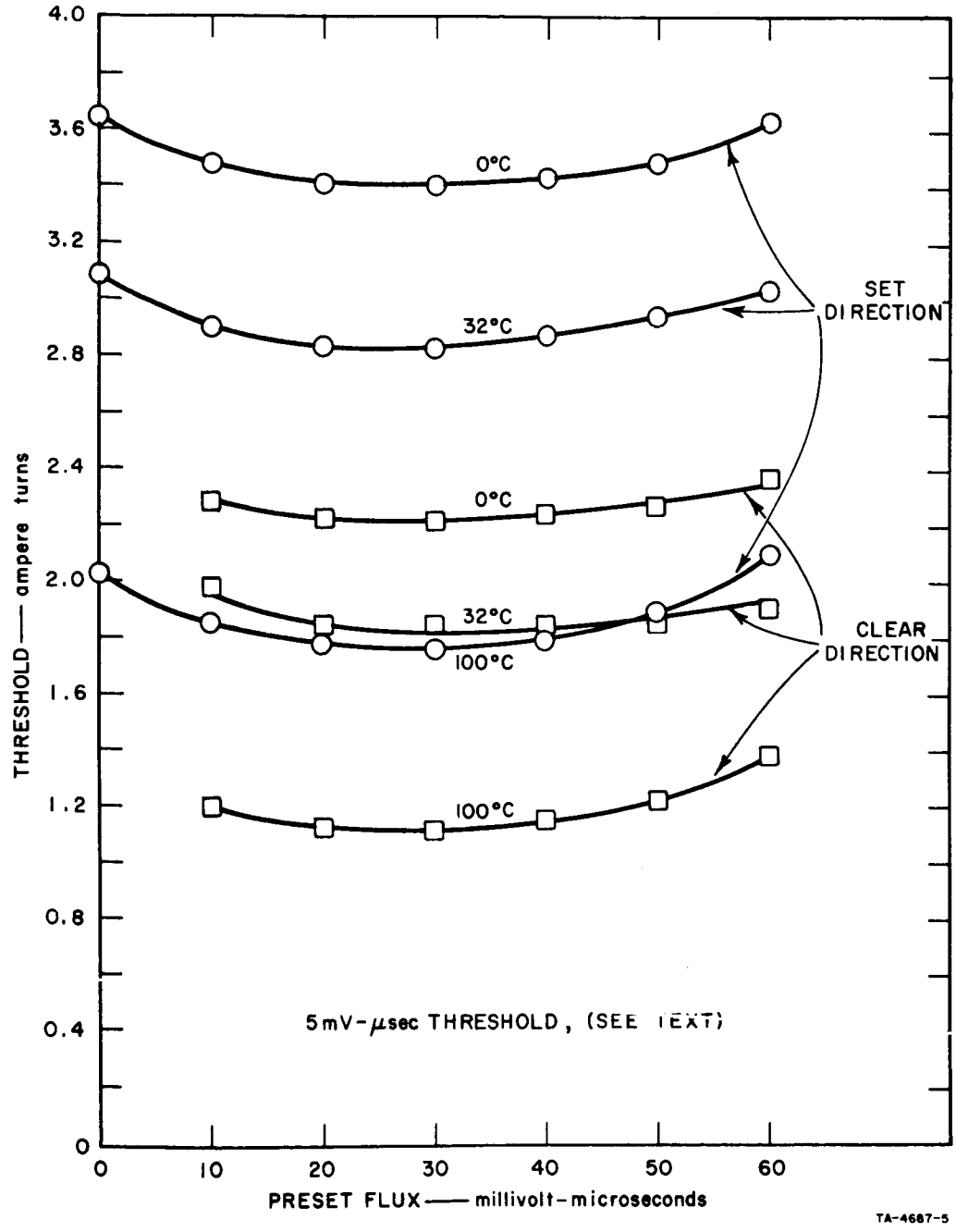


FIG. 7 THRESHOLD CHARACTERISTIC OF PRESSED STOPPER CORE AT 0, 32, AND 100°C

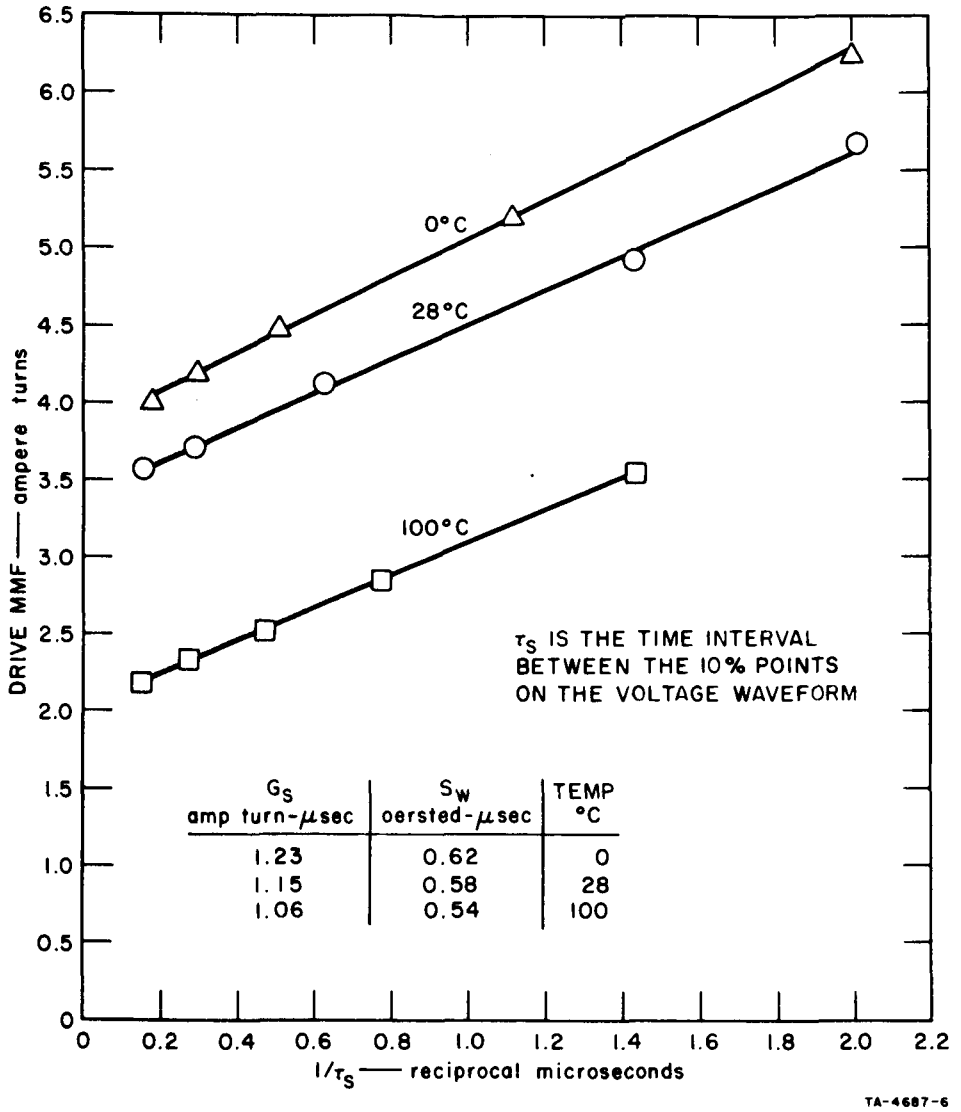


FIG. 8 SWITCHING CHARACTERISTIC OF PRESSED STOPPER CORE

they are for the ultrasonically cut core. It is important to realize that the stopper logic circuit makes use of both TH_{ps} and TH_{pc} in its operation; this feature is discussed in the following section of this report.

One might naturally ask if the ultrasonically cut core has in some peculiar manner achieved an enhancement in TH_{ps} that it is not possible to get in a conventional pressed core. The answer to this is negative, as is shown in Fig. 9, which gives data for the MC 129 "parent"

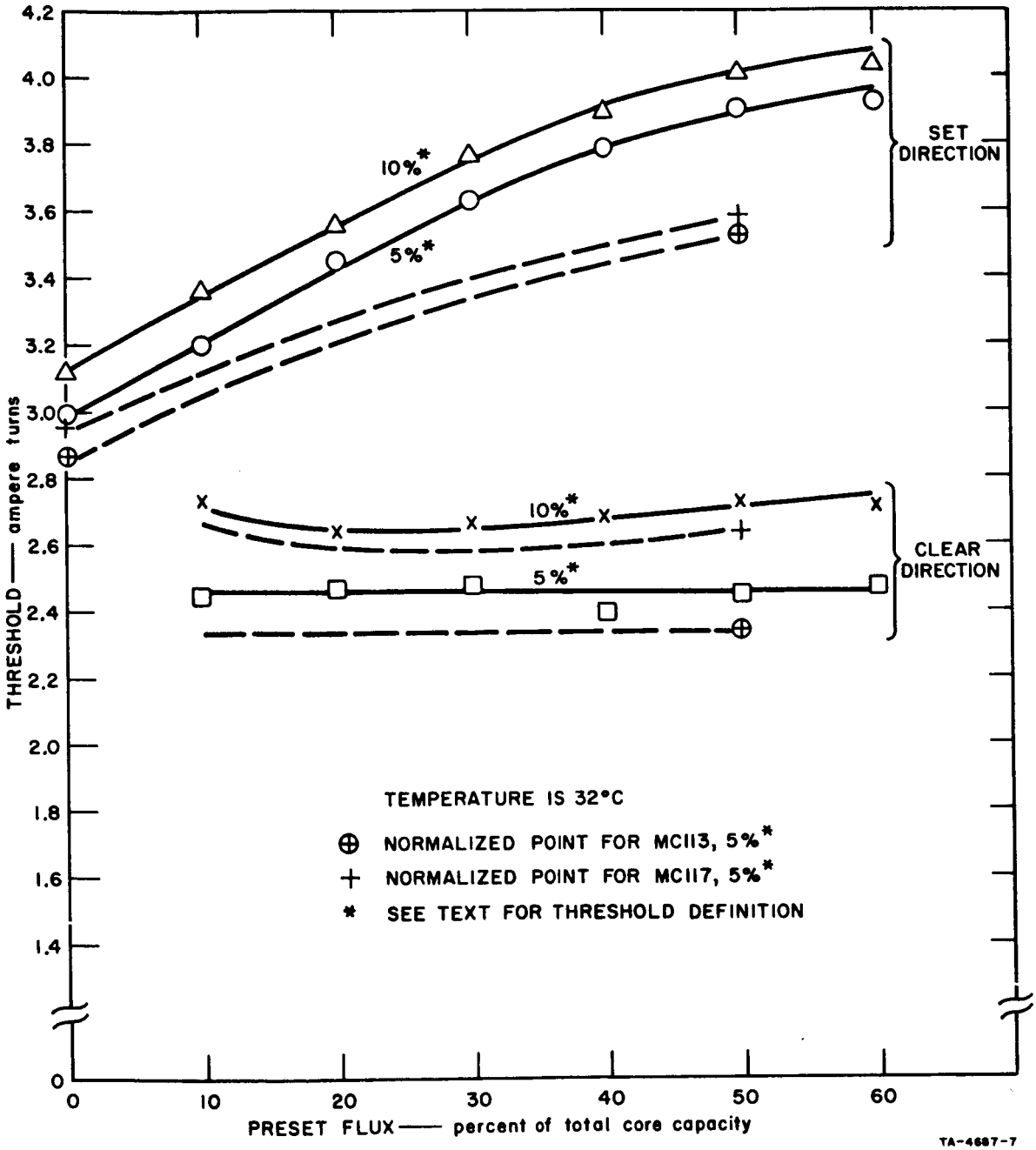


FIG. 9 THRESHOLD CHARACTERISTICS OF S-4 TOROIDS AT 32°C

core and also normalized points for MC 113 and MC 117 toroids. The normalization is with respect to the average diameters of the toroids. The MC 113 is a 50-80 toroid and the MC 117 is a 30-50 toroid; both are made from S-4 material as is the MC 129.

To our knowledge this enhancement feature has not been pointed out in the literature, although the inverse of this characteristic has been used to advantage in certain multipath magnetic circuits (the inverse effect permits the use of ϕ^* as a gain mechanism).[3] We have made experiments other than those described, to verify that this enhancement of TH_{ps} is not an anomaly peculiar to the ultrasonically cut stopper cores. In fact, during this report writing period conclusive evidence has established that it is not an anomaly. This evidence almost makes some of the previous discussion and figures obsolete, but they are retained for completeness. The pertinent experiment is the following: Several of the pressed cores, F2271, were placed in an oven and slowly heated to approximately 1000°C in an air atmosphere, and were then slowly cooled. After this treatment, the cores were tested for flux capacity, TH, TH_{ps}, TH_{pc}, and switching characteristic as described above. The important features of all these characteristics were changed and found to be the same or better than those of the ultrasonically cut stopper core! Specifically, the average of the partially switched thresholds, $1/2(TH_{ps} + TH_{pc})$, is 40 percent greater than that of the original pressed core. Time has not permitted a proper assessment of this new development, but its significance is obvious. The next step that is planned is to repeat the heat treatment in a more controlled fashion.† The threshold characteristic obtained after heat treatment is shown in Fig. 10 for comparison to the normal F2271 core and to the ultrasonically cut core.

Because of the importance of both TH_{ps} and TH_{pc} to the operation of the stopper circuit, measurements were made on a number of different types of 30-50 and 50-80 memory cores from different manufacturers. Some 40 cores were tested, their selection being based upon what we could readily obtain. These cores were tested in a manner similar to that

†The heat treatment was carried out in a small hobby-type ceramics kiln.

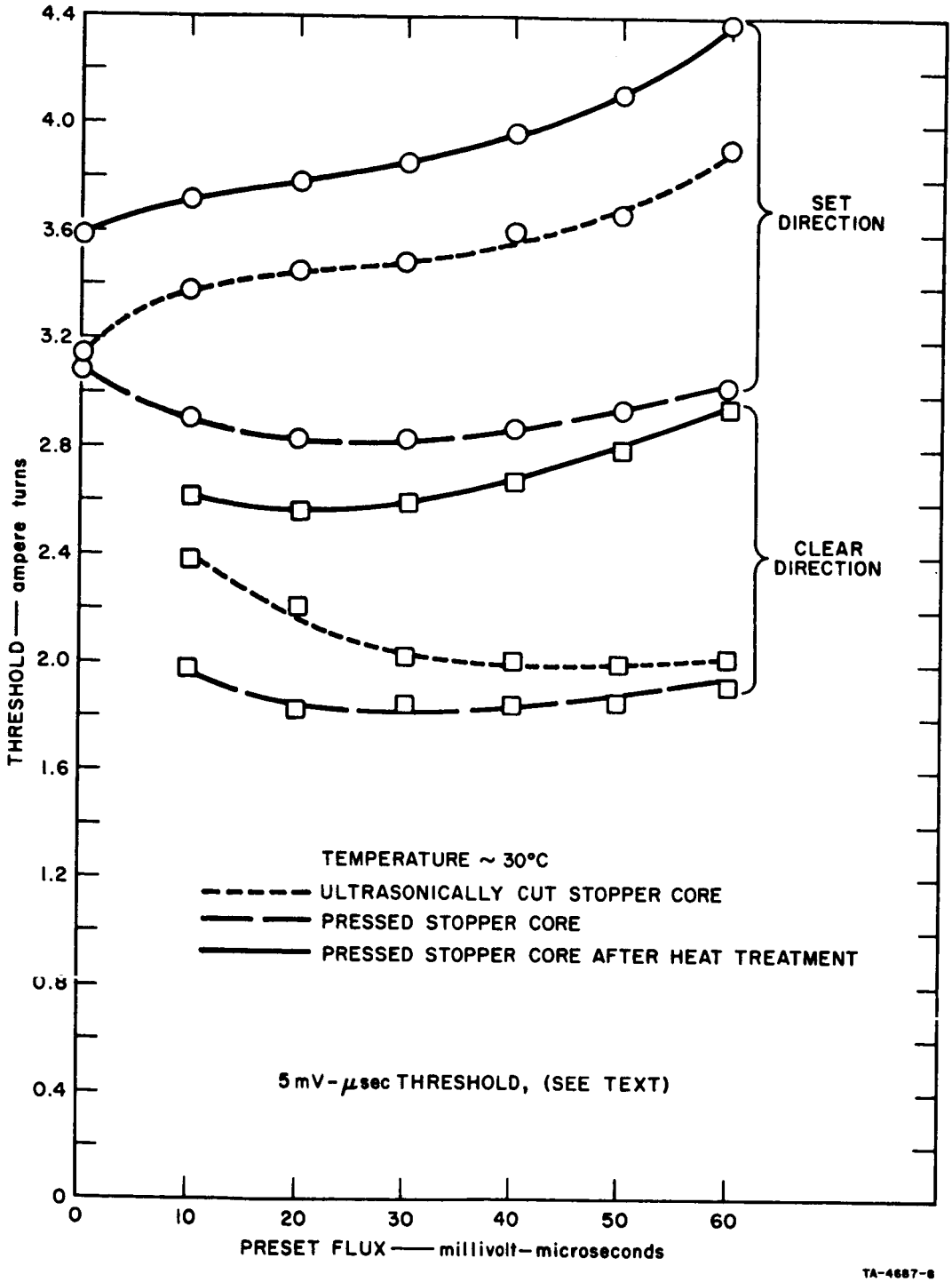


FIG. 10 EFFECT OF HEAT TREATMENT ON THRESHOLD

described above except that the partially set thresholds were measured at the 50 percent preset level only. For each core the average of the partial switched thresholds was compared to the average for the S-4 memory cores. Ten of the forty cores have an average threshold value that is greater than it is for the S-4 cores. These ten all show a greater partial set direction enhancement than do the S4 cores. We have only limited information on the composition of these ferrites, but we tentatively conclude that the addition of zinc to an Mg-Mn ferrite is undesirable. A few lithium ferrite cores were tested; none of them showed enhancement. We conclude from these memory core measurements that S-4 was neither the best nor the worst choice to have made, and we expect that a significant increase in circuit operating range can be achieved by using a different ferrite material.

3. Effects of Core Characteristics on Circuit and Mechanical Design

The operation of the stopper circuit is dependent upon the threshold characteristics of the stopper cores. As shown in the section above, the cores cut ultrasonically from Indiana General MC 129 S-4 toroids exhibited a change in the threshold associated with their partially switched flux state. Their partial clear threshold is somewhat less than their threshold when well cleared; however, their partial set threshold is greater than that when they are well cleared. In magnetic logic circuits the lowering of the threshold is generally an undesirable effect, since it reduces the operating range. In the stopper circuits, however, the two stopper cores are coupled together by two coupling loops--the stopper loop and the flux source loop. The effect of these two loops is to cause the circuit to be dependent upon the average characteristics of the two stopper cores. It is this effect which compensates for the reduction in the threshold of the one stopper by the increase in threshold of the other stopper core. This compensation is effective at the time information is transferred out of a stage. The new pressed cores, Indiana General F2271, have a well cleared threshold essentially that of the ultrasonically cut cores. The partial clear threshold is somewhat lower (10 percent to 20 percent) but the partial set threshold is below the well-cleared threshold and therefore provides

little compensation. The average thresholds of both the ultrasonically cut and pressed cores as a function of both the ZERO and ONE level are shown in Figs. 11 and 12. In order to achieve substantial compensation, the following special conditions must exist: the impedance of the flux source loop must be low, the threshold(s) of the flux source cores must not be exceeded by the compensation current caused to flow in the flux source loop, the impedance of the stopper loops must be low, and the partially switched characteristics of the stopper cores must exhibit a partial set threshold that is higher than their partial clear threshold.

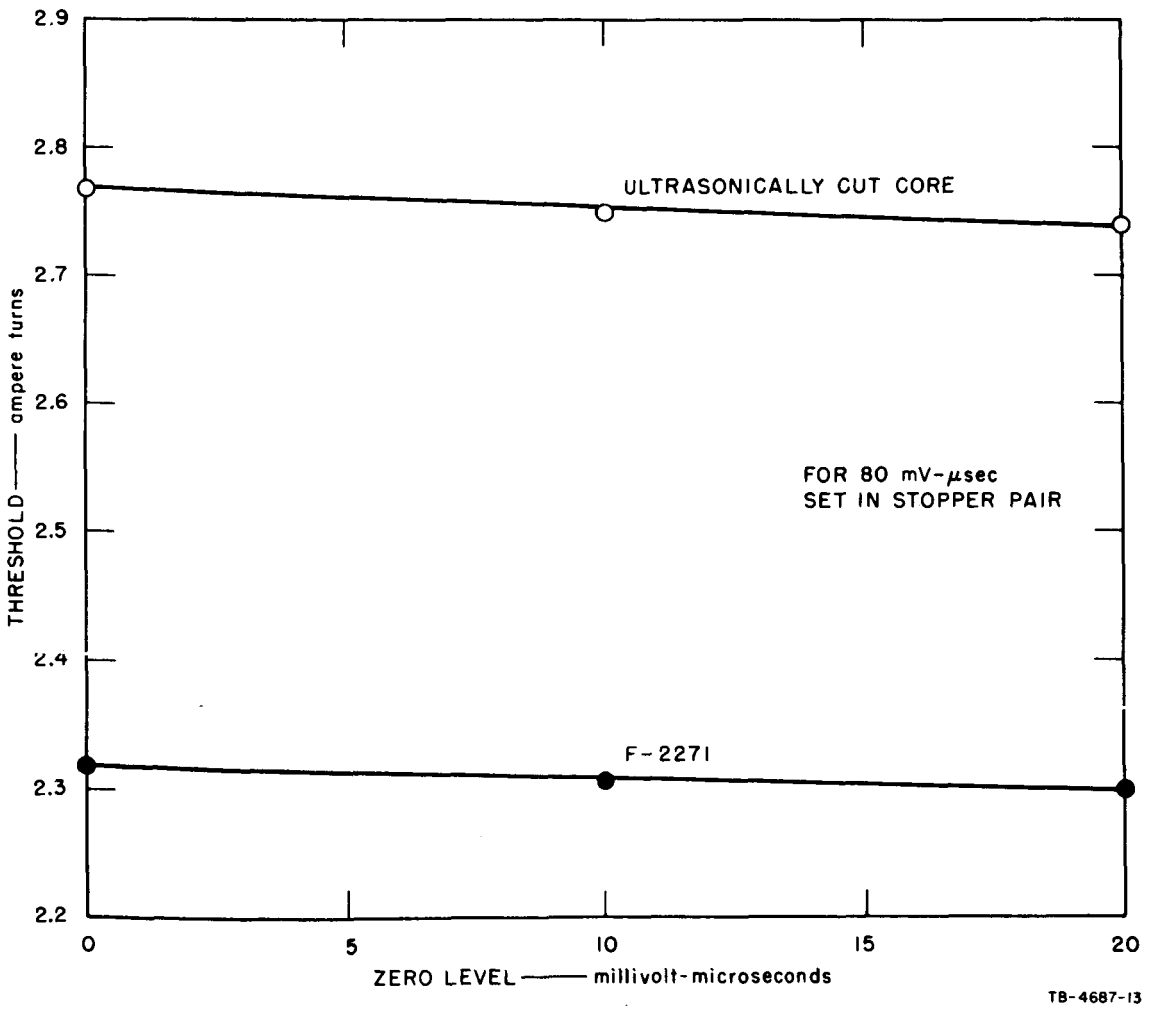


FIG. 11 AVERAGE THRESHOLD FOR ZERO TRANSFER

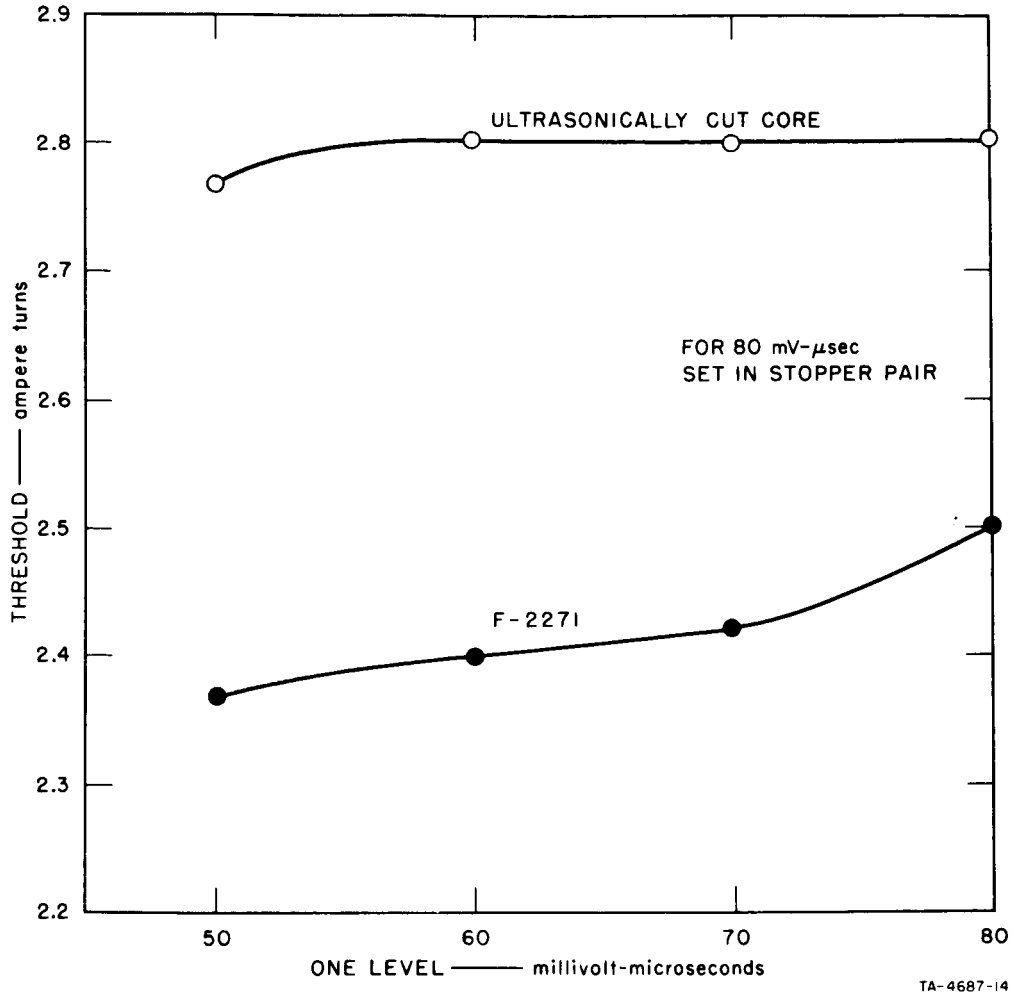


FIG. 12 AVERAGE THRESHOLD FOR ONE TRANSFER

The effects of leakage flux at clear time have been found to lower the stopper core thresholds. This occurs because of the losses in the flux source loop which results in less flux being set in the stopper cores than that switched in the flux source core by the advance drive pulse. When all cores are cleared at clear time, the flux source loop losses are less. As a result, the stopper cores reach their clear state before the flux source core. The flux source core must then complete its switching by inducing a large current in the flux source loop. This current results in a softening of the thresholds of the stopper cores. It has been found that this effect can be eliminated by either of two approaches: applying a post clear pulse, or applying the advance

drive pulse to the stopper cores rather than the flux source cores. In the latter case the flux source (now a sink) core serves the same function as before--i.e., limiting the flux set into the stopper pair--but it accomplishes this by virtue of the low impedance of the coupling loop when the flux "sink" core saturates.

C. Limitations of Number of Analog Channels

The fact that a logical OR is used to connect the outputs of all of the channels to a single-sense amplifier naturally raises the question of the limitation on the number of channels that may be so connected. The limitations considered here are confined to those effective for the present logic circuits. Methods for connecting groups of channels either by means of isolating semiconductor circuits or additional magnetic logic circuits will not be treated.

The circuit used to OR the outputs of the channels to the single input of the sense amplifier is a series connection of the output windings of the Balanced Magnetic Comparator associated with each channel. The limitations in the number of channels that may be so connected are due to the cumulative effect of noise introduced at each OFF channel and ultimately the dispersion of the signal due to non-ideal transmission-line characteristics. The nature of these factors makes them quite dependent upon the physical characteristics of the circuit and for this reason they can be determined only by testing of the circuits themselves. This was not possible during this phase as a result of the core problem mentioned above. The possible sources of noise can be delineated, however. These are: partial setting of the balanced pair of an OFF channel, different saturation permeabilities established in a balanced pair by the action of the measurand and weight currents, and inductive and capacitive coupling between the drive and output windings.

The occurrence of partial switching of a balanced pair of an OFF channel is an indication that the clipper core has insufficient flux capacity. This would be a circuit design fault and would require a larger flux capacity of the clipper. The noise produced by the differences in the saturation permeability arises as follows: The balanced pair of

each off channel are in their cleared state during sampling of a selected channel. In the absence of measurand and weight currents they would remain at the remanent point on their hysteresis curve, as shown by the solid dot in Fig. 13. The resultant of the measurand and weight currents will apply an MMF that displaces the state of each core in different directions from this remanent state. This is shown by the open

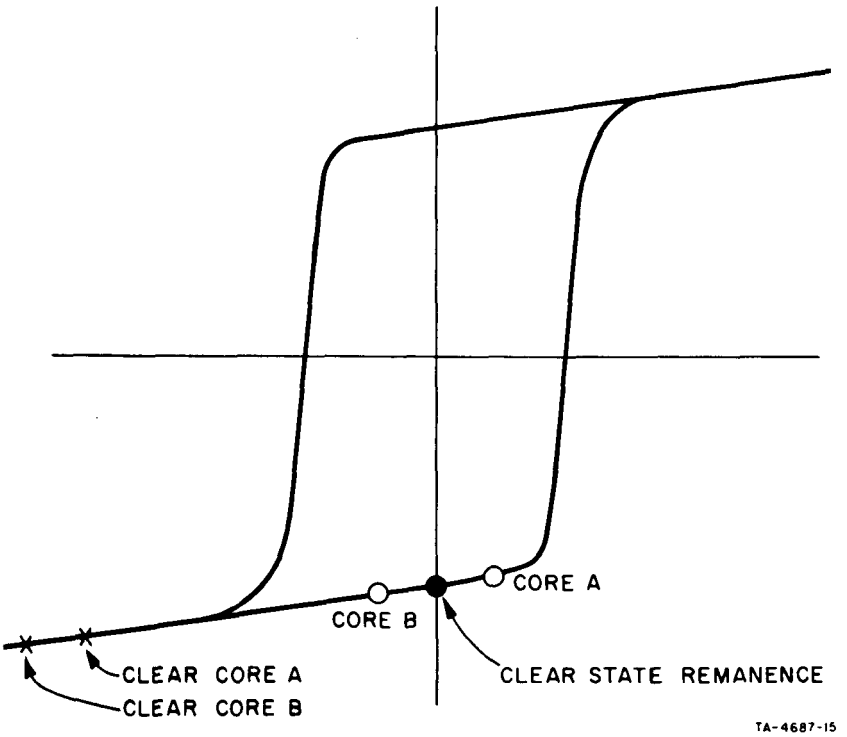


FIG. 13 DISPLACEMENT NOISE IN OFF CHANNEL

circles in the figure. The permeability (slope of the curve) of this saturation portion of the core characteristic curve is not constant. When both cores are cleared, the flux change in each core is different by a small amount. This difference will appear as a noise signal on the output winding of the balanced pair. The magnitude of this signal is small for one channel and it is a function of the magnitude of the displacement from remanence. This displacement varies from channel to channel and also from sample to sample and therefore is subject to

statistical treatment. The noise generated by the inductive and capacitive coupling is the most variable and least amenable to quantitative analysis. This noise is highly dependent on the mechanical design. Although it is not possible to determine its magnitude a priori, it is possible to reduce the magnitude of this noise through the introduction of a noise-bucking signal.

D. Reliability Flow Diagram

A reliability flow diagram provides a means for making a comparative evaluation of a system. It consists of a group of rectangles or blocks connected in series and parallel, as determined by the relation of the failure of a part to the successful operation of the system, or to part of the system. Each rectangle represents a group of parts that are associated together; any one part in the block is essential for the operation of the portion of the system represented by the block--i.e., a failure of one part means that the entire block fails to operate. If two blocks are connected in series it means both must operate for that branch of the diagram to be operable, and, therefore, these two blocks can be merged into one. A parallel connection indicates that the operation of either one or both blocks permits operation of that branch of the diagram. For each block in the diagram a reliability number (the probability of success) is assigned, and by this means the reliability of the entire system is calculated. In our case here, we use the "parts count" approach to assigning reliability numbers to each block. This consists of counting the number of like parts (e.g., solder joints, transistors) and multiplying each number by the failure rate for that part and summing to find the failure rate for the block (we assume the exponential reliability law is applicable).

1. Analysis of Breadboard

The reliability flow diagram for the feasibility breadboard developed in Phase II of this contract is shown in Fig. 14. For this diagram, "success" for the system is defined as achieving seven-bit digitization of the input presented to one balanced magnetic comparator. For the digital and sync channels this means that all seven input signals

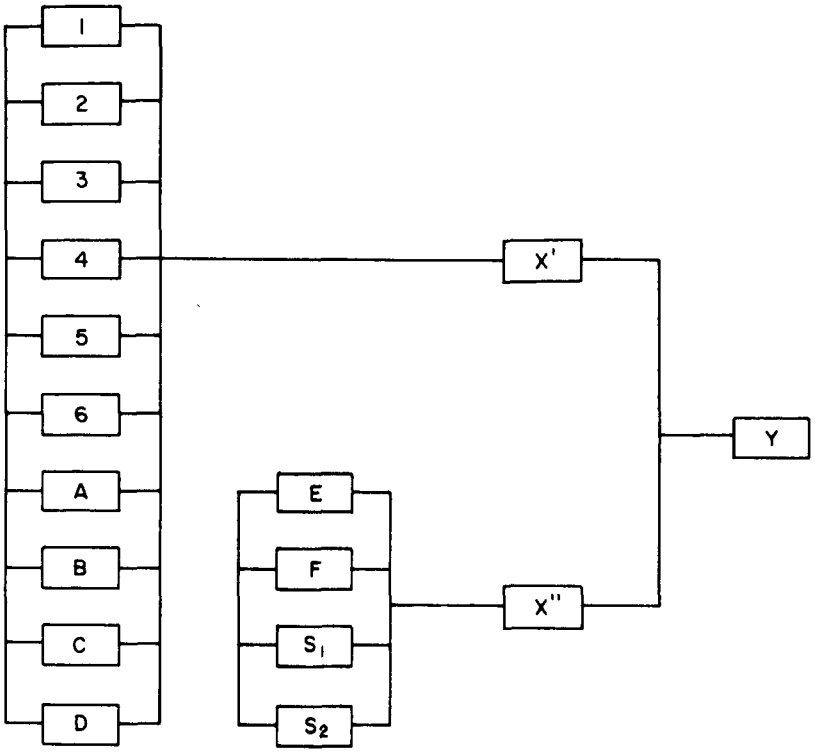


FIG. 14 RELIABILITY FLOW DIAGRAM

to a particular BMC must be present. (A more complex diagram could be drawn that would consider the detection and processing of only one of the seven bits in a digital channel as success, but this complication is unwarranted, as will be apparent shortly).

The blocks labeled 1 through 6, A through F, and S_1 and S_2 identify the BMC's in the figure. (To be more precise, these blocks do not include the BMC output sense windings or the BMC weight current windings because a failure in these would cause the entire system to fail.) The block labeled X' and the one labeled X'' are each portions of the digit channel detector circuit. It is necessary to split this circuit into two blocks because the system operation depends upon its mode of failure. If it fails in a manner that results in the pulse

(τ_2) always being present, then only the analog channel information can be processed; if (τ_2) is never present, then only the digital channel information can be processed.

A tabulation of the number of parts that are represented by each block is listed in Table II. It is apparent from this table that the reliability of the entire system is essentially the same as the reliability of block Y. The contribution of block X′ or X′′ and one of

Table II

PARTS COUNT

Blocks in Fig. 14	Parts	No. of Parts
BMC's 1 through D and E through S_2	Ferrite toroids	70
	Solder joints	40
Blocks X′ and X′′	Ferrite toroids	10
	Solder joints	20
Block Y	Ferrite toroids	500
	Solder joints	1640
	Transistors	45
	Diodes	40
	Capacitors	49
	Resistors	84
	Tuning fork	1

the fourteen BMC's to the calculation is so small compared to that of block Y that we group all of the components together for the calculation to follow. This is the same as redefining "system success" as being the digitization of all channels. The results shown in Table III are based upon this definition, and the failure rate for the system is 271×10^{-8} failures per hour. This corresponds to an 88.5-percent probability of success for a five-year mission. One salient point shown by this tabulation is that one component, the tuning fork, contributes more than one-third of the total system failure rate! Another salient point is that the semiconductors contribute another one-third to the total failure rate. On the basis of this analysis the tuning fork and semiconductors are targets for future work that is aimed at increasing reliability.

Table III

SYSTEM RELIABILITY SUMMARY

Part Type	No. of Parts	Failures per 10^8 Hours* per Part	Failures per 10^8 Hours, per Part Type
Tuning fork	1	100	100
Transistors, silicon planar	45	2	90
Diodes, silicon (glass type)	40	1	40
Solder joints	1700	0.01	17
Capacitors, poly-carbonate, mica, and ceramic	49	0.2	10
Resistors, carbon composition	84	0.1	8
Toroids, ferrite	580	0.01†	6
TOTAL FAILURE RATE			271

$\lambda = 271 \times 10^{-8}$ failures per hour

MTBF = $1/\lambda$ = 369,000 hours

Probability of mission success for five-year period = $e^{-\lambda t}$ = 88.6%

*These failure rates were supplied by NASA-Langley for this evaluation. They are based on high component reliability employing 100 percent screening for known weaknesses, approved derating policies (stress level assumed to be 50 percent), and approved fabrication techniques. Failure rates correspond to 65°C (50°C maximum ambient and 15°C temperature rise for part).

†No figure known--assumes worst case.

It is instructive to break the total system into parts to make comparative reliability evaluations of one portion versus another, and of one implementation of a portion versus another implementation. Since there was a considerable project effort directed at developing drivers that minimized the number of semiconductors, let us compare the part count reliability of all the logic drivers when implemented by multipulse drivers and when implemented by transistorized drivers. For the comparison we will estimate the parts that would be required to implement L_2 by a multipulse technique. The rest of the multipulse driver parts will be counted as realized in the feasibility breadboard. For estimating the parts required for the transistorized version we assume that it takes one transistor, one diode, and one resistor for each pulse generated, except for L_2 where the actual count in the breadboard will be used. The assumptions we are making here put the transistorized version in as favorable a light as possible while for the multipulse it is just the reverse. Table IV summarizes this comparison. The total contribution to the failure rate of the system that the transistorized version

Table IV

LOGIC DRIVER RELIABILITY

	Multipulse Version		Transistorized Version	
Part Type	No. of Parts	Failures per 10^8 Hours, per Part Type	No. of Parts	Failures per 10^8 Hours, per Part Type
Transistors	7	14	29	58
Diodes	17	17	29	29
Resistors	28	3	29	3
Capacitors	38	8		
TOTAL FAILURE RATE		42		90

makes is twice that for the multipulse version even for this weighted comparison. Additionally, we think that a further decrease in the number of transistors is possible for the multipulse version. This comparison supports our hypothesis that the multipulse driver would significantly increase system reliability.

E. Semiconductor Redundancy

Minimizing the use of semiconductors has been a goal throughout this work. The philosophy has been that with fewer semiconductors, redundancy becomes tractable. The system as represented in the feasibility breadboard of Phase II has 45 transistors and 40 diodes. This number can be further reduced, and we have some specific ideas on how this might be accomplished. However, the purpose of this section of the report is to examine the system as it is presently implemented to see how redundancy can be applied and to see what benefit and complications accrue as a result.

One good way to increase the system reliability is to use standby redundancy wherein one unit or one group of units is switched out of the system and another switched in upon failure of the first. This approach requires error detection, a communications link to activate the switch-over device, and the switch itself. Because this form of redundancy requires a communications link and error detection, it involves more than this "system" per se and therefore we have not fully assessed this approach. We can, however, point out the following features of this approach: (1) it generally provides at least as large an increase in the system reliability as other redundancy approaches, (2) the number of additional parts required is small by comparison, (3) power consumption of a redundant system is essentially the same as for the non-redundant system, (4) a communication link between the space vehicle and earth is already available, (5) error detection by monitoring the system output at the earth receiving station appears to be a simple process, and (6) there is a possibility of capitalizing on the reliability of magnetic techniques in the switch-over circuitry.

In general, redundancy should be applied to a system after the individual circuits are made as reliable as possible, consistent with relevant system considerations. As shown by the failure rate given above, the use of the tuning fork is to be questioned. In anticipation of a recommendation that is to follow, we consider the application of redundancy to the system as it has been described except that the tuning

fork is replaced by a completely reliable device. For a five-year mission this increases the probability of success from 88.6 percent to 92.8 percent.

For this modified system, the reliability increase that will result from applying redundancy to the semiconductors can be appreciated by assuming that all transistors and diodes are replaced by quadded equivalents. (It should be recognized that quadding requires a large increase in the number of components, and even if it were possible in all of the circuits, other approaches would be taken where applicable.) The reliability or probability of successful operation of a quadded circuit can be expressed as $P = \frac{3}{2}p - \frac{1}{2}p^3$ where p is the probability of success for the individual component, and P is the probability of success for the quadded circuit. This expression assumes that failure by shorting is equally probable to failure by opening. p is taken to equal $e^{-\lambda t}$. Using the values given in Sec. III-D for the transistor and diode failure rates, and a five-year mission time, the reliability of the 40 quadded diode circuits is $1 - (1 \times 10^{-5})$, of the 45 quadded transistor circuits is $1 - (5 \times 10^{-5})$, and of the remainder of the (non-redundant) circuits is 1.8×10^{-2}). The entire system reliability is the product of these three terms--namely, 98.2 percent.

We conclude from this qualitative analysis that a significant improvement in system reliability can be achieved by applying redundancy, and we proceed to briefly examine each semiconductor circuit. For each circuit we point out one or two approaches to redundancy that are compatible with that particular circuit, in addition to the standby redundancy already mentioned. Attention will be focused upon the transistors since it is trivial from a circuit point of view to quad the diodes, and this is a good redundancy approach for them.

1. Oscillator

The oscillator circuit occupies a unique position in the system from the reliability standpoint because of the tuning fork. As shown in Table III this one component accounts for one-third of the total system failure rate. For this reason it is not worthwhile to apply semiconductor redundancy to this circuit, but rather an effort

should be made to get rid of the tuning fork (or alternatively, find a means for making it more reliable). This approach is discussed briefly in Sec. III-F.

2. Sense Amplifier

For redundancy purposes the sense amplifier can be broken down into two parts--one that contains linear amplifiers and one that contains on-off switches. For the linear amplifier portion a good approach is to apply redundancy on the circuit level and use two amplifier circuits having a common input. The present sense amplifier has a high input impedance, so a parallel rather than series input connection is called for. Resistors placed in series with each amplifier protect against signal loss in the event of a short in the transistor input circuit.

The part of the amplifier that comprises transistors used as on-off switches presents a different redundancy problem. The parallel channel approach can be used here if desired except for the output of the amplifiers. The amplitude of the output pulse current from the redundant amplifier should not be dependent upon internal circuit failures, and therefore simply paralleling the outputs is not acceptable. A good approach here is to apply component redundancy by quadding the output stage and triggering it "on" from each of the parallel channels (an OR circuit from a logic point of view).[4]

3. Weight-Current Drivers

Transistors are used here in a feedback amplifier. In principle this means that standby redundancy can be effectively applied to this circuit. This approach leads to complex circuitry for detecting and correcting errors, as mentioned above. For this reason, if this type of redundancy is applied it should be at the sub-system level--i.e., applied to the weight current drivers as a unit rather than individually to each of the seven drivers.

An alternate approach, and one that appears better suited to this system, is to use component redundancy in a special type of a quad circuit that is applicable when a transistor is used in its active

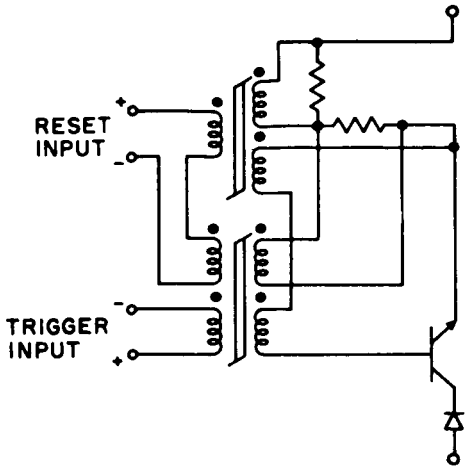
region.[5] The fact that the amplifiers in this driver make use of feedback can probably be used to advantage in applying this type of quad redundancy.

Associated with each transistor amplifier there is a clamping diode that cannot be quadded and therefore requires special consideration. By adding a parallel diode and increasing the input current, the driver can be protected against a diode open-circuit failure. In order to protect against a diode short, an additional square loop core with parallel diodes and a diode OR circuit is required. This circuit provides the input to the special quad circuit.

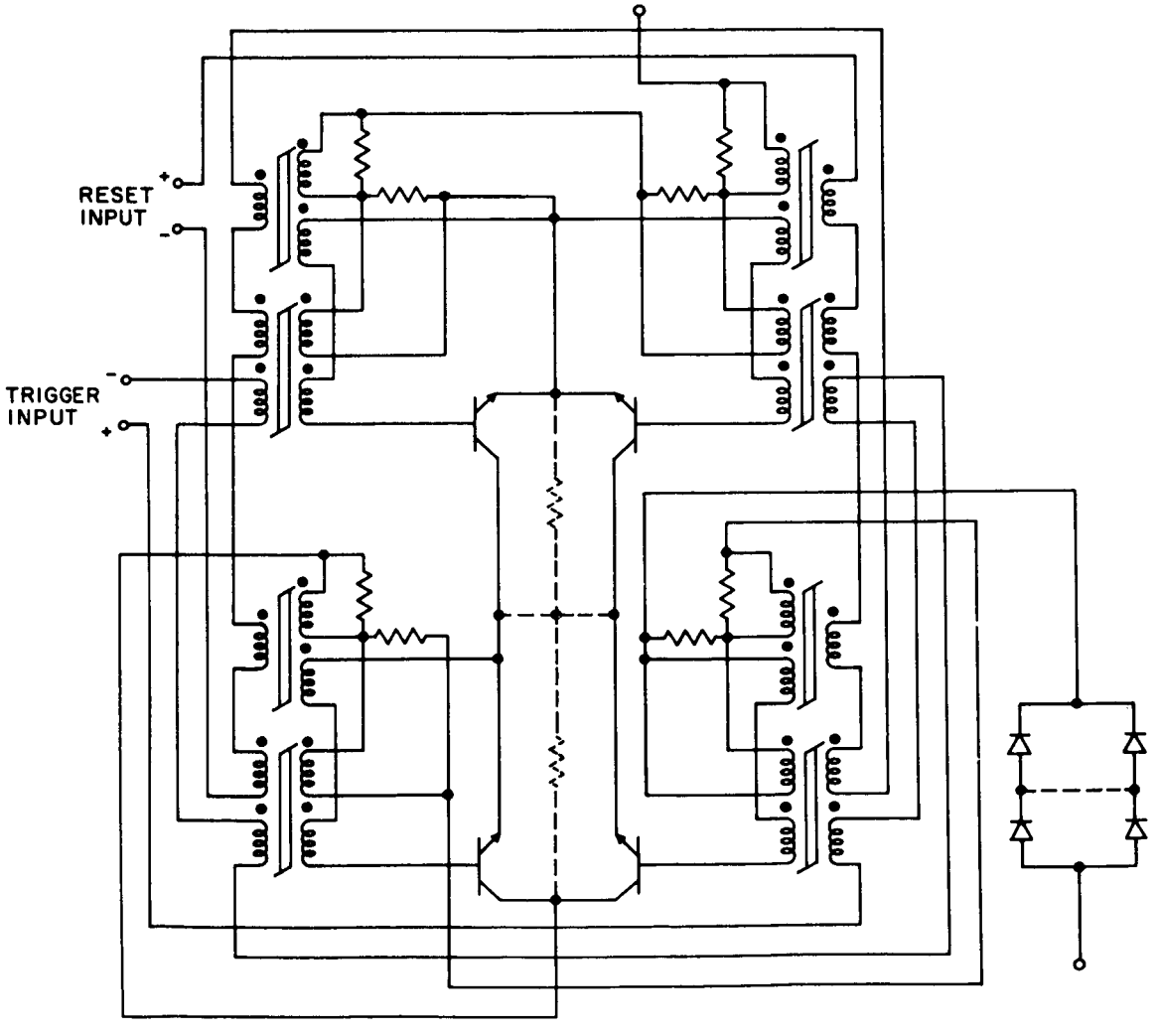
4. Multipulse Logic Drivers

On the component level, quadding the transistors in each multipulse driver is a useful approach to redundancy. The problems faced here are similar to those to be faced in quadding the output of the sense amplifier, and any effort on one circuit would benefit circuit work on the other. The circuit for quadding one transistor in a multipulse driver is shown in Fig. 15. A discussion of a similar circuit is found in Ref. 4.

Another possible approach uses two complete driver circuits to replace each driver in the nonredundant realization. In the normal operation of this redundant system each pair of drivers would be used but they would be triggered on alternately. When one driver fails, the other one would continue to operate, but the output of this driver combination would now have only half as many pulses as before the failure. The portion of the system driven by this driver combination would correspondingly have its repetition rate halved. Because of the sequential nature of the system, the repetition rate will be halved for all the events that occur in the cycle of operation after the time position occupied by this driver output. We have not worked out the details of the triggering of each driver in the pairs but it seems practical. This sub-system redundancy approach assumes protective measures have been taken so that a short in one circuit does not cause the power supply to malfunction.



(a) NON-REDUNDANT CIRCUIT



(b) QUADDED CIRCUIT

TB-4687-10

FIG. 15 SWITCH CIRCUIT FOR MULTIPULSE

F. Low-Frequency Oscillators

This system uses a 400-cps signal as its basic timing source. Since the frequency stability required is ±0.1%, it is not necessary to use a high-frequency quartz crystal oscillator and a count-down circuit. The Phase II breadboard used a tuning-fork controlled oscillator that had more than adequate frequency stability, but the reliability assigned to the tuning fork (Table III) is so low that another type of oscillator is needed.

In searching for an oscillator type that is suitable for this application, the two salient features that we used for evaluation are reliability and adequate frequency stability. There are three types that seem to meet these requirements--linear LC oscillators, linear RC oscillators, and pulse oscillators using square-loop cores.[6] Stability of ±0.1% is difficult to obtain with this latter type, and since it offers no peculiar advantages we recommend the use of one of the linear types. Both the LC and RC types can meet the frequency-stability requirement of ±0.1% as temperature and voltage are varied. These oscillator types would require from three to six transistors, while the tuning fork oscillator required two transistors. These additional transistors would have at most a combined failure rate contribution of 8×10^{-8} failures per hour compared with 100×10^{-8} failures per hour for the tuning fork, thus providing a significant increase in system reliability.

We conclude that LC and RC oscillators can be used for this application.

IV RECOMMENDED MODIFICATIONS

A. Circuit Modifications

The logic circuits for future models of this all-magnetic telemetry system must be packaged in an improved manner. It is recommended that the design be based on a planar configuration wherein all cores associated with one circuit are physically located in the same plane. In this manner the wiring common to groups of circuits is simplified. It may be accomplished by first aligning the circuits and then pushing through the wires, effecting the simultaneous wiring of multiple circuits. The considerations relating to mechanical design discussed in Sec. III-A must be used in order to maintain the performance of the magnetic logic circuits--namely, low-impedance stopper loops and flux source loops.

A second recommendation relates to the selection of the flux source core for the stopper circuits. By using Indiana General MC113 (S-4 material 50/80 size) cores in place of the Ampex 802-40 cores for use as the flux source in the stopper circuits, an increase in circuit operating range will be achieved. The MC113 has a higher threshold and will therefore permit the full enhancement of the threshold of the stopper cores to be obtained.

It is also recommended that the advance drive winding through the flux source core be deleted and placed through the stopper pair instead. This change will then use the flux source core as a flux sink as discussed in Sec. III-A, and provide additional increase in the operating range. The latter occurs because leakage flux patterns that effect a reduction in the threshold of the stopper cores will not occur when driven in this manner.

The findings indicated in the reliability flow diagram emphasize the need for replacing the tuning fork oscillator with an RC transistorized oscillator as discussed in Sec. III-F. This will result in an improved reliability figure assignable to the system.

The final circuit recommendation is to change the input circuit for the digital and sync channels to provide a pulse source to set the cores associated with each digital sensor when closed. This pulse, the channel clear pulse, would replace the dc supply originally used for this purpose and would occur once each channel commutation. The outputs of each such core would be OR'd together and provide the input for the BMC associated with that channel. This circuit is shown in Fig. 1. The effect of this change and the associated logic change was described in Sec. III-A.

B. Logic Modifications

Associated with the circuit modification of the inputs to the digital and sync channels, a logic change to eliminate the digital channel detector logic circuit is recommended together with its associated amplifier. The output from this circuit (τ_2) is then replaced by τ_2. The need for the function performed by the digital detection circuit--viz., prevention of the repetitive turn-on of the weight-current drivers--is eliminated by the above-mentioned circuit change on the channel inputs.

It is recommended that the length of the weight-current programmer be extended one stage to be eight stages long. This change eliminates the requirement for a special circuit for the last stage of the weight-current programmer and allows all stages to be identical.

The final recommendation resulting from the review conducted in this phase is a conditional one. It relates to the interface amplifiers interposed between the super and prime channels and also between the timing generators and driver L_6. It is expected that these amplifiers may be eliminated, but this is influenced by the mechanical difficulties of providing sufficiently low-impedance coupling loops in their place. Providing that low-impedance coupling loops are compatible with the fabrication techniques used, it is recommended that these amplifiers be eliminated.

The logic diagram for the 12-channel Magnetic Telemetry System has been modified to reflect these recommendations and is shown in Fig. 16.

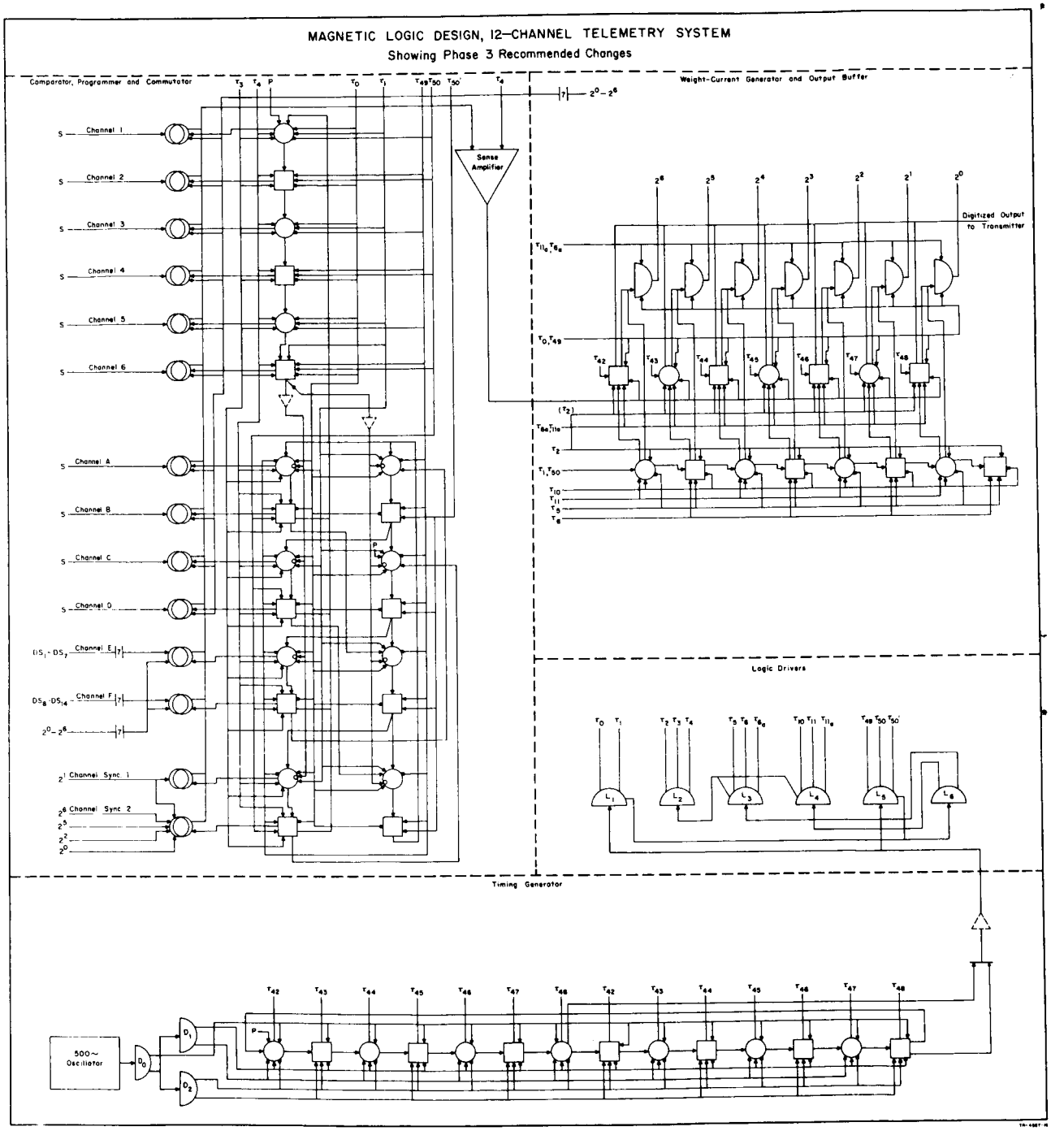


FIG. 16 MAGNETIC LOGIC DESIGN, 12-CHANNEL TELEMETRY SYSTEM, SHOWING RECOMMENDED CHANGES

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"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof."

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