METAL-OXIDE-SILICON TECHNOLOGY

A LITERATURE REVIEW

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A LITERATURE REVIEW

1.0 Introduction

This literature review has been made to assist scientists and engineers working in the field in their efforts to develop improved MOS devices and to promote a better understanding of the processes and designs by which improved devices are obtained.

The history of the developments leading to the invention of MOS devices is summarized in section 2.1. The basic physical principles governing MOS device behavior are covered in section 2.2. The fabrication process for MOS devices is described in section 2.3. Section 2.4 deals with the various techniques for evaluation of oxides. Models for the oxide structure and oxide-dependent behavior of devices are the subject of section 2.5. The variety of empirical findings and efforts to develop improved oxides are collected in section 2.6. The effects of radiation on MOS devices are reviewed in section 2.7.

The compilation was completed on September 10, 1965.

2. LITERATURE REVIEW AND CORRELATION OF PUBLISHED INFORMATION

2.1 History of MOS Devices

The growth and development of the semiconductor device industry has been strongly dependent on the understanding of semiconductor surface properties. The development of device designs and processing techniques that make the best use of surface properties (or reduce their effect) has played a major role in the history of semiconductor devices.

2.1.1 Early Field Effect Transistors

In 1948 Shockley and Pearson[114] made a structure with a thin insulating sheet between a germanium sample and an evaporated metal film. They measured the change in conductance of the germanium as a function of the voltage applied to the metal. They found that only approximately 10% of the charge induced in the germanium was mobile. They postulated that the rest resided in bound states on the germanium surface.

In 1952 Shockley[115] devised the unipolar field-effect transistor in which he isolated the channel, in which the conductance was to be controlled, from the carrier immobilizing surface states by means of depletion layers formed at the surfaces. However, this device had the disadvantage that it could only be operated in the depletion mode. At about the same time, the invention of the bipolar transistor (a device in which the active region was located within the semiconductor so that surface properties were of less importance) overshadowed the work on field effect transistors.

2.1.2 Passivation of Bipolar Transistors

During the 1950's, large numbers of germanium transistors were produced in which acceptable surface properties were achieved by empirically developed processing techniques. To protect these transistors from severe surface problems, they were packaged in hermetically sealed packages containing very carefully controlled ambients.

In 1959, Atalla et al[3,5] studied the silicon-silicon dioxide system where the oxide was produced by thermal oxidation and found that such an oxide produced stable and reproducible surface properties. Combining this knowledge with an earlier finding[30] that SiO_2 can be used as a diffusion mask to form device structures, planar silicon transistors and diodes were invented[51].

These planar devices were found to have improved electrical characteristics in those parameters (or at those operating points) for which the surface effects (at the edge of the junction where the junction meets the surface) were significant. Such improved parameters include I_{CBO}, noise figure, and h_{FE} at low currents.

However, eventhough oxides make the silicon much more insensitive to the ambient gas, ionic drift in the fringing electric field at the periphery of the junctions induces changes in the distribution of the surface potential and thereby causes the electrical characteristics to drift[4].

2.1.3 Metal-Oxide-Silicon Devices

In 1960 Kahng and Atalla[64] proposed a silicon structure in which an insulated gate was used to induce conduction between two diodes. The theory of this device was developed by Ihantola[59] in 1961. In 1962, Hofstein and Heiman[44,52] described a metal-oxide-semiconductor, or MOS, field-effect transistor with an insulated gate on single crystal silicon. This device has good silicon surface properties and therefore does not have the trapping problems found by Shockley and Pearson[114]. It also has the desirable feature that, unlike the junction unipolar field effect transistor, it can be operated in either the enhancement or the depletion mode. Many papers[2,10,107,133-137] appeared describing a variety of useful applications for this device and noted its advantages:

1. Very high input impedance
2. Functions with signals of either polarity
3. Low noise level at high frequencies
4. Simplifies circuit design
5. Relatively insensitive to temperature
6. No carrier storage
7. No offset voltage
8. Ease of fabrication
9. Larger packing densities are possible because no isolation is necessary between components and because MOS transistors can be used as resistors.

Another advantage claimed[133,134] for field effect transistors was that they could tolerate radiation up to a value where mobility or the doping level change -- generally about ten times the dose at which lifetime degradation begins. On this basis, field effect transistors might be expected to tolerate a radiation dose approximately ten times greater than bipolar transistors of comparable dimensions. Recently it has been shown[8,57,58,66,102,124,126] that the effect of radiation on the oxide layer begins at a level well below that which directly affects the silicon.

The oxide and oxide-silicon interface properties play a very important role in determining MOS ddvice performance, stability and reliability. Because the oxide between the gate electrode and the channel is very thin (only 1000 to 2000 Å), even a small applied voltage sets up a strong electric field, which causes the motion of ions in the oxide and produces undesirable effects on the device characteristics. For example, only four volts applied to the gate of a 1000 Å thick oxide produces an electric field of 10^5 volts/cm. This high field drifts any mobile ions in the oxide, especially at higher temperatures. Since the oxide layer is so thin, ions can very quickly drift from one face of the layer to the other. This changing distribution of charge in the oxide induces undesirable drift in the electrical parameters of the device.

A further problem arises in that even if the charge in the oxide is immobile and does not cause drift in the device characteristics, it causes a transistor to have a threshold voltage not desired by the circuit designer. The undesired level of threshold voltage results from the fact that immobile charges in the oxide affect the surface potential of the silicon. This undesirable charge causes a p-channel transistor to require a higher voltage than desirable to induce channel conductance, and causes an n-channel device to conduct even at zero gate-to-source voltage on the gate.

2.2 Physical Principles

2.2.1 Literature Describing Physical Principles of MOS Devices

MOS device description and design equations have been presented by a number of authors including those of references 13, 28, 46, 50, 52, 59, 60, 62, 83, 87, 88, 106, 126, 128, and 134. The following briefly describe the physical principles upon which MOS devices are based, as extracted from the referenced literature.

2.2.2 Basic Device Structure

The structural form of an MOS device is that of a parallel-plate capacitor in the form of a three layer sandwich of metal, oxide, and silicon, as shown in Figure 1.

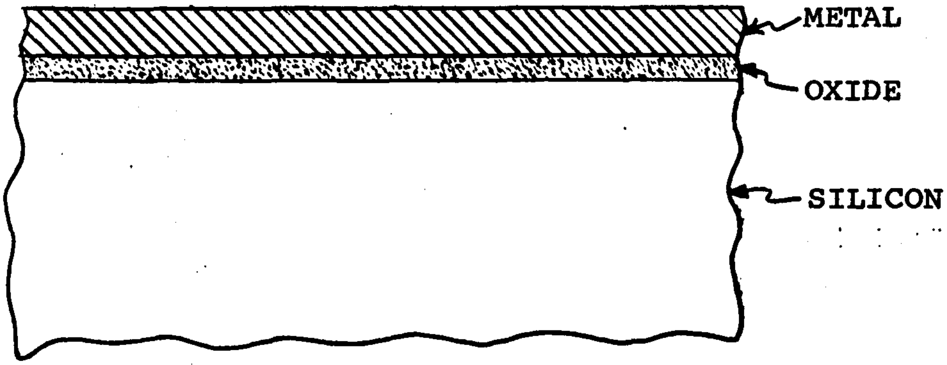

Figure 1: Representation of structural form of MOS device.

The basic physical principle of MOS devices is that the density of charge in a layer of silicon beneath an oxide can be controlled by the voltage applied to a layer of metal on top of the oxide. The net charge in the silicon is that due either to immobile ions in a depletion layer or that due to an accumulation or inversion layer of mobile charges. More precisely, with n-type silicon a positive voltage on the metal attracts electrons to the surface of the silicon, forming an accumulation layer of electrons. A negative voltage on the metal repels electrons and forms a depletion layer in n-type silicon. As the voltage applied to the metal is made more negative, mobile positive carriers (holes) form an inversion layer at the silicon surface within the depletion layer. These situations are depicted in Figure 2.

The depletion layer and the inversion layer play importance parts in determining the electrical behavior of MOS capacitors and transistors.

2.2.3 MOS Capacitors

In a simplified picture a MOS capacitor can be considered a series combination of the capacitance of the oxide and that of the depletion layer. When the accumulation layer exists,

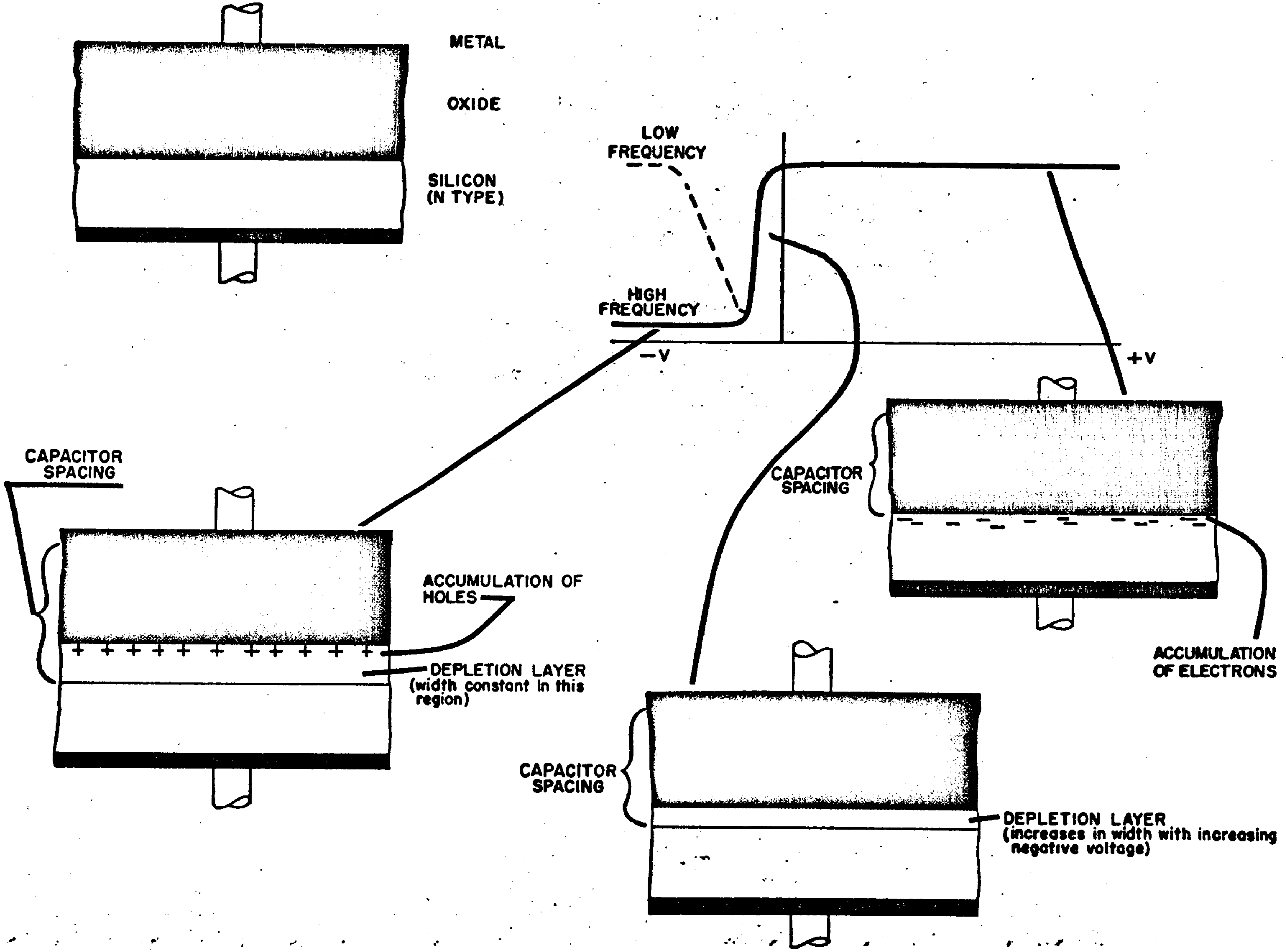
METAL
OXIDE
SILICON (N TYPE)
LOW FREQUENCY
HIGH FREQUENCY
—V
+V
CAPACITOR SPACING
CAPACITOR SPACING
ACCUMULATION OF HOLES
DEPLETION LAYER (width constant in this region)
CAPACITOR SPACING
ACCUMULATION OF ELECTRONS
CAPACITOR SPACING
DEPLETION LAYER (increases in width with increasing negative voltage)

Figure 4.^{2}

there is no depletion layer and one therefore observes only the high capacitance of the oxide. As a voltage is applied to repel the majority carriers away from the oxide in the silicon, the series capacitance of the resultant depletion layer decreases the over-all capacitance. As the voltage is increased further, an inversion layer forms within the depletion layer at the interface with the oxide. Because the charge density in the inversion layer can vary over a wide range, d-c voltage changes do not cause changes in the depletion layer thickness. Therefore, the capacitance is insensitive to the d-c voltage in the range in which the inversion layer exists.

If the measurement frequency is low and the inversion layer is formed, as one increases the applied voltage the capacitance increases to a value as high as that for the oxide capacitance. This happens at low measurement frequencies because the inversion layer charge density can change as rapidly as the measurement signal voltage changes. In this case, changes in voltage are impressed only across the oxide (the voltage change across the depletion layer is negligible) and so only the capacitance of the oxide is measured.

The frequency at which the capacitance-voltage curve changes from a low frequency characteristic to a high frequency characteristic depends on the rate at which the inversion layer charge density can be changed. This rate depends on the density and character of allowed energy states, the presence of ionizing radiation, the temperature, and the presence of a nearby region rich in the carrier type from the inversion layer.

2.2.4 MOS Transistors

In an MOS transistor, the inversion layer forms the channel (conductive layer) of which the conductance can be controlled. This channel is located between a source region and a drain region as shown in Figure 3, and its conductance can be varied by varying the voltage on the gate electrode.

2.2.5 Study of MOS Device Behavior

Although MOS transistors are more important commercially, MOS capacitors are simpler to work with and provide a very valuable tool for the study of the problem areas in MOS transistors.

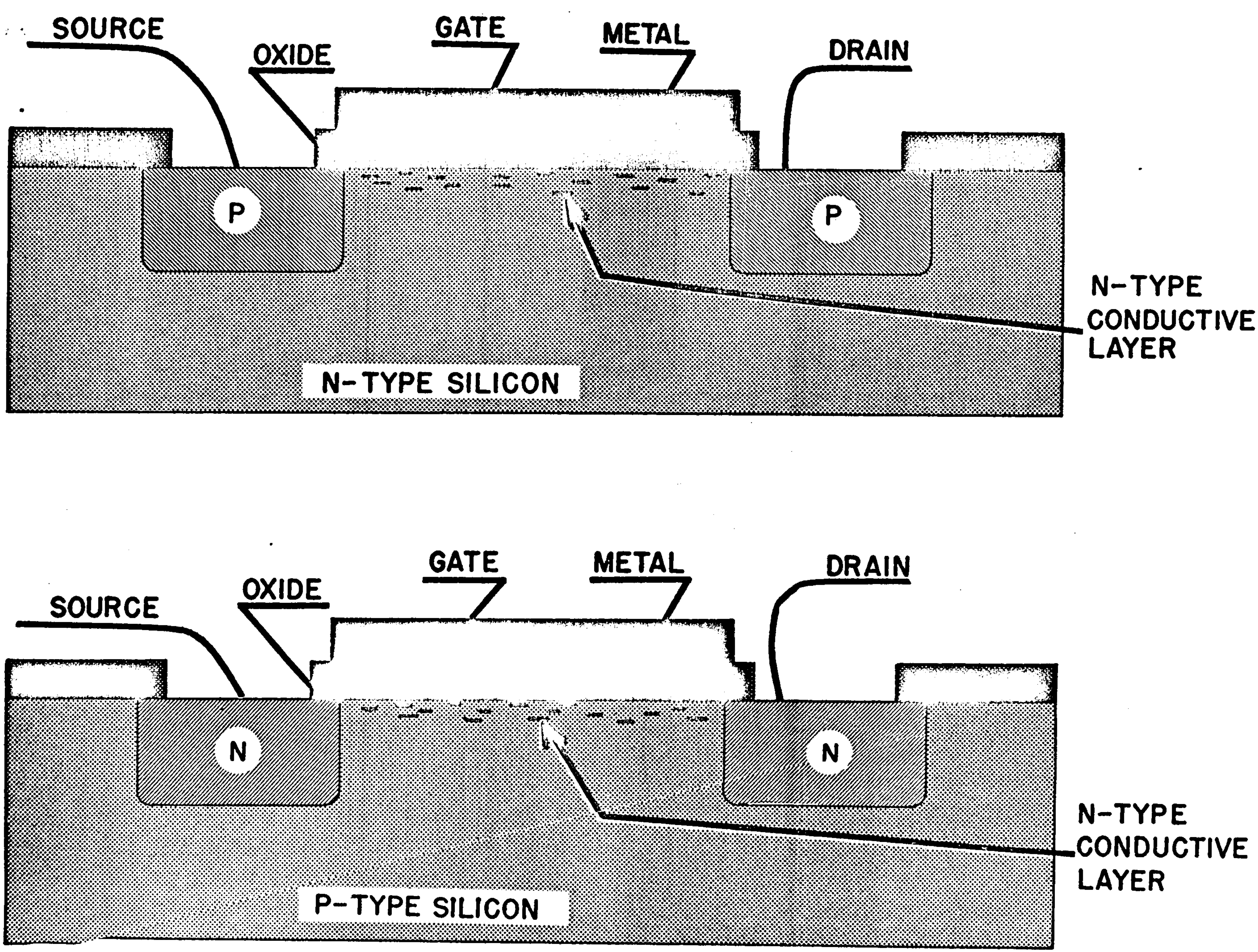
SOURCE
OXIDE
GATE
METAL
DRAIN
P
P
N-TYPE CONDUCTIVE LAYER
N-TYPE SILICON
SOURCE
OXIDE
GATE
METAL
DRAIN
N
N
N-TYPE CONDUCTIVE LAYER
P-TYPE SILICON

Figure 3.

Whereas MOS devices are a good medium for the study of oxide related properties, there is the attendant troublesome fact that they are very sensitive to minute differences in the oxide. Any charge in the oxide or at the oxide-silicon interface influences the electrostatic potential at the silicon surface and thereby influences the area density of charge in the depletion and inversion layers. Therefore any charge in the oxide influences the capacitance and the conductance of a device.

The effect of oxide charge on the silicon surface potential is added to that of the applied voltage. Its effect thus is to shift the device characteristics curves along the voltage axis. If there is a change in the distribution of charge in the oxide due to the formation (due to heat treating or readiation effects) or annihilation of charge or due to movement of charges in the oxide (such as under the influence of an electric field at higher temperatures), the shift of the characteristic curves along the voltage axis occurs without a change in the shape of the curves. If the distribution of the charge in the oxide depends on the applied voltage (as is the case if energy states exist in the oxide which can be filled or empty depending on their position relative to the Fermi level), one can expect a change in the shape of the curve as it shifts along the voltage axis.

From the above basic description, one can understand the behavior of MOS devices under varying conditions of applied voltage, temperature, and radiation ambient. As shown in Section V, one can study the density and distribution of charges and traps in the oxide by means of the electrical device behavior.

2.3 Fabrication of MOS Devices

2.3.1 Typical Processing Procedure for Thermal Oxides

On the basis of published information relating to the fabrication of MOS structures, the following outline gives the typical important processing steps involved.

1. Prepare silicon wafer for oxidation by a series of cleaning and etching operations.
2. Oxidize the wafer to a thickness of about 6000 Å.
3. Photolithographically cut openings in the oxide to delineate the mask pattern in preparation for diffusion of the source and drain regions.
4. Diffuse the source and drain regions.
5. Remove oxide from the back of the silicon; nickel plate and heat so that the nickel getters metallic impurities from the silicon.
6. Photolithographically reduce the oxide thickness for the gate region and cut openings for the contacts to the source and drain regions.
7. Deposit the contact metal (usually aluminum) layer and etch (again using photolithographic processes)

the layer to form the contacts to the source, gate and drain regions.

8. Heat treat the processed wafer to reduce the resistance at the electrode contacts.

9. Scribe the wafer, bond the chips to headers, bond device leads to package terminals, and seal packages in a controlled ambient.

Due to the sensitivity of the device parameters to minute differences in the condition of the oxide, those processes which affect the oxide condition are the most critical steps in the fabrication sequence.

2.3.2 Thermal Oxidation

Frosch and Derrick[30] in 1957 showed that silicon surfaces could be oxidized to form a mask for the diffusion step which forms the various regions of a transistor structure. Atalla et al.[5] showed how the oxide passivates the surface, making the underlying device insensitive to the ambient gas, and thereby stabilizing the electrical parameters of the device. At the 1960 Electron Devices Meeting, Hoerni[51] showed how the above described properties could be combined to make planar transistors and diodes.

Ligenza and Spitzer[76] prepared oxides using combinations of O^{16} and O^{18} isotopes to study the mechanisms for silicon oxidation. By measuring the infrared transmission through these oxides as a function of oxide layer thickness as the oxide layer was etched away, they were able to determine that the diffusing species during oxidation is oxygen. They noted that an oxygen exchange occurred during the oxidation process at a rate at least as fast as the rate of growth. They inferred that the actual oxidation and the rate limiting step takes place at the silicon oxide interface. Pliskin and Gnall[96] used a selective etch technique to again show that the oxidation takes place at the silicon interface.

Jorgenson[63] applied an electric field across the oxide during oxidation and showed that the dependence of the oxidation rate on the field strength and polarity is such as to indicate that oxygen ions are the predominant species diffusing through a growing oxide film. Goetzberger[35] recently showed that oxidation in an electric field can reduce the densities of surface changes in steam or wet oxygen oxidations. No influence on field was found on surface charge density during dry oxygen oxidations. Schmidt[111] prepared sodium free oxides that changed by less than 10^{11} charges per cm^2 in steam at 300°C for 26 hours with a field of 10^6 v/cm, with the silicon negative.

Deal[21] studied the oxidation of silicon in dry oxygen, wet oxygen and steam. He found that wet oxygen produced oxides with the best protective characteristics from the standpoint of density, dielectric strength, masking ability, and freedom from defects.

Fuller and Streiter[33] reported on similar work which agrees with that of Deal. Ligenza[77] studied the oxidation of silicon by high pressure steam (25 to 500 atmospheres).

Deal and Sklar[20] studied the oxidation of heavily doped silicon.

Lieberman et al[75] studied the effects of water vapor pressure on the rate of thermal oxidation of silicon.

2.3.3 Oxide Properties

A good recent review article on the formation and properties of oxides on silicon has been prepared by Donovan[23]. He discusses the kinetics of various oxidizing reactions and the results from typical experimental systems. He also describes several models for the accumulation of electrons near the surface of oxidized silicon.

2.3.4 Other Oxidation Processes

A number of other processes have been studied for forming oxides on silicon which at the time of this writing have not found favor with the producers of MOS devices. Ligenza[78] has oxidized silicon in an oxygen gas plasma excited by a microwave generator.

Pliskin and Lehman[95] studied pyrolytically deposited films because of their lower deposition temperature. Such an oxide deposition leaves the silicon surface undisturbed. These considerations are important when there is concern about the changes that may take place in the silicon during oxidation. They developed a technique for densifying pyrolytically deposited films to improve their effectiveness as passivation layers and diffusion masks.

Peterson et al[94] reported on a chemical vapor deposition technique. Valletta et al[132], and Fuller and Baird[32] formed films by reactively sputtering a silicon cathode in oxygen. Ligenza and Povilonis[79] sputtered silicon through an oxygen plasma to form silica layers on silicon at substrate temperatures down to 25°C.

Pliskin[99] evaporated SiO_2 with an electron gun.

Schmidt and Owen[108] used a wet anodic process to form oxides at room temperature. Duffek et al[24] anodically oxidized silicon in ethylene glycol solutions. Tokuyama[130] formed a two-layer oxide in which the outer layer consisted of a mixture of PbO and SiO_2. Tung and Caffrey[131] deposited oxide on silicon by reacting a metal halide with a hydrogen-carbon mixture.

2.4 Techniques for Evaluation of Oxides

This subsection reviews the various experimental techniques which have been used to evaluate and study the properties of oxides and are described in the literature.

2.4.1 Capacitance-Voltage Relationship

A simple and useful measurement is that of the capacitance of an MOS capacitor as a function of such variables as the applied d-c voltage, the measurement frequency or the temperature.

Terman[128], and Lehovec et al.[72] measured the capacitance of MOS diodes as a function of the applied d-c voltage and the measurement frequency. They made an effort to locate energy levels in the energy gap and to evaluate the associated time constants.

As investigators became aware of the utility of the C-V measurement technique, a number of papers were published describing its use. The team consisting of Grove, Snow, Deal, and Sah published[39-41,43] a number of papers describing how C-V characteristics uncovered a variety of pieces of information about the oxide behavior.

Other authors have also written papers[22,54,73] describing the manner in which C-V measurements can be used to study oxide properties.

Sprague et al.[123] have studied oxide properties in MOS capacitors with the emphasis on the properties desired for good capacitors -- permittivity and loss tangent.

Snow[119] has used C-V measurements on two-layer (glass and oxide) MOS structures to study the movement of ions in glasses.

Zaininger and Warfield[143] have recently discussed the limitations of the MOS capacitance method for the determination of semiconductor device properties.

2.4.2 Conductivity Measurements

Lehovec[74] used a capacitor with a large circumference-to-area ratio to study the migration of charges in the region surrounding the metal electrode of an MOS capacitor.

Heiman et al.[45], and Clark[16] have discussed ways to determine the conductivity type of the silicon in MOS diodes.

Hofstein[55] has shown that the measurement of channel d-c conductance of an MOS transistor has an advantage over capacitance measurements in that faster response times can be measured.

Goetzberger[34] developed a technique using a ring-dot structure that permits measurement of the conductance of inversion layers under oxides which have not been subjected to the diffusions necessary for a MOS transistor structure.

2.4.3 Other Measurements

Although the C-V and conductance measurements have found the widest use, other evaluation techniques are available. Heiman and Miiller[47] suggest a way in which a temperature coefficient of MOS transistors can be used to determine the surface state density.

Nicollian and Goetzberger[89] combined C-V measurements with measured losses in an MOS capacitor to evaluate surface state parameters.

Shockley et al.[116,117] used surface potential measurements to study charge motion over the surface of the oxide.

Yamin[140] studied d-c current properties of oxides. Such measurements permit the study of various kinds of electrolytic effects, charge storage, rectification at boundaries, etc.

Lindmayer[81] investigated transient currents to study charge trapped in SiO_2 and SiO.

Green and Nathanson[37] used a scanning electron microscope to observe inversion layers under insulated gate electrodes.

Green et al.[36] mention that one can use an electron beam of varying energy to study the location within the oxide of radiation damage sites that affect device performance.

Pliskin and Lehman[98] have evaluated structural differeneces, density, porosity, refractive index and passivation efficiency by means of infrared absorption spectroscopy, preferential etch procedures, and technique known as VAMFO (Variable Angle Monochromatic Fringe Observation)[97,100].

Infrared transmission measurements can be used[1] to determine the pressure of "water" in the form of OH groups in fused silicon.

Rosier[105] made a special diode structure to measure the surface recombination velocity beneath an oxide as a function of the voltage applied to a metal electrode on the oxide.

Grove and Fitzgerald[42] introduced sodium ions into the oxide covering a p-n junction to create higher fields which enable them to show that anomalous channel currents are due to a breakdown mechanism in the channel.

Schroen[112] used a spot of light to create non-equilibrium carriers in small local areas to affect the breakdown voltage of p-n^+ junctions and MOS structures to study the distribution of traps.

2.5 Model for Oxide Structure and for Oxide Dependent Behavior of Devices

2.5.1 Glasses

The oxide on oxidized silicon is amorphous SiO_2. It is in the glasslike or vitreous state, a state believed to be a solid with the disorder of a liquid frozen into its structure. Although the history of man's work with glass spans a greater time than his work with most other materials, there still is disagreement over the theory of glass structure.

The first real advance in the theory of glass structure was due to the development of the random network theory which describes glass as lacking symmetry and periodicity in contrast with the srystalline state. The competing theory says that glass contains microscopic crystals with definite stoichiometric compositions joined together by amorphous zones. More detailed discussion of glass structure may be found in several references, including 56 and 138. In 1932 a number of simple rules were proposed relating the way oxygen anions and the cations must link together for an oxide to exist in the glassy state. Briefly, the rules state that the glass forming cations (e.g., B^{3+}, Si^{4+}, P^{5+}) are surrounded by polyhedra of oxygen ions in the form of triangles or tetrahedrons. The oxygen ions are of two kinds, viz., bridging oxygen ions, each of which link two polyhedra, and non-bridging oxygen ions, each of which belongs to only one polyhedron. Such a system would produce a polymer structure with long chains cross linked at intervals. In such a structure, there are regions of unbalanced negative charge where the oxygen ions are non-bridging. Cations of low positive charge and large size (Na^+, K^+, Ca^{2+}) may exist in holes between oxygen polyhedra where they compensate the excess negative charge of the non-bridging oxygen atoms.

Some cations of large charge and small size may isomorphically substitute silicon ions in the structural network of the glass. Oxides forming the basis of a glass are called network formers, and those which are soluble in the network are network modifiers.

It has been established that glasses can be formed of B_2O_3, SiO_2, GeO_2, P_2O_5, As_2O_5, As_2O_3, and Sb_2O_3. Possible glass formers include V_2O_5, ZrO_2, and Bi_2O_3. Oxides of Ti, Zn, Pb, Al, Th and Be do not apparently form glasses but they modify certain properties of glass. Oxides of Sc, La, Y, Sn, Ga, In, Mg, Li, Ba, Ca, Sr, Cd, K, Rb, Hg, and Cs may act as network modifiers.

2.5.2. Silicon Oxide

Donovan[23] has written a good review paper on the properties of oxides on silicon. He notes that silica glass is thermodynamically unstable below 1710°C and should devitrify to a stable crystallized form. However, the rate of devitrification is negligible at temperatures below 1000°C. Silicon ions, due to their large charge, cannot move without breaking four oxygen bonds. Oxygen ions, on the other hand, are freer to move through the lattice, since bridging oxygen ions are attached to only two silicon ions and non bridging atoms to only one. A network modifier, when introduced as an oxide, ionizes and gives up an oxygen atom to the network. The modifier metal ion occupies an interstitial position in the network and the oxygen ion enters the network, producing two non bridging oxygen ions where formerly there was one bridging oxygen ion. This weakens the network, as manifested by a lower melting point.

The water content of silica glass is regarded as an important factor in determining its properties. Water vapor can enter the silica glass network either as hydroxyl ions or molecular water, or both. The hydroxyl ion can also be formed by the attachment of hydrogen ions to nonbridging oxygen atoms, producing a tightly bound stable hydroxyl ion, or it may be formed in less stable configurations by other hydrogen-silica reactions. These hydroxyl ions are not contained in water but may produce the same net effects as water, because the effects of water may be totally due to the hydroxyl ions.

The presence of hydroxyls in silica glass tends to weaken the structure by breaking oxygen bonds and replacing them with singly-bound hydroxyl ions. The effect is analogous to changing bridging oxygen ions to nonbridging oxygen ions.

Donovan further reports that when divalent ions such as Ca^{++} or Sr^{++} are introduced to silica, the mobility of alkali ions in the silica decreases.

2.5.3 Charge Motion in Silica

Greater detail and depth concerning some electrolysis phenomena and the effect of water in vitreous silica can be found in references 7, 25, and 49.

Proctor and Sutton[101] have studied the motion of ions in glass. The observed behavior agrees with a model in which cations are mobile but anions are not.

Collins[17] has proposed several mechanisms to explain the polarization of charge in oxide films.

Owen and Douglas[91] examined the d-c electrical conductivity of various samples of fused silica and found it to depend particularly on the sodium concentration. The d-c conductivity is substantially independent of the water content, whereas the dielectric properties are almost entirely determined by the water content. The nature of d-c conductivity is discussed in greater detail by Owen[92].

The motion of surface charge on the oxide[8,86,93] was described as the mechanism responsible for the failure of Telstar. Shockley et al.[116,117] used a Kelvin probe to show that the motion of charges along oxide-covered silicon surfaces can form channels and/or change the device characteristics.

Castrucci and Logan[12] have used a diode structure with a control ring electrode to study the effects of charge motion parallel to the oxide surface.

2.5.4 Structure of Silicon Dioxide

Revesz[103] has recently reviewed the structure of grown silicon dioxide films from the viewpoint of a physical chemist. The defect structure is shown to determine many of the phenomena observed in MOS devices. This defect structure is quite sensitive to variations in oxide growth techniques and to the thermal and ambient gas treatments following the formation of the oxide. According to the proposed model, thermal growth of silicon dioxide proceeds through the migration of oxygen interstitials which act as acceptors. The presence of water in the oxidizing ambient, an aftertreatment in hydrogen, or some reactions with the gate metal introduce a donor state in the form of trivalent silicon. Due to electronic interactions between the oxide and silicon, these defects influence the silicon surface potential and therefore they are similar to the surface states. The silicon surface potential can be affected by injecting positive metal ions into the oxide and by moving ionized and/or injected ionic defects in the oxide.

Besides the relationship between defects and oxide growth, Revesz discusses the interactions between the silicon and its oxide, reactions at the gate-oxide interface, and the effects due to an inhomogeneous distribution of defects.

2.5.5 Semiconductor-Oxide Interface

Schmidt and Sandor[109] reviewed the state of knowledge concerning the semiconductor-oxide interface. They discuss how the various properties of the silicon surface change with thermal oxidation of the surface. For example, oxidiation may tie up dangling bonds at the surface and thereby reduce the density of fast states. On the other hand, states located within the oxide, which are not in intimate electrical contact with the silicon, are observed as slow states which are added during the oxidation.

Some of the important properties of the oxide-semiconductor interface can be predicted when the interface is treated as a heterojunction, as discussed by Lindmayer[80,82].

Schmidt[110] describes the effect of protons and alkali ions in oxide films on the surface recombination velocity. These impurities in the oxide are presumed to change the

Fermi level in the oxide and thereby cause a charge transfer between the oxide and the silicon.

2.5.6 Heat Treatment

Seraphim et al.[113] have studied the effects of chemical additives and of annealing procedures, and have listed some of the electro-chemical reactions that might take place within the oxide.

Since heat treating processes are known to induce large changes in MOS device characteristics, it is worth noting that Schmidt and Sandor[109] measured compressive stresses of 50,000 psi on steam- and dry oxygen-oxidized thin silicon webs, and that Griggs and Blacic[38] report that the strength of synthetic quartz crystals containing water is a hundredfold lower at 600°C than at 300°C. Fuller and Logan[31] reported that donors are introduced into silicon by heating in the 300°C to 500°C temperature range and are caused to disappear at higher temperatures. They give evidence showing that oxygen is the impurity from which the donors are formed.

2.5.7 Model of MOS Capacitor

The most useful tool for studying the charge in oxides is the measurement of the capacitance as a function of the voltage. The basic physical principles involved have been described in a number of papers[29,39,40,43,73,129].

Figure 4 shows the MOS capacitor structure and how the characteristic C-V curve is established. For n-type silicon, when positive voltage is applied to the metal, electrons accumulate at the silicon surface adjacent to the oxide. In this case, the capacitance is insensitive to the applied d-c voltage and is that capacitance due to the thickness and dielectric constant for the oxide. If a negative voltage is applied to the metal, the electrons are repelled and a depletion layer forms. The formation of this depletion layer effectively forms a wider spacing of of the capacitor and the capacitance decreases. As higher negative voltages are applied, an inversion layer of holes forms in the layer of silicon adjacent to the oxide. The area density of charge in this inversion layer can vary greatly with applied voltage (as described by the Boltzmann equation). Therefore, further increases in applied negative voltage are supported by an increased field across the oxide without significant change in the field within the depletion layer. For this reason, the depletion layer width becomes insensitive to applied voltage when the inversion layer exists. Since the depletion layer width is insensitive to voltage, the capacitance is insensitive to voltage. This voltage insensitivity at the higher negative voltages is only observed at high measurement frequencies.

If the measurement frequency is sufficiently low that the density of holes in the inversion layer can change during one cycle of the measurement signal, then the a-c signal voltage is supported entirely by the varying field across the oxide and one again measures a capacitance due to the oxide. The frequency at which the low frequency characteristics are observed depends on the ability of the holes density to change rapidly. One finds, therefore, that the low frequency characteristic curve can be observed at higher frequencies when the

a. Generation rate for carriers is increased by heating the silicon or exposing it to light or other irradiation,

b. Region near the inversion layer has a high density of holes which can move into and out of the inversion layer quickly[53].

The transition voltage of an MOS capacitor is that voltage at which the slope of the C-V curve is maximum. The transition voltage is closely related to the surface potential that exists in the silicon when no voltage is applied. This surface potential is dependent on the distribution of charge in the oxide and/or at the oxide-silicon interface. One can determine from the C-V curves the effective density of charge in the oxide or at the surface.

One can study the effects of heat treatment, aging under an applied bias voltage, or of irradiation on the charge in the oxide by examining the change in the C-V curve.

Snow et al.[118] have developed a model for the ionic motion in the oxide which is in excellent agreement with the experimental results. It is based on a division of the oxide into two regions:

1) A thick boundary layer near the metal-oxide interface in which ion transport is by diffusion, and

2) The remainder of the oxide where field drift dominates.

Analysis of the C-V curve can be extended to study the distribution and time constants of traps or slow states as described in reference 48.

2.6 Empirical Findings and Efforts to Develop Improved Oxides

This part of the literature review is intended to present a body of published information that has been recorded by investigators who are studying the effects of various oxide preparation and treatment processes with the purpose of creating improved oxides. These empirical, and in many cases seemingly unrelated, pieces of information have not been well explained theoretically. However, this information, combined with similar information now being developed in various laboratories, must form the basis of a good basic theoretical understanding of the present problems of high threshold voltage and instability in MOS transistors.

2.6.1 Energy Band Diagram

Williams[139] experimented with the photoemission of electrons from silicon into silicon dioxide and was able to draw the energy diagram in Figure 4.

Besides uncovering energy relationships expressed in the diagram, he found traps in the oxide at a level below 2 eV below the conduction band of the SiO_2. He found that he could fill these traps by irradiating with ultraviolet light and then empty them with visible light. The density of traps

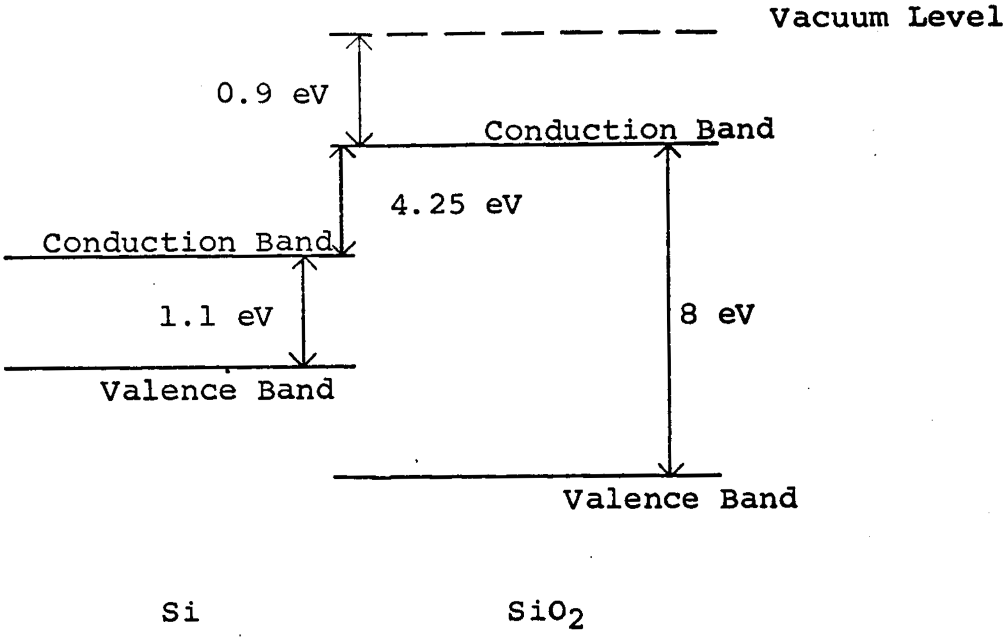

Figure 4.

was ~3 x $10^{14}/cm^3$ with a capture cross section of 10^{-12} cm^2. The mobility of electrons in the oxide is 20 to 40 cm^2 per volt-sec.

2.6.2 Asymmetry of Oxide Leakage Current

Hofstein[55] showed that in alkali ion-free oxides, ions suspected of being protons can be moved from the silicon toward the metal at a rate up to five orders of magnitude faster than movement from the metal toward the silicon. This, he postulates, is due to traps at the metal-oxide interface. The true charge mobility in the oxide is that represented by motion toward the metal.

2.6.3 Gold Doped Silicon

Sah et al[74] reported on how gold doping of the silicon affects the C-V characteristics of MOS capacitors.

2.6.4 Redistribution of Impurities During Oxidation

Deal et al[19] have found the MOS structure useful in the study of the amount of redistribution of various impurities during thermal oxidation.

2.6.5 Hydrogen and Hydroxyl

Lee[68-70] has done extensive work studying the diffusion of hydrogen in fused silicon and has discussed the role of the hydroxyl in this connection.

Heating (200 to 350°C, 5 min.) an MOS capacitor (p-type Si) in hydrogen causes an n-type inversion layer to form in the p-type silicon surrounding the metal electrode[9,142]. Olmstead et al[90] also report that heating in hydrogen (625°C, 15 min.) induces an n-type layer which can be removed by baking in oxygen, nitrogen, argon or vacuum (3 to 10 min. at 500 to 800°C). Balk[6] studied in detail the effects of hydrogen and inferred that the H_2 treatment annihilates fast states. Balk says that if these states are related to vacancies accompanied by chemically unsaturated bands and unpaired electrons near the interface, then the H_2 annealing may chemically saturate these bands at the vacancies.

2.6.6 Heat Treatment

Lehman[71] has studied the effects of various fabrication variables, such as the gate metal, heat treatment temperature or ambient gas, on the surface conduction properties of passivated junction devices. The effects of low temperature annealing were described by Cheroff et al[15,14].

Revesz and Zaininger[104] have discussed the influence of oxidation rate and heat treatment on the surface state density. They mention that the presence of boron and SiO_2 is thought to facilitate the incorporation of hydroxyl through defect reactions.

Stickler[125] studied the structure of thermally grown oxides as a function of various heat treatments and found that uniform films can be obtained which contain gross defects such as cracks resulting from specialized heat treatments.

2.6.7 Phosphosilicate Layer

A variety of independent experiments[61,65] have shown that the presence of a phosphosilicate layer over the oxide has a stabilizing effect on the electrical properties of the oxide and oxide-silicon interface.

2.6.8 Charge Species Responsible for Oxide Instability

The identity of the cationic species responsible for oxide instability has not been definitely determined. It has been suggested by Thomas and Young[129], and by Seraphim et al.[113] that the cation may be an oxygen vacancy in the oxide film. This seems implausible in view of recent measurements of the diffusion constant and diffusion activation energy of the ionic species responsible for polarization of the oxide[17]. Hydration of the oxide has been shown by Kuper and Nicollian[67] to set up a condition of reversible instability.

2.6.9 Impurities

Snow et al[118] and Logan and Kerr[84] have intentionally contaminated oxides with alkali ions and have shown that such oxides exhibit the instabilities found in planar passivated transistors and MOS devices.

Busen and Lindmayer[11] have studied the effect of impurities and structural parameters on silicon/silicon oxide interfaces and related the results to their heterojunction model.

Seraphim et al.[113] have found that when the SiO_2 is doped with B_2O_3 and is then electrically biased, it is possible to cause the charges to move within its oxide to the point where after the bias is removed the silicon surface potential is positive.

Yamin[141] found that diffusion of boron into a phosphorus-stabilized oxide destroys the stabilization, while even a light phosphorus diffusion over a boron-diffused oxide restores the stability.

2.7 Radiation Effects

2.7.1 Optimistic Predictions

It was predicted[133,134] that MOS transistors might be more tolerant of radiation than bipolar transistors because they are majority carrier devices. In this reasoning, the assumption was made that the failure mechanism would be either degradation of mobility or change in the density of mobile charges.

2.7.2 Gamma Radiation

Unfortunately, when MOS transistors were tested by Hughes and Giroux[57] in a Co^{60} source, it was discovered that the channel conductance and transconductance were severely degraded by exposure to 2×10^5 rads, even though the bulk conductivity and lifetime changes are negligible to absorbed dose levels of 10^6 rads. This degradation was attributed to ionization in the transistor by Compton electrons produced by the gamma radiation.

Hughes and Giroux[58] used an MOS structure to study the effects of ionizing radiation on the $Si-SiO_2$ interface. They found that the leakage current increase that caused the Telstar failure (which was explained by Blair[8] and Peck, et al.[93] as being due to ionization of the gaseous ambient and the subsequent drift of these ions in the fringing electric field at the edge of the junction) could be duplicated on devices in a vacuum of $<10^{-9}$ Torr.

Sonder and Templeton have studied the energy levels introduced in silicon in gamma radiation[120-122].

2.7.3 Fast Neutrons

Raymond et al.[102] irradiated MOS transistors with fast neutrons up to 5×10^{14} NVT and found that the most significant neutron-induced parameter change is in the threshold voltage. Although they noted that comparison of the behavior of the MOS and the bipolar transistor is difficult because of the lack of good criteria, they concluded that MOS transistors have shown a potential advantage in radiation environments compared to junction and bipolar transistors.

Messenger[85] exposed MOS transistors to reactor neutrons and showed that the neutrons produced displacement damage in the form of positively charged oxygen vacancies in the oxide lattice or at the Si-SiO_2 interface.

2.7.4 Electron Irradiation

The effects of electron (1.5 MeV) irradiation on P-MOST's were examined by Stanley[124]. He found the drain leakage current to rise beginning at a dose level of about 5 x 10^{12} electrons/cm^2. The turn-on voltage increased with total electron flux, and after a total dose of 5 x 10^{14} e/cm^2 it was no longer possible to turn on the device. After irradiation the leakage current decayed very slowly, reaching the pre-irradiation level after several months storage at room temperature. This was accompanied by a very gradual lowering of turn-on voltage. Stanley explained these results in terms of an induced n-type inversion layer in the p-type drain region.

Szedon and Sandor[127] used low energy (10-16 KeV) electrons to irradiate MOS capacitors. They found that a positive charge was induced in the oxide and were able to remove it by annealing for fifteen minutes at 150 to 200°C.

Green et al.[36] mention that electron irradiation of varying energy can be used to study the location of damage sites that affect device performance.

2.7.5 Flash X-Ray

Sullivan[126] studied the response of MOS transistors to flash X-ray radiation, and found that the principal effects were leakage current through the oxide between the gate and substrate and through the drain-substrate p-n junction.

Kreuger and Griffin[66] also used flash X-ray radiation and studied the effect on both p-channel and n-channel silicon MOS thin-film transistors on a sapphire substrate. They noted that such devices were easier to analyze because they have a lower level of isolation junction photocurrent.

2.7.6 Ionization in Gas Discharge

Estrup[26,27] has used a gas discharge to create both positive and negative ions which he used in a variety of ways to study the surface effects of gaseous ions and electrons on semiconductor devices.

2.7.7 Improved Resistance to Radiation

It has been reported[144] that silicon planar transistors which had had the oxide formed in dry oxygen show a higher tolerance level to radiation than do oxides formed in wet oxygen.

2.8 Conclusions

This body of literature provides the necessary background to support a better understanding of the present status of MOS and related planar device technology as a basis for further experimental work and for predicting technologies which are likely to result in improved MOS devices.

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