AN ALGORITHM FOR DETERMINING PROGRAM FEASIBILITY OF A MULTI-MODE PAM COMMUTATOR TELEMETRY SYSTEM

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TECHNICAL REPORT NO. 10

SYSTEMS ENGINEERING GROUP

BUREAU OF ENGINEERING RESEARCH

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ABSTRACT

This is the tenth report in a series of technical reports concerned with the Telemetry Systems to be used on the Saturn Vehicle. It is concerned with the design of an appropriate algorithm for evaluating strapping arrangement programs for an All Purpose PAM Multi-Mode Commutation System.

Both manual and digital computer methods for programming commutators to the gates of the master control unit of an M Channel Multi-Mode Commutator System are included. Additionally, the algorithm has been used to determine all feasible programs for a 30-Channel Multi-Mode Commutator System and the results are summarized as an Appendix to the report.

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I. INTRODUCTION

The 30-channel multi-mode pulse amplitude modulated (PAM) commutator system is a solid state system consisting of a master control unit, high level commutator units, and/or low level commutator units. A simplified schematic of the PAM System is shown in block diagram form in Figure 1. System output is a 50 percent duty cycle pulse train (pedestal synchronization optional) as illustrated in Figure 2. Output repetition rate is 3600 pulses per second (pps) with an amplitude from zero to five volts making it suitable for modulating a 70 kilocycle ($\pm$ 30%) sub-carrier oscillator in a frequency modulated telemetry system.

THE MASTER CONTROL UNIT

The master control unit is basically a 30-gate, two pole, 100 percent duty cycle, sequencer switch. It opens its gates (1 through 30) sequentially and each gate receives a sampling of 30 channels (i.e. one frame) from each commutator. It scans each of the 30 channel high and low level commutator outputs four times each second. This makes it possible to transmit as many as 900 channels (30 gates x 30 channels/gate). Each gate samples at a rate of four samples/second. Consequently, each of the 30 gates is opened at the rate of 120 gates/second which results in each gate being opened for 1/120 second or 8.3 milliseconds. This permits exactly one frame from a 30 channel commutator (see Figure 2) to pass through the opened gate.

HIGH AND/OR LOW LEVEL COMMUTATOR UNITS

Each high and/or low level commutator has 30 channels, namely, 27 data channels and 3 sync channels. They contain an internal clock for independent operation and may also be synchronized from an external source such

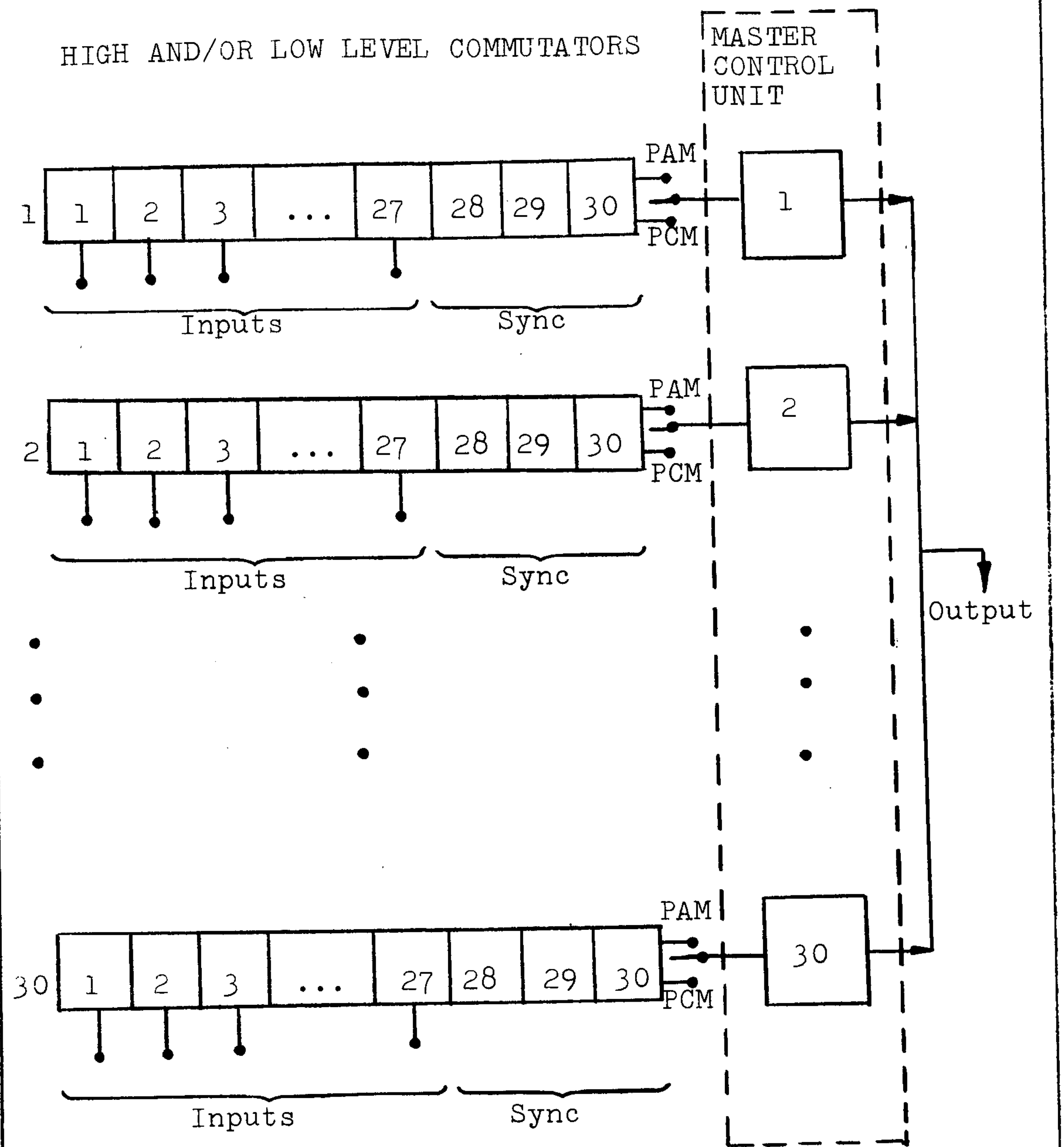
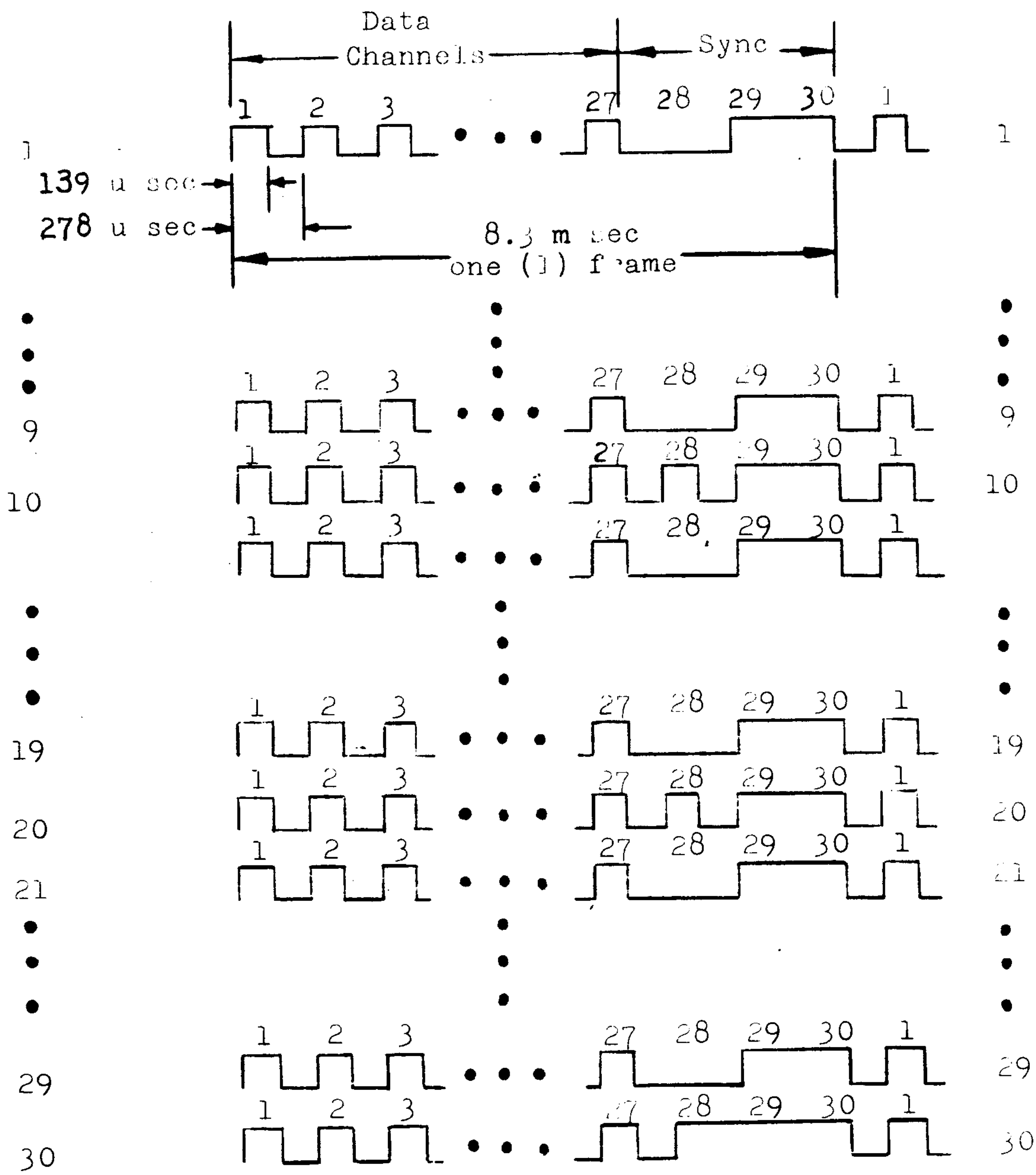


FIGURE 1. An All Purpose PAM Commutation System (30 Channel Multi-Mode Commutator System)



NOTE: 1. Frames 1-10, 11-20, 21-30 are called Master Sub-frames.

2. Frames 1-30 are called Master Frames and represent one complete scanning of the master control unit gates.

FIGURE 2. System Output

as the master control unit. Commutator units may be operated individually or in conjunction with the master control unit. They may be procured either with or without pedestals which are internally generated pulses of one-volt amplitude. Low level commutators are designed to accept signal inputs from zero to 50 millivolts. High level commutators are designed to accept signal inputs from zero tc five volts.

As previously noted each high and low level commutator has 30 channels. One complete scan of the 30 channels is identified as a frame. Each of the 30 channels is sampled at a rate of 120 samples/sec. This rate is equivalent to 120 frames a second or 3600 channels a second (30 channels at 120 samples a second). Sampling time for one channel is 1/30 of 8.3 milliseconds which equals 279 microseconds (μ sec). Channel-on-time is 50 percent of 279 μ sec which equals 139 μ sec (see Figure 2).

OPERATING MODES

The system may be operated in any one of the following modes:

(1) Commutators operating serially under the control of an internally synchronized master control unit.

(2) Commutators operating serially under the control of the externally synchronized master control unit.

(3) More than one master control unit may be synchronized by an external source such as a pulse code modulated (PCM) programmer.

Each of the commutators used in the system may also be used independently of the master control unit in the following modes:

(1) Each commutator operating under the control of its own internal clock (free-running).

(2) Each commutator operating under the control of an external clock other than the master control unit.

SYNCHRONIZATION AND IDENTIFICATION

Synchronization and identification within the output wave train is provided for the master frame, the master sub-frames, and the commutator frame. It should be remembered that in this system a frame is referred to as one complete scanning of the 30 channels of a single commutator. A master frame is one complete scanning of the 30 gates of the master control unit, and a master sub-frame is the scanning of gates one through ten, eleven through twenty, or twenty-one through thirty of the master control unit.

MASTER FRAME. Each gate of the master control unit has two poles, one of which scans the commutator outputs with pedestals (for PAM applications); the other pole scans the commutator outputs without pedestals (for PCM applications). Master frame synchronization is achieved as follows: when gate 30 of the master control unit is sampling, a pulse from the master control unit is applied to all commutators. This causes a five-volt pulse for 100 percent duty cycle to appear on the outputs of channel 28 of all commutators. As shown in Figure 2, channels 28 and 29 and the first 50 percent of channel 30 now appear as one continuous pulse of five volts amplitude within the output wave train.

MASTER SUB-FRAMES. Master sub-frames are identified by a five volt pulse for 50 percent duty cycle which appears on channel 28 of each commutator when gate 10 of the master control unit is sampling, and again when gate 20 is sampling (see Figure 2). This pulse is the result of a signal from the master control unit which is applied to the commutators.

COMMUTATOR FRAME. The last three channels (28, 29 and 30) of each 30 channel commutator frame are reserved for synchronization. This produces a total of 90 channels (3 channels x 30 commutators) to be used for servo reference and frame identification. Therefore the system has a maximum capacity of: 900-90 = 810 information channels. Each commutator is thus capable of producing its own frame identification. This identification consists of a five-volt pulse on channel 29 and the first 50 percent of channel 30 (see Figure 2).

OUTPUT IDENTIFICATION. The output of the master control unit bears the following identification:

(1) Each frame of the 30 channel output of an individual high and/or low level commutator that passes through a gate of the master control unit ends with a five-volt pulse one and one-half channels (29 and 1/2 of 30) in duration.

(2) The 10th and 20th frames (master sub-frames) end with a five-volt pulse one half channels in duration (1/2 of channel 28) followed by another five volt pulse one and one half channels (29 and 1/2 of 30) in duration.

(3) Every 30th frame (master frame) ends with a five-volt pulse two and one half channels in duration (28, 29, and 1/2 of 30).

OPERATION

The system is extremely flexible in its application and may be programmed in many different ways to produce a variety of different sampling rates and numbers of channels. Since sampling rate requirements vary with the nature of the information being sampled, the fact that the system provides sampling rates from four frames or 120 samples a second to 120 frames or 3600 samples a second makes it unique in telemetry application. Different sampling rates are obtained by strapping a single commutator to more than one gate of the master control unit. Figure 3 illustrates how five commutators might be programmed if each commutator is strapped to six gates of the master control unit. This particular program provides 150 channels each sampled at a rate of 24 samples a second. Many other programs are made possible by the fact that several commutators each strapped to a different number of gates of the master control unit may be simultaneously used in combination. Symmetrical sampling is used in programming the system to facilitate reconstruction of input data and to simplify the identification and separation of individual outputs.

PRESENTATION

Obviously if the system is to be effectively utilized, a method of programming the commutators to the gates of the master control unit to produce desired sampling rates and channel capacities must be available. This report presents an algorithm for programming which is designed to achieve this purpose. It should be emphasized that the following discussion does not consider the ways in which inputs may be strapped to more than one of the 27 channels of a commutator, but rather with strapping the output of one or more commutators to one or more of the gates of the master control unit.

Chapter 2 presents the underlying logic and development of the programming algorithm.

Chapter 3 illustrates the manual application of the designed algorithm to determine the feasible strapping arrangement programs available when using the 30-Gate (Channel) Multi-mode PAM Commutator System. A procedure is also presented for program selection. Specific strapping arrangements for the 30-channel system are attached as Appendix B.

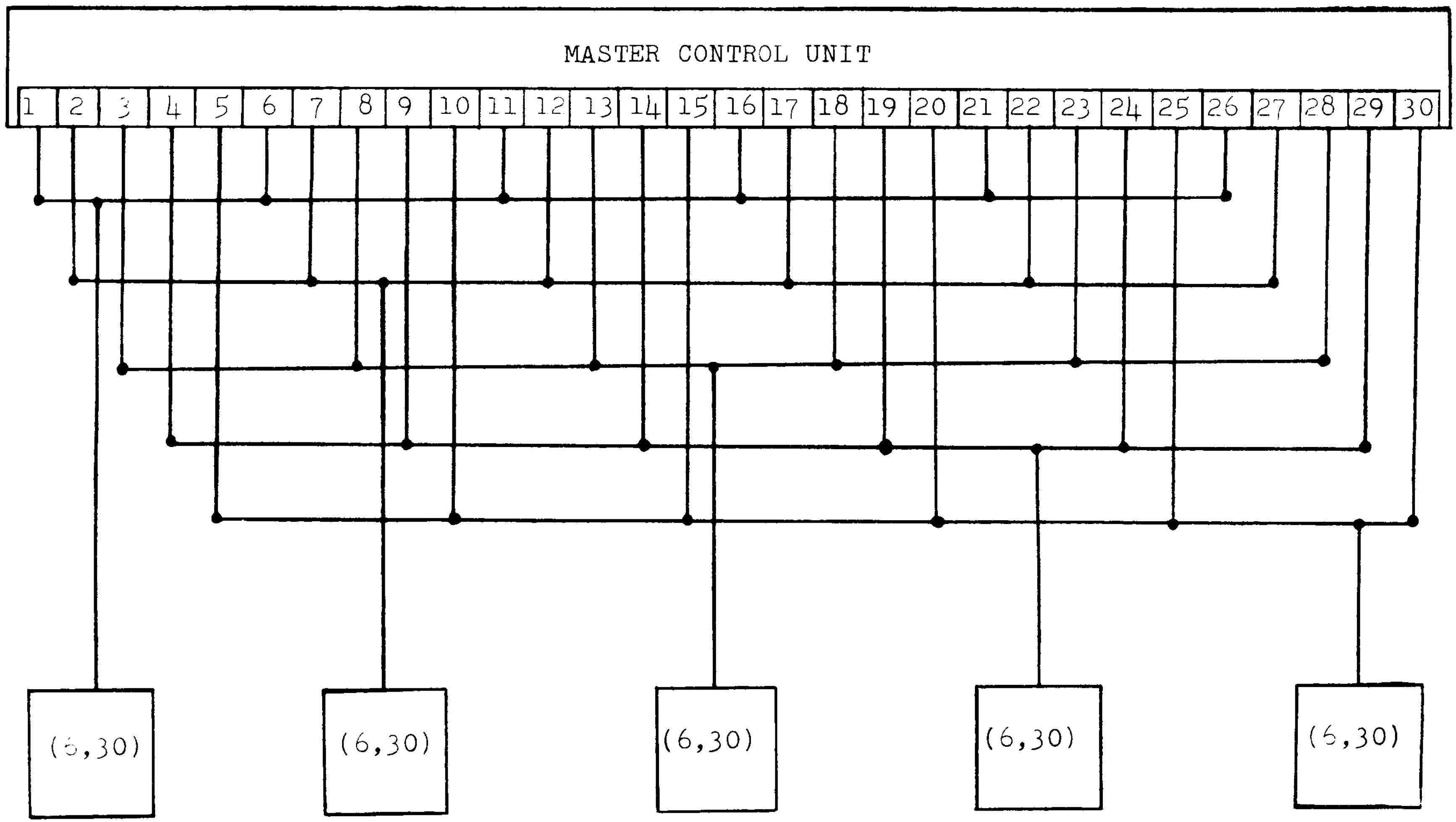


FIGURE 3. Schematic Diagram of a Strapping Arrangement Program When Using Five Type (6, 30) Commutators

Chapter 4 describes a Fortran IV Computer program written for the UNIVAC 1107 to permit the computer programming of an M-gate PAM Commutator System. It is anticipated that the material presented will be of significant value in the design of future systems.

The report is summarized in Chapter 5. Recommendations are also presented for further research to expand the capabilities of the 30-Channel Multi-mode Commutator System.

II. PROGRAMMING LOGIC

This chapter presents the underlying logic and design of an algorithm for programming a multi-mode commutator system with any number of master control unit gates. The derived algorithm may be used to systematically determine feasible combinations of sampling rates and channel capacities, and the strapping arrangements they require. Initially, the basic design problem will be summarized and then analyzed in terms of program criteria and programming requirements. After this has been accomplished, the basic structure of the programming algorithm will be described.

THE BASIC PROBLEM

From a design viewpoint, the basic problem with which we are concerned is the establishment of a systematic computational procedure or algorithm for programming a multi-mode commutator system. Ultimately, the unique ways in which the output of one or more commutators may be feasibly strapped to the gates of the commutator system's master control unit must be determined. As used here, a strapping arrangement's uniqueness is evaluated in terms of the particular channel capacities it offers at specific rates of sampling. Its feasibility is determined by whether or not it fulfills all system requirements; i.e., symmetrical sampling, complete utilization of gate capacity, etc. The basic inputs to the programming algorithm are master control unit gate capacity, channels per commutator available, and master control unit scanning rate.

PROGRAM CRITERIA

A feasible commutator program may be defined as a unique strapping arrangement using one or more commutators in such a way that all of the gates of the master control unit are utilized and all restrictions are met. For programming purposes, it will be convenient to classify the commutators used by two parameters - (1) the number of master control unit gates to which they are attached and (2) the number of channels they possess. Letting g indicate the former and N the latter, a particular commutator will be designated as Type (g, N). As an example, Type (15, 30) would indicate a 30 channel commutator attached to 15 master control unit gates. A particular program may thus be described in terms of the set of commutators used and then identified and evaluated in terms of its channel capacities and sampling rates. Let us now consider how these two criteria are computed.

CHANNEL CAPACITY. System channel capacity is restricted in any multi-mode commutator system when a single commutator is strapped to more than one gate of the master control unit. Maximum system channel capacity occurs when each commutator included in a program is attached to a single master control unit gate. Consequently, if a set of commutators included in a program each has N channels and each is attached to a single gate of a master control unit which has M gates, a maximum system capacity of MN channels occurs. Conversely, a minimum system channel capacity of N channels occurs if a single commutator is attached to all of the M master control unit gates available. Hence, it becomes apparent that system channel capacity may vary from N to MN channels. If a program is composed of only one type of commutator, the system channel capacity, C, may be determined as:

$$C = N\,(M/g);\ \text{where}\quad 1 \leq g \leq M.$$

This is true because M/g will indicate the number of commutators used. It should be noted that essentially each commutator used retains its N channel capacity and changes only in sampling rate when strapped to more than one gate.

Consequently, the above system channel capacity relationship may not be used if two or more different types of commutators are included in the program to be evaluated. When different types of commutators are included in a program, channel capacity will be evaluated by commutator type rather than on a total program basis. This aspect of program evaluation will be discussed in detail in this chapter.

SAMPLING RATE. Sampling rates of the multi-mode commutator system are a function of the r number of times a second each master control unit gate is opened, the g number of gates to which a specific type of commutator is strapped, and the N number of commutator channels. This functional relationship for determining the sampling rate in channels a second, R_c, may be stated as follows:

$$R_c = r\,Ng \quad \text{channels/second}$$

Sampling rates may also be expressed in frames per second (R_f) as follows:

$$R_f = r\,g \quad \text{frames/second.}$$

The sampling rate of each data channel is most usefully reflected in this form. This is particularly true from the users viewpoint since each commutator channel may conceivably be used to transmit data. For program evaluation purposes, sampling rates must always be stated in such a way as to relate them to a specific type of commutator.

PROGRAMMING RESTRICTIONS

In programming the multi-mode commutator system, three basic requirements must be met: symmetrical sampling must be used, joint occupancy of a master control unit gate must not occur, and each gate of the master control unit must be utilized. Each of these requirements restrict the way in which the system may be programmed and must be considered when determining program feasibility. As is inferred, a program is considered feasible only when all three of these requirements have been met.

SYMMETRICAL SAMPLING. At the present time the designers of the multi-mode PAM commutator system feel that a symmetry requirement is necessary to facilitate data reconstruction and to simplify the identification and separation of individual outputs from a specific location in the wave train. Symmetry, as used here, is defined as keeping a constant number of pulses between the successive outputs of a particular commutator. This requirement thus limits the number of ways and manner in which a single commutator may be strapped to the gates of the master control unit.

JOINT OCCUPANCY. The physical design of the multi-mode commutator system permits the input of only one frame to each of the master control unit gates. When this requirement is violated joint occupancy occurs. The fact that joint occupancy is prohibited results in two other restrictions in programming the multi-mode commutator system - a positional restriction and a combinatorial restriction.

Strapping of individual commutators to the master control gates is restricted positionally by the fact that even though a single commutator may be attached to more than one master control unit gate, it may not be attached to a single gate more than once. This restriction then limits the number of different ways (positions) in which a commutator may be strapped to the master control unit and will be referred to as the positional restriction.

Joint occupancy may also occur as the result of using a specific type of commutator in combination with one or more other commutators. Consequently, a combinatorial restriction analogous to the positional restriction is required to preclude the joint occupancy of a single master control unit gate by two or more different commutators. This means that even though two or more commutators may be attached simultaneously to the master control unit gates, more than one commutator may not be attached to the same gate.

MASTER CONTROL UNIT GATE CAPACITY. Although not an absolute necessity, it is highly desirable that all master control unit gates be utilized in programming the commutator system. Ordinarily, gate capacity will be specified on the basis of need. Therefore, unused gate capacity will be eliminated. Consequently, for programming purposes, feasible programs will also be restricted to those which fully utilize the available master control unit gate capacity.

THE PROGRAMMING ALGORITHM

Now that the basic design problem has been formulated and the programming restrictions summarized, the step-by-step development of the programming algorithm may be described. Basically, the algorithm may be divided chronologically into five steps:

1. Feasible commutator types are determined from the input of the number of master control unit gates available.

2. All of the specific ways in which each feasible type of commutator may be attached to the gates of the master control unit are then generated.

3. Feasible combinatorial positions based on the simultaneous use of two or more commutators are generated, their strapping arrangements specified and ultimately formed into programs.

4. The generated strapping arrangement programs are then evaluated in terms of channel capacities and sampling rates.

5. The procedure is completed by summarizing the generated programs to facilitate application.

DETERMINATION OF FEASIBLE COMMUTATOR TYPES. The symmetrical sampling requirement and the positional restriction primarily determine the types of commutators which may be used when programming a specific multi-mode commutator system. In addition, the number of master control unit gates to which a commutator may be attached obviously may not exceed the number of gates available. From the symmetry viewpoint a commutator may be attached to any number of the master control unit gates so long as that number is a factor of the total number of gates. Strapping a commutator to any other number of gates will result in a varying number of pulses between the desired measurements. Adherence to the preceding practice will also preclude the violation of the positional restriction. Capacity-wise the number of gates to which a commutator is attached must be equal to or less than the number of gates available. More precisely: $1 \leq g \leq M$. In summary, a commutator may be feasibly attached to any g number of the master control unit gates so long as:

1. g is a factor of M
2. $1 \leq g \leq M$
3. It is not attached to the same gate more than once.

Recall that commutators are classified by the number of gates to which they are strapped and their number of channels as Type (g, N). In practice, N will remain fixed. Therefore, we are concerned only with determining every feasible g which may be used when a particular multi-mode commutator system has been specified. The particular system used must be specified in terms of its master control unit gate capacity M for programming purposes. This immediately results in one determination since a g equal to M may always be used. A flow chart for determining the remaining g's which may be used is presented as Figure 4. The procedure essentially determines the factors of M which at the same time fulfills the other restrictions stated above. In application, the factors thus determined are then used to define the feasible commutator types. To illustrate the use of the procedure, consider two different multi-mode commutator systems which have 6 and 9 master control unit gates respectively. In the first case, K is computed as 6/2 or 3. The integers 1, 2, and 3 each divide evenly into 6 and therefore are retained indicating that four different commutator types may be used - Types (1, N), (2, N), (3, N) and (6, N). The last type included arises from the fact that a commutator attached to M gates will always be feasible. In the second case since 9 is an odd number, K is computed as (9 + 1)/2 or 5. The integers 1, 2, 3, 4, and 5 are successively divided into 9 and only 1 and 3 are retained. This indicates that three different types of commutators may be used in the system - Types (1, N), (3, N) and (9, N).

GENERATION OF PRIMARY STRAPPING POSITIONS. The previously noted positional restriction limits the number of different ways in which a single specific type of commutator may be strapped to the master control unit. This number of ways will be designated as P (g, N) and is equal to M/g positions. Each of the enumerated positions may be defined by the gates it includes as a subset of the universal set of all master control unit gates available. By knowing the number of positions in which a particular type of commutator may be used, it is possible to generate the set of gates required for each position. A flow chart of a procedure for generating these primary positions is presented as Figure 5. It is interesting to note that P (g, N) indicates not only

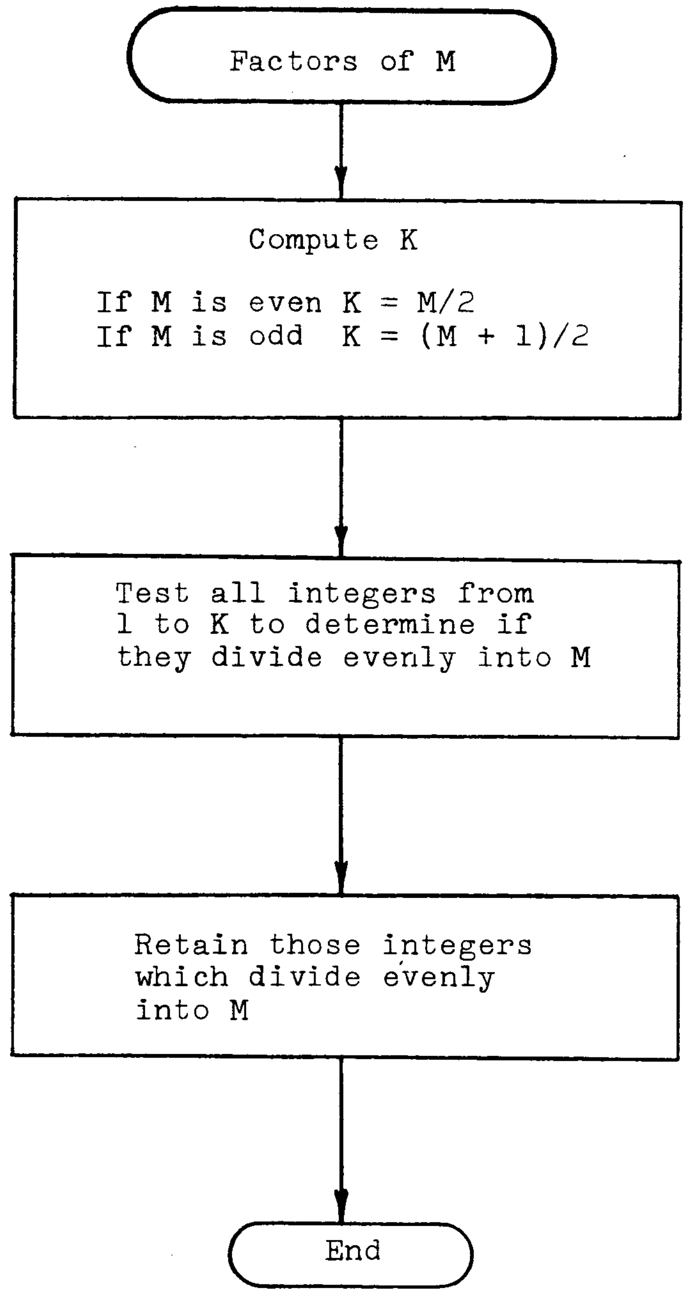


FIGURE 4. Procedure for Determining the Factors of M to be Used in Specifying Feasible Commutator Types

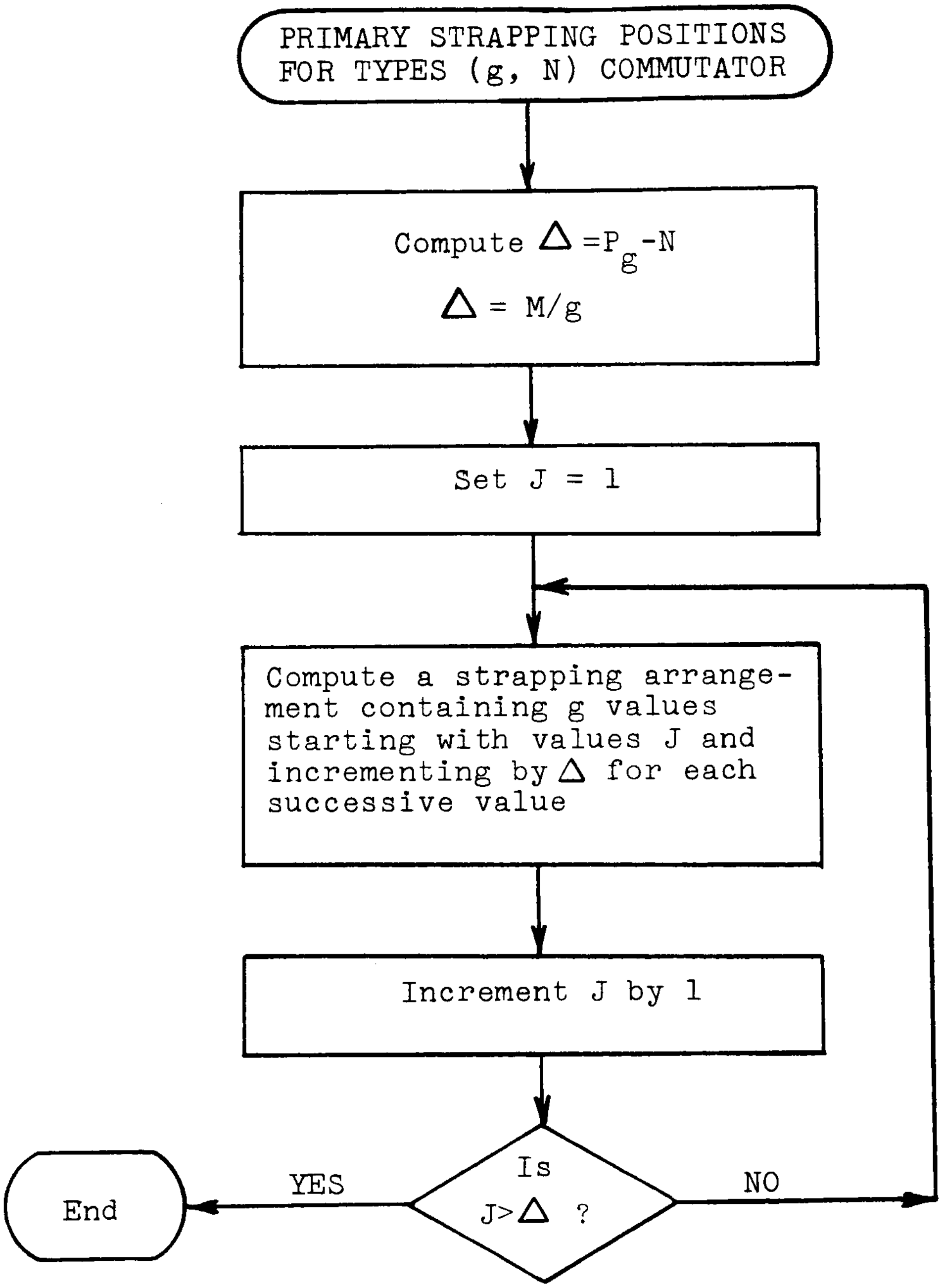


FIGURE 5. Procedure for Generating the Primary Strapping Arrangements for a Type (g, N) Commutator

the number of feasible strapping arrangements, but also indicates the number of gates which must be incremented to determine successive strapping points. It should also be noted that the procedure precludes joint occupancy and the necessity for checking this restriction in regard to the primary positions thus generated.

To illustrate the procedure for generating primary positions, assume that a Type (3, N) commutator is to be used in a multi-mode commutator system which has 6 master control unit gates. In this case then, M is equal to 6 and g is 3. Therefore:

$$P\ (g,\ N) = M/g = 6/3 = 2.$$

We now know that two primary positions must be defined. Referring to Figure 5, note that Δ is equal to P (g, N) which has just been found to equal 2. As specified, a starting point j is set equal to 1. Next, a strapping arrangement containing g = 3 values is generated starting with gate 1 and incrementing by Δ for each successive value; i.e., 1, 1 + 2, 1 + 2 + 2; to give gates 1, 3, and 5. If we let P_1 represent this first position, P_1 may be defined as a set or aggregate of the master control unit gates 1, 3, and 5. Symbolically, the set would be denoted as:

$$P_1 = \left\{1,\ 3,\ 5\right\}.$$

Each member of the set is termed an element: i.e., 1, 3, and 5. We continue the procedure incrementing j by 1 giving 2. Since j equals 2 is not greater than Δ , the procedure is repeated resulting in the second primary position; i.e., 2, 4, and 6. This position may be denoted as:

$$P_2 = \left\{2,\ 4,\ 6\right\}.$$

Continuing the procedure, j is again incremented by 1 giving 3 which is greater than Δ and the procedure is terminated. The primary strapping arrangements thus generated are identified as "Primary Strapping Positions for Type (3, N) Commutators" and each position is assigned a number according to the j used to initiate its generation. The positions and their strapping arrangements are then summarized as follows:

Position	Master Control Unit Gates Occupied		
1	1	3	5
2	2	4	6

The preceding procedure must be accomplished for each feasible commutator type which may be used within the system. When this has been done, all of the feasible primary positions for the system will have been determined. It is important to note that for a particular commutator type each of its primary positions is independent and mutually exclusive. From a programming viewpoint this means:

1. Each primary position for a particular commutator type may be used either individually or collectively without regard to the particular commutator type's other primary positions.

2. The gates required for strapping any one primary position of a particular commutator type are not utilized in strapping any of the same commutator's remaining primary positions.

These two facts will be particularly important in the generation of combinatorial programs for a given commutator system.

In considering the sections which follow, it will be helpful to keep in mind that the primary positions are defined as subsets of the universal set of master control unit gates available in a specific system. If we let $\mathcal{U}$ represent the universal set of master control unit gates, the set may be denoted as:

$$\mathcal{U} = \left\{1, 2, \ldots, M\right\}.$$

A particular primary position may then be denoted:

$$P_i = \left\{ x \in \mathcal{U} \,\middle|\, \begin{array}{l} x \text{ is a gate feasibly attached to} \\ \text{a single specific type commutator} \end{array} \right\} .$$

Letting p (x) represent the condition that x is a gate feasibly attached to a single specific type commutator, we may then write:

$$P_i = \left\{ x \in \mathcal{U} \mid p\,(x) \right\} ,$$

read P_i is the set of those elements x of $\mathcal{U}$ which satisfy the conditions p (x). Also recall that as used here "feasibly" infers that the symmetry, positional and capacity restrictions as they apply to the primary positions have been met.

GENERATION OF COMBINATORIAL POSITIONS. Operationally, a combinatorial position occurs when two or more commutators are strapped simultaneously to the gates of the master control unit. In actual practice, this can be accomplished only if both of the following requirements are met:

1. The number of gates required must not exceed those available.

2. Joint occupancy must not be required.

Mathematically, a combinatorial position may be defined, formed, and tested for feasibility by using set operations on the sets used in defining the primary positions. A possible combinatorial position may thus be defined as the union of two or more sets of gates, where each set represents a primary position. To illustrate, let P_1 and P_2 represent two sets defined as subsets of the universal set $\mathcal{U}$ of master control unit gates. Then, the union of P_1 and P_2, denoted by $P_1 \cup P_2$, is the set of elements of $\mathcal{U}$ which are members of either P_1 or P_2 or both. This may be stated symbolically as:

$$P_1 \cup P_2 = \left\{ x \in \mathcal{U} \,\middle|\, x \in P_1 \text{ or } x \in P_2 \right\}$$

and is read as "P_1 union P_2 is the set of those elements x of $\mathcal{U}$ for which x is an element of either P_1 or P_2 or both". Figure 6a illustrates the union graphically as a Venn diagram. The large rectangular area represents the universal set of master control unit gates. Each of the two primary positions P_1 and P_2 is represented as a circle. Both P_1 and P_2 represent subsets of the universal set of master control unit gates since each and every one of their elements is also an element of $\mathcal{U}$. This fact may be denoted symbolically as:

$$P_1 \subseteq \mathcal{U} \quad \text{and} \quad P_2 \subseteq \mathcal{U} .$$

The set $P_1 \cup P_2$ is represented by the shaded area. It is important to note two additional facts:

1. A union may consist of more than two sets and thus might be more correctly denoted as: $P_1 \cup P_2 \ldots \cup P_n$.

2. The word "or" used in defining the union of sets is used in its inclusive sense and not in its exclusive sense.

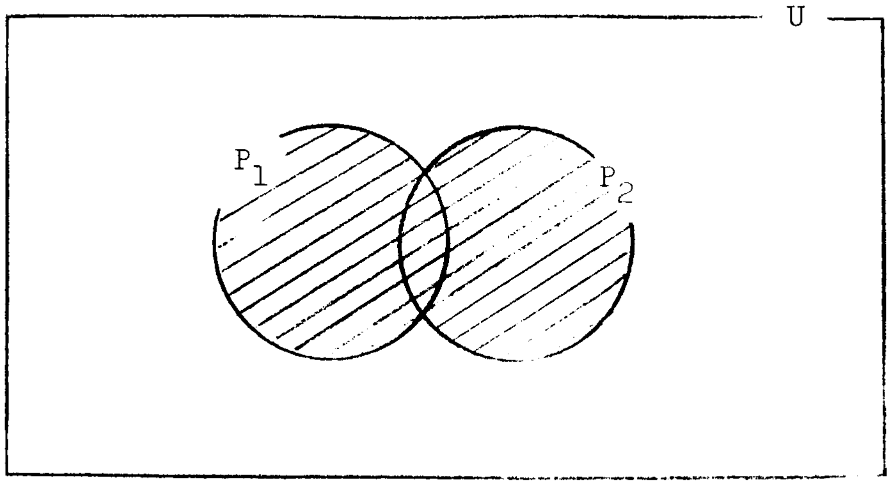
Another important connotation is that the set of elements which are common to two or more subsets of a universal set is termed the intersection of the subsets. Symbolically:

$$P_1 \cap P_2 = \left\{ x \in \mathcal{U} \,\middle|\, x \in P_1 \text{ and } x \in P_2 \right\}$$

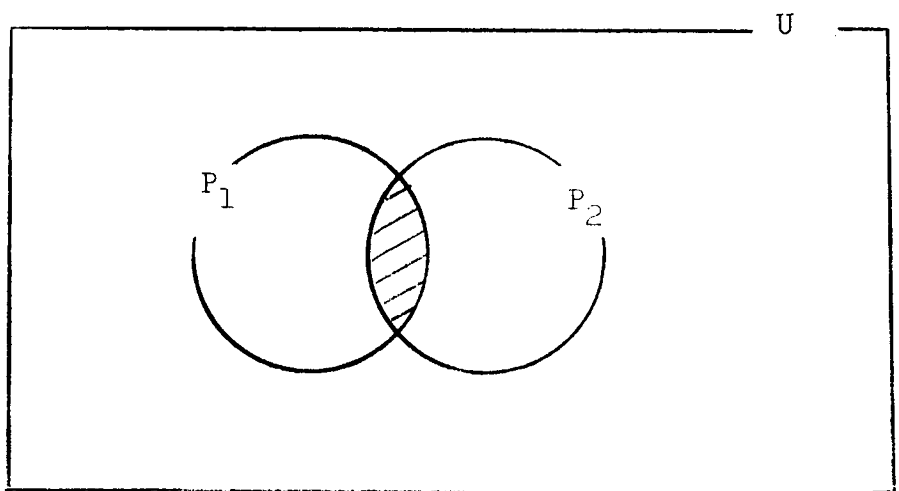
read "P_1 intersection P_2 is the set of those elements x of $\mathcal{U}$ such that x is both an element of P_1 and an element of P_2." The intersection of the two sets P_1 and P_2 is illustrated graphically by a Venn diagram in Figure 6b. Again, the universal set of master control unit gates is portrayed as a rectangular area and the two subsets P_1 and P_2 by circles. The intersection is represented by the shaded area. This intersection involves two possibilities which are extremely important in determining the feasibility of a possible combinatorial position. Sets P_1 and P_2 may either be joint or disjoint. They are said to be joint if the two sets have at least one element in common. If, on the other hand, two sets have no common elements, they are said to be disjoint or mutually exclusive. In the latter case, the set formed by the intersection is termed the empty or null set $\emptyset$; i.e., it has no elements. From a feasibility viewpoint then, joint occupancy does not occur if the intersection of two or more sets is the null set $\emptyset$. This indicates that the sets are disjoint and could be portrayed as non-overlapping circles in an appropriate Venn diagram To illustrate, let

$$P_1 = \{1, 3, 5, 7, 9, 12\} \quad \text{and} \quad P_2 = \{1, 7\} .$$

The union of the two sets, $P_1 \cup P_2 = \{1, 3, 5, 7, 9, 12\}$, defines a possible combinatorial set. However, the intersection of the two sets $P_1 \cap P_2 = \{1, 7\}$ and therefore,



A: A Venn Diagram Illustrating the Union of Two Sets $P_1 \cup P_2$.



B: A Venn Diagram Illustrating the Intersection of Two Sets $P_1 \cap P_2$.

FIGURE 6. Set Concepts Used in Defining Combinatorial Positions

not the null set. Hence, the combinatorial position is not feasible from the joint occupancy viewpoint. Now, consider the case where we let $P_1 = \{1, 3, 5, 7, 9, 12\}$ and $P_3 = \{2, 8\}$. Let $P_1 \cup P_3$ represent a possible combinatorial position. In this case, $P_1 \cap P_3$ is the null set $\emptyset$ and consequently, feasible from the joint occupancy viewpoint. If, in addition, the sum of the gates required for the combinatorial position is equal to or less than those available, the combinatorial position is feasible and may be defined as $P_1 \cup P_3$. This latter restriction may be stated symbolically as: $\Sigma g \leq M$. Summarizing:

1. A possible combinatorial position may be identified and defined as the union of two or more of the sets used to define primary positions; i.e., $P_1 \cup P_2 \ldots \cup P_n$.

2. The combinatorial position will be feasible if for the sets of which they are composed:

   a. $\Sigma g \leq M$

   b. $P_1 \cap P_2 \ldots \cap P_n = \emptyset$.

3. A feasible combinatorial position will also define a feasible commutator program if for the sets of which it is composed $\Sigma g = M$.

Now let us consider how combinatorial positions are counted, ordered, and formed into feasible commutator programs.

<u>Counting Combinatorial Positions</u>. Three counts must be considered in determining the number of possible combinatorial positions:

1. The number of ways in which a single commutator of a particular type may be strapped to the gates of the master control unit.

2. The number of ways in which more than one commutator of a particular type may be simultaneously strapped to the gates of the master control unit.

3. The number of ways in which two or more commutators of different types may be simultaneously strapped to the gates of the master control unit.

Starting with the first case, it has previously been shown that the number of different ways, P (g, N), in which a single Type (g, N) commutator may be strapped to a master control unit with M gates could be stated as:

$$P\ (g,\ N) = M/g.$$

A simple extension of this relationship will permit the determination of the number of ways in which more than one commutator of a particular type may be simultaneously strapped to the gates of the master control unit. This extended relationship may be stated as follows:

$$S\ (G,\ g) = \frac{P\ (g,\ N)!}{[P\ (g,\ N) - G]!\ G!}$$

where

S (G, g) = the number of combinatorial strapping arrangements available when G of a particular type of commutators are used.

P (g, N) = the number of ways in which a single Type (g, N) commutator may be strapped to M master control unit gates.

G = the specific number of Type (g, N) commutators to be used simultaneously. $G \leq P\ (g,\ N)$

g = the number of gates to which a commutator is strapped.

It should be noted that this expression may also be used to determine the number of different positions in which a single commutator may be used by substituting M/g for (P_g, N). To illustrate both of these aspects, consider how it would be used in a system which has six master control unit gates to determine the ways in which a Type (2, N) commutator might be used. First, let us determine the number of ways in which the commutator could be used singly:

$$S\ (1,\ 2) = \frac{(6/2)\ !}{[(6/2) - 1]\ !\ 1\ !}$$

$$= \frac{3\ !}{2\ !\ 1\ !} = 3 \text{ Positions.}$$

Considering the master control unit gate capacity, two different combinatorial possibilities exist when using only Type (2, N) commutators: G = 2 and G = 3.

$$S\ (G,\ g) = \frac{P\ (g,\ N)}{[P\ (g,\ N) - G]\ !\ G\ !}$$

For G = 2

$$S\ (2,2) = \frac{3\ !}{(3 - 2)\ !\ 2\ !} = \frac{3.2.1}{1.2.1} = 3 \text{ Positions}$$

For G = 3

$$S\ (3,2) = \frac{3\ !}{(3 - 3)\ !\ 3\ !} = \frac{3.2.1}{1.3.2.1} = 1 \text{ Position}$$

These results indicate that there are three ways in which two Type (2, N) commutators may be simultaneously strapped to the gates of the master control unit and only one way when three Type (2, N) commutators are used simultaneously. Assume that the three primary positions in which a Type (2,N) commutator may be used are denoted 1, 2, and 3. The specific ways in which two of the commutators can be used may be designated as compounds of these primary positions as: 1, 2; 1, 3: and 2, 3. Similarly, the specific way in which three of the commutators may be used simultaneously may also be denoted as a compound of the primary positions; i.e., 1, 2, 3. Recall that each of the primary positions is defined as an independent, mutually exclusive set of gates. This means that joint occupancy has been precluded and each of the possible combinatorial positions in this case are also feasible positions. In addition, when three Type (2, N) commutators are used, all of the master control unit gates are occupied; i.e., $\Sigma g = M$, and consequently, this combinatorial position defines a feasible commutator program.

Now consider the third case in which two or more different types of commutators are used simultaneously. Building on the previous example, consider the simultaneous use of Type (2, N) commutators and Type (3, N) commutators in a system with six master control unit gates. As noted above, the Type (2, N) commutator has 3 primary positions. For the Type (3, N) commutator, P (3, N) is equal to two positions. Also note that for the Type (3, N) commutator: S (1, 3) = 2, and S (2, 3) = 1. Again considering the master control unit gate capacity, only one mixed combinatorial position is feasible; i.e., 1 Type (2, N) and 1 Type (3, N) commutator. It is seen that in this case Σg is equal to five which is less than the six gates available. The total number of possible combinatorial positions when using the designated commutators is given by the product of S (1, 2) and S (1, 3):

$$[S\ (1,\ 2)]\ [S\ (1,\ 3)] = (3)\ (2) = 6 \text{ Positions.}$$

In general, if one particular type of commutator can be strapped to the master control unit in "a" ways and another in "b" ways, then there are "ab" possible ways to strap the combination. As before, each of the "ab" possibilities may or may not be feasible depending upon the combinatorial restriction and the master control unit capacity. Again assume that the primary positions in which a Type (2, N) may be used are denoted as 1, 2, and 3. Further assume that the primary positions in which the Type (3, N) commutator may be used are designated positions 1 and 2. Compounds of these designations may also be used to identify the six combinatorial positions as: 1, 1; 1, 2; 2, 1; 2, 2; 3, 1; and 3, 2. The first digit represents a primary position of the Type (2, N) commutator and the second digit represents a primary position of the Type (3, N) commutator. Each of the combinatorial positions must be evaluated to determine if they require joint occupancy. This is accomplished by first generating the primary positions for each commutator using the procedure presented in Figure 5. These positions may be summarized as follows:

Commutator Type	Primary Position	Set of Gates Required
(2, N)	1	1 4
	2	2 5
	3	3 6
(3, N)	1	1 3 5
	2	2 4 6

Next, each combinatorial position is defined as the union of the two sets of gates required by the two primary positions. The intersection of each of these two sets of gates is then checked to determine whether the sets are disjoint and thus feasible. This has been accomplished for this example. By further identifying the primary positions of the Type (2, N) commutator and the Type (3, N) commutator with the prefixes

A and B respectively to facilitate set notation, the findings may be summarized as follows:

Combinatorial Position	Defined by	Set of Gates Required	Common Gates	Conclusion
1, 1	A1 U B1	1 3 4 5	1	A1 ∩ B1 ≠ ∅
1, 2	A1 U B2	1 2 4 6	4	A1 ∩ B2 ≠ ∅
2, 1	A2 U B1	1 2 3 5	5	A2 ∩ B1 ≠ ∅
2, 2	A2 U B2	2 4 5 6	2	A2 ∩ B2 ≠ ∅
3, 1	A3 U B1	1 3 5 6	3	A3 ∩ B1 ≠ ∅
3, 2	A3 U B2	2 3 4 6	6	A3 ∩ B2 ≠ ∅

It is seen above that all of the possible combinatorial positions are not feasible. Consequently, it must be concluded that the two types of commutators may never be used simultaneously.

Ordering Combinatorial Positions. In the preceding combinatorial examples it was a fairly easy task to identify and order the possible combinatorial positions since very few possibilities were involved. However, in many multi-mode commutator systems the number of possible combinatorial positions is extremely large. Consequently, procedures are needed to systematically identify and order the possible combinatorial positions and programs when large commutator systems are involved. In describing suitable procedures for these purposes, a distinction will be made in regard to the use of the words order and ordering. As used here, the word order will be related to the number of either primary positions or commutators required to identify a particular combinatorial position. A combinatorial position will be referred to as a first order combinatorial position if it is composed of two and only two commutators (or primary positions depending on which of the two is used in defining the combinatorial position). Higher orders are designated as the number of primary positions utilized minus one. A fourth order combinatorial position thus infers that five primary positions have been combined in forming the position in question. The term ordering, on the other hand, will be used to indicate the listing of commutators, combinatorial positions, and combinatorial programs in sequence. Ordinarily, the sequence of listing will be a descending order according to g_i of Type (g_i, N). Two different procedures will be presented for ordering.

The first procedure, presented as Figure 7, is used to systematically generate and list all possible first order combinatorial positions. After the listing is completed, each of the positions generated may then be evaluated in terms of the combinatorial restriction. In this way, the commutators which may never be used simultaneously in combination are determined. This permits them to be eliminated as possible components in higher order combinatorial positions and thereby eliminates a great deal of unnecessary labor. Let us return to our six gate commutator system to illustrate the procedure. It was previously determined that four different types of commutators may feasibly be used singly within the system; i.e., Types (6, N), (3, N), (2, N), and (1, N). The commutators have been listed in descending order according to g_i of Type (g_i, N) to initiate the procedure. Next, the Type (6, N) commutator is selected since it has the largest g_i. A comparison is then made to determine if g_i (i.e., 6 in this trial) is less than M (in this case M is also equal to 6). Since it is not, the commutator is discarded and replaced with the Type (3, N); i.e., the commutator with the next lowest g_i. Again g_i is compared to M and in this case $3 < M$. Therefore, g_i is entered into a first order positional array; i.e., (3, _). Since the array does not contain two elements, a second Type (3, N) commutator is selected and entered into the array; i.e.,

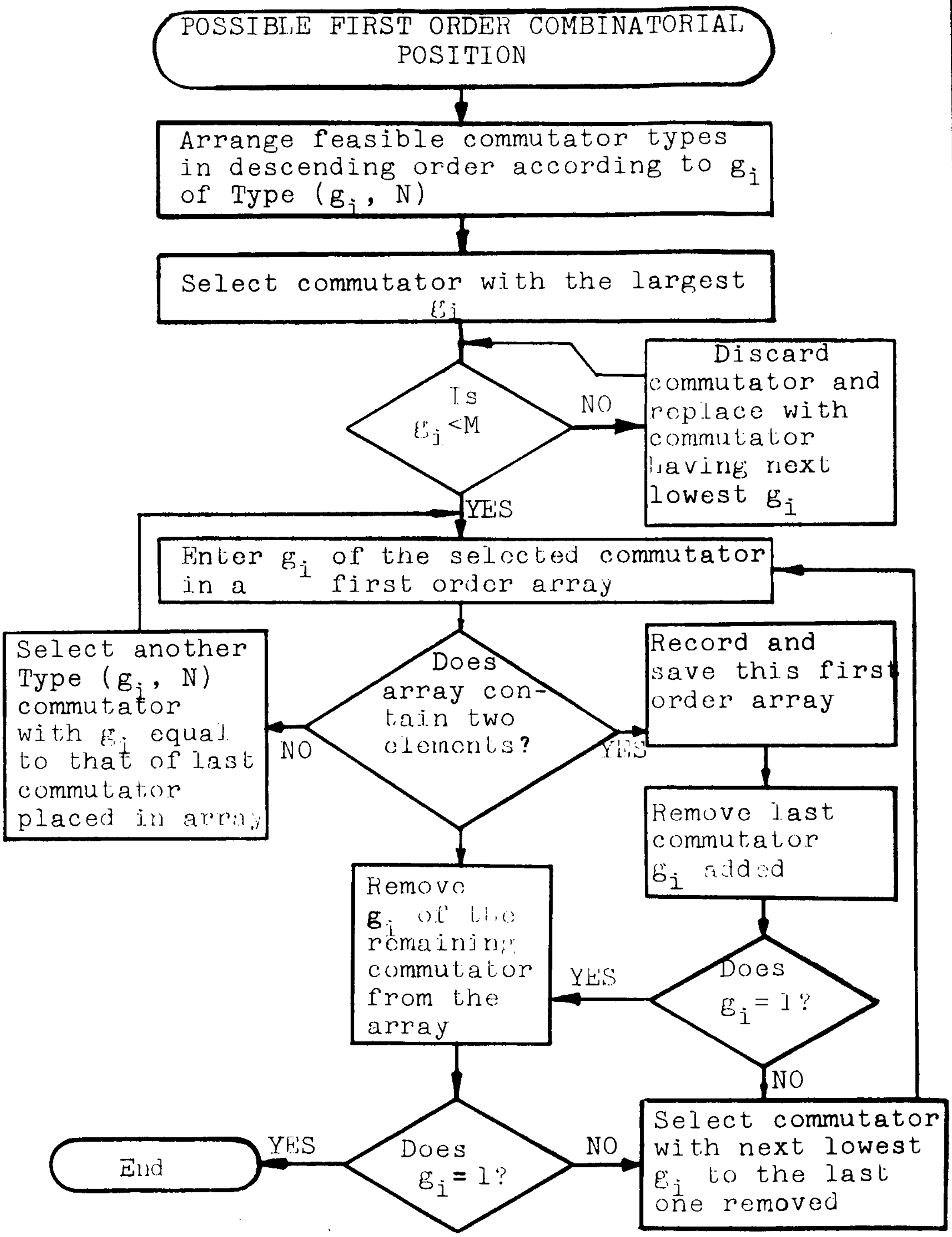


FIGURE 7: Procedure for Ordering First Order Combinatorial Positions

(3, 3). The array now contains two elements and is recorded and saved. The last g_i is removed from the saved array; i.e., (3, _). Since the removed g_i is not equal to one, the commutator with the next lowest g_i is selected; i.e., Type (2, N). Its g_i, 2, is now entered in the positional array giving (3, 2) which is recorded and saved since the array now contains two elements. In a similar way, the next array (3, 1) is generated, recorded, and saved. In this case, when the g_i of the last commutator added is removed from the array, it is found to be equal to one. Consequently, the remaining g_i (i.e., 3) is also removed from the array leaving (_, _). Since it is not equal to one, the commutator with the next lowest g_i is then selected; i.e., Type (2, N). Its g_i is used to initiate a new first order array; i.e., (2, _). The preceding procedure is then repeated generating positions: (2, 2); (2, 1); and (1, 1). After the last 1 of position (1, 1) has been removed, g_i will equal 1 and consequently the procedure will be terminated. The possible first order combinatorial positions when using a system with six master control unit gates may thus be summarized in terms of the g_i's of the type commutators used to form them as:

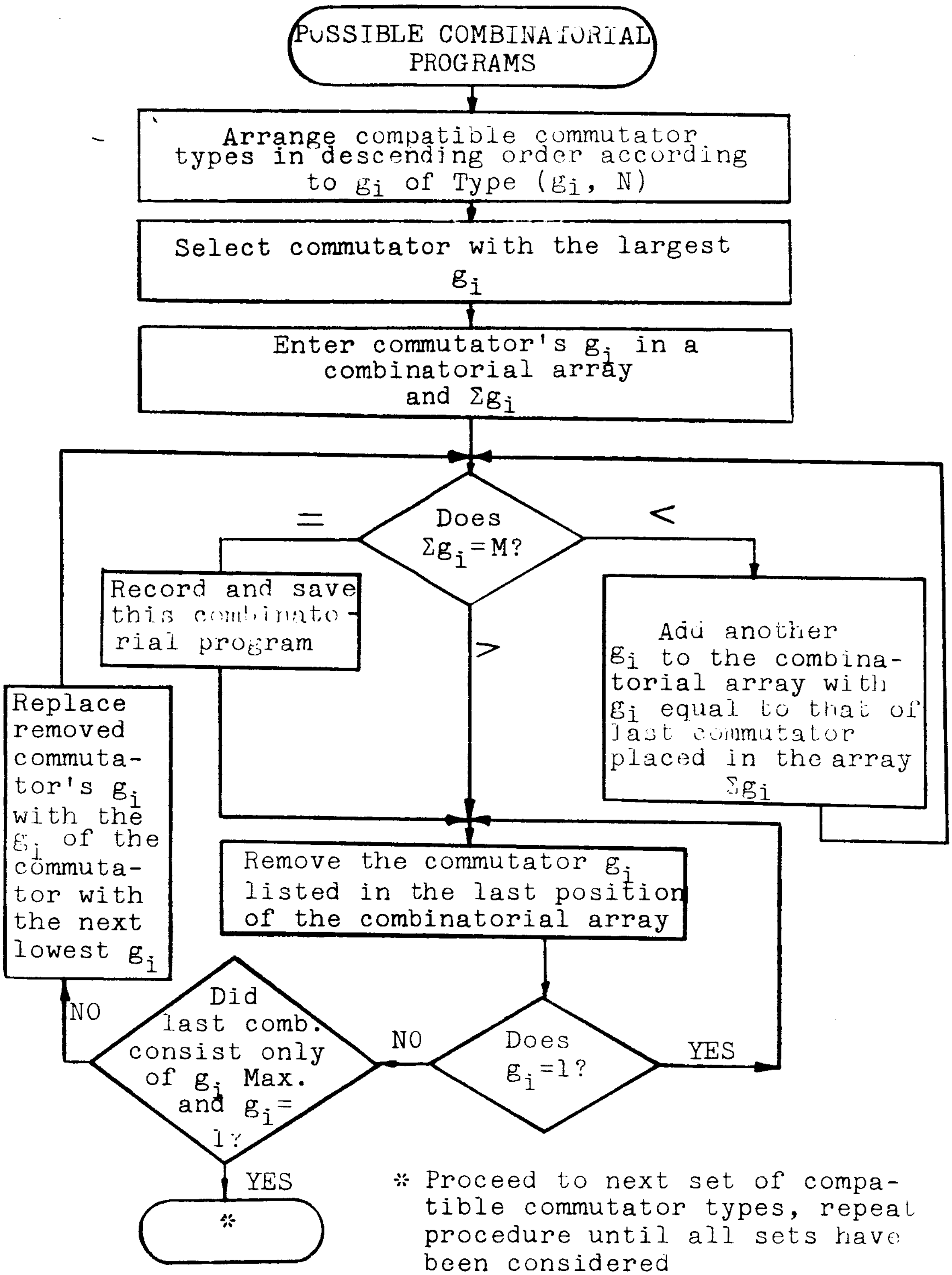
1. (3, 3)
2. (3, 2)
3. (3, 1)
4. (2, 2)
5. (2, 1)
6. (1, 1)

Each of these positions must be checked for feasibility. Positions 1, 4, and 6 are each composed of a single type of commutator and would immediately be concluded feasible for reasons previously explained. The second position is as indicated composed of a Type (3, N) commutator and a Type (2, N) commutator. In the example of the previous section, this particular combination was evaluated and it was found that the two types of commutators may never be used simultaneously. A Type (1, N) commutator may always be used in any unoccupied gate. Consequently, both positions 3 and 5 are concluded to be feasible since neither requires all the master control unit gates available. At this point, three sets of commutators may be defined for further consideration in forming higher order combinatorial positions:

1. Type (3, N), Type (1, N)
2. Type (2, N), Type (1, N)
3. Type (1, N)

Each itemized set includes a group of commutators which we shall refer to as compatible types. Compatibility in this case has been determined on the basis that the commutators may be used simultaneously in first order combinatorial positions. The groups have been based on g_i of the first commutator listed and includes all commutators of lesser g_i's with which it may possibly be used to form higher order combinatorial positions and ultimately combinatorial programs.

Figure 8 presents a procedure for converting a set of compatible commutators into an ordered list of possible combinatorial commutator programs. Each program is defined in terms of the g_i's of the commutators of which it is composed. To illustrate the procedure, consider the first set of compatible commutators generated in the previous example. The two commutator types included in the compatible commutator set are first listed in descending order according to g_i of Type (g_i, N) to initiate the procedure; i.e., Type (3, N), Type (1, N). Next, the Type (3, N) commutator is selected since it is the commutator with the largest g_i. Its g_i is then entered in a combinatorial array as: (3, _, ..., _). At this time, $\Sigma\, g_i$ for the array is 3 which is less than the gates available. Consequently, another Type (3, N) commutator is selected and its g_i entered into



* Proceed to next set of compatible commutator types, repeat procedure until all sets have been considered

FIGURE 8. Procedure for Ordering Possible Combinatorial Commutator Programs

the combinatorial array, i.e.; (3, 3, ..., _). Now Σ g_i for the array is 6 and consequently equal to M. The array which now represents a possible combinatorial program is recorded as (3, 3) and is also saved for further manipulation. The g_i listed in the last position of the combinatorial array (3) is removed leaving (3, _). This g_i is not equal to 1 and the last combination did not consist only of g_i max and g_i's equal to one so the procedure is continued. The removed g_i is replaced by inserting 1 (the g_i of the commutator with the next lowest g_i) in the vacated position of the combinatorial array; i.e., (3, 1). This results in Σ g_i equal to 4 which is less than M. Consequently, another 1 is added to the array to give (3, 1, 1). The sum of the g_i's is thus raised to 5 which is still less than M. Again a 1 is added to the combinatorial array to give: (3, 1, 1, 1). As a result Σ g_i is raised to 6 which is now equal to M. This array also now represents a possible combinatorial program and hence is recorded and saved. The last g_i is removed from the array and since it is equal to 1 the next g_i is also removed leaving: (3, 1, _, _). This g_i is also equal to 1 and so the next g_i is removed leaving (3, _, _, _). Since the last g_i removed was also equal to 1, the remaining g_i is removed, leaving an empty array (_, _, _, _). This g_i is 3 and so the last combinatorial position consisted of g_i max and g_i's equal to one only and so the procedure is terminated. At this time, the procedure would normally be repeated for each of the remaining compatible commutator sets. After this has been accomplished, each of the possible combinatorial programs generated must then be checked for feasibility in regard to the combinatorial restriction. It should be noted that the procedures used in generating the possible programs precludes violation of the symmetrial sampling and capacity requirements. Consequently, no further check is required in regard to the restrictions imposed by these requirements. A description of a systematic procedure for checking the feasibility of the programs from a combinatorial restriction viewpoint follows.

Formation of Feasible Commutator Programs. In the preceding section possible combinatorial positions have been generated and defined (or identified) by the g_i of the Type (g_i, N) commutators which they utilize. While this mode of definition conveniently serves to identify a particular combinatorial program it does not directly facilitate the determination of the program's adherence to the combinatorial restriction. For testing joint occupancy, a program must necessarily be defined in terms of the particular gates required. It is also apparent that this is the best mode of definition from a strapping viewpoint. The following procedures use a two-step transform in accomplishing this necessity. A positional array, such as that presented as Figure 9, is used to transform a particular possible commutator program's definition from the type commutators of which it is composed to the primary positions required for its strapping. These primary positions are then transformed to the master control gates they require. In this form, the program's definition may be examined for joint occupancy and if found feasible, to specify the required strapping arrangement. To illustrate the procedure, consider the positional array format presented in Figure 9. Note that this array is suitable only for transforming a first order combinatorial position. It should also be recalled, however, that higher order positions may be formed by compounding other primary positions with a first order combinatorial position. The preceding fact will become more apparent as the illustrated example is explained. To illustrate, let us consider how the possible combinatorial program (3, 1, 1, 1) of the 6 gate

		TYPE (g_j, N) PRIMARY POSITIONS (b_j)					
		b_1	b_2	...	b_j	...	b_n
TYPE (g_i, N) PRIMARY POSITIONS (a_i)	a_1	s_{11}	s_{12}	...	s_{1j}	...	s_{1n}
	a_2	s_{21}	s_{22}	...	s_{2j}	...	s_{2n}
	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
	a_i	s_{i1}	s_{i2}	...	s_{ij}	...	s_{in}
	a_m	s_{m1}	s_{m2}	...	s_{mj}	...	s_{mn}

Definitions:

b_j A particular primary strapping arrangement for a Type (g_j, N) commutator.

a_i A particular primary strapping arrangement for a Type (g_i, N) commutator.

s_{ij} A possible combinatorial strapping arrangement utilizing a Type (g_i, N) and a Type (g_j, N) commutator simultaneously. Note that $m = M/g_i$ and $n = M/g_j$. Also $\Sigma(g_i + g_j) \leq M$: where M is the number of master control unit gates.

FIGURE 9. A Positional Array Format for First Order Combinatorial Positions.

system developed in a previous example might be defined and evaluated for feasibility. Recall that it has been determined that a Type (3, N) commutator has two primary positions in this system. It can be determined in a similar manner that the Type (1, N) commutator has six primary positions. We begin the procedure to be illustrated by constructing a positional array to determine the first order combinatorial positions which may be formed when using the specified types of commutators. This has been accomplished and is presented as Table 1. The information required for, and the accomplishment of, the two-step transform is included as a part of Table 1. Each space in the array provides an alternate way for defining the first order combinatorial position (3, 1) i.e.; (3, N) U (1, N) in terms of the primary positions which may be utilized. This definition is then transformed to the gates required for strapping the primary positions involved. For example, consider the element s_{11} which is defined in terms of its primary positions as: 1, 1. In this notation, the first 1 represents primary position 1 of a Type (3, N) commutator and the second 1 represents primary position 1 of a Type (1, N) commutator. Referring to the table below the array, it can be seen that the former requires the set of gates $= \{1, 3, 5\}$ and the latter requires the set of gates $= \{1\}$. The set of gates thus required for the combinatorial position are the gates 1, 3, and 5 resulting from the union of the two subsets. It also becomes apparent that the joint occupancy of gate one is required; i.e., $I \cap J \neq \emptyset$. It is thus concluded that the use of this set of gates is not feasible from a combinatorial restriction viewpoint. This is then indicated in the array by entering the gate which is jointly occupied in the appropriate array space within parentheses. Each of the remaining spaces must be similarly evaluated. This has been accomplished and the results noted in the array. The results have also

TABLE 1. Positional Array for a Single Type (3, N) Commutator Used in Combination With a Single Type (1, N) Commutator With Tabular Definitions

		TYPE (1, N) PRIMARY POSITIONS					
		1	2	3	4	5	6
TYPE (3, N) PRIMARY POSITIONS	1	1,1 (1)	1,2	1,3 (3)	1,4	1,5 (5)	1,6
	2	2,1	2,2 (2)	2,3	2,4 (4)	2,5	2,6 (6)

Commutator Type	Position	Set of Gates Required			
(3, N)	1	1	3	5	
	2	2	4	6	
(1, N)	1	1			
	2	2			
	3	3			
	4	4			
	5	5			
	6	6			
(3, N)U(1, N)	1, 1	1	3	5	
	1, 2	1	2	3	5
	1, 3	1	3	5	
	1, 4	1	3	4	5
	1, 5	1	3	5	
	1, 6	1	3	5	6
	2, 1	1	2	4	6
	2, 2	2	4	6	
	2, 3	2	3	4	6
	2, 4	2	4	6	
	2, 5	2	4	5	6
	2, 6	2	4	6	

been summarized in terms of the set of gates required in the tables below the array. In addition, a graphical interpretation of the feasibility checks are presented as Venn diagrams in Figure 10. The set intersections are represented by the shaded area of the diagrams. Thus, it is seen that in terms of primary positions the combinatorial position in question may feasibly be defined alternately as: 1, 2; 1, 4; 1, 6; 2, 1; 2, 3; or 2, 5. These feasible first order combinatorial positions will now be used to define the possible second order combinatorial positions.

A positional array is again used to form the second order combinatorial positions which will be used to define the program (3, 1, 1, 1). The general format to be used is presented as Figure 11 and the specific array employed is presented as Table 2. Again, the information for definitive and evaluation purposes has been included in the latter. The resulting feasible second order combinatorial positions defined as (3, N) U (1, N) U (1, N) may be summarized as follows:

Combinatorial Positions	Set of Gates Required				
1, 2, 4	1	2	3	4	5
1, 2, 6	1	2	3	5	6
1, 4, 2	1	2	3	4	5
1, 4, 6	1	3	4	5	6
1, 6, 2	1	2	3	5	6
1, 6, 4	1	3	4	5	6
2, 1, 3	1	2	3	4	6
2, 1, 5	1	2	4	5	6
2, 3, 1	1	2	3	4	6
2, 3, 5	2	3	4	5	6
2, 5, 1	1	2	4	5	6
2, 5, 3	2	3	4	5	6

Every other possibility was rejected on the basis of joint occupancy of at least the gate indicated within parenthesis on the array.

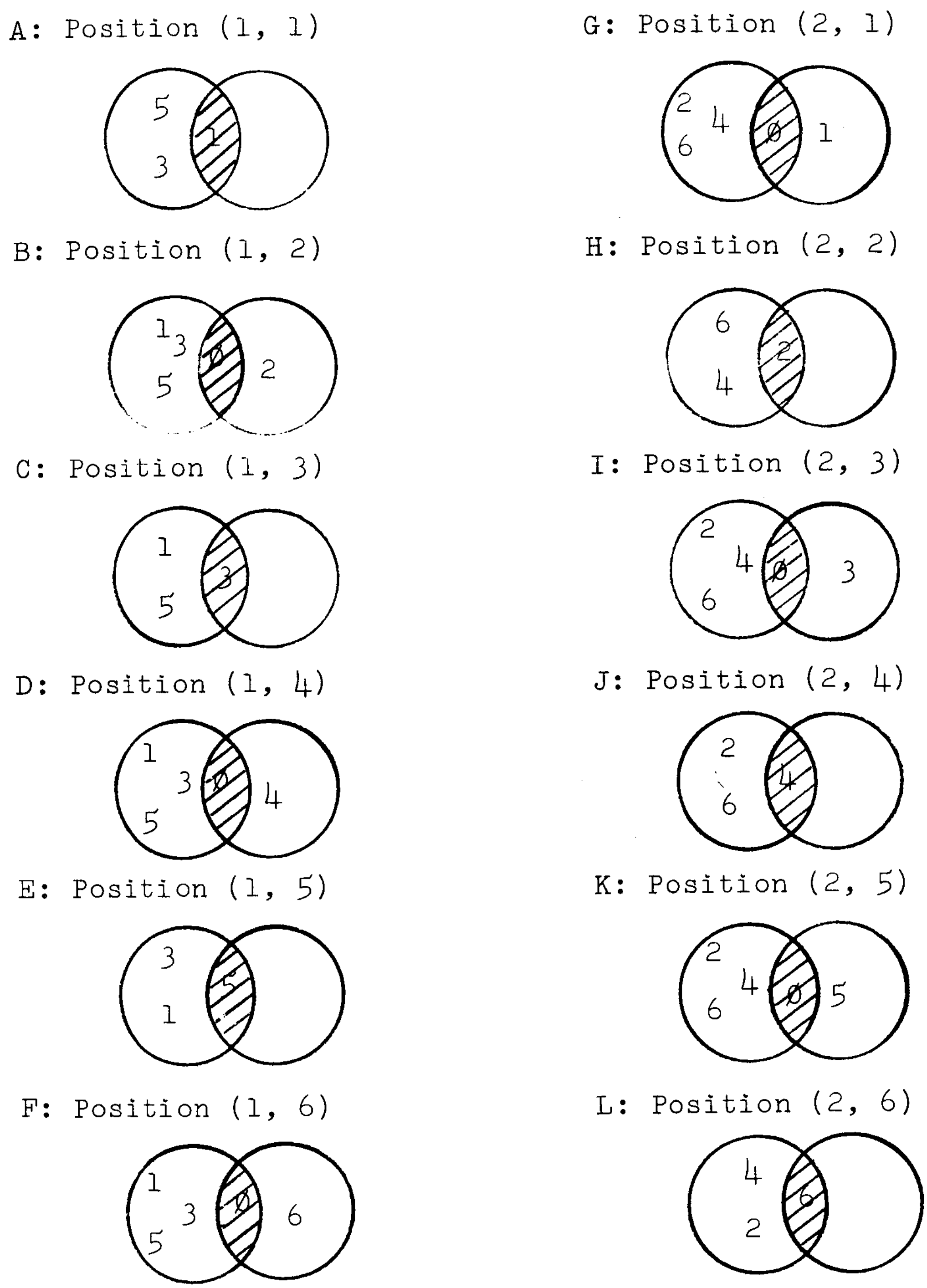


FIGURE 10. Venn Diagrams of the Sets Used to Define the Possible Combinatorial Positions When Using a Single Type(3, N) Commutator in Combination With a Single Type (1, N) Commutator

		TYPE (g_j, N) PRIMARY POSITIONS (b_j)					
		b_1	b_2	...	b_j	...	b_n
FEASIBLE COMBINATORIAL POSITIONS (a_i) $a_i = (g_i, N)U(g_j, N)\ldots$	a_1	t_{11}	t_{12}	...	t_{1j}	...	t_{1n}
	a_2	t_{21}	t_{22}	...	t_{2j}	...	t_{2n}
	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	a_i	t_{i1}	t_{i2}	...	t_{ij}	...	t_{in}
	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	a_m	t_{m1}	t_{m2}	...	t_{mj}	...	t_{mn}

Definitions:

a_i — A feasible combinatorial strapping arrangement utilizing two or more commutators simultaneously.

b_j — A particular primary strapping arrangement for a Type (g_j, N) commutator, $1 \leqslant b_j \leqslant M/g_j$.

t_{ij} — A possible combinatorial strapping arrangement utilizing three or more commutators simultaneously.

FIGURE 11. Positional Array Format for Higher Order Combinatorial Positions.

TABLE 2. Positional Array for a Combinatorial Position Defined as (3, N) U (1, N) U (1, N) With Tabular Definitions

		TYPE (1, N) PRIMARY POSITIONS					
		1	2	3	4	5	6
FEASIBLE COMBINATORIAL POSITIONS (3, N) U (1, N)	1,2	1,2,1 (1)	1,2,2 (2)	1,2,3 (3)	1,2,4	1,2,5 (5)	1,2,6
	1,4	1,4,1 (1)	1,4,2	1,4,3 (3)	1,4,4 (4)	1,4,5 (5)	1,4,6
	1,6	1,6,1 (1)	1,6,2	1,6,3 (3)	1,6,4	1,6,5 (5)	1,6,6 (6)
	2,1	2,1,1 (1)	2,1,2 (2)	2,1,3	2,1,4 (4)	2,1,5	2,1,6 (6)
	2,3	2,3,1	2,3,2 (2)	2,3,3 (3)	2,3,4 (4)	2,3,5	2,3,6 (6)
	2,5	2,5,1	2,5,2 (2)	2,5,3	2,5,4 (4)	2,5,5 (5)	2,5,6 (6)

Commutator Type	Position	Set of Gates Required			
(1, N)	1	1			
	2	2			
	3	3			
	4	4			
	5	5			
	6	6			
(3, N)U(1, N)	1, 2	1	2	3	5
	1, 4	1	3	4	5
	1, 6	1	3	5	6
	2, 1	1	2	4	6
	2, 3	2	3	4	6
	2, 5	2	4	5	6

Finally, a positional array for the third combinatorial position defined as (3, N) U (1, N) U (1, N) U (1, N); i.e., (3, 1, 1, 1), is constructed. To accomplish this, the preceding second order positions have been used in conjunction with the primary positions of the Type (1, N) commutator. The resulting array is presented as Table 3. A visual check of the sets of gates required by each of the array's elements was made to determine if joint occupancy was required. The affirmative cases have again been noted by entering a gate which would be jointly occupied in the appropriate elemental spaces and then enclosing it with parentheses. The third order combinatorial positions which were found to be feasible may be summarized as follows:

Combinatorial Positions	Set of Gates Required					
1, 2, 4, 6	1	2	3	4	5	6
1, 2, 6, 4	1	2	3	4	5	6
1, 4, 2, 6	1	2	3	4	5	6
1, 4, 6, 2	1	2	3	4	5	6
1, 6, 2, 4	1	2	3	4	5	6
1, 6, 4, 2	1	2	3	4	5	6
2, 1, 3, 5	1	2	3	4	5	6
2, 1, 5, 3	1	2	3	4	5	6
2, 3, 1, 5	1	2	3	4	5	6
2, 3, 5, 1	1	2	3	4	5	6
2, 5, 1, 3	1	2	3	4	5	6
2, 5, 3, 1	1	2	3	4	5	6

Note in the above summary that all master gates are now used, $\Sigma g = M$. Therefore, the third order combinatorial positions listed also represent a feasible commutator program. It is also interesting to note that although twelve positions are listed, only one set of gates is involved. Both of these observations are true from a set theory viewpoint since two sets are said to be equal if and only if every element of one

TABLE 3. Positional Array for a Combinatorial Position Defined as (3, N) U (1, N) U (1, N) U (1, N)

		TYPE (1, N) PRIMARY POSITIONS					
		1	2	3	4	5	6
FEASIBLE COMBINATORIAL POSITIONS (3, N) U (1, N) U (1, N)	1,2,4	1,2,4,1 (1)	1,2,4,2 (2)	1,2,4,3 (3)	1,2,4,4 (4)	1,2,4,5 (5)	1,2,4,6
	1,2,6	1,2,6,1 (1)	1,2,6,2 (2)	1,2,6,3 (3)	1,2,6,4	1,2,6,5 (5)	1,2,6,6 (6)
	1,4,2	1,4,2,1 (1)	1,4,2,2 (2)	1,4,2,3 (3)	1,4,2,4 (4)	1,4,2,5 (5)	1,4,2,6
	1,4,6	1,4,6,1 (1)	1,4,6,2	1,4,6,3 (3)	1,4,6,4 (4)	1,4,6,5 (5)	1,4,6,6 (6)
	1,6,2	1,6,2,1 (1)	1,6,2,2 (2)	1,6,2,3 (3)	1,6,2,4	1,6,2,5 (5)	1,6,2,6 (6)
	1,6,4	1,6,4,1 (1)	1,6,4,2	1,6,4,3 (3)	1,6,4,4 (4)	1,6,4,5 (5)	1,6,4,6 (6)
	2,1,3	2,1,3,1 (1)	2,1,3,2 (2)	2,1,3,3 (3)	2,1,3,4 (4)	2,1,3,5	2,1,3,6 (6)
	2,1,5	2,1,5,1 (1)	2,1,5,2 (2)	2,1,5,3	2,1,5,4 (4)	2,1,5,5 (5)	2,1,5,6 (6)
	2,3,1	2,3,1,1 (1)	2,3,1,2 (2)	2,3,1,3 (3)	2,3,1,4 (4)	2,3,1,5	2,3,1,6 (6)
	2,3,5	2,3,5,1	2,3,5,2 (2)	2,3,5,3 (3)	2,3,5,4 (4)	2,3,5,5 (5)	2,3,5,6 (6)
	2,5,1	2,5,1,1 (1)	2,5,1,2 (2)	2,5,1,3	2,5,1,4 (4)	2,5,1,5 (5)	2,5,1,6 (6)
	2,5,3	2,5,3,1	2,5,3,2 (2)	2,5,3,3 (3)	2,5,3,4 (4)	2,5,3,5 (5)	2,5,3,6 (6)

set is also an element of the other set and conversely. From an application point of view any one of the twelve may be used equally well.

EVALUATION OF GENERATED PROGRAMS. As previously noted, generated programs are evaluated in terms of two criteria - channel capacity and sampling rate. Each of these criteria was discussed at length in the first part of this chapter; consequently, here we will be concerned with the specific way in which a particular program may be evaluated. To illustrate, consider how the program generated in the previous section might be evaluated; i.e., (3, 1, 1, 1) defined as (3, N) U (1, N) U (1, N) U (1, N). Recall that the system used has six master control unit gates.

Channel capacity will normally be indicated for each specific commutator required by a particular program. To illustrate, assume that the commutators in the above referenced program each have twelve channels. The particular commutators used could be listed as follows:

Type (3, 12)
Type (1, 12)
Type (1, 12)
Type (1, 12)

Now note that by summing the second digit of the type identification across all commutators, it is determined that the program provides a total of 48 commutator channels. We may also arrive at this same determination through a subtraction process. Since the master control unit has six gates and each commutator has twelve channels, the system has a maximum capacity of 72 channels. It is also known that a commutator's channel capacity does not change even though it is attached to more than one gate. It should be noted, however, that such a practice does reduce the system's total maximum channel capacity, since the total number of commutators which may be used simultaneously is reduced. It has been previously shown that for the system in question a commutator may be alternately strapped to 1, 2, 3, or 6 gates. The reduction R_i in total maximum channel capacity which must be taken for each occurrence of a particular type commutator may be determined as: $R_i = N (g_i - 1)$. For the preceding commutator types the reductions would be computed as follows:

Type (1, 12), $R_1 = 12 (1 - 1) = 0$ Chan./Occ.
Type (2, 12), $R_2 = 12 (2 - 1) = 12$ Chan./Occ.
Type (3, 12), $R_3 = 12 (3 - 1) = 24$ Chan./Occ.
Type (6, 12), $R_6 = 12 (6 - 1) = 60$ Chan./Occ.

The system channel capacity Sc when using a particular program is now determined as:

Sc = Maximum Capacity - Restricted Capacity.

For program (3, 1, 1, 1):

$$Sc = NM - \Sigma f R_i$$
$$= (12)(6) - [(1)(24) + 3(0)]$$
$$= 48 \text{ Channels.}$$

From a system "user's" viewpoint, channel capacity expressed as data channels available at a given sampling rate is of primary importance. To pursue this point of view, let us first compute the sampling rates offered by our illustrative program. Two different sampling rates must be computed. Assuming that each gate of the master control unit is opened four times a second, the required computations are as follows:

$R_f = r\ g$ data channels/sec.

For $g_i = 1$

$R_f = (4)(1) = 4$ channels/sec.

For $g_i = 3$

$$R_f = (4)\ (3) = 12 \text{ channels/sec.}$$

Next, the number of data channels offered by each type of commutator utilized must be determined. To accomplish this, the total number of channels offered by each commutator must be reduced by the number of channels required for synchronization and identification. Assume that three channels are required for these purposes. Each type of commutator used will thus offer a capacity of nine data channels; i.e., (12 - 3). Consequently, program (3, 1, 1, 1) may now be summarized from the user's viewpoint as follows:

Commutator Type	Channel Capacity (data channels)	Sampling Rate (data chan./second)
Type (3, 12)	9	12
Type (1, 12)	9	4
Type (1, 12)	9	4
Type (1, 12)	9	4

A more concise format will be used in the chapter which follows for program identification purposes. By letting the illustrative program be identified as program 2, the format which will be used may be illustrated as:

Program Number	Data Channels	Samples a Second
2	9	12
	27	4

Note that channel capacity has been expressed as the total number of data channels available at a given sampling rate. The term "samples a second" has been used instead of "data channels a second" which was previously used. In this way, the common jargon of telemetry personnel is reflected without serious loss of technical correctness.

PRESENTATION OF PROGRAMS. In summarizing the programs generated, the views of two different groups of personnel must be considered - the system users and the system operators. From the user's point of view, the generated programs must be presented in such a way as to facilitate the specification of the program which most nearly matches his data sampling requirements. On the other hand, the system operator is primarily interested in the strapping arrangement required to set up the system once a particular program has been specified. Consequently, he is interested in a presentation oriented in this direction. To serve the needs of each of the parties, it is suggested that two different summaries be used.

Figure 12 presents the format of a summary which will facilitate program identification by data channel capacity and sampling rate. This summary should be of primary interest to the system user. Each generated program is assigned a unique number based on the order of generation. These numbers are entered serially in the column designated "Program Number". The adjacent column is used to indicate the total number of data channels available at a given sampling rate provided by a particular program. Where more than one sampling rate is provided by a program, each rate is listed in descending order in separate rows. To select a program, it is suggested that the user first establish the desired sampling rates and channel capacities at each rate which most nearly reflect his needs. It will be desirable for the user to familiarize himself with the various sampling rates and channel capacities provided by the system to be used before accomplishing the preceding step. After the desired program has been formulated, an attempt should then be made to match it with one of the programs listed in the summary. If a match is made, the program may then be specified by its number.

PROGRAM IDENTIFICATION BY DATA CHANNEL CAPACITY AND SAMPLING RATE IN DATA CHANNELS A SECOND

Program Number	Data Channels	Samples a Second
1	12	24
2	24	12
3	12 36	12 4
4	36	8
5	24 24	8 4
6	12 48	8 4
7	72	4

FIGURE 12. Sample Summary Format to Facilitate Program Identification

If none of the summarized programs match the requirements, a compromise must be made and the program which most nearly meets the desired requirements specified by number.

Figure 13 presents the format of a summary which will facilitate the strapping of a specified program. In contrast to the previous summary, this summary will be of primary interest to the system operators. As before, each feasible program which has been generated is assigned a number based on the order of generation. Consequently, the same number is used in both tables to identify a particular program. These numbers are entered in column (1) of the summary. The

PAM COMMUTATION SYSTEM PROGRAMS
6-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

(1) Program Number	(2) Requires Sampling Rate	(3) Commutator Type	(4) Master Control Unit Program
1	24	6-12	1, 2, ..., 6
2	12	3-12	1, 3, 5
	12	3-12	2, 4, 6
3	12	3-12	1, 3, 5
	4	1-12	2
	4	1-12	4
	4	1-12	6
4	8	2-12	1, 4
	8	2-12	2, 5
	8	2-12	3, 6
5	8	2-12	1, 4
	8	2-12	2, 5
	4	1-12	3
	4	1-12	6
6	8	2-12	1, 4
	4	1-12	2
	4	1-12	3
	4	1-12	5
	4	1-12	6
7	4	1-12	1
	4	1-12	2
	4	1-12	3
	4	1-12	4
	4	1-12	5
	4	1-12	6

FIGURE 13. Sample Summary Format to Facilitate Strapping of Specified Programs

combination of sampling rates offered by a particular program are listed in descending order in the rows of column (2). Each commutator utilized by a specific program is listed in column (3) adjacent to the sampling rate it provides. Column (4) is used to list the master control unit gates to which each specific commutator included in a particular program must be strapped.

III. MANUAL PROGRAMMING OF THE 30-CHANNEL MULTI-MODE PAM COMMUTATOR SYSTEM

Chapter I presented in detail the description of a 30-channel multi-mode PAM commutator system. At that time it was noted that if the described system was to be effectively utilized, a method of programming the system's commutators to its master control unit's gates would have to be made available. Chapter II described and illustrated an algorithm which was specifically designed for this purpose. This chapter will show how the algorithm may be manually applied to determine all the strapping arrangement programs that may be feasibly utilized when operating the 30-channel multi-mode PAM commutator system.

Three basic facts concerning the commutator system should be noted before initiating the programming procedures:

1. The master control unit is basically a 30 gate, two pole sequencer switch.
2. The master control unit opens its gates sequentially at a rate of four times a second.
3. Each high and/or low level commutator has 30 channels

From a programming viewpoint, these facts indicate that:

1. M, the required input to the programming system, is equal to thirty.
2. For program evaluation purposes, r is equal to four and N is equal to thirty.

Keeping these facts in mind, let us now consider how each of the algorithm's five basic steps must be accomplished.

DETERMINATION OF FEASIBLE COMMUTATOR TYPES

For programming purposes, it has been stated that commutators will be classified by the number of gates to which they are strapped and by their number of channels. It was also noted that a commutator may be attached to any number of the master control unit gates so long as that number is a factor of the total number of gates. In this particular case, the master control unit is known to have 30 gates. Consequently, the first step is to utilize the procedure flow chart in Figure 4 to determine the factors of 30.

Step one of the procedure is to compute a maximum divisor K. In this case, since M equals 30, an even number K is computed as M/2 or 15.

Step two is to test all integers from 1 to K to see if they divide evenly into M. Consequently, since K is equal to 15 each integer from 1 through 15 is successively divided into 30. Those integers which divide into 30 an even number of times are retained; all other divisors are discarded.

Based on this procedure, the factors retained are 1, 2, 3, 5, 6, 10, and 15. A factor equal to M (30 in this case) may always be used. Consequently, eight different types of commutators may be used satisfactorily within the system: Type (30, 30), Type (15, 30), Type (10, 30), Type (6, 30), Type (5, 30), Type (3, 30), Type (2, 30), and Type (1, 30).

GENERATION OF PRIMARY STRAPPING POSITIONS

A procedure for generating the primary strapping positions was presented in Figure 5 and must be applied for each type of commutator. This has been accomplished and the results are summarized as Tables 4 through 11.

TABLE 4. Primary Strapping Positions for Type (30, 30) Commutators

Position	Master Control Unit Gates Occupied
1	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26 27, 28, 29, 30

TABLE 5. Primary Strapping Positions for Type (15, 30) Commutators

Position	Master Control Unit Gates Occupied														
1	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29
2	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30

TABLE 6. Primary Strapping Positions for Type (10, 30) Commutators

Position	Master Control Unit Gates Occupied									
1	1	4	7	10	13	16	19	22	25	28
2	2	5	8	11	14	17	20	23	26	29
3	3	6	9	12	15	18	21	24	27	30

TABLE 7. Primary Strapping Positions for Type (6, 30) Commutators

Position	Master Control Unit Gates Occupied					
1	1	6	11	16	21	26
2	2	7	12	17	22	27
3	3	8	13	18	23	28
4	4	9	14	19	24	29
5	5	10	15	20	25	30

TABLE 8. Primary Strapping Positions for Type (5, 30) Commutators

Position	Master Control Unit Gates Occupied				
1	1	7	13	19	25
2	2	8	14	20	26
3	3	9	15	21	27
4	4	10	16	22	28
5	5	11	17	23	29
6	6	12	18	24	30

TABLE 9. Primary Strapping Positions for Type (3, 30) Commutators

Position	Master Control Unit Gates Occupied		
1	1	11	21
2	2	12	22
3	3	13	23
4	4	14	24
5	5	15	25
6	6	16	26
7	7	17	27
8	8	18	28
9	9	19	29
10	10	20	30

TABLE 10. Primary Strapping Positions for Type (2, 30) Commutators

Position	Master Control Unit Gates Occupied	
1	1	16
2	2	17
3	3	18
4	4	19
5	5	20
6	6	21
7	7	22
8	8	23
9	9	24
10	10	25
11	11	26
12	12	27
13	13	28
14	14	29
15	15	30

TABLE 11. Primary Strapping Positions for Type (1, 30) Commutators

Position	Master Control Unit Gates Occupied	Position	Master Control Unit Gates Occupied
1	1	16	16
2	2	17	17
3	3	18	18
4	4	19	19
5	5	20	20
6	6	21	21
7	7	22	22
8	8	23	23
9	9	24	24
10	10	25	25
11	11	26	26
12	12	27	27
13	13	28	28
14	14	29	29
15	15	30	30

GENERATION OF COMBINATORIAL POSITIONS

With the exception of the Type (30, 30) commutator, all of the other commutators may be used in combination with one or more other types. As previously noted, the actual types which may be used in combination are dependent upon the combinatorial restriction and the master control unit gate capacity. Recall from Chpater II that:

1. A possible combinatorial position may be identified and defined as the union of two or more of the sets of gates used to define the primary positions; i.e., $P_1 \cup P_2 \ldots \cup P_n$.

2. The combinatorial position will be feasible if:

   a. $\Sigma g \leq M$

   b. $P_1 \cap P_2 \ldots \cap P_n = \emptyset$

3. A feasible combinatorial position will also define a feasible commutator program if for the sets of which it is composed $\Sigma g_i = M$.

It has also been noted that for a particular commutator type each of its primary positions is independent and mutually exclusive. Keeping these facts in mind, a close examination of Tables 4 through 11 leads to the conclusion that there are eight feasible programs, each of which utilizes a single type of commutator, which may be defined without further analysis. The first is a primary program and the remainder combinatorial programs. The composition of the eight programs may be summarized as follows:

A. a single Type (30, 30) commutator
B. two Type (15, 30) commutators
C. three Type (10, 30) commutators
D. five Type (6, 30) commutators
E. six Type (5, 30) commutators
F. ten Type (3, 30) commutators
G. fifteen Type (2, 30) commutators
H. thirty Type (1, 30) commutators

Other feasible combinatorial programs are not as apparent, but may be determined by the positional array method. When manually applying the positional array method, it will normally be desirable to first try a single commutator of each specific type in combination with a single commutator of every other specific type. As previously noted, in this way those commutator types which may never be used in combination are quickly discovered thereby eliminating much unnecessary labor. The number of comparisons which must be made may be predetermined. Such a determination is ordinarily not required and this step may be omitted if desired. The procedure will be illustrated here to give support to the practice of first testing the first order combinatorial positions before generating the higher order combinatorial programs.

COUNTING COMBINATORIAL POSITIONS. In counting the number of first order comparisons to be made, the number of primary strapping positions by type of commutator are first summarized as follows:

Commutator Type	Number of Primary Strapping Positions
Type (15, 30)	2
Type (10, 30)	3
Type (6, 30)	5
Type (5, 30)	6
Type (3, 30)	10
Type (2, 30)	15
Type (1, 30)	30

Next, the determination of the number of comparisons which must be made when considering the combinatorial use of a single specific type of commutator with a single commutator of all other specific types, will be illustrated. Consider the Type (15, 30) commutator as used in a first order combinatorial position. It has been previously stated that if one particular type of commutator may be strapped to the master control unit in "a" ways and another type in "b" ways, then there are "ab" possible ways to strap the combination. Therefore, since a Type (15, 30) commutator may be strapped in 2 ways there are:

Possible Strapping Arrangements	When it is used singly in combination with
6 = (2)(3)	A Type (10, 30) commutator
10 = (2)(5)	A Type (6, 30) "
12 = (2)(6)	A Type (5, 30) "
20 = (2)(10)	A Type (3, 30) "
30 = (2)(15)	A Type (2, 30) "
60 = (2)(30)	A Type (1, 30) "

The number of comparisons for each of the other commutator types may be determined in a similar manner. In light of the number involved, the complexity of the manual programming problem should be readily apparent.

FIRST ORDER COMBINATORIAL POSITIONS. The procedure presented in Figure 7 has been utilized to systematically identify and order the possible first order combinatorial positions appropriate to the 30-channel commutator system. The results have been summarized and are presented as Table 12. Positions 1, 8, 14, 19, 23, 26 and 28 each require only a single type of commutator. Each of the commutator types utilized for these positions can be used in two or more mutually exclusive, independent primary positions. In addition, the procedure used to generate them precluded exceeding the gates available. Consequently, each of these primary positions may be concluded to be feasible without further verification. Similarly, positions 7, 13, 14, 22, 25, and 27 may also be concluded to be feasible without further verification, but for a different reason. A Type (1, 30) commutator may always be used in any unoccupied gate. In each of the preceding positions, each Type of commutator with which a Type (1, 30) commutator was paired, left more than one gate unoccupied; thus justifying the foregoing conclusion. Each of the other positions has been checked for feasibility using the positional array method for testing the combinatorial restriction. To illustrate the procedures employed for this purpose consider first the positional array for a Type (15, 30) commutator used in combination with a Type (10, 30) presented as Table 13. The six different combinatorial positions have been generated by cross classification of the appropriate primary positions and identified as 1, 1; 1, 2; ...; 2, 3.

TABLE 12. Possible First Order Combinatorial Positions for the 30 Channel Commutator System Identified by g_i of Type (g_i, N) of the Commutators Which Compose Them

Position Number	Composition	Position Number	Composition
1	(15, 15)	15	(6, 5)
2	(15, 10)	16	(6, 3)
3	(15, 6)	17	(6, 2)
4	(15, 5)	18	(6, 1)
5	(15, 3)	19	(5, 5)
6	(15, 2)	20	(5, 3)
7	(15, 1)	21	(5, 2)
8	(10, 10)	22	(5, 1)
9	(10, 6)	23	(3, 3)
10	(10, 5)	24	(3, 2)
11	(10, 3)	25	(3, 1)
12	(10, 2)	26	(2, 2)
13	(10, 1)	27	(2, 1)
14	(6, 6)	28	(1, 1)

TABLE 13. Positional Array for Testing Joint Occupancy of a Single Type (15, 30) Commutator Used in Combination with a Single Type (10, 30) Commutator

		TYPE (10, 30) PRIMARY POSITIONS		
		1	2	3
TYPE (15, 30) PRIMARY POSITIONS	1	1,1 (1)	1,2 (5)	1,3 (3)
	2	2,1 (4)	2,2 (2)	2,3 (6)

Each of the combinatorial positions was examined, one at a time, for joint occupancy by referring to Tables 5 and 6. The test employed was to determine if the intersection of the two sets of gates, whose union defines the combinatorial position in question, was the null set $\emptyset$. If so, the position was concluded to be feasible. Otherwise, the two sets were concluded to be joint and the position consequently not feasible. The findings of this examination were as follows:

Combination	Summary of Findings
1, 1	Joint occupancy of at least gate 1
1, 2	Joint occupancy of at least gate 5
1, 3	Joint occupancy of at least gate 3
2, 1	Joint occupancy of at least gate 4
2, 2	Joint occupancy of at least gate 2
2, 3	Joint occupancy of at least gate 6

These findings were entered on the positional array as numbers within parentheses indicating that the particular combinations being considered called for joint occupancy of at least the gate number indicated. Since joint occupancy is not permitted and examination of each of all the possible combinations indicates the joint occupancy of at least the encircled common gate, it must obviously be concluded that the two commutator types may never be used simultaneously.

Similar findings are presented in the positional array in Table 14 indicating that a Type (6, 30) commutator also may never be used in combination with a Type (15, 30) commutator.

Next, the possibility of using a Type (5, 30) commutator in combination with a Type (15, 30) commutator is considered in the positional array of Table 15. In this case, it was concluded that there were six ways in which the two commutators may be used singly in combination.

TABLE 14. Positional Array for Testing Joint Occupancy of a Single Type (15, 30) Commutator Used in Combination with a Single Type (6, 30) Commutator

		TYPE (6, 30) PRIMARY POSITIONS				
		1	2	3	4	5
TYPE (15, 30) PRIMARY POSITIONS	1	1,1 (1)	1,2 (7)	1,3 (3)	1,4 (9)	1,5 (5)
	2	2,1 (6)	2,2 (2)	2,3 (8)	2,4 (4)	2,5 (10)

TABLE 15. Positional Array for Testing Joint Occupancy of a Single Type (15, 30) Commutator Used in Combination with a Single Type (5, 30) Commutator

		TYPE (5, 30) PRIMARY POSITIONS					
		1	2	3	4	5	6
TYPE (15, 30) PRIMARY POSITIONS	1	1,1 (1)	1,2	1,3 (3)	1,4	1,5 (5)	1,6
	2	2,1	2,2 (2)	2,3	2,4 (4)	2,5	2,6 (6)

Table 16 indicates that there are ten ways in which a Type (15, 30) commutator and a Type (3, 30) commutator may be used in combination.

TABLE 16. Positional Array for Testing Joint Occupancy of a Single Type (15, 30) Commutator Used in Combination with a Single Type (3, 30) Commutator

		TYPE (3, 30) PRIMARY POSITIONS									
		1	2	3	4	5	6	7	8	9	10
TYPE (15, 30) PRIMARY POSITIONS	1	1,1 (1)	1,2	1,3 (3)	1,4	1,5 (5)	1,6	1,7 (7)	1,8	1,9 (9)	1,10
	2	2,1	2,2 (2)	2,3	2,4 (4)	2,5	2,6 (6)	2,7	2,8 (8)	2,9	2,10 (10)

Table 17 indicates, on the other hand, that a Type (2, 30) commutator may never be used in combination with a Type (15, 30) commutator.

Finally, as previously noted, a Type (1, 30) commutator may always be used in any unoccupied gate. Since each of the two positions available when using a Type (15, 30) commutator leaves fifteen unoccupied gates, it is concluded that there are 30 ways in which a Type (15, 30) commutator may be used in combination with a Type (1, 30) commutator.

By a similar process each of the other types of commutators have been paired with those commutator types requiring less master gate capacity. The arrays used are presented as Tables A-1 through A-10 of Appendix A and the results summarized in Table 18.

TABLE 17. Positional Array for Testing Joint Occupancy of a Single Type (15, 30) Commutator Used in Combination with a Single Type (2, 30) Commutator

		TYPE (2, 30) PRIMARY POSITIONS														
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TYPE (15, 30) PRIMARY POSITIONS	1	1,1 (1)	1,2 (17)	1,3 (3)	1,4 (19)	1,5 (5)	1,6 (21)	1,7 (7)	1,8 (23)	1,9 (9)	1,10 (25)	1,11 (11)	1,12 (27)	1,13 (13)	1,14 (29)	1,15 (15)
	2	2,1 (16)	2,2 (2)	2,3 (18)	2,4 (4)	2,5 (20)	2,6 (6)	2,7 (22)	2,8 (8)	2,9 (24)	2,10 (10)	2,11 (26)	2,12 (12)	2,13 (28)	2,14 (14)	2,15 (30)

TABLE 18. Summary of the Ways in Which Two Different Types of Commutators May Be Used Singly in Combination in the 30-Gate PAM Commutator System

TYPE (g_i, N) COMMUTATORS	TYPE (g_i, N) COMMUTATORS: 30-30	15-30	10-30	6-30	5-30	3-30	2-30	1-30
30-30	0	0	0	0	0	0	0	0
15-30	0	2	0	0	6	10	0	30
10-30	0	0	6	0	12	0	30	60
6-30	0	0	0	20	0	40	60	120
5-30	0	6	12	0	30	30	60	150
3-30	0	10	0	40	30	90	120	[illegible]
2-30	0	0	30	60	60	120	210	[illegible]
1-30	0	30	60	120	150	270	420	[illegible]

ORDERING POSSIBLE COMBINATORIAL PROGRAMS. At this point, the sets of commutators which may be used together to form feasible first order combinatorial positions have been determined. The procedure presented in Figure 8 is next employed to systematically identify and order the possible combinatorial programs. This has been accomplished with the result that there are in excess of 600 possible programs which must be evaluated for feasibility. Rather than listing each of these here, let us consider for illustrative purposes a single set of the compatible commutators. Table 19 summarizes the programs possible when considering only the set of compatible commutators which may be used singly with a Type (15, 30) commutator. Note that there are five other sets of compatible commutators which had to be treated similarly.

TABLE 19. An Ordered Set of Possible Combinatorial Programs Utilizing the Type (15, 30) Commutator

Combinatorial Program Number	Commutator Types (g_i, 30) Used to Form the Combinatorial Program
1	15, 15
2	15, 5, 5, 5
3	15, 5, 5, 3, 1, 1
4	15, 5, 5, 1, 1, 1, 1, 1
5	15, 5, 3, 3, 3, 1
6	15, 5, 3, 3, 1, 1, 1, 1
7	15, 5, 3, 1, 1, 1, 1, 1, 1, 1
8	15, 5, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1
9	15, 3, 3, 3, 3, 3
10	15, 3, 3, 3, 3, 1, 1, 1
11	15, 3, 3, 3, 1, 1, 1, 1, 1, 1
12	15, 3, 3, 1, 1, 1, 1, 1, 1, 1, 1, 1
13	15, 3, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1
14	15 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1

TESTING THE POSSIBLE COMBINATORIAL PROGRAMS. To proceed with the evaluation, each of the sets of possible combinatorial positions enumerated were next considered in respect to the positional and combinatorial restrictions. The ordered set of possible combinatorial programs utilizing the Type (15, 30) commutator which was summarized in Table 19 will be used to illustrate the procedure used.

Consider first Combinatorial Program Number 1. Since this program contains two similar types of commutators and further, since the primary positions in which these commutators can be used are mutually exclusive from a positional viewpoint, no further verification is required. We can immediately conclude that the program is feasible. Also, since only two primary positions are available for this particular type of commutator and both must be utilized, no further definition of the required strapping arrangement is necessary. Consequently, we can immediately progress to Combinatorial Program Number 2.

Combinatorial Program Number 2 calls for a Type (15, 30) commutator used in combination with three Type (5, 30) commutators. To determine the feasibility of this program two steps will be required. The first step is to construct a positional array as indicated in Table 20 using the output of Table 15 cross classified with the Primary Positions of a single Type (5, 30) commutator. After positional and combinatorial restrictions have been imposed, it is found that there are twelve ways that a Type (15, 30) commutator may be used in combination with two Type (5, 30) commutators which do not call for joint occupancy of at least one master control unit gate. Proceeding with the second step another positional array is constructed as shown in Table 21. In this array the output of the array in Table 20 has been cross classified with the Primary Positions for a Type (5, 30) commutator. Again both the positional and combinatorial restrictions are imposed and

TABLE 20. Positional Array for Testing Joint Occupancy of a Single Type (15, 30) Commutator Used in Combination with Two Type (5, 30) Commutators

COMBINATORIAL POSITIONS TYPE (15, 30), TYPE (5, 30)		TYPE (5, 30) PRIMARY POSITIONS 1	2	3	4	5	6
	1,2	1,2,1 (1)	1,2,2 (2)	1,2,3 (3)	1,2,4	1,2,5 (5)	1,2,6
	1,4	1,4,1 (1)	1,4,2	1,4,3 (3)	1,4,4 (4)	1,4,5 (5)	1,4,6
	1,6	1,6,1 (1)	1,6,2 (3)	1,6,3	1,6,4	1,6,5 (5)	1,6,6 (6)
	2,1	2,1,1 (1)	2,1,2 (2)	2,1,3	2,1,4 (4)	2,1,5	2,1,6 (6)
	2,3	2,3,1	2,3,2 (2)	2,3,3 (3)	2,3,4 (4)	2,3,5	2,3,6 (6)
	2,5	2,5,1	2,5,2 (2)	2,5,3	2,5,4 (4)	2,5,5 (5)	2,5,6 (6)

TABLE 21. **Positional Array for Testing the Compatibility of a Single Type (15, 30) Commutator Used in Combination with Three Type (5, 30) Commutators**

COMBINATORIAL POSITIONS TYPE (15, 30), TYPE (5, 30), TYPE (5, 30)		TYPE (5, 30) PRIMARY POSITIONS					
		1	2	3	4	5	6
	1,2,4	1,2,4,1 (1)	1,2,4,2 (2)	1,2,4,3 (3)	1,2,4,4 (4)	1,2,4,5 (5)	1,2,4,6
	1,2,6	1,2,6,1 (1)	1,2,6,2 (2)	1,2,6,3 (3)	1,2,6,4	1,2,6,5 (5)	1,2,6,6 (6)
	1,4,2	1,4,2,1 (1)	1,4,2,2 (2)	1,4,2,3 (3)	1,4,2,4 (4)	1,4,2,5 (5)	1,4,2,6
	1,4,6	1,4,6,1 (1)	1,4,6,2	1,4,6,3 (3)	1,4,6,4 (4)	1,4,6,5 (5)	1,4,6,6 (6)
	1,6,2	1,6,2,1 (1)	1,6,2,2 (2)	1,6,2,3 (3)	1,6,2,4	1,6,2,5 (5)	1,6,2,6 (6)
	1,6,4	1,6,4,1 (1)	1,6,4,2	1,6,4,3 (3)	1,6,4,4 (4)	1,6,4,5 (5)	1,6,4,6 (6)
	2,1,3	2,1,3,1 (1)	2,1,3,2 (2)	2,1,3,3 (3)	2,1,3,4 (4)	2,1,3,5	2,1,3,6 (6)
	2,1,5	2,1,5,1 (1)	2,1,5,2 (2)	2,1,5,3	2,1,5,4 (4)	2,1,5,5 (5)	2,1,5,6 (6)
	2,3,1	2,3,1,1 (1)	2,3,1,2 (2)	2,3,1,3 (3)	2,3,1,4 (4)	2,3,1,5	2,3,1,6 (6)
	2,3,5	2,3,5,1	2,3,5,2 (2)	2,3,5,3 (3)	2,3,5,4 (4)	2,3,5,5 (5)	2,3,5,6 (6)
	2,5,1	2,5,1,1 (1)	2,5,1,2 (2)	2,5,1,3	2,5,1,4 (4)	2,5,1,5 (5)	2,5,1,6 (6)
	2,5,3	2,5,3,1	2,5,3,2 (2)	2,5,3,3 (3)	2,5,3,4 (4)	2,5,3,5 (5)	2,5,3,6 (6)

we find there are twelve feasible strapping arrangements for the combinatorial program any one of which will serve our purposes. Since in the array the feasible arrangements are stated as combinations of primary positions, at this time they must be restated in terms of the actual strapping arrangements. To illustrate this procedure consider the combinatorial position 1, 2, 4, 6 as shown in row one of Table 21. We begin by listing the commutator types represented by this combination. Then by referring to Tables 5 and 8 the transformation to particular strapping arrangements may be accomplished as follows:

Commutator Type	Primary Position	Master Control Unit Gates Occupied
15-30	1	1, 3, 5, ..., 29 (odd integers only)
5-30	2	2, 8, 14, 20, 26
5-30	4	4, 10, 16, 22, 28
5-30	6	6, 12, 18, 24, 30

To further illustrate, we proceed to the evaluation of Combinatorial Program Number 3. In this case, the output of Table 15 is cross classified with the Primary Positions of a Type (3, 30) commutator to construct the positional array presented as Table 22. After the positional and combinatorial restrictions have been imposed, it becomes obvious that a Type (3, 30) commutator can never be used in combination with a single Type (15, 30) and a single Type (5, 30) commutator simultaneously. Consequently, no further analysis is needed for this combinatorial program and we may proceed immediately to the evaluation of Combinatorial Program Number 4.

In evaluating Combinatorial Program Number 4 it is not necessary to construct a positional array. The knowledge gained from the evaluation of Combinatorial Program Number 2

TABLE 22. Positional Array for Testing the Compatibility of a Single Type (15, 30) Commutator Used in Combination with a Single Type (5, 30) Commutator and a Single Type (3, 50) Commutator

COMBINATORIAL POSITIONS TYPE (15, 30), TYPE (5, 30)	TYPE (3, 30) PRIMARY POSITIONS 1	2	3	4	5	6	7	8	9	10
1,2	1,2,1 (1)	1,2,2 (2)	1,2,3 (3)	1,2,4 (14)	1,2,5 (5)	1,2,6 (26)	1,2,7 (7)	1,2,8 (8)	1,2,9 (9)	1,2,10 (20)
1,4	1,4,1 (1)	1,4,2 (22)	1,4,3 (3)	1,4,4 (4)	1,4,5 (5)	1,4,6 (16)	1,4,7 (7)	1,4,8 (28)	1,4,9 (9)	1,4,10 (10)
1,6	1,6,1 (1)	1,6,2 (12)	1,6,3 (3)	1,6,4 (24)	1,6,5 (5)	1,6,6 (6)	1,6,7 (7)	1,6,8 (18)	1,6,9 (9)	1,6,10 (30)
2,1	2,1,1 (1)	2,1,2 (2)	2,1,3 (13)	2,1,4 (4)	2,1,5 (25)	2,1,6 (6)	2,1,7 (7)	2,1,8 (8)	2,1,9 (19)	2,1,10 (10)
2,3	2,3,1 (21)	2,3,2 (2)	2,3,3 (3)	2,3,4 (4)	2,3,5 (15)	2,3,6 (6)	2,3,7 (27)	2,3,8 (8)	2,3,9 (9)	2,3,10 (10)
2,5	2,5,1 (11)	2,5,2 (2)	2,5,3 (23)	2,5,4 (4)	2,5,5 (5)	2,5,6 (6)	2,5,7 (17)	2,5,8 (8)	2,5,9 (29)	2,5,10 (10)

together with the fact that a Type (1, 30) commutator may always be used in any unoccupied gate permit this conclusion. To determine the required strapping arrangement, it is simply necessary to remove one of the Type (5, 30) commutators and to replace it with five Type (1, 30) commutators utilizing the master control unit gates vacated. Thus the resulting strapping arrangement may be illustrated as follows:

Commutator Type	Primary Position	Master Control Unit Gates Occupied
15-30	1	1, 3, 5, ..., 29 (odd integers only)
5-30	2	2, 8, 14, 20, 26
5-30	4	4, 10, 16, 22, 28
1-30	6	6
1-30	12	12
1-30	18	18
1-30	24	24
1-30	30	30

Evaluation of Combinatorial Program Number 3 precluded the necessity for further evaluation of Combinatorial Programs Numbers 5, 6, and 7. Each of these programs involve the simultaneous use of Type (15, 30), Type (5, 30) and Type (3, 30) commutators and this possibility was ruled out as a result of the prior evaluation.

Combinatorial Program Number 8 is treated in a manner similar to that used to evaluate Program 4. The strapping arrangement for Program 4 is modified by removing one of the Type (5, 30) commutators and replacing it with five Type (1, 30) commutators. In this way, Combinatorial Position 8 is thus evaluated without having to construct an additional array. The new strapping arrangement is easily defined by simply assigning the Type (1, 30) commutators to the gates vacated by the Type (5, 30) commutator.

Tables 23 through 26 present the positional arrays required to test Combinatorial Program Number 9 for joint occupancy. These same tables facilitated the testing of Combinatorial Programs 10 through 14. In the latter cases, it is seen that by successively replacing the Type (3, 30) commutators with Type (1, 30) commutators the strapping arrangements for each of the programs may be determined. It is therefore concluded that each of these combinatorial programs furnish several feasible strapping arrangements for their accomplishment.

We have thus determined that Combinatorial Programs 1, 2, 4, 8, 9, 10, 11, 12, 13, and 14 each have one or more feasible strapping arrangements. Consequently, each now belongs to the set of feasible PAM Commutation System Programs for the 30-Channel Multi-mode Commutator System.

EVALUATION OF GENERATED PROGRAMS

Each program generated must next be evaluated in terms of the channel capacities and sampling rates it offers. The accomplishment of this requirement is described in the following paragraphs.

CHANNEL CAPACITY. The maximum channel capacity of the 30-channel PAM commutator system is 900 channels. This occurs when each 30-channel commutator is attached to a single gate of the 30 gate master control unit and is computed as follows:

$$C = N(M/g) = 30(30/1) = 900 \text{ channels.}$$

A minimum channel capacity of 30 results when a single commutator is strapped to all 30 gates of the master control unit.

TABLE 23. Positional Array for Testing Joint Occupancy of a Single Type (15, 30) Commutator Used in Combination with Two Type (3, 30) Commutator

COMBINATORIAL POSITIONS TYPE (15, 30), TYPE (3, 30)	TYPE (3, 30) PRIMARY POSITIONS									
	1	2	3	4	5	6	7	8	9	10
1,2	1, 2,1 (1)	1, 2,2 (2)	1, 2,3 (3)	1, 2,4	1, 2,5 (5)	1, 2,6	1, 2,7 (7)	1, 2,8	1, 2,9 (9)	1, 2,10
1,4	1, 4,1 (1)	1, 4,2	1, 4,3 (3)	1, 4,4 (4)	1, 4,5 (5)	1, 4,6	1, 4,7 (7)	1, 4,8	1, 4,9 (9)	1, 4,10
1,6	1, 6,1 (1)	1, 6,2	1, 6,3 (3)	1, 6,4	1, 6,5 (5)	1, 6,6 (6)	1, 6,7 (7)	1, 6,8	1, 6,9 (9)	1, 6,10
1,8	1, 8,1 (1)	1, 8,2	1, 8,3 (3)	1, 8,4	1, 8,5 (5)	1, 8,6	1, 8,7 (7)	1, 8,8 (8)	1, 8,9 (9)	1, 8,10
1,10	1,10,1 (1)	1,10,2	1,10,3 (3)	1,10,4	1,10,5 (5)	1,10,6	1,10,7 (7)	1,10,8	1,10,9 (9)	1,10,10 (10)
2,1	2, 1,1 (1)	2, 1,2 (2)	2, 1,3	2, 1,4 (4)	2, 1,5	2, 1,6 (6)	2, 1,7	2, 1,8 (8)	2, 1,9	2, 1,10 (10)
2,3	2, 3,1	2, 3,2 (2)	2, 3,3 (3)	2, 3,4 (4)	2, 3,5	2, 3,6 (6)	2, 3,7	2, 3,8 (8)	2, 3,9	2, 3,10 (10)
2,5	2, 5,1	2, 5,2 (2)	2, 5,3	2, 5,4 (4)	2, 5,5 (5)	2, 5,6 (6)	2, 5,7	2, 5,8 (8)	2, 5,9	2, 5,10 (10)
2,7	2, 7,1	2, 7,2 (2)	2, 7,3	2, 7,4 (4)	2, 7,5	2, 7,6 (6)	2, 7,7 (7)	2, 7,8 (8)	2, 7,9	2, 7,10 (10)
2,9	2, 9,1	2, 9,2 (2)	2, 9,3	2, 9,4 (4)	2, 9,5	2, 9,6 (6)	2, 9,7	2, 9,8 (8)	2, 9,9 (9)	2, 9,10 (10)

TABLE 24. Positional Array for Testing Joint Occupancy of a Single Type (15, 30) Commutator Used in Combination with Three Type (3, 30) Commutators

COMBINATORIAL POSITIONS TYPE (15, 30), TYPE (3, 30), TYPE (3, 30)	TYPE (3, 30) PRIMARY POSITIONS									
	1	2	3	4	5	6	7	8	9	10
1,2,4	1,2,4,1 (1)	1,2,4,2 (2)	1,2,4,3 (3)	1,2,4,4 (4)	1,2,4,5 (5)	1,2,4,6	1,2,4,7 (7)	1,2,4,8	1,2,4,9 (9)	1,2,4,10
1,2,6	1,2,6,1 (1)	1,2,6,2 (2)	1,2,6,3 (3)	1,2,6,4	1,2,6,5 (5)	1,2,6,6 (6)	1,2,6,7 (7)	1,2,6,8	1,2,6,9 (9)	1,2,6,10
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2,9,7	2,9,7,1	2,9,7,2 (2)	2,9,7,3	2,9,7,4 (4)	2,9,7,5	2,9,7,6 (6)	2,9,7,7 (7)	2,9,7,8 (8)	2,9,7,9 (9)	2,9,7,10 (10)

TABLE 25. Positional Array for Testing Joint Occupancy of a Single Type (15, 30) Commutator Used in Combination with Four Type (3, 30) Commutators

COMBINATORIAL POSITIONS TYPE (15,30) TYPE (3,30) TYPE (3,30)	TYPE (3, 30) PRIMARY POSITIONS								
	1	2	3	. . .	6	7	8	9	10
1,2,4,6	1,2,4,6,1 (1)	1,2,4,6,2 (2)	1,2,4,6,3 (3)	⋮	1,2,4,6,6 (6)	1,2,4,6,7 (7)	1,2,4,6,8	1,2,4,6,9 (9)	1,2,4,6,10
1,2,4,8	1,2,4,8,1 (1)	1,2,4,8,2 (2)	1,2,4,8,3 (3)	⋮	1,2,4,8,6	1,2,4,8,7 (7)	1,2,4,8,8 (8)	1,2,4,8,9 (9)	1,2,4,8,10
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2,9,7,5	2,9,7,5,1	2,9,7,5,2 (2)	2,9,7,5,3	.	2,9,7,5,6 (6)	2,9,7,5,7 (7)	2,9,7,5,8 (8)	2,9,7,5,9 (9)	2,9,7,5,10 (10)

TABLE 26. Positional Array for Testing Joint Occupancy of a Single Type (15, 30) Commutator Used in Combination with Four Type (3, 30) Commutators

COMBINATORIAL POSITIONS TYPE (15,30) TYPE (3,30) TYPE (3,30) TYPE (3,30)	TYPE (3, 30) PRIMARY POSITIONS						
	1	2	...	7	8	9	10
1,2,4,6,8	1,2,4,6, 8,1 (1)	1,2,4,6 8,2 (2)	⋮	1,2,4,6, 8,7 (7)	1,2,4,6, 8,8 (8)	1,2,4,6, 8,9 (9)	1,2,4,6, 8,10
1,2,4,6,10	1,2,4,6,10,1 (1)	1,2,4,6,10,2 (2)	⋮	1,2,4,6,10,7 (7)	1,2,4,6,10,8	1,2,4,6,10,9 (9)	1,2,4,6,10,10 (10)
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2,9,7,5,3	2,9,7,5, 3,1	2,9,7,5, 3,2 (2)	⋮	2,9,7,5, 3,7 (7)	2,9,7,5, 3,8 (8)	2,9,7,5, 3,9 (9)	2,9,7,5, 3,10 (10)

It has been shown that a single commutator may be strapped to the gates of the 30-channel commutator system's master control unit in only eight different ways. Thus, a single commutator may be strapped to 1, 2, 3, 5, 6, 10, 15, or 30 gates. Consequently, the reduction in total maximum channel capacity which must be taken for each occurrence of these strapping arrangements may be summarized as follows:

Number of Gates Strapped to a Single Commutator	Reduction in Total Channel Capacity/Occurrence
30	870
15	420
10	240
6	150
5	120
3	60
2	30
1	0

It has also been noted, that when a single commutator is strapped to more than one gate it retains its inherent channel capacity (30 in this case). Expressed in terms of data channels, each commutator in the 30-channel system will have a capacity of thirty minus three or 27 data channels. In evaluating the capacity for a particular program, it should be recalled that capacity will be summarized as the total available at a given sampling rate. Examples of alternative ways to accomplish this will be illustrated in the remaining sections of this chapter.

SAMPLING RATE. As previously noted, sampling rates (R_f) expressed in samples a second are a function of the time rate r at which each gate is opened and the number of gates g to which a commutator is strapped. In general, the relationship is expressed as: $R_f = r\ g$. The master control unit gates of the 30-channel commutator system are scanned sequentially at a rate of 4 times a second. Consequently, sampling rates for each of the eight commutators provided by the system may be summarized as follows.

Commutator Type	Sampling Rate Data Channels or Samples/Second
30-30	120
15-30	60
10-30	40
6-30	24
5-30	20
3-30	12
2-30	8
1-30	4

The format to be used in indicating the sampling rates for a particular program will be illustrated in the following sections of this chapter.

PRESENTATION OF PROGRAMS

Appendix B summarizes the feasible programs, a total of 305, which may be used with the 30-channel multi-mode PAM commutator system. A sample page from the Appendix is presented as Table 27. The programs have been listed in descending order according to the sampling rates included within and between programs and each program assigned a number as indicated in column one of the table. Column two indicates the sampling rate or rates included in a particular program expressed in frames per second (or data channels per second). Commutator type is indicated in column three. Note that by summing the latter half of the commutator type identification of all the commutators within a particular program, the total commutator channel capacity for the program may be determined. For instance, the channel capacity for program 2 is 30 plus 30 or 60 channels. Column four indicates the specific master control unit gates to which the outputs of a particular commutator within a program must be strapped.

TABLE 27. Sample Page from Appendix B Illustrating Program Format

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
1	120	30-30	1, 2, 3, ..., 30
2	60	15-30	1, 3, 5, ..., 29 (odd integers)
	60	15-30	2, 4, 6, ..., 30 (even integers)
3	60	15-30	1, 3, 5, ..., 29 (odd integers)
	20	5-30	2, 8, 14, 20, 26
	20	5-30	4, 10, 16, 22, 28
	20	5-30	6, 12, 18, 24, 30
4	60	15-30	1, 3, 5, ..., 29 (odd integers)
	20	5-30	2, 8, 14, 20, 26
	20	5-30	4, 10, 16, 22, 28
	4	1-30	6
	4	1-30	12
	4	1-30	18
	4	1-30	24
	4	1-30	30
5	60	15-30	1, 3, 5, ..., 29 (odd integers)
	20	5-30	2, 8, 14, 20, 26
	4	1-30	4
	4	1-30	10
	4	1-30	16
	4	1-30	22
	4	1-30	28
	4	1-30	6
	4	1-30	12
	4	1-30	18
	4	1-30	24
	4	1-30	30

PROGRAM SELECTION

Programs for the 30-channel multi-mode commutator system provide a choice of eight different sampling rates in a variety of combinations. Specifically, the rates which may be elected are 4, 8, 12, 20, 24, 40, 60 and 120 data channels a second. Sampling rate requirements must be determined primarily on the basis of the nature of the information being sampled. This determination must be tempered, however, by the fact that as the sampling rate is increased, the total number of data channels available decreases. It should be noted that data channels available change in discrete increments of 27 channels (or 30 commutator channels) each.

The following procedure is suggested as an aid to the users of the 30-channel multi-mode PAM commutator system in selecting a specific program from the 305 feasible strapping arrangement programs available.

First, establish the desired sampling rates and the number of channels to be sampled at each rate. In accomplishing this step remember that only eight different rates are available as listed above. Also recall that the number of data channels utilized must be a multiple of 27.

Next, consult Table 28 which presents a summary of all the feasible programs which may be used with the 30-channel multi-mode PAM commutator system. Note that each program is identified by the data channels it offers at specific sampling rates expressed in data channels a second. Select the program or programs which most nearly meets the specified sampling requirements. Remember if none of the programs fit the requirements exactly, a compromise must be reached.

After a particular program has been selected from Table 28, match the selected program number with the identical program number listed in Appendix B. The type commutators required and the specific strapping arrangements to be used are then read directly from the program listed in Appendix B.

TABLE 28. Program Identification by Data Channel Capacity and Sampling Rate in Data Channels a Second

Program Number	Data Channels	Samples a Second
1	27	120
2	54	60
3	27 81	60 20
4	27 54 35	60 20 4
5	27 27 270	60 20 4
6	27 135	60 12
7	27 108 81	60 12 4
8	27 81 162	60 12 4
9	27 54 243	60 12 4
10	27 27 324	60 12 4
11	27 405	60 4
12	81	40
13	54 54	40 20
14	54 27 135	40 20 4
15	54 135	40 8
16	54 108 54	40 8 4
17	54 81 108	40 8 4
18	54 54 162	40 8 4
19	54 27 216	40 8 4
20	54 270	40 4
21	27 108	40 20
22	27 81 135	40 20 4
23	27 54 135	40 20 4
24	27 54 108 54	40 20 8 4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second
25	27	40
	54	20
	81	8
	108	4
26	27	40
	54	20
	54	8
	162	4
27	27	40
	54	20
	27	8
	216	4
28	27	40
	54	20
	270	4
29	27	40
	27	20
	135	8
	135	4
30	27	40
	27	20
	108	8
	189	4
31	27	40
	27	20
	81	8
	243	4
32	27	40
	27	20
	54	8
	297	4
33	27	40
	27	20
	27	8
	351	4
34	27	40
	27	20
	405	4
35	27	40
	270	8
36	27	40
	243	8
	54	4
37	27	40
	216	8
	108	4
38	27	40
	189	8
	162	4
39	27	40
	162	8
	216	4
40	27	40
	135	8
	270	4
41	27	40
	108	8
	324	4
42	27	40
	81	8
	378	4
43	27	40
	54	8
	432	4
44	27	40
	27	8
	486	4
45	27	40
	540	4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second
46	135	24
47	108	24
	54	12
48	108	24
	27	12
	81	4
49	81	24
	108	12
50	81	24
	81	12
	81	4
51	81	24
	54	12
	81	8
52	81	24
	54	12
	54	8
	54	4
53	81	24
	54	12
	27	8
	108	4
54	81	24
	54	12
	162	4
55	81	24
	27	12
	81	8
	81	4
56	81	24
	27	12
	54	8
	135	4
57	81	24
	27	12
	27	8
	189	4
58	54	24
	162	12
59	54	24
	135	12
	81	4
60	54	24
	108	12
	81	8
61	54	24
	108	12
	54	8
	54	4
62	54	24
	108	12
	27	8
	108	4
63	54	24
	108	12
	162	4
64	54	24
	81	12
	81	8
	81	4
65	54	24
	81	12
	54	8
	135	4
66	54	24
	81	12
	27	8
	189	4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second
67	54	24
	81	12
	243	4
68	54	24
	54	12
	162	8
69	54	24
	54	12
	135	8
	54	4
70	54	24
	54	12
	108	8
	108	4
71	54	24
	54	12
	81	8
	162	4
72	54	24
	54	12
	54	8
	216	4
73	54	24
	81	12
	27	8
	270	4
74	54	24
	54	12
	324	4
75	54	24
	27	12
	162	8
	81	4
76	54	24
	27	12
	135	8
	135	8
77	54	24
	27	12
	108	8
	189	4
78	54	24
	27	12
	81	8
	243	4
79	54	24
	27	12
	54	8
	297	4
80	54	24
	27	12
	27	8
	351	4
81	54	24
	27	12
	405	4
82	27	24
	216	12
83	27	24
	189	12
	81	4
84	27	24
	162	12
	81	8
85	27	24
	162	12
	54	8
	54	4
86	27	24
	162	12
	27	8
	108	4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second
87	27	24
	162	12
	162	4
88	27	24
	135	12
	81	8
	81	4
89	27	24
	135	12
	54	8
	135	4
90	27	24
	135	12
	27	8
	189	4
91	27	24
	135	12
	243	4
92	27	24
	108	12
	135	8
93	27	24
	108	12
	135	8
	54	4
94	27	24
	108	12
	108	8
	108	4
95	27	24
	108	12
	81	8
	162	4
96	27	24
	108	12
	54	8
	216	4
97	27	24
	108	12
	27	8
	270	4
98	27	24
	108	12
	324	4
99	27	24
	81	12
	162	8
	81	4
100	27	24
	81	12
	135	8
	135	4
101	27	24
	81	12
	108	8
	189	4
102	27	24
	81	12
	81	8
	243	4
103	27	24
	81	12
	54	8
	297	4
104	27	24
	81	12
	27	8
	351	4
105	27	24
	81	12
	405	4
106	27	24
	54	12
	243	8

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second	Program Number	Data Channels	Samples a Second
107	27	24	116	27	24
	54	12		27	12
	216	8		243	8
	54	4		81	4
108	27	24	117	27	24
	54	12		27	12
	189	8		216	8
	108	4		135	4
109	27	24	118	27	24
	54	12		27	12
	162	8		189	8
	162	4		189	4
110	27	24	119	27	24
	54	12		27	12
	135	8		162	8
	216	4		243	4
111	27	24	120	27	24
	54	12		27	12
	108	8		135	8
	270	4		297	4
112	27	24	121	27	24
	54	12		27	12
	81	8		108	8
	324	4		351	4
113	27	24	122	27	24
	54	12		27	12
	54	8		81	8
	378	4		405	4
114	27	24	123	27	24
	54	12		27	12
	27	8		54	8
	432	4		459	4
115	27	24	124	27	24
	54	12		27	12
	486	4		27	8
				513	4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second	Program Number	Data Channels	Samples a Second
125	27 27 567	24 12 4	137	27 27 594	24 8 4
126	27 324	24 8	138	27 648	24 4
127	27 297 54	24 8 4	139	162	20
			140	135 135	20 4
128	27 270 108	24 8 4	141	108 135	20 8
129	27 243 162	24 8 4	142	108 108 54	20 8 4
130	27 216 216	24 8 4	143	108 81 108	20 8 4
131	27 189 270	24 8 4	144	108 54 162	20 8 4
132	27 162 324	24 8 4	145	108 27 216	20 8 4
133	27 135 378	24 8 4	146	108 270	20 4
134	27 108 432	24 8 4	147	81 135	20 12
			148	81 108 81	20 12 4
135	27 81 486	24 8 4	149	81 81 162	20 12 4
136	27 54 540	24 8 4			

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second
150	81	20
	54	12
	243	4
151	81	20
	27	12
	324	4
152	81	20
	135	8
	135	4
153	81	20
	108	8
	189	4
154	81	20
	81	8
	243	4
155	81	20
	54	8
	297	4
156	81	20
	27	8
	351	4
157	81	20
	405	4
158	54	20
	135	12
	135	4
159	54	20
	108	12
	27	8
	162	4
160	54	20
	108	12
	216	4
161	54	20
	81	12
	54	8
	189	4
162	54	20
	81	12
	27	8
	243	4
163	54	20
	81	12
	297	4
164	54	20
	54	12
	81	8
	216	4
165	54	20
	54	12
	54	8
	270	4
166	54	20
	54	12
	27	8
	324	4
167	54	20
	54	12
	378	4
168	54	20
	27	12
	108	8
	243	4
169	54	20
	27	12
	81	8
	297	4
170	54	20
	27	12
	54	8
	351	4
171	54	20
	27	12
	27	8
	405	4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second
172	54	20
	27	12
	459	4
173	54	20
	270	8
174	54	20
	243	8
	54	4
175	54	20
	216	8
	108	4
176	54	20
	189	8
	162	4
177	54	20
	162	8
	216	4
178	54	20
	135	8
	270	4
179	54	20
	108	8
	324	4
180	54	20
	81	8
	378	4
181	54	20
	54	8
	432	4
182	54	20
	27	8
	486	4
183	54	20
	540	4
184	27	20
	135	12
	270	4
185	27	20
	108	12
	54	8
	243	4
186	27	20
	108	12
	27	8
	297	4
187	27	20
	108	12
	351	4
188	27	20
	81	12
	108	8
	216	4
189	27	20
	81	12
	81	8
	270	4
190	27	20
	81	12
	54	8
	324	4
191	27	20
	81	12
	27	8
	378	4
192	27	20
	81	12
	432	4
193	27	20
	81	12
	162	8
	189	4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second
194	27	20
	54	12
	135	8
	243	4
195	27	20
	54	12
	108	8
	297	4
196	27	20
	54	12
	81	8
	351	4
197	27	20
	54	12
	54	8
	405	4
198	27	20
	54	12
	27	8
	459	10
199	27	20
	54	12
	513	4
200	27	20
	27	12
	216	8
	162	4
201	27	20
	27	12
	189	8
	216	4
202	27	20
	27	12
	162	8
	270	4
203	27	20
	27	12
	135	8
	324	4
204	27	20
	27	12
	108	8
	378	4
205	27	20
	27	12
	81	8
	432	4
206	27	20
	27	12
	54	8
	486	4
207	27	20
	27	12
	27	8
	540	4
208	27	20
	27	12
	594	4
209	27	20
	270	8
	135	4
210	27	20
	243	8
	189	4
211	27	20
	216	8
	243	4
212	27	20
	189	8
	297	4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second
213	27	20
	162	8
	351	4
214	27	20
	135	8
	405	4
215	27	20
	108	8
	459	4
216	27	20
	81	8
	513	4
217	27	20
	54	8
	567	4
218	27	20
	27	8
	621	4
219	27	20
	675	4
220	270	12
221	243	12
	81	4
222	216	12
	81	8
223	216	12
	54	8
	54	4
224	216	12
	27	8
	108	4
225	216	12
	162	4
226	189	12
	81	8
	81	4
227	189	12
	54	8
	135	4
228	189	12
	27	8
	189	4
229	189	12
	243	4
230	162	12
	162	8
231	162	12
	135	8
	54	4
232	162	12
	108	8
	108	4
233	162	12
	81	8
	162	4
234	162	12
	54	8
	216	4
235	162	12
	27	8
	270	4
236	162	12
	324	4
237	135	12
	162	8
	81	4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second
238	135	12
	135	8
	135	4
239	135	12
	108	8
	189	4
240	135	12
	81	8
	243	4
241	135	12
	54	8
	297	4
242	135	12
	27	8
	351	4
243	135	12
	405	4
244	108	12
	243	8
245	108	12
	216	8
	54	4
246	108	12
	189	8
	108	4
247	108	12
	162	8
	162	4
248	108	12
	135	8
	216	4
249	108	12
	108	8
	270	4

Program Number	Data Channels	Samples a Second
250	108	12
	81	8
	324	4
251	108	12
	54	8
	378	4
252	108	12
	27	8
	432	4
253	108	12
	486	4
254	81	12
	243	8
	81	4
255	81	12
	216	8
	135	4
256	81	12
	189	8
	189	4
257	81	12
	162	8
	243	4
258	81	12
	135	8
	297	4
259	81	12
	108	8
	351	4
260	81	12
	81	8
	405	4
261	81	12
	54	8
	459	4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second	Program Number	Data Channels	Samples a Second
262	81 27 513	12 8 4	274	54 54 540	12 8 4
263	81 576	12 4	275	54 27 594	12 8 4
264	54 324	12 8	276	54 648	12 4
265	54 297 54	12 8 4	277	27 324 81	12 8 4
266	54 270 108	12 8 4	278	27 297 135	12 8 4
267	54 243 162	12 8 4	279	27 270 189	12 8 4
268	54 216 216	12 8 4	280	27 243 243	12 8 4
269	54 189 270	12 8 4	281	27 216 297	12 8 4
270	54 162 324	12 8 4	282	27 189 351	12 8 4
271	54 135 378	12 8 4	283	27 162 405	12 8 4
272	54 108 432	12 8 4	284	27 135 459	12 8 4
273	54 81 486	12 8 4	285	27 108 513	12 8 4

TABLE 28. (Continued)

Program Number	Data Channels	Samples a Second
286	27	12
	81	8
	567	4
287	27	12
	54	8
	621	4
288	27	12
	27	8
	675	4
289	27	12
	729	4
290	405	8
291	378	8
	27	4
292	351	8
	108	4
293	324	8
	162	4
294	297	8
	216	4
295	270	8
	270	4
296	243	8
	324	4
297	216	8
	378	4
298	189	8
	432	4
299	162	8
	486	4
300	135	8
	540	4
301	108	8
	594	4
302	81	8
	648	4
303	54	8
	702	4
304	27	8
	756	4
305	810	4

IV. COMPUTER PROGRAMMING OF AN M-GATE PAM COMMUTATOR SYSTEM

Programming logic presented in Chapter II and extended in Chapter III outlined an algorithm for generating feasible strapping arrangement programs to be used with a multi-mode pulse amplitude modulated commutator system. With minor modifications this procedure may be performed by a Digital Computer. This chapter presents the modified procedure and includes a Fortran IV computer program written for the UNIVAC 1107 Computer for its accomplishment.

THE DIGITAL COMPUTER PROGRAM

The digital computer program presented in this chapter was written to determine how both individual and combinations of commutators can be strapped to the gates of the master control unit of the Multi-mode PAM Commutator System. Input required by the program is the number of master control unit gates (M), the number of commutator channels (N), and the number of times a second each master control unit gate is opened (R).

In the design of the program it has been assumed that all feasible strapping arrangements are desired. Consequently, no provision has been made for printing only a portion of the desired strapping arrangements.

Input to the program at present is <u>limited to 60 master control unit gates or less</u>. This limitation was based on the storage capacity available when using the UNIVAC 1107 Computer.

Experience with the program has indicated that the arrays of numbers generated may become extremely large, thus over-running the computer core capacity. This usually occurs when determining combinatorial programs which fully utilize the master control unit capacity. Utilization of the UNIVAC 1107's fast access scratch drum has been made to overcome this problem. As a result, the run time for the program is somewhat longer than would normally be required if the core capacity had been adequately large. Although the use of the scratch drum is faster than the use of magnetic tape for this purpose, it is still necessary to spend much time transferring information into and out of core. Consequently, if it is necessary to run the program on a computer which does not have scratch drums, scratch tapes may be used with only a minor penalty in running time.

MATHEMATICAL PROCEDURES

As previously noted, the mathematical methods used in the computer program follow very closely those presented in the programming logic as discussed in Chapter II. The mathematical and programming nomenclature required have been summarized and are presented as Table 29.

In general, the method utilized may be summarized as follows: The factors (g_i) of the number of master control unit gates (M) are computed and stored to be used later to find the gates to which a specific type commutator may be strapped. Next, the number of ways that a specific type commutator can be strapped to the master control unit are found. These ways or strapping arrangements are then generated and stored. There will be M/g ways of strapping a single Type (g, N) commutator to the master control unit and each strapping arrangement will make use of g gates. When enough commutators are strapped in combination to the master control unit simultaneously, all of the unit's gates will be occupied thereby creating a strapping arrangement program. The computer program generates all the possible strapping arrangement programs which will utilize exactly M gates. Each program

TABLE 29. Mathematical and Programming Nomenclature

Math Symbol	Program Symbol	Definition
	M	Master control unit gate capacity.
	N	Number of channels per commutator.
	R	Number of times a second master control unit gate is opened.
g_i	IDIV(I)	The i^{th} integral divisor of M less than M. Number of gates to which the commutator is attached.
	ICNT	The number of integers less than M that divide M evenly.
	IWD(I, J, K)	A position in which a Type (g, N) commutator may be used.
	ICOMB(I)	An array of commutators that are possibilities for strapping.
	LTH	The number of gates strapped to a commutator when combining two types of commutators.
	LGNTH	The number of unique ways that any two types of commutators can be combined so that joint occupancy does not occur.
Δ	IDEL	The number of distinct positions in which a Type (g, N) commutator may be used.
	IVAL	Dummy array for transferring information from tape.
	IARRAY(I)	An array of gates that are checked for joint occupancy.

thus generated is tested to see if joint occupancy is required. If joint occupancy is not required, the strapping arrangement program is saved to be printed out later; otherwise, it is discarded. A detailed flow chart of the modified procedure has been included as Appendix C.

INPUT PREPARATION AND OUTPUT DESCRIPTION

Input to the computer program requires only one data card punched in the following format:

Column	Word Type	Definition
1-10	fixed	Number of master control unit gates available (must be equal to or less than 60).
11-20	fixed	Number of channels per commutator.
21-30	floating	Number of times a second each master control unit gate is opened.

Three types of output are given. They are the factors of M, the primary positions and the strapping arrangement programs.

Table 30 illustrates the first two types of output. The factors of M are identified as divisors and represent the commutator types which may be used within a particular system. Primary Position Output immediately follows. It lists the commutators by type and indicates the various ways in which each may be individually strapped. Sampling rates (SR) are given and immediately follow the Type (g, N) identification. Each row in the column of numbers listed immediately below a particular commutator type identification represents a unique strapping arrangement. Because of space limitations, commas have been omitted between strapping points. Consequently, particular care should be exercised in interpreting the strapping arrangements where ten or more master control unit gates are required.

TABLE 30. A Sample Output for a 6 Gate Master Control Unit Strapping Arrangement Program Set - Page 1

Page 1

```
DIVISORS OF 6 ARE 1 2 3

                    PRIMARY POSITIONS
TYPE (1, 30)        COMMUTATOR (SR _ 4.00)
     1
     2
     3
     4
     5
     6
TYPE (2, 30)        COMMUTATOR (SR _ 8.00)
     1     4
     2     5
     3     6

TYPE (3, 30)        COMMUTATOR (SR _ 12.00)

     1  3  5
     2  4  6
```

Table 31 indicates the format used to present individual strapping arrangement programs. Each program or STRAPPING ARRANGEMENT is first identified by listing the g's of the Type (g, N) commutators of which it is composed. For instance, STRAPPING ARRANGEMENT 3 1 1 1 indicates a combinatorial program utilizing one Type (3, N) commutator and three Type (1, N) commutators. The 3 1 1 1 notation also indicates how to interpret the associated strapping arrangements presented as arrays immediately under the identification line. Each row of the array presents a feasible strapping arrangement. For this example the array presents two choices listed as 1 3 5 2 4 6 and 2 4 6 1 3 5. The 3 1 1 1 notation together with these choices would be interpreted as follows:

Array Listing	Commutator Type	Master Control Unit Program
1 3 5 2 4 6	Type (3, N)	1, 3, 5
	Type (1, N)	2
	Type (1, N)	4
	Type (1, N)	6
2 4 6 1 3 5	Type (3, N)	2, 4, 6
	Type (1, N)	1
	Type (1, N)	3
	Type (1, N)	5

TABLE 31. A Sample Output for a 6 Gate Master Control Unit Strapping Arrangement Program Set, Page 2

Page 2

STRAPPING ARRANGEMENT 3 3

1 3 5 2 4 6

STRAPPING ARRANGEMENT 3 1 1 1

1 3 5 2 4 6
2 4 6 1 3 5

STRAPPING ARRANGEMENT 2 2 2

1 4 2 5 3 6

STRAPPING ARRANGEMENT 2 2 1 1

1 4 2 5 3 6
1 4 3 6 2 5
2 5 3 6 1 4

STRAPPING ARRANGEMENT 2 1 1 1 1

1 4 2 3 5 6
2 5 1 3 4 6
3 6 1 2 4 5

STRAPPING ARRANGEMENT 1 1 1 1 1 1

1 2 3 4 5 6

OPERATION INFORMATION

Both program and data are input on standard key-punched cards. Two scratch drum areas (or scratch tapes) are required during processing. The deck setup and control cards used are standard to the UNIVAC 1107 Computer system.

End of run will occur when the strapping arrangement program is found to be composed of Type (1, N) commutators only. Normal exit will occur at this time.

Run time for this program is a function of the number of master control unit gates M, the number of divisors of M, and the imposed restrictions. Consequently, run time required is extremely hard to estimate. Compilation and run time for the example in this chapter (a master control unit with 6 gates) required 40 seconds. Print out is also a function of the preceding factors. For M equal to 6, two pages were required for the print out. However, it is anticipated that the compilation and run time for a 30-gate system may require more than an hour. Also, the print out might include as many as 100 pages.

PROGRAM INFORMATION

Complete program listings for the designed Fortran IV Computer are attached as Appendix D of this report. In designing the program, the following UNIVAC 1107 Library Subroutines were utilized:

NPAUS$	NBUFF$	NIER$
NTAB$	NFOUT$	NFINP$
NFMT$	NOUT$	NRWND$
NINPT$	NFTV$	

The program requires 5,275 octal* locations for code and

* The octal number system has a radix of eight and uses the digits 0, 1, 2, 3, 4, 5, 6, and 7. The number 5,278 octal may be indicated alternately as $5{,}275_8$ and is interpreted in powers of 8 notation as:

$$5(8)^3 + 2(8)^2 + 7(8)^1 + 5(8)^0.$$

$45{,}766_8$ locations for data. If it becomes necessary to run the program on a computer with less than 65 K core storage, it is suggested that M be limited to 30 or less. In this way, storage requirements would be reduced by approximately 32,274 octal locations. To accomplish this, the dimensions of IWD should be changed to (10, 30, 15).

As written, the program is divided into seven parts - a main program and six subroutines. The variables used have been presented in Table 29. A discussion of the program segments follows.

MAIN PROGRAM. The main program reads all inputs and controls the flow of the program. Normal exit from the program is also through the main program. Storage requirements are 151_8 cells for the code and $43{,}213_8$ for the data.

SUBROUTINE DIVISOR (M, IDIV, ICNT). Subroutine DIVISOR finds the factors of M which are used to define the commutator types which may be used within the PAM system. Storage requirements are 52_8 cells for code and 12_8 for the data.

SUBROUTINE PTRN (IDIV, I, M, IWD). Subroutine PTRN generates a list of the commutator types which may be used and the primary strapping arrangements for each type. Storage requirements are 110_8 cells for code and 24_8 for data.

SUBROUTINE DIVCMB (M, IDIV, ICNT, IWD). Subroutine DIVCMB generates all the possible combinatorial positions which if found to be feasible would fully utilize the master control unit gate capacity. Storage requirements are 204_8 cells for code and 230_8 for data.

SUBROUTINE SETUP (J, ICOMB, M, IWD, IDIV, IKK). Subroutine SETUP tests those possible combinatorial positions generated in DIVCMB to determine if they meet the previously defined positional, combinatorial and capacity restrictions. Storage requirements are 241_8 cells for code and 227_8 for data.

SUBROUTINE FIND (IKK, M, II, IDIV, LGNTH, LTH, ICOMB, IVAL, K). Subroutine FIND is utilized as a integral part of Subroutine SETUP. It attempts to strap a particular type of commutator to a master control unit which already has one or more commutators strapped to it. Storage requirements are 255_8 cells for code and 144_8 for data.

SUBROUTINE SAVE (IWD, LTH, II, JJ, MTEST, IVAL). Subroutine SAVE stores all feasible strapping arrangement programs on the scratch drum. Storage requirements are 101_8 cells for code and 117_8 for the data.

It should be noted that the required octal locations listed were based on a computation by UNIVAC 1107 Fortran IV dated February 10, 1965, F 4003. As the basic language is revised in the future the octal locations listed may also require revision.

V. SUMMARY AND RECOMMENDATIONS

The 30-channel multi-mode PAM commutator system offers many outstanding features. Triple redundancy in its master control unit and mixing circuits assures the ultra reliability of the system. Its use simplifies and reduces the weight of missile wiring since small commutator units may be placed close to their signal sources. Large bundles of long wires leading to the commutator assembly may thus be eliminated. This in turn results in not only a weight reduction, but also in a reduction of system noise as well. The system's high and/or low level commutators are directly interchangeable because their output characteristics are the same. All types of commutation requirements can thus be handled by only two basic types of commutator units. The master control unit and the commutators used may be synchronized either internally or with an external clock and the system may be operated in any one of five different modes. In addition, the commutators may be operated independently of the master control unit. Special master sub-frame synchronization pulses are inserted after the tenth and twentieth frames and after the thirtieth frame to facilitate data identification. The system's most outstanding feature, however, is its flexibility in the many different combinations of channel capacities and sampling rates it offers. Channel capacities offered by the system may be varied from thirty through 900 channels. A choice of eight different sampling rates is provided: 4, 8, 12, 20, 24, 40, 60, and 120 data channels or samples a second. Over 300 different channel capacity and sampling rate combinations are provided by the system. The system also permits the elimination of unused data channels.

SUMMARY

The underlying logic and development of an algorithm to be used in programming the system was presented in Chapter II. A description of how the algorithm was applied to determine all of the feasible programs for the system was presented in Chapter III and the developed programs attached as Appendix B to this report. Thus, the 30 channel system's potential flexibility has been assured. An important fact however, is that the developed algorithm may be used to determine the feasible programs for similar multi-mode commutator systems which have any M number of master control unit gates. In addition, a Fortran IV computer program for executing the algorithm has been presented in Chapter IV. Consequently, the many man-hours of work normally required for programming will no longer be required in programming and evaluating future systems.

RECOMMENDATIONS

During the performance of the work reported here, many ideas for further research on multi-mode commutator systems became apparent to the authors. Some of the ideas concerned possible improvements in the present system while others were concerned with the development of future systems. Several seemed to have possible merit and are summarized here as recommendations for further research.

PROGRAMMING COMMUTATOR INPUTS. The effort described in this report has been concerned with determining the feasible ways in which the output of one or more commutators may be strapped to one or more gates of the system's master control unit. Our expressed objective was to provide a variety of commutator programs differing in the combinations of channel capacities and sampling rates offered. It seems that a similar effort should be made to determine the feasible ways in which inputs may be strapped to more than one of the channels of a commutator. In this way, perhaps an even greater variety of sampling rates and channel capacities may be found possible without modifying the present system. This same study should also consider the feasibility of strapping an input to more than one commutator.

COMPARATIVE EVALUATION WITH OTHER SYSTEMS. The commutator system which was the object of this study was noted to have many inherent advantages. The true worth of the system may be only determined, however, by comparing it with alternative systems. Consequently it is recommended that a comparative study be performed to accomplish this objective. The evaluation should include such factors as cost, weight, accuracy, precision and reliability.

MODIFIED SYNCHRONIZATION AND IDENTIFICATION. Programming of the present system has assumed that the symmetrical sampling requirement must be based on a sampling cycle limited to one master frame; i.e., 30 gates of the master control unit. It seems possible that by modifying the synchronization and identification mechanisms of the present system, the sampling cycle might be changed to some other multiple of the master frame. For example, a sampling cycle might be redefined to include two scannings of the master control unit gates. If this practice is found to be feasible, it would have the same effect as increasing the number of master control unit gates available. Consequently a greater variety of sampling rates and channel capacities should result. Therefore it is recommended that a study be made to determine the practicability of this suggestion.

VARIABLE SCANNING RATE. In the present system the rate of scanning the master control unit's gates is "fixed" at four times a second. If a variable scanning rate could be provided, it would provide an almost unlimited variety of data channel sampling rates. An investigation is therefore recommended to determine the feasibility of this suggestion.

OPTIMIZATION OF SYSTEM PARAMETERS. A multi-mode system may be classified by M, N, and R. The present system has M = 30, N = 30, and R = 4. A question thus arises as to why these particular values were specified. If criteria can be developed for specifying these parameters, a procedure might be developed to optimize these parameters in the design of future systems. Consequently, a study to determine a basis for these parameters is also recommended.

APPENDIX A

Positional Arrays for Testing the Joint Occupancy When Using Two Different Types of Commutators Singly in Combination in a 30-Gate PAM Commutator System

TABLE A1. Positional Array for Testing the Joint Occupancy of a Single Type (10, 30) Commutator in Combination with a Single Type (6, 30) Commutator

TYPE (10, 30) PRIMARY POSITIONS	TYPE (6, 30) PRIMARY POSITIONS: 1	2	3	4	5
1	1,1 (1)	1,2 (7)	1,3 (13)	1,4 (4)	1,5 (10)
2	2,1 (11)	2,2 (2)	2,3 (8)	2,4 (14)	2,5 (5)
3	3,1 (6)	3,2 (12)	3,3 (3)	3,4 (9)	3,5 (15)

TABLE A2. Positional Array for Testing the Joint Occupancy of a Single Type (10, 30) Commutator in Combination with a Single Type (5, 30) Commutator

TYPE (10, 30) PRIMARY POSITIONS	TYPE (5, 30) PRIMARY POSITIONS: 1	2	3	4	5	6
1	1,1 (1)	1,2	1,3	1,4 (4)	1,5	1,6
2	2,1	2,2 (2)	2,3	2,4	2,5 (5)	2,6
3	3,1	3,2	3,3 (3)	3,4	3,5	3,6 (6)

TABLE A3. Positional Array for Testing the Joint Occupancy of a Single Type (10, 30) Commutator in Combination with a Single Type (3, 30) Commutator

TYPE (10, 30) PRIMARY POSITIONS	TYPE (3, 30) PRIMARY POSITIONS: 1	2	3	4	5	6	7	8	9	10
1	1,1 (1)	1,2 (22)	1,3 (13)	1,4 (4)	1,5 (25)	1,6 (16)	1,7 (7)	1,8 (28)	1,9 (19)	1,10 (10)
2	2,1 (11)	2,2 (2)	2,3 (23)	2,4 (14)	2,5 (5)	2,6 (26)	2,7 (17)	2,8 (8)	2,9 (29)	2,10 (20)
3	3,1 (21)	3,2 (12)	3,3 (3)	3,4 (24)	3,5 (15)	3,6 (6)	3,7 (27)	3,8 (18)	3,9 (9)	3,10 (30)

TABLE A4. Positional Array for Testing the Joint Occupancy of a Single Type (10, 30) Commutator in Combination with a Single Type (2, 30) Commutator

TYPE (10, 30) PRIMARY POSITIONS	TYPE (2, 30) PRIMARY POSITIONS: 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1,1 (1)	1,2	1,3	1,4 (4)	1,5	1,6	1,7 (7)	1,8	1,9	1,10 (10)	1,11	1,12	1,13 (13)	1,14	1,15
2	2,1	2,2 (2)	2,3	2,4	2,5 (5)	2,6	2,7	2,8 (8)	2,9	2,10	2,11 (11)	2,12	2,13	2,14 (14)	2,15
3	3,1	3,2	3,3 (3)	3,4	3,5	3,6 (6)	3,7	3,8	3,9 (9)	3,10	3,11	3,12 (12)	3,13	3,14	3,15 (15)

TABLE A5. Positional Array for Testing the Joint Occupancy of a Single Type (6, 30) Commutator in Combination with a Single Type (5, 30) Commutator

		TYPE (5, 30) PRIMARY POSITIONS					
		1	2	3	4	5	6
TYPE (6, 30) PRIMARY POSITIONS	1	1,1 (1)	1,2 (26)	1,3 (21)	1,4 (16)	1,5 (11)	1,6 (6)
	2	2,1 (7)	2,2 (2)	2,3 (27)	2,4 (22)	2,5 (17)	2,6 (12)
	3	3,1 (13)	3,2 (8)	3,3 (3)	3,4 (28)	3,5 (23)	3,6 (18)
	4	4,1 (19)	4,2 (14)	4,3 (9)	4,4 (4)	4,5 (29)	4,6 (24)
	5	5,1 (25)	5,2 (20)	5,3 (15)	5,4 (10)	5,5 (5)	5,6 (30)

TABLE A6. Positional Array for Testing the Joint Occupancy of a Single Type (6, 30) Commutator in Combination with a Single Type (3, 30) Commutator

		TYPE (3, 30) PRIMARY POSITIONS									
		1	2	3	4	5	6	7	8	9	10
TYPE (6, 30) PRIMARY POSITIONS	1	1,1 (1)	1,2	1,3	1,4	1,5	1,6 (6)	1,7	1,8	1,9	1,10
	2	2,1	2,2 (2)	2,3	2,4	2,5	2,6	2,7 (7)	2,8	2,9	2,10
	3	3,1	3,2	3,3 (3)	3,4	3,5	3,6	3,7	3,8 (8)	3,9	3,10
	4	4,1	4,2	4,3	4,4 (4)	4,5	4,6	4,7	4,8	4,9 (9)	4,10
	5	5,1	5,2	5,3	5,4	5,5 (5)	5,6	5,7	5,8	5,9	5,10 (10)

TABLE A7. Positional Array for Testing the Joint Occupancy of a Single Type (6, 30) Commutator in Combination with a Single Type (2, 30) Commutator

TYPE (6, 30) PRIMARY POSITIONS	TYPE (2, 30) PRIMARY POSITIONS: 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1,1 (1)	1,2	1,3	1,4	1,5	1,6 (6)	1,7	1,8	1,9	1,10	1,11 (11)	1,12	1,13	1,14	1,15
2	2,1	2,2 (2)	2,3	2,4	2,5	2,6	2,7 (7)	2,8	2,9	2,10	2,11	2,12 (12)	2,13	2,14	2,15
3	3,1	3,2	3,3 (3)	3,4	3,5	3,6	3,7	3,8 (8)	3,9	3,10	3,11	3,12	3,13 (13)	3,14	3,15
4	4,1	4,2	4,3	4,4 (4)	4,5	4,6	4,7	4,8	4,9 (9)	4,10	4,11	4,12	4,13	4,14 (14)	4,15
5	5,1	5,2	5,3	5,4	5,5 (5)	5,6	5,7	5,8	5,9	5,10 (10)	5,11	5,12	5,13	5,14	5,15 (15)

TABLE A8. Positional Array for Testing the Joint Occupancy of a Single Type (5, 30) Commutator in Combination with a Single Type (3, 30) Commutator

		TYPE (3, 30) PRIMARY POSITIONS									
		1	2	3	4	5	6	7	8	9	10
TYPE (5, 30) PRIMARY POSITIONS	1	1,1 (1)	1,2	1,3 (13)	1,4	1,5 (25)	1,6	1,7 (7)	1,8	1,9 (19)	1,10
	2	2,1	2,2 (2)	2,3	2,4 (14)	2,5	2,6 (26)	2,7	2,8 (8)	2,9	2,10 (20)
	3	3,1 (21)	3,2	3,3 (3)	3,4	3,5 (15)	3,6	3,7 (27)	3,8	3,9 (9)	3,10
	4	4,1	4,2 (22)	4,3	4,4 (4)	4,5	4,6 (16)	4,7	4,8 (28)	4,9	4,10 (10)
	5	5,1 (11)	5,2	5,3 (23)	5,4	5,5 (5)	5,6	5,7 (17)	5,8	5,9 (29)	5,10
	6	6,1	6,2 (12)	6,3	6,4 (24)	6,5	6,6 (6)	6,7	6,8 (18)	6,9	6,10 (30)

TABLE A9. Positional Array for Testing the Joint Occupancy of a Single Type (5, 30) Commutator in Combination with a Single Type (2, 30) Commutator

TYPE (5, 30) PRIMARY POSITIONS	TYPE (2, 30) PRIMARY POSITIONS														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1,1 (1)	1,2	1,3	1,4 (19)	1,5	1,6	1,7 (7)	1,8	1,9	1,10 (25)	1,11	1,12	1,13 (13)	1,14	1,15
2	2,1	2,2 (2)	2,3	2,4	2,5 (20)	2,6	2,7	2,8 (8)	2,9	2,10	2,11 (26)	2,12	2,13	2,14 (14)	2,15
3	3,1	3,2	3,3 (3)	3,4	3,5	3,6 (21)	3,7	3,8	3,9 (9)	3,10	3,11	3,12 (27)	3,13	3,14	3,15 (15)
4	4,1 (16)	4,2	4,3	4,4 (4)	4,5	4,6	4,7 (22)	4,8	4,9	4,10 (10)	4,11	4,12	4,13 (28)	4,14	4,15
5	5,1	5,2 (17)	5,3	5,4	5,5 (5)	5,6	5,7	5,8 (23)	5,9	5,10	5,11 (11)	5,12	5,13	5,14 (29)	5,15
6	6,1	6,2	6,3 (18)	6,4	5,5	6,6 (6)	6,7	6,8	6,9 (24)	6,10	6,11	6,12 (12)	6,13	6,14	6,15 (30)

TABLE A10. Positional Array for Testing the Joint Occupancy of a Single Type (3, 30) Commutator in Combination with a Single Type (2, 30) Commutator

TYPE (3, 30) PRIMARY POSITIONS	TYPE (2, 30) PRIMARY POSITIONS														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1,1 (1)	1,2	1,3	1,4	1,5	1,6 (21)	1,7	1,8	1,9	1,10	1,11 (11)	1,12	1,13	1,14	1,15
2	2,1	2,2 (2)	2,3	2,4	2,5	2,6	2,7 (22)	2,8	2,9	2,10	2,11	2,12 (12)	2,13	2,14	2,15
3	3,1	3,2	3,3 (3)	3,4	3,5	3,6	3,7	3,8 (23)	3,9	3,10	3,11	3,12	3,13 (13)	3,14	3,15
4	4,1	4,2	4,3	4,4 (4)	4,5	4,6	4,7	4,8	4,9 (24)	4,10	4,11	4,12	4,13	4,14 (14)	4,15
5	5,1	5,2	5,3	5,4	5,5 (5)	5,6	5,7	5,8	5,9	5,10 (25)	5,11	5,12	5,13	5,14	5,15 (15)
6	6,1 (16)	6,2	6,3	6,4	6,5	6,6 (6)	6,7	6,8	6,9	6,10	6,11 (26)	6,12	6,13	6,14	6,15
7	7,1	7,2 (17)	7,3	7,4	7,5	7,6	7,7 (7)	7,8	7,9	7,10	7,11	7,12 (27)	7,13	7,14	7,15
8	8,1	8,2	8,3 (18)	8,4	8,5	8,6	8,7	8,8 (8)	8,9	8,10	8,11	8,12	8,13 (28)	8,14	8,15
9	9,1	9,2	9,3	9,4 (19)	9,5	9,6	9,7	9,8	9,9 (9)	9,10	9,11	9,12	9,13	9,14 (29)	9,15
10	10,1	10,2	10,3	10,4	10,5 (20)	10,6	10,7	10,8	10,9	10,10 (10)	10,11	10,12	10,13	10,14	10,15 (30)

APPENDIX B

Summary of Feasible Strapping Arrangement Programs for the 30 Channel Multi-Mode PAM Commutator System

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
1	120	30-30	1, 2, ..., 30
2	60	15-30	1, 3, ..., 29 (odd integers only)
	60	15-30	2, 4, ..., 30 (even integers only)
3	60	15-30	1, 3, ..., 29 (odd integers only)
	20	5-30	2, 8, 14, 20, 26
	20	5-30	4, 10, 16, 22, 28
	20	5-30	6, 12, 18, 24, 30
4	60	15-30	1, 3, ..., 29 (odd integers only)
	20	5-30	2, 8, 14, 20, 26
	20	5-30	4, 10, 16, 22, 28
	4	1-30	6
	4	1-30	12
	4	1-30	18
	4	1-30	24
	4	1-30	30
5	60	15-30	1, 3, ..., 29 (odd integers only)
	20	5-30	2, 8, 14, 20, 26
	4	1-30	4
	4	1-30	6
	4	1-30	10
	4	1-30	12
	4	1-30	16
	4	1-30	18
	4	1-30	22
	4	1-30	24
	4	1-30	28
	4	1-30	30
6	60	15-30	1, 3, ..., 29 (odd integers only)
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	12	3-30	8, 18, 28
	12	3-30	10, 20, 30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
7	60	15-30	1, 3, ..., 29 (odd integers only)
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	12	3-30	8, 18, 28
	4	1-30	10
	4	1-30	20
	4	1-30	30
8	60	15-30	1, 3, ... 29 (odd integers only)
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	4	1-30	8
	4	1-30	10
	4	1-30	18
	4	1-30	20
	4	1-30	28
	4	1-30	30
9	60	15-30	1, 3, ..., 29 (odd integers only)
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	4	1-30	6
	4	1-30	8
	4	1-30	10
	4	1-30	16
	4	1-30	18
	4	1-30	20
	4	1-30	26
	4	1-30	28
	4	1-30	30
10	60	15-30	1, 3, ..., 29 (odd integers only)
	12	3-30	2, 12, 22
	4	1-30	4
	4	1-30	6
	4	1-30	8
	4	1-30	10
	4	1-30	14
	4	1-30	16
	4	1-30	18
	4	1-30	20
	4	1-30	24
	4	1-30	26
	4	1-30	28
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
11	60	15-30	1, 3, ..., 29 (odd integers only)
	4	1-30	2
	4	1-30	4
	4	1-30	6
	4	1-30	8
	4	1-30	10
	4	1-30	12
	4	1-30	14
	4	1-30	16
	4	1-30	18
	4	1-30	20
	4	1-30	22
	4	1-30	24
	4	1-30	26
	4	1-30	28
12	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	40	10-30	2, 5, 8, 11, 14, 17, 20, 23, 26, 29
	40	10-30	3, 6, 9, 12, 15, 18, 21, 24, 27, 30
13	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	40	10-30	2, 5, 8, 11, 14, 17, 20, 23, 26, 29
	20	5-30	3, 9, 15, 21, 27
	20	5-30	6, 12, 18, 24, 30
14	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	40	10-30	2, 5, 8, 11, 14, 17, 20, 23, 26, 29
	20	5-30	3, 9, 15, 21, 27
	4	1-30	6
	4	1-30	12
	4	1-30	18
	4	1-30	24
	4	1-30	30
15	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	40	10-30	2, 5, 8, 11, 14, 17, 20, 23, 26, 29
	8	2-30	3, 18
	8	2-30	6, 21
	8	2-30	9, 24
	8	2-30	12, 27
	8	2-30	15, 30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
16	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	40	10-30	2, 5, 8, 11, 14, 17, 20, 23, 26, 29
	8	2-30	3, 18
	8	2-30	6, 21
	8	2-30	9, 24
	8	2-30	12, 27
	4	1-30	15
	4	1-30	30
17	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	40	10-30	2, 5, 8, 11, 14, 17, 20, 23, 26, 29
	8	2-30	3, 18
	8	2-30	6, 21
	8	2-30	9, 24
	4	1-30	12
	4	1-30	15
	4	1-30	27
	4	1-30	30
18	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	40	10-30	2, 5, 8, 11, 14, 17, 20, 23, 26, 29
	8	2-30	3, 18
	8	2-30	6, 21
	4	1-30	9
	4	1-30	12
	4	1-30	15
	4	1-30	24
	4	1-30	27
	4	1-30	30
19	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	40	10-30	2, 5, 8, 11, 14, 17, 20, 23, 26, 29
	8	2-30	3, 18
	4	1-30	6
	4	1-30	9
	4	1-30	12
	4	1-30	15
	4	1-30	21
	4	1-30	24
	4	1-30	27
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
20	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	40	10-30	2, 5, 8, 11, 14, 17, 20, 23, 26, 29
	4	1-30	3
	4	1-30	6
	4	1-30	9
	4	1-30	12
	4	1-30	15
	4	1-30	18
	4	1-30	21
	4	1-30	24
	4	1-30	27
	4	1-30	30
21	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	3, 9, 15, 21, 27
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	20	5-30	6, 12, 18, 24, 30
22	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	3, 9, 15, 21, 27
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	4	1-30	6
	4	1-30	12
	4	1-30	18
	4	1-30	24
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
23	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	8	2-30	3, 18
	8	2-30	6,21
	8	2-30	9,24
	8	2-30	12, 27
	8	2-30	15,30
24	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	8	2-30	3,18
	8	2-30	6,21
	8	2-30	9,24
	8	2-30	12,27
	4	1-30	15
	4	1-30	30
25	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	8	2-30	3, 18
	8	2-30	6,21
	8	2-30	9,24
	4	1-30	12
	4	1-30	15
	4	1-30	27
	4	1-30	30
26	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	8	2-30	3,18
	8	2-30	6,21
	4	1-30	9
	4	1-30	12
	4	1-30	15
	4	1-30	24
	4	1-30	27
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
27	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	8	2-30	3, 18
	4	1-30	6
	4	1-30	9
	4	1-30	12
	4	1-30	15
	4	1-30	21
	4	1-30	24
	4	1-30	27
	4	1-30	30
28	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	4	1-30	3
	4	1-30	6
	4	1-30	9
	4	1-30	12
	4	1-30	15
	4	1-30	18
	4	1-30	21
	4	1-30	24
	4	1-30	27
	4	1-30	30
29	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	8	2-30	3, 18
	8	2-30	6, 21
	8	2-30	9, 24
	8	2-30	12, 27
	8	2-30	15, 30
	4	1-30	5
	4	1-30	11
	4	1-30	17
	4	1-30	23
	4	1-30	29

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
30	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	8	2-30	3, 18
	8	2-30	6, 21
	8	2-30	9, 25
	8	2-30	12, 27
	4	1-30	5
	4	1-30	11
	4	1-30	15
	4	1-30	17
	4	1-30	23
	4	1-30	29
	4	1-30	30
31	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	8	2-30	3, 18
	8	2-30	6, 21
	8	2-30	9, 25
	4	1-30	5
	4	1-30	11
	4	1-30	12
	4	1-30	15
	4	1-30	17
	4	1-30	23
	4	1-30	27
	4	1-30	29
	4	1-30	30
32	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	8	2-30	3, 18
	8	2-30	6, 21
	4	1-30	5
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	15
	4	1-30	17
	4	1-30	23
	4	1-30	24
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
33	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	8	2-30	3, 18
	4	1-30	5
	4	1-30	6
	4	1-30	9
	4	1-30	11
	4	1-30	15
	4	1-30	17
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	27
	4	1-30	29
	4	1-30	30
	4	1-30	12
34	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	20	5-30	2, 8, 14, 20, 26
	4	1-30	3
	4	1-30	5
	4	1-30	6
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	15
	4	1-30	17
	4	1-30	18
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
35	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	12, 27
	8	2-30	14, 29
	8	2-30	15, 30
36	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	12, 27
	8	2-30	14, 29
	4	1-30	15
	4	1-30	30
37	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	12, 27
	4	1-30	14
	4	1-30	15
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
38	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	27
	4	1-30	29
	4	1-30	30
39	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30
40	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
41	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	4	1-30	8
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30
42	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
43	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	8	2-30	2, 17
	8	2-30	3, 18
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30
44	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	8	2-30	2, 17
	4	1-30	3
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
45	40	10-30	1, 4, 7, 10, 13, 16, 19, 22, 25, 28
	4	1-30	2
	4	1-30	3
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	18
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30
46	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	24	6-30	4, 9, 14, 19, 24, 29
	24	6-30	5, 10, 15, 20, 25, 30
47	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	24	6-30	4, 9, 14, 19, 24, 29
	12	3-30	5, 15, 25
	12	3-30	10, 20, 30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
48	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	4, 9, 14, 19, 24, 29
	24	6-30	5, 10, 15, 20, 25, 30
	12	3-30	3, 13, 23
	4	1-30	8
	4	1-30	18
	4	1-30	28
49	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
50	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	12	3-30	4, 14, 24
	12	3-30	9, 19, 29
	12	3-30	5, 15, 25
	4	1-30	10
	4	1-30	20
	4	1-30	30
51	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	24	6-30	4, 9, 14, 19, 24, 29
	12	3-30	5, 15, 25
	12	3-30	10, 20, 30
	8	2-30	1, 16
	8	2-30	6, 21
	8	2-30	11, 26
52	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	24	6-30	4, 9, 14, 19, 24, 29
	12	3-30	5, 15, 25
	12	3-30	10, 20, 30
	8	2-30	1, 16
	8	2-30	6, 21
	4	1-30	11
	4	1-30	26

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
53	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	12	3-30	4, 14, 24
	12	3-30	9, 19, 29
	8	2-30	5, 20
	4	1-30	10
	4	1-30	15
	4	1-30	25
	4	1-30	30
54	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	12	3-30	4, 14, 24
	12	3-30	9, 19, 29
	4	1-30	5
	4	1-30	10
	4	1-30	15
	4	1-30	20
	4	1-30	25
	4	1-30	30
55	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	12	3-30	4, 14, 24
	8	2-30	5, 20
	8	2-30	10, 25
	8	2-30	15, 30
	4	1-30	9
	4	1-30	19
	4	1-30	29
56	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	12	3-30	4, 14, 24
	8	2-30	5, 20
	8	2-30	10, 25
	4	1-30	9
	4	1-30	15
	4	1-30	19
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
57	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	24	6-30	3, 8, 13, 18, 23, 28
	12	3-30	4, 14, 24
	8	2-30	5, 20
	4	1-30	9
	4	1-30	10
	4	1-30	15
	4	1-30	19
	4	1-30	25
	4	1-30	29
	4	1-30	30
58	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
59	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	4	1-30	10
	4	1-30	20
	4	1-30	30
60	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	8	2-30	5,20
	8	2-30	10, 25
	8	2-30	15, 30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
61	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	8	2-30	5, 20
	8	2-30	10, 25
	4	1-30	15
	4	1-30	30
62	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	8	2-30	5, 20
	4	1-30	10
	4	1-30	15
	4	1-30	25
	4	1-30	30
63	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	4	1-30	9
	4	1-30	10
	4	1-30	19
	4	1-30	20
	4	1-30	29
	4	1-30	30
64	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	4	1-30	10
	4	1-30	20
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
65	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	12	3-30	5, 15, 25
	8	2-30	4, 19
	8	2-30	9, 24
	4	1-30	10
	4	1-30	14
	4	1-30	20
	4	1-30	29
	4	1-30	30
66	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	12	3-30	4, 14, 24
	8	2-30	5, 20
	4	1-30	9
	4	1-30	10
	4	1-30	15
	4	1-30	19
	4	1-30	25
	4	1-30	29
	4	1-30	30
67	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
68	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	4, 19
	8	2-30	9, 24
	8	2-30	14, 29
	8	2-30	5, 20
	8	2-30	10, 25
	8	2-30	15, 30
69	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	4, 19
	8	2-30	9, 24
	8	2-30	14, 29
	8	2-30	5, 20
	8	2-30	10, 25
	4	1-30	15
	4	1-30	30
70	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17 22, 27
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	4, 19
	8	2-30	9, 24
	8	2-30	14, 29
	8	2-30	5, 20
	4	1-30	10
	4	1-30	15
	4	1-30	25
	4	1-30	30
71	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	4, 19
	8	2-30	9, 24
	8	2-30	14, 29
	4	1-30	5
	4	1-30	10
	4	1-30	15
	4	1-30	20
	4	1-30	25
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
72	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	4, 19
	8	2-30	9, 24
	4	1-30	5
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	20
	4	1-30	25
	4	1-30	29
	4	1-30	30
73	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	4, 19
	4	1-30	5
	4	1-30	9
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	20
	4	1-30	24
	4	1-30	25
	4	1-30	29
	4	1-30	30
74	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	4	1-30	4
	4	1-30	5
	4	1-30	9
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	19
	4	1-30	20
	4	1-30	24
	4	1-30	25
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
75	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	14, 29
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	15, 30
	4	1-30	8
	4	1-30	18
	4	1-30	28
76	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	14, 29
	4	1-30	8
	4	1-30	15
	4	1-30	18
	4	1-30	28
	4	1-30	30
77	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	9, 24
	8	2-30	10, 25
	4	1-30	8
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
78	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	9, 24
	4	1-30	8
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	25
	4	1-30	28
	4	1-30	29
	4	1-30	30
79	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	8	2-30	4, 19
	8	2-30	5, 20
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	24
	4	1-30	25
	4	1-30	28
	4	1-30	29
	4	1-30	30
80	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	8	2-30	4, 19
	4	1-30	5
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	20
	4	1-30	24
	4	1-30	25
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
81	24	6-30	1, 6, 11, 16, 21, 26
	24	6-30	2, 7, 12, 17, 22, 27
	12	3-30	3, 13, 23
	4	1-30	4
	4	1-30	5
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	24
	4	1-30	25
	4	1-30	28
	4	1-30	29
	4	1-30	30
82	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	7, 17, 27
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	12	3-30	2, 12, 22
83	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	7, 17, 27
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	4	1-30	10
	4	1-30	20
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
84	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	8, 18, 28
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	2, 17
	8	2-30	7, 22
	8	2-30	12, 27
85	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	8, 18, 28
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	2, 17
	8	2-30	7, 22
	4	1-30	12
	4	1-30	27
86	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	8, 18, 28
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	2, 17
	4	1-30	7
	4	1-30	12
	4	1-30	22
	4	1-30	27

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
87	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	7, 17, 27
	12	3-30	8, 18, 28
	4	1-30	9
	4	1-30	10
	4	1-30	19
	4	1-30	20
	4	1-30	29
	4	1-30	30
88	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	8	2-30	2, 17
	8	2-30	7, 22
	8	2-30	12, 27
	4	1-30	10
	4	1-30	20
	4	1-30	30
89	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	7, 17, 27
	12	3-30	8, 18, 28
	8	2-30	5, 20
	8	2-30	10, 25
	4	1-30	9
	4	1-30	15
	4	1-30	19
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
90	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	12	3-30	8, 18, 28
	8	2-30	2, 17
	4	1-30	7
	4	1-30	10
	4	1-30	12
	4	1-30	19
	4	1-30	21
	4	1-30	27
	4	1-30	30
91	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	7, 17, 27
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	28
	4	1-30	29
	4	1-30	30
92	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	8	2-30	2, 17
	8	2-30	7, 22
	8	2-30	12, 27
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
93	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	12, 27
	4	1-30	13
	4	1-30	28
94	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	2
	8	2-30	3
	8	2-30	7
	8	2-30	12
	4	1-30	8
	4	1-30	13
	4	1-30	23
	4	1-30	28
95	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	8	2-30	2, 17
	8	2-30	7, 22
	8	2-30	12, 27
	4	1-30	9
	4	1-30	10
	4	1-30	19
	4	1-30	20
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
96	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	8	2-30	2, 17
	8	2-30	7, 22
	4	1-30	12
	4	1-30	27
	4	1-30	9
	4	1-30	10
	4	1-30	19
	4	1-30	20
	4	1-30	29
	4	1-30	30
97	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	8	2-30	2, 17
	4	1-30	7
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	27
	4	1-30	29
	4	1-30	30
98	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
99	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	12	3-30	3, 13, 23
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	14, 29
	8	2-30	15, 30
	4	1-30	18
	4	1-30	8
	4	1-30	28
100	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	8	2-30	2, 17
	8	2-30	7, 22
	8	2-30	12, 27
	8	2-30	3, 18
	8	2-30	8, 23
	4	1-30	13
	4	1-30	28
	4	1-30	10
	4	1-30	20
	4	1-30	30
101	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	8	2-30	2, 17
	8	2-30	7, 22
	8	2-30	12, 27
	8	2-30	3, 18
	4	1-30	8
	4	1-30	10
	4	1-30	13
	4	1-30	20
	4	1-30	23
	4	1-30	28
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
102	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	8	2-30	2, 17
	8	2-30	7, 22
	8	2-30	12, 27
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	28
	4	1-30	29
	4	1-30	30
103	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	8	2-30	5-20
	8	2-30	10, 25
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	15
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
104	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	8	2-30	5, 20
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	15
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
105	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	12	3-30	3, 13, 23
	4	1-30	4
	4	1-30	5
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	24
	4	1-30	25
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
106	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	4, 19
	8	2-30	9, 25
	8	2-30	14, 29
	8	2-30	5, 20
	8	2-30	10, 25
	8	2-30	15, 30
107	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	4, 19
	8	2-30	9, 24
	8	2-30	14, 29
	8	2-30	5, 20
	8	2-30	10, 25
	4	1-30	15
	4	1-30	30
108	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	4, 15
	8	2-30	9, 24
	8	2-30	14, 29
	8	2-30	5, 20
	4	1-30	10
	4	1-30	15
	4	1-30	25
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
109	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	4, 19
	8	2-30	9, 24
	8	2-30	14, 29
	4	1-30	5
	4	1-30	10
	4	1-30	15
	4	1-30	20
	4	1-30	25
	4	1-30	30
110	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	4, 19
	8	2-30	9, 24
	4	1-30	14
	4	1-30	29
	4	1-30	5
	4	1-30	10
	4	1-30	15
	4	1-30	20
	4	1-30	25
	4	1-30	30
111	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	4, 19
	4	1-30	9
	4	1-30	14
	4	1-30	24
	4	1-30	29
	4	1-30	5
	4	1-30	10
	4	1-30	15
	4	1-30	20
	4	1-30	25
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
112	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	4	1-30	4
	4	1-30	5
	4	1-30	9
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	19
	4	1-30	20
	4	1-30	24
	4	1-30	25
	4	1-30	29
	4	1-30	30
113	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	8	2-30	3, 18
	8	2-30	8, 23
	4	1-30	13
	4	1-30	28
	4	1-30	4
	4	1-30	5
	4	1-30	9
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	19
	4	1-30	20
	4	1-30	24
	4	1-30	25
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
114	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	8	2-30	3, 18
	4	1-30	8
	4	1-30	13
	4	1-30	23
	4	1-30	28
	4	1-30	4
	4	1-30	5
	4	1-30	9
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	19
	4	1-30	20
	4	1-30	24
	4	1-30	25
	4	1-30	29
	4	1-30	30
115	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	12	3-30	7, 17, 27
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
116	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	13, 28
	8	2-30	14, 29
	8	2-30	15, 30
	4	1-30	17
	4	1-30	7
	4	1-30	27
117	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	4, 19
	8	2-30	9, 24
	8	2-30	14, 29
	8	2-30	5, 20
	8	2-30	10, 25
	4	1-30	7
	4	1-30	17
	4	1-30	27
	4	1-30	15
	4	1-30	30
118	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	4, 19
	8	2-30	9, 24
	8	2-30	14, 29
	8	2-30	10, 25
	4	1-30	7
	4	1-30	17
	4	1-30	27
	4	1-30	5
	4	1-30	20
	4	1-30	15
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
119	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	4, 19
	8	2-30	9, 24
	8	2-30	14, 28
	4	1-30	7
	4	1-30	17
	4	1-30	27
	4	1-30	5
	4	1-30	10
	4	1-30	15
	4	1-30	20
	4	1-30	25
	4	1-30	30
120	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	4, 19
	8	2-30	5, 20
	4	1-30	7
	4	1-30	17
	4	1-30	27
	4	1-30	29
	4	1-30	30
	4	1-30	9
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	19
	4	1-30	20

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
121	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	8, 23
	4	1-30	7
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
122	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
123	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	20
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
124	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	19
	4	1-30	20
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
125	24	6-30	1, 6, 11, 16, 21, 26
	12	3-30	2, 12, 22
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
126	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	8	2-30	13, 28
	8	2-30	14, 29
	8	2-30	15, 30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
127	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	8	2-30	13, 28
	8	2-30	14, 29
	4	1-30	15
	4	1-30	30
128	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	8	2-30	13, 28
	4	1-30	14
	4	1-30	15
	4	1-30	29
	4	1-30	30
129	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
130	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
131	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
132	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
133	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
134	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
135	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
136	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	8	2-30	3, 18
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
137	24	6-30	1, 6, 11, 16, 21, 26
	8	2-30	2, 17
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
138	24	6-30	1, 6, 11, 16, 21, 26
	4	1-30	2
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
139	20	5-30	1, 7, 13, 19, 25
	20	5-30	2, 8, 14, 20, 26
	20	5-30	3, 9, 15, 21, 27
	20	5-30	4, 10, 16, 22, 28
	20	5-30	5, 11, 17, 23, 29
	20	5-30	6, 12, 18, 24, 30
140	20	5-30	1, 7, 13, 19, 25
	20	5-30	2, 8, 14, 20, 26
	20	5-30	3, 9, 15, 21, 27
	20	5-30	4, 10, 16, 22, 28
	20	5-30	5, 11, 17, 23, 29
	4	1-30	6
	4	1-30	12
	4	1-30	18
	4	1-30	24
	4	1-30	30
141	20	5-30	2, 8, 14, 20, 26
	20	5-30	3, 9, 15, 21, 27
	20	5-30	5, 11, 17, 23, 29
	20	5-30	6, 12, 18, 24, 30
	8	2-30	1, 16
	8	2-30	7, 22
	8	2-30	13, 28
	8	2-30	4, 19
	8	2-30	10, 25
142	20	5-30	2, 8, 14, 20, 26
	20	5-30	3, 9, 15, 21, 27
	20	5-30	5, 11, 17, 23, 29
	20	5-30	6, 12, 18, 24, 30
	8	2-30	1, 16
	8	2-30	7, 22
	8	2-30	13, 28
	8	2-30	4, 19
	4	1-30	25
	4	1-30	10

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
143	20	5-30	2, 8, 14, 20, 26
	20	5-30	3, 9, 15, 21, 27
	20	5-30	5, 11, 17, 23, 29
	20	5-30	6, 12, 18, 24, 30
	8	2-30	1, 16
	8	2-30	7, 22
	8	2-30	13, 28
	4	1-30	4
	4	1-30	10
	4	1-30	19
	4	1-30	25
144	20	5-30	2, 8, 14, 20, 26
	20	5-30	3, 9, 15, 21, 27
	20	5-30	5, 11, 17, 23, 29
	20	5-30	6, 12, 18, 24, 30
	8	2-30	1, 16
	8	2-30	7, 22
	4	1-30	4
	4	1-30	10
	4	1-30	13
	4	1-30	19
	4	1-30	25
	4	1-30	28
145	20	5-30	2, 8, 14, 20, 26
	20	5-30	3, 9, 15, 21, 27
	20	5-30	5, 11, 17, 23, 29
	20	5-30	6, 12, 18, 24, 30
	8	2-30	1, 16
	4	1-30	4
	4	1-30	7
	4	1-30	10
	4	1-30	13
	4	1-30	19
	4	1-30	22
	4	1-30	25
	4	1-30	28

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
146	20	5-30	2, 8, 14, 20, 26
	20	5-30	3, 9, 15, 21, 27
	20	5-30	5, 11, 17, 23, 29
	20	5-30	6, 12, 18, 24, 30
	4	1-30	1
	4	1-30	4
	4	1-30	7
	4	1-30	10
	4	1-30	13
	4	1-30	16
	4	1-30	19
	4	1-30	22
	4	1-30	25
	4	1-30	28
147	20	5-30	2, 8, 14, 20, 26
	20	5-30	4, 10, 16, 22, 28
	20	5-30	6, 12, 18, 24, 30
	12	3-30	1, 11, 21
	12	3-30	3, 13, 23
	12	3-30	5, 15, 25
	12	3-30	7, 17, 27
	12	3-30	9, 19, 29
148	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	20	5-30	5, 11, 17, 23, 29
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	12	3-30	8, 18, 28
	4	1-30	10
	4	1-30	20
	4	1-30	30
149	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	20	5-30	5, 11, 17, 23, 29
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	4	1-30	8
	4	1-30	10
	4	1-30	18
	4	1-30	20
	4	1-30	28
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
150	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	20	5-30	5, 11, 17, 23, 29
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	4	1-30	6
	4	1-30	8
	4	1-30	10
	4	1-30	16
	4	1-30	18
	4	1-30	20
	4	1-30	26
	4	1-30	28
	4	1-30	30
151	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	20	5-30	5, 11, 17, 23, 29
	12	3-30	2, 12, 22
	4	1-30	4
	4	1-30	6
	4	1-30	8
	4	1-30	10
	4	1-30	14
	4	1-30	16
	4	1-30	18
	4	1-30	20
	4	1-30	24
	4	1-30	26
	4	1-30	28
	4	1-30	30
152	20	5-30	1, 7, 13, 19, 25
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	8	2-30	3, 18
	8	2-30	6, 21
	8	2-30	9, 24
	8	2-30	12, 27
	8	2-30	15, 30
	4	1-30	4
	4	1-30	10
	4	1-30	16
	4	1-30	22
	4	1-30	28

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
153	20	5-30	1, 7, 13, 19, 25
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	8	2-30	3, 18
	8	2-30	6, 21
	8	2-30	9, 24
	8	2-30	12, 27
	4	1-30	4
	4	1-30	10
	4	1-30	15
	4	1-30	16
	4	1-30	22
	4	1-30	28
	4	1-30	30
154	20	5-30	1, 7, 13, 19, 25
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	8	2-30	3, 18
	8	2-30	6, 21
	8	2-30	9, 24
	4	1-30	4
	4	1-30	10
	4	1-30	12
	4	1-30	15
	4	1-30	16
	4	1-30	22
	4	1-30	27
	4	1-30	28
	4	1-30	30
155	20	5-30	1, 7, 13, 19, 25
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	8	2-30	3, 18
	8	2-30	6, 21
	4	1-30	4
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	15
	4	1-30	16
	4	1-30	22
	4	1-30	24
	4	1-30	27
	4	1-30	28
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
156	20	5-30	1, 7, 13, 19, 25
	20	5-30	2, 8, 14, 20, 26
	20	5-30	5, 11, 17, 23, 29
	8	2-30	3, 18
	4	1-30	4
	4	1-30	6
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	15
	4	1-30	16
	4	1-30	21
	4	1-30	22
	4	1-30	24
	4	1-30	27
	4	1-30	28
	4	1-30	30
157	20	5-30	1, 7, 13, 19, 25
	20	5-30	2, 8, 14, 20, 26
	20	5-30	3, 9, 15, 21, 27
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
158	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	12	3-30	8, 18, 28
	12	3-30	10, 20, 30
	4	1-30	5
	4	1-30	11
	4	1-30	17
	4	1-30	23
	4	1-30	29
159	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	12	3-30	8, 18, 28
	8	2-30	5, 20
	4	1-30	10
	4	1-30	11
	4	1-30	17
	4	1-30	23
	4	1-30	29
	4	1-30	30
160	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	12	3-30	8, 18, 28
	4	1-30	5
	4	1-30	10
	4	1-30	11
	4	1-30	17
	4	1-30	20
	4	1-30	23
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
161	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	8	2-30	5, 20
	8	2-30	8, 23
	4	1-30	10
	4	1-30	11
	4	1-30	17
	4	1-30	18
	4	1-30	28
	4	1-30	29
	4	1-30	30
162	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	8	2-30	5, 20
	4	1-30	8
	4	1-30	10
	4	1-30	11
	4	1-30	17
	4	1-30	18
	4	1-30	23
	4	1-30	28
	4	1-30	29
	4	1-30	30
163	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	4	1-30	5
	4	1-30	8
	4	1-30	10
	4	1-30	11
	4	1-30	17
	4	1-30	18
	4	1-30	20
	4	1-30	23
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
164	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	8	2-30	5, 20
	8	2-30	8, 23
	8	2-30	11, 26
	4	1-30	6
	4	1-30	10
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	28
	4	1-30	29
	4	1-30	30
165	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	8	2-30	5, 20
	8	2-30	8, 23
	4	1-30	6
	4	1-30	10
	4	1-30	11
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	26
	4	1-30	28
	4	1-30	29
	4	1-30	30
166	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	8	2-30	5, 20
	4	1-30	6
	4	1-30	8
	4	1-30	10
	4	1-30	11
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	23
	4	1-30	26
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
167	20	5-30	1, 7, 13, 19, 25
	20	5-30	3, 9, 15, 21, 27
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	10
	4	1-30	11
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	20
	4	1-30	23
	4	1-30	26
	4	1-30	28
	4	1-30	29
	4	1-30	30
168	20	5-30	6, 12, 18, 24, 30
	20	5-30	4, 10, 16, 22, 28
	12	3-30	9, 19, 29
	8	2-30	2, 17
	8	2-30	5, 20
	8	2-30	8, 23
	8	2-30	11, 26
	4	1-30	1
	4	1-30	3
	4	1-30	7
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	21
	4	1-30	25
	4	1-30	27

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
169	20	5-30	6, 12, 18, 24, 30
	20	5-30	4, 10, 16, 22, 28
	12	3-30	9, 19, 29
	8	2-30	2, 17
	8	2-30	5, 20
	8	2-30	8, 23
	4	1-30	1
	4	1-30	3
	4	1-30	7
	4	1-30	11
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	21
	4	1-30	25
	4	1-30	26
	4	1-30	27
170	20	5-30	6, 12, 18, 24, 30
	20	5-30	4, 10, 16, 22, 28
	12	3-30	9, 19, 29
	8	2-30	2, 17
	8	2-30	5, 20
	4	1-30	1
	4	1-30	3
	4	1-30	7
	4	1-30	8
	4	1-30	11
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	21
	4	1-30	23
	4	1-30	25
	4	1-30	26
	4	1-30	27

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
171	20	5-30	6, 12, 18, 24, 30
	20	5-30	4, 10, 16, 22, 28
	12	3-30	9, 19, 29
	8	2-30	2, 17
	4	1-30	1
	4	1-30	3
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	11
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	25
	4	1-30	26
	4	1-30	27
172	20	5-30	6, 12, 18, 24, 30
	20	5-30	4, 10, 16, 22, 28
	12	3-30	9, 19, 29
	4	1-30	1
	4	1-30	2
	4	1-30	3
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	11
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	25
	4	1-30	26
	4	1-30	27

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
173	20	5-30	1, 7, 13, 19, 25
	20	5-30	4, 10, 16, 22, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	12, 27
	8	2-30	14, 29
	8	2-30	15, 30
174	20	5-30	1, 7, 13, 19, 25
	20	5-30	4, 10, 16, 22, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	12, 27
	8	2-30	14, 29
	4	1-30	15
	4	1-30	30
175	20	5-30	1, 7, 13, 19, 25
	20	5-30	4, 10, 16, 22, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	12, 27
	4	1-30	14
	4	1-30	15
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
176	20	5-30	1, 7, 13, 19, 25
	20	5-30	4, 10, 16, 22, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	27
	4	1-30	29
	4	1-30	30
177	20	5-30	1, 7, 13, 19, 25
	20	5-30	4, 10, 16, 22, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30
178	20	5-30	1, 7, 13, 19, 25
	20	5-30	4, 10, 16, 22, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
179	20	5-30	1, 7, 13, 19, 25
	20	5-30	4, 10, 16, 22, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	4	1-30	8
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30
180	20	5-30	1, 7, 13, 19, 25
	20	5-30	4, 10, 16, 22, 28
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
181	20	5-30	1, 7, 13, 19, 25
	20	5-30	4, 10, 16, 22, 28
	8	2-30	2, 17
	8	2-30	3, 18
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30
182	20	5-30	1, 7, 13, 19, 25
	20	5-30	4, 10, 16, 22, 28
	8	2-30	2, 17
	4	1-30	3
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
183	20	5-30	1, 7, 13, 19, 25
	20	5-30	2, 8, 14, 20, 26
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
184	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	12	3-30	8, 18, 28
	12	3-30	10, 20, 30
	4	1-30	3
	4	1-30	5
	4	1-30	9
	4	1-30	11
	4	1-30	15
	4	1-30	17
	4	1-30	21
	4	1-30	23
	4	1-30	27
	4	1-30	29

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
185	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	12	3-30	8, 18, 28
	8	2-30	5, 20
	8	2-30	15, 30
	4	1-30	3
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	17
	4	1-30	21
	4	1-30	23
	4	1-30	27
	4	1-30	29
186	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	12	3-30	8, 18, 28
	8	2-30	5, 20
	4	1-30	3
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	17
	4	1-30	21
	4	1-30	23
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
187	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	12	3-30	8, 18, 28
	4	1-30	3
	4	1-30	5
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	17
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	27
	4	1-30	29
	4	1-30	30
188	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	8, 23
	8	2-30	15, 30
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	17
	4	1-30	21
	4	1-30	27
	4	1-30	28
	4	1-30	29

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
189	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	8	2-30	3, 18
	8	2-30	5, 20
	8	1-30	8, 23
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	17
	4	1-30	21
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
190	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	8	2-30	3, 18
	8	2-30	5, 20
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	17
	4	1-30	21
	4	1-30	23
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
191	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	8	2-30	3, 18
	4	1-30	5
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	17
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
192	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	12	3-30	6, 16, 26
	4	1-30	3
	4	1-30	5
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	17
	4	1-30	18
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
193	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	11, 26
	8	2-30	15, 30
	4	1-30	9
	4	1-30	10
	4	1-30	16
	4	1-30	17
	4	1-30	27
	4	1-30	28
	4	1-30	29
194	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	11, 26
	4	1-30	9
	4	1-30	10
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
195	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
196	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	23
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
197	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	8	2-30	3, 18
	8	2-30	5, 20
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	21
	4	1-30	23
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
198	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	8	2-30	3, 18
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
199	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	12	3-30	4, 14, 24
	4	1-30	3
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
200	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	14, 29
	8	2-30	15, 30
	4	1-30	4
	4	1-30	10
	4	1-30	16
	4	1-30	17
	4	1-30	27
	4	1-30	28

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
201	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	14, 29
	4	1-30	4
	4	1-30	10
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	27
	4	1-30	28
	4	1-30	30
202	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	4	1-30	4
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
203	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	4	1-30	4
	4	1-30	10
	4	1-30	11
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
204	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	4	1-30	4
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
205	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	4	1-30	4
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
206	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	5, 20
	4	1-30	4
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
207	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	8	2-30	3, 18
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
208	20	5-30	1, 7, 13, 19, 25
	12	3-30	2, 12, 22
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	20
	4	1-30	21
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
209	20	5-30	1, 7, 13, 19, 25
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	12, 27
	8	2-30	14, 29
	8	2-30	15, 30
	4	1-30	4
	4	1-30	10
	4	1-30	16
	4	1-30	22
	4	1-30	28
210	20	5-30	1, 7, 13, 19, 25
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	12, 27
	8	2-30	14, 29
	4	1-30	4
	4	1-30	10
	4	1-30	15
	4	1-30	16
	4	1-30	22
	4	1-30	28
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
211	20	5-30	1, 7, 13, 19, 25
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	8	2-30	12, 27
	4	1-30	4
	4	1-30	10
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	22
	4	1-30	28
	4	1-30	29
	4	1-30	30
212	20	5-30	1, 7, 13, 19, 25
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	11, 26
	4	1-30	4
	4	1-30	10
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	22
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
213	20	5-30	1, 7, 13, 19, 25
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	8	2-30	9, 24
	4	1-30	4
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	22
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
214	20	5-30	1, 7, 13, 19, 25
	8	2-30	2, 12
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	8, 23
	4	1-30	4
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	22
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
215	20	5-30	1, 7, 13, 19, 25
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	8	2-30	6, 21
	4	1-30	4
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
216	20	5-30	1, 7, 13, 19, 25
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	5, 20
	4	1-30	4
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
217	20	5-30	1, 7, 13, 19, 25
	8	2-30	2, 17
	8	2-30	3, 18
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	20
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
218	20	5-30	1, 7, 13, 19, 25
	8	2-30	2, 17
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	18
	4	1-30	20
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
219	20	5-30	1, 7, 13, 19, 25
	4	1-30	2
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	20
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
220	12	3-30	1, 11, 21
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	6, 16, 26
	12	3-30	7, 17, 27
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
221	12	3-30	1, 11, 21
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	6, 16, 26
	12	3-30	7, 17, 27
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	4	1-30	10
	4	1-30	20
	4	1-30	30
222	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	7, 17, 27
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	1, 16
	8	2-30	6, 21
	8	2-30	11, 26
223	12	3-30	9, 19, 29
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	10, 20, 30
	12	3-30	7, 17, 27
	12	3-30	8, 18, 28
	8	2-30	1, 16
	8	2-30	6, 21
	4	1-30	11
	4	1-30	26
224	12	3-30	1, 11, 21
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	10, 20, 30
	12	3-30	5, 15, 25
	12	3-30	6, 16, 26
	12	3-30	7, 17, 27
	12	3-30	8, 18, 28
	8	2-30	9, 24
	4	1-30	4
	4	1-30	14
	4	1-30	19
	4	1-30	29

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
225	12	3-30	1, 11, 21
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	6, 16, 26
	12	3-30	7, 17, 27
	12	3-30	8, 18, 28
	4	1-30	9
	4	1-30	10
	4	1-30	19
	4	1-30	20
	4	1-30	29
	4	1-30	30
226	12	3-30	1, 11, 21
	12	3-30	2, 12, 22
	12	3-30	10, 20, 30
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	6, 16, 26
	12	3-30	7, 17, 27
	8	2-30	8, 23
	8	2-30	13, 28
	8	2-30	3, 18
	4	1-30	9
	4	1-30	19
	4	1-30	29
227	12	3-30	8, 18, 28
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	9, 19, 29
	12	3-30	7, 17, 27
	8	2-30	1, 16
	8	2-30	6, 21
	4	1-30	11
	4	1-30	26
	4	1-30	10
	4	1-30	20
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS 30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
228	12	3-30	1, 11, 21
	12	3-30	2, 12, 22
	12	3-30	10, 20, 30
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	6, 16, 26
	12	3-30	7, 17, 27
	8	2-30	8, 23
	4	1-30	3
	4	1-30	9
	4	1-30	13
	4	1-30	18
	4	1-30	19
	4	1-30	28
	4	1-30	29
229	12	3-30	1, 11, 21
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	6, 16, 26
	12	3-30	7, 17, 27
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	28
	4	1-30	29
	4	1-30	30
230	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	1, 16
	8	2-30	6, 21
	8	2-30	11, 26
	8	2-30	2, 17
	8	2-30	7, 22
	8	2-30	12, 27

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
231	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	1, 16
	8	2-30	6, 21
	8	2-30	11, 26
	8	2-30	2, 17
	8	2-30	7, 22
	4	1-30	12
	4	1-30	27
232	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	1, 16
	8	2-30	6, 21
	8	2-30	11, 26
	8	2-30	2, 17
	4	1-30	7
	4	1-30	12
	4	1-30	22
	4	1-30	27
233	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	1, 16
	8	2-30	6, 21
	8	2-30	11, 26
	4	1-30	2
	4	1-30	7
	4	1-30	12
	4	1-30	17
	4	1-30	22
	4	1-30	27

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
234	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	1, 16
	8	2-30	6, 21
	4	1-30	11
	4	1-30	2
	4	1-30	7
	4	1-30	12
	4	1-30	17
	4	1-30	22
	4	1-30	26
	4	1-30	27
235	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	8, 18, 28
	12	3-30	9, 19, 29
	12	3-30	10, 20, 30
	8	2-30	6, 21
	4	1-30	1
	4	1-30	2
	4	1-30	7
	4	1-30	11
	4	1-30	12
	4	1-30	16
	4	1-30	17
	4	1-30	22
	4	1-30	26
	4	1-30	27

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
236	12	3-30	1, 11, 21
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	12	3-30	6, 16, 26
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
237	12	3-30	1, 11, 21
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	6, 16, 26
	12	3-30	7, 17, 27
	8	2-30	10, 25
	8	2-30	15, 30
	8	2-30	5, 20
	8	2-30	4, 19
	8	2-30	9, 24
	8	2-30	14, 29
	4	1-30	8
	4	1-30	18
	4	1-30	28

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Sampling Rate	Commutator Type	Master Control Unit Program
238	12	3-30	7, 17, 27
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	8, 18, 28
	8	2-30	5, 20
	8	2-30	10, 25
	8	2-30	15, 30
	8	2-30	6, 21
	8	2-30	11, 26
	4	1-30	16
	4	1-30	1
	4	1-30	9
	4	1-30	19
	4	1-30	29
239	12	3-30	7, 17, 27
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	8, 18, 28
	8	2-30	5, 20
	8	2-30	10, 25
	8	2-30	15, 30
	8	2-30	1, 16
	4	1-30	6
	4	1-30	9
	4	1-30	11
	4	1-30	19
	4	1-30	21
	4	1-30	26
	4	1-30	29
240	12	3-30	7, 17, 27
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	8, 18, 28
	8	2-30	5, 20
	8	2-30	10, 25
	8	2-30	15, 30
	4	1-30	1
	4	1-30	6
	4	1-30	9
	4	1-30	11
	4	1-30	16
	4	1-30	19
	4	1-30	21
	4	1-30	26
	4	1-30	29

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
241	12	3-30	7, 17, 27
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	8, 18, 28
	8	2-30	5, 20
	8	2-30	10, 25
	4	1-30	1
	4	1-30	6
	4	1-30	9
	4	1-30	11
	4	1-30	15
	4	1-30	16
	4	1-30	19
	4	1-30	21
	4	1-30	26
	4	1-30	29
	4	1-30	30
242	12	3-30	7, 17, 27
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	8, 18, 28
	8	2-30	5, 20
	4	1-30	1
	4	1-30	6
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	15
	4	1-30	16
	4	1-30	19
	4	1-30	21
	4	1-30	25
	4	1-30	26
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
243	12	3-30	1, 11, 21
	12	3-30	2, 12, 22
	12	3-30	3, 13, 23
	12	3-30	4, 14, 24
	12	3-30	5, 15, 25
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
244	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	2, 17
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	8	2-30	14, 29
	8	2-30	15, 30
245	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	5, 20
	8	2-30	10, 25
	8	2-30	15, 30
	8	2-30	2, 17
	8	2-30	7, 22
	8	2-30	12, 27
	8	2-30	4, 19
	8	2-30	9, 24
	4	1-30	14
	4	1-30	29

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
246	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	2, 17
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	4	1-30	14
	4	1-30	15
	4	1-30	29
	4	1-30	30
247	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	5, 20
	8	2-30	10, 25
	8	2-30	15, 30
	8	2-30	2, 17
	8	2-30	7, 22
	8	2-30	12, 27
	4	1-30	4
	4	1-30	9
	4	1-30	14
	4	1-30	19
	4	1-30	24
	4	1-30	29

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
248	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	2, 17
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	9, 24
	4	1-30	10
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	25
	4	1-30	27
	4	1-30	29
	4	1-30	30
249	12	3-30	1, 11, 21
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	12	3-30	6, 16, 26
	8	2-30	5, 20
	8	2-30	10, 25
	8	2-30	15, 30
	8	2-30	2, 17
	4	1-30	4
	4	1-30	7
	4	1-30	9
	4	1-30	12
	4	1-30	14
	4	1-30	19
	4	1-30	22
	4	1-30	24
	4	1-30	27
	4	1-30	29

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
250	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	2, 17
	8	2-30	4, 19
	8	2-30	5, 20
	4	1-30	7
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	22
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	29
	4	1-30	30
251	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	2, 17
	8	2-30	4, 19
	4	1-30	5
	4	1-30	7
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	20
	4	1-30	22
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
252	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	8	2-30	2, 17
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	29
	4	1-30	30
253	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	3, 13, 23
	12	3-30	8, 18, 28
	4	1-30	2
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
254	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	13, 28
	8	2-30	14, 29
	8	2-30	15, 30
	4	1-30	7
	4	1-30	17
	4	1-30	27
255	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	13, 28
	8	2-30	14, 29
	4	1-30	7
	4	1-30	15
	4	1-30	17
	4	1-30	27
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
256	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	13, 28
	4	1-30	7
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	27
	4	1-30	29
	4	1-30	30
257	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	4	1-30	7
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
258	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	8, 23
	8	2-30	9, 24
	4	1-30	7
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
259	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	8, 23
	4	1-30	7
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
260	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
261	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	8	2-30	4, 19
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	20
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
262	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	2, 12, 22
	8	2-30	3, 18
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	19
	4	1-30	20
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
263	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	12	3-30	2, 12, 22
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
264	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	8	2-30	13, 28
	8	2-30	14, 29
	8	2-30	15, 30
265	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	8	2-30	13, 28
	8	2-30	14, 29
	4	1-30	15
	4	1-30	30
266	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	8	2-30	13, 28
	4	1-30	14
	4	1-30	15
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
267	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	28
	4	1-30	29
	4	1-30	30
268	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
269	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
270	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
271	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
272	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
273	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
274	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	8	2-30	3, 18
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
275	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	8	2-30	2, 17
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
276	12	3-30	1, 11, 21
	12	3-30	6, 16, 26
	4	1-30	2
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
277	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	8	2-30	13, 28
	8	2-30	14, 29
	8	2-30	15, 30
	4	1-30	6
	4	1-30	16
	4	1-30	26

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
278	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	8	2-30	13, 28
	8	2-30	14, 29
	4	1-30	6
	4	1-30	15
	4	1-30	16
	4	1-30	26
	4	1-30	30
279	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	8	2-30	13, 28
	4	1-30	6
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	26
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
280	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	12, 27
	4	1-30	6
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	26
	4	1-30	28
	4	1-30	29
	4	1-30	30
281	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	4	1-30	6
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
282	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	4	1-30	6
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
283	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	8	2-30	8, 23
	4	1-30	6
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
284	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	7, 22
	4	1-30	6
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
285	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
286	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	4	1-30	5
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
287	12	3-30	1, 11, 21
	8	2-30	2, 17
	8	2-30	3, 18
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
288	12	3-30	1, 11, 21
	8	2-30	2, 17
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
289	12	3-30	1, 11, 21
	4	1-30	2
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
290	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	11, 26
	8	2-30	12, 27
	8	2-30	13, 28
	8	2-30	14, 29
	8	2-30	15, 30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
291	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	11, 26
	8	2-30	12, 27
	8	2-30	13, 28
	8	2-30	14, 29
	4	1-30	15
	4	1-30	30
292	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	11, 26
	8	2-30	12, 27
	8	2-30	13, 28
	4	1-30	14
	4	1-30	15
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
293	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	11, 26
	8	2-30	12, 27
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	28
	4	1-30	29
	4	1-30	30
294	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	8	2-30	11, 26
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
295	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	8	2-30	10, 25
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
296	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	7, 22
	8	2-30	8, 23
	8	2-30	9, 24
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
297	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	7, 22
	8	2-30	8, 23
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30
298	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	6, 21
	8	2-30	7, 22
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
299	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	8	2-30	6, 21
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
300	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	8	2-30	5, 20
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
301	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	8	2-30	4, 19
	4	1-30	5
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	20
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
302	8	2-30	1, 16
	8	2-30	2, 17
	8	2-30	3, 18
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	19
	4	1-30	20
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
303	8	2-30	1, 16
	8	2-30	2, 17
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE COMMUTATOR SYSTEM

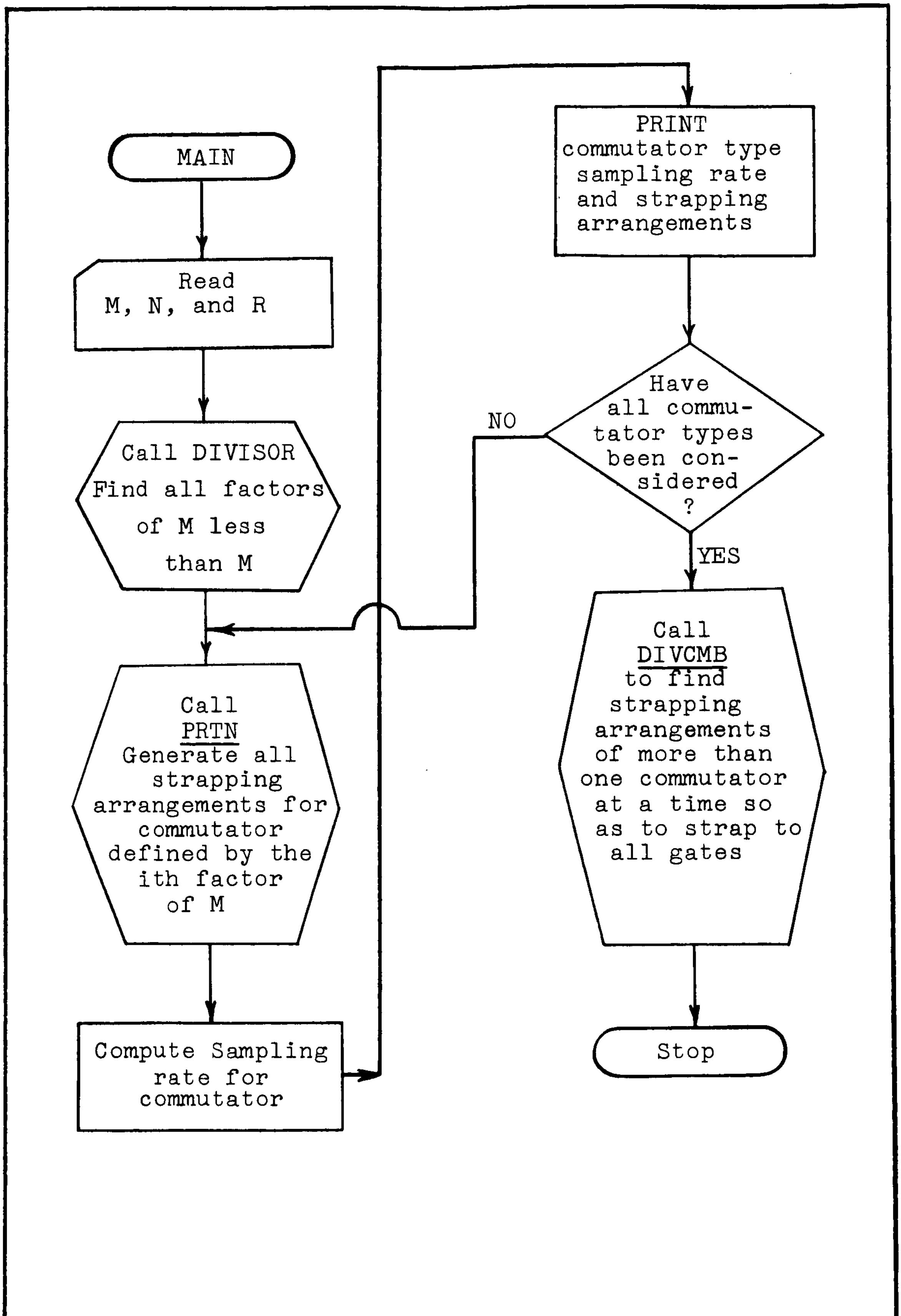
Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
304	8	2-30	1, 16
	4	1-30	2
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

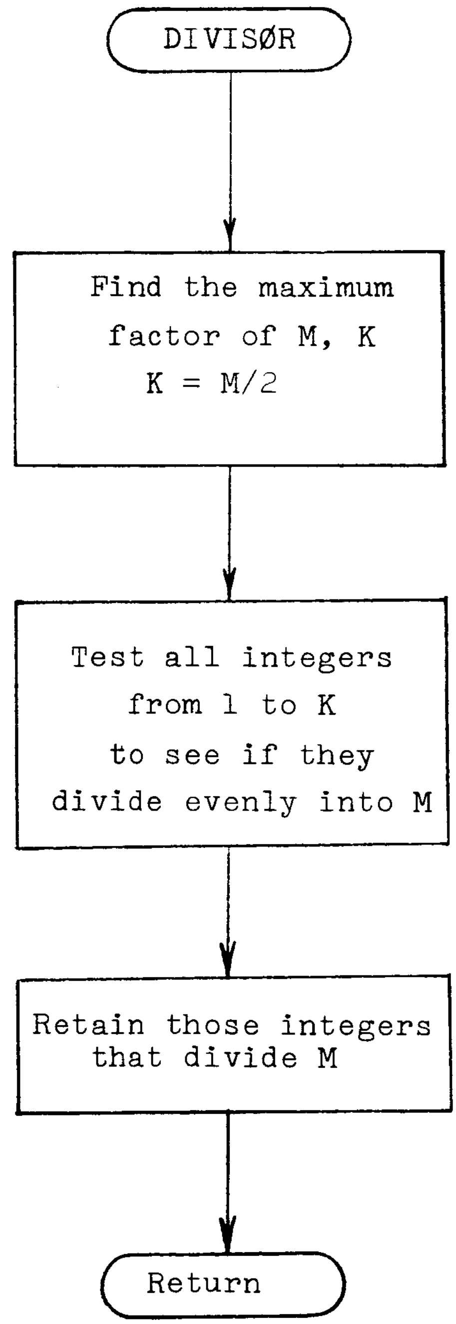
PAM COMMUTATION SYSTEM PROGRAMS
30-CHANNEL MULTI-MODE
COMMUTATOR SYSTEM

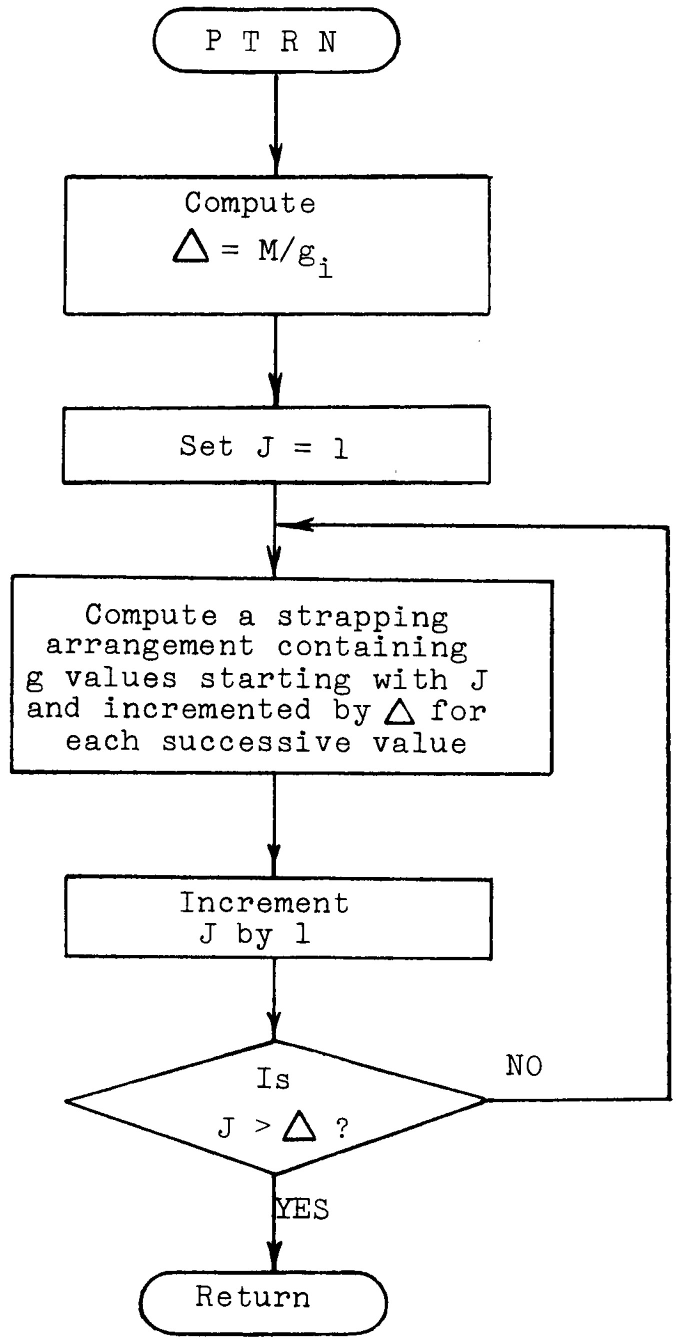
Program Number	Required Sampling Rate	Commutator Type	Master Control Unit Program
305	4	1-30	1
	4	1-30	2
	4	1-30	3
	4	1-30	4
	4	1-30	5
	4	1-30	6
	4	1-30	7
	4	1-30	8
	4	1-30	9
	4	1-30	10
	4	1-30	11
	4	1-30	12
	4	1-30	13
	4	1-30	14
	4	1-30	15
	4	1-30	16
	4	1-30	17
	4	1-30	18
	4	1-30	19
	4	1-30	20
	4	1-30	21
	4	1-30	22
	4	1-30	23
	4	1-30	24
	4	1-30	25
	4	1-30	26
	4	1-30	27
	4	1-30	28
	4	1-30	29
	4	1-30	30

APPENDIX C

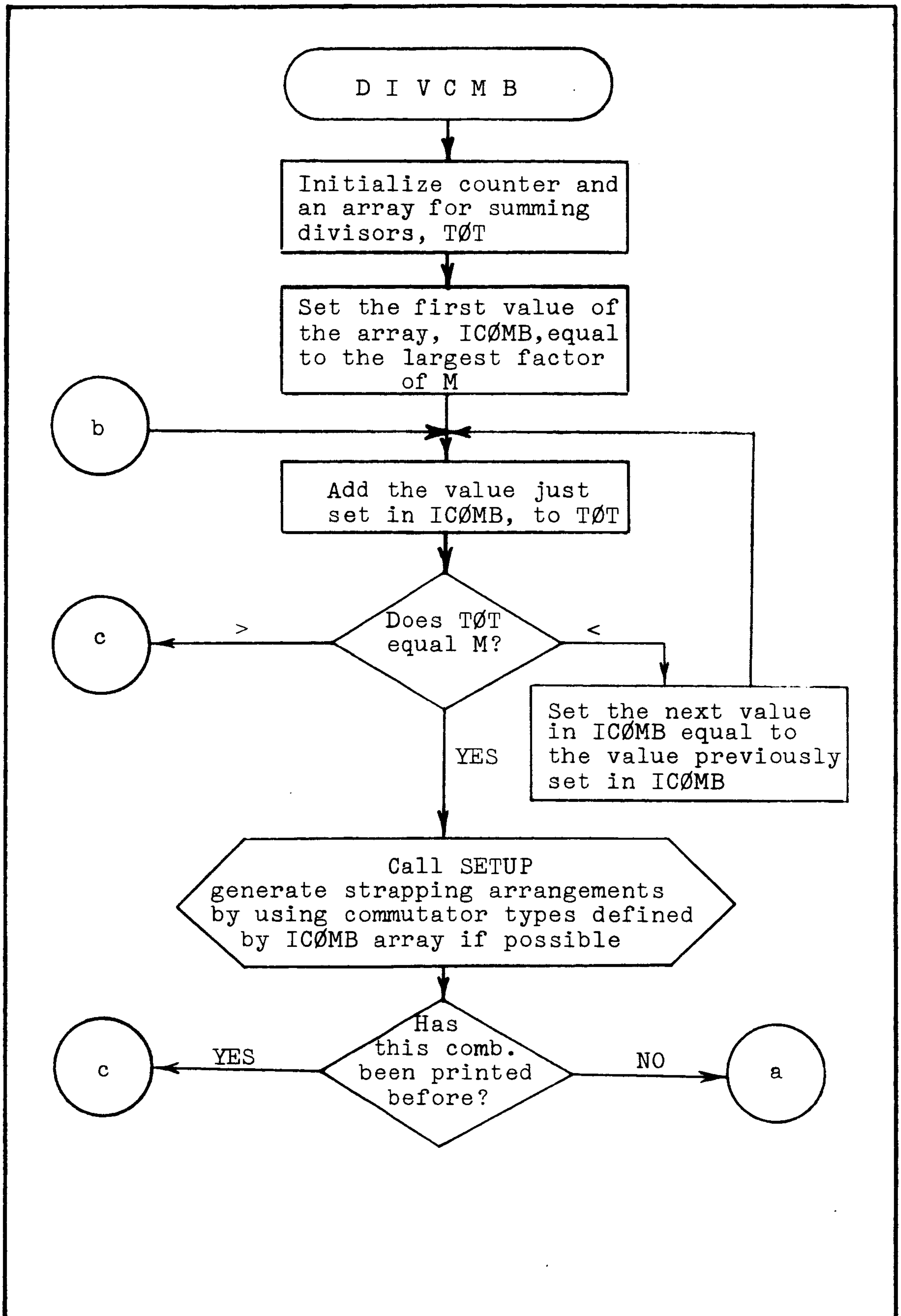
Procedural Flow Charts for the Computer Programming of an M-Channel PAM Commutator System

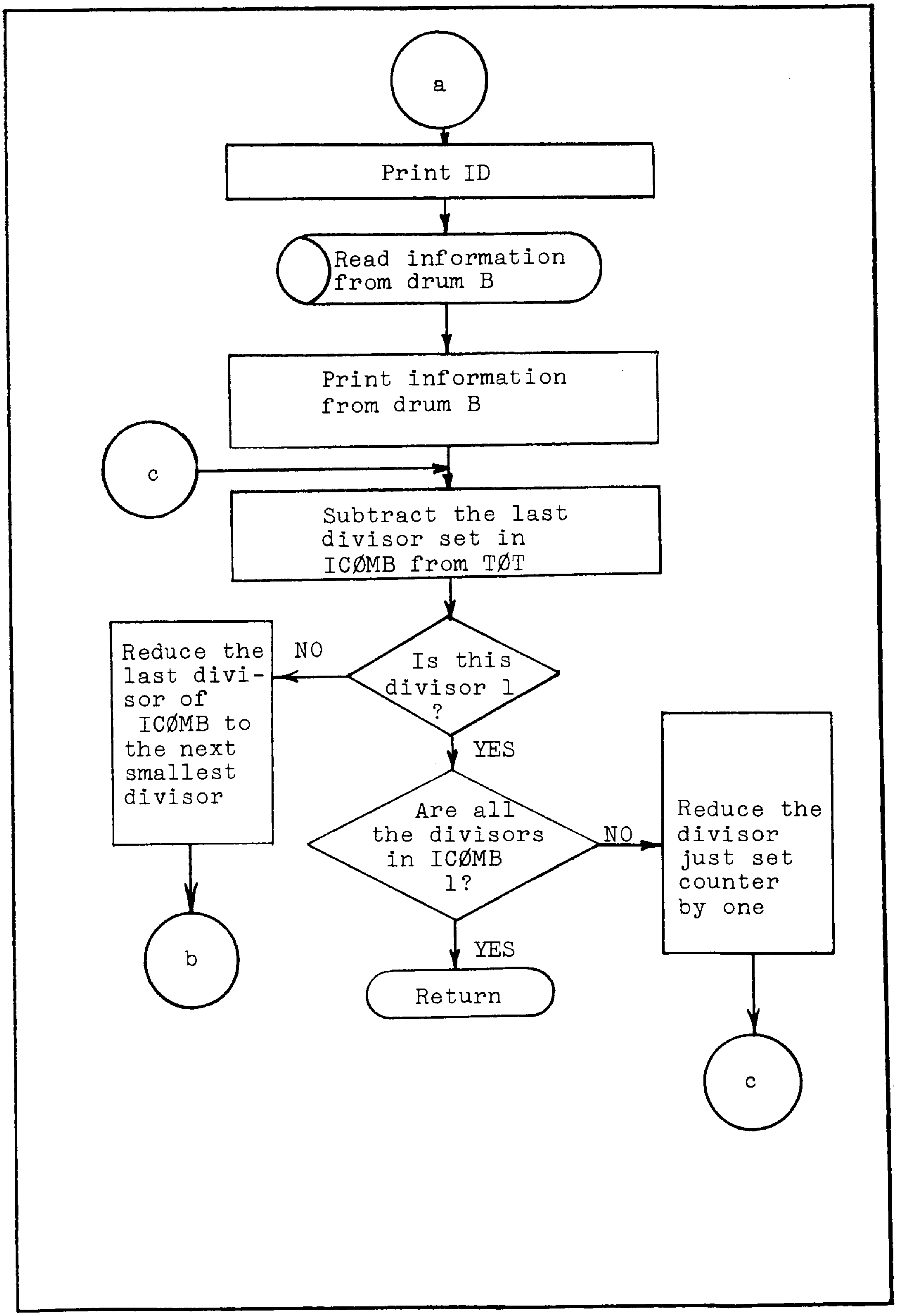

MAIN
Read M, N, and R
Call DIVISOR Find all factors of M less than M
Call PRTN Generate all strapping arrangements for commutator defined by the ith factor of M
Compute Sampling rate for commutator
PRINT commutator type sampling rate and strapping arrangements
Have all commutator types been considered ?
NO
YES
Call DIVCMB to find strapping arrangements of more than one commutator at a time so as to strap to all gates
Stop

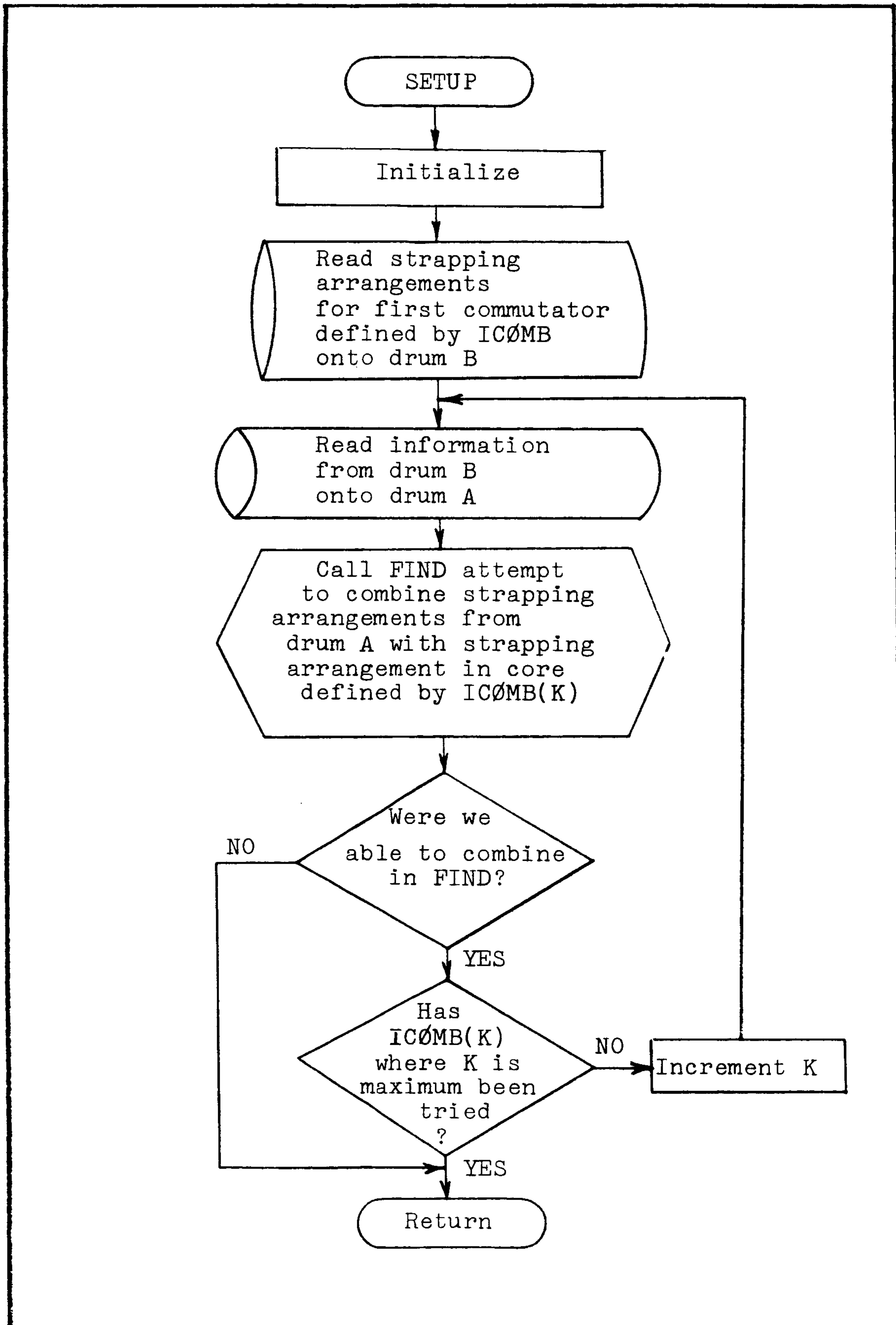

DIVISØR
Find the maximum
factor of M, K
K = M/2
Test all integers
from 1 to K
to see if they
divide evenly into M
Retain those integers
that divide M
Return

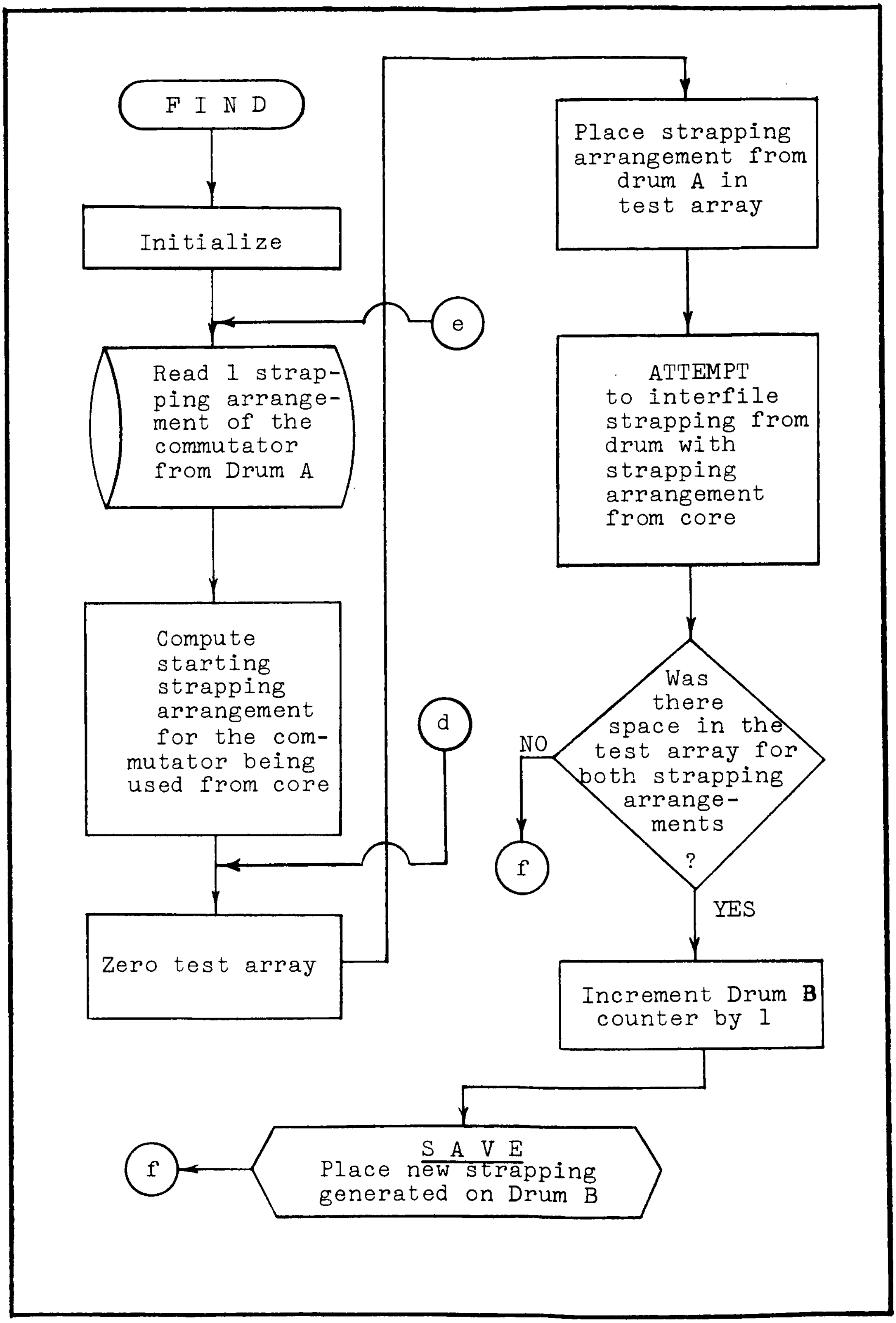


P T R N
Compute
△ = M/g_i
Set J = 1
Compute a strapping arrangement containing g values starting with J and incremented by △ for each successive value
Increment J by 1
Is J > △ ?
NO
YES
Return

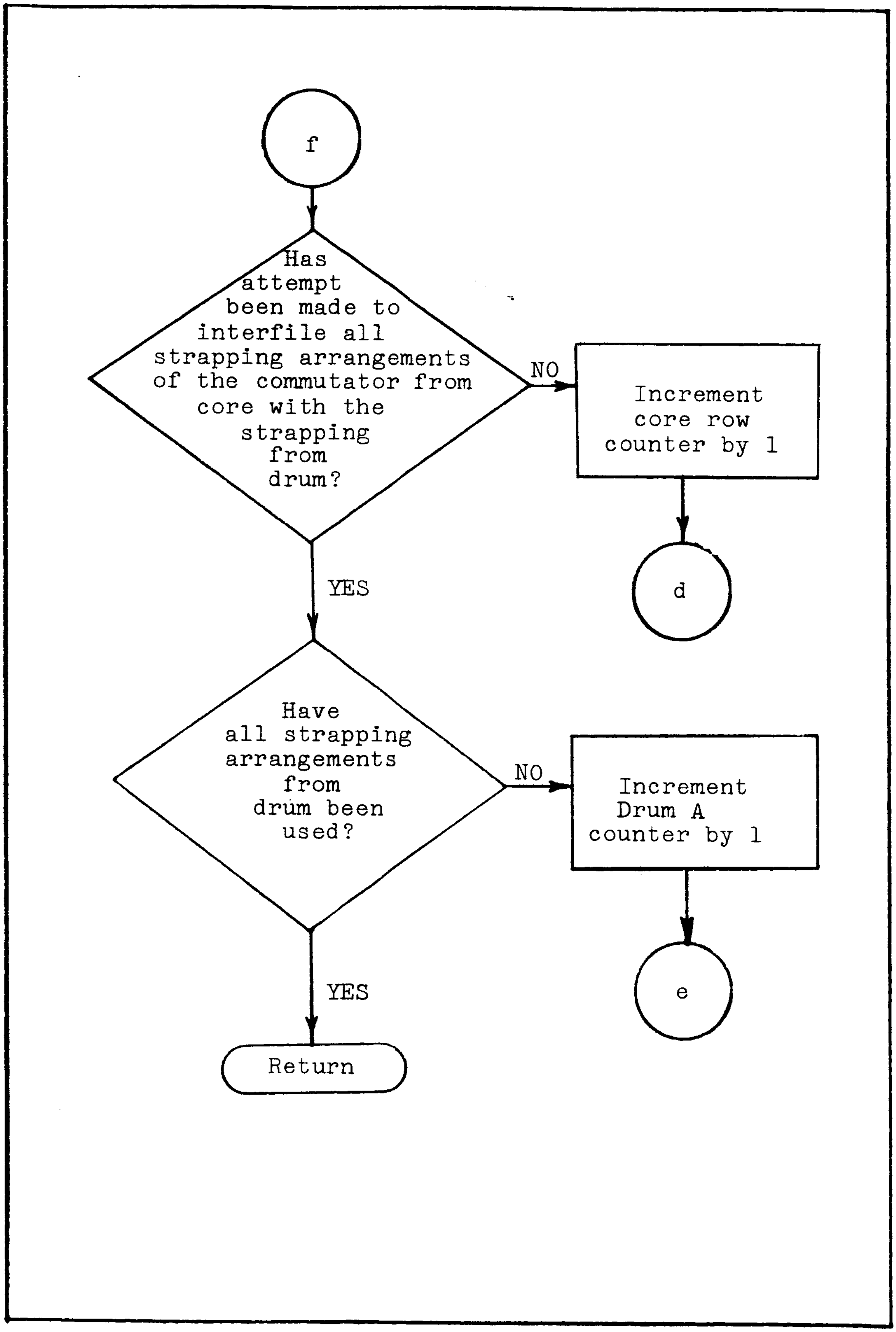

D I V C M B
Initialize counter and an array for summing divisors, TØT
Set the first value of the array, ICØMB, equal to the largest factor of M
b
Add the value just set in ICØMB, to TØT
Does TØT equal M?
c
>
<
Set the next value in ICØMB equal to the value previously set in ICØMB
YES
Call SETUP generate strapping arrangements by using commutator types defined by ICØMB array if possible
Has this comb. been printed before?
c
YES
NO
a

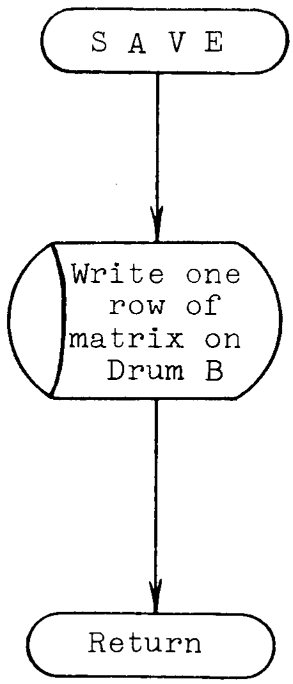

a
Print ID
Read information from drum B
Print information from drum B
c
Subtract the last divisor set in ICØMB from TØT
Is this divisor 1 ?
NO
Reduce the last divisor of ICØMB to the next smallest divisor
b
YES
Are all the divisors in ICØMB 1?
NO
Reduce the divisor just set counter by one
c
YES
Return


SETUP
Initialize
Read strapping arrangements for first commutator defined by ICØMB onto drum B
Read information from drum B onto drum A
Call FIND attempt to combine strapping arrangements from drum A with strapping arrangement in core defined by ICØMB(K)
Were we able to combine in FIND?
NO
YES
Has ICØMB(K) where K is maximum been tried ?
NO
Increment K
YES
Return



F I N D
Initialize
Read 1 strapping arrangement of the commutator from Drum A
Compute starting strapping arrangement for the commutator being used from core
Zero test array
e
d
Place strapping arrangement from drum A in test array
ATTEMPT to interfile strapping from drum with strapping arrangement from core
Was there space in the test array for both strapping arrangements ?
NO
f
YES
Increment Drum B counter by 1
S A V E
Place new strapping generated on Drum B
f


f
Has attempt been made to interfile all strapping arrangements of the commutator from core with the strapping from drum?
NO
Increment core row counter by 1
d
YES
Have all strapping arrangements from drum been used?
NO
Increment Drum A counter by 1
e
YES
Return


SAVE
Write one row of matrix on Drum B
Return

APPENDIX D

A Fortran IV Computer Program Utilizing a Univac 1107 Computer for the Programming of an M-Channel PAM Commutator System

```
C*****PROGRAM FOR FINDING STRAPING POSITIONS
C
      DIMENSION IDIV(10),IWD(10,60,30)
      READ (5,1) M,N,R
    1 FORMAT(2I10,F10.0)
C     FIND DIVISORS OF M
      CALL DIVSOR(M,IDIV,ICNT)
      WRITE (6,5) M,(IDIV(I), I=1,ICNT)
    5 FORMAT(1H1,10X,10HFACTORS OF ,I3,1X,3HARE,10(I2,1X))
      WRITE (6,6)
    6 FORMAT(////48X,17HPRIMARY POSITIONS/)
      DO 10 I=1,ICNT
C     FIND DIVISOR PATTERNS
      CALL PTRN(IDIV,I,M,IWD)
      IDEL=M/IDIV(I)
      SR=R*FLOAT(IDIV(I))
      WRITE (6,2) IDIV(I),N,SR
    2 FORMAT(//10X,5HTYPE(,I2,1H,I2,20H) COMMUTATOR  (SR - ,F5.2,1H)/)
      III=IDIV(I)
      DO 20 L=1,IDEL
      WRITE (6,3) (IWD(I,L,K) ,K=1,III)
    3 FORMAT(20X,30(I2,1X))
   20 CONTINUE
   10 CONTINUE
      WRITE (6,4)
```

```
    4 FORMAT(1H1)
C     FIND MAXIMUM COMBINATION OF PATTERNS AND THOSE OF LESS THAN
C     MAXIMUM CAPICITY
      CALL DIVCMB(M,IDIV,ICNT,IWD,N)
      STOP
      END
      SUBROUTINE DIVCMB(M,IDIV,ICNT,IWD,N)
      DIMENSION IDIV(1),ICOMB(60),IDUM(60),IWD(10,60,30)
C*****SUBROUTINE FOR DIVISING PATTERNSMADE BY DIVISORS OF M WHEN THEIR
C*****TOTAL ADD UP TO M
C
      ITOT=0
      I=ICNT
      J=1
   10 ITOT=ITOT+IDIV(I)
      ICOMB(J)=IDIV(I)
      IF(ITOT-M) 20,30,40
   20 J=J+1
      GO TO 10
   30 CALL SETUP(J,ICOMB,M,IWD,IDIV,IKK,ICNT)
      IF (IKK) 40,40,110
  110 REWIND 26
      WRITE (6,1) (ICOMB(NO) ,NO=1,J)
    1 FORMAT(//1X,21HSTRAPPING ARRANGEMENT,2X,30(I2,1X)/)
      IC=J*N
```

```
      DO 120 NO=1,IKK
      READ (26) (IDUM(KNDX), KNDX=1,M)
      WRITE (6,2) (IDUM(KNDX), KNDX=1,M)
    2 FORMAT(10X,30(I2,1X))
  120 CONTINUE
   40 ITOT=ITOT-ICOMB(J)
      IF(ICOMB(J)-1) 50,60,50
   50 I=1
   70 IF(ICOMB(J)-IDIV(I)) 80,90,80
   80 I=I+1
      GO TO 70
   90 I=I-1
      GO TO 10
   60 J=J-1
      IF(J-1) 100,40,40
  100 RETURN
      END
C**** PROGRAM TO INITIALIZE INTERFILLING PATTERNS
C
      SUBROUTINE SETUP(J,ICOMB,M,IWD,IDIV,IKK,ICNT)
      DIMENSION ICOMB(1),IWD(10,60,30),IDIV(1),        ID(60),IVAL(60)
      WRITE (6,77) (ICOMB(IJJ), IJJ=1,4)
   77 FORMAT (1X,30(I2,1X))
      I=ICOMB(1)
      LGNTH=M/I
```

```
      ID(1)=I
      LTH=I
      DO 20 IJJ=1,ICNT
      IF (I-IDIV(IJJ)) 20,50,20
   20 CONTINUE
   50 REWIND 26
      DO 100 JNDX=1,LGNTH
      WRITE (26) (IWD(IJJ,JNDX,KNDX) ,KNDX=1,LTH)
  100 CONTINUE
      DO 80 K=2,J
      REWIND 25
      REWIND 26
      DO 30 JNDX=1,LGNTH
      READ (26) (IVAL(KNDX) ,KNDX=1,LTH)
      WRITE (25) (IVAL(KNDX) ,KNDX=1,LTH)
   30 CONTINUE
      II=ICOMB(K)
      ID(K)=II
      REWIND 25
      REWIND 26
      CALL FIND(IKK,M,II,IWD,IDIV,LGNTH,LTH,ICOMB,IVAL,K,ICNT)
      IF(IKK) 40,10,40
   40 LTH=LTH+ID(K)
      LGNTH=IKK
   80 CONTINUE
```

```
   10 RETURN
      END
      SUBROUTINE FIND(IKK,M,II,IWD,IDIV,LGNTH,LTH,ICOMB,IVAL,KI,ICNT)
C**** SUBROUTINE TO INTERFILE TWO PATTERNS
C
      DIMENSION IARRAY(60),IWD(10,60,30),IDIV(1),ICOMB(1),IVAL(1)
      IND=LTH-II+1
      IKK=0
      ITEST=M/II
      MTEST=II
      DO 90 JKL=1,ICNT
      IF(II-IDIV(JKL)) 90,100,90
   90 CONTINUE
  100 DO 10 J=1,LGNTH
      READ (25) (IVAL(K),K=1,LTH)
      IK=IVAL(IND)
      IF(ICOMB(KI)-ICOMB(KI-1)) 80,70,80
   80 IK=1
   70 DO 20 JJ=IK,ITEST
      DO 30 IN=1,M
      IARRAY(IN)=0
   30 CONTINUE
      DO 40  K=1,LTH
      INDEX=IVAL(K)
      IARRAY(INDEX)=INDEX
```

```
40 CONTINUE
   DO 50  KK=1,MTEST
   IDUM=IWD(JKL,JJ,KK)
   IF(IARRAY(IDUM)) 20,60,20
60 IARRAY(IDUM)=IDUM
50 CONTINUE
   IKK=IKK+1
   CALL SAVE(IWD,LTH,JKL,JJ,MTEST,IVAL)
20 CONTINUE
10 CONTINUE
   RETURN
   END
   SUBROUTINE SAVE(IWD,LTH,II,JJ,MTEST,IVAL)
   DIMENSION IWD(10,60,30) ,IVAL(1),IBLNK(60)
   DO 10 KKK=1,LTH
   IBLNK(KKK)=IVAL(KKK)
10 CONTINUE
   DO 20 KKK=1,MTEST
   IBLNK(KKK+LTH)=IWD(II,JJ,KKK)
20 CONTINUE
   ISUM=LTH+MTEST
   WRITE (26) (IBLNK(KKK),KKK=1,ISUM)
   RETURN
   END
   SUBROUTINE PTRN(IDIV,I,M,IWD)
```

```
      DIMENSION IDIV(1),IWD(10,60,30)
      IDEL=M/IDIV(I)
      L=1
      II=IDIV(I)
      DO 20  J=1,IDEL
      IWD(I,L,1)=J
      IF(II-1) 30,40,30
   30 DO 10  K=2,II
      IWD(I,L,K)=IWD(I,L,K-1)+IDEL
   10 CONTINUE
   40 L=L+1
   20 CONTINUE
      RETURN
      END
      SUBROUTINE DIVSOR(M,IDIV,ICNT)
      DIMENSION IDIV(1)
      K=M/2
      ICNT=0
      DO 10  I=1,K
      J=M/I
      ITST=I*J
      IF (ITST-M)  10,20,10
   20 ICNT=ICNT+1
      IDIV(ICNT)=I
   10 CONTINUE
```

```
RETURN
END
```