First Quarterly Report

for

A Program of Research and Development of Low Input Voltage Conversion and Regulation

(14 June 1965 - 14 September 1965)

Contract No. NAS 5-9212

Prepared by

Honeywell, Inc.
Ordnance Division
Hopkins, Minnesota

for

Goddard Space Flight Center
Greenbelt, Maryland

A PROGRAM OF RESEARCH AND DEVELOPMENT OF LOW INPUT VOLTAGE CONVERSION AND REGULATION

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Goddard Space Flight Center

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SUMMARY

This report discusses the work completed and the problems encountered on Contract Number NAS-5-9212 during the first quarter. The report also discusses the work planned for the next interval.

During this quarter, an investigation sought means of maintaining high Low Input Voltage Converter (LIVC) efficiencies at increased operating frequencies. High speed power transistors were used in this investigation. This investigation indicated that certain circuit parameters can limit the rise time of the switching signal, thereby slowing the switching speed. This limitation is significantly large compared to the inherent switching speed of the transistors. These circuit parameters include the leakage inductance associated with the power and/or current feedback transformers, the inductance of the switching reactor after saturation, and the response of the current feedback transformer core. The significance of these parameters is increased when high-speed, diffused-based transistors are used because the switching speed of these transistors is approximately ten times faster than that of previously used alloy junction transistors.

During laboratory testing, transformer leakage reactances were reduced by evenly distributing the windings around the toroidal core. Also, several four-layer diode circuits were considered as replacements for the switching reactor. This testing indicated that some performance improvement could be realized by these modifications. They will be more thoroughly investigated in the future. It is felt that the very fast switching of the four-layer diode will enable us to apply the switching signal faster than was possible with the switching reactor.

A study of the response of various core materials indicated that a Ferrite core would give the fastest induced voltage rise resulting from a switching current pulse. The responses of Supermalloy and Permalloy cores were approximately equal to each other and only slightly slower than Ferrite.

Under switching conditions felt to be representative of the LIVC application, the fastest response was realized with a high switching-current to winding-turns ratio. It is recommended that this be examined more closely in actual circuit application. The core testing also verified that the core response can be increased by applying increased amounts of switching current through a fixed number of windings. The limitations imposed by related circuitry on increasing the switching current to a very high value should be more fully analyzed in the future.

Work was also extended to develop a redundant LIVC synchronization circuit which would reliably maintain synchronous operation without decreasing the reliability afforded by the LIVC redundancy. This report discusses a circuit which looks promising. Testing and analysis of other circuits, however, will continue during the next interval to more firmly establish one which is suitable.

An analysis of the load sharing resulting when separate thermoelectric source-LIVC combinations are operated into a common load was conducted this quarter. Assuming identical LIVCs, the common output forces equal input voltages when each is delivering power even though the inputs are separate. Thus, the power delivered by each source is dependent on its current capability at that voltage where the lead requirements and the source's capabilities are equal. It is also noteworthy that more power is delivered to a fixed resistive load when the number of high impedance redundant sources delivering power to that load is increased. The load sharing resulting when redundant regulators are included should be analyzed in the future.

Initial reliability calculations have shown that it is desirable to design this power system configuration so that a certain percentage decline in available output power can be tolerated at the end of the anticipated three year space mission. Based upon initial assumptions, a 50% decline would provide an

MTBF of at least 23.5 years which is a much longer life than required. It is recommended that the allowable degradation be established and that the reliability assumptions for the individual modules should be compared with that obtainable with present technology in order to establish more accurate estimates for the selection of the optimum redundant system configuration.

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SECTION I

ACTIVITIES OF THE FIRST QUARTER

A. INTRODUCTION

This report discusses the progress made during the first three months of contract NAS-5-9212 for "A Research and Development Program in Low Input Voltage Conversion and Regulation". This program is a continuation and amplification of work completed under Contracts NAS-5-3441 and NAS-5-3899 toward advancing the state-of-the-art of Low Input Voltage Conversion and Regulation (LIVCR) for use with new energy conversion sources in future satellites. The purpose of this program is:

1. Advance low input voltage conversion and regulation technology to:

   a) reduce weight

   b) increase efficiency

   c) increase reliability.

2. Study the "trade-offs" of various combinations of redundant sources and redundant LIVCRs with a storage battery to achieve higher reliability and higher power capability (300 watts) for a three year satellite mission.

3. Study and solve the redundant source-redundant LIVCR system integration and operational problems.

4. Breadboard the optimum 300 watt redundant source-redundant LIVCR battery system using several simulated thermoelectric generator sources.

The work performed during this quarter included:

1. Investigation of LIVC operation at high frequencies (10KC) with emphasis on circuit and device parameters that limit the power oscillator switching speed and the use of new devices and circuitry to accomplish switching.

2. Investigation of redundant LIVC synchronizing circuits.

3. An analysis of the redundant LIVC common output load sharing.

4. Initial reliability analysis of various redundant source-redundant LIVC configurations.

The investigation of the power oscillator operation at higher frequencies disclosed that transformer leakage inductances, the inductance of the saturated switching reactor, and the response of the current feedback transformer core limited the rise time of the transistor drive signal. The slow drive signal rise time was found to be the primary reason for slow transistor switching and high switching losses. Circuits which diminished the effect of leakage inductance and circuits utilizing fast switching four-layer diodes were incorporated to increase the oscillator switching speed and study its switching characteristics.

Several circuits for synchronizing the frequencies of two current feedback oscillators were tested to reveal possible problem areas and solutions to provide a reliable synchronization for all of the expected operating conditions. The load sharing and initial redundant configuration reliability analysis will be beneficial in determining the best redundant configuration for the system.

B. TECHNICAL DISCUSSION

1. High Speed Switching Investigations

Investigations directed towards higher operating frequencies utilizing high speed transistors have shown that the switching speed has been limited by the rise time of the base drive wave forms. These investigations have shown that the saturating choke coil commonly used to accomplish switching does not produce the desired fast rise time because the toroidal reactor still contains an appreciable inductance after the steel core has saturated. This remaining inductance has been sufficient to limit the rise time to a few microseconds. It has also been noted that the windings of the power transformer and the feedback transformer may contain sufficient leakage inductance which will limit the rise time of the switching signal. Another factor which may limit the switching speed is the transient loading of the main oscillator by the switching signal when the switching reactor core saturates.

Thus these studies have shown that it is not enough to merely insert high speed transistors into the circuit. The drive signal circuitry and component parameters must be optimized to provide the desired fast rise time drive signals. Ideally the desired drive signals would have the following characteristics:

1. Fast rise from back bias to forward bias voltage.
2. Fast fall from forward bias to back bias voltage.
3. Accomplish 1 and 2 (above) without loading the oscillator during the switching interval.

Laboratory experiments have shown that the drive waveforms of the present oscillator tend to round off towards the end of the half cycle. This results in insufficient drive which may cause the conducting transistor to come out

of saturation towards the end of the cycle. Also, if the recycling circuit causes transient loading of the oscillator, the transistor collector current may increase. This transient loading causes the device to come out of saturation for an interval prior to switching and increases the switching losses due to a higher net voltage-current product during switching. These experiments have indicated that the main cause of slow switching has been the slow rise and fall times of the base drive signals. To rectify this situation experiments are currently being directed towards circuit changes to improve the drive signal waveforms. This is being directed toward the following areas:

1. Minimization of power transformer leakage reactance.
2. Minimization of feedback transformer leakage reactance.
3. The use of impedance elements which have much faster switching times.

(a) Influence of Transformer Leakage Reactance - The leakage reactance in the power transformer winding N3 will tend to slow the rise time when the recycling impedance switches. To minimize this it is desirable to distribute this winding evenly about the toroidal core. The effect of the leakage inductance of winding N3 on transformer T2 can be nullified by placing a filter between winding N3 on T2 and the feedback transformer recycling winding N3 on T1. This filter consists of inductance L1 and capacitor C1 shown on Figure 1. In this circuit, capacitor C1 provides a low impedance source of surge current for recycling, and inductance L1 provides the charging current path for C1, while also preventing capacitor from loading the oscillator at the start of each half cycle.

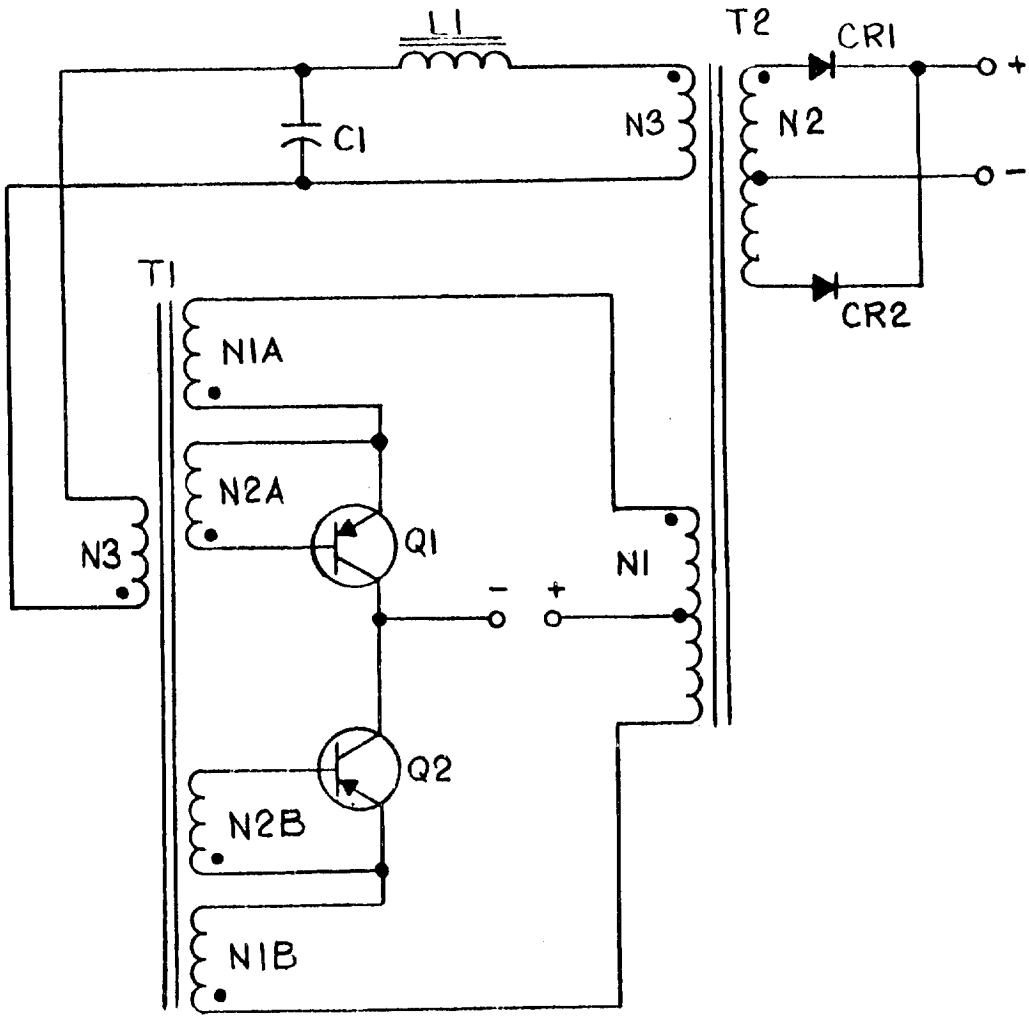


Figure 1 - CIRCUIT DIAGRAM OF LOW INPUT VOLTAGE CONVERTER

The leakage reactance of the feedback transformer should also be minimized by even distribution of the winding about the transformer core. The use of several parallel multifilar windings can provide advantage by providing a uniform layer throughout the surface of the core.

(b) Influence of the Residual Inductance of the Switching Reactor - The present current feedback power oscillator uses reactor L1 shown in Figure 1 to accomplish the switching. When L1 saturates, negative feedback current flows from winding N3 on transformer T2 through L1 to winding N3 on current feedback transformer T1. This negative feedback current overrides the inherent positive feedback in current transformer T1 to recycle the circuit. The current flow through this loop accomplishes switching by two methods:

1. The sudden flow of current through this loop loads the power oscillator momentarily and tends to cause the power oscillator transistor to come out of saturation. This causes the transistors to run out of drive and operate in a region of lower gain.

2. The negative feedback current through winding N3 on T1 opposes the positive drive through windings N1A and N1B and overrides the inherent positive feedback of the oscillator to cause the feedback transformer induced voltage to reverse.

The combination of these two mechanisms produces an overwhelming signal which causes the power oscillator to switch in a very positive manner. This method of switching can provide a very high instantaneous energy transfer which guarantees switching under all conditions. Thus, experience has shown that this switching method is positive and very reliable. The only disadvantage that we have found to date is that switching is not accomplished as rapidly as desired. Because of this, effort has been directed towards the investigation of other methods which would also switch the oscillator in a positive manner

and yet accomplish the switching more rapidly so that the power oscillator switching losses could be reduced to provide higher efficiency at higher operating frequencies. The investigation of these new approaches is discussed in Sections B:1:(d) and (e).

(c) Influence of Transformer Core Switching Time - The switching time of a magnetic core is generally defined as the time necessary to switch from flux saturation in one direction to saturation in the opposite direction. This switching time is inversely proportional to the magnitude of the switching signal as each core has a specific volt-second integral defined by the number of turns, core material, and geometry. While this switching time is a measure of the material response to a drive signal, it is not an absolute measure of the response time of the core as related to the switching of the power transistors in LIVCs. For purposes of transistor switching in LIVCs, the rise time of the back biasing induced voltage in response to the switching signal is of primary importance. Thus, the initial speed at which the rate of change of flux in the core is switched is of primary concern.

The initial laboratory testing involved a determination of the core switching times for Ferrite, Permalloy, Supermalloy, and Ferrite-Permalloy combined with various magnitudes of current drive (Figure 2). While total flux switching time is not the parameter of interest for LIVC transistor switching, these measurements were taken to determine if a significant correlation existed between them and the response of interest. The toroidal cores tested were the same size except that for the Ferrite-Permalloy core two equal size cores were placed together to form the composite core. Thus, this composite core actually had twice the area of the single material cores.

The test circuit and typical waveforms for current switching are indicated in Figure 3. A bias current is maintained through a winding to provide a reference for the described switching. It may be seen that the induced voltage

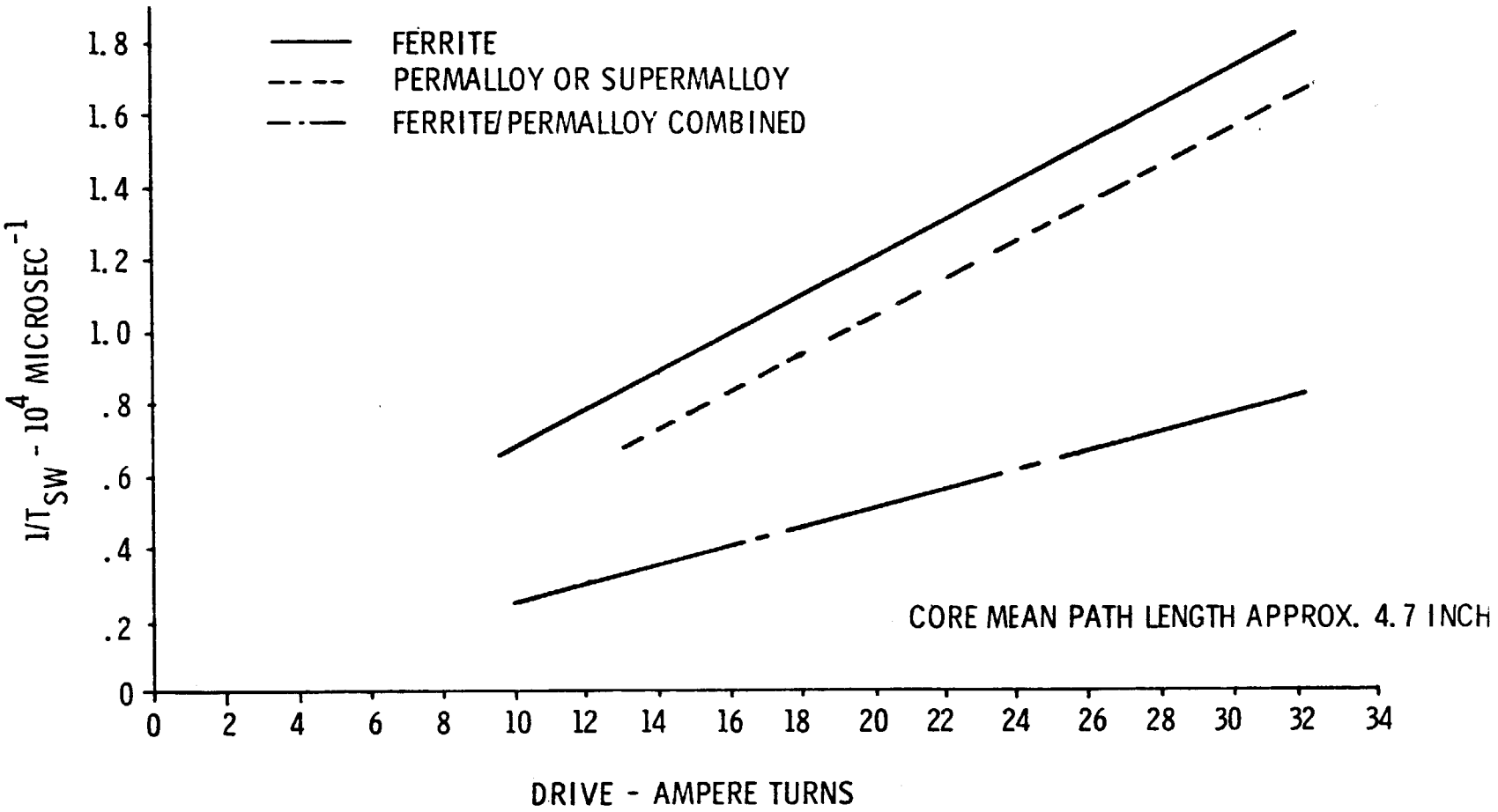


Figure 2 - MEASURED MAGNETIC CORE SWITCHING TIMES

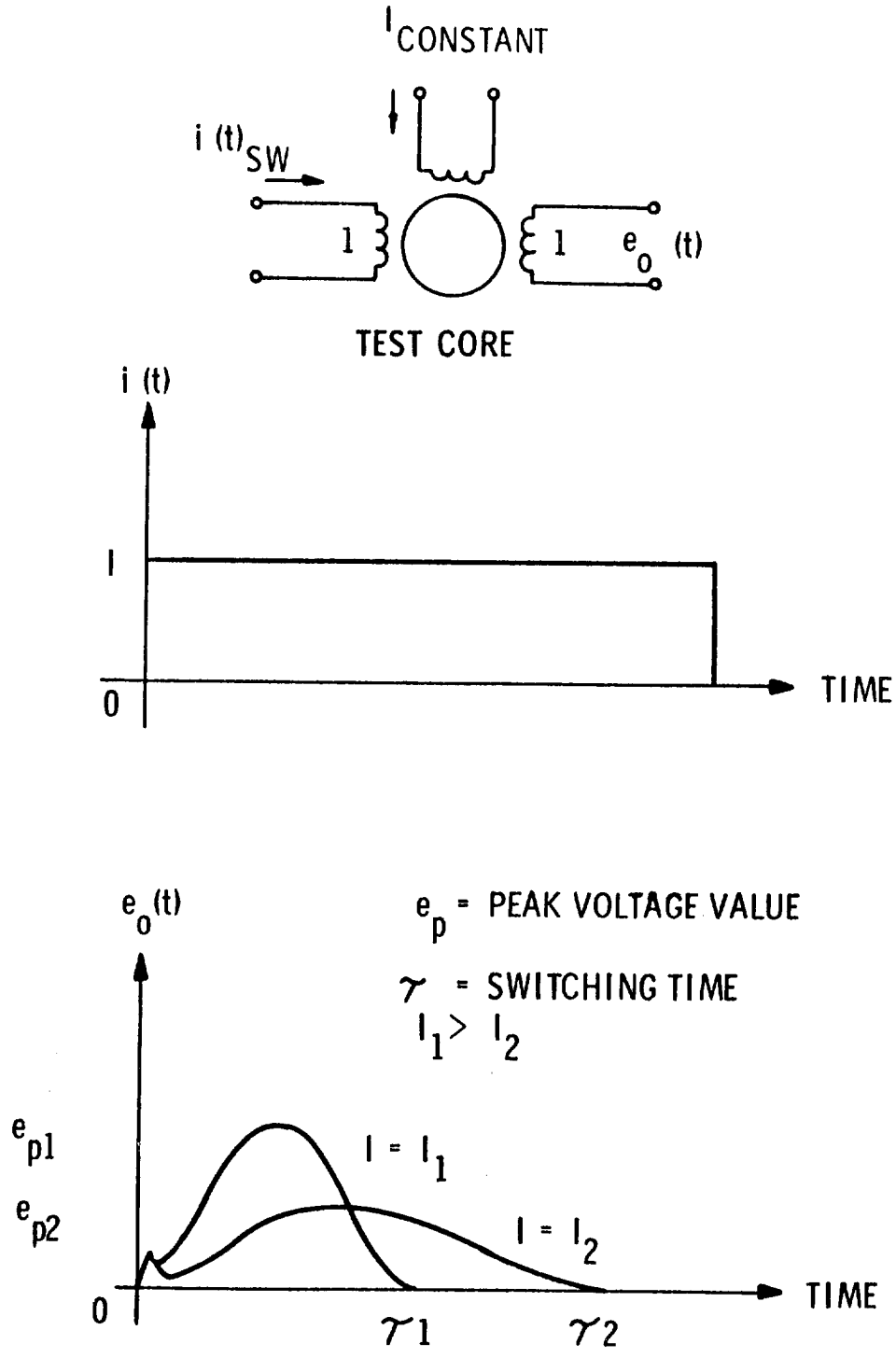


Figure 3 - RESPONSE WAVEFORMS FOR CONSTANT CURRENT SWITCHING

on the core increases as the magnitude of the switching current pulse increases, but the area under the volt-second curve remains constant. It follows that the switching time decreases with increased current drive. While the switching signal in the LIVC application is not a pure current signal, it is felt that it more closely approximates this than it does a voltage switching signal. This is assumed because the LIVC usually operates from a high impedance voltage source which, when reflected through the power transformer, usually is large compared to the switching circuit impedance during switching.

Referring to Figure 2, note that the Ferrite core has the fastest switching time. (All cores tested were of the same geometry and size except that the Ferrite-Permalloy combined consisted of two rather than one core.) Permalloy and Supermalloy exhibited equal switching times. Note also that the slope of the curve is steeper for those materials with shorter switching times. The steeper slope indicates a lower switching coefficient (a commonly defined core parameter). The curve presented for the composite Ferrite-Permalloy core indicates a relatively slow switching speed.

It should be noted that the switching time curves for Ferrite involves variable maximum flux densities; the curve for Permalloy and Supermalloy involves switching between fixed maximum material flux densities (± Bmax). The flux density in the Ferrite varies because the maximum switching amp-turns applied is less than that required to produce the saturation flux density in the core tested. Therefore, the switching in the Ferrite involved a progression from a flux density in one direction to an equal flux density in the opposite direction dependent on the amp-turns of drive applied. However, the important result of this testing (which has been verified by available data) seems to be that the switching coefficient of the Ferrite material is indeed lower than that of Permalloy or Supermalloy. The switching coefficient is defined as the reciprocal of the slope of the core switching time curve (Figure 2).

The induced voltage change resulting from the application of the switching signal characteristically had a faster rise time with a Ferrite core than with a Permalloy or Supermalloy core. It was also found that for equal amp-turns of switching signal, a faster induced voltage rise time was realized on each type core when the ratio of current to turns was increased (Figure 4 and 5). This was largely due to the fact that the current source did not have infinite impedance. As the impedance of the core became more significant (by increasing the turns), the switching current pulse was shaped more so that its rise time had a RL time constant rather than a step characteristic. Therefore, for equal "steady state" values of switching amp-turns, the fastest induced voltage rise time was realized with the current pulse having the fastest rise time. In turn, the fastest rise time for the current pulse was realized with the minimum number of turns on core (because the impedance was lower). This may also be true in the LIVC where the source of switching signal approximates a current source with a finite impedance. The direct applicability of this result will of course depend on the specific characteristics of related LIVC component design and the characteristic of the LIVC source.

The response of the Ferrite vs. that of the Permalloy can be compared by matching those plots with corresponding drive conditions. Comparing the responses of Figure 4A and 5A, the induced volts/turn on Ferrite reaches 1.4 volts within 0.75 μ sec. as compared to 1.25 volts within 1.0 μ sec. on Permalloy. Comparing the responses of Figures 4C and 5C, a level of 0.9 induced volts/turn is reached within 1 μ sec. with a Ferrite core and a level of 0.8 volts/turn is reached in the same time with a Permalloy core. Note that the final switching conditions are equal in each comparison even though the rise time of the switching current pulse may not be equal. Also, a faster induced voltage rise is obtained with the lower turns to current ratio of the switching winding (Figure 4A and 5A) even though the final amp-turns of switching signal are equal in each case considered. The increased speed realized by applying more switching current through a fixed number of turns

can be seen by comparing Figures 4B to 4C and 5B to 5C respectively. Note that the slope of the induced voltage/turn versus time is nearly doubled by doubling the current drive.

The switch (mercury relay) used to apply the current switching pulse characteristically had a rise time in the 0.5 microsecond range. The rise time of the oscilloscope used to measure the induced voltage rise time; however, was much faster than 0.5 microseconds. Therefore, although the test equipment did limit the accuracy of the measurements somewhat it is felt that the limitation was reasonably small.

The responses shown in Figure 4 and 5 were measured with an open circuited sense winding. It is known that loading a secondary winding on the core will increase the switching time and slow the response of the induced voltage. The experimental measurements of this effect is shown in Figures 6-8.

Note also that when comparing the response of Figure 6B to Figure 5C, the rise time of Figure 6B is considerably slower. (The verticle scale on Figure 6B has been reduced). The final drive amp-turns are equal but the turns to current ratios are unequal. The end switching current does not at first appear to be equal as represented by Figure 6A but for the time interval shown the maximum current is still being somewhat limited by the core and in time the switching current does equal 1 amp.

The response of the Ferrite-Permalloy core cannot be compared directly to the response of the other cores because its core area is larger. The measured response is presented in Figure 8, to provide a basis for an approximate comparison.

As in the investigation of core switching times, the magnetic path lengths for the various cores tested here were equal.

(d) Investigation of Circuits Using Alternative Frequency Determining and Switching Circuitry - The investigation of higher switching speeds for the current feedback power oscillator has lead to the consideration of other impedance elements in place of the saturable reactor L1 shown on Figure 1. The four-layer diode has been considered for this application because it has very fast switching characteristics. This diode presents a very high impedance to the flow of current as long as the voltage impressed across it is maintained below its breakdown voltage; however, if the impressed voltage reaches the breakdown voltage, its impedance will be reduced to a very low value, and it will remain conductive as long as the current flow through it is above its holding current value. In order to use the four-layer diode to control the operating frequency of the current feedback converter, it is necessary to incorporate some form of timing mechanism with the diode.

The following elements can be used in the timing circuit:

1. Capacitor
2. Inductance plus a capacitor
3. Saturating and non-saturating reactors.

(1) Four-Layer Diode With Capacitor Timing - A preliminary circuit is shown in Figure 9. In this circuit the timing is accomplished by the impedance Z1 and the value of the capacitor C1. The four-layer diode D1 is connected into the circuit by means of the bridge rectifier CR1 through CR4. After a time interval depending upon the Z1, C1, time constant and the voltage impressed by windings N3 on transformer T2, the capacitor charge will reach a value which will cause the four layer diode D1 to break over. When this occurs, capacitor C1 will discharge through the four layer diode into winding N3 on the feedback transformer T1 and tend to reverse the induced voltage in the feedback transformer. This signal reverses the voltage induced in the feedback transformer windings N2A and N2B. This back biases the formerly conducting

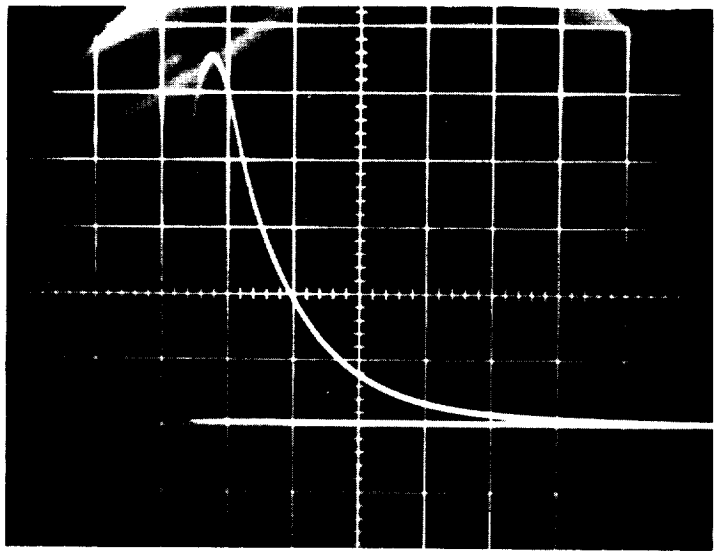


Figure 4A

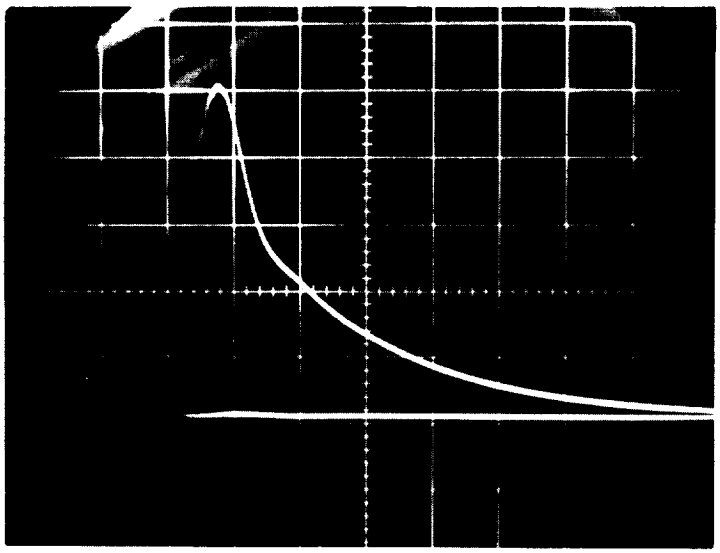


Figure 4B

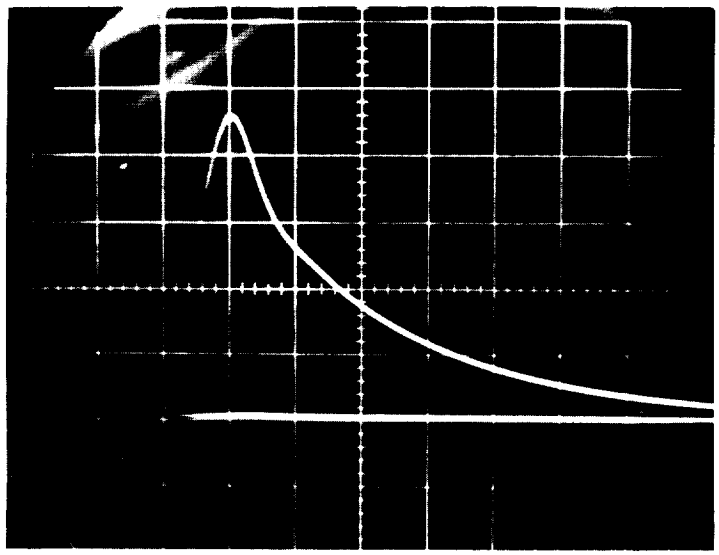


Figure 4C

INDUCED VOLTAGE RESPONSE WITH FERRITE CORE

	Figure 4A	Figure 4B	Figure 4C
SCALE			
Vertical	0. 25 V/turn/div.	0. 1 V/turn/div.	0. 2 V/turn/div.
Horizontal	1. 0 μ s/div.	1. 0 μ s/div.	1. 0 μ s/div.
DRIVE CONDITIONS			
Constant	N=2T	N=5T	N=5T
	I=0. 5A	I=0. 1A	I=0. 2A
Switch	N_s = 2T	N_s = 5T	N_s = 5T
	I_s =-1. 0A	I_s =-0. 2A	I_s = -0. 4A

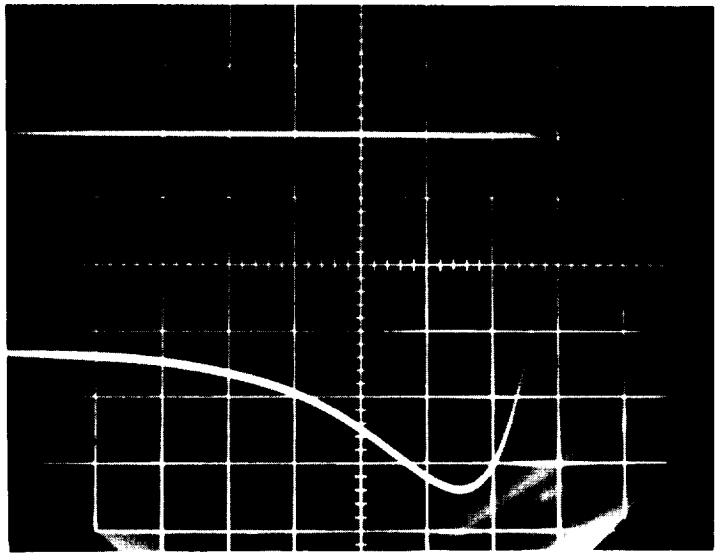


Figure 5A

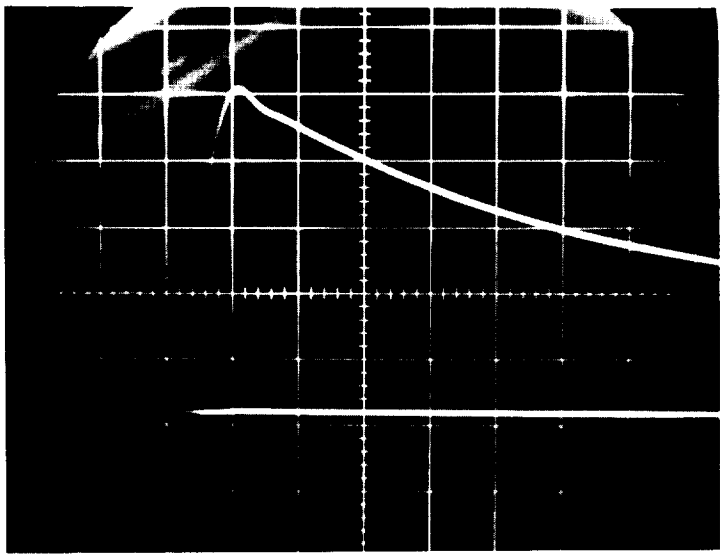


Figure 5B

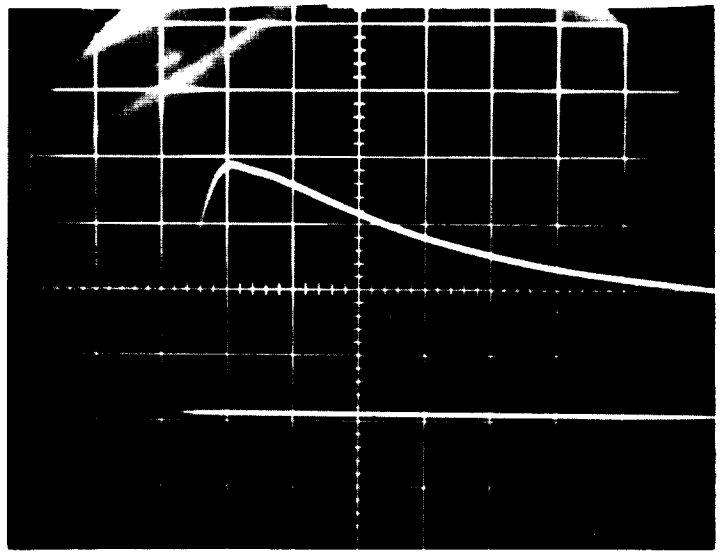


Figure 5C

INDUCED VOLTAGE RESPONSE WITH PERMALLOY CORE

	Figure 5A	Figure 5B	Figure 5C
SCALE			
Vertical	0.25 V/turn/div.	0.1 V/turn/div.	0.2 V/turn/div.
Horizontal	1.0 μ s/div.	1.0 μs/div.	1.0 μs/div.
DRIVE CONDITIONS			
Constant	N=2T	N=5T	N=5T
	I=0.5A	I=0.1A	I=0.2A
Switch	N_s = 2T	N_s = 5T	N_s = 5T
	I_s = 1.0A	I_s = 0.2A	I_s = 0.4A

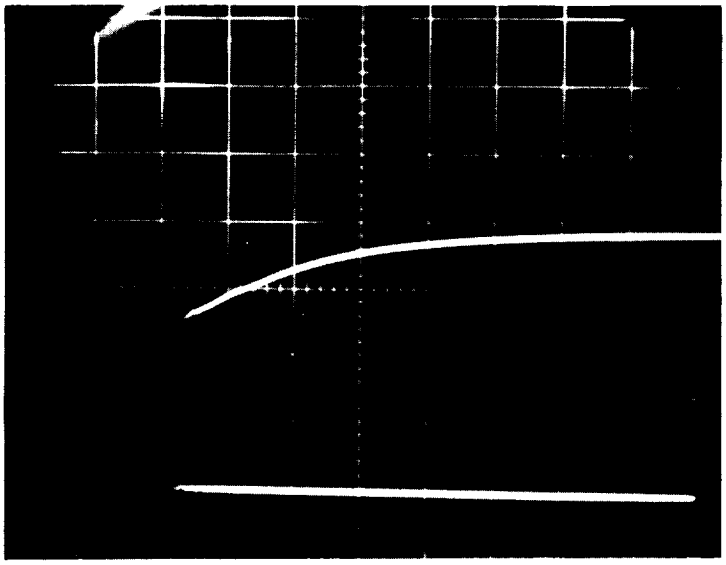


Figure 6A

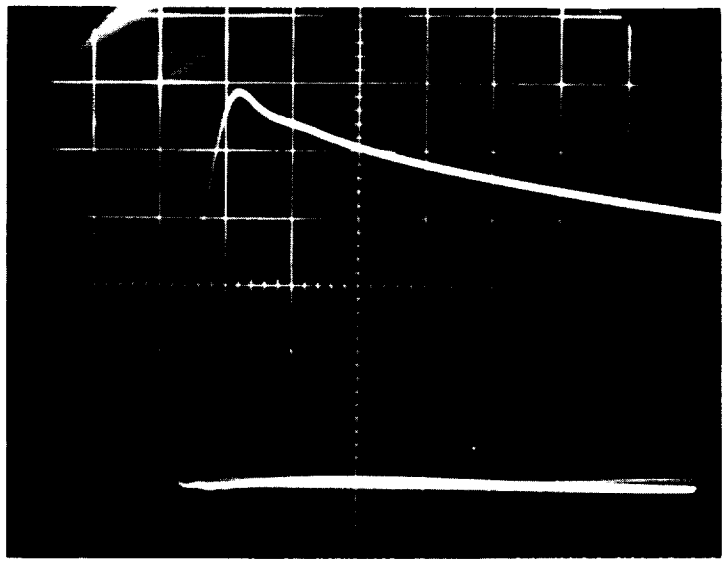


Figure 6B

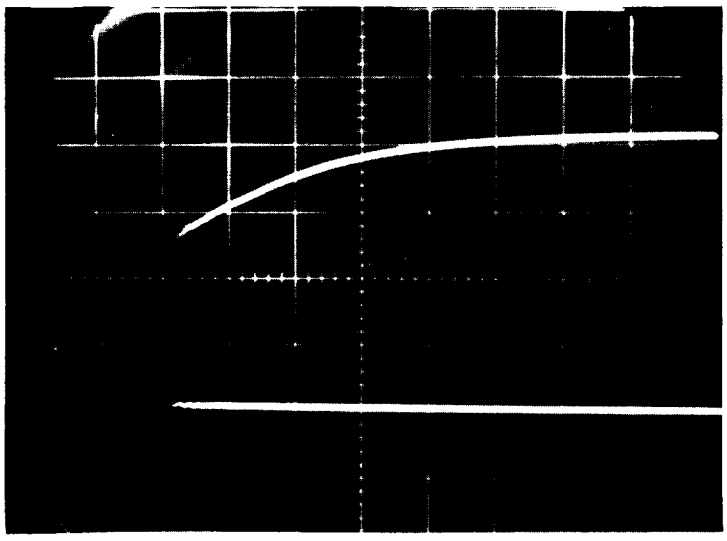


Figure 6C

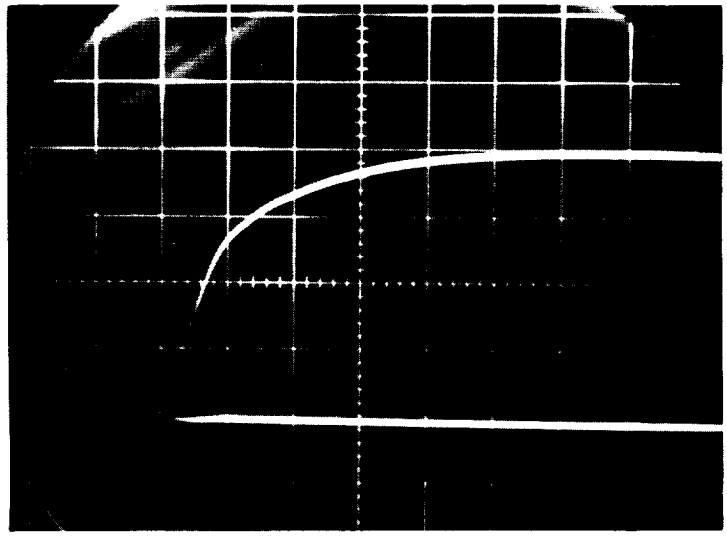


Figure 6D

EFFECTS OF LOADING A PERMALLOY CORE DURING CURRENT SWITCHING

	Figure 6A	Figure 6B	Figure 6C	Figure 6D
Title	Switching Current vs. Time	Induced Voltage vs. Time	Switching Current vs. Time	Induced Voltage vs. Time
Scale				
Vert.	20 mA/div.	25 mV/turn/div.	20 mA/div.	5 mV/turn/div.
Horiz.	1 μ s/div.	1 μ s/div.	1 μ s/div.	1 μ s/div.
Constant Bias	1 Amp-Turn		1 Amp-Turn	
Switching Turns	20T		20T	
Sense Turns	20T (No Load)		20T (4.7 Ohm Load)	
Remarks		Response of Figure 6A drive		Response of Figure 6C drive

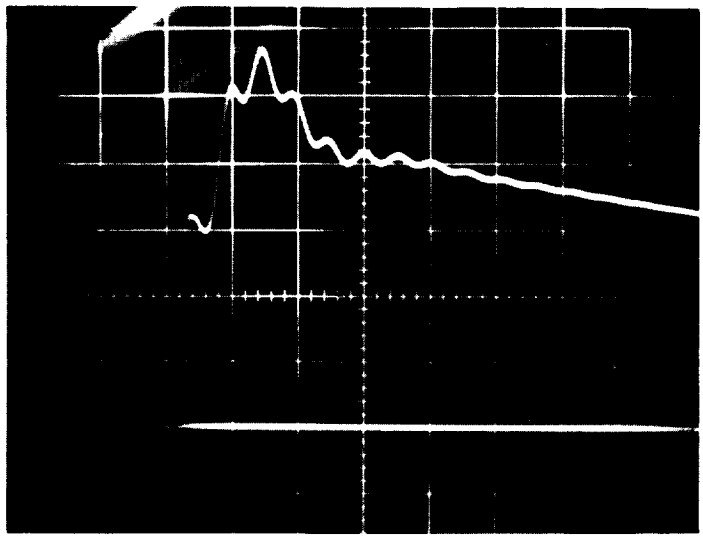


Figure 7A

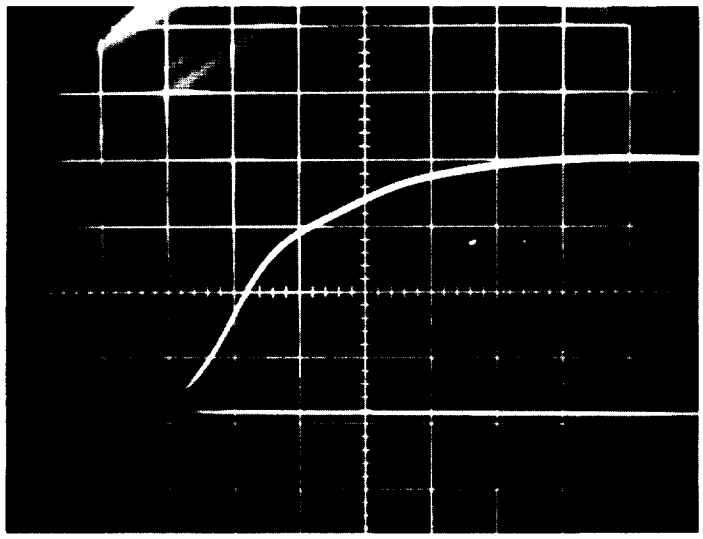


Figure 7B

EFFECTS OF LOADING A FERRITE CORE DURING CURRENT SWITCHING

	Figure 7A	Figure 7B
Title	Induced Voltage vs. Time	Induced Voltage vs. Time
Scale		
Horiz.	50 mV/turn/div.	10 mV/turn/div.
Vert.	1.0 μs/div.	1.0 μs/div.
Constant Bias	2 Amp-Turns	2 Amp-Turns
Switching Turns	20T	20T
Switching Current	0.2A	0.2A
Sense Turns	20T (No Load)	20T (4.7 Ohm Load)

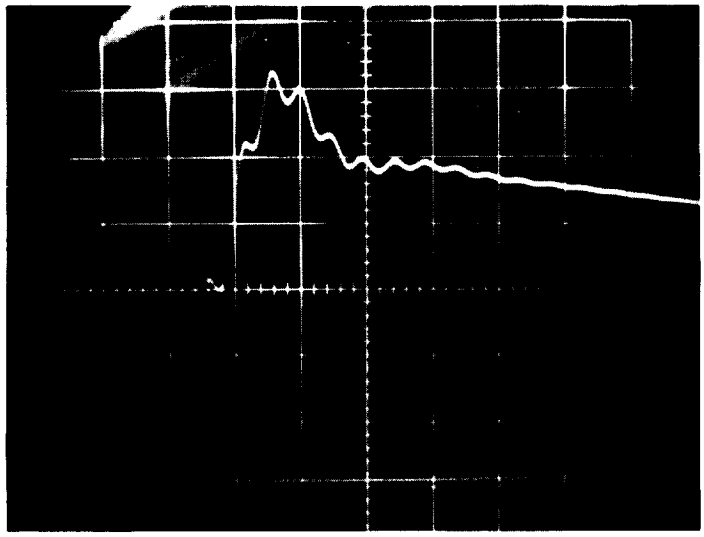


Figure 8A

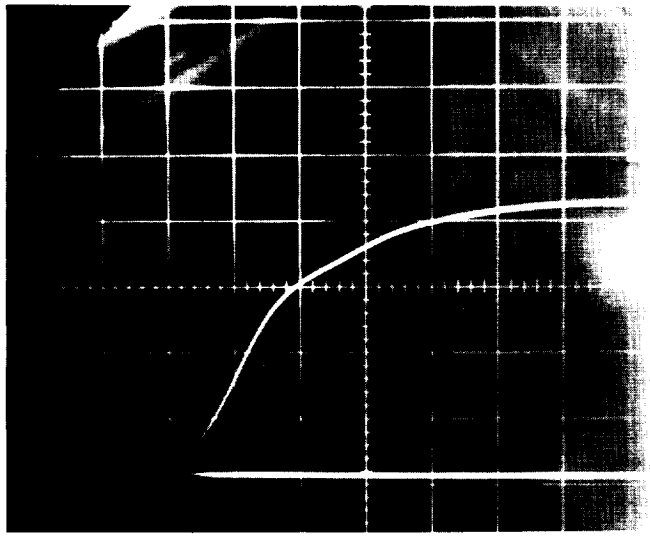


Figure 8B

EFFECTS OF LOADING A FERRITE - PERMALLOY CORE DURING CURRENT SWITCHING

	Figure 8A	Figure 8B
Title	Induced Voltage vs. Time	Induced Voltage vs. Time
Scale		
Vert.	50 mV/turn/div.	10 mV/turn/div.
Horiz.	1.0 μs/div.	1 μs/div.
Constant Bias	2 Amp-Turns	2 Amp-Turns
Switching Turns	20T	20T
Switching Current	0.2A	0.2A
Sense Turns	20T (No Load)	20T (4.7 Ohm Load)

transistor and switches the formerly non-conducting transistor on. To switch the induced voltage in feedback transformer T1, it is necessary to override the total ampere turns induced in T1 by the positive feedback ampere turns inherent in windings N1A or N1B. Thus, the recycle surge ampere turns in winding N3 on T1 must exceed the inherent positive feedback ampere turns provided by windings N1A or N1B on T1. To accomplish this, the capacitor C1 must have sufficient charge so that it can override this inherent positive feedback signal for a duration sufficient to switch the oscillator. The net current through winding N3 consists of the capacitor discharge current plus the value of quiescent current which is flowing through impedance Z1 at the instant the four layer diode D1 fires. If the impedance Z1 is high then nearly all of the recycling energy must be provided by the discharge of capacitor C1. If the impedance of Z1 is low at the time the four layer diode breaks over, then a considerable portion of the overriding signal can flow from winding N3 on the power transformer T2 through impedance Z1. Experiments have shown that it is difficult to override and synchronize a current feedback power oscillator because the inherent positive current feedback provides a considerable amount of overdrive. Thus, to override the positive signal it is necessary to store a considerable quantity of energy in the capacitor. Experiments have shown that effective synchronization can be accomplished if the impedance Z1 falls to a very low value prior to the firing of the four layer diode D1. This then allows not only the energy stored in the capacitor C to be dumped into the T1, N3 override winding but also it allows a considerable amount of energy to flow from T2 N3 into the feedback transformer winding N3. Although a very positive synchronization was achieved when the impedance of Z1 was low just prior to switching, it also has a disadvantage in that the power oscillator is loaded by the low impedance.

(2) Four-Layer Diode With Inductor-Capacitor Timing - When a saturable reactor is used for Z1, the impedance remains high until Z1 saturates and the sudden reduction in impedance allows the capacitor C1 to be charged rapidly. During this interval the oscillator is loaded excessively and the power

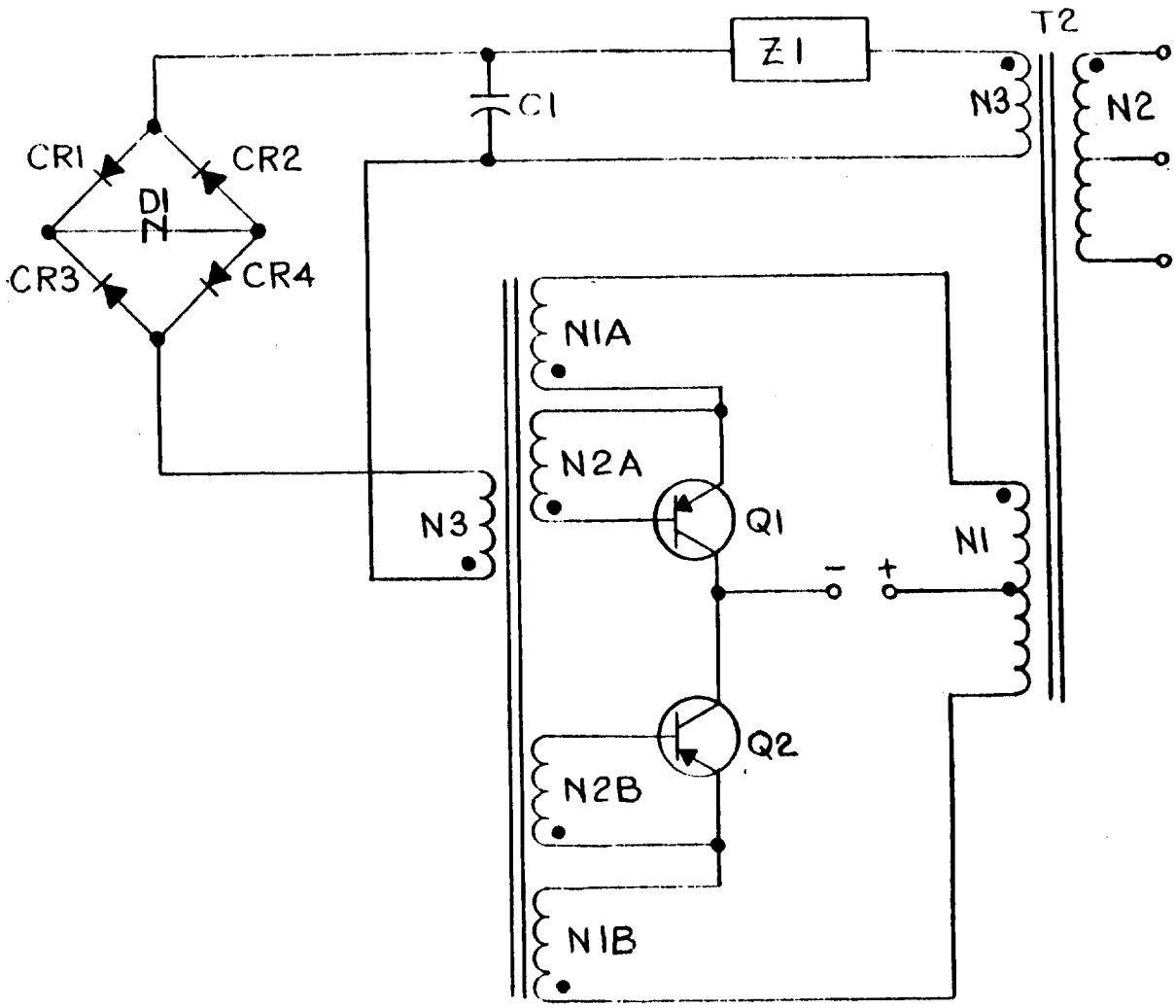


Figure 9 - CIRCUIT DIAGRAM OF LIVC WITH FOUR-LAYER DIODE SWITCH

oscillator transistors come out of saturation for an appreciable duration. This increases the oscillator losses. When the capacitor voltage builds up to the breakdown voltage of D1, the four-layer diode fires and dumps not only the capacitor charge but also allows the negative feedback from winding N3 to flow through Z1 into the feedback transformer winding N3. This provides a very positive override of the inherent positive feedback signal and accomplishes positive switching. The switching is also very rapid hence the actual switching losses are very low; however, since the transistors come out of saturation for an appreciable period just prior to switching this tends to increase the over-all circuit losses. Because of this, it is necessary to make further investigations to improve the over-all switching characteristics.

(3) Four-Layer Diode with Two Inductors-Capacitor Timing - Experiments have been conducted using two inductances in place of a single inductance Z1. As shown on Figure 10, one inductance L1 had square loop characteristics which provided an initial high impedance to the flow of current, the other inductance L2 contained a powdered permalloy core and had a much lower inductance; however, it would not saturate. In using the combination of the two inductances the main timing function was provided by the saturable core reactor. After this core would saturate the capacitor would then be charged through the smaller inductor having linear characteristics. This diminished the loading of the power oscillator during intervals when the capacitor was being charged because the smaller inductor L2 maintained an impedance in series with the charging current path. When the capacitor voltage reached a level which would break over the four layer diode, the capacitor then discharged through the diode network into winding N3 to recycle the circuit. The amount of current which could flow directly from the power transformer winding N3 into the feedback transformer winding was limited by the value of inductance of the nonsaturating reactor L2. Thus, this approach diminished the loading of the oscillator just prior to the switching interval; however, it also diminished the amount of negative feedback which could be fed directly from the power transformer to the feedback transformer.

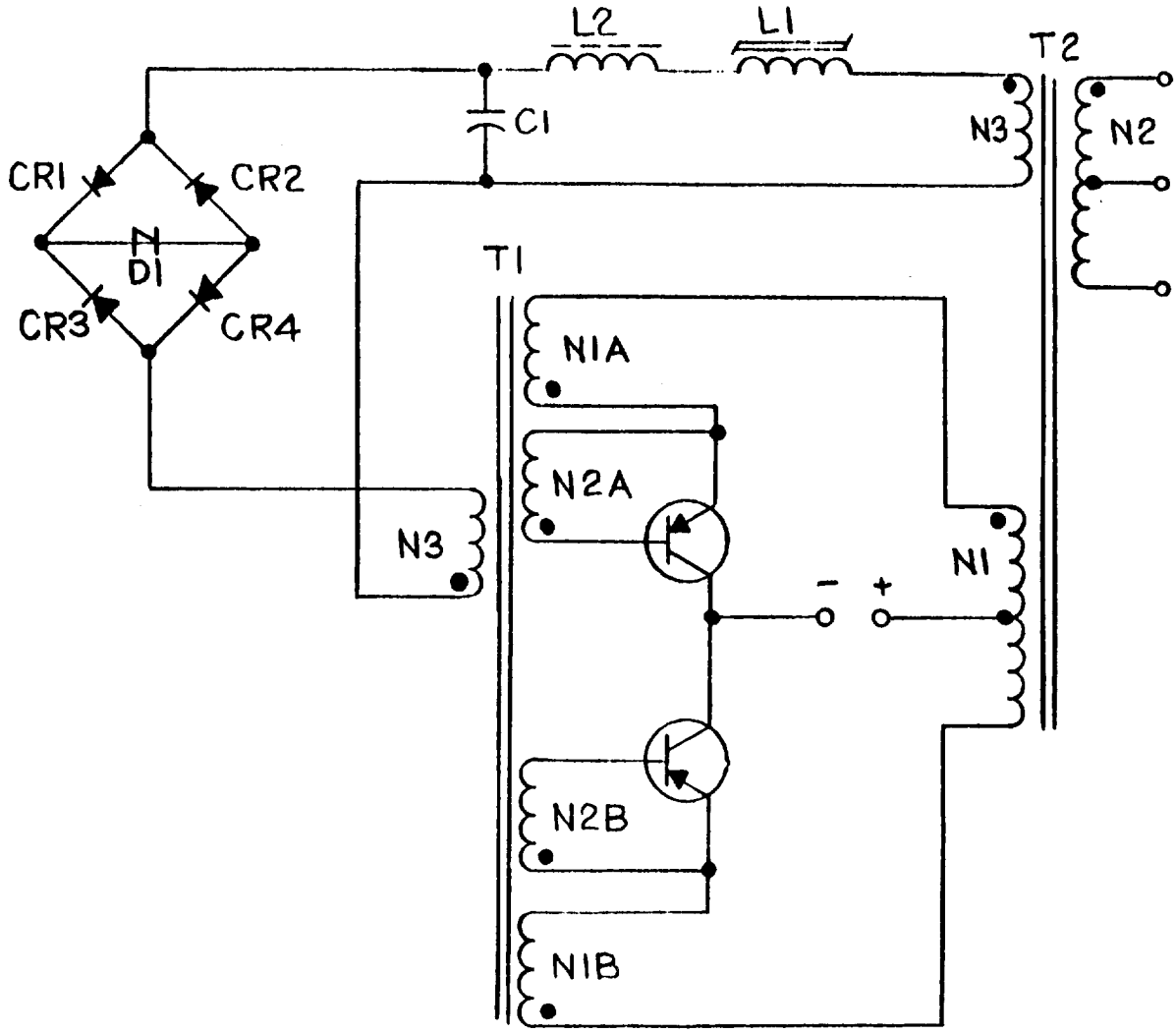


Figure 10 - CIRCUIT DIAGRAM OF LIVC WITH TWO REACTORS INCORPORATED IN THE FOUR-LAYER DIODE RECYCLING NETWORK

Although the recycling function was obtained, the switching characteristics was not as good as in the previous mode and not as reliable under various circuit parameter changes. This arrangement reduced the transistor saturation losses by diminishing the tendency of the device to come out of saturation just prior to switching; however, the fact that the power available for overriding the inherent feedback of the oscillator was lower tended to diminish the positive recycle action and this resulted in less reliable frequency control and it also resulted in an oscillation during the switching interval which increased the switching losses.

In summary, the preliminary experiments with the four layer diode approach to frequency control have shown that this method can be used successfully. However, the initial experiments have disclosed some problems with the approaches used. These problems have been due to the loading of the oscillator just before the four layered diode is initiated and the difficulty in getting sufficient power transfer from the capacitor that has been used in the timing circuit. Thus these experiments have shown that the major problems have been primarily due to the type of timing circuit used in controlling the four layer diode. Because the four layer diode does have desirable characteristics, it is therefore necessary to develop a timing circuit which would trigger the four-layer diode and provide the desired timing function without loading the power oscillator prior to switching.

(e) Approaches Suggested for Future Investigation - During the next interval, switching speed investigations will be expanded to include arrangements which utilize two four-layer diodes in place of a single diode and a bridge network. The circuit with a single four layer diode (Figure 9) has occasionally shown a condition in which the four-layer diode does not cease conduction at the end of the half cycle.

During the initial portion of the switching interval, both the power transformer winding N3 and the feedback transformer winding N3 cause the recycle current to flow. As the device switches, the feedback transformer induced voltage can reverse diminishing the forcing E. M. F. Also the secondary T2 N3 voltage can decline to a low value due to the transistor coming out of saturation. A point is reached during this transistion where the T2 N3 voltage is very low.

If the sum of the induced voltages of the two transformer windings passes through zero rapidly, due to the voltage reversal on either or both, it may be possible for the four-layer diode to maintain conduction while the current shifts to the opposite diodes in the bridge circuit. When this condition occurs, the degenerative feedback would delay switching, cause an oscillation during switching, or stop the oscillator.

To avoid this condition, two four-layer diodes (D1 and D2) can be used and arranged as shown in Figure 11. Steering diodes CR1 and CR2 are used to insure the firing of the proper diode. With this circuit, current can flow in only one direction when either four layer diode breaks over and a current reversal would shut off the diode.

With the arrangement of Figure 11, a separate timing circuit consisting of winding N4 on T2, saturable reactor L1, and impedance R1 can be used to alternately fire the four layer diodes D1 and D2. Since the timing function is separated from the negative feedback recycling current path, the energy and size of components required for timing are much smaller than the Figure 9 configuration where the recycling energy flows through the timing circuit.

Preliminary experiments are currently being conducted on this circuit and will be discussed in more detail in the next quarter's report. Another aspect which should receive further analysis is the determination of the effects of the magnitudes of positive feedback and negative recycling feedback upon the power oscillator switching characteristics.

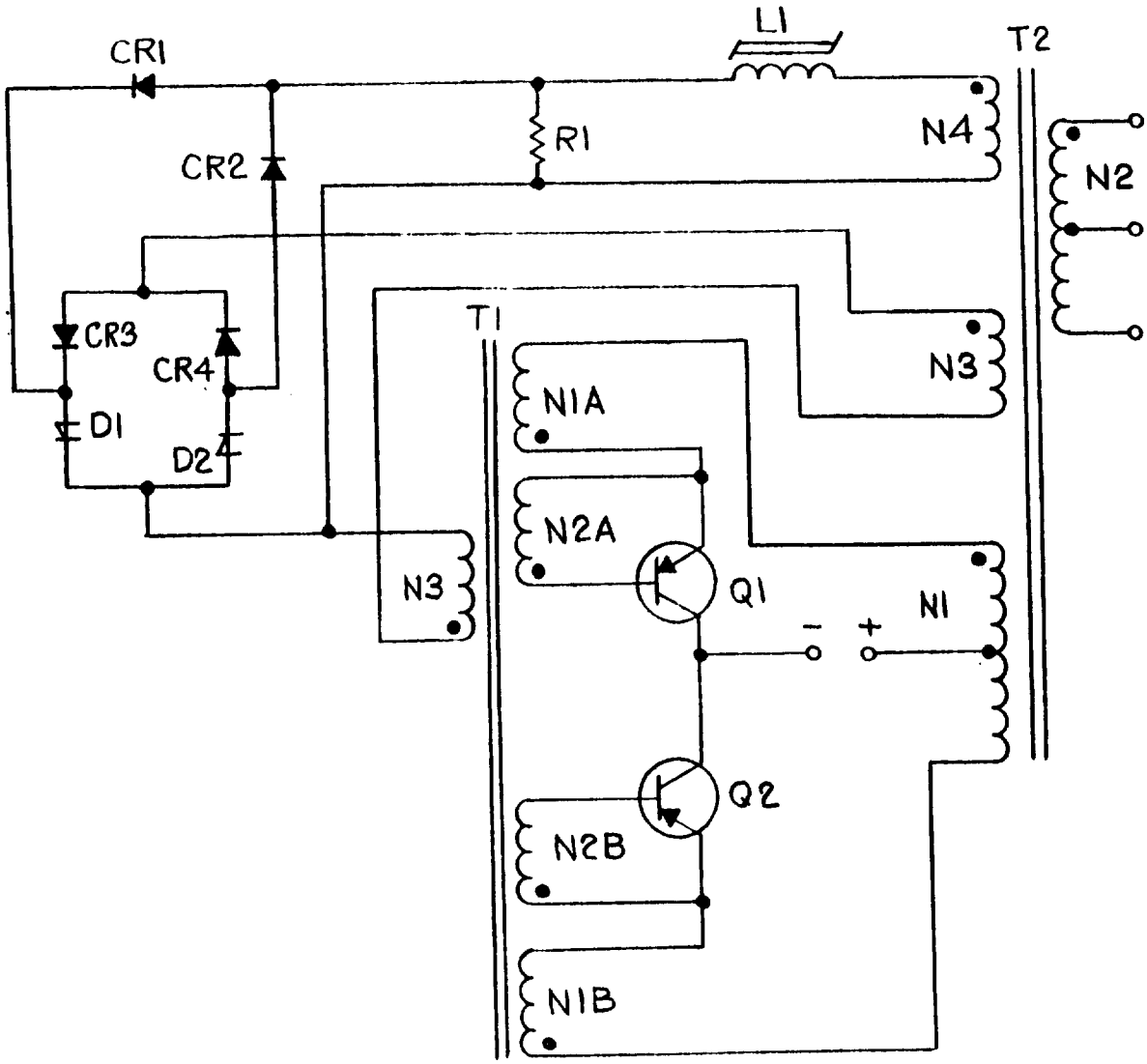


Figure 11 - CIRCUIT DIAGRAM OF LIVC WITH TWO FOUR-LAYER DIODES SERVING AS THE RECYCLING SWITCH

It can be concluded that the initial results have shown some promising results in that with certain circuits positive synchronization or switching could be achieved, and that when the four-layer diode was switched rapid switching can also be obtained, providing that the recycle source could provide sufficient power to override the inherent positive feedback. During the next quarter, methods of triggering and timing the four layer diode will be investigated. Effort will be directed towards achieving the triggering and timing without loading the source and providing a low impedance path from the power transformer winding N3 directly to the four-layer diode and then into the feedback transformer N3 winding. These experiments will be directed towards the use of a separate timing circuit which will apply a pulse across the four layer diode to trigger it and towards the use of two four layer diodes instead of the bridge network with a single four layer diode.

2. Redundant LIVC Synchronization

The synchronization of redundant LIVCs is a present design consideration and is a subject of laboratory testing. The redundant LIVCs may be operated from a common source and/or into a common load. Synchronization is desirable because it reduces any tendency for the LIVCs to oscillate or "beat" against each other when so connected. Specifically, the synchronization eliminates the very low frequency ripple components which are generated by the beating of two unsynchronized converter oscillators. The beating is undesirable because the resulting low frequency ripple is very difficult to remove by filtering. Breadboard systems have been fabricated and various synchronization schemes are being evaluated in the laboratory.

Several necessary considerations in the synchronization design are discussed in the following paragraphs.

If the LIVCs are operating from separate sources, the synchronized frequency must be high enough to avoid saturation of individual LIVC transformer cores under all combinations of respective input voltages. For example, the situation may arise where one LIVC has a higher input voltage than the other. (This would be possible for a regulated redundant LIVCR.) It follows that for identically designed output transformers and a synchronized operating frequency, the flux density in the power transformer with the greatest input voltage will be higher. Therefore, the synchronized frequency must be high enough to avoid saturation of that power transformer. This is necessary even though it results in lower than usual flux densities in the power transformer with the lower input voltage. Operation at the frequency dictated by the highest input voltage results in increased switching losses in the LIVC with the lower input voltage, but avoids those high input current spikes characteristic of output transformer saturation. If the output transformer of one were allowed to saturate under these conditions of unequal input voltage, additional circuitry would be necessary to maintain synchronization. Normally it is felt that to achieve high efficiencies, the synchronous frequency should be a function of the input voltage and controlled by some means other than saturation of the output transformer. When operating from separate but nearly identical high impedance sources, the input voltages tend to balance equally because of load sharing tendencies. Possible changes in source characteristics, etc. however make it necessary to include the condition of unequal source voltages.

The individual LIVCs should be designed so that under conditions of very light load they can maintain operation. If light load operation is not considered, a LIVC may turn off because of insufficient current drive to maintain conduction. Because the parameters of the transistors in the respective LIVCs may be different, auxiliary circuitry may be necessary to maintain synchronous operation under this light load operation. By carefully designing the individual LIVCs, such auxiliary synchronous circuitry for light load operation may be avoided.

The synchronization circuitry should be incorporated in a manner that does not decrease the reliability of the redundant LIVC combination. Because a synchronization circuit must provide some link between redundant systems, precaution must be taken so that it does not also detrimentally link any possible failure of a single system into the redundant combination. Those possible failures include (1) source failures resulting in a short or open on an individual input and (2) LIVC failures which could result in effectively shorted or open windings on transformers in the synchronous link.

The synchronous link should be designed so that (1) the basic frequency control for the operating redundant LIVCs is not destroyed by an individual system failure and (2) an individual failure does not adversely load the operating redundant LIVCs through the synchronous link.

The LIVC synchronization circuit shown on Figure 12 is one scheme presently being investigated in the laboratory. For this investigation, the LIVCs are being operated from sources having output characteristics similar to a thermo-electric generator. The LIVCs are unregulated and are operating into resistive loads. Several source-load combinations have been investigated but the most emphasis is being placed on operation into a common load from separate and common sources respectively. Of these two modes of operation, the operation of separate source LIVC combinations into a common load poses the most difficult problem for reliable synchronization. The circuit presented in Figure 12 has operated quite well under these conditions and thus was chosen for this discussion. Each of the two converter circuits shown has an independent frequency determining network sensitive to the respective input voltage of the individual converters. These independent frequency determining networks are identical to those used on previous LIVCs. They are composed of windings on the power transformers in series with a saturating inductor which when saturated introduces negative feedback to switch the converter. The synchronization link is provided by windings on the two respective current feedback transformers and the inductor L2. The current feedback transformer windings in the synchronous

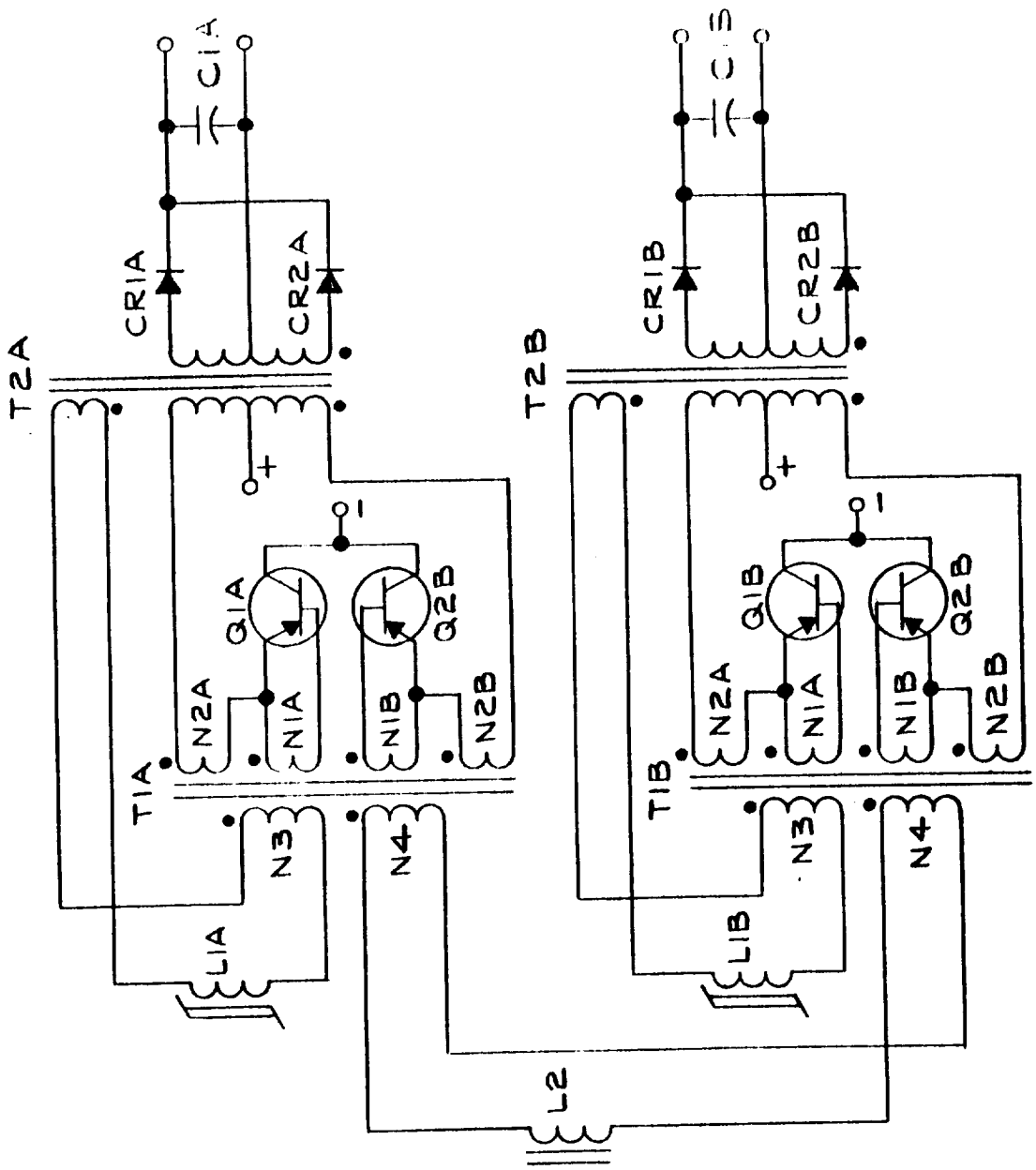


Figure 12 - LIVC SYNCHRONIZATION CIRCUIT

link are connected so that their nearly equal respective voltages subtract to determine the voltage across inductor L2 between switching operations. When one of the converters is switched, the voltage across its current feedback transformer winding N4 is reversed and the voltage across inductor L2 is increased. When inductor L2 saturates, this introduces a switching signal to winding N4 on the current feedback transformer for the redundant LIVC. Thus synchronization is realized with the phase shift of the synchronization determined by the size of the inductor L2. The incorporation of the inductor L2 provides a variable phase shift control and limits the current in its series path except when saturated. This current limiting feature is one of the main advantages of the circuit as it does not require excessive power when the respective input voltages are different. Also the synchronized operating frequency is determined by the converter with the highest independent frequency. Another desirable feature of this circuit is that the synchronization link can be introduced or removed without disturbing the wiring of the individual LIVCs.

This circuit will be investigated further to work out any problems which may occur during continued laboratory testing and analysis.

Alternatives to this circuit and other circuits will be considered during the program to arrive at a suitable synchronization scheme.

3. Redundant LIVC Common Output Load Sharing

The operation of redundant unregulated LIVCs into a common load causes the input voltages as well as the output load voltage to be equal if all redundant LIVCs are contributing power to the load. If the LIVCs are operating from a common source, the equal voltages are of course forced by the common connections. If the LIVCs are operating from separate sources, the equal input voltages are forced by the reflection of the load voltages through respective LIVC transformers (assuming identical transformers). The condition of equal

input and output voltages has considerable significance in determining the load sharing in the redundant LIVCs. When operating from a common source, the load sharing is very nearly equal if the LIVCs have approximately the same efficiency. When operating from separate sources, the load sharing is very much dependent on the individual source characteristics.

Two redundant LIVCs will be assumed in discussing the load sharing when operating from separate sources into a common load. Generally we can say that the load sharing will be dependent on the individual source characteristics and that operating voltages at which the load requirements and the sources' capabilities are equal. This is discussed in more detail in the following analytical discussion and is shown in Figure 13 for a specific load of 100 milliohms. Note that more power is delivered to this fixed resistive load when two sources are operated redundantly. The following discussion is presented assuming that the resistive load on the source is that load presented by the LIVC-output resistor combination.

An analytical consideration of the load sharing resulting when a resistive load is powered by high impedance, redundant sources may be made by first considering the characteristics of Figure 13. The characteristics presented may be typical of two identical thermoelectric generators operating at different temperatures. It is assumed they have the same source impedance and that this impedance is purely resistive. Therefore, it follows that

$$V_1 = m (I_{m1} - I_1) \tag{1}$$

and

$$V_2 = m (I_{m2} - I_2). \tag{2}$$

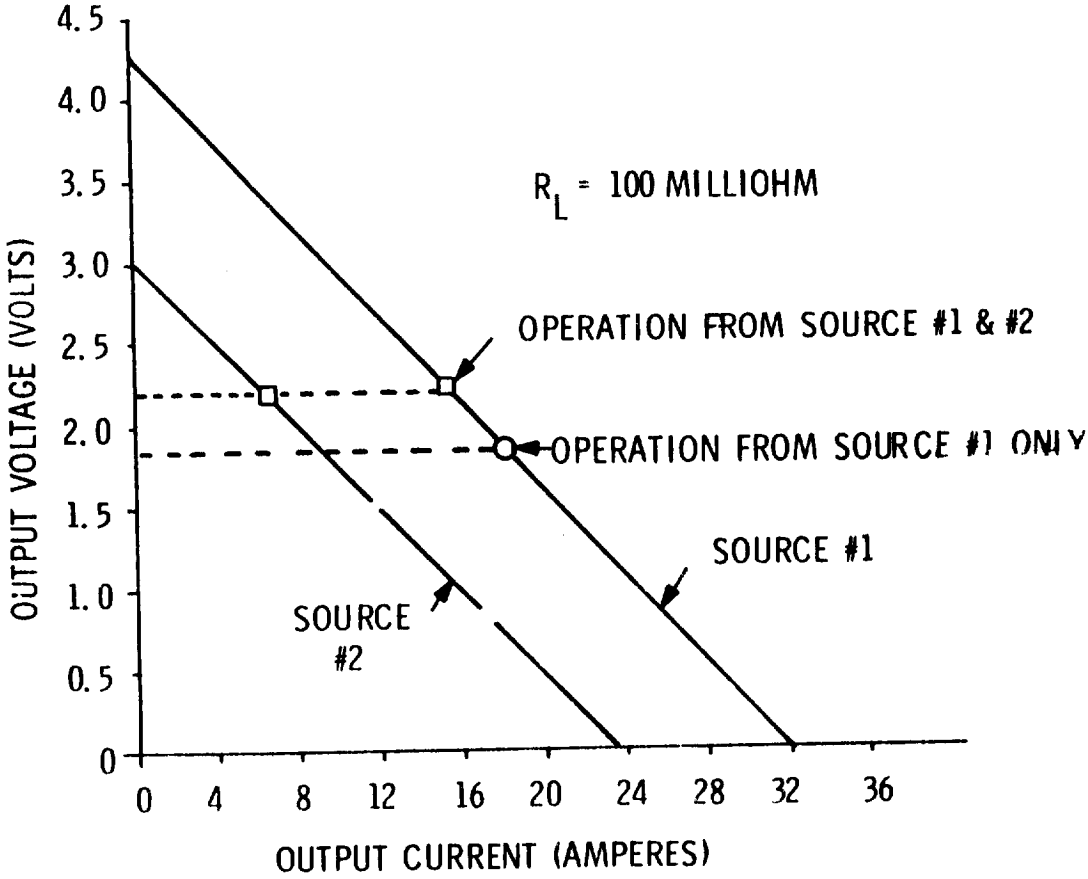


Figure 13 - THERMOELECTRIC GENERATOR SOURCE CHARACTERISTICS AND COMMON OUTPUT LOAD SHARING

Where m = source impedance

V_1 = terminal voltage of source 1

V_2 = terminal voltage of source 2

I_1 = output current of source 1

I_2 = output current of source 2

I_{m1} = maximum current of source 1 characteristic

I_{m2} = maximum current of source 2 characteristic.

Case I.

It may be of interest to first consider powering a resistive load from only source 1. The following equations then hold

$$\frac{V_1^2}{R_L} = V_1 I_1 \tag{3}$$

where R_L = resistive load

$$\text{or} \quad \frac{V_1}{R_L} = I_1 = \frac{m(Im_{i1} - I_1)}{R_L} = \frac{mB}{R_L} \tag{4}$$

where $B = Im_1 - I_1$

$$\text{or} \quad I_1 = \frac{mIm_1}{R_L} \quad \frac{1}{m/R_L + 1} = \frac{Im_1}{1 + R_L/m} \tag{5}$$

Case II.

Considering operation from two redundant sources into a common load, we see first that

$$V_1 = V_2 \tag{6}$$

$$\text{or} \quad m(Im_1 - I_1) = m(Im_2 - I_2) \tag{7}$$

$$\text{and} \quad Im_1 - I_1 = Im_2 - I_2 \tag{8}$$

The power equations then must be

$$\frac{V_1^2}{R_L} = V_1 I_1 + V_2 I_2 = V_1 (I_1 + I_2) \tag{9}$$

This can be reduced to

$$\frac{V_1}{R_L} = I_1 + I_2 \tag{10}$$

Now solving for I_1 by substituting equations (1) and (8) into (10) we get

$$\frac{m(Im_1 - I_1)}{R_L} = 2 I_1 + Im_2 - Im_1 \tag{11}$$

$$\text{or} \quad I_1 = Im_1 \frac{m + R_L}{2R_L + m} - Im_2 \frac{R_L}{2R_L + m}$$

$$= \frac{1 + R_{L/m}}{1 + 2R_{L/m}} - Im_2 \frac{R_{L/m}}{2R_{L/m} + 1} \tag{12}$$

Likewise I_2 can be solved for

$$I_2 = Im_2 \frac{1 + R_{L/m}}{1 + 2R_{L/m}} - Im_1 \frac{R_{L/m}}{2R_{L/m} + 1} \quad (13)$$

Comparing the deviation from the maximum current possible from each source, we find that in Case I referring to equations (4) and (5)

$$B^{(I)} = Im_1 \frac{R_L}{m + R_L} \quad (14)$$

For Case II, referring to (11),

$$B^{(II)} = (Im_1 + Im_2) \frac{R_L}{2R_L + m} \quad (15)$$

Note that if the value of B (defined as the deviation of the operating current from the maximum current of the characteristic) for Case II is larger than Im_2, no load power will be delivered by source #2.

The same analysis is valid when considering powering the resistive load from the same sources but through redundant LIVCs. The only modification necessary will be the inclusion of the power transformer turns ratio and the inefficiency of the LIVCs.

4. Redundant Source-Converter Combination Reliability Trade-Offs

One of the prime objects of this program is to determine the optimum redundant source-converter configuration to provide a reliable power system for a three year space mission.

Power supply reliability is a very important factor in the achievement of the three year operating lifetime power requirements. Therefore, special consideration has been given to minimize equipment failure in a preliminary analysis of source-converter combinations. This preliminary analysis was conducted utilizing the following:

Assume:

1. No degradation is allowed (i. e. no failures)
2. 50% degradation is allowed (i. e. system can provide 50% of rated output)
3. Reliability of the individual sources is equal to the reliability of the individual converters = 0. 90
4. Twelve (12) sources are required with a maximum number of six (6) converters allowed.

Equation:

$$R = \sum_{j=o}^{K-1} \frac{N!}{j!\,(n-j)!} (1-R_s{}^n . R_c)^j (R_s{}^n . R_c)^{N-j}$$

Where:

R = Source-converter reliability for a given amount of degradation allowed.

K-1 = Allowable number of parallel element failures without incurring loss of the system function

j = Number of element failures occurring

N = Number of parallel elements (or strings)

R_s = Reliability of the individual source

R_c = Reliability of the individual converter

Six cases were considered; two each for 2.2 volts, 4.4 volts and 6.6 volts. Results are presented in Table 1 with the configurations and corresponding equations shown in Figure 14A and 14B.

Additional analysis will be conducted to determine the optimum source-converter combination with special emphasis given to predominant failure modes as applicable to power supply reliability.

TABLE 1

SOURCE-CONVERTER RELIABILITY - PRELIMINARY TRADE-OFF STUDIES

Example	Source Voltage	No Degradation Allowed Reliability	MTBF	50% Degradation Allowed Reliability	MTBF
Case I	2.2 V	$R \cong .151$	1.59 years	$R \cong .985$	198.7 years
Case II	4.4 V	$R \cong .151$	1.59 years	$R \cong .953$	62.4 years
Case III	6.6 V	$R \cong .185$	1.78 years	$R \cong .880$	23.5 years
Case IV a	2.2 V	$R \cong .229$	2.04 years	$R \cong .900$	28.5 years
IV b	2.2 V	$R \cong .185$	1.78 years	$R \cong .996$	747.7 years
Case V	4.4 V	$R \cong .185$	1.78 years	$R \cong .983$	175.2 years
Case VI	6.6 V	$R \cong .185$	1.78 years	$R \cong .933$	43.4 years

Where:

$R = e^{-\lambda t}$

$\lambda = \frac{1}{m}$

$m = \frac{t}{\ln R}$

t = 3 years.

R = Reliability

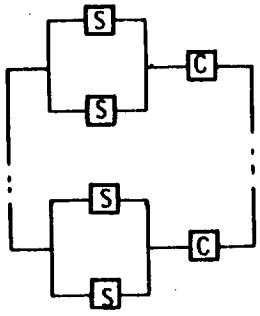
m = M. T. B. F. (meantime between failure)

λ = Failure rate.

Table 1 shows that if the reliability of the individual source and individual converter modules is 0. 90 then the MTBF of the system composed of twelve sources and various numbers of converters will range between 1. 59 and 2. 04 years if 100% performance is required of each module to furnish 300 watts of power at the end of the three year mission. Thus each module has an MTBF of 28. 5 years but if they are incorporated into a system and all modules are required for mission success then the MTBF is much lower as indicated. However, it is anticipated that this satellite power system will contain storage batteries and it will be possible to achieve mission objectives with much less power than the continuous 300 watts. Thus mission objectives can probably be achieved with only 50% of the original power by reducing the frequency at which heavy power drains are required toward the end of the three year mission. This may mean that certain experiments are performed or monitored only a few times per orbit at the end of the three year mission in place of several times per orbit. If the power capability of the redundant source - redundant cover system is allowed to diminish to the 50% level after three years then the mean time between failures for the configurations considered in Table 1 will range between 23. 5 years and 747. 7 years.

It can be concluded from the assumptions made and the initial analysis that some degradation in performance should be allowed after the three year mission in order to obtain an MTBF sufficiently high to accomplish mission success. If the reliabilities of the individual modules is 0. 9 then a 50% degradation is much more than required; hence, a 25% degradation maybe sufficient. It will be necessary to examine these aspects in greater detail next quarter and, in conjunction with this attempt to determine if a reliability of 0. 9 per module is a realistic assumption or if other values should be used for the source and the converter.

CASE I - 2.2 VOLTS



12 SOURCES 6 CONVERTERS

NO DEGRADATION ALLOWED

$R = (R_S^2 R_C)^N = R_S^{18}$

$R = 0.1508$

50% DEGRADATION ALLOWED

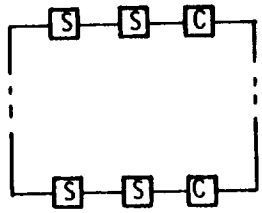
$R = R_{S-C}^6 + 6QR_{S-C}^5 + 15Q^2R_{S-C}^4 + 20Q^3R_{S-C}^3$

WHERE: $R_{S-C} = \left[R_S^2 + R_S(1-R_S)\right] R_C$

$Q = 1-R_{S-C}$

$R = .9852$

CASE II - 4.4 VOLTS



12 SOURCES 6 CONVERTERS

$R = (R_S^2 R_C)^N = R_S^{18}$

$R = 0.1508$

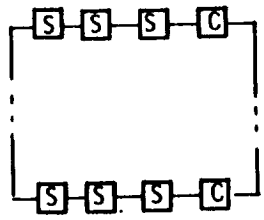
$R = R_{S-C}^6 + 6QR_{S-C}^5 + 15Q^2R_{S-C}^4 + 20Q^3R_{S-C}^3$

WHERE: $R_{S-C} = R_S^2 R_C$

$Q = 1-R_S^2 R_C$

$R = .9526$

CASE III - 6.6 VOLTS



12 SOURCES 4 CONVERTERS

$R = (R_S^3 R_C) = R_S^{16}$

$R = .1853$

$R = R_{S-C}^4 + 4QR_{S-C}^3 + 6Q^2R_{S-C}^2$

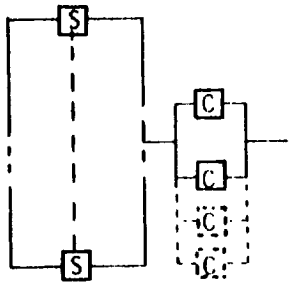
WHERE: $R_{S-C} = R_S^3 R_C$

$Q = 1-R_S^3 R_C$

$R = .8799$

Figure 14 - REDUNDANT SOURCE CONVERTER COMBINATIONS (2 Pages)

CASE IV - 2.2 VOLTS



(A) 12 SOURCES 2 CONVERTERS
(B) 12 SOURCES 4 CONVERTERS

NO DEGRADATION ALLOWED

CASE IV A. $R = R_S^{12} R_C^{2} = R_S^{14}$

$R = 0.2288$

CASE IV B. $R = R_S^{12} R_C^{4} = R_S^{16}$

$R = 0.1853$

50% DEGRADATION ALLOWED

$R = (R_S^{12} + 12 R_S^{11} Q + 66 R_S^{10} Q^2 + 220 R_S^{9} Q^3 + 495 R_S^{8} Q^4 + 792 R_S^{7} Q^5 + 814 R_S^{6} Q^6)$

$\bullet \left[R_C^{2} + R_C(1-R_C) \right]$ IN CASE IVA

OR

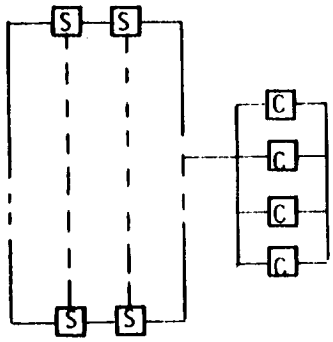
$\bullet \left[R_C^{4} + 4(1-R_C) R_C^{3} + 6(1-R_C)^2 R_C^{2} \right]$ IN CASE IVB

WHERE: $Q = (1-R_S)$

A. $R = 0.900$

B. $R = 0.996$

CASE V - 4.4 VOLTS



12 SOURCES 4 CONVERTERS

$R = (R_S^{2})^{6} R_C^{4} = R_S^{16}$

$R = 0.1853$

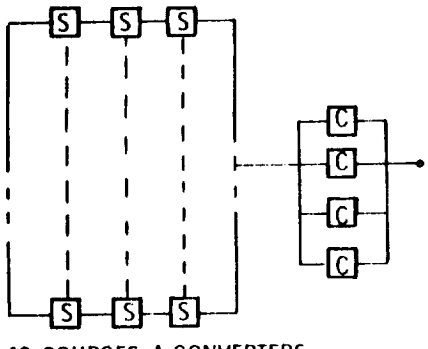
$R = \left[(R_S^{2})^{6} + (R_S^{2})^{5} Q_S + 15 (R_S^{2})^{4} Q_S^{2} + 20 (R_S^{2})^{3} Q_S^{3} \right] \bullet (R_C^{4} + 4 Q_C R_C^{3} + 6 Q_C^{2} R_C^{2})$

WHERE: $Q_S = 1 - R_S^{2}$

$Q_C = 1 - R_C$

$R = 0.9826$

CASE VI - 6.6 VOLTS



12 SOURCES 4 CONVERTERS

$R = (R_S^{3})^{4} R_C^{4} = R_S^{16}$

$R = 0.1853$

$R = \left[(R_S^{3})^{4} + 4 (R_S^{3})(1-R_S^{3}) + 6 (R_S^{3})^{2} (1-R_S^{3})^{2} \right] \bullet \left[R_C^{4} + 4 R_C^{3} (1-R_C) + 6 R_C^{2} (1-R_C)^{2} \right]$

$R = 0.9331$

Figure 14 (Continued)

SECTION II

NEW TECHNOLOGY

During this first quarter, work has been directed towards experiments utilizing four-layer diodes and new timing circuits to provide more rapid application of negative feedback and increase the power oscillator switching speed. This work is still in the experimental stage and is adequately described in Section I: C:1:d of this report. Additional experiments have been directed towards circuitry to synchronize two current feedback power oscillators and this work is discussed in detail under Section I: C: 2. of this report.

It must be pointed out that these circuit investigations are still in the experimental stage and further testing and modifications may be required to produce circuitry which can be used in practical applications.

SECTION III

PROGRAM FOR NEXT QUARTER

During the next quarter, the investigation and laboratory testing of various LIVC synchronization schemes will be continued. Emphasis will be placed on those system considerations related to the synchronization circuitry as stated in this report. Additional studies will be conducted to assure that the synchronous circuitry finally incorporated in the redundant model will result in a reliable system with a low ripple output voltage.

Further effort will be directed toward maintaining LIVC efficiency while reducing weight through higher frequency operation. Unique circuitry and core materials as well as new transistors to realize this will be subjects of design analysis and laboratory testing. In conjunction with these studies, weight-efficiency trade-offs will be made so that the advantage for a system application may be evaluated.

The reliability analysis of various redundant source-LIVC configurations initiated this past quarter will be expanded next quarter to present a more complete table of configuration reliability trade-offs.

The fabrication of a 300 watt system model using a simulated thermoelectric generator as the source will be initiated. Consideration will be given to the design or selection of manual switches which will be used to achieve the appropriate redundant connections.

SECTION IV

CONCLUSIONS AND RECOMMENDATIONS

Investigations of the power oscillator switching characteristics have shown that the base drive signals as well as the transistor characteristics determine the switching speed of the power oscillator. In the circuits utilizing high speed transistors, the rise time of the base drive signals was found to be a factor limiting the oscillator switching speed. It was concluded that the inductance of the saturated switching reactor, the leakage inductance of the recycle winding on the power transformer, the leakage inductance of the recycle winding on the feedback transformer, and the feedback transformer core switching characteristics limit the rise time of the base drive signals and diminish the power oscillator switching speed. The saturated reactor inductance and the transformer leakage inductance limits the rise time of the recycle surge current and thereby diminishes the rise time of the base drive signals. To reduce this effect it is desirable to limit the leakage inductance by evenly distributing the windings around the torroidal cores.

An investigation of the comparative switching times of Ferrite, Permalloy, and Supermalloy showed that Ferrite had the lowest switching coefficient. Supermalloy and Permalloy had approximately equal switching coefficients. The switching coefficient is defined as the incremental decrease in required switching time per incremental increase in magnetizing force. Thus the switching time of Ferrite can be decreased by a larger percentage than that of Permalloy for a corresponding increase in magnetizing force. The rise time of the individual voltage in response to a current pulse seems to be proportional to the switching coefficient. Thus for equal current drive conditions, the induced voltage with a Ferrite core has a faster rise than with a Permalloy or Supermalloy core. During the conduction of tests involving the induced voltage rise time, it was also found that the fastest rise time for a fixed amp-turn drive was obtained when the amperes to turns

ratio was the highest. This is true because fewer turns on the core resulted in lower impedance afforded by it and this in turn reduced the shaping of the pulse current wave front from the finite impedance switching current source. It is recommended that this conclusion be evaluated in the LIVC circuitry to determine if the assumption made during the core testing applies to this circuitry.

The speed of response of the induced voltage on the current feedback transformer core to a switching current pulse can be increased by increasing the ampere-turns of the switching signal. The magnitude of this pulse must be tempered, however, by a consideration of the effect it has on the saturation voltage of the power transistors. It is recommended that this be further analyzed in the LIVC circuit.

To determine if higher speed power oscillator switching characteristics can be obtained, effort has been directed towards the use of other switching elements in the oscillator recycling circuit. To date this work has been directed towards the use of four-layer diodes as the switching element. These devices have very high switching speeds and several methods of timing and triggering the four-layer diode have been investigated. The results have shown that if the timing circuit is used to pass the recycle current, then a condition exists where the power oscillator is excessively loaded just prior to switching. This causes the conducting oscillator transistor to come out of saturation for an appreciable duration just prior to switching and tends to increase the transistor dissipation. Where a single four-layer diode has been used for timing and recycling, conditions have been noted where the four-layer diode continues conduction for an appreciable period after switching. To diminish these effects, circuitry is currently being investigated which uses two four-layer diodes (to insure turn off of the diodes after recycling) and separate timing circuitry (to diminish loading of the oscillator prior to switching and to reduce the size of time circuit components).

We can conclude from the initial investigations that the four layer diode approach to frequency control and recycling appears promising and further investigation of these approaches should lead to higher oscillator switching speeds. (Actually fast switching speeds have been observed but to date the circuits which have accomplished this have had other undesirable features.) It is necessary to refine the circuitry and analyze the parameters in the positive feedback loops so that these conditions can be optimized for higher switching speeds which are necessary to increase the operating frequency, increase the efficiency, and reduce the device weight.

The initial circuit studies utilizing the four-layer diode switching element have shown promise in that faster switching has been obtained. It is therefore recommended that effort be continued in this area to determine what oscillator switching speeds can be obtained with the available transistors. In this regard it is also recommended that the magnitudes of positive and negative recycling feedback during switching should be analyzed to determine the optimum circuit parameters for fast switching.

The synchronization circuitry should be incorporated in a manner that does not decrease the increased reliability afforded by a redundant source - LIVC combination. The initial analysis and testing of synchronization circuits indicate that they can be incorporated in a manner which provides reliable synchronization and yet allows operation of a redundant LIVC after the failure of another without adverse affects. This should be studied further in the future however.

The analysis of the load sharing resulting when redundant unregulated LIVCs are operated into a common load shows that the sharing is dependent on the individual source characteristics. Assuming identical LIVCs, the power supplied by each redundant source - LIVC will be determined by the operating voltage at which the load requirements and the sources capabilities are equal. When the sources have a high impedance characteristic,as is true of the thermo-

electric generators, the power delivered to a fixed resistive load is significantly increased when the number of redundant sources delivering power is increased. The load sharing equations presented in this report should be of assistance in evaluating and predicting an redundant system performance. Additional work should be done to evaluate the load sharing when redundant regulators are also incorporated to power the then voltage regulated load.

The initial redundant configuration reliability analysis has shown that it is desirable to design the system for a slightly reduced power output at the end of the three year mission in order to achieve a satisfactory M. T. B. F. It is recommended that the degradation allowable be estimated so that the required converter and source reliabilities can be more firmly established and compared with existing technology. This will be a factor in selecting the optimum redundant configuration. It is also recommended that design of LIVCR's for the redundant system should be initiated in the next quarter.

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