A NONLINEAR ENCODER

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TECHNICAL REPORT NO. 1

Under

CONTRACT NUMBER NAS8-5341

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May 9, 1964 - September 9, 1964

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ABSTRACT

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A time-base encoding system is described which can be adapted to high precision without reaching a point of inaccurate digital representation of the reference voltage. The system uses a sinusoidal reference voltage and a counter which is capable of accumulating pulses in such a way that the encoder output is an accurate digital representation of the reference during the encoding interval. There is no need for sample and hold circuitry in this particular encoder. The design of the comparator, the clock inhibit circuit, and the nonlinear counter are discussed.

ACKNOWLEDGEMENT

This report has been prepared for the Navigation Branch, Astrionics Division, George C. Marshall Space Flight Center, Huntsville, Alabama under Contract NAS8-5341.

The authors wish to acknowledge the assistance of Professor Longino A. Woodman, Director, Bureau of Engineering Research, in handling administrative details of the work. The valuable work of Mr. Hubert T. Nagle and Mr. David P. Nicolas, graduate research assistants, in drawing the figures and performing the necessary experimental procedures presented herein is gratefully acknowledged. Also, the authors are particularly grateful to Mr. Hugh Taylor and Mr. George Kirby of the Astrionics Division for their excellent counsel during the work period.

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INTRODUCTION

There are several problems that exist in time-base encoders which have been stated in recent literature.[1] The generation of an accurate reference voltage which is strictly periodic and which does not produce undesirable switching transients resulting from abrupt variations is a serious problem. If the generation of a suitable reference voltage is accomplished there is the problem of accurately comparing this reference to the signal which is to be encoded. Most time-base encoders are designed for high precision operation which places strict requirements on the voltage sensitivity of the comparator. When the comparator functions properly there is the problem of designing a counter which can produce the coded value of the reference voltage in the entire encoding range. The use of a linear counter is adequate only if the encoded value of the reference voltage is linear to the extent of the precision being used. This limits the amount of precision which can be acquired through the use of an exponential reference voltage.

In this paper an encoding system is discussed which eliminates the use of an aperiodic reference voltage with discontinuous properties. This is accomplished using a sinusoidal reference that is digitally represented at any time during the encoding interval by a nonlinear counter. Also, a suitable comparator for this encoder is presented.

THE ENCODING SYSTEM

The encoding system shown in Fig. 1 represents a new approach to time-base encoding in that a sinusoidal reference voltage is used and the

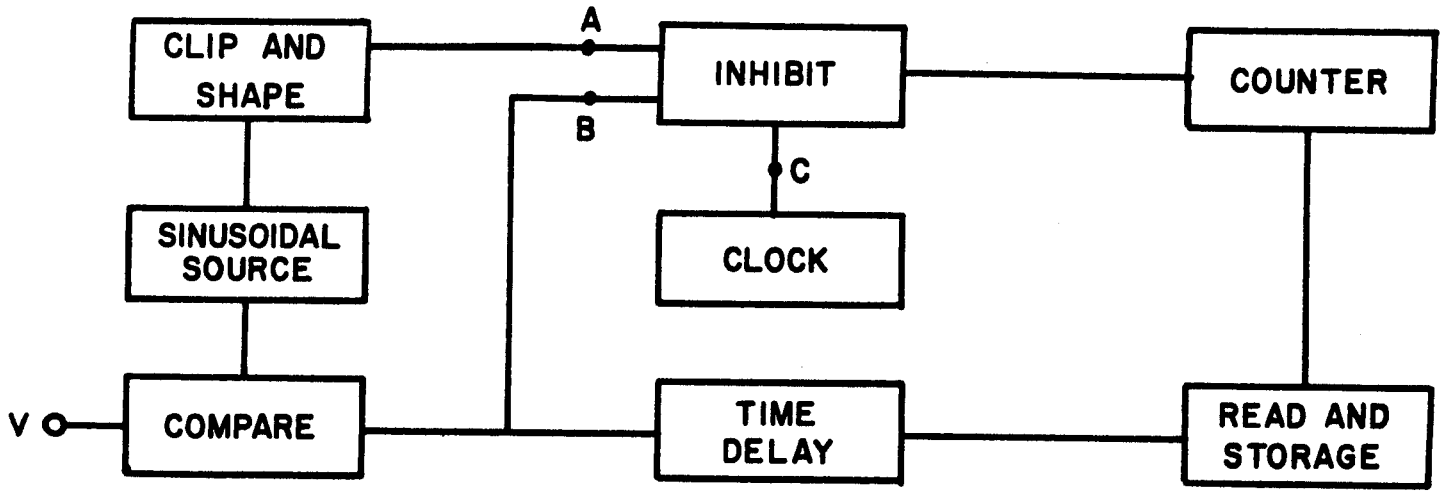

Fig. 1 A nonlinear encoding system.

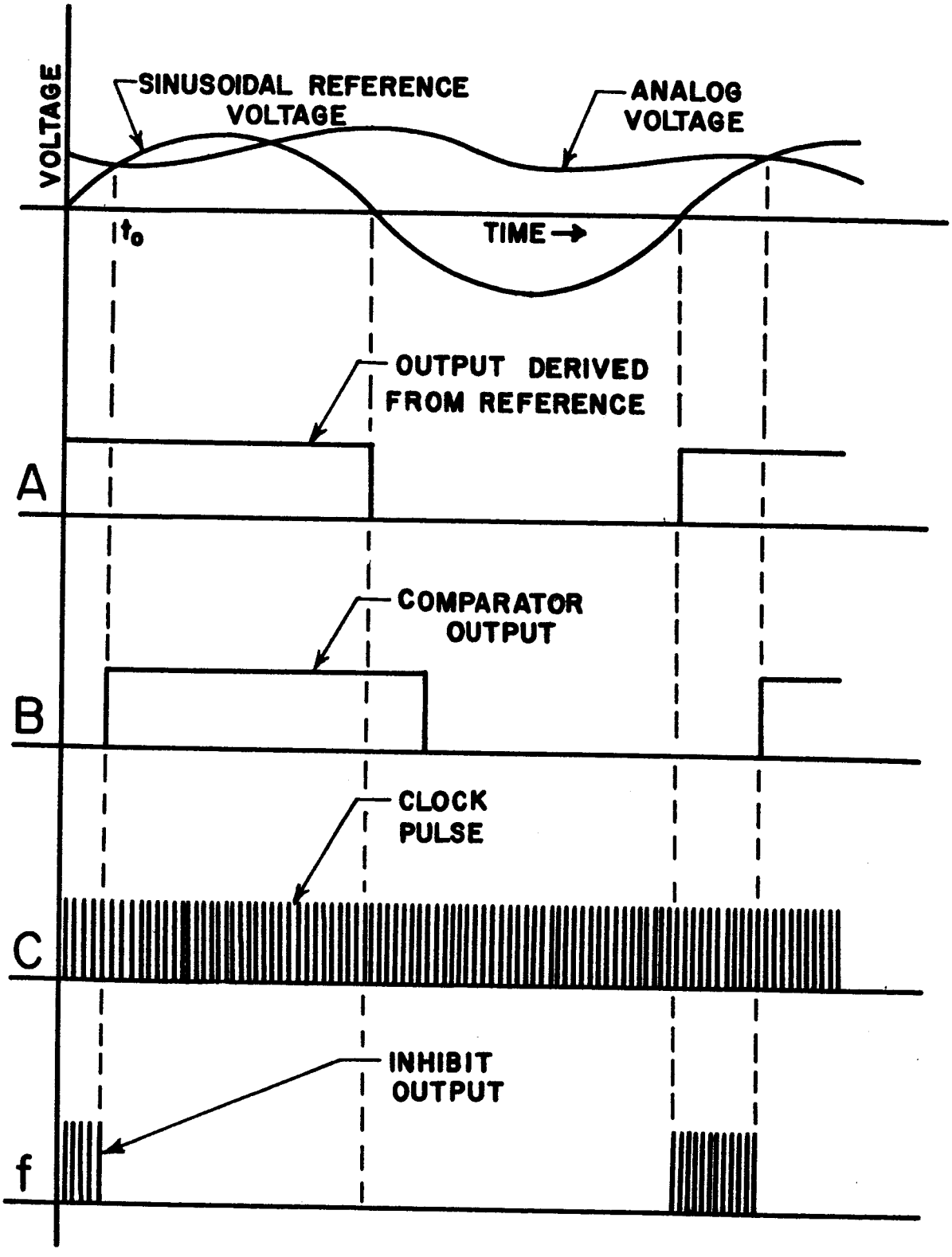

Fig. 2. Waveforms at several points within the encoding system.

counter is designed to accumulate the clock pulses so that the coded output represents the value of the sinusoidal voltage from the positive going zero crossing to the maximum value of the encoding range, which is less than the peak value of the sinusoidal voltage. Discussion of the theory of operation is facilitated by the graphical representation of Fig. 2 which shows a complete cycle of the sinusoidal reference and an arbitrary signal to be encoded.

The output of the counter on discrete, but equal, intervals determined by the clock frequency, represents the encoded value of the reference beginning at the positive going zero crossing. The comparator continuously monitors the difference between the reference and the signal and produces an output when the zero difference occurs that inhibits the clock pulse to an extent that the counter ceases counting. The comparator output is also delivered through a suitable time delay to actuate the read, store, and reset circuitry which records the digital information contained in the counter and resets the counter. This digital information represents the analog signal at time t_o. Inhibition of the clock pulse must be maintained until the next positive going zero crossing.

THE COMPARATOR

As the precision of the encoding system increases the need of a comparator with increased sensitivity becomes necessary. The comparator of Fig. 3 has demonstrated the necessary sensitivity for use in a high precision encoding system.[2] Comparison of the analog signal is accomplished by biasing the tunnel diode so that the peak diode current and

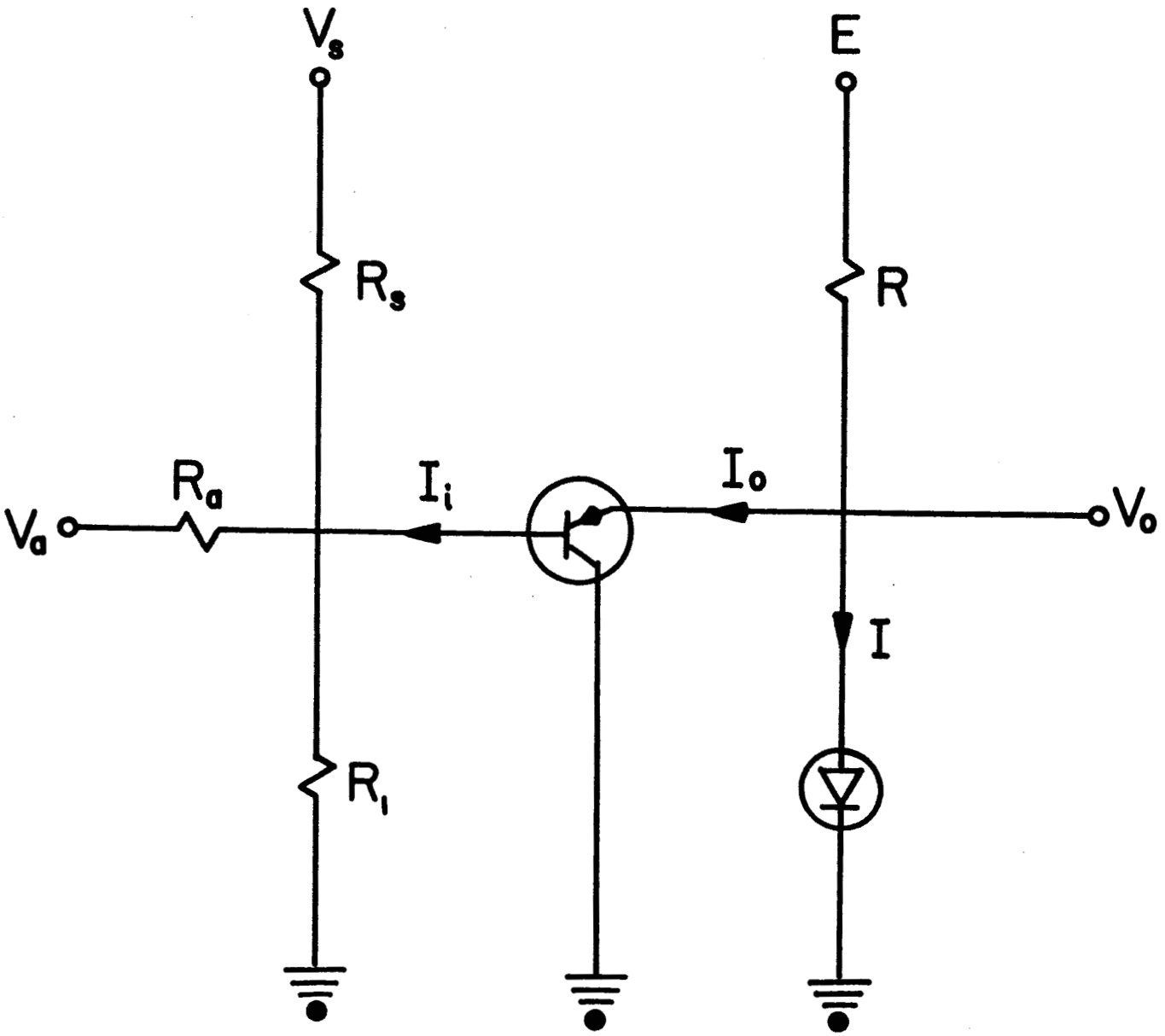

Fig. 3. The compare circuit.

the transistor leakage current are supplied by the voltage E when the transistor is in the off state, which allows the diode to switch to its high voltage state and thereby produce an indication of the transistor off state. This off state results from a small increase in the magnitude of the reference voltage above the magnitude of the analog signal value. The amount of increase necessary to switch the transistor to the off state is set by the required sensitivity of the encoder.

Since a pnp transistor is used to amplify the difference in the tunnel diode current supplied by the reference signal and the analog signal, and to limit the amount of difference current, only negative analog values will be accepted. The use of an npn transistor would reverse these conditions and would allow only positive analog values to be accepted. In either case a suitable transistor switch at the input can be used to appropriately change the sign of the analog signal and to produce an indication of this sign change as an additional bit of information along with the coded output. The tunnel diode is biased so that it is reset to the low voltage state by the negative portion of the reference voltage. The output of the comparator is loaded by the inhibit circuit and the time delay network.

The comparator of Fig. 3 has been built and constructed using a 2N1034 transistor, a 1N2940 tunnel diode, and precision resistors. The upper trace of Fig. 4 represents a reference voltage of 10 volts amplitude and 100-Kc which is compared with an analog value of 5 volts to yield the comparator output illustrated by the lower trace which has a pulse height of 0.55 volts.

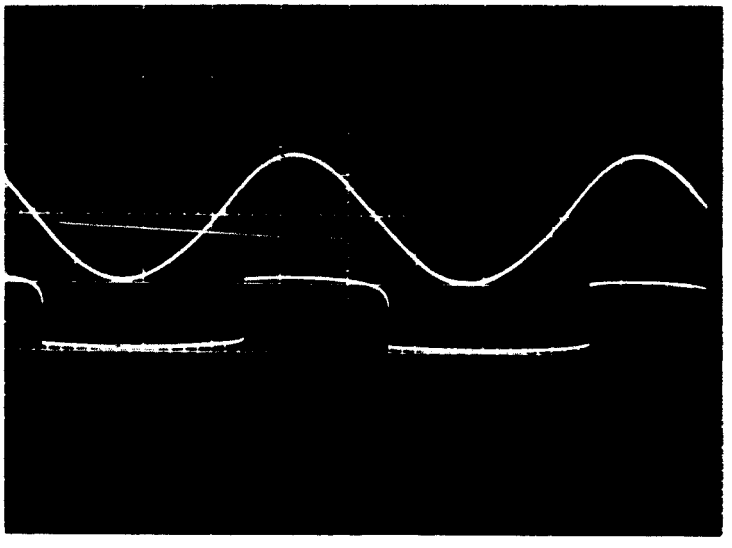

Fig. 4. Traces of the reference voltage and the comparator output.

THE INHIBIT CIRCUIT

The waveforms of Fig. 2 represent the sinusoidal reference, an arbitrary analog signal, and the waveforms at the three inputs of the inhibit circuit that are necessary to properly pulse the counter. The points in the system where these waveforms occur are indicated in the block diagram of Fig. 1. Traces of the waveforms are shown in Fig. 5 with the upper group representing the sinusoidal reference voltage, a constant analog value, and the inhibited clock pulse. The three inputs to the inhibit circuit are represented by the three lower traces. The frequencies of the reference voltage and the clock are 400 cps and 1 Mcps, respectively.

The output of the inhibit circuit may be expressed as $f = A\bar{B}C$ where A is the square waveform derived directly from the reference, B is the comparator output and C is the clock pulse. For suitable pulsing of the counter it is necessary to produce satisfactory waveforms and to give sufficient consideration to the amount of time delay in each part of the inhibit circuit.

THE COUNTER

Using the sinusoidal reference voltage requires a counter which accumulates clock pulses from the time of a positive going zero crossing until the equality of the reference voltage and the analog signal is indicated by the comparator with the maximum value of the encoding range as the upper limit. These clock pulses occur periodically but the counter is designed to produce an output corresponding to discrete levels of the

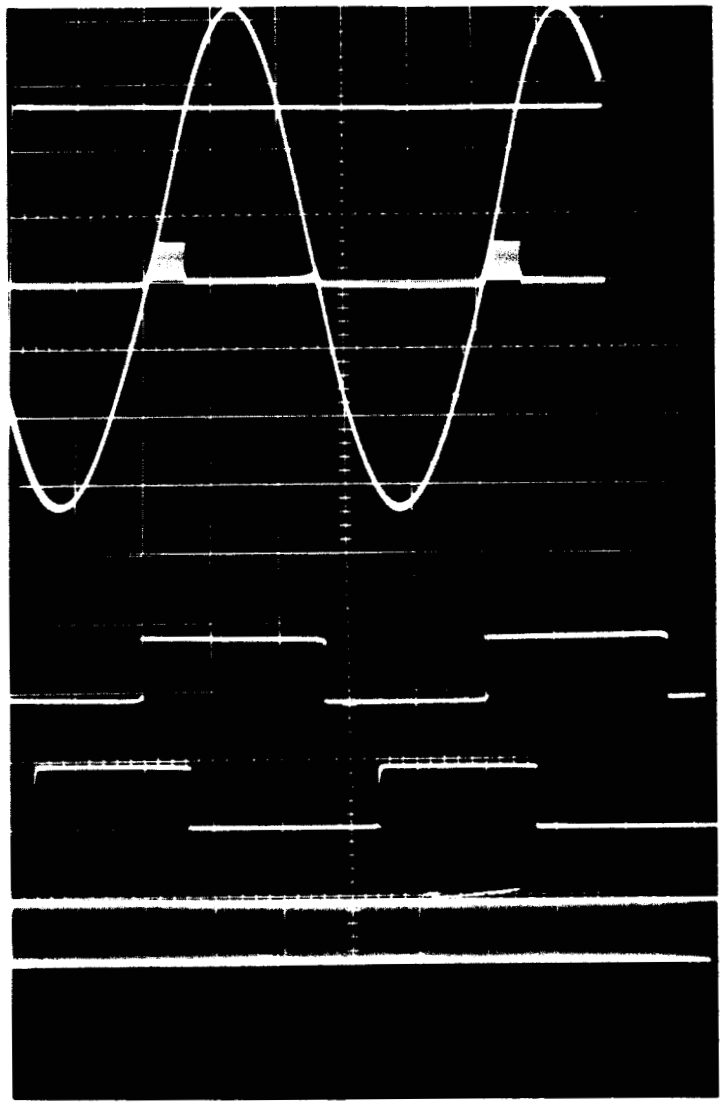

Fig. 5. Traces of the reference voltage, analog value, inhibited clock, output derived from reference, inverted comparator output, and the clock.

sinusoidal reference. The amplitude of the reference voltage should be selected to exceed the maximum analog value by an amount which will eliminate the use of the flat portion of the reference voltage because of the high sensitivity of the comparator needed in this region.

For brevity and simplicity of explanation it is convenient to use relatively low precision to illustrate the logical design of the counter. The values of Table I represent the possible counter outputs that are necessary to represent a sinusoidal reference of 10 volts amplitude with four bit precision for an encoding range of 0.0 to 7.5 volts, or minus 7.5 to plus 7.5 volts if a sign bit is used.

TABLE I

SEQUENCE OF COUNT

t	Reference Voltage	Decoded Output	Counter Output time (t)				time (t+1)			
			A	B	C	D	A	B	C	D
0	0.000	0.0	0	0	0	0	0	0	0	1
1	0.5234	0.5	0	0	0	1	0	0	1	1
2	1.5643	1.5	0	0	1	1	0	1	0	1
3	2.5882	2.5	0	1	0	1	0	1	1	1
4	3.5837	3.5	0	1	1	1	1	0	0	1
5	4.5399	4.5	1	0	0	1	1	0	1	1
6	5.4464	5.5	1	0	1	1	1	1	0	1
7	6.2932	6.5	1	1	0	1	1	1	1	0
8	7.0711	7.0	1	1	1	0	1	1	1	1
9	7.7715	7.5	1	1	1	1	0	0	0	0

The resulting flip-flop difference equations in simplified form are

$$A^{t+1} = \left[(\bar{B}D + \bar{C}D + B\bar{C}\bar{D})A + (BCD)\,\bar{A} \right]^{t}$$

$$B^{t+1} = \left[(\bar{C}D + AC\bar{D})B + (CD)\,\bar{B} \right]^{t}$$

$$C^{t+1} = \left[(\overline{A}BD + AB\overline{D})C + (\overline{B}D + AD)\,\overline{C}\right]^{t}$$

$$D^{t+1} = \left[(\overline{A} + \overline{B})D + (ABC + \overline{ABC})\,D\right]^{t}$$

Using this method introduces an error less than the least significant bit in representing the sinusoidal reference; however, the total encoding error is greater for particular analog values because these values are not available at the counter output and the nearest level differs by an amount greater than the least significant bit. The maximum error occurs at the lower analog levels because the reference increases more rapidly between two consecutive clock pulses at these levels. This error is predictable since the reference is known to vary sinusoidally and the error can be reduced to a desired value by increasing the precision to produce a more accurate representation of the reference. Reduction of error by increasing precision is not always possible with an exponential reference since increased precision with a linear count can reach the point where the reference cannot be approximated as a linear function accurately to the desired precision.

DESIGN CONSIDERATIONS

With the increased precision in representing the sinusoidal reference the complexity of the logic required to implement the nonlinear counter reaches a level that is difficult to manage. For example, the simplification of the flip-flop difference equations is too large a problem to be performed manually.

It is also possible that the sophistication of the logic will reach a level that is not practical for implementation. In this case the digital representation of the reference can be accomplished using two separable units. One unit will accumulate the clock pulses in a linear manner and produce an indication of the number of accumulations when the reference is equal to the analog value. If the encoder is to be used in a hybrid analog-digital system where a digital computer is used to analyze the digital information at the output of the encoder then the conversion of the linear digital accumulation to discrete sinusoidal levels can be included in the analyzing procedures performed by the computer. For use of the encoder in a digital control system this conversion can be performed by a logic conversion unit connected at the output of the linear counter.

Special consideration is presently being given to generalized computer programs and flow charts which will completely automate the logical design of logic conversion units and most counters. The generalization is with respect to the types of codes that are to be used in the conversion units and the counters, and with respect to the sequence of count that is required of the counter. These automated design procedures can be accomplished using numerical representations of Boolean functions and numerical simplification procedures.[3] This automation of logical design is very useful in designing digital devices which operate with large word lengths.

CONCLUSIONS

This nonlinear encoder uses a readily available reference voltage

and the accumulation of the pulses can be accomplished using standard digital modules. It is adaptable to very high precision, particularly with a linear accumulation of the clock pulse and with the high precision there is no loss of accuracy as in the case of an exponential reference. There is no need of sample and hold circuitry in this encoder unless a strictly periodic encoder is needed.

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