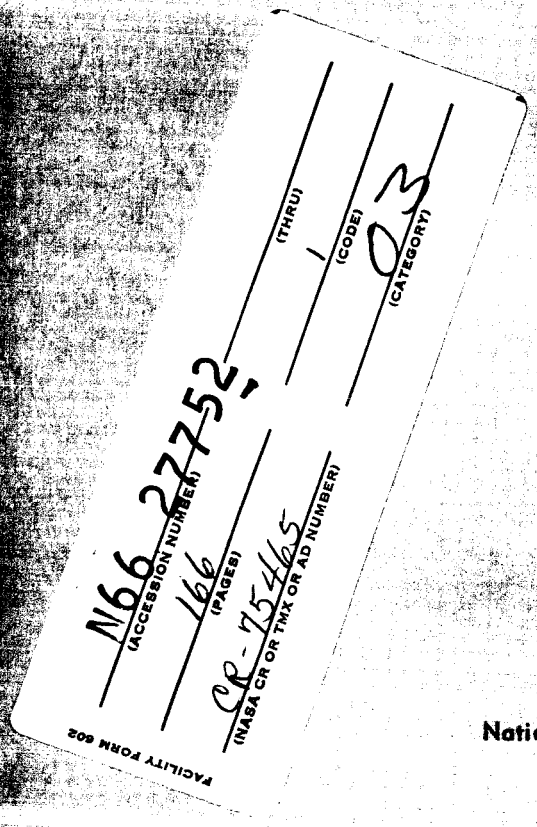
NIMBUS-B SOLAR-CONVERSION POWER SUPPLY SUBSYSTEM

QUARTERLY TECHNICAL REPORT NO. 2

DECEMBER 1965 THROUGH FEBRUARY 1966



Contract No. NAS5-9668

Prepared by

Astro-Electronics Division
Defense Electronic Products
Radio Corporation of America
Princeton, New Jersey

for

National Aeronautics and Space Administration
Washington, D.C.

NIMBUS-B SOLAR-CONVERSION POWER SUPPLY SUBSYSTEM

QUARTERLY TECHNICAL REPORT NO. 2

DECEMBER 1965 THROUGH FEBRUARY 1966

Contract No. NAS5-9668

Prepared by

Astro-Electronics Division
Defense Electronic Products
Radio Corporation of America
Princeton, New Jersey

for

National Aeronautics and Space Administration
Washington, D.C.

AED R-2925

Issued: March 31, 1966

PREFACE

This is the second in a series of quarterly technical reports on the development of the Nimbus-B Solar-Conversion Power Supply Subsystem for the Nimbus Meteorological Satellite. This project is being conducted by the Astro-Electronics Division (hereafter called AED) of RCA for the National Aeronautics and Space Administration (NASA) under Contract No. NAS5-9668. The present report covers the work accomplished during the period of December 1965 through February 1966.

TABLE OF CONTENTS

Section		Page
	PREFACE	iii
I	GENERAL	1
	A. SYSTEM DESCRIPTION	1
	1. Solar Array	2
	2. Battery Modules	3
	3. Electronics Module	3
	B. SYSTEM OPERATION	4
II	SYSTEMS CONSIDERATIONS	5
	A. REGULATED BUS-LOAD CAPABILITY	5
	1. Power Subsystem Computer Model Description	5
	2. System Design Factors	12
	3. Regulated Bus-Load Capability	14
	4. Regulation	15
	5. S-Band Transmitter Operation	28
	6. Power Subsystem Operating Point	28
	7. Power Subsystem Operation with Six and Eight Storage Modules	28
	8. Summary	29
	B. SHUNT DISSIPATOR	29
	1. Threshold Voltage Range Determination	30
	2. Determination of Maximum Power to be Dissipated	30
	C. POWER SUPPLY SYSTEM FAILURE MODE AND EFFECTS ANALYSIS	32
	D. INVESTIGATION OF MULTIPLE OPERATING POINTS	48
	1. Multiple Operating Points and Lock-up	48
	2. Analysis of the Nimbus-B Power Subsystem Operation	51
	3. Summary and Conclusions	52
	4. Construction of I-V Characteristic Curves	55
	E. POWER SYSTEM FUSE STUDY	59

TABLE OF CONTENTS (Continued)

Section		Page
	F. FUSE-REGULATOR INTERFACE PROBLEM	67
	1. Fuse Characteristics	67
	2. Regulator Short-Circuit Transient Characteristics	67
	3. Preliminary Conclusions	69
	4. Approach for Resolving the Problem	69
	G. POWER SUBSYSTEM TELEMETRY	73
	1. Battery Voltage Telemetry	73
	2. Regulated and Unregulated-Bus Voltage Telemetry	74
	3. Battery Temperature Telemetry	74
	4. Auxiliary Regulator Telemetry	75
	5. Regulated-Bus and Solar-Array Telemetry	75
	6. Summary of Telemetry Measurements and Typical Calibration Curves	76
III	STORAGE BATTERIES	83
	A. GENERAL	83
	B. ANALYSIS OF "CRANE" DATA	83
	C. PRELIMINARY "PARAMETRIC STUDY" CURVES	90
	D. PRELIMINARY "LAUNCH PHASE" CURVES	90
	E. BATTERY MODULE POWER TO REGULATED BUS FUSES (SPECIAL TEST)	90
	F. BATTERY MODULE PACKAGING DESIGN	104
	1. Mechanical Design	104
	G. THERMAL ANALYSIS	114
	1. General	114
	2. Module Design and Conditions	114
	3. Analysis and Results	115
	4. Conclusion	118
IV	BATTERY CONTROL AND PROTECTION CIRCUITS	121
	A. GENERAL	121

TABLE OF CONTENTS (Continued)

Section		Page
	B. CURRENT REGULATOR	121
	C. BATTERY VOLTAGE-TEMPERATURE REGULATION	122
	D. HIGH-TEMPERATURE CUTOFF CIRCUIT	122
	E. BATTERY MODULE ELECTRONICS PERFORMANCE LIMITS	127
	F. CHARGE AND DISCHARGE-CURRENT TELEMETRY	129
V	ELECTRONICS MODULE	131
	A. ELECTRICAL DESIGN	131
	1. General	131
	2. Regulated Bus Comparator	131
	3. Auxiliary Regulator	134
	4. Shunt Dissipator	135
	5. Power Dissipations and System Efficiencies	138
	B. MECHANICAL DESIGN	140
	1. General	140
	2. Printed-Circuit Boards	140
	3. Connectors and Wiring	140
	4. Electromagnetic Compatibility	140
	5. Weight	142

LIST OF ILLUSTRATIONS

Figure		Page
1	Nimbus-B Power Supply Subsystem, Revised Functional Block Diagram	7
2	Nimbus-B Electronics Module, Revised Functional Block Diagram	9
3	Nimbus-B Power Subsystem, Simplified Block Diagram for Energy Balance Calculations	11
4	General Load Profile Used to Determine Nimbus-B Average Power Capability	15
5	Regulated Bus Average Power Versus Time in Orbit Using 25° C Battery	16
6	Regulated Bus Average Power Versus Time in Orbit Using 15° C Battery	17
7	Regulated Bus Average Power Versus Time in Orbit Using 35° C Battery	18
8	Power Subsystem Regulated-Bus-Load Capability with Nominal System Design and 25° C Battery for One-Year Orbital Life	19
9	Power Subsystem Regulated-Bus-Load Capability with Worst-Case System Design and 25° C Battery for One-Year Orbital Life	20
10	Power Subsystem Regulated-Bus-Load Capability with Best-Case System Design and 25° C Battery for One-Year Orbital Life	21
11	Power subsystem Regulated-Bus-Load Capability with Nominal System Design and 15° C Battery for One-Year Orbital Life	22
12	Power Subsystem Regulated-Bus-Load Capability with Worst-Case System Design and 15° C Battery for One-Year Orbital Life	23

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
13	Power Subsystem Regulated-Bus-Load Capability with Best-Case System Design and 15° C Battery for One-Year Orbital Life	24
14	Power Subsystem Regulated-Bus-Load Capability with Nominal System Design and 35° C Battery for One-Year Orbital Life	25
15	Power Subsystem Regulated-Bus-Load Capability with Worst-Case System Design and 35° C Battery for One-Year Orbital Life	26
16	Power Subsystem Regulated-Bus-Load Capability with Best-Case System Design and 35° C Battery for One-Year Orbital Life	27
17	Nimbus-B Power Supply Failure Mode Functional Block Diagram	33
18	Power System Output Multiple-Operating-Point Characteristic Curve	49
19	Power Subsystem, Simplified Block Diagram	51
20	Beginning-of-Life I-V Characteristics at AVR Input	53
21	End-of-Life I-V Characteristics at AVR Input	54
22	Picofuse Time Versus Current Curves	60
23	5-Ampere Rating Picofuse Time Versus Current Curve	61
24	15-Ampere Rating Picofuse Time Versus Current Curve	62
25	Oscilloscope Tracings of Three 5-Ampere Picofuses in Parallel, 15-Ampere Rating	63
26	Oscilloscope Tracings of Two 5-Ampere Picofuses in Parallel (10-Ampere Rating), and Comparison of High-Reliability and Commercial 5-Ampere Fuses	64
27	Samples of Encapsulated Fuses	66

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
28	Current Versus Time-to-Blow Graph of 15-Ampere Picofuse	68
29	Regulator Equivalent Circuit	69
30	Fuse Currents (5, 10, and 15-Ampere) Versus Time for Regulator Short-Circuit Condition	70
31	Current Limiting and Battery Tap System, Functional Block Diagram	71
32	Battery Voltage Telemetry Circuit Diagram	73
33	Battery Temperature Telemetry Circuit Diagram	74
34	Auxiliary Regulator Voltage Telemetry	75
35	Regulated-Bus and Solar-Array Current Telemetry Circuit Diagram	76
36	Typical Battery Voltage Telemetry Calibration Curve	78
37	Typical Temperature Telemetry Calibration Curve	78
38	Typical Charge Current Telemetry Calibration Curve	79
39	Typical Discharge Current Telemetry Calibration Curve	79
40	Typical Regulated-Bus Voltage Telemetry Calibration Curve	80
41	Typical Unregulated-Bus Voltage Telemetry Calibration Curve	80
42	Typical Auxiliary Regulator Voltage Telemetry Calibration Curve	81
43	Typical Regulated-Bus and Solar-Array Current Telemetry Calibration Curve	82
44	Average Cell Voltage Versus Depth-of-Discharge and Temperature at 2250 Cycles	84

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
45	Average Cell Voltage Versus Depth-of-Discharge and Temperature at 2250 Cycles	85
46	Average Cell Voltage Versus Depth-of-Discharge and Temperature at 2750 Cycles	86
47	Average Cell Voltage Versus Depth-of-Discharge and Temperature at 3250 Cycles	87
48	Average Cell Voltage Versus Temperature at 3750 cycles	88
49	Average Cell Voltage Versus Cycle at 10 Percent Depth of Discharge	89
50	Average Cell Voltage Versus Cycle at 15 Percent Depth of Discharge	89
51	Average Cell Voltage Versus Cycle at 20 Percent Depth of Discharge	89
52	Cell Charge and Discharge Voltages Versus Time at 15° C, First-Day Estimate	91
53	Cell Charge and Discharge Voltages Versus Time at 15° C, 6 months Cycling Estimate	92
54	Cell Charge and Discharge Voltages Versus Time at 15° C, 9 months Cycling Estimate	93
55	Cell Charge and Discharge Voltages Versus Time at 15° C, 12 months Cycling Estimate	94
56	Cell Charge and Discharge Voltages Versus Time at 35° C, First-Day Estimate	95
57	Cell Charge and Discharge Voltages Versus Time at 35° C, 6 months Cycling Estimate	96
58	Cell Charge and Discharge Voltages Versus Time at 35° C, 9 Months Cycling Estimate	97
59	Cell Charge and Discharge Voltages Versus Time at 35° C, 12 Months Cycling Estimate	98

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
60	Cell Discharge Voltages Versus Time at 25° C, First-Day and 6 Months Cycling Estimates	99
61	Cell Discharge Voltages Versus Time at 25° C, 9 and 12 Months Cycling Estimates	100
62	Cell Charge and Discharge Voltages Versus Time at 15 to 25° C, Launch-Phase Estimate	101
63	Cell Charge and Discharge Voltages Versus Time at 35° C, Launch-Phase Estimate	102
64	Battery Module Special Test Circuit	103
65	Nimbus-B Battery Module Structural and Interface Drawing (RCA Dwg No. 1849618)	105
66	Nimbus-B Battery Module Schematic Diagram (RCA Dwg No. 1759588)	107
67	Nimbus-B Battery Cell Assembly Drawing (RCA Dwg No. 1849586)	109
68	Nimbus-B Heat Sink Assembly Drawing (RCA Dwg No. 1849596)	111
69	Major Component Heat Dissipation Versus Time, Battery Module Thermal Analysis	115
70	Identification of Nodes Used in Battery Module Thermal Analysis	117
71	Temperature Versus Time for Several Nodes in Battery Module Thermal Analysis	118
72	Nimbus-B Battery Module Electronics, Functional Block Diagram	123
73	Current Regulator Schematic Diagram	125
74	Battery Voltage-Temperature Regulation Circuit, Schematic Diagram	126

LIST OF ILLUSTRATIONS (Continued)

Figure		Page
75	High-Temperature Cutoff Circuit, Schematic Diagram	127
76	Recommended Voltage Limit Versus Temperature Curve	128
77	Battery Charge-Current Telemetry Circuit, Schematic Diagram	130
78	Regulated-Bus Comparator, Functional Block Diagram	133
79	Auxiliary Regulator Circuit, Schematic Diagram	136
80	Shunt Dissipator Circuit, Simplified Schematic Diagram	137
81	Proposed Nimbus-B Electronics Module Configuration	141

LIST OF TABLES

Table		Page
1	Size and Weight of Subsystem Assemblies	2
2	Shunt Dissipator Power Requirements	31
3	Power Supply "Black-Box" Malfunction Definitions	34
4	Intra-System Failures	35
5	External Malfunctions	47
6	Reflected Battery Discharge Characteristics	56
7	Reflected Battery Charge and Limiter Characteristics	57
8	Power Subsystem Telemetry Measurements	77
9	Cell Cycle Life Versus Temperatures at 15 Percent Depth of Discharge	88

LIST OF TABLES (Continued)

Table		Page
10	Summary of Battery Module Special Test Results.	103
11	Calculated Component Dissipation and Temperature	119
12	Electronics Module Power Dissipations and System Efficiencies	139

SECTION I
GENERAL

The Nimbus-B Solar-Conversion Power Supply Subsystem provides the necessary power to operate the spacecraft and its subsystems. During the spacecraft day, an array of N-on-P silicon solar cells, mounted on two sun-oriented platforms, converts solar radiation to electrical power. This daytime, solar-array power is supplied to the spacecraft loads; it is also used to recharge the batteries. During the spacecraft night and also during peak daytime load periods, parallel-connected battery modules (housing series-connected nickel-cadmium storage cells) supply power to the spacecraft loads.

The solar-conversion power supply subsystem provides the following general functions:

- Acquisition of incident solar radiation and photovoltaic conversion to electrical power;
- Energy storage by electrochemical means; and
- Regulation of the electrical power to provide a voltage level suitable for distribution to the spacecraft subsystems.

A. SYSTEM DESCRIPTION

The Nimbus-B Solar-Conversion Power Supply Subsystem consists of eight identical battery modules, one electronics module, and two solar-cell platforms. Each battery module contains 23 series-connected nickel-cadmium cells, together with a group of electronic circuits designed to provide control and protection for the power supply circuits and components. These battery circuits are housed in cast-magnesium containers with sheet-magnesium covers, while the other electronics circuits are housed in the machined-aluminum electronics module. The electronics module and the battery modules are mounted in the sensory ring which is separated from the control housing by the truss supports of the spacecraft. The solar-cell platforms are attached to the control housing by means of the platform driveshaft. Slip rings on the shaft provide electrical interface connections between the solar platforms and the rest of the power supply. The structural separation and relatively simple mechanical and electrical interface connections between the solar platform, control housing, and sensory ring provide for independent thermal control of each of these major assemblies. The anticipated weights of the individual assemblies of the power supply subsystem are given in Table 1. The entire subsystem weight is approximately 220 pounds.

TABLE 1. SIZE AND WEIGHT OF SUBSYSTEM ASSEMBLIES

Assembly	Width (in.)	Height (in.)	Depth (in.)	Volume (cu in.)	Weight (pounds)
Solar-Cell Platform including Transition Section	46.75	96	-	-	40.0
Battery Module	6	8	6.5	312	15.0
Electronics Module	6	8	13	614	20.0

1. Solar Array

The radiative energy from the sun is utilized in direct photovoltaic conversion to provide electrical power for the spacecraft. The platform assembly of phosphorous-doped silicon N-on-P cells provide the photovoltaic mechanism to accomplish this energy conversion. The solar-cell platform assembly intercepts an active solar energy equivalent to 5822 watts (140 milliwatts per square centimeter nominal intensity) during the sunlight period. By considering the GFE *solar-cell module efficiency of 10.5 percent (at air-mass-zero), the environment in space, and the power supply operating characteristics, it is estimated that a minimum of 415 watts will be obtained from the cells in the design operating range at a temperature of 40°C at the beginning of life.

Each of the solar-cell platforms consists of a solar-cell mounting structure with its solar-cell array, a transition section, a latching assembly, a drive motor with an associated gear-reduction unit, and a control shaft clamp.

Since the vehicle launch time yields a retrograde polar orbit that contains the earth-sun line, acquisition of the sun is simplified by requiring only one axis of rotation for the solar array. The solar cells, mounted on one side of the aluminum honeycomb platforms, are maintained continuously incident to the earth-sun line and are, therefore, able to intercept a maximum of solar energy during the sunlight period. Sun sensors, circling the driveshaft of each platform, detect solar radiation and control the position of the panels with respect to the sun-spacecraft line so that the panels remain normal to the sun vector. A servo motor, located in the control housing, rotates the panel driveshaft. During orbit, approximately 73 minutes will be spent in sunlight and 35 minutes in the earth's shadow. When the satellite is on the dark side of the earth, a preset potentiometer continues to provide a signal to turn the platforms until they reach the position to acquire the rising sun.

*Government furnished equipment

2. Battery Modules

Each battery module contains a series string of 23 nickel-cadmium storage cells. The charge current available during satellite day is determined by the solar-array output and the spacecraft subsystem load power requirements. Charge current is regulated as a function of battery voltage and temperature with a closed-loop charge controller. Charge current is reduced to a safe level if either the battery voltage or temperature reaches a predetermined limit. A ground-command override circuit (in the electronics module) permits restoration of normal charging during emergencies.

Telemetry voltages proportional to battery temperature, voltage, and current are provided as module outputs.

A shunt dissipator in each module provides control of the dissipation of approximately 75 watts of solar-array bus power. All shunt regulators in the system are controlled by a single amplifier in the electronics module.

In the negative leg of each battery string, is a battery disconnect magnetic latching relay which can be actuated by ground command.

3. Electronics Module

The electronics module contains redundant pulse-width-modulator (PWM) type regulators, a regulated bus comparator, redundant auxiliary regulators, a shunt regulator drive amplifier, regulated-bus current and voltage telemetry, and array-bus current and unregulated-bus voltage telemetry.

The PWM regulator switches automatically from one redundant series switching element to the other when required by the regulated-bus comparator. The regulated-bus comparator (RBC) senses the regulated bus continuously. When a change of more than ±2 volts from the regulated -24.5 volts occurs, the RBC provides the logic and command to turn on the standby element and shut off the operating series switching element.

One auxiliary regulator (AR) is utilized to provide power for battery-module-protection circuitry while the other provides power for the electronics module circuitry (primarily the RBC). Each auxiliary regulator is diode-gated with the regulated bus to provide power to the spacecraft clock receivers should the regulated bus be temporarily lost.

A differential amplifier senses the unregulated-bus voltage and, at a preset value, provides the driving signal to each of the eight shunt regulators in the battery modules. This effectively loads the solar array and prevents high-voltage damage to the regulators and charge controllers.

The charge control override circuit on ground command, provides a signal which cancels out over-voltage and over-temperature signals in each module. All charge controllers are then operating in their normal current limiting mode.

Regulated bus current and solar-array bus current telemetry signals are generated by magnetic amplifier circuits which use a common oscillator.

Battery-module power ground is returned to the electronics module, with only one power-supply ground connection made to the spacecraft ground. All telemetry circuits have been provided with a separate telemetry ground.

Spacecraft subsystem power for non-critical loads is drawn from the regulated bus through appropriate fuses. Critical loads are supplied directly from the regulated bus.

B. SYSTEM OPERATION

During satellite night, the spacecraft loads are supplied by the PWM regulator whose input power is derived from the discharge of the eight nickel-cadmium batteries. When the spacecraft enters the sun lighted portion of its orbit, the solar array begins to provide the input power to the PWM regulator. In addition, power is supplied through the charge controllers to recharge the batteries. As the batteries charge, their terminal voltages rise. A "voltage versus temperature" circuit compares each battery voltage and temperature to a pre-established function, and reduces the charge current as necessary to remain within these limits. As each battery charge current is reduced to a minimum, the array-bus voltage will increase; the operating point changes on the array I-V curve, until, under light spacecraft loads, the array voltage will reach the threshold voltage of the shunt dissipator. Excess array power is then dissipated in the dissipative elements so the array-bus voltage is limited to 39 volts. (The shunt dissipator may or may not be activated each orbit, this will be determined by the load programming and the battery temperature.)

When the spacecraft is again eclipsed (on the dark side of the orbit), the batteries will discharge to provide the load power. When the system is in energy balance for that orbit, the batteries will establish that the energy discharged during satellite night had been replaced during satellite day with enough excess energy to account for battery inefficiencies.

SECTION II
SYSTEMS CONSIDERATIONS

During the second quarter, the systems engineering effort has been concentrated on evaluating the power subsystem performance. Shunt-dissipator-threshhold-voltage range and power-dissipation requirements have been determined. A study was conducted to investigate the possibility of undesirable operating points in the power subsystem. An analysis was performed to determine the effects on power-subsystem operation of "black-box" failure modes within the power subsystem. A subsystem definition has been prepared for use in the spacecraft integration interface documentation, and a power subsystem performance specification has been started. The power subsystem regulated, bus-load capability has been defined for all anticipated conditions in normal orbital operation for one year of life.

Since the last report (Quarterly Technical Report No. 1), a revision to the electronics module circuitry has been made and this is reflected in both the power supply subsystem functional block diagram (Figure 1) and electronics module functional block diagram, Figure 2.

A. REGULATED BUS-LOAD CAPABILITY

The regulated bus-load capability of the Nimbus-B power subsystem for 0, 6, 9, and 12 months in orbit is covered in this section. The Nimbus-B Energy Balance Computer Program was utilized to predict the subsystem performance for conditions of 15°, 25°, and 35°C battery temperature and nominal, worst-case, and best-case system design factors. Included in this section are the effects of the above lifetime, temperature, and design factor parameters on the following:

(1) Balance between satellite nightime and daytime loads,

(2) Voltage regulation,

(3) S-Band transmitter operation,

(4) Power subsystem operating point, and

(5) Subsystem operation with other than seven storage modules.

1. Power Subsystem Computer Model Description

The simplified functional power subsystem that was used to permit efficient computer operation is shown in Figure 3. This subsystem is entirely equivalent to

the actual Nimbus-B power subsystem described in Section I. A characterization of each of the functional components of the simplified subsystem follows:

a. SOLAR ARRAY

The solar array is identical in configuration to that used on Nimbus-A, having effectively 112 parallel solar-cell strings with 98 series-connected cells in 80 of the strings, and 97 series-connected cells in 32 of the strings. The basic array I-V curve is a series-parallel multiplication of the mean solar-cell I-V curve described in Section III-B of Quarterly Technical Report No. 1 (AED R-2889).

b. BATTERY

One large battery is assumed, having the combined capacity of seven Nimbus-B storage modules (capacity = 7 x 4.5 = 31.5 amp-hrs). A capacity of 4.5 ampere-hours is defined at the minus one standard deviation at 25°C in Section IV-B of Quarterly Technical Report No. 1. The validity of combining the average characteristics of seven batteries into one large capacity unit is based on measured data which shows that unequal battery voltages at the end of a charge period are very rapidly equalized during discharge. Approximately equal current sharing is maintained on a long-term basis (for several orbits) provided the individual battery temperatures are not widespread and the battery discharge diodes are closely matched with respect to their forward-biased characteristics.(1) The discharge diodes will be matched for use in the Nimbus-B power subsystem. Nimbus-B battery cell charge and discharge data used in the computer work is presented in Section III.

c. CHARGE CONTROLLER

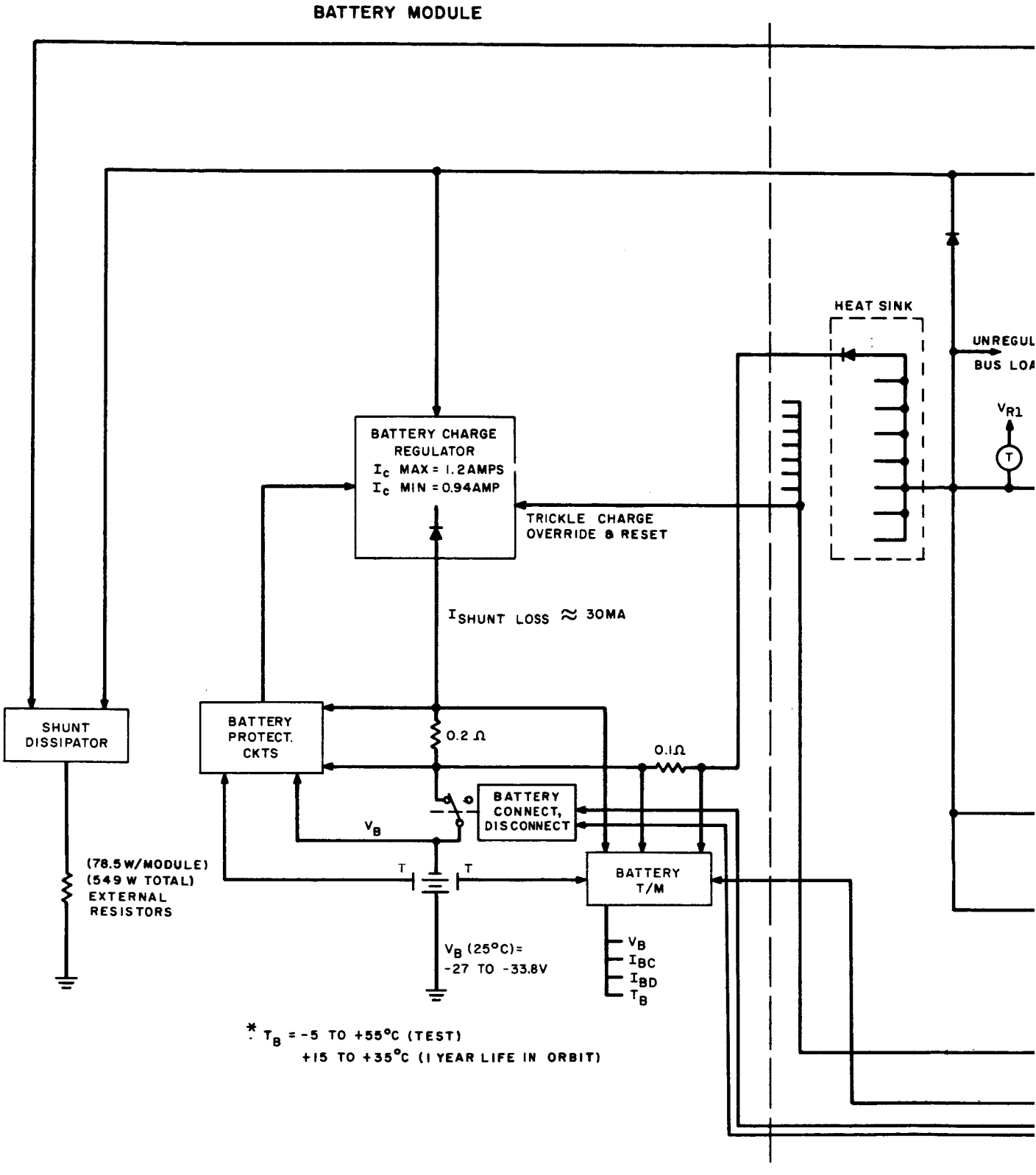
One taper-charge, current-limiting, charge controller is used in conjunction with the single battery. The voltage across the charge controller includes all voltage drops between the array bus and the battery. A linear I-V characteristic is assumed between the dead-zone voltage (voltage at which charge current will begin to flow) and the knee voltage (voltage at which maximum charge current is reached) of the charge controller.

d. SHUNT DISSIPATOR

A single shunt dissipator accepts the unused solar-array current when the subsystem operating point voltage on the solar-array bus exceeds the threshhold voltage. A transconductance of 25 mhos describes the I-V characteristic of the shunt dissipator at voltages exceeding the threshhold voltage.

---

(1) "Final Report - Nimbus Battery Bussing Test", File No. SP-S-994, November 17, 1964


BATTERY MODULE
HEAT SINK
UNREGUL
BUS LOA
V_{R1}
BATTERY CHARGE REGULATOR
I_c MAX = 1.2AMPS
I_c MIN = 0.94AMP
TRICKLE CHARGE OVERRIDE & RESET
$I_{SHUNT\ LOSS} \approx$ 30MA
SHUNT DISSIPATOR
BATTERY PROTECT. CKTS
0.2 Ω
0.1Ω
BATTERY CONNECT, DISCONNECT
V_B
(78.5W/MODULE) (549 W TOTAL) EXTERNAL RESISTORS
T
T
BATTERY T/M
V_B (25°C)= -27 TO -33.8V
V_B
I_{BC}
I_{BD}
T_B
* T_B = -5 TO +55°C (TEST)
+15 TO +35°C (1 YEAR LIFE IN ORBIT)

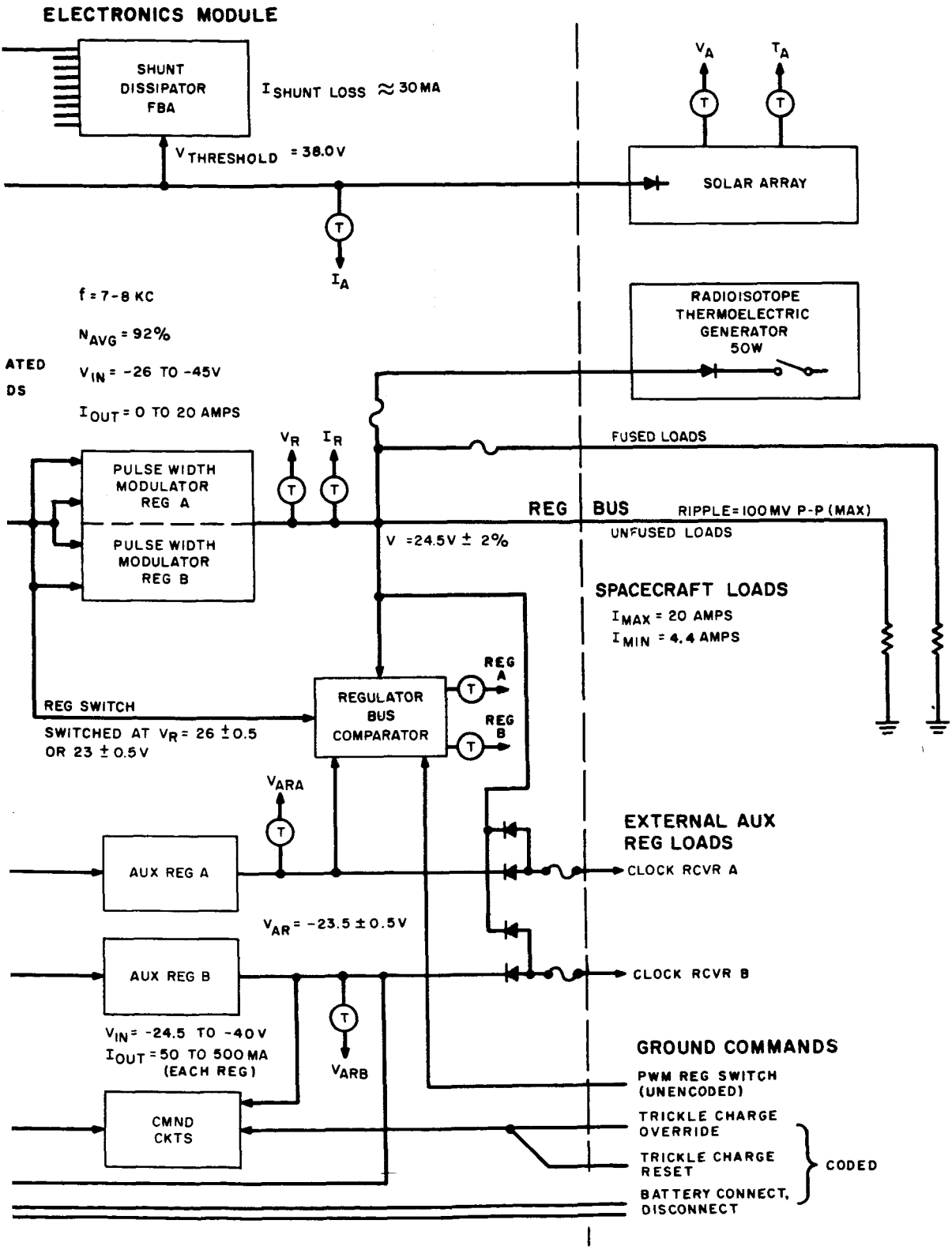
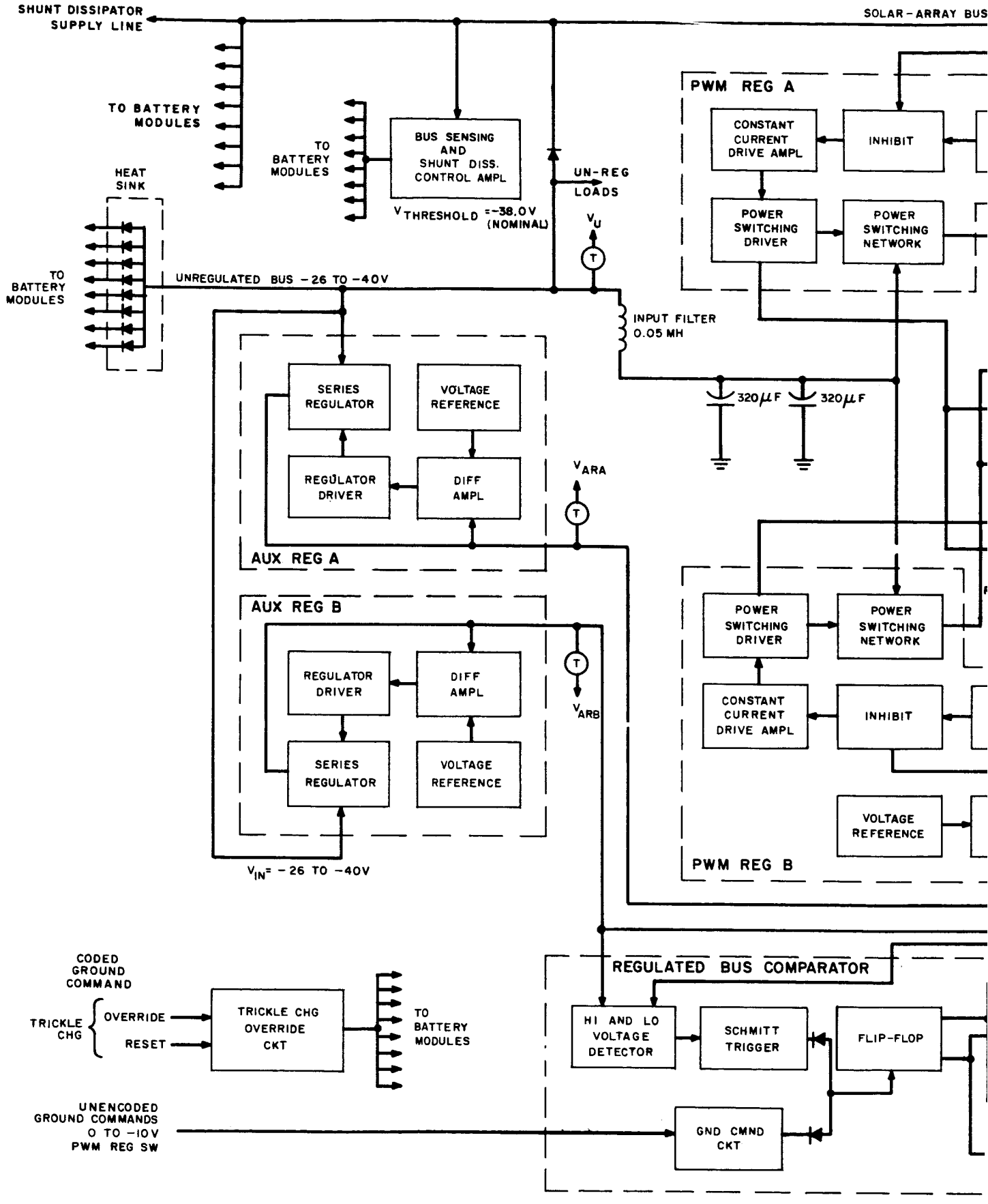


Figure 1. Nimbus-B Power Supply Subsystem, Revised Functional Block Diagram


SHUNT DISSIPATOR SUPPLY LINE
SOLAR-ARRAY BUS
TO BATTERY MODULES
TO BATTERY MODULES
BUS SENSING AND SHUNT DISS. CONTROL AMPL
$V_{THRESHOLD}$ =-38.0V (NOMINAL)
UN-REG LOADS
HEAT SINK
TO BATTERY MODULES
UNREGULATED BUS -26 TO -40V
V_U
INPUT FILTER 0.05 MH
320μF
320μF
PWM REG A
CONSTANT CURRENT DRIVE AMPL
INHIBIT
POWER SWITCHING DRIVER
POWER SWITCHING NETWORK
SERIES REGULATOR
VOLTAGE REFERENCE
REGULATOR DRIVER
DIFF AMPL
V_{ARA}
AUX REG A
AUX REG B
REGULATOR DRIVER
DIFF AMPL
SERIES REGULATOR
VOLTAGE REFERENCE
V_{ARB}
V_{IN}= -26 TO -40V
POWER SWITCHING DRIVER
POWER SWITCHING NETWORK
CONSTANT CURRENT DRIVE AMPL
INHIBIT
VOLTAGE REFERENCE
PWM REG B
CODED GROUND COMMAND
TRICKLE CHG
OVERRIDE
RESET
TRICKLE CHG OVERRIDE CKT
TO BATTERY MODULES
REGULATED BUS COMPARATOR
HI AND LO VOLTAGE DETECTOR
SCHMITT TRIGGER
FLIP-FLOP
UNENCODED GROUND COMMANDS 0 TO -10V PWM REG SW
GND CMND CKT

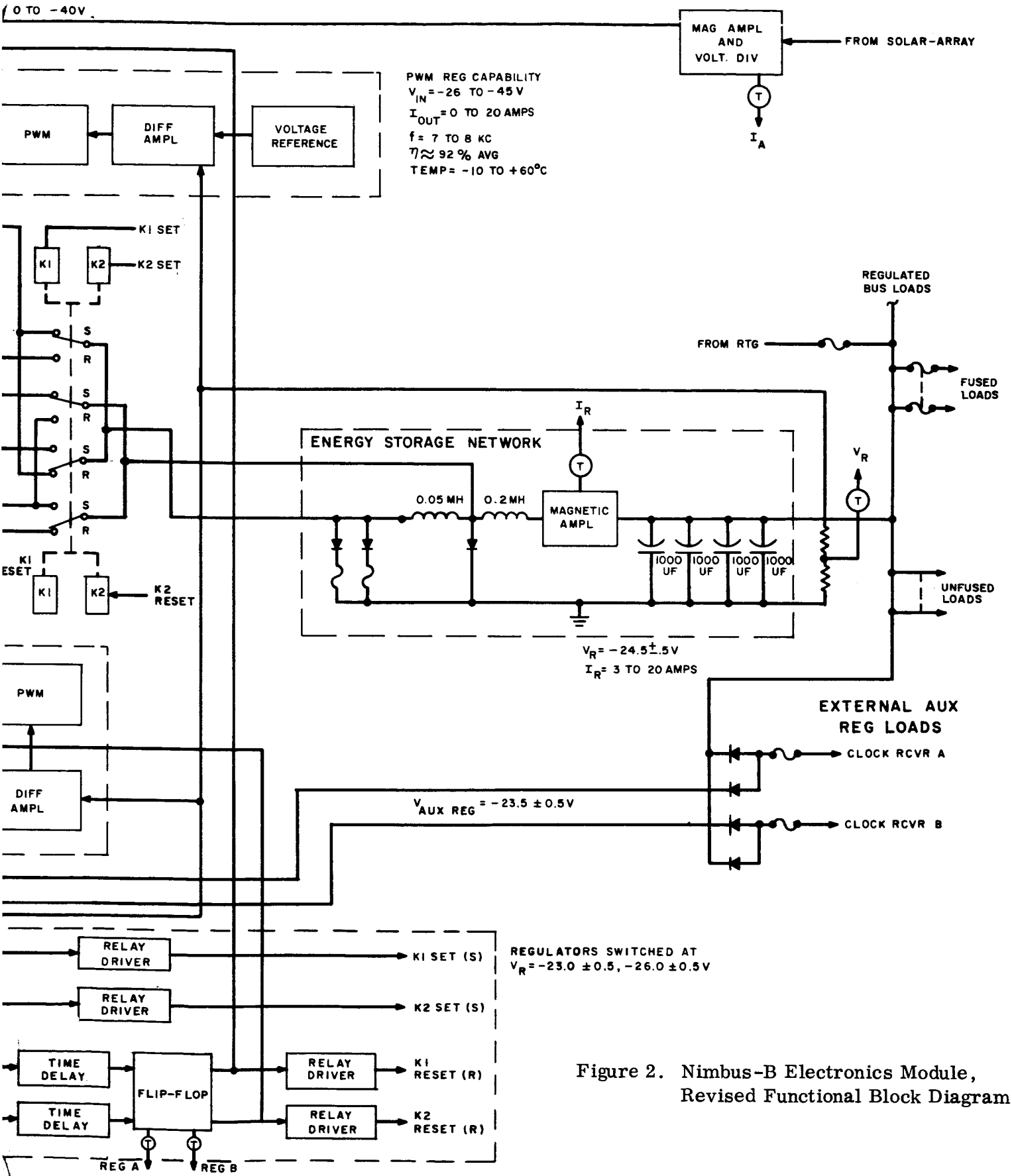


Figure 2. Nimbus-B Electronics Module, Revised Functional Block Diagram

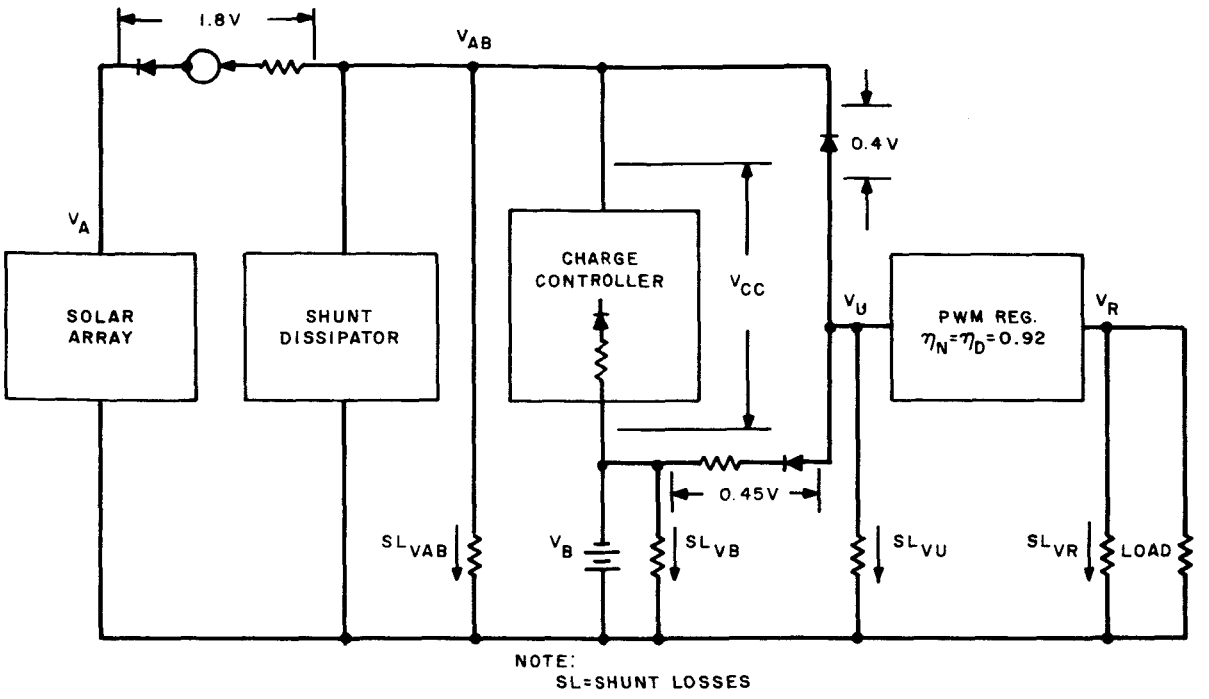


Figure 3. Nimbus-B Power Subsystem, Simplified Block Diagram for Energy Balance Calculations

e. PWM REGULATOR

A constant efficiency $(V_{REG} \times I_{OUT})/(V_{UNREG} \times I_{IN})$ equal to 0.92 and a constant output voltage of $V_{REG} = 24.5V$ are the only characteristics of the regulator needed to perform energy balance calculations. The efficiency is a conservative average value taken from the AVR report (2).

f. LOAD

The regulated bus load is defined as the power demand, at -24.5 volts, of all spacecraft subsystems except the power supply subsystem. All loads are considered to be in steady-state condition.

g. SHUNT LOSSES

The power supply subsystem derives power from the solar-array bus, unregulated bus, batteries, and regulated bus to operate functional and protective

(2) Advanced Voltage Regulator Research and Development Program, Final Report, July 31, 1964, Prepared for NASA by RCA under Contract No. NAS 5-3248.

circuitry. These shunt losses have been combined and are represented as an equivalent power loss from the unregulated bus.

Because of the experimental status of the SNAP-19 program, no power contribution from the RTG (radioisotope thermoelectric generator) is considered.

2. System Design Factors

Prediction of subsystem performance is significantly affected by the values of various degradation factors selected for each component in the subsystem. Because of the uncertainty involved in assigning values to the degradation factors, the selection of most factors is categorized as being nominal, worst case, or best case. Environmental factors (temperature and irradiation) influence the subsystem performance, as do such items as power losses at component interfaces. Certain system constants such as shunt-dissipator threshhold voltage, isolation diode voltage drops, and maximum allowable battery charge voltage are selected to be sufficiently conservative for all operating conditions. All the above considerations are termed system design factors, and are defined below.

a. GENERAL SYSTEM DESIGN FACTORS AND CONSTANT VALUES

Electron and proton irradiation fluxes = estimated 1968 values.[1]

Orbit period = 108 minutes

Satellite nighttime = 35 minutes per orbit

Shunt losses: = 13 watts (satellite nighttime)
20 watts (satellite daytime)

The voltage drop between solar array and solar-array bus = 1.8 volts. (This includes array blocking diodes, slip-ring loss, and harness and connector loss.)

The voltage drop (diode voltage) between solar-array bus and unregulated bus = 0.4 volt.

The voltage drop between the battery and unregulated bus = 0.45 volt. (This includes the blocking diode, discharge current telemetry resistor, and wiring and connector loss.)

b. SHUNT DISSIPATOR DESIGN FACTORS

Threshhold voltage = 38.0 volts

Transconductance = 25 mhos

c. CHARGE CONTROLLER DESIGN FACTORS

Maximum charge current: = 7.7 amps (nominal)
7.0 amps (worst case)
8.4 amps (best case)

Dead zone voltage = 0.7 volt (nominal and best case)
1.5 volts (worst case)

Knee voltage = 1.2 volts (nominal and best case)
2.4 volts (worst case)

Maximum battery voltage: = 34.0 volts (15°C)
33.5 volts (25°C)
33.0 volts (35°C)

d. BATTERY DESIGN FACTORS

Charge-to-discharge ratio $\frac{\text{(amp-min. in)}}{\text{(amp-min. out)}}$ = 1.15(15°C)
1.25(25°C)
1.35(35°C)

e. SOLAR ARRAY DESIGN FACTORS:

	Nominal	Worst-Case	Best-Case
Ultraviolet damage	0.96	0.95	0.97
Standard cell error	0.93	0.902	0.958
Current measurement error	1.0	0.98	1.02
Solar constant	1.0	0.965	1.035
Intensity correction	1.022	1.022	1.022
Voltage measurement error	1.0	0.98	1.02
Series resistance	0.98	0.98	0.98

The thermal-cycling degradation factor is 1.0 for the first day in orbit calculations and 0.982 for all other times.

The solar-array design factors are further discussed in Quarterly Technical Report No. 1. The tabulated values presented above are applicable throughout the orbital liftetime.

In the first quarterly report, two solar-array raw flux radiation damage calculations were defined for six, nine, and twelve months (1 year). The six months estimate for the 1963 raw flux radiation damage read incorrectly 4.06×10^{-12}. It should read 4.06×10^{-14}.

3. Regulated Bus-Load Capability

The appropriate solar-cell I-V curve, array temperature-time profile, battery charge and discharge data, and system design factors for a particular time in life, battery temperature, and selection of design factors (nominal, worst or best case), along with several power-time load profiles constitute the input to the Nimbus-B Energy Balance Computer Program. The computer solves the applicable system equations at one-minute intervals in the orbit period, and prints out battery state-of-charge, accumulated ampere-minutes, battery, array, unregulated bus voltages and currents, and array power at two-minute intervals. One computer run is made for each load profile. The resulting printout for each run is inspected to determine if the proper battery C/D ratio was obtained for a given load. The power subsystem is in energy balance on a per orbit basis when the load power is satisfied, the battery has been overcharged by the proper amount and all voltages in the subsystem have been maintained within their permissible ranges.

a. POWER SUBSYSTEM AVERAGE POWER CAPABILITY

Figure 4 shows the general load profile that was used to determine the Nimbus-B average power capability. The same value of load power is specified for both satellite nighttime and daytime. In addition, the S-band transmitter load of 164 watts for 7.5 minutes is superimposed on the average power during the daytime portion of the orbit. In a typical 24-hour period, transmitter operation will occur about three times during satellite nighttime and about six times during satellite daytime, with the remaining four or five of the 14 orbits having no transmitter operation[3]. Therefore, basing energy-balance calculations on a transmitter load during the daytime portion of every orbit is a conservative assumption.

Several values of average load power were used for the computer input for each combination of battery temperature, orbit lifetime and design factor selection; thereby zeroing in on the maximum average load, the spacecraft can sustain and still be in energy balance. Figures 5, 6, and 7 present the average power that may be obtained from the regulated bus versus time in orbit for battery temperatures of 25°, 15°, and 35°C, respectively. Each figure shows the available power for nominal, worst-case, and best-case system design factors.

b. BALANCE BETWEEN DAY POWER AND NIGHT POWER

The load profile of Figure 4 was changed to determine what combinations of load power during satellite nighttime and satellite daytime could be supported with the power subsystem still remaining in energy balance. Transmitter operation during

---

(3) Nimbus "C" Power Summary Report No. 1, G. E. Report No. 4713-040, dated January 5, 1965.

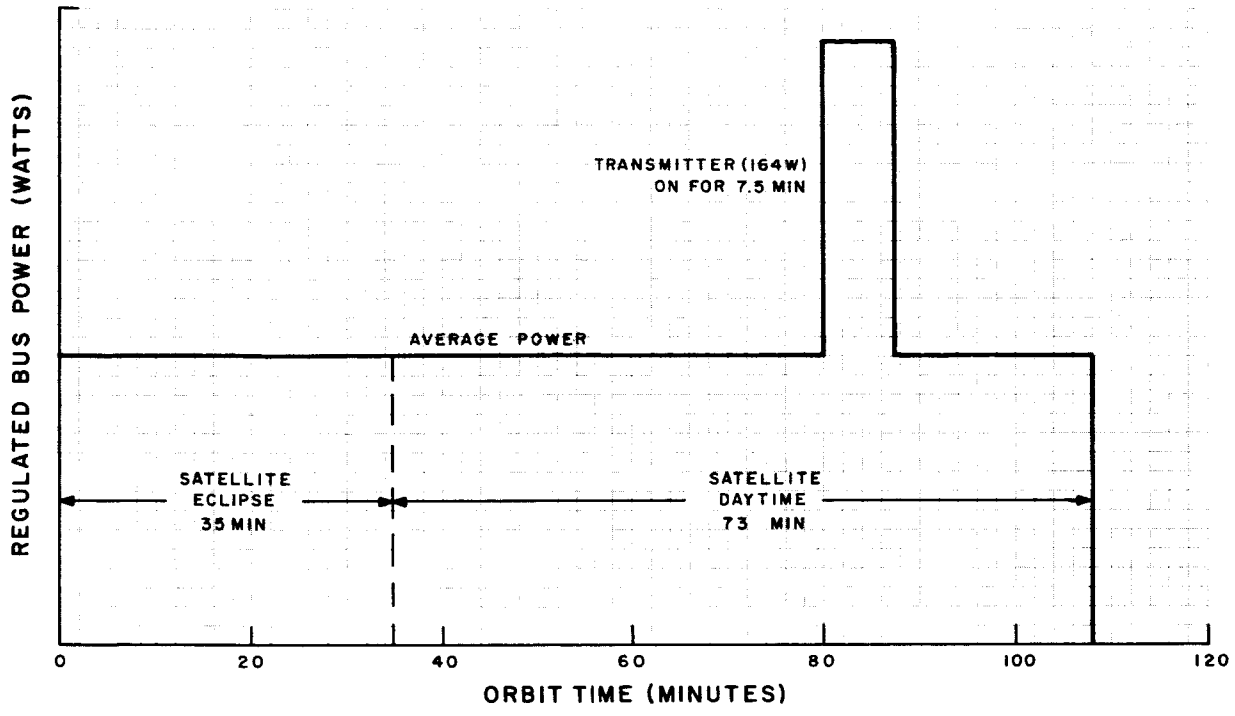


Figure 4. General Load Profile Used to Determine Nimbus-B Average Power Capability

satellite daytime was maintained in all cases. Figures 8, 9, and 10 show the balance of load power available during satellite nighttime and satellite daytime at 0, 6, 9, and 12 months in orbit with a 25°C battery for nominal, worst-case, and best-case system design factors. Equivalent curves for a 15°C battery are shown in Figures 11, 12, and 13, and in Figures 14, 15, and 16 for a 35°C battery.

4. Regulation

The PWM voltage regulator has been designed to supply steady-state d-c loads of up to 20 amperes at a voltage of -24.5 ± 0.5 volts for an input voltage range of -26 to -45 volts.(2) In the Nimbus-B power subsystem the most negative regulator input voltage (unregulated bus voltage) is limited by the shunt dissipator, which does not permit unregulated bus voltages to be less than -38 volts. The least negative regulator input voltages occur during satellite nighttime and are determined by the battery end-of-discharge voltage and the voltage drop between the battery and the unregulated bus.

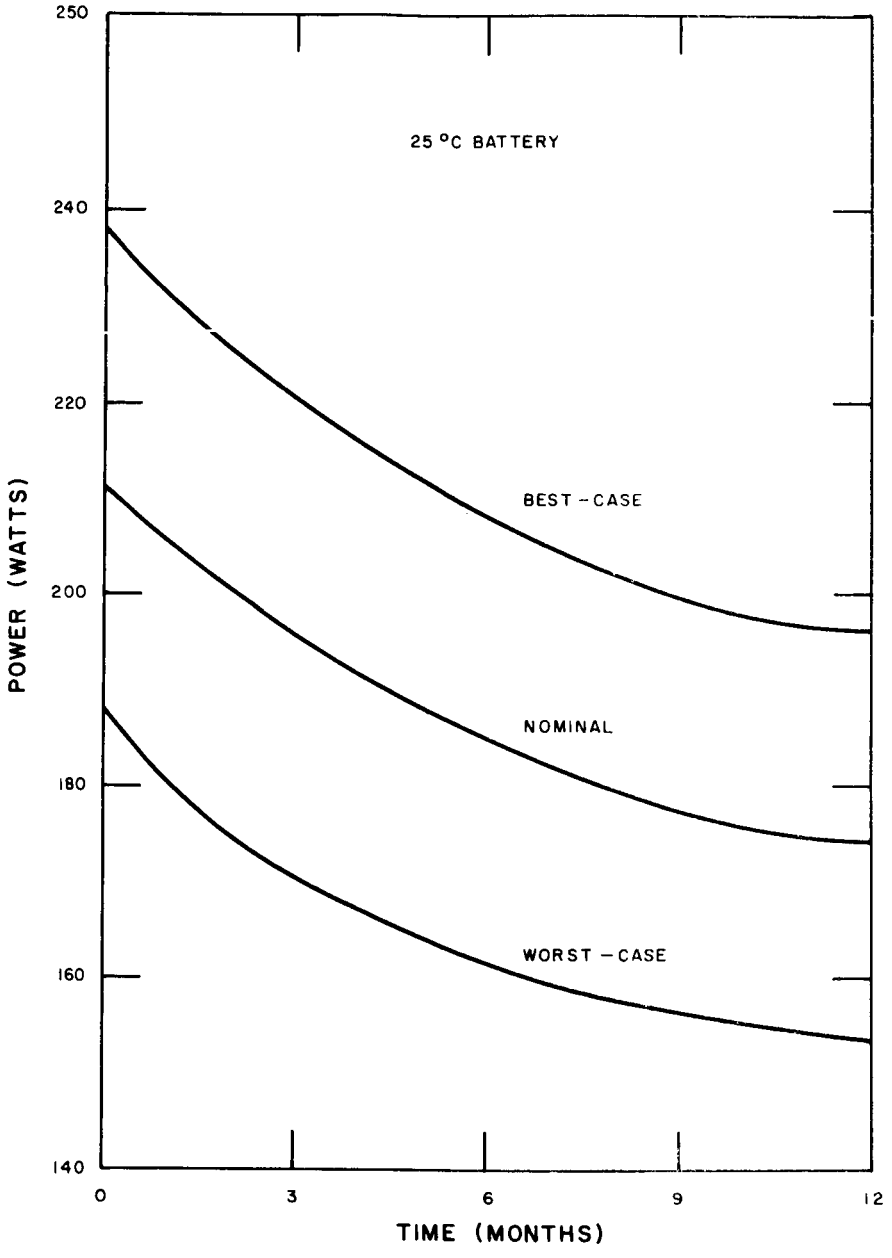


Figure 5. Regulated Bus Average Power Versus Time in Orbit Using 25°C Battery

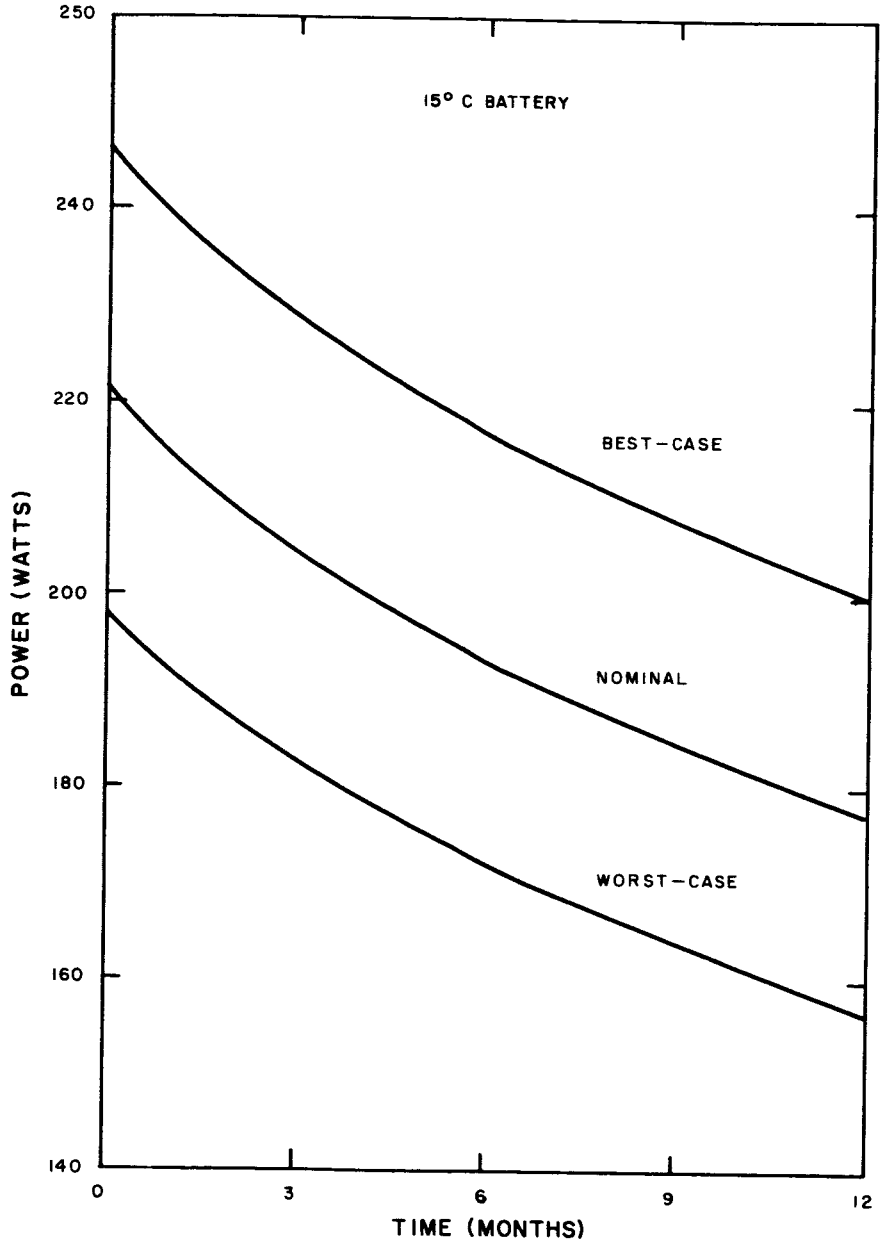


Figure 6. Regulated Bus Average Power Versus Time in Orbit Using 15°C Battery

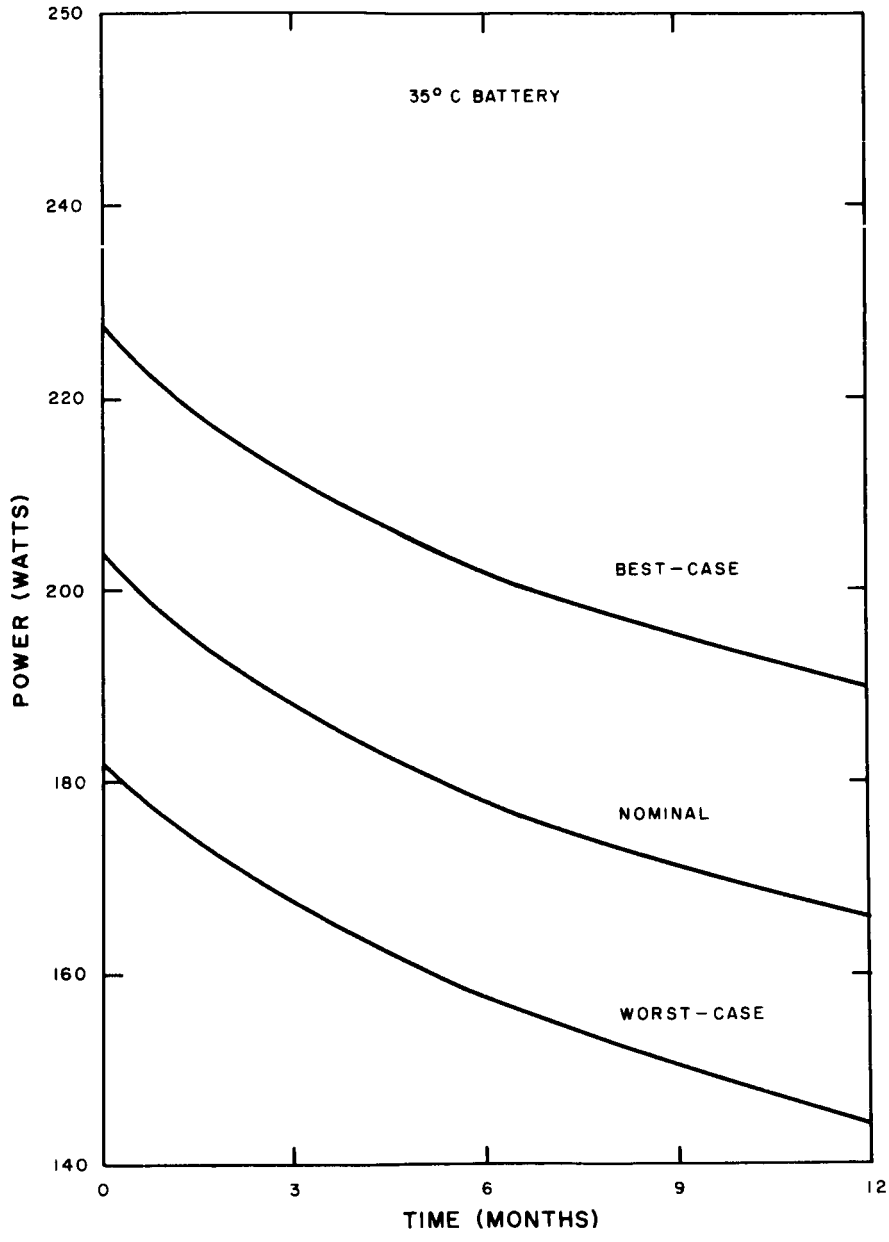


Figure 7. Regulated Bus Average Power Versus Time in Orbit Using 35°C Battery

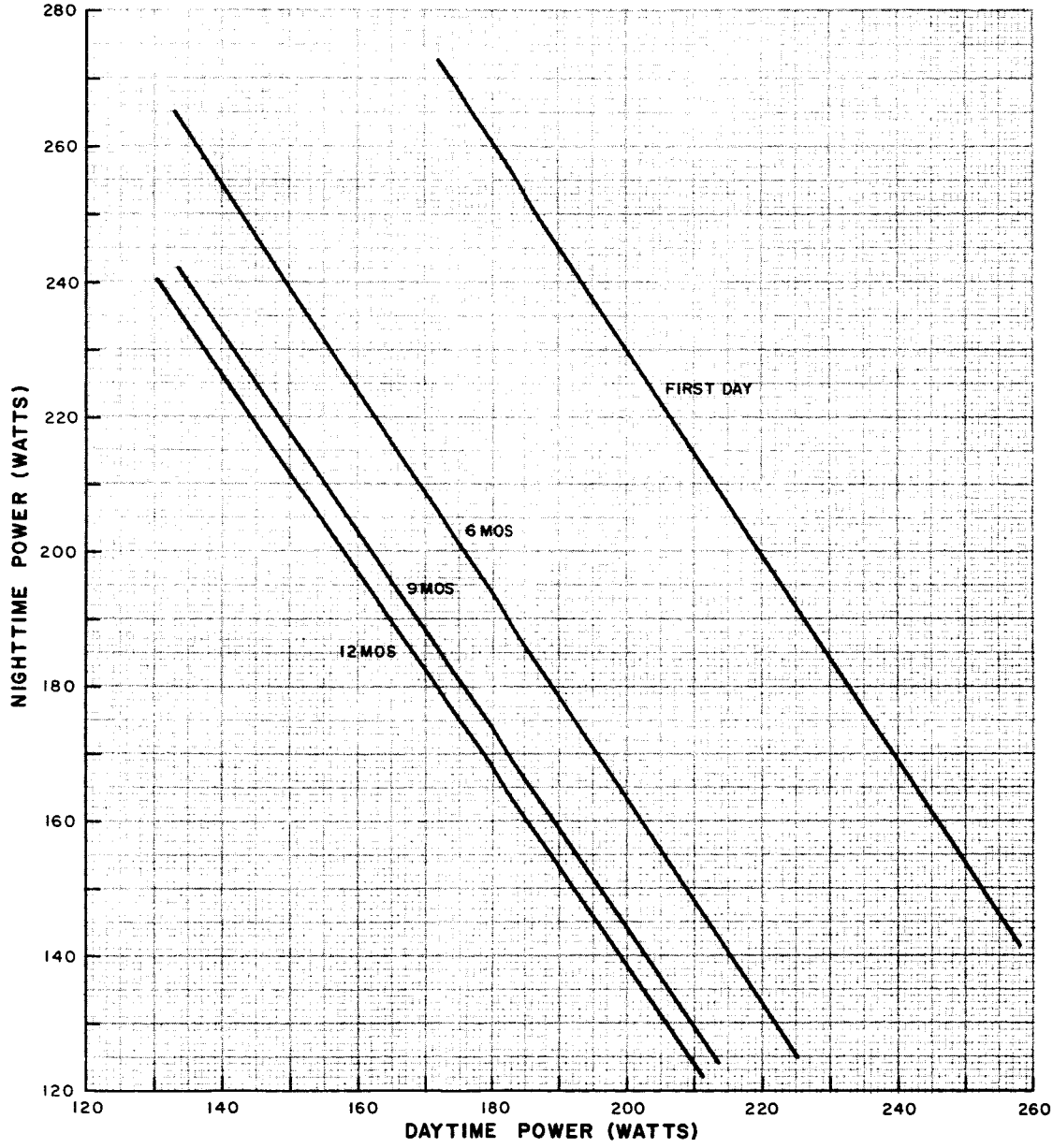


Figure 8. Power Subsystem Regulated-Bus-Load Capability with Nominal System Design and 25°C Battery for One-Year Orbital Life

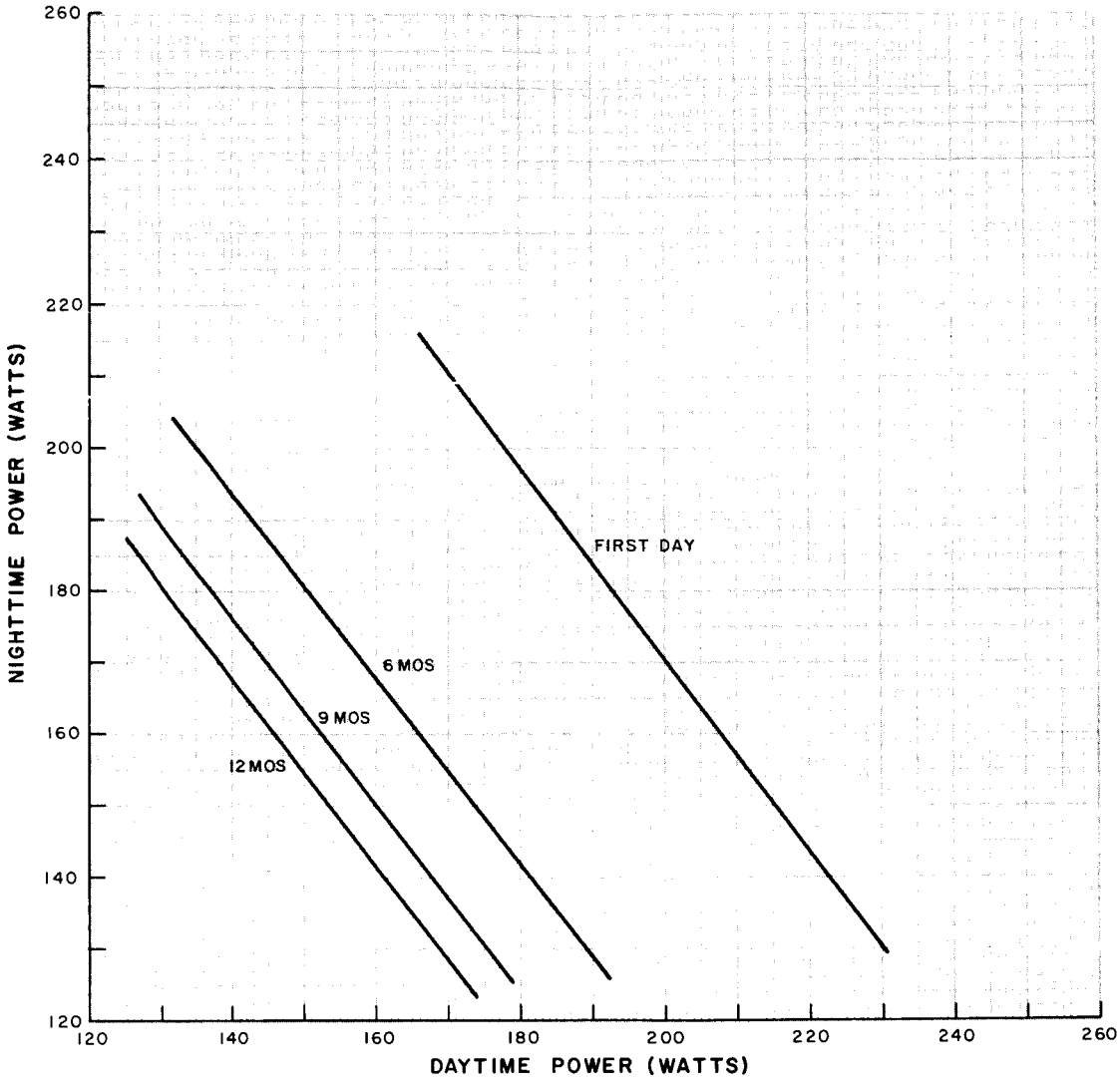


Figure 9. Power Subsystem Regulated-Bus-Load Capability with Worst-Case System Design and 25°C Battery for One-Year Orbital Life

Based on the predicted battery performance and the results of the energy balance computer runs, the following summary is made:

(1) The unregulated bus voltage is more negative than -26.0 volts for all values of regulated bus, average load power shown in Figures 5, 6, and 7.

(2) With a 15° and 25°C battery temperature, the unregulated bus voltage is more negative than -26.0 volts for all values of satellite day and night load power shown in Figures 8 through 13 for nominal, worst-case, and best-case design factors for one year of satellite operation.

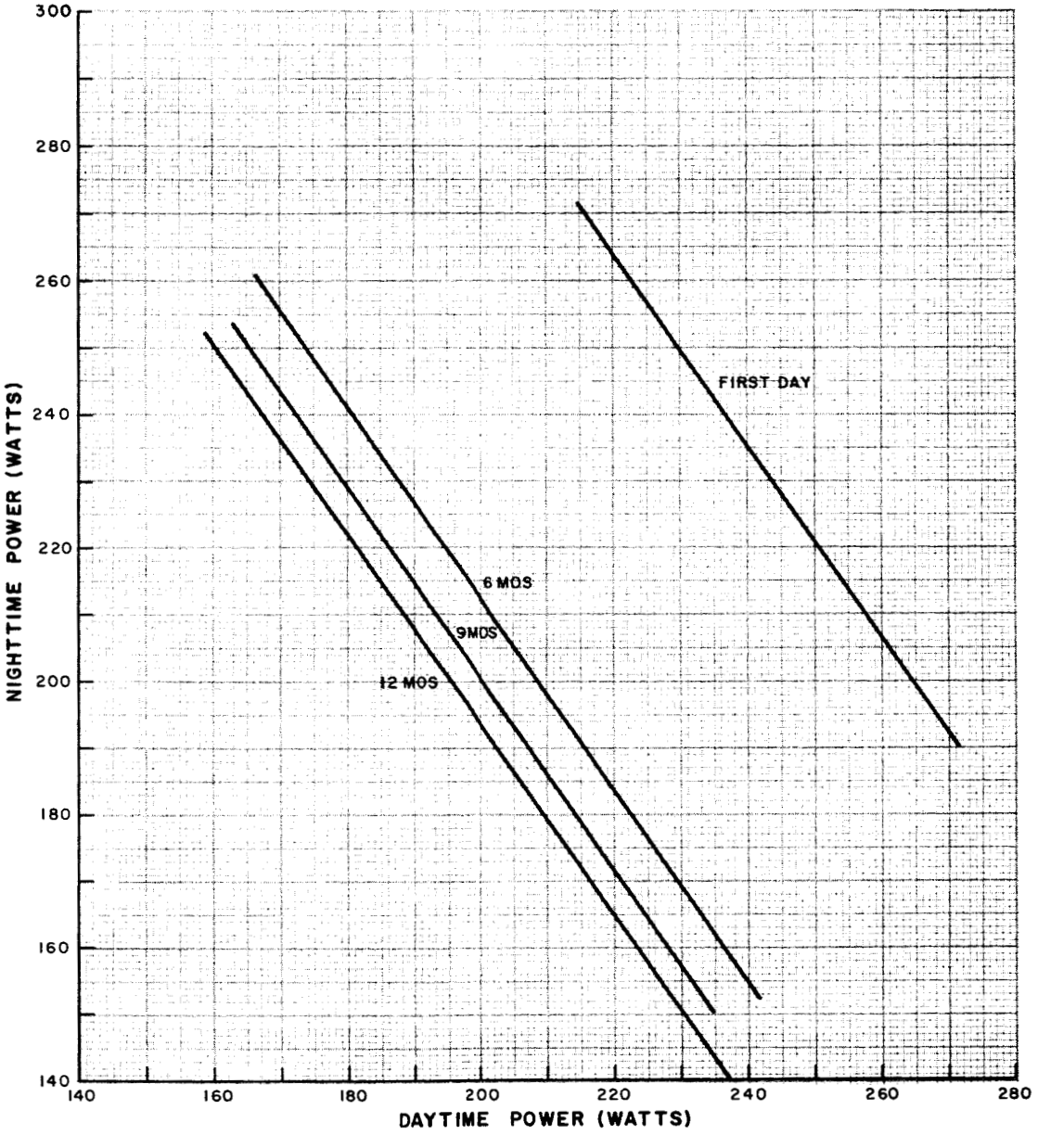


Figure 10. Power Subsystem Regulated-Bus-Load Capability with Best-Case System Design and 25°C Battery for One-Year Orbital Life

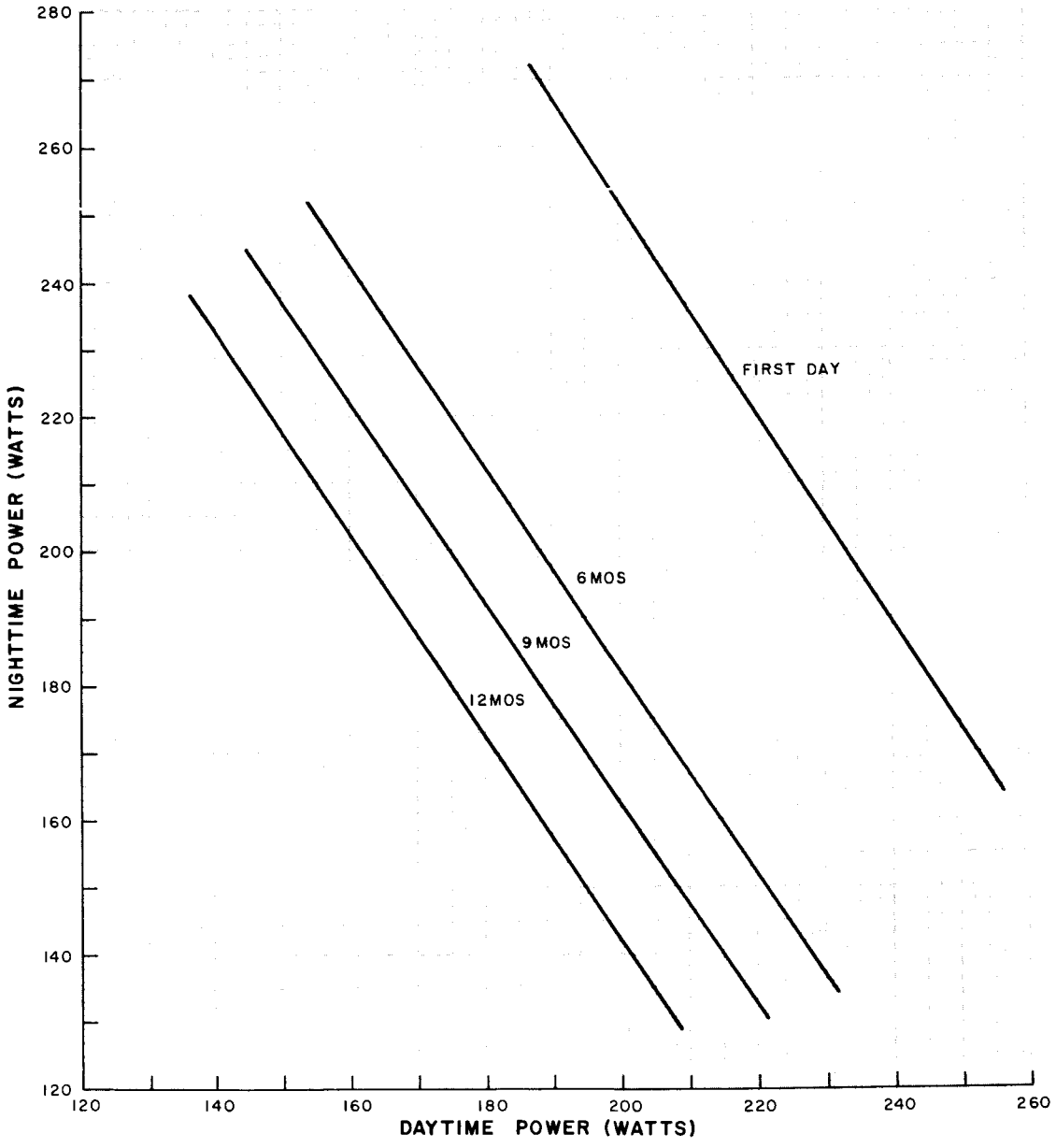


Figure 11. Power Subsystem Regulated-Bus-Load Capability with Nominal System Design and 15°C Battery for One-Year Orbital Life

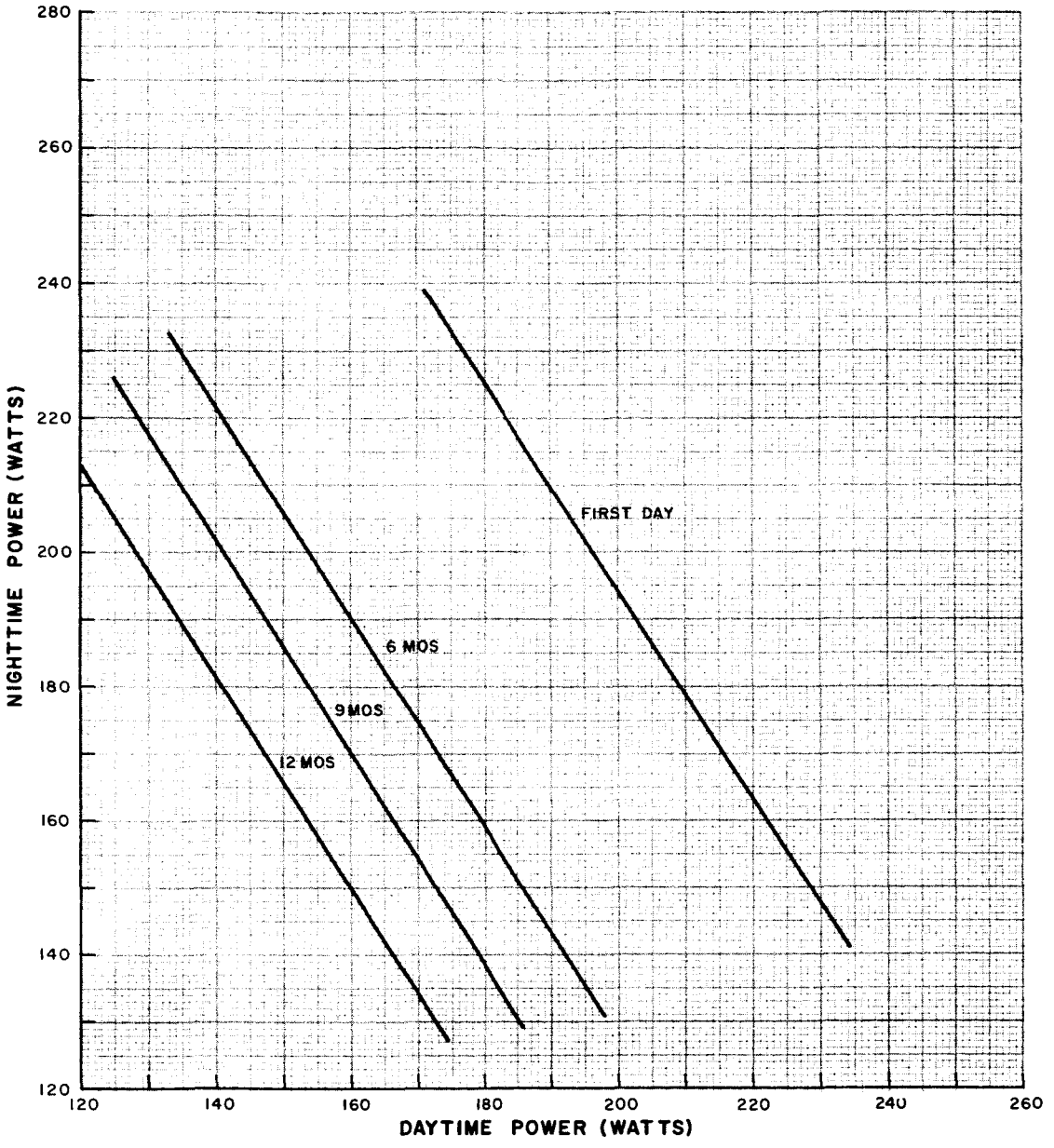


Figure 12. Power Subsystem Regulated-Bus-Load Capability with Worst-Case System Design and 15°C Battery for One-Year Orbital Life

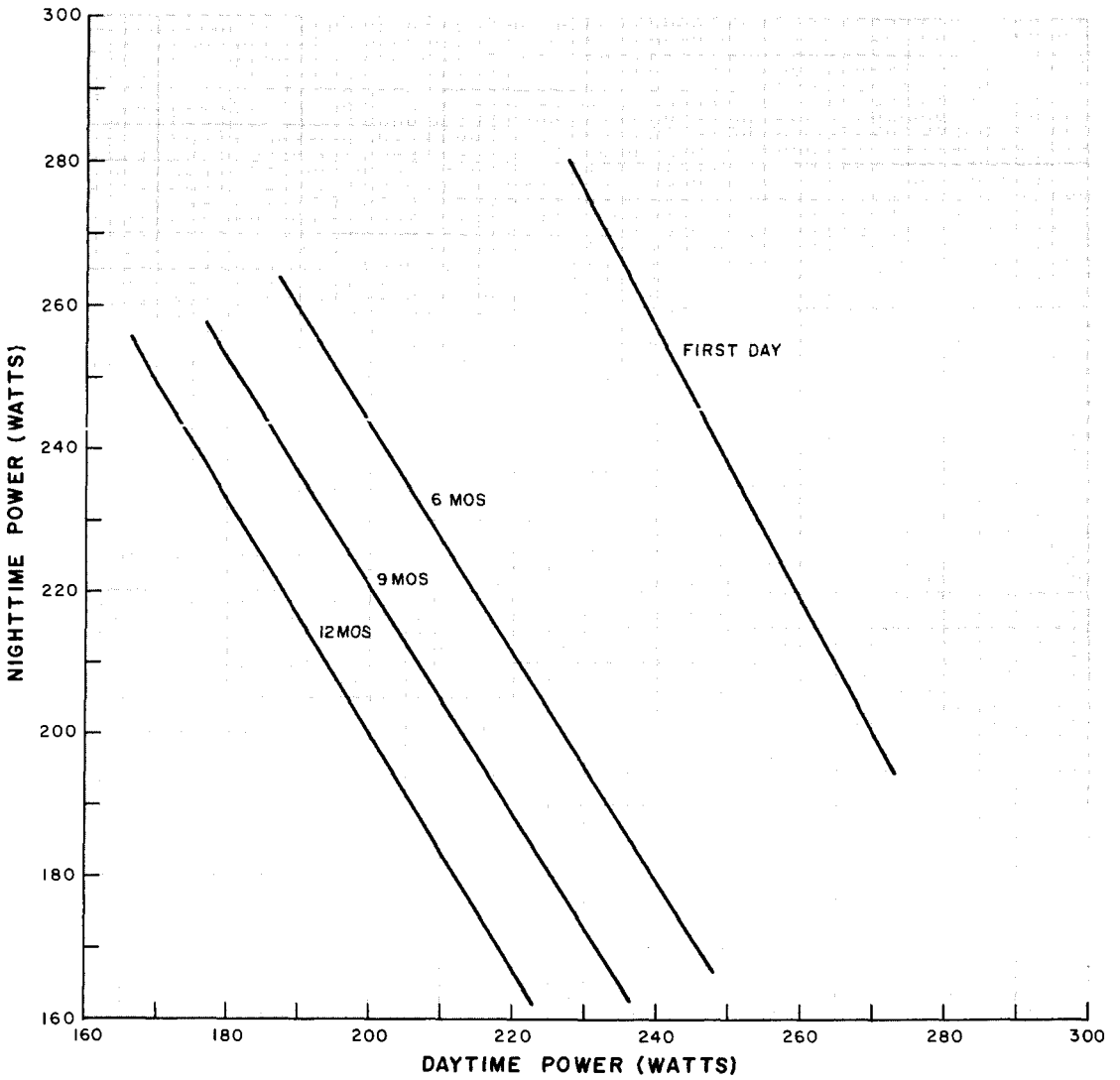


Figure 13. Power Subsystem Regulated-Bus-Load Capability with Best-Case System Design and 15°C Battery for One-Year Orbital Life

(3) With a 35°C battery temperature, the unregulated bus voltage is more negative than -26.0 volts for all values of satellite day and night load power shown in Figures 14, 15, and 16 for nominal, worst-case, and best-case design factors for nine months of satellite operation.

(4) At the end of one year of satellite operation with a 35°C battery temperature, the unregulated bus voltage is more negative than -26.0 volts for all values of satellite daytime load power shown in Figures 14, 15, and 16 for nominal, worst-case, and best-case design factors. However, during satellite nighttime operation after one year in orbit, the unregulated bus voltage will be more positive than -26.0 volts for regulated bus loads greater than 150 watts. With a 200 watt load, the unregulated bus voltage is estimated to be -25.7 volts at the end of a 35-minute nighttime discharge.

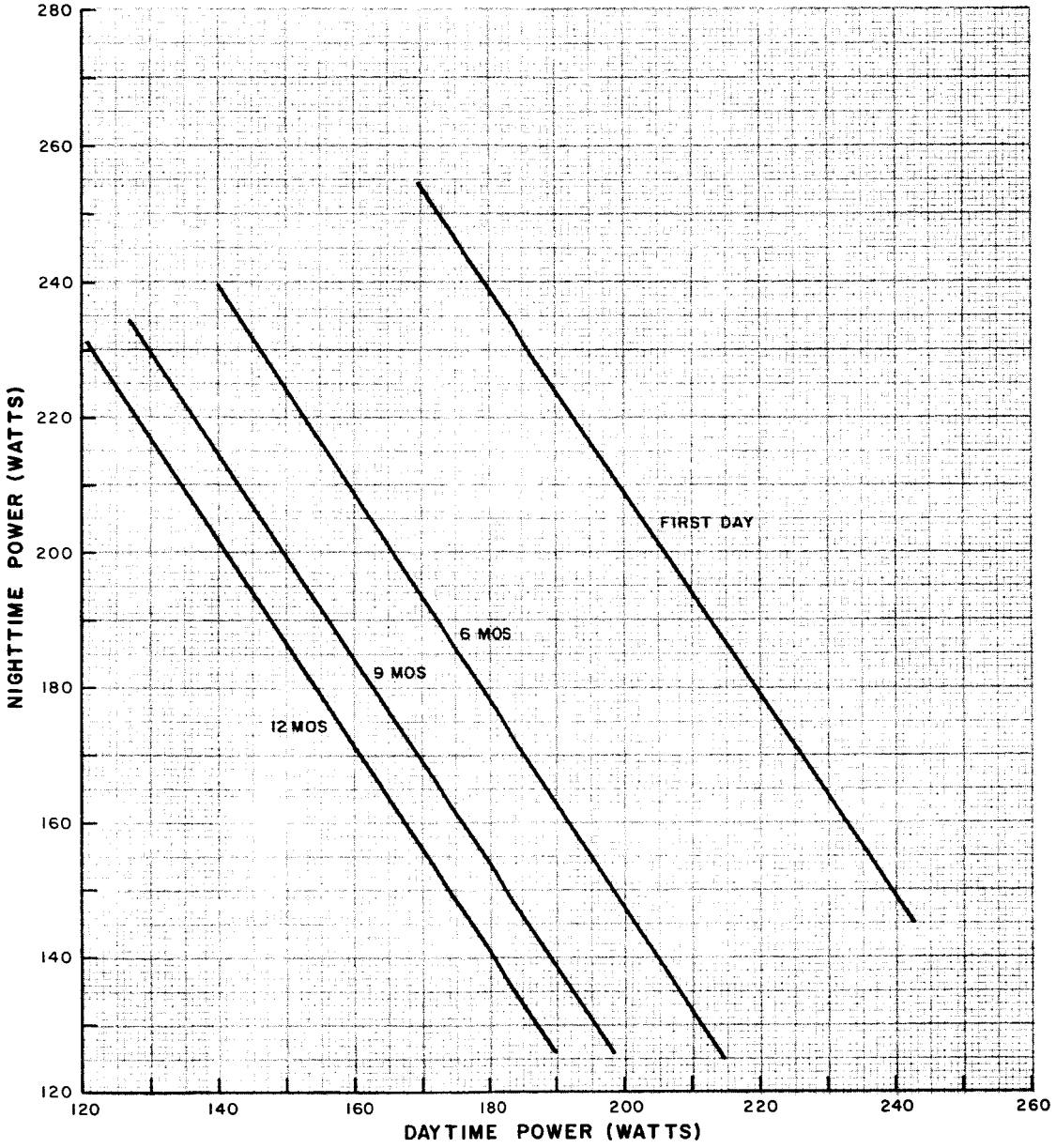


Figure 14. Power Subsystem Regulated-Bus-Load Capability with Nominal System Design and 15°C Battery for One-Year Orbital Life

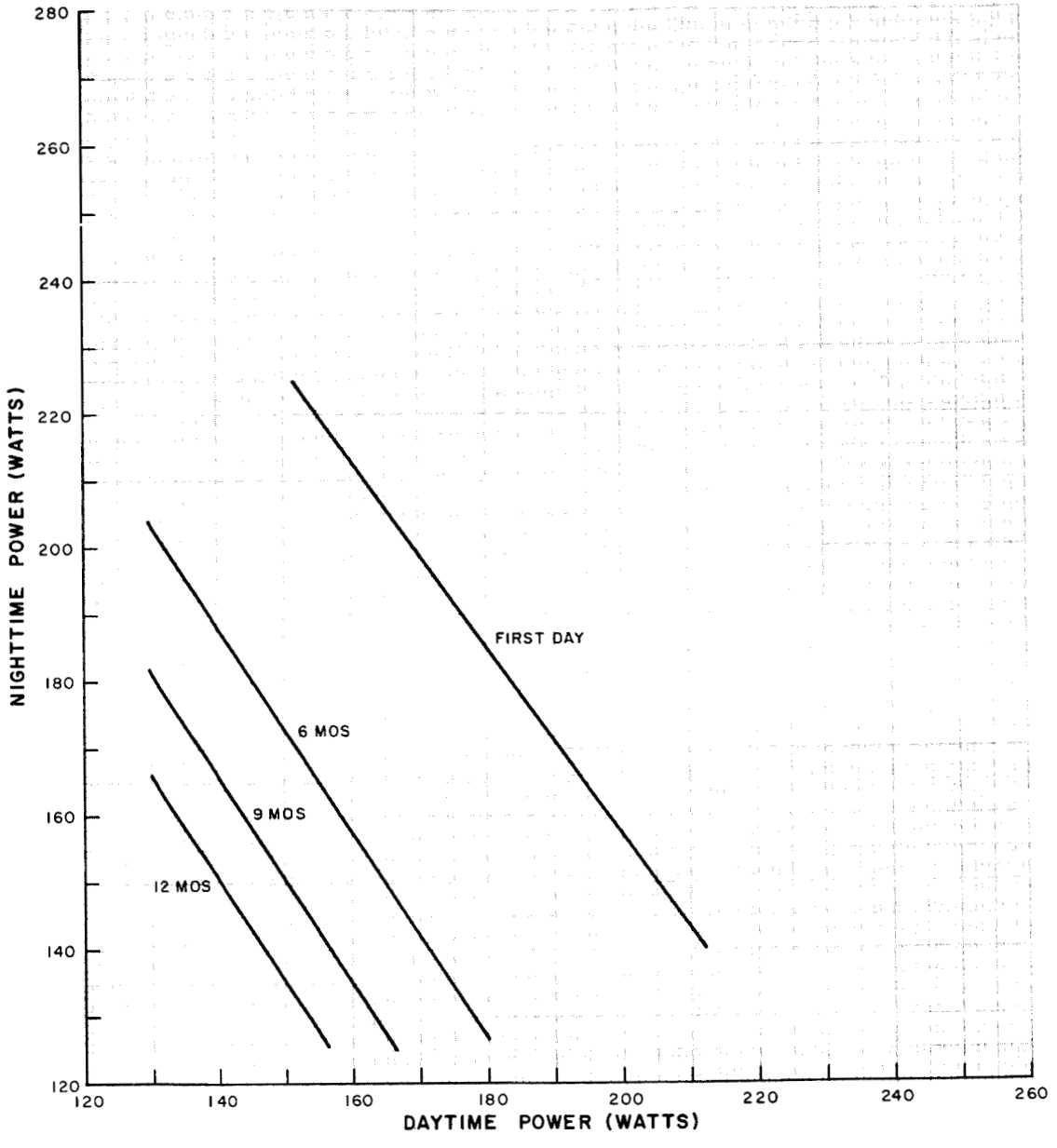


Figure 15. Power Subsystem Regulated-Bus-Load Capability with Worst-Case System Design and 35°C Battery for One-Year Orbital Life

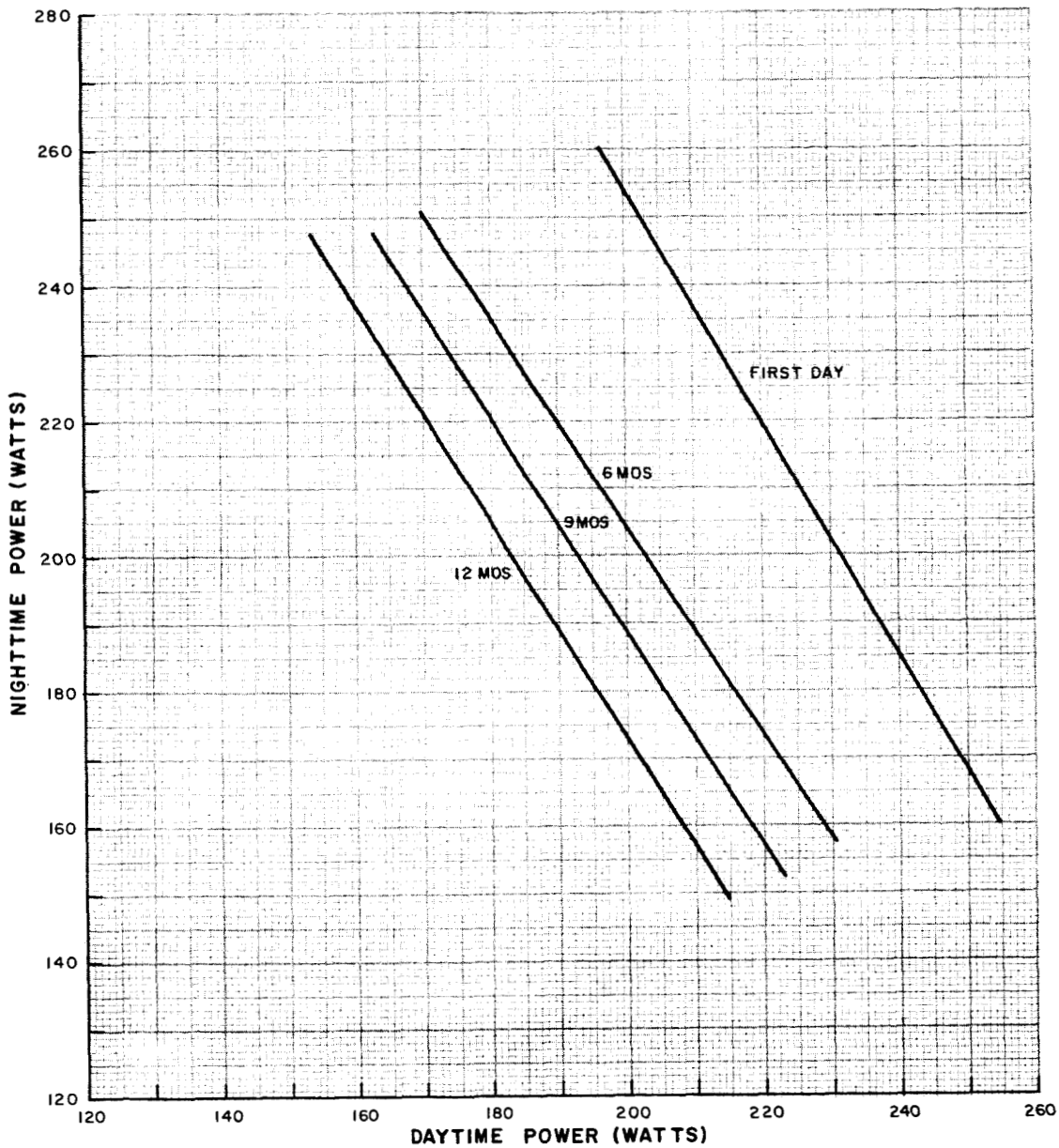


Figure 16. Power Subsystem Regulated-Bus-Load Capability with Best-Case System Design and 35°C Battery for One-Year Orbital Life

5. S-Band Transmitter Operation

Normal, once-per-orbit operation of the S-band transmitter during satellite daytime, nighttime, or transition period can be maintained for one year in orbit for all anticipated normal power subsystem conditions without adversely affecting energy balance or violating the PWM regulator input voltage requirements. Because of the geographical locations of both the Gilmore Creek and Rosman, North Carolina, ground stations, nighttime interrogation of the spacecraft can occur only during the first half of the satellite eclipse period. During this time, even at one year in orbit, the battery is only slightly discharged (up to 6 or 7 percent), and the battery voltage is sufficient to ensure -26 volts on the unregulated bus with the transmitter load on.

6. Power Subsystem Operating Point

The voltage on the solar-array I-V curve at which the Nimbus-B power subsystem will operate is determined by the battery-charge voltage at that charge current available after the regulator load has been satisfied. Typically, the array-operating voltage will range between -30 and -35 volts during an orbit, depending on battery state-of-charge and temperature. Near the end of satellite life (9 to 12 months), the array will supply power within a few watts of its maximum available power during a large portion of satellite daytime. At 12 months, and worst-case conditions, the array maximum power varies between 342 and 360 watts during the last 50 minutes of the daytime portion of the orbit, due to array temperature change. The power delivered to the subsystem varies between 341 and 358 watts during this time. This indicates that the Nimbus-A array series parallel configuration (adopted for use on the Nimbus-B solar paddles) is a near-optimum design, allowing almost all of the converted solar energy to be delivered to the solar-array bus at end of life.

7. Power Subsystem Operation with Six and Eight Storage Modules

The Nimbus-B power subsystem has been designed for nominal operation with seven storage modules. The effect on subsystem performance of having six or eight operational storage modules is presented below.

a. SIX-MODULE SYSTEM

Subsystem operation with six battery modules instead of seven would result in approximately a 2 to 3 percent deeper depth of discharge during satellite nighttime. Typically, this would increase the amount of battery discharge from 15 to 17.5 percent, which would not adversely affect the battery-life cycling capability. As a result of the deeper discharge, the battery end-of-discharge voltages may be a few (1 to 3) tenths of a volt lower than with a seven-module system. Based on the predicted battery performance, the unregulated bus voltage, with a six-module

system, will not drop below -26.0 volts except at end of life (1 year) with a 35°C battery temperature. Energy balance in the power subsystem will not be affected by operation with six modules since the same number of ampere-minutes of recharge current will be available as with a seven-module system.

b. EIGHT-MODULE SYSTEM

The additional battery capacity of an eight-storage module subsystem would yield a smaller depth of discharge and, consequently, slightly higher end-of-discharge battery voltages. Better regulation at end of life with a 35°C battery temperature would occur. However, greater nighttime regulated bus loads cannot be supported with an eight-module system because of the limitations imposed by solar-array power available for recharging the batteries.

8. Summary

The system design factors and the assumptions made in order to predict the Nimbus-B power subsystem performance have been presented. The regulated bus power available to the various spacecraft subsystems has been determined for the range of battery temperatures and tolerance of design factors anticipated for one year of orbital operation. The balance between power available for nighttime and daytime use has been defined so that the scheduling of experiment turn-on can extract maximum usefulness from the available converted and stored solar energy. Because of the high capacity of the Nimbus-B batteries and the fact that the power subsystem is array-limited, the subsystem can support the defined regulated bus loads with a six, seven, or eight-storage module system. Normal daytime and nighttime operation of the S-band transmitter can occur for one year. Unregulated bus voltage requirements for proper PWM regulation are maintained under all conditions, except for a slightly low end-of-nighttime voltage at end of life with a 35°C battery temperature.

B. SHUNT DISSIPATOR

The purpose of the shunt dissipator in the Nimbus-B power subsystem is to limit the maximum voltage that may appear on the solar-array bus. During conditions of low spacecraft power demand, the power subsystem operating point will attempt to move along the solar array I-V curve in a direction towards the array open-circuit voltage. For a current demand of five amperes, the operating point could be at array voltages exceeding -60 volts at cold-array temperatures. The two important parameters governing the design of the shunt dissipator are: (1) the threshhold voltage, and (2) the amount of power to be dissipated.

1. Threshold Voltage Range Determination

The most negative operating voltage that can be tolerated in the power subsystem is defined by the auxiliary regulator input voltage requirement. The Advanced Voltage Regulator report[2] defines the most negative voltages as -40 volts. Assuming a transconductance value of 25 mhos in the shunt dissipator and a maximum array current of 15 amperes, the most negative limit of shunt-dissipator threshhold voltage on the solar-array bus is -39.5 volts.

Data supplied by the AED Battery Group show that the maximum safe charging voltage for the Nimbus-B battery at -5°C is -35.2 volts. A temperature of -5°C is the coldest anticipated during testing of the Nimbus-B power subsystem and, therefore, the temperature at which the highest battery voltages will be encountered. The minimum voltage between the battery and solar-array bus that will allow the maximum charge current (1.1 ± 0.1 amps) to enter the battery is estimated to be 2.4 volts, worst-case. To eliminate the possibility of not being able to charge at the maximum charge-current value, the least-negative shunt dissipator threshhold voltage is -35.2 ± 2.4 = 37.6 volts on the solar-array bus.

2. Determination of Maximum Power to be Dissipated

The maximum power dissipation requirement for the shunt dissipator is determined by conditions of cold array and open PWM regulator on the first day in orbit. With an open PWM regulator, the only spacecraft load is approximately one ampere into the auxiliary regulators. No battery charge current can exist since the -24.5-volt supply is at zero volts and the charge controller functions are inoperative. For a threshhold voltage of -39.5 volts, the total array current is determined as follows:

Array voltage = -39.5 + diode, slipring and harness loss
= -39.5 and -1.8 = -41.3 volts

$$\text{Voltage per solar cell} = \frac{41.3 \text{ volts}}{98 \text{ series cells}} = 0.422 \text{ volt}$$

Current per solar cell at 0.422 volt under conditions of maximum array output = 0.133 ampere

Total array current = 0.133 ampere x 112 parallel solar cell strings

Total array current = 14.9 amperes

Total current into the shunt dissipator is equal to the total array current minus the total load current. For the conditions being considered,

Shunt dissipator current = 14.9 -1 = 13.9 amperes.

The worst-case power dissipation requirement is the product of the solar-array bus voltage and the current into the shunt dissipator:

$$P_{max} \text{ (shunt dissipator)} = 39.5 \times 13.9 = 549 \text{ watts.}$$

Power dissipated for conditions of threshhold voltage at -37.6 and -39.5 volts for an open PWM regulator and minimum, normal spacecraft load has been calculated and is shown in Table 2. Minimum spacecraft load is defined as 108 watts at the regulated bus, 20 watts of shunt losses at the unregulated bus, and 700 milliamperes of trickle-charge current. The total load current for minimum spacecraft conditions and a threshhold voltage of -39.5 volts is determined as follows:

$$\text{Total load current} = \frac{108}{0.92\left[39.5 - 0.4 \text{ (diode drop between solar array bus and unregulated bus)}\right]} + \frac{20}{(39.5-0.4)} + 0.70 \text{ ampere,}$$

where: 0.92 is the power-conversion efficiency of the PWM regulator

$I_{T4} = 3.00 + 0.51 + 0.70$, or

$I_{T4} = 4.21$ amperes

Having obtained the total load current, the shunt dissipator power is found with the same procedure used in the open PWM regulator example. Shunt dissipator power requirements for values of threshhold voltage between the limit values may be determined by linear interpolation.

TABLE 2. SHUNT DISSIPATOR POWER REQUIREMENTS

Load Condition	Threshhold Voltage (volts)	Shunt Dissipator Power (watts)
Open PWM Regulator	-37.6	526
	-39.5	549
Minimum Spacecraft load	-37.6	398
	-39.5	421

C. POWER SUPPLY SYSTEM FAILURE MODE AND EFFECTS ANALYSIS

The Nimbus-B power supply subsystem as shown in Figure 17 was analysed to determine the effect on the system of various "black-box" malfunctions. Table 3 provides a description of what each black box includes. Table 4 (Intra-System Failures) and Table 5 (External Malfunctions) present the results of the study. The analysis was made of the system as it was defined on January 10, 1966. Any changes that were made since January 10 are not considered in this report.

It should be pointed out that specific "black box" output failures assumed were those most probable as determined by a cursory study of the circuits in each black box. If, after a failure mode and effects analysis is completed for each black box, there are output failure modes other than those covered in Table 3, further system investigation will be necessary.

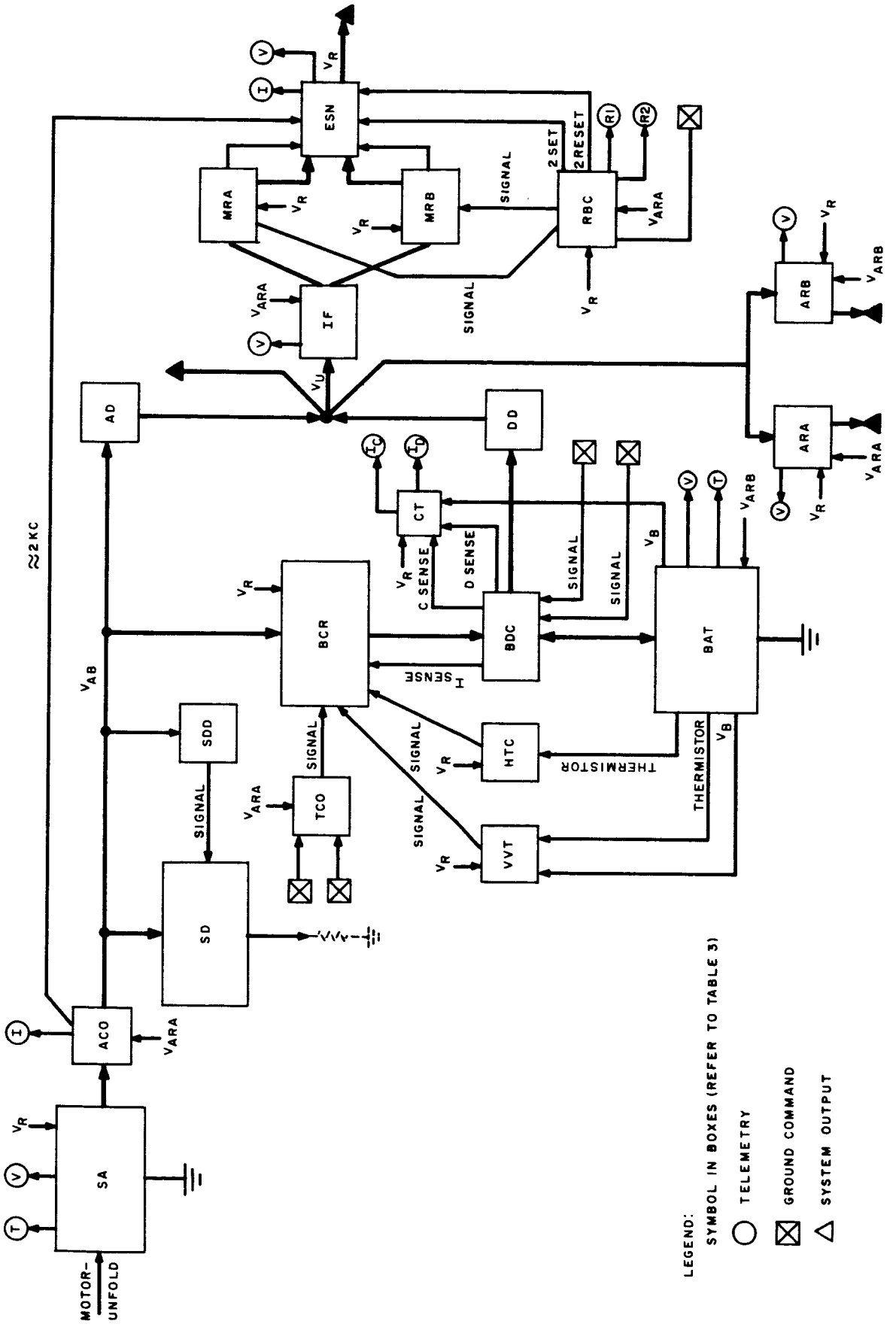


Figure 17. Nimbus-B Power Supply Failure Mode Functional Block Diagram

TABLE 3. POWER SUPPLY "BLACK-BOX" MALFUNCTION DEFINITIONS

Symbol*	Name	Description
SA	Solar Array	Solar cells, drive motors, temperature telemetry, voltage telemetry
ACO	Array Current T/M and Osc.	Array current T/M circuit, 2 KC oscillator
SD	Shunt Dissipator	Circuit which is part of the storage module
SDD	Shunt Dissipator Driver	Circuit which is part of the electronics module
BCR	Battery Charge Regulator	Charge control circuit
TCO	Trickle Charge Override	Circuit within electronics module
BDC	Battery Disconnect	Includes relay and charge and discharge sensing resistors.
BAT	Battery	Includes 23 cells and V_B T/M and T_B T/M circuitry
CT	Battery Current Telemetry	Includes charge and discharge current T/M circuits less sensing resistors
VVT	V_B V_{rs} Temp. Circuit	Battery protection circuit
HTC	Hi Temp Cut-off	Battery protection circuit
AD	Array Bus Diode	Array input to electronics module
DD	Discharge Diode	One diode for each storage module
ARA ARB	Aux. Regulator	Includes auxiliary regulator, voltage telemetry and gating diodes
IF	Input Filter	Consists of choke, capacitors and voltage telemetry.
MRA MRB	Main Regulator	PWM load bus regulator
RBC	Regulated Bus Comparator	Controls switching of main regulators
ESN	Energy Storage Network	Includes switching relay, output filter, regulated bus current and voltage telemetry.

* Refer to Figure 15.

TABLE 4. INTRA-SYSTEM FAILURES

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Solar Array (SA)	No deployment or partial deployment	Power supply will continue to operate and provide regulated bus for approximately 6.5 hours from launch (assuming 4.4 ampere minimum satellite load). At that time, regulated bus will begin to decrease to zero volts quite rapidly.	Array current and voltage T/M will be close to zero. Array temperature T/M will indicate lower than normal temperatures.
	Array bus shorted to ground	Same as above	Array current T/M may or may not yield any indication (depending where short is). Array voltage T/M will be zero.
	No regulated bus input to array temperature T/M.	Power subsystem will function normally but temperature T/M will be inoperative.	Array temperature T/M signal will be zero.
Array Current T/M (ACO)	No. 2 KC oscillator signal	Array current and regulated bus current T/M will be inoperative	Array current and regulated bus current T/M signal will be zero.
	Oscillator output drifts from 2 KC	If the frequency is higher than 2 KC, no detrimental effect will be noted. If the frequency is lower, the array current T/M and regulated bus current T/M performance will be degraded	None

T/M = Telemetry

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Shunt Dissipator (SD)	Shorted pass element in one module	There will be a continuous drain on the array bus of 1.5 to 2.0 amperes. At the beginning of life this may not limit full capability but at end of life there will definitely be the need for reduced programming of spacecraft loads.	No direct indication. May be detected if $I_A - (I_L + I_B \text{ Total} + I_{SH})$ is computed.
	Shorted diode (CR18) is one module.	The pass element in that module will always turn on first and will draw approximately .5a more than other pass elements. Therefore, this element will probably be cycled on and off with greater frequency that other shunt dissipator elements.	None
Shunt Dissipator Driver (SDD)	Shorted driver transistor	All shunt dissipator elements will be turned full ON thus loading the array bus. Batteries will discharge during satellite day in order to maintain regulated bus. If only minimum satellite loads are on, the regulated bus will be maintained for approximately 6.5 hours from inception of shorted transistor.	Charge current telemetry will always read 0 and discharge current T/M will be indicating battery discharge during satellite day.
	No driver output	Shunt dissipator elements will never turn on. The array bus will then rise, during periods of light load and low state of discharge of batteries, to	Array voltage T/M signal will indicate array voltages of greater than 40 volts.

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Shunt Dissipator Driver (SDD) (Cont'd)		between 45 and 55 volts (depending on array temperature and time in orbit). Main regulator, Aux. regulator and charge regulator input components will be overstressed and may possibly fail.	
	Threshold voltage is less than 38 volts	Batteries may not be fully charged each orbit. The maximum state of charge would be a function of battery temperature, array temperature, actual turn-on voltage of shunt dissipator driver and the spacecraft load requirement.	No direct indication. May be detected if $I_A - (I_L + I_{B_{TOTAL}} + I_{SH})$ is computed.
Charge Regulator (BCR)	Open pass element in one module	The battery in that module will not be charged and will not contribute to the load during satellite nite because its voltage will be lower than the rest of the batteries.	Charge current T/M signal will be zero.
	Shorted pass element in one module	That battery will charge at a higher rate than the others in the system and, as a result, will be fully charged earlier in the orbit. The amount of overcharge (since no current cutback will be possible) will be determined by the load requirement, the initial state of charge of the batteries and the battery	Charge current and battery voltage T/M will be higher for that module than any other in system. Charge current will increase above 1.2 amps as other modules are cut back to trickle charge.

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Charge Regulator (BCR) (Cont'd)		temperature. It is possible for the module to receive overcharge at high rates - an undesirable condition at low battery temperatures. Explosive cell failure could occur.	
	Shorted diode in one module	During satellite day, the charging rate for this module will be slightly higher than for the others in the system but system performance will not be affected since the V_B vrs Temp circuit will cut back the charge controller when the limits are reached. During satellite night, no detrimental effects will be observed.	None
Trickle Charge Override (TCO)	Open coil of relay	Effect will depend on initial position of relay and on which coil opens. If relay is in "normal" position and "normal" coil opens, T/C override command will be operative but a return to normal will be impossible. Effect on system will be determined by why batteries were in trickle charge to start with. If the "override" coil opens, T/C override command will be ineffective.	Charge current T/M signals will indicate inability to command T/C override or normal functions.

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Trickle Charge Override (TCO) (Cont'd)		If relay is in "T/C override" position and normal coil opens, it will be impossible to return the charge controllers to normal operation. If "T/C override" coil opens, a return to normal on command will occur but "T/C override" can never be reinstituted.	
	Contacts welded together	Relay will not actuate and will remain in its present position. Effect on system will be determined by cause which necessitated initiation of commands.	Charge current T/M will remain unchanged when command is sent.
Battery Disconnect (BDC)	Open charge current sensing resistor (one of two)	Charge current limiting will be at .6a (rather than normal 1.2a) for the particular battery module. The battery voltage and the charge current will both be less than that normally observed. As a result this battery may never reach a full state of charge but this should not be a problem since night time discharge will be less than the other batteries.	No direct indication.
	Open discharge current resistor (one of two)	Reduced depth of discharge for the module will result. No other detrimental effect will be noted.	No direct indication.

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Battery Disconnect (BDC) (Cont'd)	Open relay coil	This will result in inability to actuate the relay. Effect on system will be dependent on relay state when malfunction occurs and on which coil is open.	No direct indication.
Battery (BAT)	One cell shorted.	Battery voltage will be almost a volt less than normal. As a result higher charge current rates will be present. Remaining cells charge current will not be cut back when their safe voltage limit is reached. (Cut-back will probably not occur until limit has been exceeded by 5 or 6 mv on some cells). Effect could be catastrophic.	V_B T/M will indicate a battery voltage lower than the rest and a charging current higher than the rest.
	One cell open.	Module is inoperative since no discharge or charge current could pass thru the remaining cells.	V_B T/M would indicate zero volts and I_B T/M would indicate zero amperes.
I_B T/M	No I_C T/M voltage	No effect on system	I_C T/M = 0
(CT)	No I_D T/M voltage	No effect on system	I_D T/M = 0

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
V_B V T_B (VVT)	No output signal	Battery will not have charge current reduced when V_B safe limit is reached. Charging will continue until battery temperature rises to the cut-off value. Prior to that time catastrophic failure may have occurred.	I_C T/M will continue to indicate a charge current greater than trickle charge rate after V_B T/M has indicated safe V_B limit has been exceeded.
	Continuous high output signal	Battery will be locked in trickle charge. T/C override command will restore normal operation. No detrimental system effect will be observed.	I_C T/M will indicate trickle charge for the module while other modules will be charging normally.
Hi Temp Cutoff (HTC)	No output signal or grounded signal output	High battery temperature will not reduce charge rate to trickle charge. Charging rate will be established by V_B V_{rs} Temp circuit. No system detrimental effects will be noted unless battery thermal runaway occurs.	Charge rate will not be reduced to trickle charge when battery temperature is above +50°C.
Array Bus Diode (AD)	One diode open	Voltage drop across remaining diode will be greater than was present before but will be less than ≈1 volt. Minimum array voltage necessary to supply -26 volt input to Regulator will be slightly higher (by ≈.3 volts.)	No direct indication

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Array Bus Diode (AD) (Cont'd)	One diode shorted	The array bus shunt losses will be supplied by the batteries during satellite night (approx. 200 ma for system). The result will be 7-10 a-m additional discharge of the batteries. No system detrimental effects will be noted during satellite day.	No direct indication.
Discharge Diode (DD)	One diode shorted.	That particular module will supply a greater amount of the current during satellite night until its V_B is approximately .3 volts less than other modules. All modules will then contribute equally to the load. At end of life, this particular module may have cell reversals. During satellite day, this module will charge thru the discharge resistor at a relatively high rate with no charge limiting. Battery disconnect command will prevent overcharge failure.	No direct indication during satellite nite, but during satellite day, I_C T/M will read zero for that module.
	One diode open.	That battery will not contribute to the load during satellite night. No other detrimental effect will be noted.	I_D T/M will read zero.

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Aux. Reg. A (ARA)	Regulator output grounded or Regulator output open.	Array current, Regulated bus current, unregulated bus voltage and Regulated bus voltage telemetry will be inoperative. The regulated bus comparator will be unable to perform its intended function. Trickle charge override circuit will also be inoperative. System performance will be normal until T/C Override is commanded or until RBC is required to switch regulators.	No I_{AB}, I_R, V_U & V_R T/M Aux. Reg. T/M will be zero.
	Shorted pass element (Voltage output is unregulated bus voltage).	The regulated bus comparator would be effected by this failure. The nature of the effect would be dependent upon the unregulated bus voltage at the time of the failure and on the minimum and maximum voltages present during satellite day and satellite night. With 38-40 volts, and RBC will probably switch regulators and then be inoperative until V_U decreases to less than 30 volts.	Regulator operate T/M may read greater than 6.4 volts. Aux. Reg. T/M may indicate as high as 10 volts (if V_U = 39.5 volts) or as low as 6.6 volts (if V_U = 26 volts.)
Aux. Reg. B (ARB)	Regulator output grounded or open.	Battery voltage and temperature telemetry will be inoperative.	Aux. Reg. T/M will be zero and there will be no V_B or T_B T/M.

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Aux. Reg. B (ARB) (Cont'd)	Shorted pass element (Voltage output is unregulated bus voltage).	Battery voltage telemetry will be inaccurate on the high side.	Aux. Reg. T/M will indicate as high as 10 volts.
Aux. Reg. A or B	Gating Diode shorted	Aux. Regulator bus voltage will be 24.5 volts less the voltage drop across CR 57 or CR 59. There will be no detrimental effect on system operation unless other types of failures occur too.	
Input Filter (IF)	Open choke.	Permanent loss of regulated bus output.	V_U T/M is zero.
	Shorted Capacitor.	Permanent loss of regulated bus output.	V_U T/M is zero.
Main Regulator A or B (MRA & MRB)	$V_R \approx V_U$ (pass element shorted)	The RBC will switch regulators automatically during satellite day. During satellite nite when the battery voltage decreases to below 27.5 volts, the regulated bus will be near 26.5 volts. The RBC (extreme case) will switch only when the regulated bus is larger than 26.5 volts. Therefore, it is possible to have the regulated bus at 25 to 26.5 volts for a period up to 20 minutes duration before switching occurs (when spacecraft enters satellite day).	V_R T/M will indicate a bus voltage between 25 and 26.5 V during satellite night.

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Main Regulator A or B (MRA & MRB) (Cont'd)	$V_R = 0$	RBC will switch to other main regulator.	Reg. #1 and Reg. #2 T/M will indicate a change of condition.
Energy Storage Network (ESN)	No regulated bus output (open choke).	RBC will switch regulators but regulated bus will not return.	V_R & I_R T/M zero.
	Reg. Bus grounded (shorted capacitors).	RBC will switch regulators. New regulator in circuit will probably burn out. No further switching possible except on ground command which will burn out other regulator when it becomes active.	V_R & I_R T/M zero.
Regulated Bus Comparator (RBC)	No inhibit signal output.	If system is operating normally and a ground command is initiated to switch regulators, no detrimental effect will be observed. If switching occurs because of a shorted pass element, then arcing across the opening contacts could occur. Arcing in itself is not necessarily detrimental but the effect on the contacts could be (and might prevent closing of the contacts again).	"Reg. operate" T/M may be zero, but this would depend on reason for loss of inhibit signal.

TABLE 4. INTRA-SYSTEM FAILURES (Continued)

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Regulated Bus Comparator (RBC) (Cont'd)	No "set" signal.	When RBC switches regulators, the output from Reg. A will be disconnected from Reg. Bus, but the output from Reg. B will not be connected. Reg. Bus will be lost until a ground command can be initiated to return to Reg. A. During the period when Reg. Bus is zero, no battery charging will be possible and charge and discharge current T/M will be inoperative.	No direct indication.
RBC	No "reset" signal.	If RBC is required to switch regulators, the output of both Reg. A and Reg. B will be applied to the input of the Energy Storage Network. Since the cause of the "reset" signal loss may also remove the inhibit signal, the reason for switching will determine the effect on the system.	No direct indication.

TABLE 5. EXTERNAL MALFUNCTIONS

Functional Block	Failure/Malfunction	Effect on Power Subsystem	Telemetry Indication of Problem
Power Supply System	TCO command signal input grounded or open.	No adverse effect other than loss of command capability.	None
	BDC command signal input grounded or open.	Same as above.	None
	RBC command signal input grounded or open.	Same as above	None
	No unfold timer power to drive motors on paddles.	Paddles will remain in folded position. Regulated bus will be supplied by batteries for up to 6.5 hours.	Array voltage T/M will indicate low voltage and array current T/M will indicate very small current.
	Shorted fused load on regulated bus (including shorted RTG converter).	See paragraph F in Section II of this report.	---
	Shorted load on unregulated bus.	If load is fused, reduced unregulated bus voltage until fuse blows. If load is not fused, reduced unregulated voltage permanently. The amount of reduction will depend on what loads are on regulated bus as well as whether spacecraft is in satellite day or nite.	V_U T/M will indicate reduced unregulated bus voltage.

D. INVESTIGATION OF MULTIPLE OPERATING POINTS

During this report period, an analysis was performed to determine the possibility of multiple operating points in the Nimbus-B power system, and what problems might occur as a result of "lock-up".

1. Multiple Operating Points and Lock-up

It has been known for some time that constant-power load requirements of certain magnitudes can be satisfied by more than one point on the power system output characteristic. This conclusion is reached often when a careful graphical analysis of a power system is pursued, and where an I-V plot of a family of fixed-power load lines is superimposed on the I-V output characteristic of the power system. In many cases, such superimposition proves that some of these load lines intersect the output characteristic more than once, i.e. twice, three times, even five times. On the assumption that a power system can be operated on any part of its I-V output characteristic, the only limitation is that the required load power equals the available source power. Thus, there are as many possible operating points as there are intersections.

The assumption made concerning the ability to operate anywhere on the source characteristic cannot be definitely supported or rejected at this time. In other words, it can only be said, with reasonable accuracy, under what load conditions the multiple intersections can occur and where. However, it cannot be said whether any one of the two or more points of intersection is unique and, if so, which one.

The problem of "lock-up" is frequently mentioned in conjunction with the possibility of multiple operating points. In a general case, where several operating points are possible, some are less desirable than others. For instance, a constant-power hyperbola may intersect the output I-V characteristic in the battery charge voltage region at one point, and in the discharge voltage region at another, the latter being clearly the less desirable, or "lock-up" condition. A limited definition of lock-up can be made; a power system is said to be in lock-up whenever an alternate operating point is presumed to exist which would result in more favorable operating conditions of energy balance.

The simplified sketch of Figure 18 is drawn to examine various multiple-operating-point possibilities. The solar-array output characteristic is defined by curve I_{sc}-o-b-v_{oc}, the battery discharge characteristic by o-d, and the battery charge plus limiter by o-l-c (or by o-t-h, showing a lower limiter setting, for a subsequent illustrative purpose), where charge limiting occurs on the l-c (t-h) part of the curve.

The power system output characteristic at the PWM regulator input (block diagram shown in Figure 18 is d-o-l-c. The load characteristics at the same point in the power system are shown by constant-power lines: $P_1 > P_2 > P_3 > P_4$. The possible

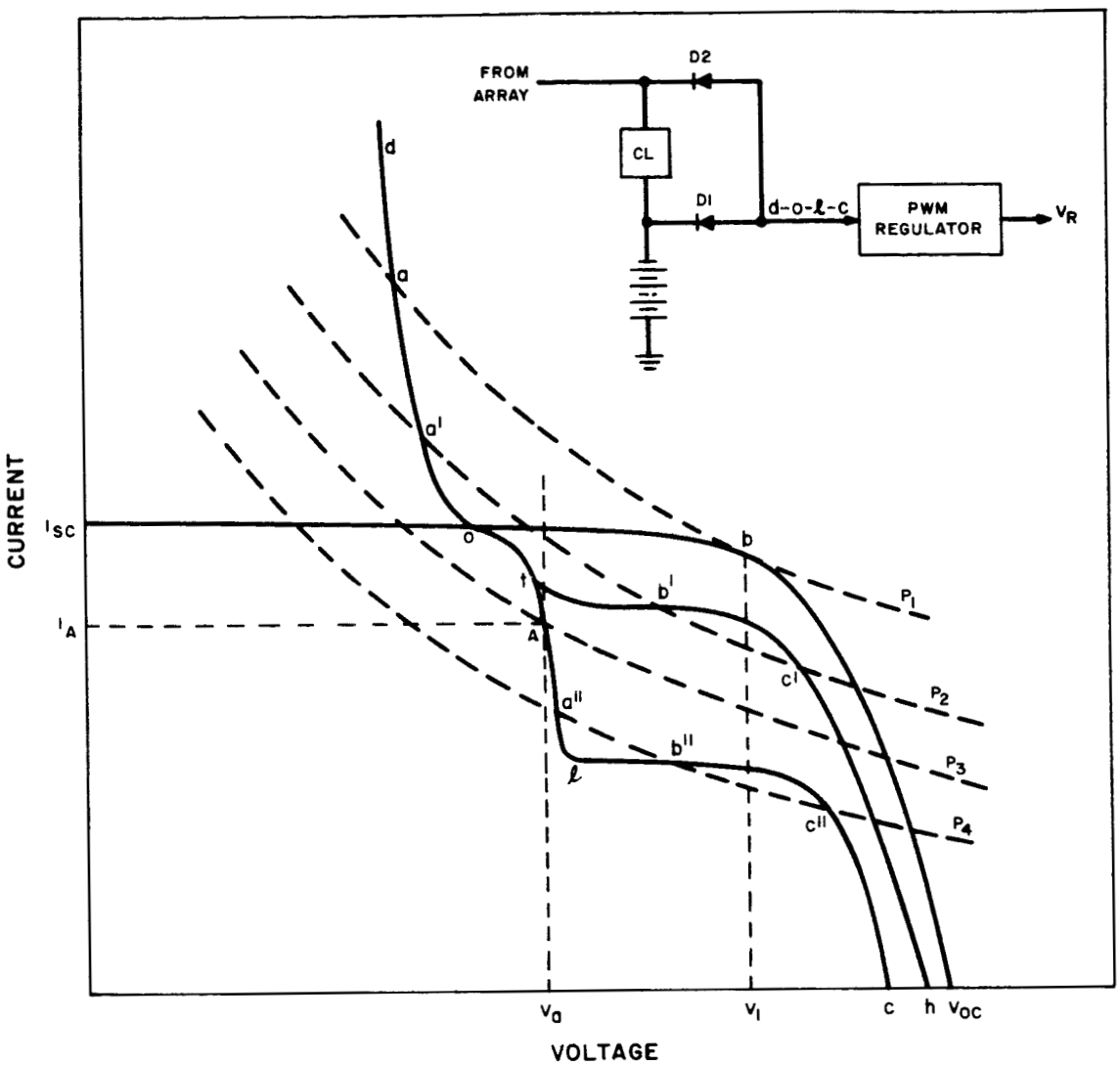


Figure 18. Power System Output Multiple-operating-Point Characteristic Curve

power system operating points at the regulator input are defined as the points of intersection of a load line with d-o-l-c. Construction details of both source and load lines are covered in paragraphs D.2 and D.4 of this section.

As shown in Figure 18, load demand P_3 (at regulator input) intersects the power system output characteristic d-o-l-c just once, at point A. There is, therefore, no question that the regulator input voltage is V_A and the input current I_A, that the battery is under charge and that the charge current is the difference between the array current at V_A (equal roughly to I_{SC}) and I_A, subject to the simplifying assumptions of ideal diodes and negligible power-system shunt losses.

A different situation is encountered if the power demand is P_4; the P_4 load line intersects the power system output characteristic three times, i.e., at a", b", and c". Assuming for the present that all three operating conditions are equally probable (the uncertainty associated with making this assumption has already been discussed), b" and c" are essentially the same to the extent that in each case the charge electronics is limiting, allowing maximum recharge in either case. The third possibility is a"; the battery is still under charge, but the charge electronics is not limiting, meaning that the amount of recharge is lower than at either of the other two possible operating points. Operating at a" is thus less advantageous, and, if operated there, the power system is considered as being in lock-up.

To illustrate a more drastic condition of lock-up, assume the power system characteristic be d-o-t-h instead, and the power demand be P_2. In the previous example (P_4 and d-o-l-c), the difference between the desired operation and lock-up was more and less charge, respectively: charge occurred in either case. In the example being considered (P_2 and d-o-t-h), both b' and c' mean full charge as did b" and c"; however with a', unlike a", means battery discharge. It is thus less desirable to be in a lock-up condition such as a', compared to a".

Finally, consider the power demand at the PWM regulator input to be P_1, such that the load requirement just matches the solar-array capability as shown by point b. Unlike the last two cases discussed, point a is not an example of lock-up in a power system such as Nimbus-B, since it is the only point where the system can operate if the demand is P_1. Even though the array is capable of supplying P_1 at voltage V_1, presence of V_1 at the input of a series-pass dissipative limiter (the type used in this system) would cause the flow of charge current to equal the current difference between curves o-v_{oc} and o-l-c (or o-t-h) and V_1. Diversion of some of the array output to the battery would result in available load power to be something less than P_1; the regulator action would kick the operating point over to "a", causing the battery to discharge. Stated a different way, a possible operating point exists only where the load line intersects the power system output characteristic such as d-o-l-c, provided both are drawn to reflect conditions at the same point of the power system.

In summary, the above discussion attemps to show what is and what is not considered a possible lock-up condition. A distinction was also made between two cases of lock-up: one, where the recharge is merely lower than indicated by the source capability; and the other, where the ability of the power system to supply both the load and charge the battery is not utilized altogether, resulting in a net discharge instead.

Reservations have been made concerning the assumption that an operating point exists whenever there is an intersection of a constant-power load line and the power system output characteristic.

2. Analysis of the Nimbus-B Power Subsystem Operation

a. TECHNIQUE AND APPROACH PLANS

Application of the technique developed in paragraph D.1 will be made to the Nimbus-B power subsystem. However, exact operating conditions will be reflected insofar as possible, approximations being made only to the extent that it is desired to examine the system in a state of typical operation, rather than all possible conditions of life, temperature, and state of charge.

Plots of the power-system output characteristics will be prepared over the significant voltage range, following which fixed load lines will be superimposed and intersections examined.

The advanced voltage regulator (AVR) input terminals will be selected as the most convenient reference point for evolving the details of the graphical analysis. At that point, it is most convenient to investigate the power-system output capability, and compare it with the load demand which appears at the AVR terminals as a family of curves approximating hyperbolas on an I-V plot.

Two specific conditions relative to the state of the power system will be analyzed: first, the beginning-of-life condition, using the reported I-V curves of the initial solar-array output and battery charge-discharge; and second, the end-of-life condition (at the end of 12 months in orbit) with corresponding array and battery characteristics. In both cases, worst-case array characteristics at +40°C will be used to correspond roughly to the equilibrium temperature condition; also, nominal battery curves, the latter drawn to approximate the conditions of +25°C battery temperature and a state-of-charge at 95 percent of full capacity. Nominal charge and shunt limiter characteristics, and

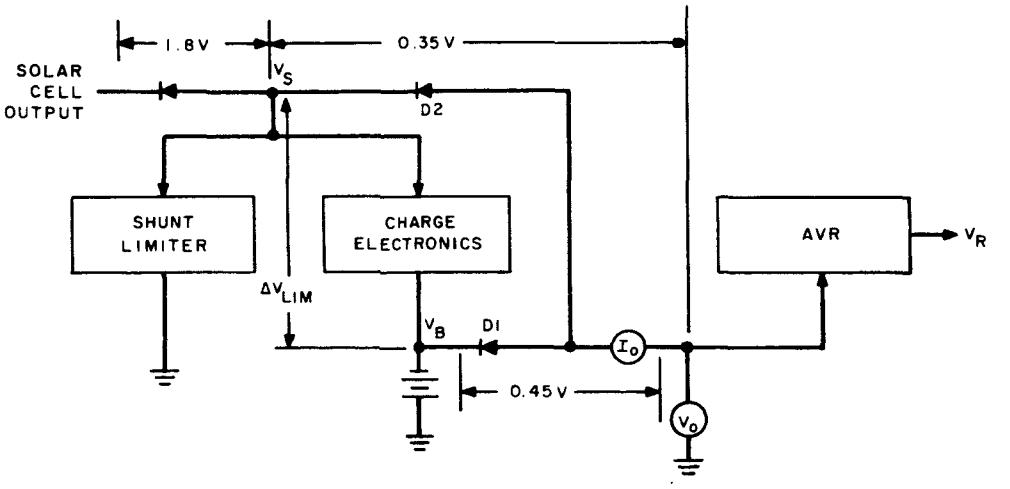


Figure 19. Power Subsystem, Simplified Block Diagram

latest reported electronics module efficiencies including AVR losses at room temperature will be used.

The simplified block diagram of the power subsystem is as shown in Figure 19, with assumed voltage drops across various parts of it as indicated whenever conducting.

Assumed shunt current losses in the subsystem (see Figure 19) are as follows:

(a) 22 ma per module at V_S,

(b) 22 ma per module at V_B, and

(c) 25 ma per module at V_R.

There are eight operating battery modules.

b. DISCUSSION OF THE CHARACTERISTIC CURVES

Figures 20 and 21, respectively, show the beginning and end-of-life conditions (I-V characteristics) at the AVR input. (Details of the construction of the various curves in Figures 20 and 21 are outlined in paragraph D.4)

As shown in Figure 20 (beginning-of-life conditions), when all batteries are capable of being fully charged, the power-system output characteristic is d-o-1-c. It is seen that, for all practical purposes, none of the fixed load lines intersect this characteristic more than once. There is, therefore, little chance of a lock-up under these conditions.

As the battery-charge controllers are reduced to trickle charge one by one, the 1-c portion of the output characteristic will move up; multiple intersections will occur, with fixed loads of around 250 watts or more, until all eight modules are in trickle charge, at which time the system output characteristic will be d-o-t-h. It can be seen in Figure 20 that the 325-watt load line intersects the latter three times, raising the possibility of a "minor lock-up" (as in paragraph D.1, for the P_4 condition at a"). It is significant to note that the lock-up condition described is not likely to occur until most of the batteries in the system are fully charged.

Close examination of the plots for the end-of-life conditions shown in Figure 21 indicates an even smaller chance of lock-up than at the beginning of life, owing primarily to the decreased voltage capability of the degraded array.

3. Summary and Conclusions

Conditions under which undesirable operation could occur have been determined. They apply over a broad range of loads bounded by approximately 250 watts at the low end and about 350 watts at the high end. Within this broad range, there is

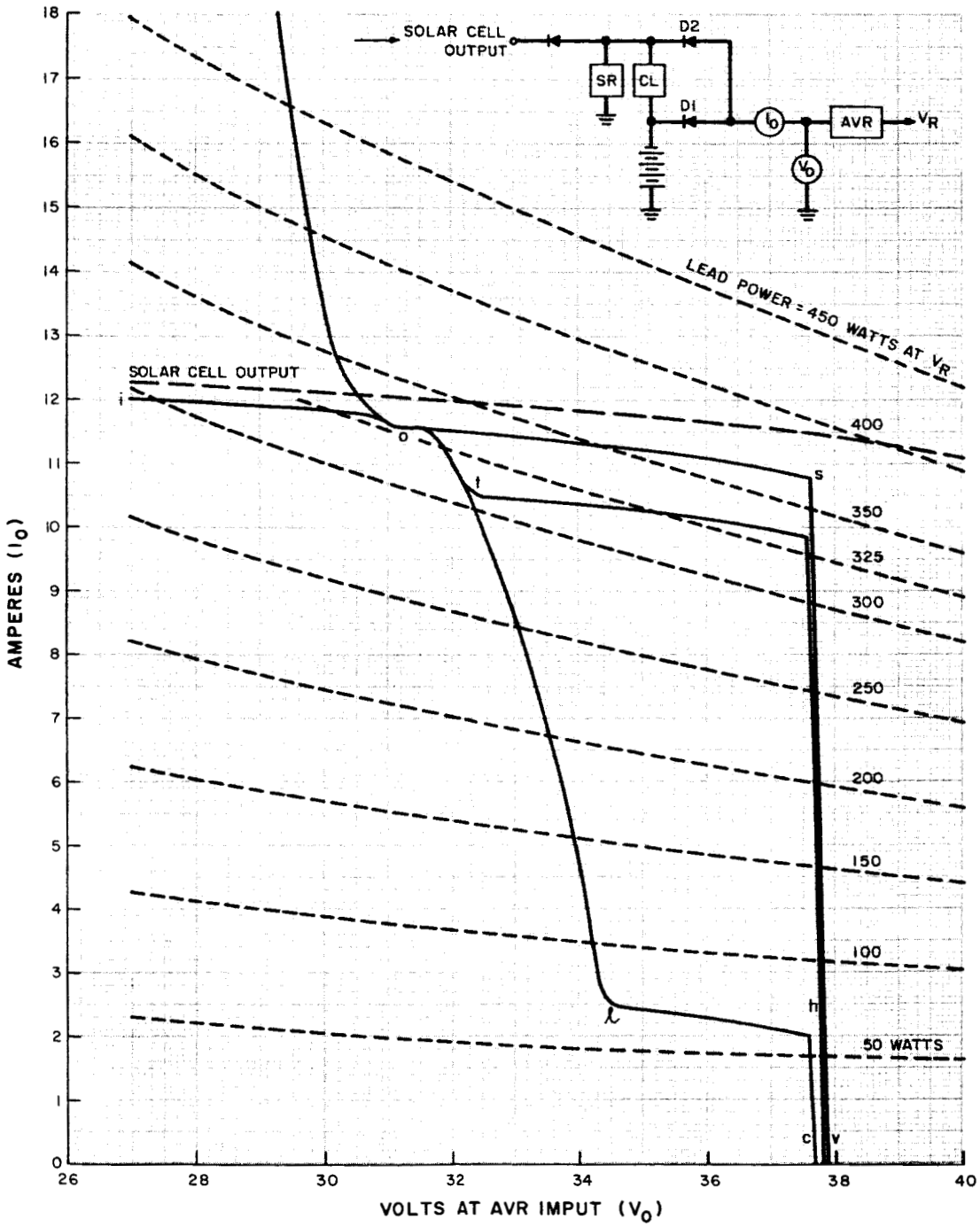


Figure 20. Beginning-of-Life I-V Characteristics at AVR Input

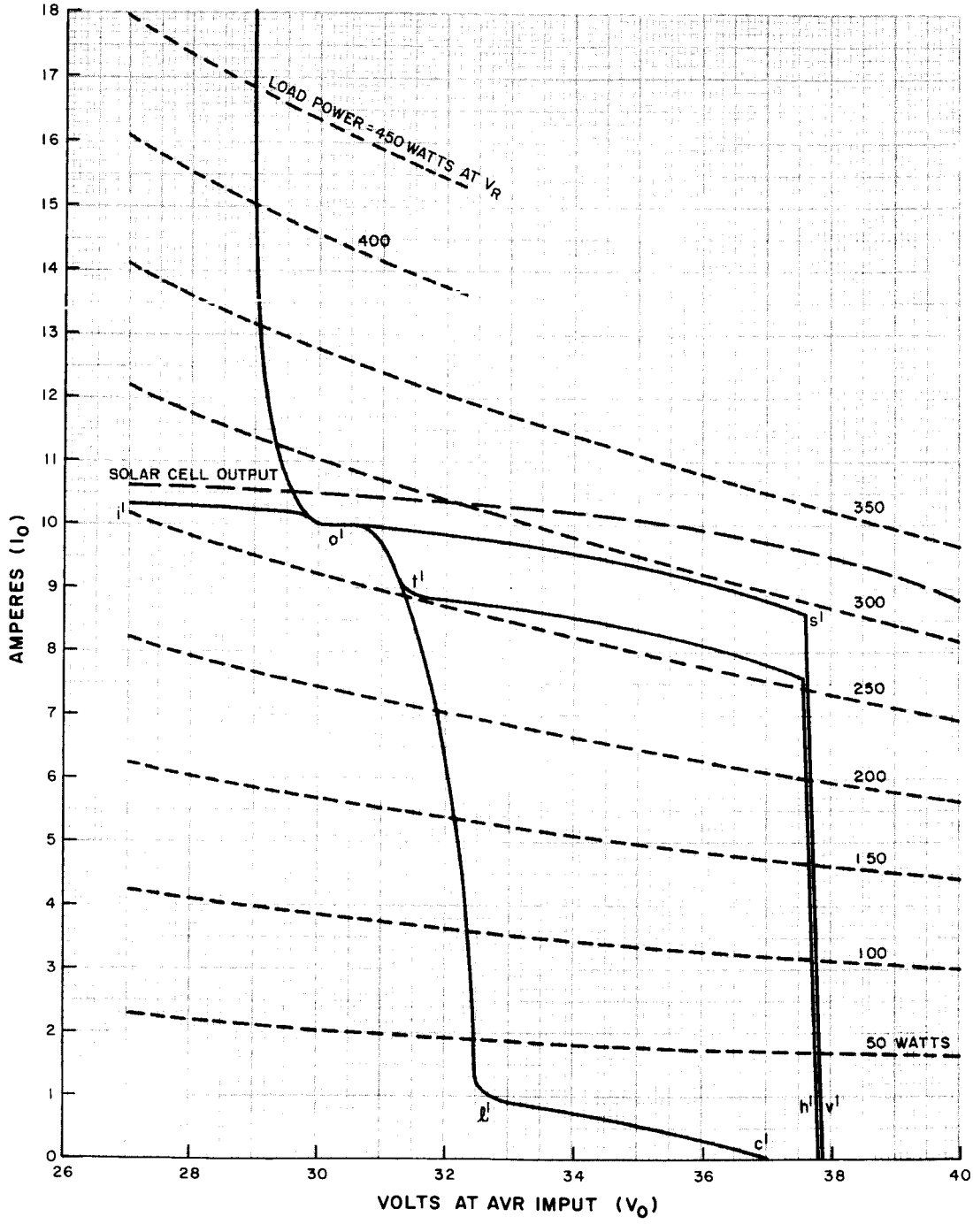


Figure 21. End-of-Life I-V Characteristics at AVR Input

a narrower range of 25 watts or so over which the so-called multiple operating points can occur. Location of the narrow range within the broad range is dependent on the time of life and state of charge of the eight batteries in the system.

In Nimbus-B, effects of this phenomenon are not serious, because:

(1) Chances of the occurrence of the multiple operating points at end of life are very small, at least under the conditions of the assumed component characteristics;

(2) The effect of an undersirable operating point is merely a moderate decrease in the recharge rate; and

(3) It appears that the effect cannot occur until at least some of the batteries (three or four) are in trickle charge.

Finally, it remains to be established whether all the multiple operating points indicated by a graphical analysis of the load lines are stable and practically possible.

Based on the specific operating conditions examined, there appear to be few, if any, possibilities of a lock-up of any significance. Chances of what has been referred-to as a minor lock-up appear to be influenced mostly by the slope of the charge controller characteristic when limiting, relative to the slope of the nearest fixed-load line. Most probable conditions for lock-up of this nature occur when the limiting portion of the charge controller characteristic is horizontal as assumed, and when operation is carried on along the constant-current part of the array curve. Under the latter conditions, the case of multiple intersections is more likely, as proven by the analysis of the beginning-of-life conditions compared to end-of-life.

It is not expected that any foreseeable departure from the assumed nominal characteristics of the individual system components will have any appreciable effect on the conclusions reached in this discussion.

4. Construction of I-V Characteristic Curves (Figures 20 and 21)

a. SOLAR ARRAY

The array output at cell level (array side of blocking diodes) is as shown in Figure 20. To reflect true conditions at AVR input (I_o, V_o), the following shifts are applied to the solar cell output curve:

(1) Voltage Shift - The entire curve shifted to the left by the amount of 1.8 + 0.35 = 2.15 volts.

(2) Current Shifts:

(a) First, the entire curve (shifted as above) is further shifted downward by the amount of the total shunt loss at V_s; thus, 22 ma x 8 modules = 0.176 amper.

(b) Second, part of the resultant curve (from the battery open-circuit voltage and to the right) is shifted by the amount of total loss at V_B, or by another 0.176 ampere.

The shifted array-output characteristic is further altered to reflect the shunt limiter. The nominal shunt-limiter characteristic shows the circuit turning on at 38 volts. The turn-on voltage, reflected to the AVR terminals, is reduced by the drop through the D2 diode path: i.e., 38 - 0.35 = 37.65 volts. At the AVR input terminals, then, the array output is limited at turn-on to that voltage, and is labeled "s" in Figure 20 where a curve may now be drawn through points i-o-s to show the reflected array output.

Point "s" in Figure 20 is located at I_o = 10.85 amperes, corresponding to 38.25 volts on the nominal shunt-limiter characteristic. At the AVR input, this becomes 38.25 - 0.35, or 37.9 volts shown as point "v" in Figure 20, where the reflected, effective array output is now completed as i-o-s-v.

b. BATTERY

(1) Reflected Battery Discharge Characteristics

Three items are significant. First, the battery discharge voltage is reduced at the AVR input by the amount of the voltage drop through the D1 path, i.e. by 0.45 volt; Secondly, there are 23 storage cells in series; and thirdly, when in discharge, there is a total shunt loss at V_B of 0.176 ampere, considering all eight modules.

The reflected battery discharge characteristics are listed in Table 6. The first two columns are the discharge voltage and current of a nominal, beginning-of-life Nimbus-B cell at +25°C and at 5% depth of discharge; the third column is the voltage at the AVR input; and the last column is the net total current through the discharge path D1.

TABLE 6. REFLECTED BATTERY DISCHARGE CHARACTERISTICS

Discharge Voltage V_{Bd} (volts per cell)	Discharge Current i_{Bd} (amperes)	AVR Input Voltage Voltage $V_o = 23V_{Bd} - 0.45$ (volts)	D1 Total Discharge Current $8i_{Bd} - 0.176$ (amperes)
1.36	0	30.85	-
1.33	0.15	30.15	1.02
1.31	0.4	29.7	3.02
1.30	0.61	29.45	4.70
1.297	0.7	29.35	5.42

Discharge characteristic o-d is generated in Figure 18 by graphically adding current values in the last column to i-o, at corresponding voltages.

(2) Reflected Battery Charge and Limiter Characteristics

The Reflected Battery Charge and Limiter Characteristics are listed in Table 7. The first two columns are the per-cell charge voltages and currents. The third column is the voltage drop from the charge limiter (CL) input to the battery terminals corresponding to charge current i_{Bc}, taken from the nominal charge-controller characteristic. The fourth column is the limiter input voltage reflected to the AVR input (i.e., the sum of the battery voltage and the limiter drop is reduced by the drop through D2). The last column is the total battery charge current.

TABLE 7. REFLECTED BATTERY CHARGE AND LIMITER CHARACTERISTICS

Charge Voltage VBC (volts per cell)	Charge Current i_{BC} (amperes)	CL Input to Batt. Term. $\Delta V_{lim.}$ (volts)	Limiter Input to AVR Input $V_o = 23V_{BC} + \Delta V_{lim} - 0.35$ (volts)	Total Charge Current $8\ i_{BC}$ (amperes)
1.36	0	0.7	31.65	0
1.38	0.16	0.85	32.3	1.28
1.40	0.35	0.96	32.55	2.8
1.42	0.54	1.04	33.4	4.32
1.44	0.77	1.13	33.9	6.16
1.456	1.10	1.25	34.4	8.8

Bottom row in the table represents the limiting condition.

The overall characteristic tabulated in the last two columns of Table 7 is constructed in Figure 20 by subtracting $8\ i_{Bc}$ from o-s at corresponding voltages, where-upon curve o-1 is drawn. Beyond point "1", the characteristic is arrived at by subtracting the limiting value of $8\ i_{Bc}$; i.e., 8.8 amps, from o-s-v. The entire power-system output characteristic during charge is thus o-1-c.

Similarly, o-t-h is drawn to show trickle charge condition; that is, one where the total charge is assumed to be limited to one ampere.

The entire power-system output characteristic as seen at the AVR input is d-o-1-c. The method of construction of the end-of-life characteristic d'-o'-1'-c' in Figure 21 is identical in every way to that outlined above.

c. CONSTRUCTION OF A FIXED LOAD LINE AT AVR INPUT

The AVR input current I_o equals:

$$I_o = \frac{P_L + P_{loss}}{e_c V_o},$$

where:

(1) P_L is the required fixed load power at $V_R = 24.5$ volts;

(2) P_{loss} is the loss at V_R, or, 25ma per module x 8 modules x 24.5 volts, or about 5 watts;

(3) e_c is the electronics module efficiency defined as the ratio of the output at V_R to the electronics module input as measured at AVR input terminals, with the battery modules disconnected; and

(4) V_o is the AVR input voltage.

Thus, if $P_L = 250$ watts as an example, $P_L + P_{loss} = 225$ watts, and . . .

V_o	e_c	I_o
36v	0.91	7.78 amps
31v	0.918	8.96 amps
26v	0.925	10.6 amps

Factor e_c is determined from data measured at room temperature, and is a function of the input voltage and the load current.

Tabulated values of V_o and I_o are plotted for this and other fixed loads in 50-watt steps.

E. POWER SYSTEM FUSE STUDY

The object of the Nimbus-B power system fuse study was to determine what fuses are suitable for use in the power supply subsystem. For small current applications (under 5 amperes) requiring "quick blow" occurrences, the Littelfuse Picofuse is available with a history of use on space programs. These fuses are hermetically sealed and have excellent shock and vibration characteristics. The impact shock resistance is 78 g for 11 milliseconds, and the fuse will withstand 20 g peak from 20 to 2000 Hg.

High-reliability Picofuses rated at 2, 3, 4, and 5 amperes were procured. These fuses were tested in air at 25°C primarily to determine how well the time-current points conform to the Littelfuse curves. From the limited number (15) of fuses tested, "bands" of tolerance were drawn around the Littelfuse curves (see Figure 22). Later, the manufacturer provided Littelfuse curves showing their bands of tolerance. These curves confirm our test results and, in general, show slightly wider bands. A second group of 45 fuses was tested to determine the feasibility of connecting fuses in parallel to increase the rating of the combination. These were the commercial equivalent of the Littelfuse Picofuse (not the high-reliability type) chosen because they are readily available. The fuse characteristics are almost identical between the two types and both have time-current curves which fall within the tolerance "band". Several parallel combinations were purposely mismatched on their cold resistance value to determine how a current inequality would affect the blow times. The test was run under thermal-vacuum conditions at temperatures of 25°C and 50°C to give additional information on effects of vacuum and temperature. Two different parallel combinations were tried: three 5-ampere Picofuses to make a 15-ampere rating, and two 5-ampere Picofuses to make a 10-ampere rating. To serve as control, single 5-ampere Picofuses were tested at the same time under the same conditions.

Results of this testing are shown in the time-current curves of Figures 23 and 24, and scope traces, Figures 25 and 26. On the time-current curves the test points were spread out to include times from 0.5 millisecond to 47 seconds. In cases of three in parallel, the three fuses are shown as a single point, at one-third the current required to blow the combination. This allows comparison to the manufacturer's curve. The two fuses in parallel are plotted in a similar way using one-half the current to blow. The significant result is that a smooth curve can be drawn through the test points showing that each 5-ampere fuse blew within the tolerance band regardless of the single, double, or triple combination (see Figure 23). Fuse No. 62 which fell outside the limits was a bad mismatch of resistance. (Also shown is a single maverick at 1 millisecond; it must be remembered that these two fuses are not the high-reliability fuses).

Reference to Figure 22 shows that actual test points taken at room temperature, in air, fall both above and below the manufacturer's curves. Reference to Figure 23 shows the new curve taken under vacuum conditions in a fixed amount lower than the air curve. This is consistent with other test results which show that it takes less current to blow

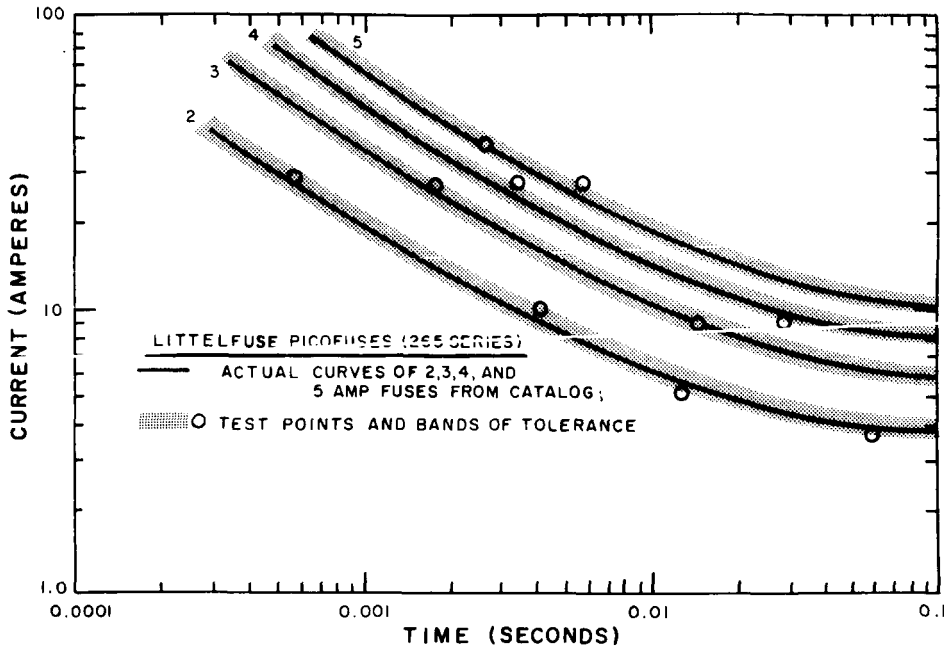


Figure 22. Picofuse Time Versus Current Curves

a fuse in a vacuum as the heat loss from the fuse is reduced. Thus, we have a measure of fuse derating necessary to use Picofuse types in a vacuum. Figure 24 is a further study of the triple combination. Here, the fuse "blow" occurrences are plotted at the actual current tested. Corrections are also made for temperature so that points shown are those of 15-ampere fuses at 25°C operating in a vacuum. The curve is that shown in the manufacturer's catalog for 5-ampere Picofuses, but the currents are tripled.

Oscilloscope tracings in Figures 25 and 26 show that the fuse-blow combination was virtually simultaneous in all cases. Figure 26 also shows a comparison between a single high-reliability type and a single commercial type Picofuse.

While it can be argued that in a mismatched combination, the "weakest" fuse blows first and then causes the remainder to blow quickly (resulting in all points falling below the manufacturer's curve), it also should be noted that the "control" single 5-ampere Picofuse also blew with its time-current curve below the manufacturer's curve. This is presented to show that the dashed line of Figure 24 is a true derating due to vacuum conditions. Judging from fuse No. 62 (Figure 24), it is recommended that the fuses in a parallel combination be matched as closely as practical.

Another possibility of the 10 and 15-ampere size fuses is the Bussman "Tron". This fuse has been tested at RCA and is currently in use on other programs. The construction is of glass with sealed metal ends. A drawback to the use of this fuse is the

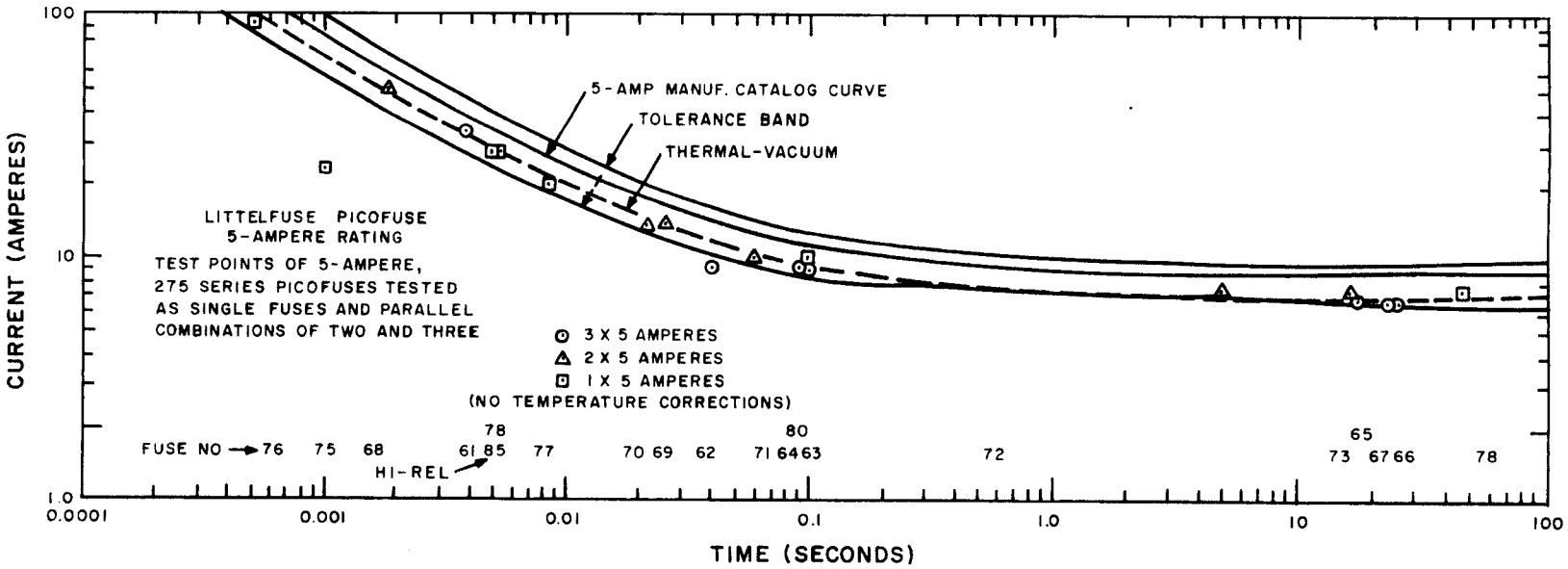


Figure 23. 5-Ampere Rating Picofuse Time Versus Current Curve

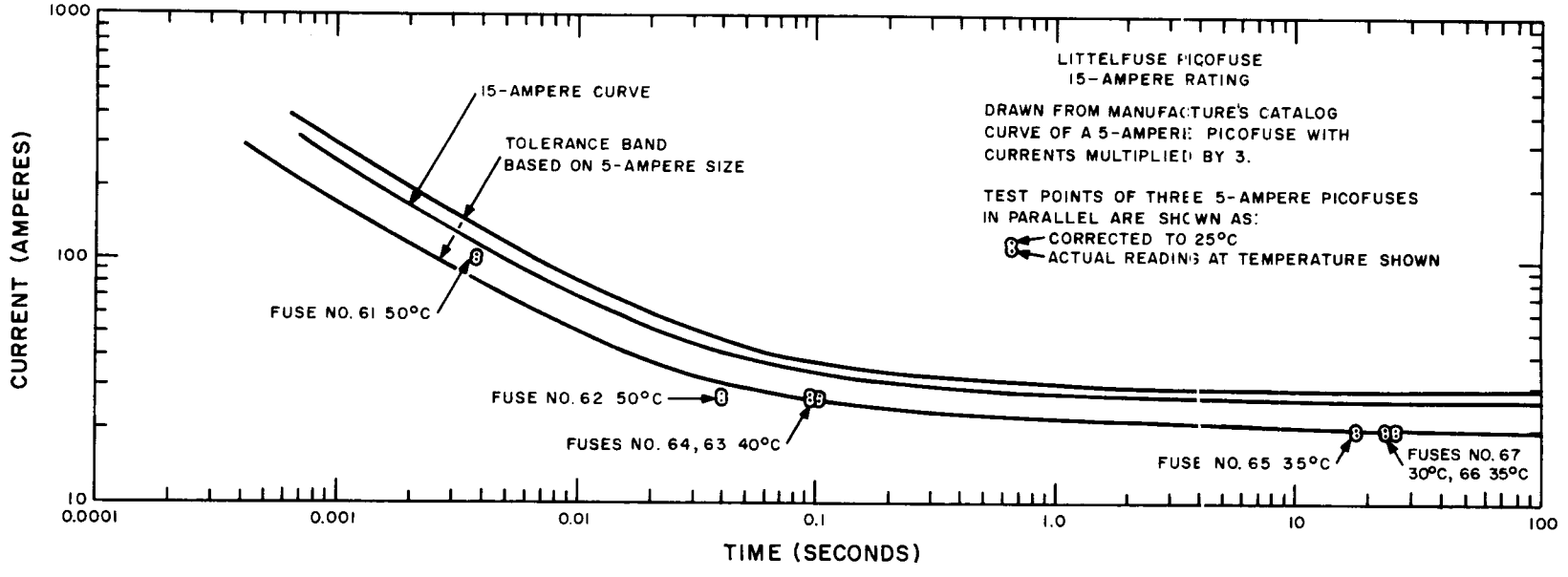
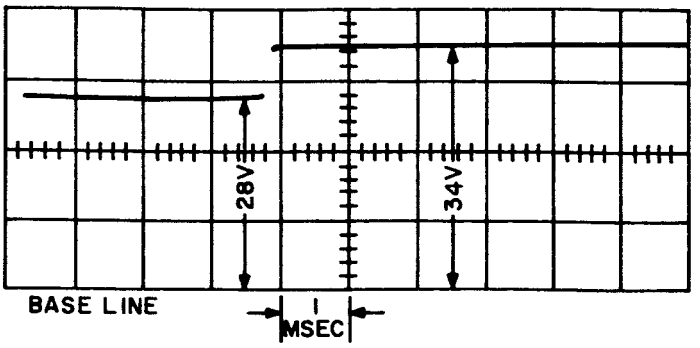
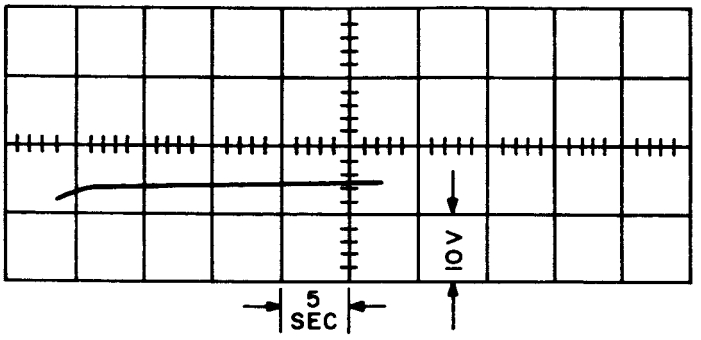


Figure 24. 15-Ampere Rating Picofuse Time Versus Current Curve



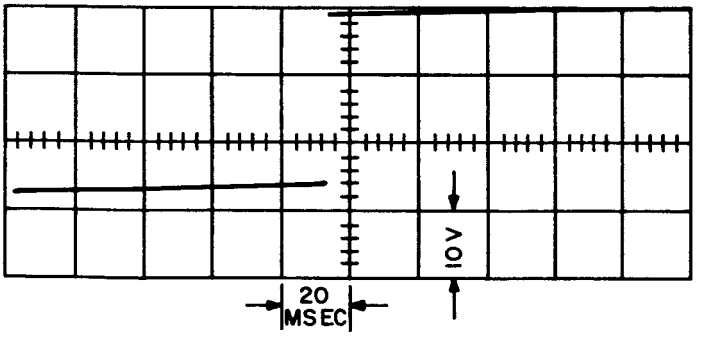
Fuse 61

3 x 5-Ampere Picofuse
100 Amps @ 3.8 msec



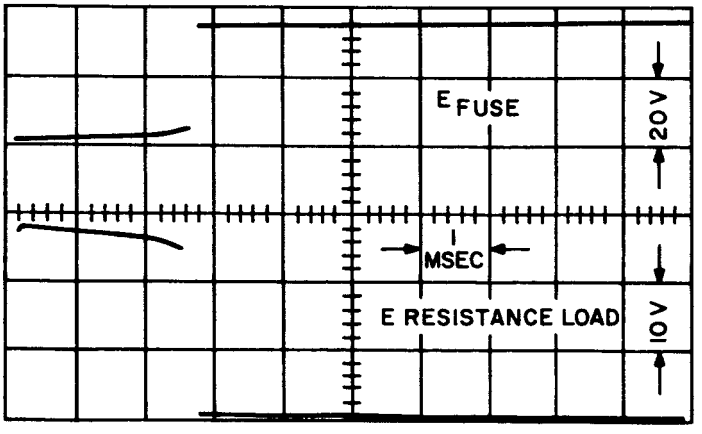
Fuse 67

3 x 5-Ampere Picofuse
20 Amps @ 24 seconds



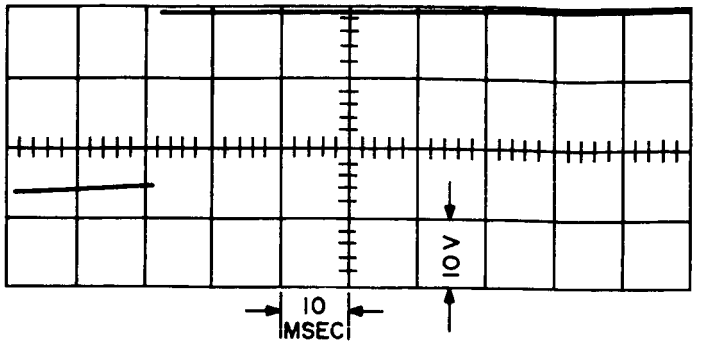
Fuse 64

3 x 5-Ampere Picoruse
27 Amps @ 97 msec



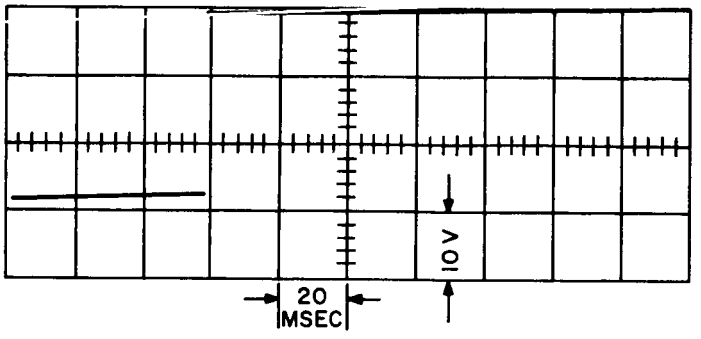
Three 5-Ampere Hi-Rel Picofuses
in Parallel
25°C in Air

Figure 25. Oscilloscope Tracings of Three 5-Ampere Picofuses in Parallel, 15-Ampere Rating



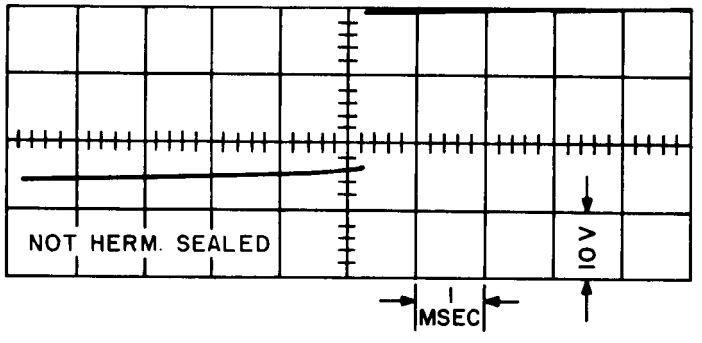
Fuse 70

2 x 5-Ampere Picofuse
27 Amps @ 21 msec



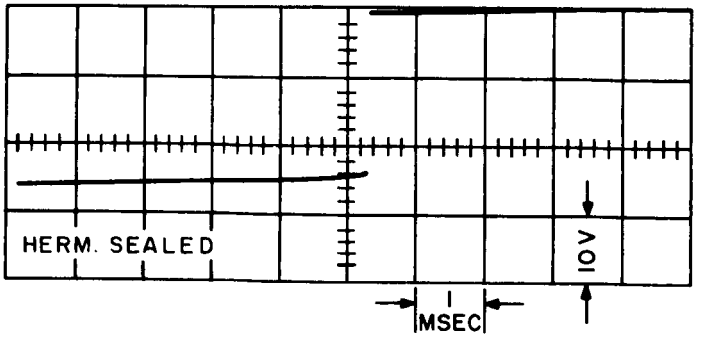
Fuse 71

2 x 5-Ampere Picofuses
20 Amps @ 59 msec



Fuse 78

5-Ampere Commercial Picofuse (275)
Cold Resistance = 0.015 ohm
27 Amps @ 5.2 msec



Fuse 85

5-Ampere High-Reliability Picofuse (265)
Cold Resistance = 0.015 ohm
27 Amps @ 5.3 msec

Figure 26. Oscilloscope Tracings of Two 5-Ampere Picofuses in Parallel (10-Ampere Rating), and Comparison of High-Reliability and Commercial 5-Ampere Fuses

relatively low-vibration resistance (1.3 to 14.5 g at 20-2000 Hz). This may require special mounting for vibration isolation. An order was placed for these fuses so they could be tested with the Picofuses, but the shipment arrived too late for tests to be covered by this report.

As a back-up program to the commercially available fuses, Pyrofuze wire was tested in an attempt to create a fuse suitable for Nimbus use. Pyrofuze has been used successfully on spacecraft but it has several drawbacks. On blowing, the vaporized metal sprays over adjacent components; the time-current characteristics put into a "slow" or "medium"-blow category; and the 2 to 4-inch length of wire needed makes it relatively large. As a possibility for use in the 10 and 15-ampere size, and on the assumption that a slower-blow characteristic may be needed in future applications, Pyrofuze was tested as follows:

(1) Various lengths of wire were tried, and 1/2-inch length seems practical; less than 1/4-inch length is useless. However, each length up to 2 inches requires a separate time-current curve.

(2) To contain the "flash" of vaporized fuse metal, various attempts were made to encapsulate the fuse wire. The thermal conductivity of the surrounding material has a great affect on blow time. A rigid epoxy would rupture from a blown fuse. Urethane filler or foam supplies a useful thermal conductivity but lack the strength to contain the "blown" fuse particles. The fuse particles were successfully contained in sizes below 0.010-inch wire diameter by sleeving with a loose teflon tube and covering with heat-shrink tubing. This allowed an expansion chamber which contained the particles in air as well as vacuum. Sizes up to 0.020-inch were contained in a 1/4-inch diameter glass epoxy tube. Each construction, however, would have its own time-current characteristic. To eliminate any joints within the encapsulated fuse, the fuse wire was brought out and the external lead portion covered with wire braid. The fuse ignition would not continue past the braid. Some examples of encapsulation are shown in Figure 27.

In general, these attempts were not successful. To mount Pyrofuze requires that the wire be held down only through a teflon sleeve, and that the container be so designed that the vaporized fuse metal does not deposit on adjacent circuitry, an adjacent fuse, or leave the container itself. One advantage Pyrofuze provides is the slower blow time. As an example, the amplitude of a 100-msec pulse can be 3.5 times the steady current required to blow the fuse.

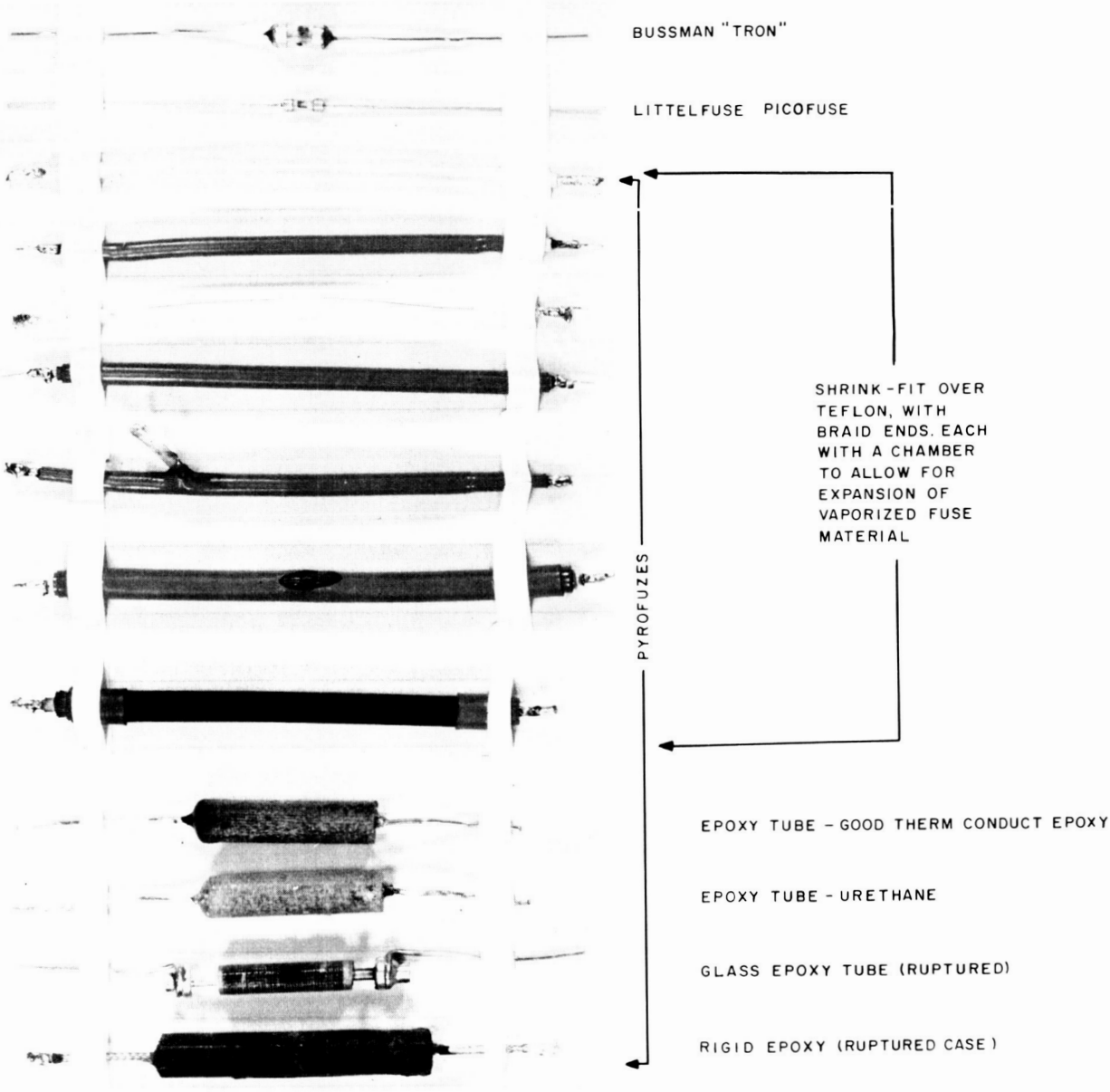


Figure 27. Samples of Encapsulated Fuses

F. FUSE-REGULATOR INTERFACE PROBLEM

In the Nimbus-B spacecraft, the non-essential loads are fused to protect the power supply from faults in these loads. If this protection is to be effective, the power system must be capable of blowing any fuse without any damage occurring within the power system.

An analysis was performed to determine what regulator-fuse interface problems exist and what corrective measures might be indicated. The results of this analysis are discussed below.

The minus 24.5-volt load-bus regulator, as developed under Contract NASA 5-3248, does not have a short-circuit protective feature and is capable of delivering a maximum load current of 20 amperes at 24.5 volts. If a subsystem with a nominal 7.5-ampere current demand is fused with a 15-ampere fuse (which assumes a 2-to-1 safety derating), will the regulator deliver the necessary fuse blowing energy without incurring a catastrophic failure? To answer the question adequately, a detailed investigation of the regulator transient short-circuit behavior and the clearing characteristics of the selected fuses was required. A secondary objective was to determine the regulator or combination regulator-system changes required if the regulator short-circuit capability was exceeded.

1. Fuse Characteristics

Fuses tentatively selected for use in the Nimbus-B power supply are Picofuses, manufactured by the Littelfuse Corporation. These fuses are presently available in ratings from 0.125 to 5 amperes. To facilitate regulator-fuse transient calculations, data on a 5-ampere fuse was extrapolated to a 15-ampere level. Curves relating fuse overload current to blow time for the 5-ampere fuses are shown in Figure 28.

2. Regulator Short-Circuit Transient Characteristics

As indicated in Figure 28, the time required for a 15-ampere fuse to clear after a load fault occurs is highly dependent on the total available source current. With a source composed of a PWM* switching regulator in series with a battery, careful consideration must be given to the ability of the main-power switching elements to sustain severe overloads.

A transient analysis of the regulator with a shorted load was conducted, using the simple equivalent circuit shown in Figure 29. Within microseconds after the short

*Pulse width modulator

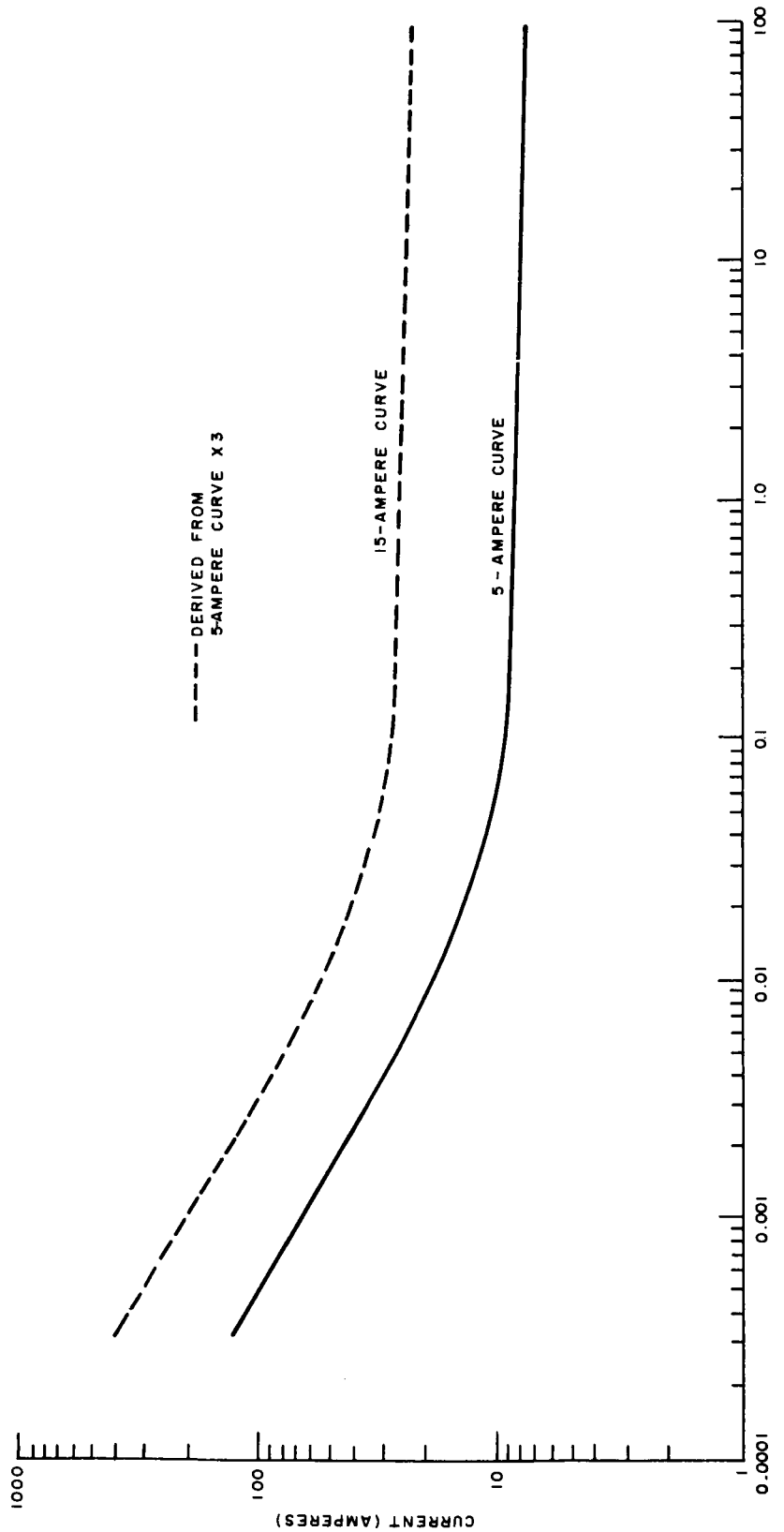


Figure 28. Current Versus Time-to-Blow Graph of 15-Ampere Picofuse

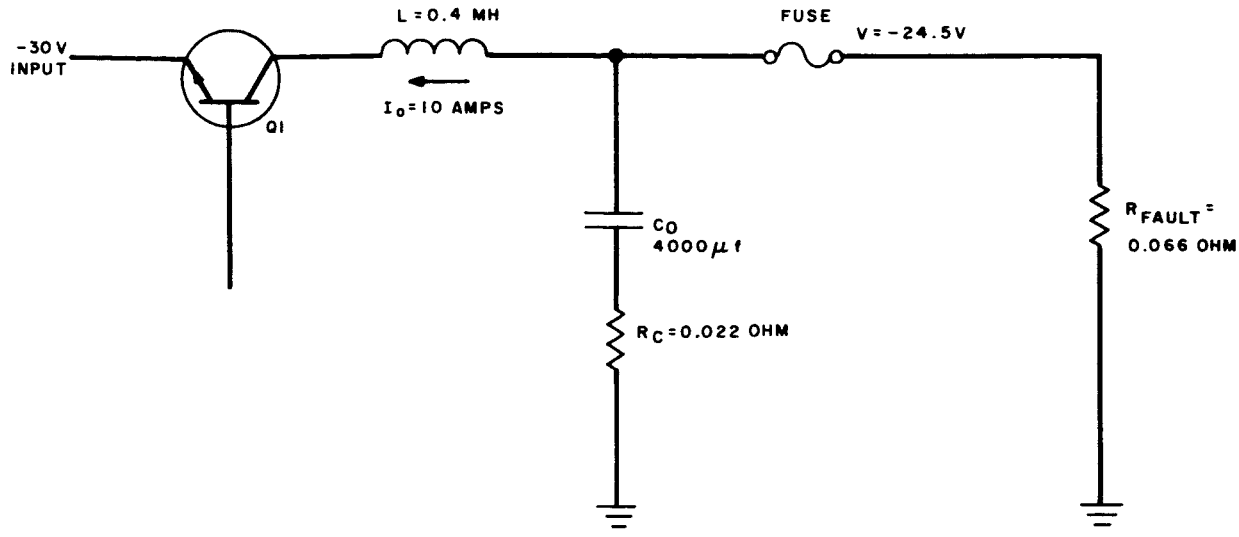


Figure 29. Regulator Equivalent Circuit

occurs, the regulator power switches (represented schematically by Q1) close and apply battery voltage to the choke L1. Calculations were based on an initial load current of 10 amperes, an output voltage of -24.5V, and the capacitor and fault resistances as indicated. Results of the analysis are shown in Figure 30. At the instant the load fault occurs, fuse current immediately climbs to roughly 300 amperes and begins an exponential decay as capacitor C_O (see Figure 29) discharges. The capacitor discharge continues to a level of approximately 50 amperes, at which time the inductor current reaches a critical saturation level of about 30 amperes. The inductor L1 saturates and allows the current to rise rapidly to a new level of typically 100 amperes. The final level is dictated by the base-drive-current gain restrictions associated with the transistor power switches. The 100-ampere level is maintained until the fuse blows, or until the transistors are destroyed by the large power overload.

3. Preliminary Conclusions

Results of the investigation as indicated in Figure 30 show that: (1) a 5-ampere Picofuse will clear without regulator damage, (2) regulator survival is highly marginal for a 10-ampere fuse, and (3) catastrophic failure is certain for fuse ratings in excess of 10 amperes.

4. Approach for Resolving the Problem

Four approaches to the problem have been considered and are discussed below:

(1) Increase the capacity of the output capacitor. An analysis of the fuse-capacitor-regulator relationship showed that approximately 60,000

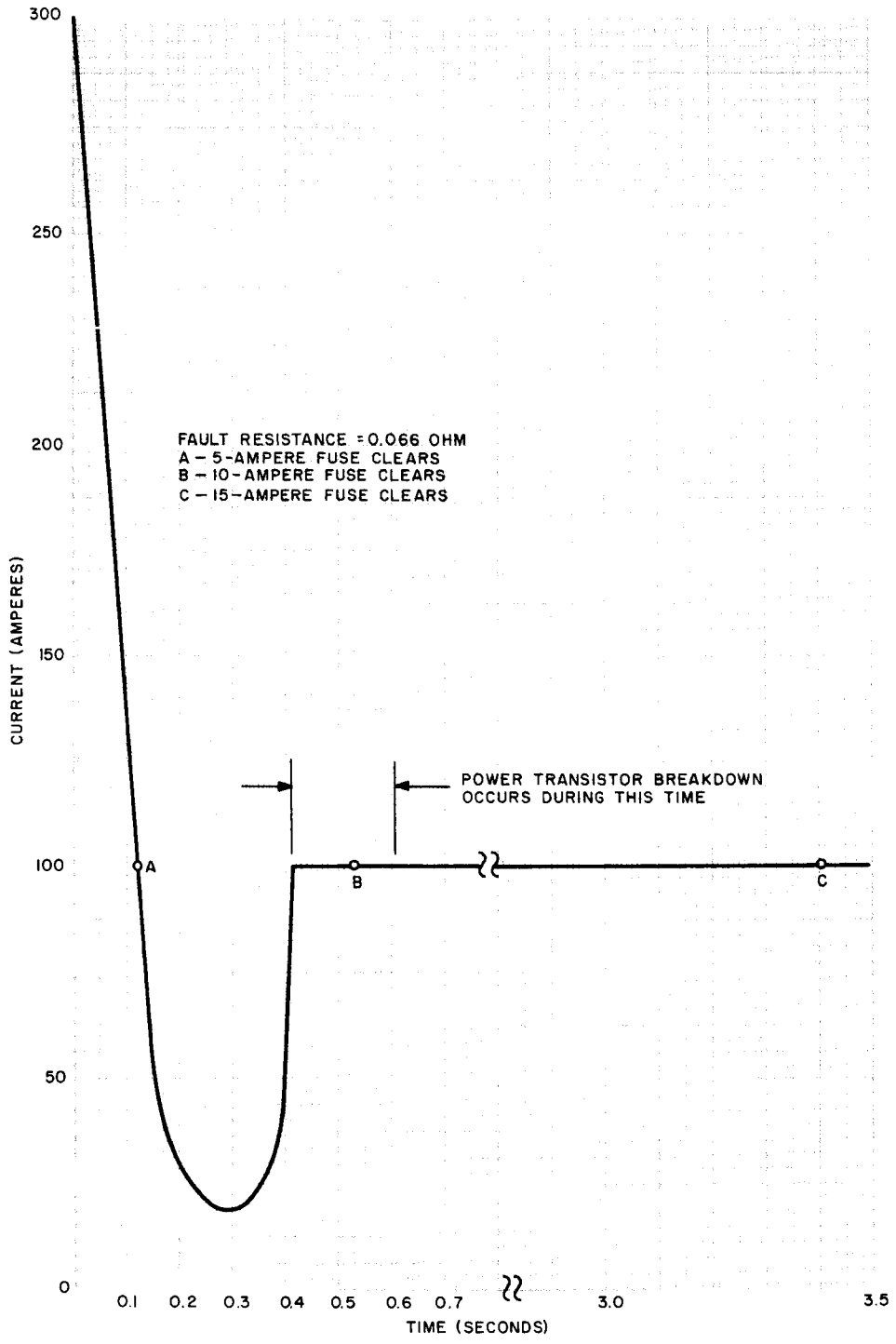


Figure 30. Fuse Currents (5, 10, and 15-Ampere) Versus Time for Regulator Short-Circuit Condition

microfarads would be required. This is fifteen times as large as the presently used capacitor, and would cause a serious turn-on problem as well as space and weight problems.

(2) Protect the regulator by limiting its maximum current. With the current limited to a safe level of 20 to 25 amperes, the regulator would be marginal for clearing a 15-ampere fuse (see Figure 28).

(3) Provide a battery-tap line to supply fuse-blowing current. A battery tap will not protect the regulator because the regulator-output voltage must drop below the battery-tap voltage before the battery tap can supply power; the regulator power-switching transistors will break down before the regulator-output voltage can be pulled down.

(4) Employ a combination of approaches (2) and (3) above.

An analysis of approaches (2) and (3) above showed that neither of these approaches would be adequate, and therefore, approach (4), a combination of (2) and (3), was selected. A functional block diagram of this concept is shown in Figure 31. The battery-tap diodes isolate the batteries from the minus 24.5-volt bus until the bus voltage falls below the battery-tap voltage. At this time, the regulated bus is clamped to the battery-tap voltage, and the batteries supply the current required to clear the fuse. The regulator will sense its output current, and will override the voltage feedback loop in a manner which will limit current to a safe level.

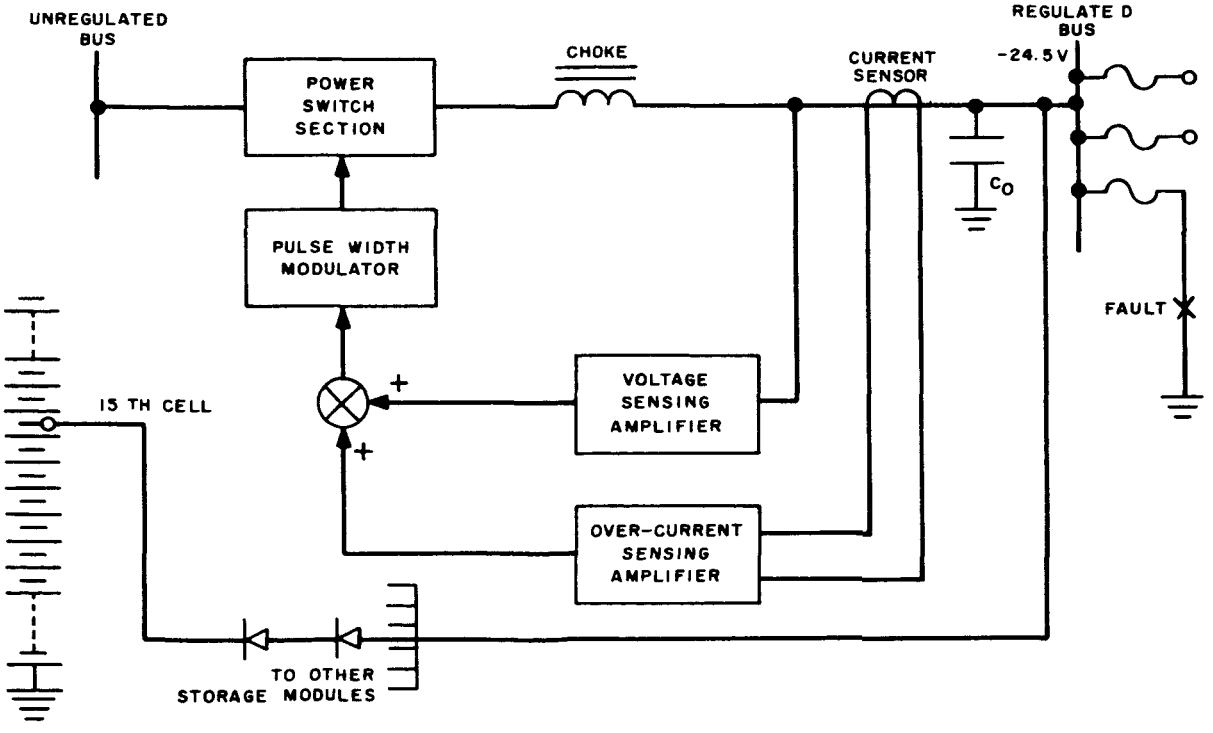


Figure 31. Current Limiting and Battery Tap System, Functional Block Diagram

a. BATTERY SURGE CAPABILITY

Surge capability of a Nimbus type battery was measured. It was determined that for room-temperature operation, a cell voltage of 1.0 volt at 30 amperes for a short duration (about 1 to 5 milliseconds) may be expected. This includes effects of intercell connectors and solder joints.

Calculation of currents required to clear the largest anticipated fuse with minimum fault resistance indicates a current requirement of approximately 28 amperes per battery (seven batteries) for 1.1 milliseconds.

b. BATTERY-TAP DIODES

Several diodes are being considered for this purpose. Thus far, only one type has been evaluated. A Westinghouse 379D, 12-ampere, silicon diode successfully passed 100 amperes for 800 milliseconds without apparent detrimental effects. The diode shorted at 100 amperes and 1 second. Further tests will commence upon receipt of ordered material.

c. CURRENT LIMITING

Several constraints have been determined for the current-limiting function:

(1) The maximum current must be limited to 20 to 25 amperes in order to eliminate the possibility of regulator damage.

(2) Limiting action must take place within two cycles of regulator operation (about 200 μ sec) in order to eliminate excessive current overshoot.

(3) The minimum, obtainable output voltage is constrained by power-switch duty cycle considerations. In other words, a low output voltage would require a low-power-switch duty cycle which is essentially unobtainable with the existing design due to storage-time phenomena. However, the battery-tap concept serves to limit the minimum output voltage; hence, it also limits the minimum duty-cycle requirement. Several design approaches are being considered and preliminary designs are in progress.

No test data will be presented for the regulators at this time, in view of the impending changes to the circuitry.

d. BATTERY AND ARRAY ISOLATION

Battery and array isolation is generally accomplished with germanium transistors connected as diodes. It has been found, however, that this connection, while having desirable forward-voltage characteristics, has extremely undesirable and unstable reverse-leakage characteristics. A search was undertaken to determine whether there was a device capable of the performance desired for Nimbus-B.

It was found that any germanium transistor connected as a diode would have similar characteristics in that the forward voltage would be low and the reverse leakage high. Only one germanium diode was found which was considered applicable. It was decided to compare this diode with performance of collector-base-junctions of several high-current germanium transistors. These tests are currently in progress.

G. POWER SUBSYSTEM TELEMETRY

1. Battery Voltage Telemetry

This circuitry (see Figure 32) provides for direct sensing of the battery voltage, and also provides an isolated signal-output return which may be connected to the encoder signal ground at any point without interference due to power-ground currents.

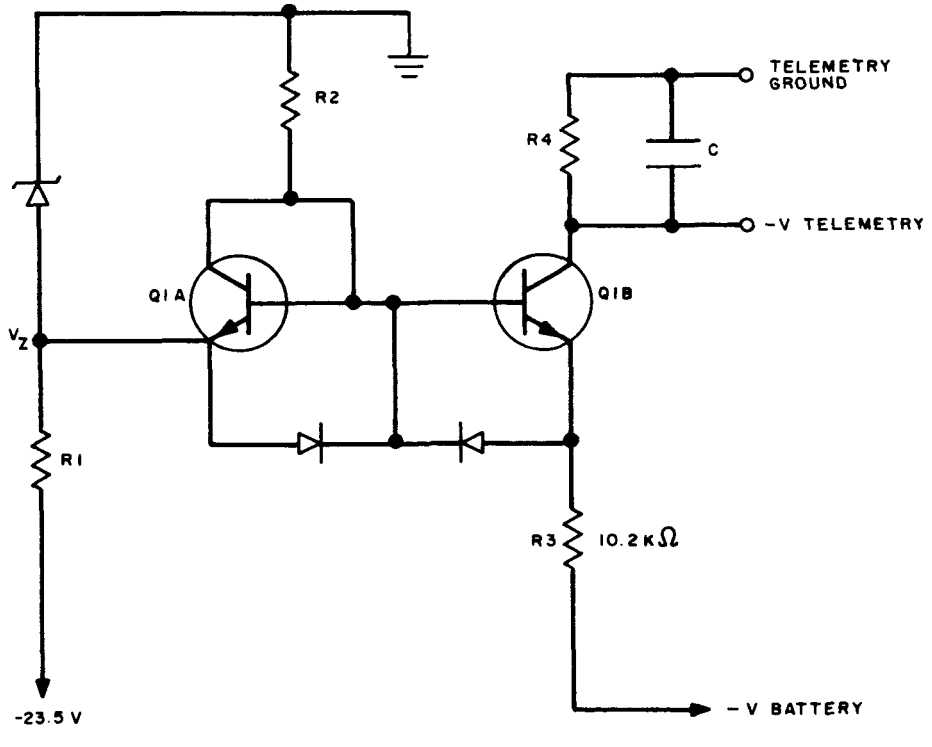


Figure 32. Battery Voltage Telemetry Circuit Diagram

The circuit was designed so that the battery voltage range of 20 to 40 volts could be telemetered at 0 to 6 volts (nominal). There is no output across resistor R4 until the voltage to be telemetered exceeds the reference voltage of the base. The voltage across R3 establishes an emitter current in transistor Q1B which for large values of current gain equals the collector current. Since the collector current is essentially independent of collector voltage, the output appearing across R4 will be independent of voltages between the power ground and the encoder telemetry ground. The capacitor across R4 reduces any high-frequency noise which might appear in the output. Transistor Q1A is connected in such a manner as to cancel temperature variations in V_{BE} of Q1B.

2. Regulated and Unregulated-Bus Voltage Telemetry

The circuit diagrams for the regulated-bus voltage telemetry and the unregulated-bus voltage telemetry are essentially the same as for Figure 32, except that the 10.2K resistor becomes 5.23K for the regulated-bus telemetry and 12.7K for the unregulated-bus telemetry.

3. Battery Temperature Telemetry

The circuit diagram for the battery temperature telemetry is shown in Figure 33.

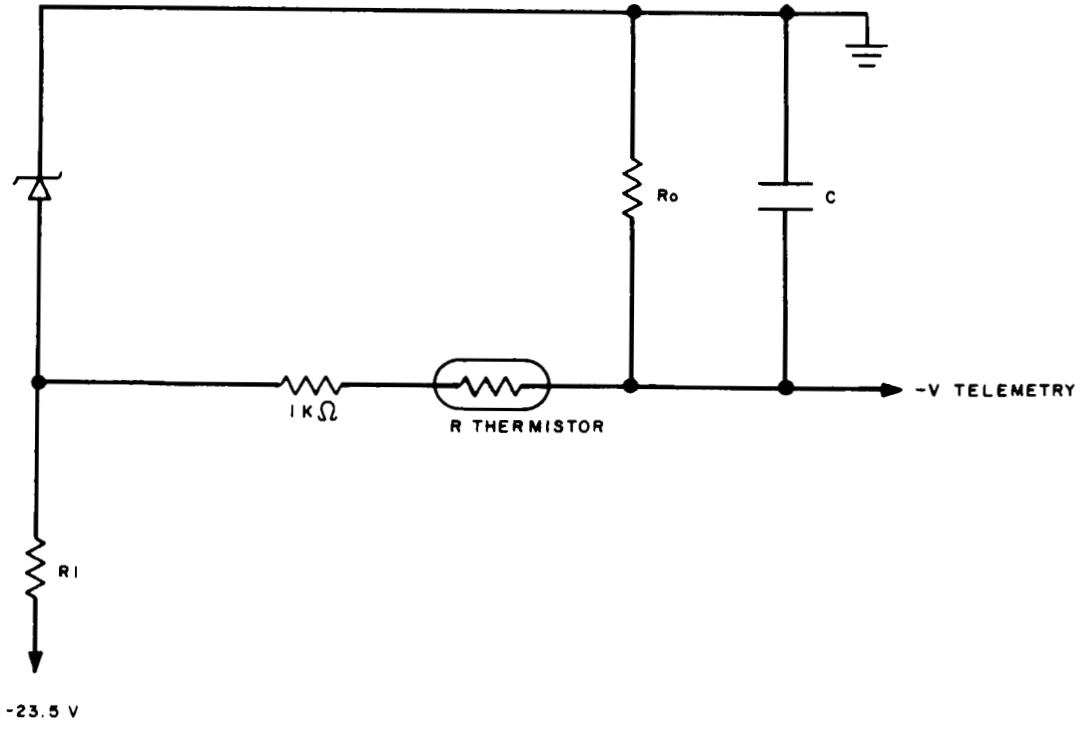


Figure 33. Battery Temperature Telemetry Circuit Diagram

The thermistor, which is located on one of the batteries, senses the battery temperature. Any change in temperature causes a change in the thermistor resistance, and, in turn, a change in the current flowing through the output resistor. A temperature-compensated zener diode is used so that a constant voltage is kept across the combination of the two resistors and the thermistor. The 1K resistor is used to keep the output voltage below 7.35 volts in case of a thermistor short.

4. Auxiliary Regulator Voltage Telemetry

To telemeter the auxiliary regulator voltage (0 to 25V), a simple two-resistor voltage divider is used (see Figure 34). This will provide a linear 0 to 6.4-volt telemetry signal. The 0.33 uf capacitor reduces any high-frequency noise which might appear in the output.

5. Regulated-Bus and Solar-Array Current Telemetry

The regulated-bus and solar-array current telemetry circuit diagram is shown in Figure 35. The current-to-voltage transducer consists of a series-connected saturable reactor (L), connected in series with a full-wave bridge (CR1, CR2, CR3, and CR4). The full-wave bridge is terminated with an accurate, wire-wound resistor (R2) and a low-pass filter (R1, R3, and C1).

The series-connected, saturable reactor is made up of two identical toroidal reactors stacked one on top the other, and electrically connected in series opposition with respect to a common control winding (N_C). When the control-current impedance is high enough, the reactor acts as a current inverter, whereby the d-c control current

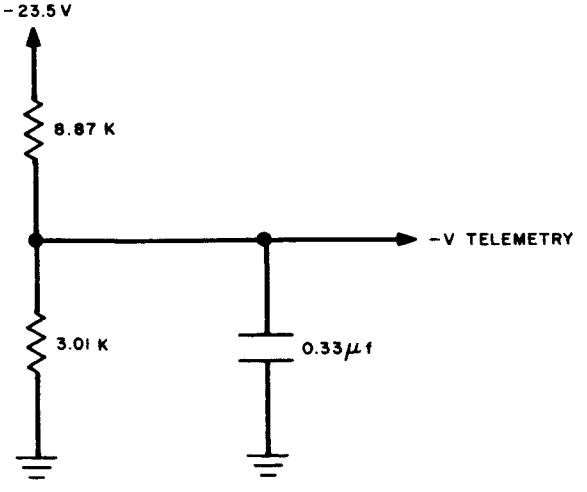


Figure 34. Auxiliary Regulator Voltage Telemetry

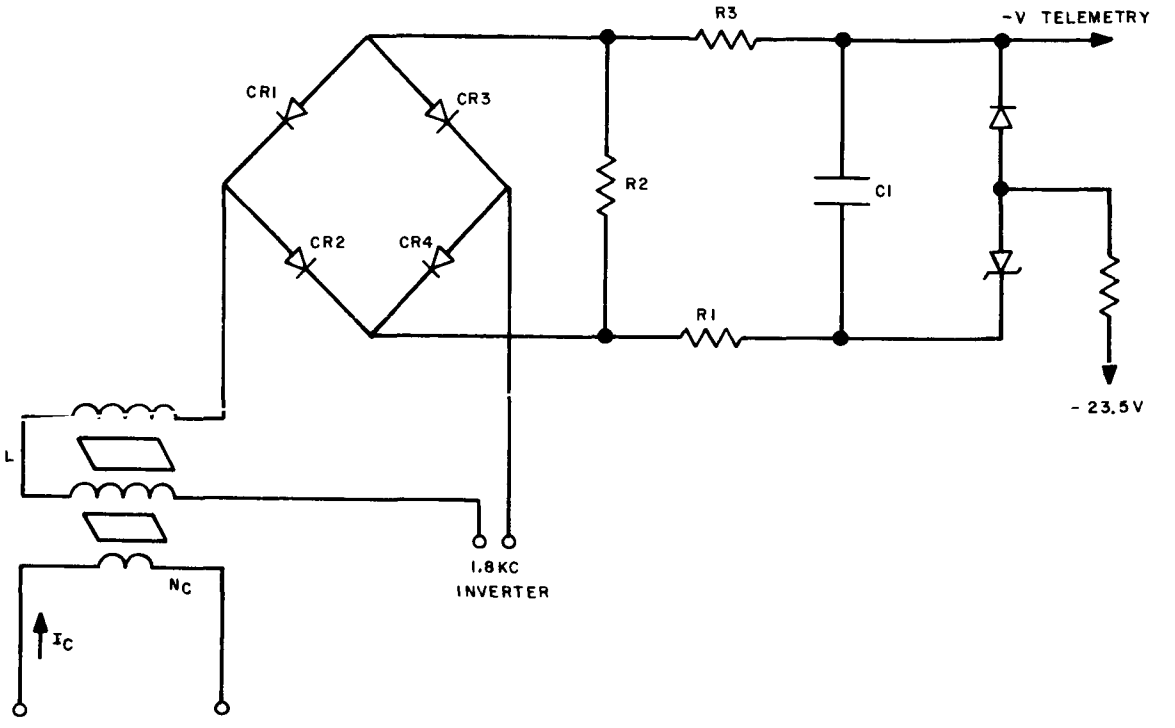


Figure 35. Regulated-Bus and Solar-Array Current Telemetry Circuit Diagram

(I_C) is converted to a square-wave current. This current is rectified by the full-wave bridge and develops a d-c voltage (plus ripple) across R2. This d-c voltage, in addition to a small amount of ripple, appears across C1. The current-telemetry transducers are excited by a 1.8 kc inverter. The two diodes across the output capacitor limit the output voltage to a maximum of approximately 6.8 volts.

The bus current (0 to 20 amperes) is telemetered at 0.06 to 6 volts (nominal) with a full-scale, worst-case, calibrated, accuracy of 2 percent, and a zero-based linearity of 2 percent.

6. Summary of Telemetry Measurements and Typical Telemetry Calibration Curves

Table 8 lists the input-output measurements, linearity, and worst-case, full-scale accuracy for the various power subsystem telemetry circuits. Figure 36 through 43 are typical calibration curves of the various battery module and electronics module telemetry circuits.

TABLE 8. POWER SUBSYSTEM TELEMETRY MEASUREMENTS

Telemetry Circuits	Input Range (Nominal)	Output Range (Nominal)	Linearity	Calibrated Worst-Case Full-Scale Accuracy
Battery Module T/M				
Battery Voltage	20 - 40 v	0 - 6 v	1% Terminal Based	1%
Battery Temperature	-10 to +70°C	0.9 - 5.75 v	3% Independent	±2°C
Battery Charge Current	0 - 1.2 amps	0.5 - 6 v	1% Terminal Based	2%
Battery Discharge Current	0 - 2.4 amps	0.5 - 6 v	1% Terminal Based	2%
Electronics Module T/M				
Reg Bus Voltage	20 - 30 v	0 - 6 v	1% Terminal Based	1%
Unreg Bus Voltage	20 - 45 v	0 - 6 v	1% Terminal Based	1%
Aux Reg Voltage	0 - 25 v	0 - 6.4 v	0.25% Terminal Based	1%
Reg Bus Current	0 - 20 amps	0.06 - 6 v	2% Zero Based	2%
Solar-Array Current				
Shunt Dissip. Current			1% Terminal Based	
Regulator Operate	This is a digital device which defines the regulator as being either on or off. The two levels are 0 volts for on, and 7.5 volts for off.			

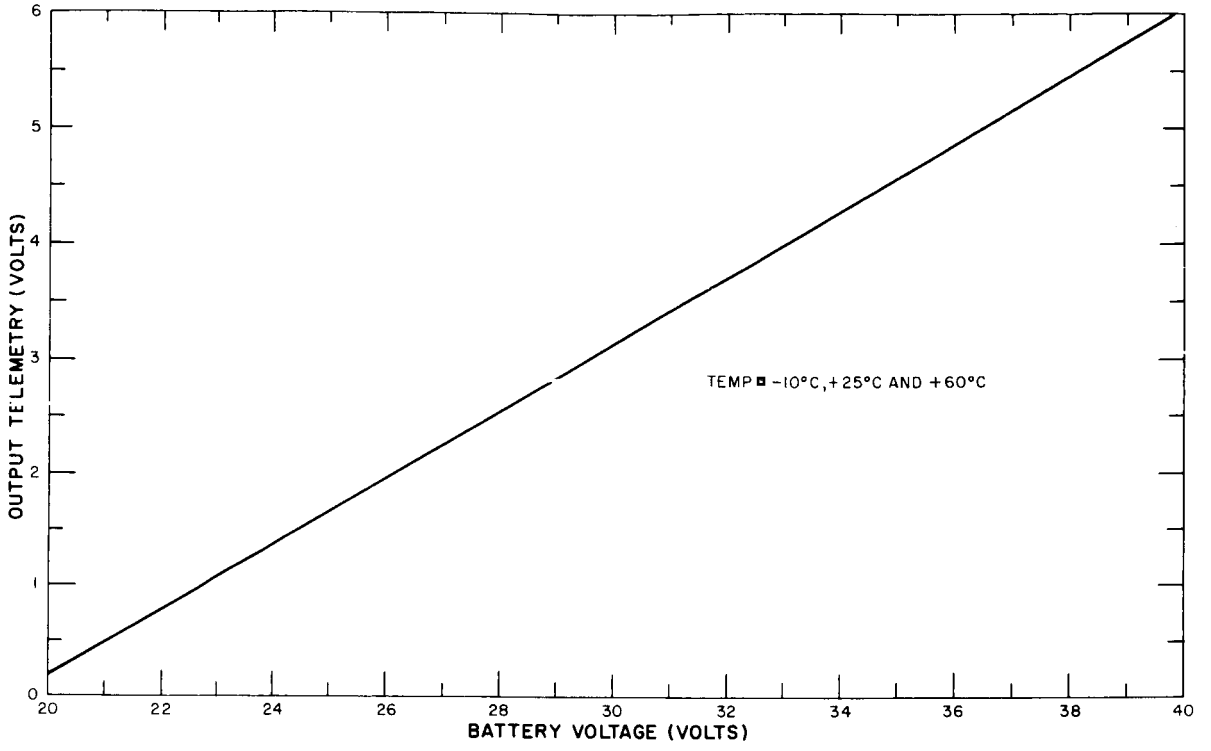


Figure 36. Typical Battery Voltage Telemetry Calibration Curve

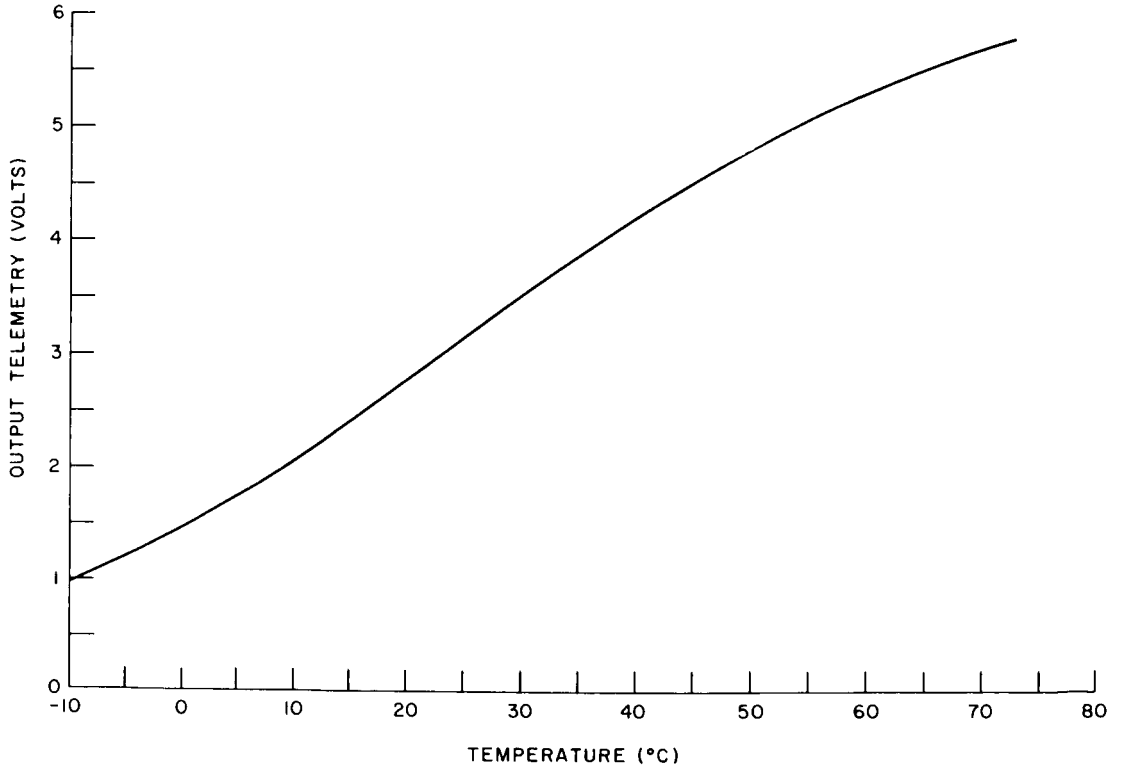


Figure 37. Typical Temperature Telemetry Calibration Curve

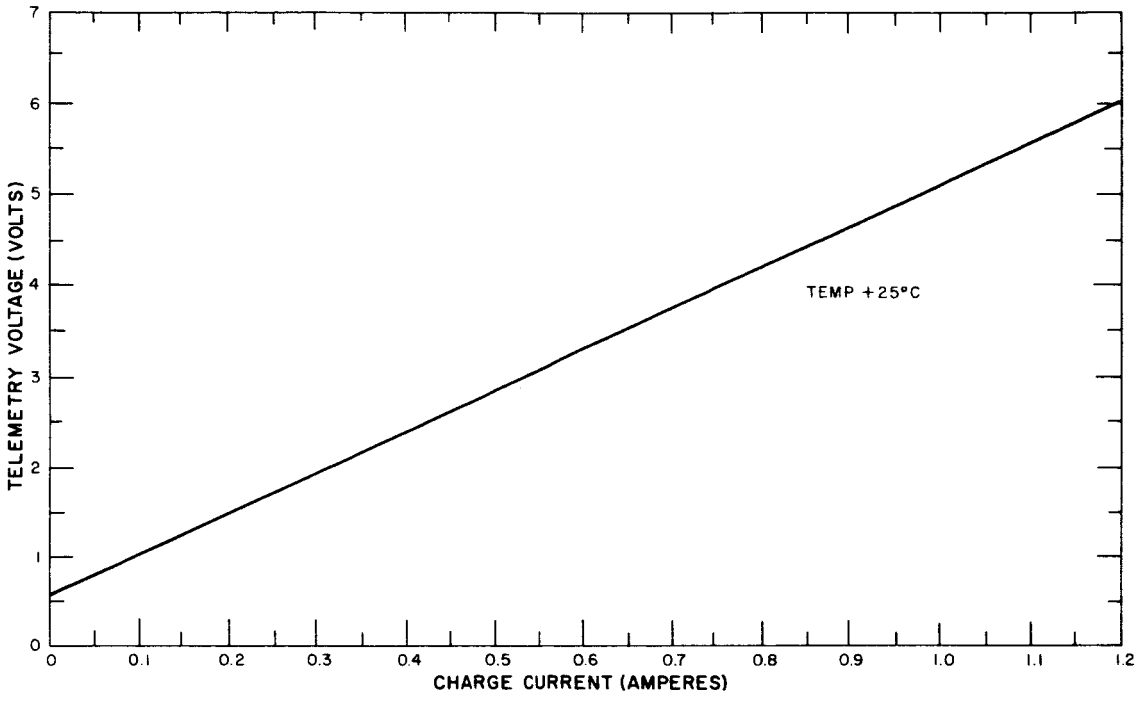


Figure 38. Typical Charge Current Telemetry Calibration Curve

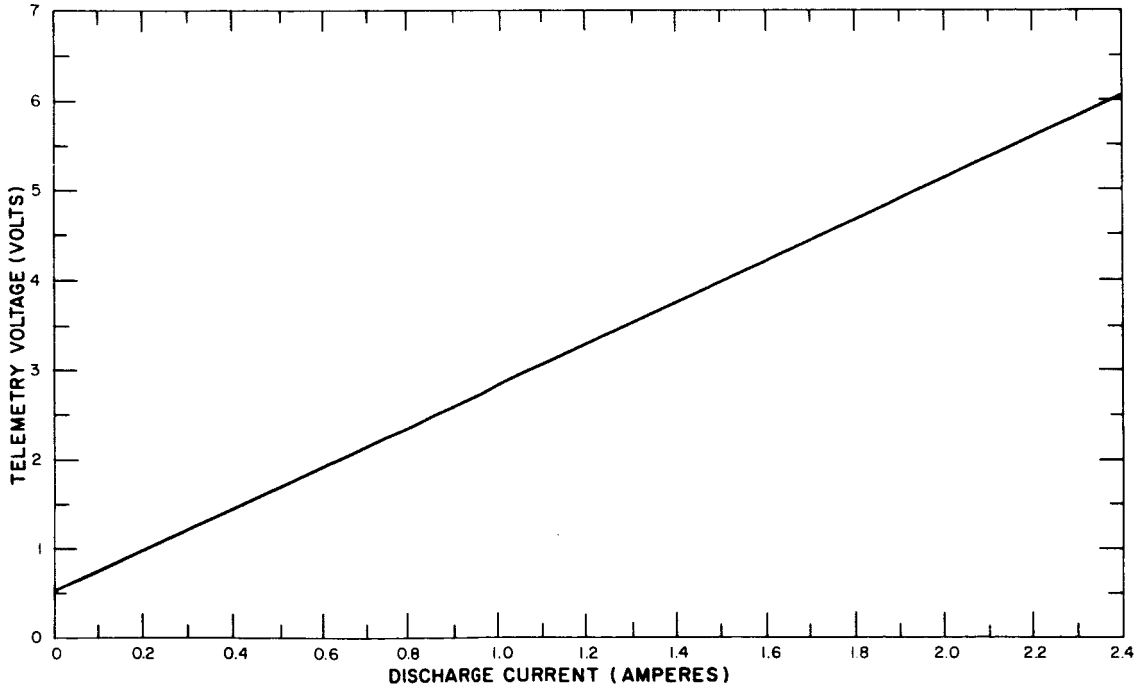


Figure 39. Typical Discharge Current Telemetry Calibration Curve

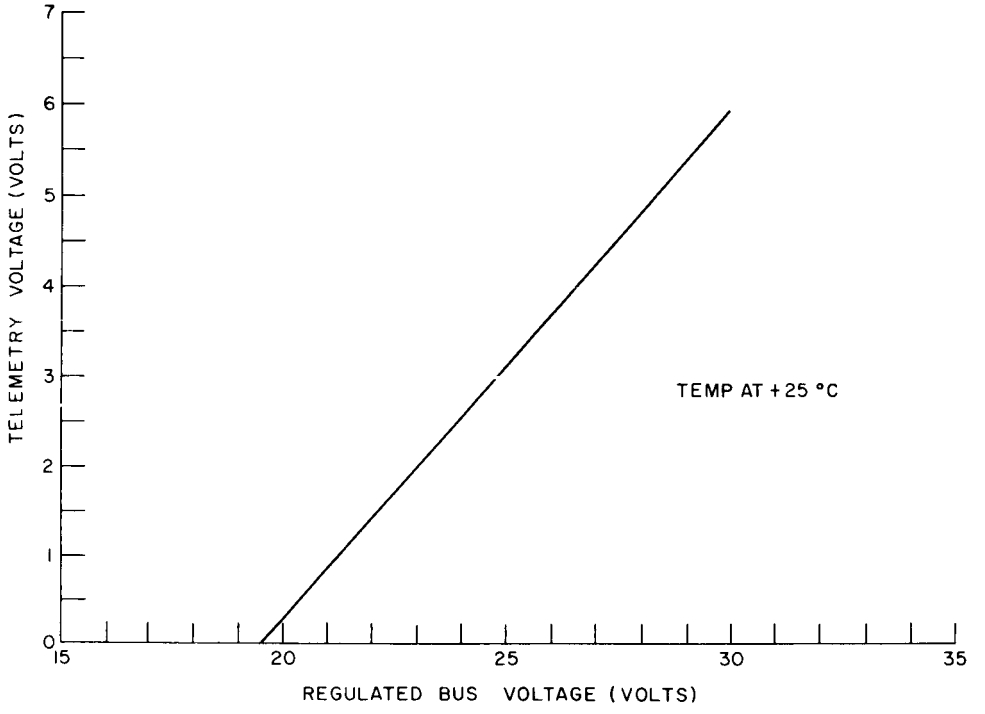


Figure 40. Typical Regulated-Bus Voltage Telemetry Calibration Curve

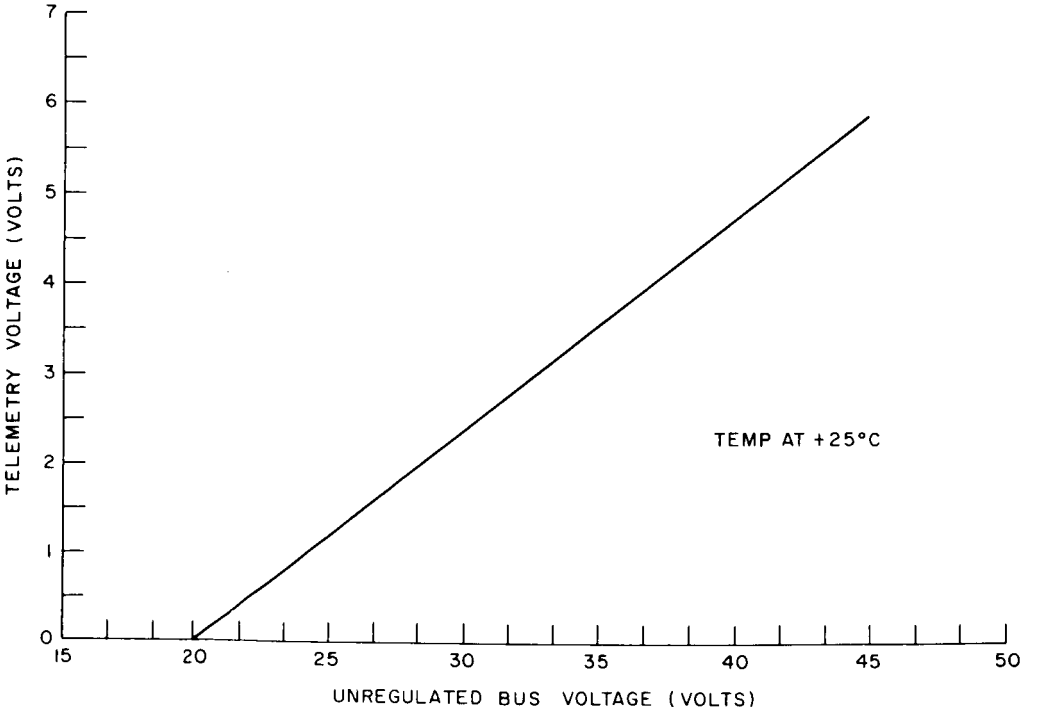


Figure 41. Typical Unregulated-Bus Voltage Telemetry Calibration Curve

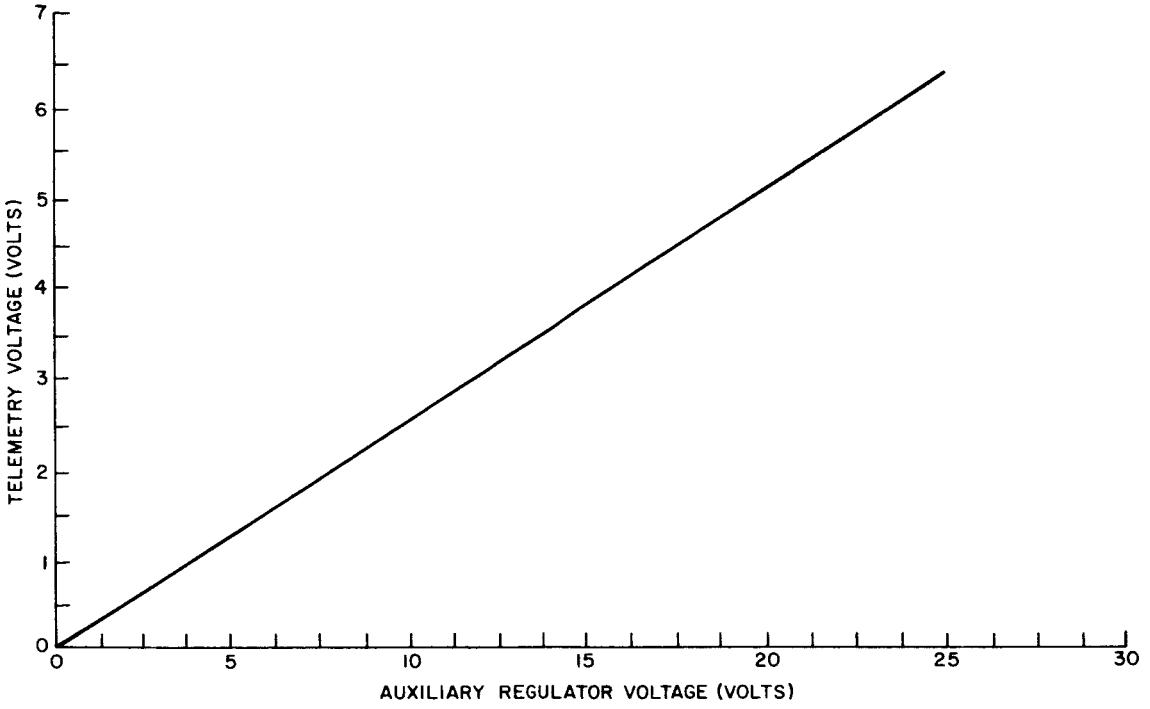


Figure 42. Typical Auxiliary Regulator Voltage Telemetry Calibration Curve

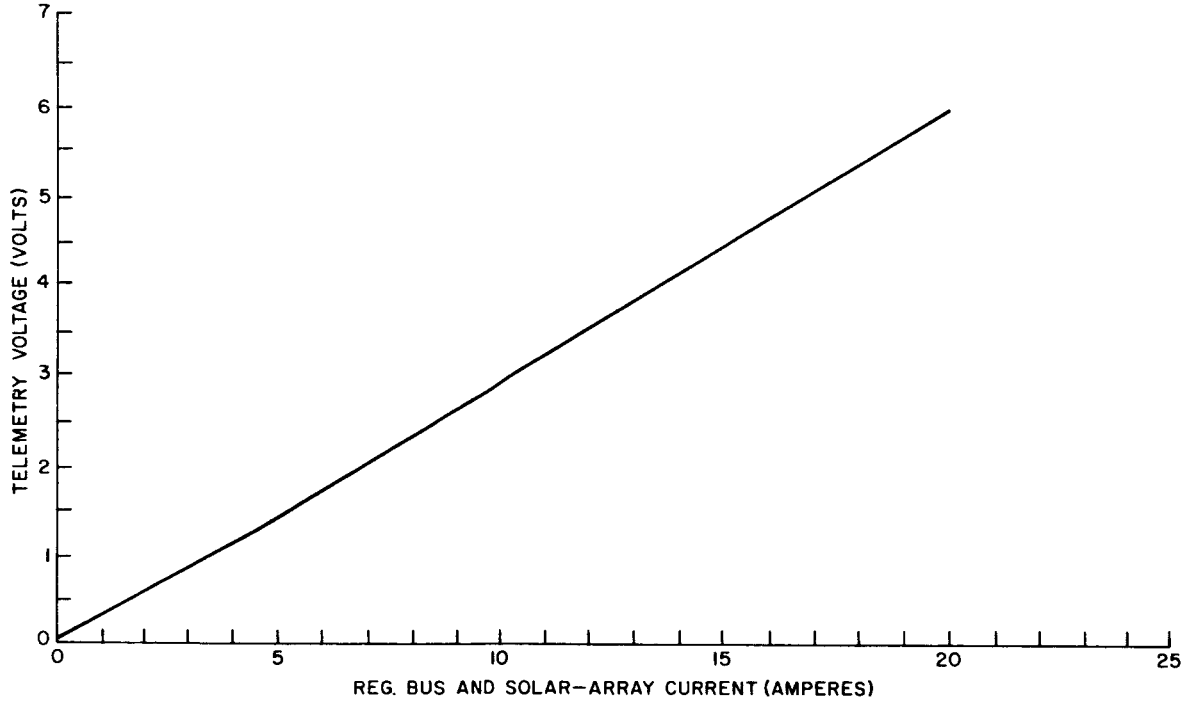


Figure 43. Typical Regulated-Bus and Solar-Array Current Telemetry Calibration Curve

BLANK PAGE 82

SECTION III
STORAGE BATTERIES

A. GENERAL

During this report period, the following technical studies were performed in the development of the Nimbus-B battery module:

(1) Analysis of "Crane" cycling data for General Electric and Gulton "Nimbus" type cells was continued;

(2) Preliminary "parametric study" curves were revised;

(3) Preliminary curves were prepared indicating cell voltages during the launch phase; and

(4) A battery module test was performed to determine the feasibility of applying battery power to blow the regulated bus fuses.

Results and data from each of the above studies are discussed in this section.

B. ANALYSIS OF "CRANE" DATA

Thirty Nimbus type cells each from General Electric and Gulton Industries were submitted to the Quality Evaluation Laboratory of the U.S. Naval Ammunition Depot at Crane, Indiana by NASA. The "Crane" cycling tests consist of testing six groups of five cells from each cell manufacturer at three temperatures (0°C, 25°C, and 40°C) and two depths of discharge. The data have been made available to AED for the first 3800 cycles for the 15 percent depth of discharge tests, and the first 3200 cycles for the 25 percent depth of discharge tests. These data are plotted on Figure 44 for the General Electric cells; both end-of-charge and end-of-discharge voltages are plotted as a function of cycle number. The data for the Gulton cells has not yet been plotted and analyzed.

The data from Figure 44 have been cross-plotted on Figures 45, 46, 47 and 48 to show the average cell voltage at end-of-discharge both as functions of depth of discharge and of temperature, for four selected time cycles: 2250 cycles, 2750 cycles, 3250 cycles, and 3750 cycles, respectively. On the graphs showing end-of-discharge voltage as a function of temperature two curves have been added to the experimental curves for 15 percent and 25 percent depths of discharge by interpolation and extrapolation of the end-of-discharge versus depth-of-discharge curves. For 3750 cycles only, the 15 percent temperature data were available.

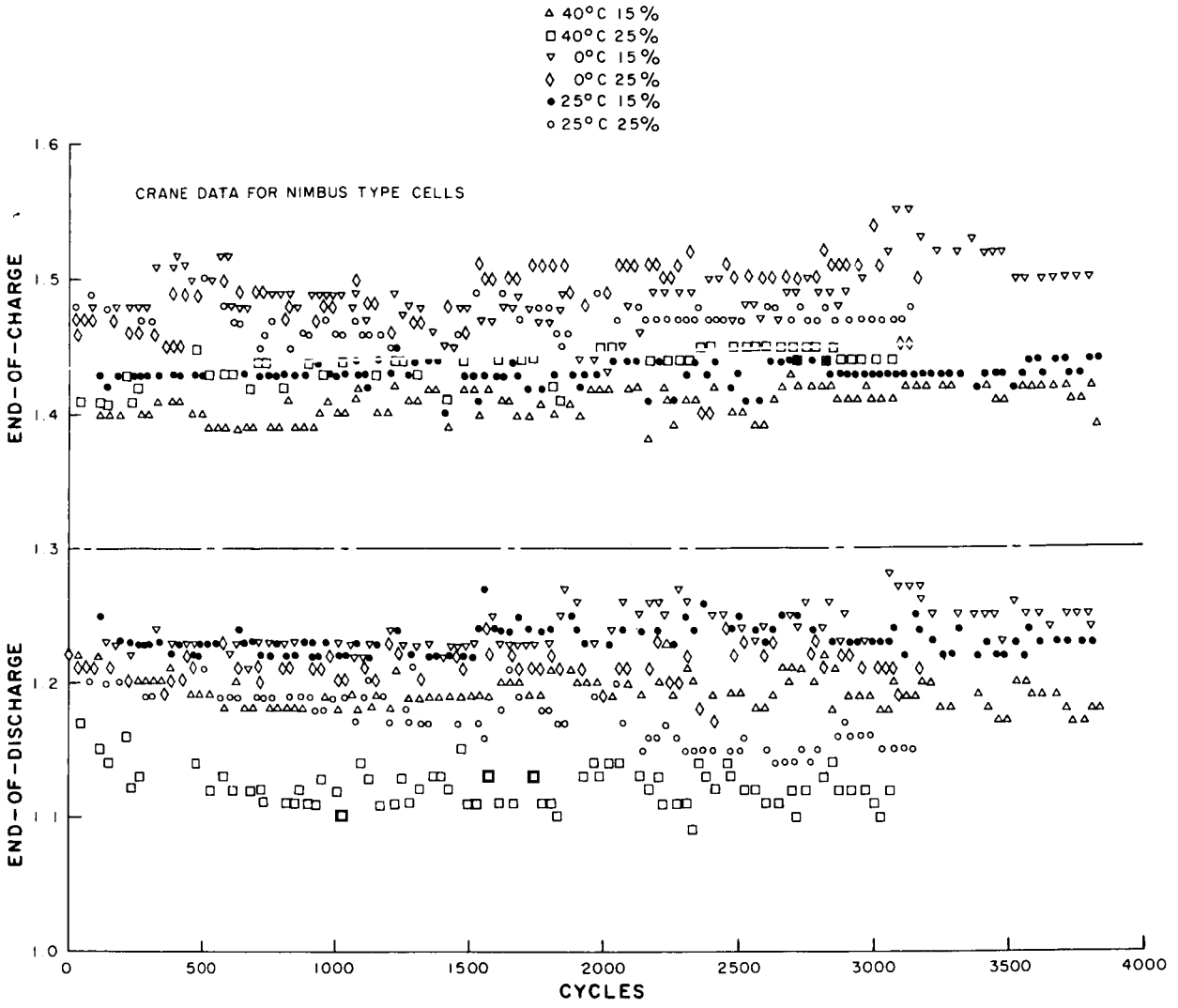
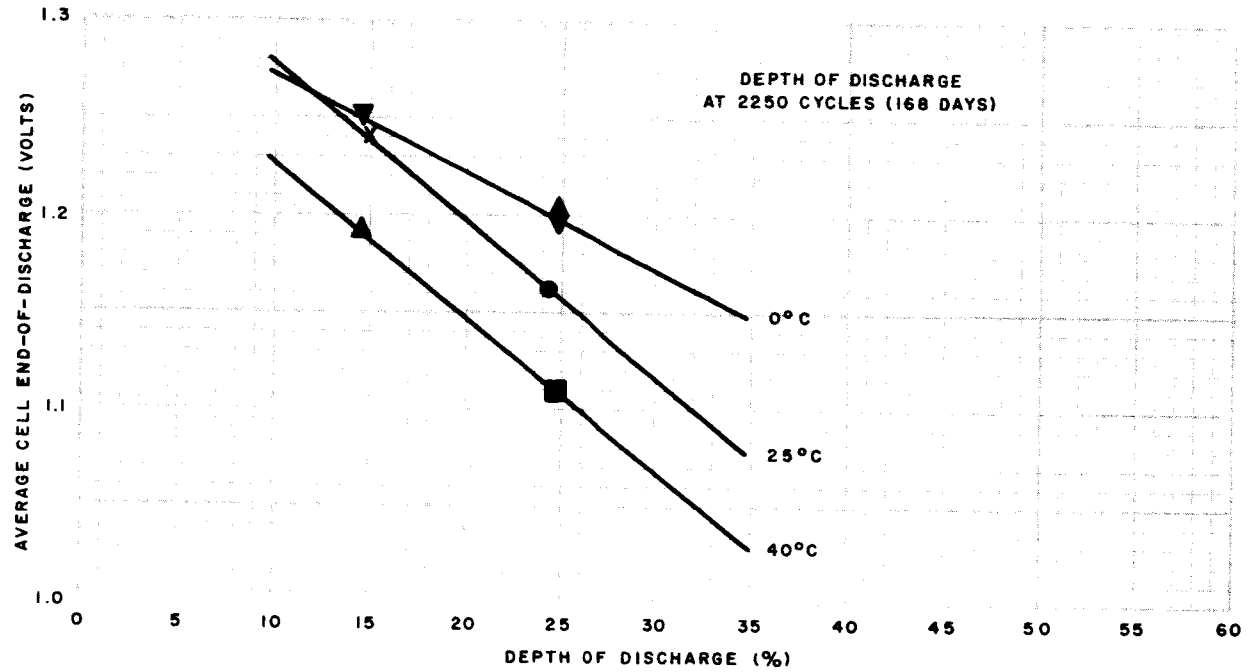


Figure 44. General Electric Average Cell Voltage Versus Cycle

Figures 49, 50 and 51 were prepared from the plots of end-of-discharge voltage as a function of temperature by interpolation and extrapolation. These latter three figures expand the "Crane" data for General Electric cells to give a clear picture of end-of-discharge voltage as a function of cycle life for 10 percent, 15 percent, and 20 percent depths of discharge, and for 10°, 20°, 30°, 35°, 40°, and 45°C temperatures at each depth of discharge. From a slight extrapolation of Figure 50 (15 percent depth of discharge) a prediction of cycling capability such as that included in Table 9 can be made (4866 cycles are equivalent to one year).



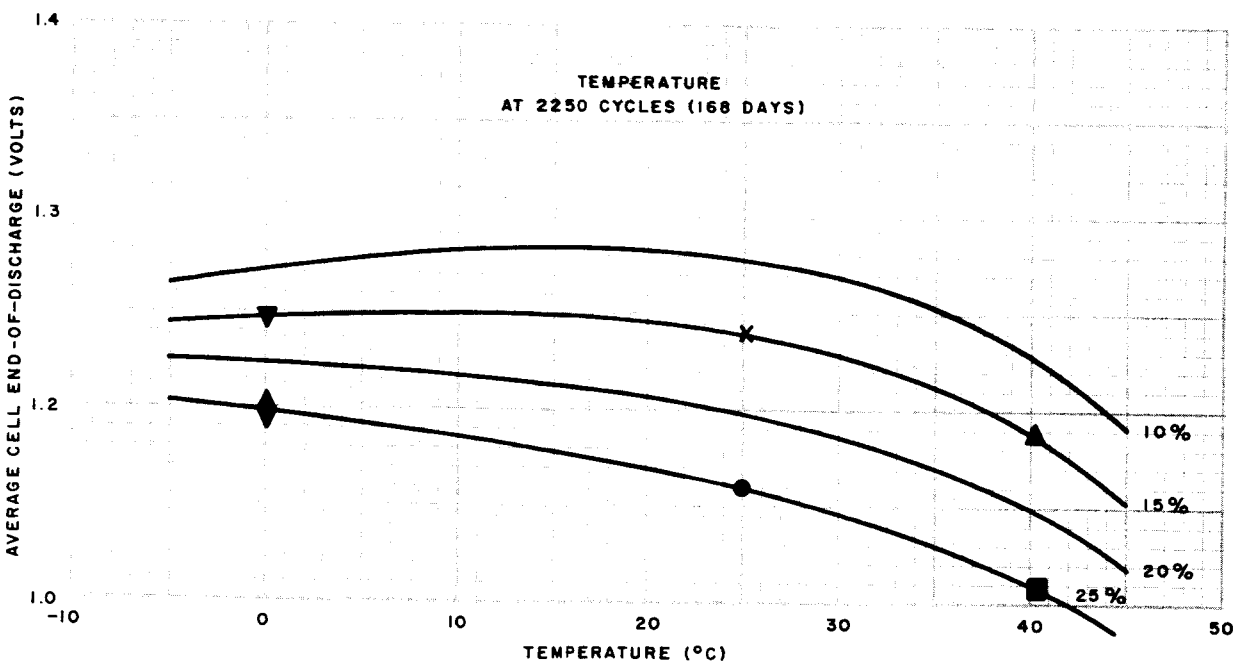
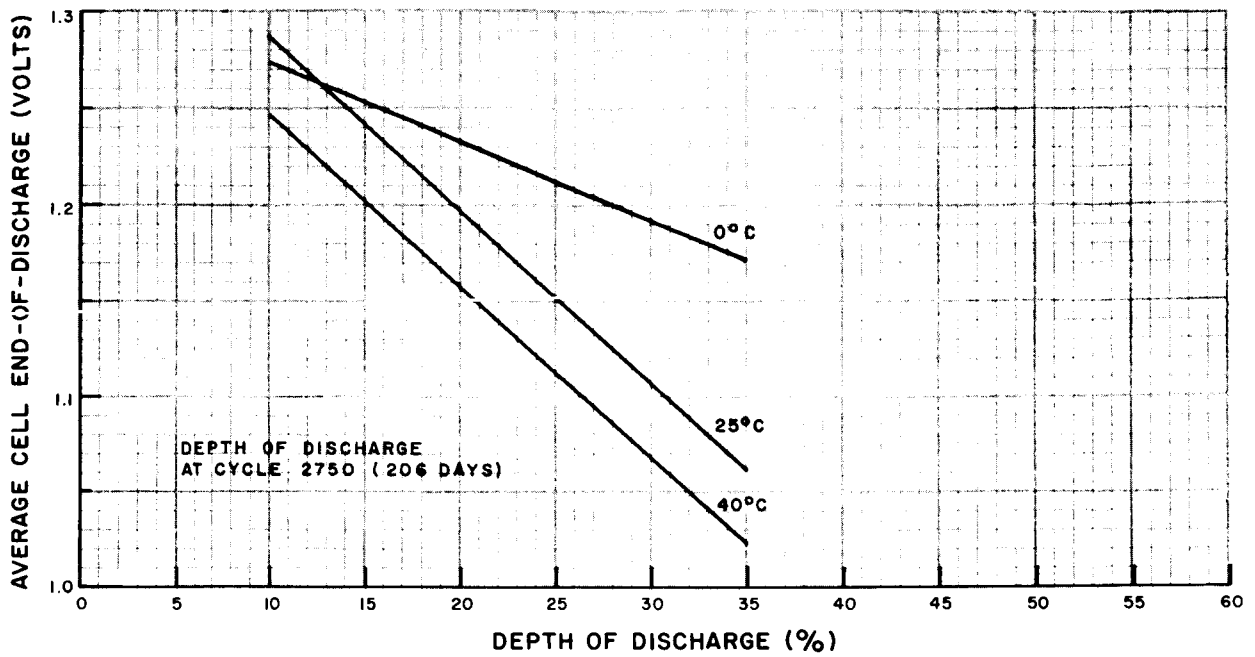


Figure 45. Average Cell Voltage Versus Depth-of-Discharge and Temperature at 2250 Cycles



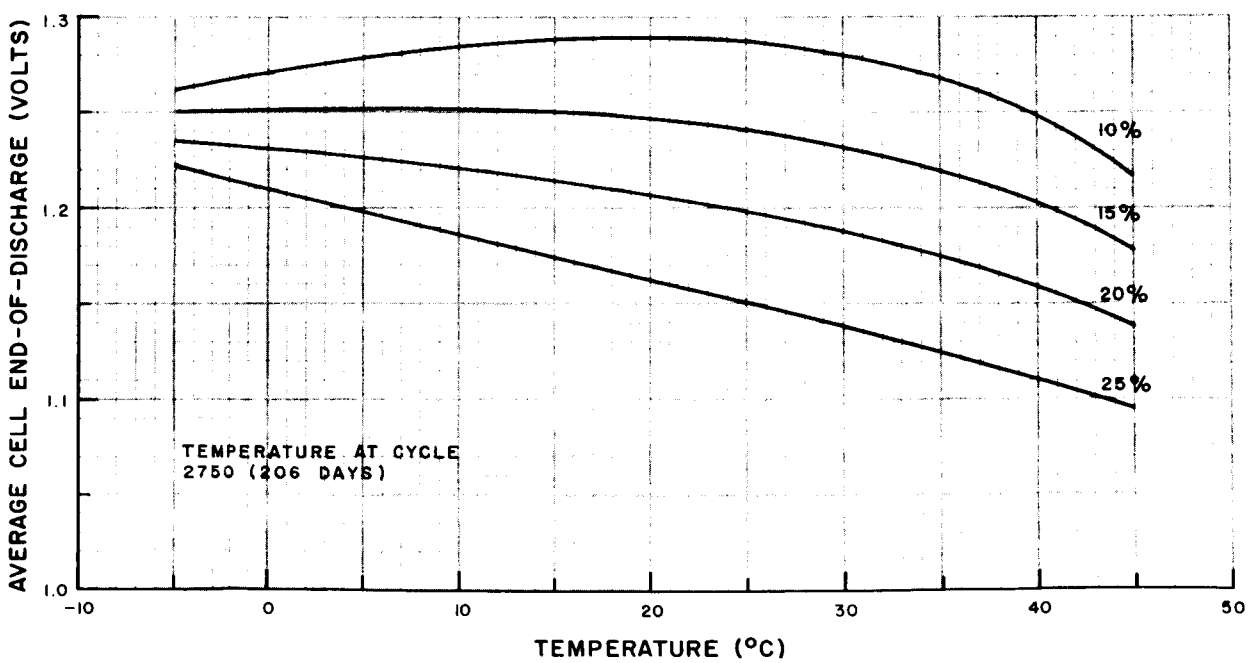
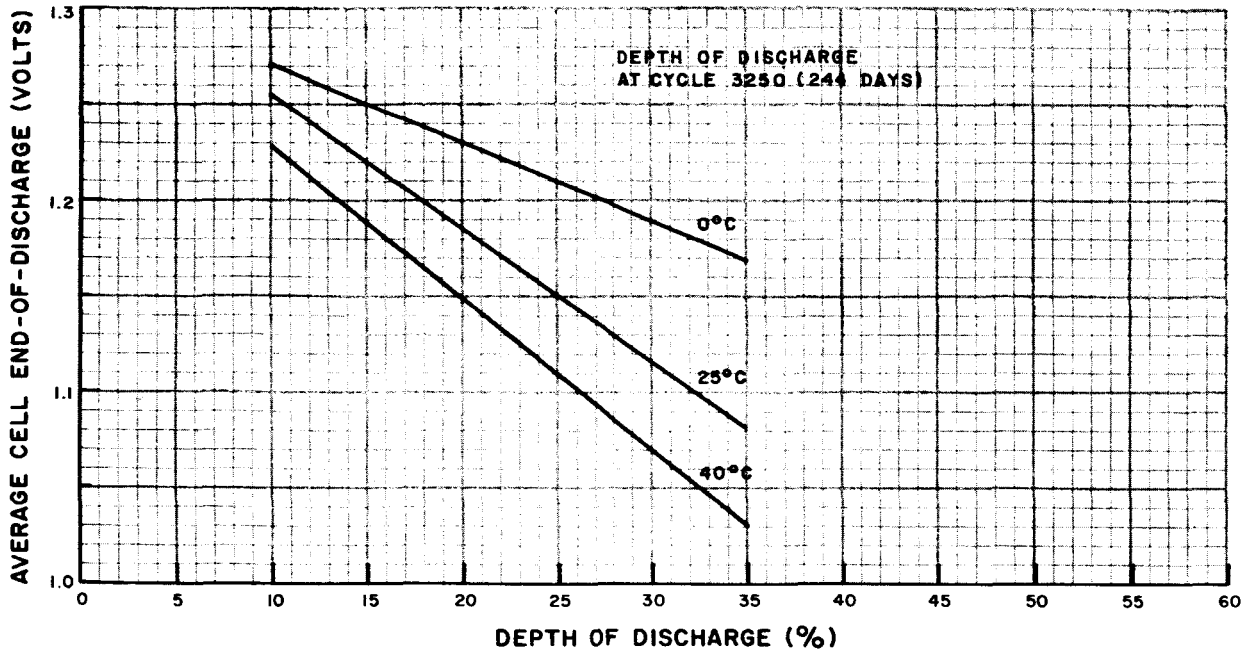


Figure 46. Average Cell Voltage Versus Depth-of-Discharge and Temperature at 2750 Cycles



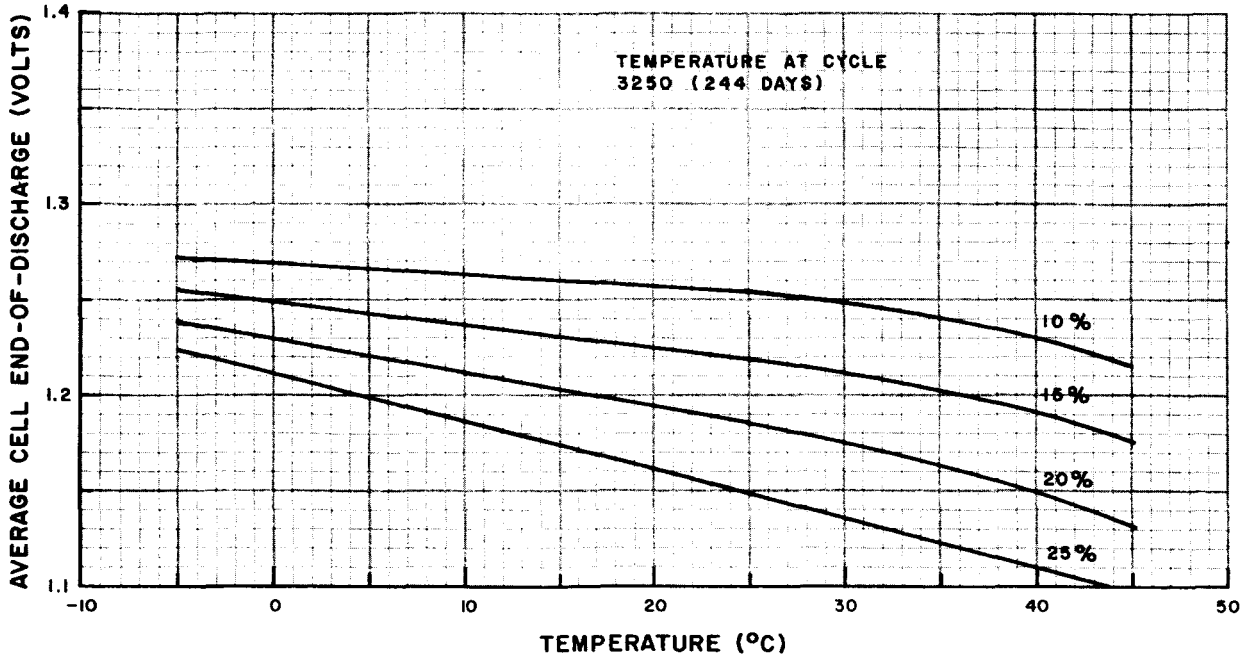


Figure 47. Average Cell Voltage Versus Depth-of-Discharge and Temperature at 3250 Cycles

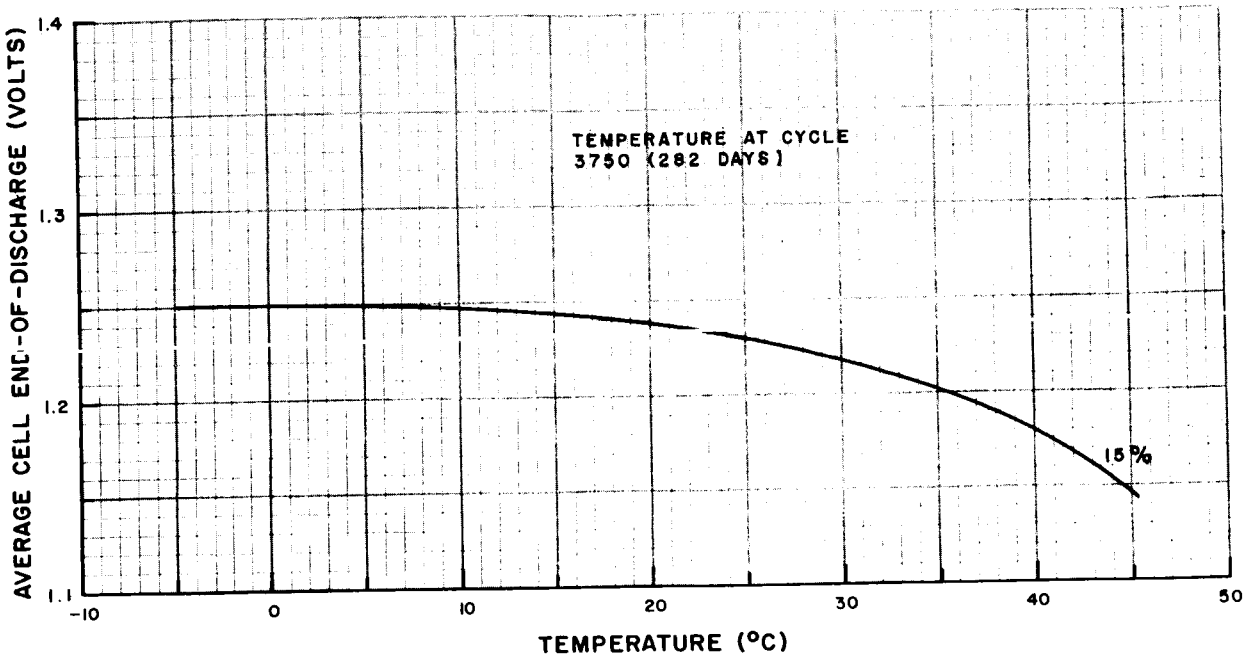


Figure 48. Average Cell Voltage Versus Temperature at 3750 Cycles

TABLE 9. CELL CYCLE LIFE VERSUS TEMPERATURES AT 15 PERCENT DEPTH OF DISCHARGE

Temperature (°C)	Number of Cycles at 15% Depth of Discharge	
	To 27.0 V/Module	To 26.5 V/Module
10	5000 +	5000 +
20	5000 +	5000 +
30	4850	5000 +
35	4600	5000
40	3850	4300
45	3100	3700

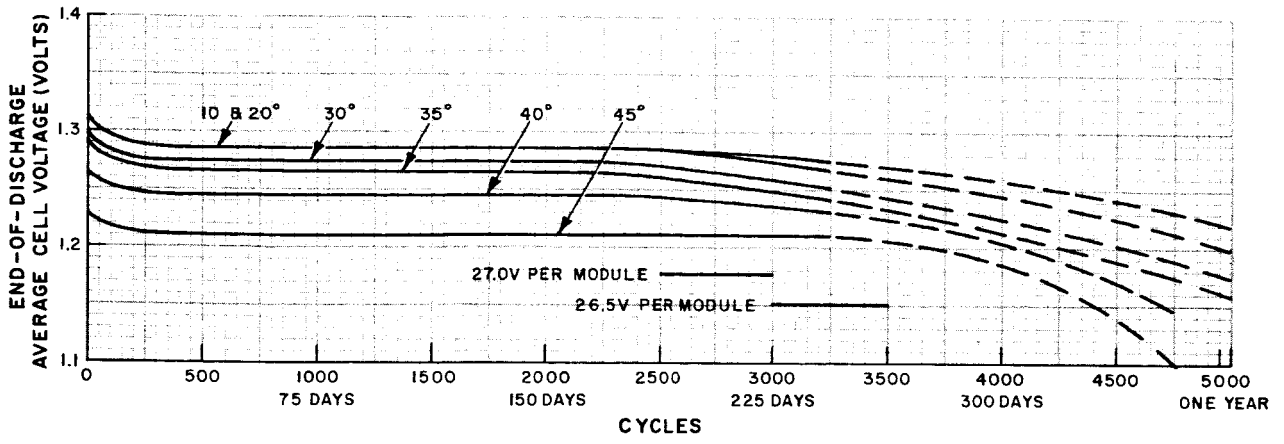


Figure 49. Average Cell Voltage Versus Cycle at 10 Percent Depth of Discharge

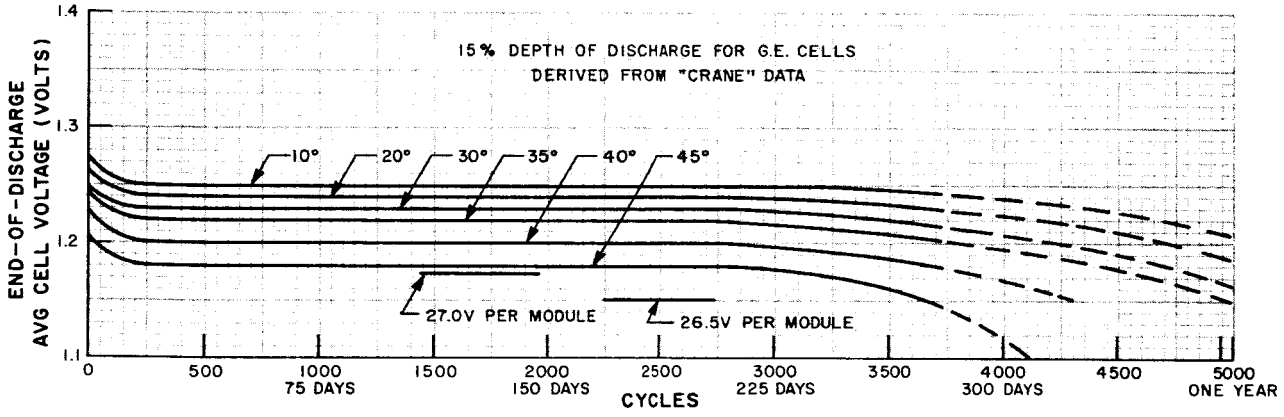


Figure 50. Average Cell Voltage Versus Cycle at 15 Percent Depth of Discharge

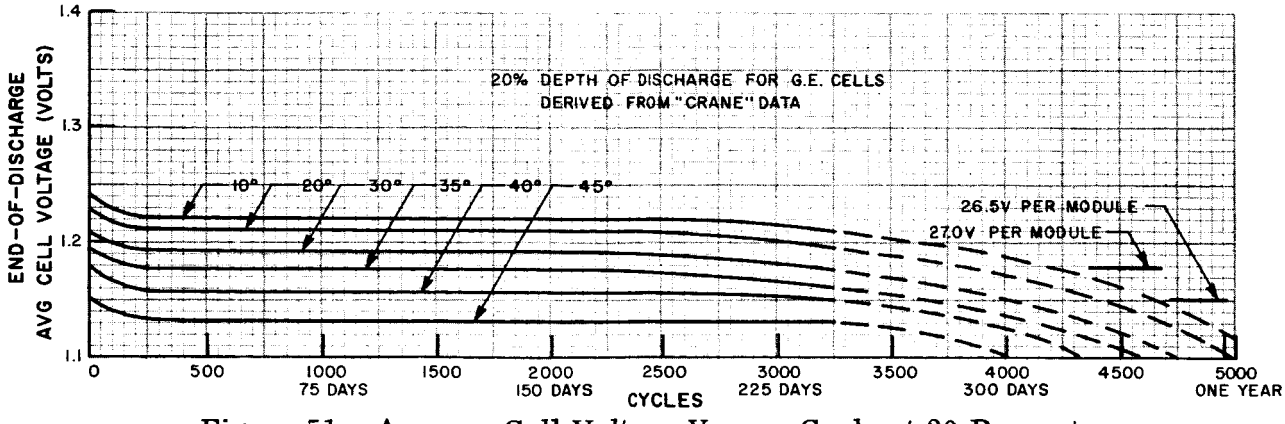


Figure 51. Average Cell Voltage Versus Cycle at 20 Percent Depth of Discharge

C. PRELIMINARY "PARAMETRIC STUDY" CURVES

In order to proceed with the computer program for the Nimbus-B power supply subsystem, it was necessary to provide data as computer inputs. Estimates had been previously made, and were included in the QuarterlyTechnical Report No. 1 for cell charge and discharge voltages at 25°C. During the current report period, the cell discharge voltage at 25°C estimates were revised, and, in addition, curves were prepared for discharge and charge cell voltages at 15°C and 35°C, reflecting first day, 6 months, 9 months, and 12 months of continuous operation. These estimates of cell voltages are shown in Figures 52 through 61.

Although the curves indicate overcharge at 1.2 amperes at 15°C, this is not a normal operating mode in the Nimbus-B power subsystem and is not recommended for the cells. The computer inputs include voltage limits as a function of temperature; the computer would, therefore, not permit the full charge current at 15°C, but would limit the voltage to 1.49 volts per cell.

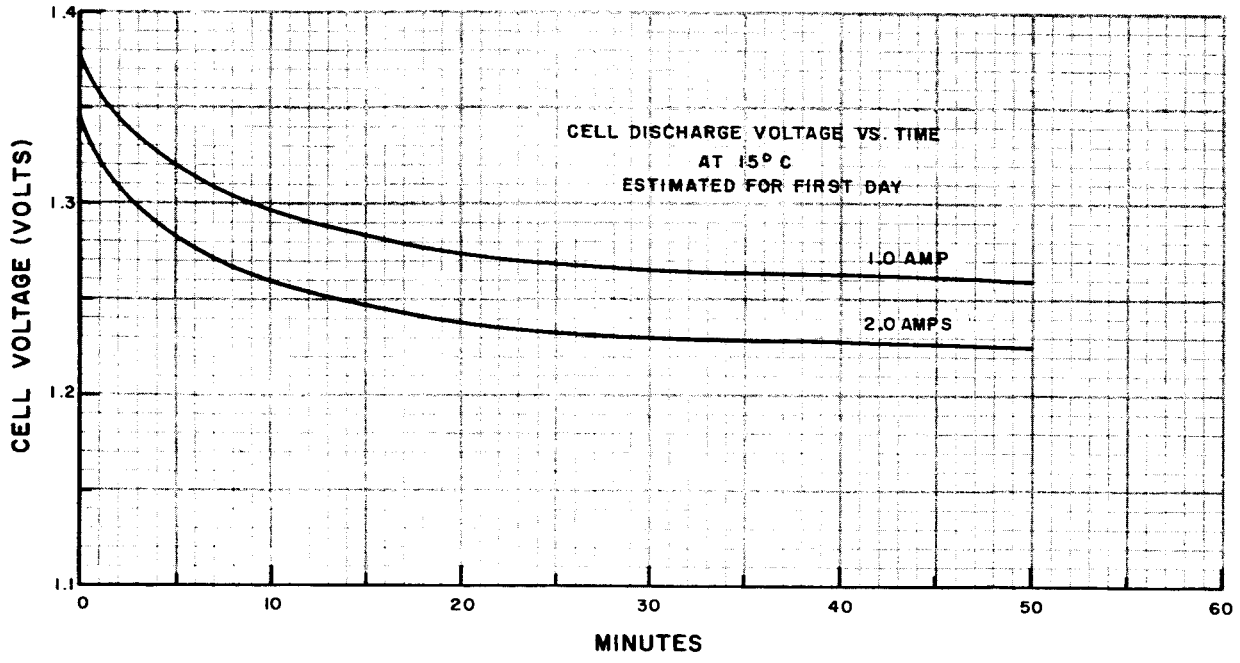
D. PRELIMINARY "LAUNCH PHASE" CURVES

Since a computer study was also scheduled to simulate the launch phase of the Nimbus-B mission, it was necessary to prepare estimates for the cell voltage during discharge and charge under the expected launch conditions. Preliminary curves were made for 15°C to 25°C, and at 35°C as shown in Figures 62 and 63. The discharge time and the various recharge curves are based on the assumption that sun acquisition is accomplished in either the first, second, or third earth orbit (either 80 minutes, 180 minutes, or 250 minutes). The discharge of 0.69 ampere is based on a 137-watt load on the battery.

E. BATTERY MODULE POWER TO REGULATED BUS FUSES (SPECIAL TEST)

On January 11, 1966, a special test was performed to determine the feasibility of applying Nimbus-B battery module power to blow the regulated-bus fuses when a short-circuit condition was present on the regulated bus. Additional power to the regulated bus during this failure mode is required in order to protect the regulator transistor in the Nimbus-B electronics module.

No deterioration of the cell wiring or the connector was noted after completion of the high-current testing. The maximum current obtained during the test was 59 amperes into a 0.25-ohm load. This special battery test indicated that the Nimbus-B battery modules can be used to supply additional power to the regulated bus fuses under malfunction conditions. It is strongly recommended that six or more isolated, parallel circuits be used in the Nimbus-B power supply subsystem to maintain the storage cell voltages above 1.0 volt during high-current discharges.



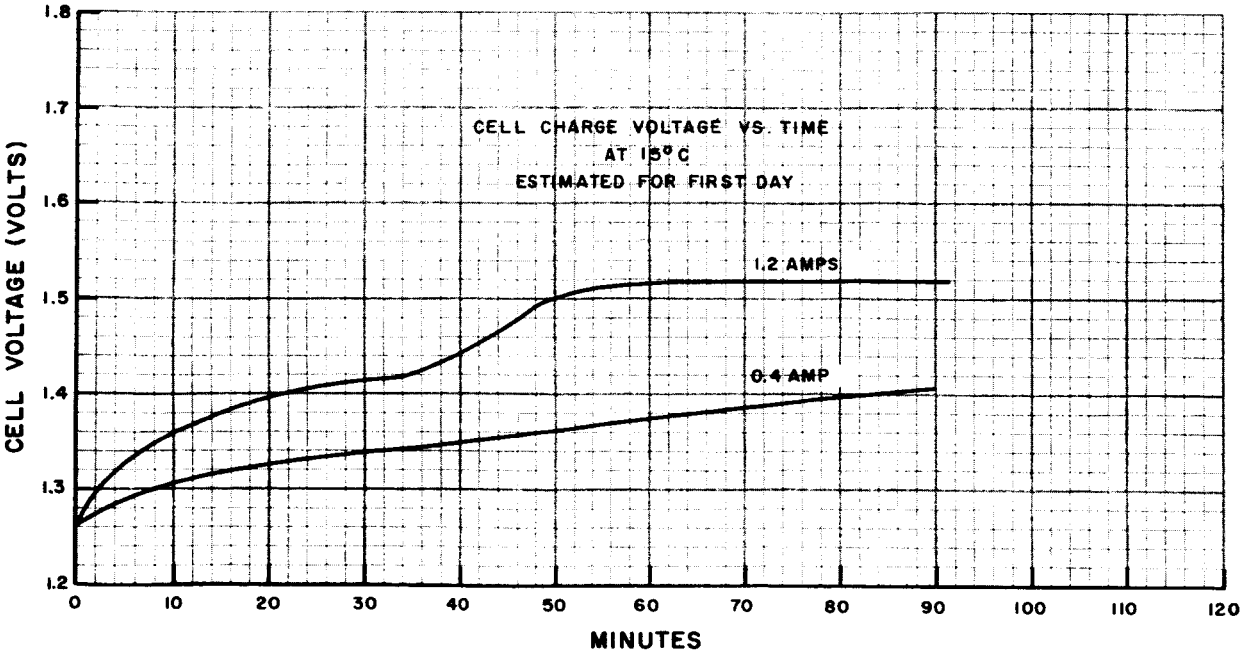


Figure 52. Cell Charge and Discharge Voltages Versus Time at 15°C, First-Day Estimate

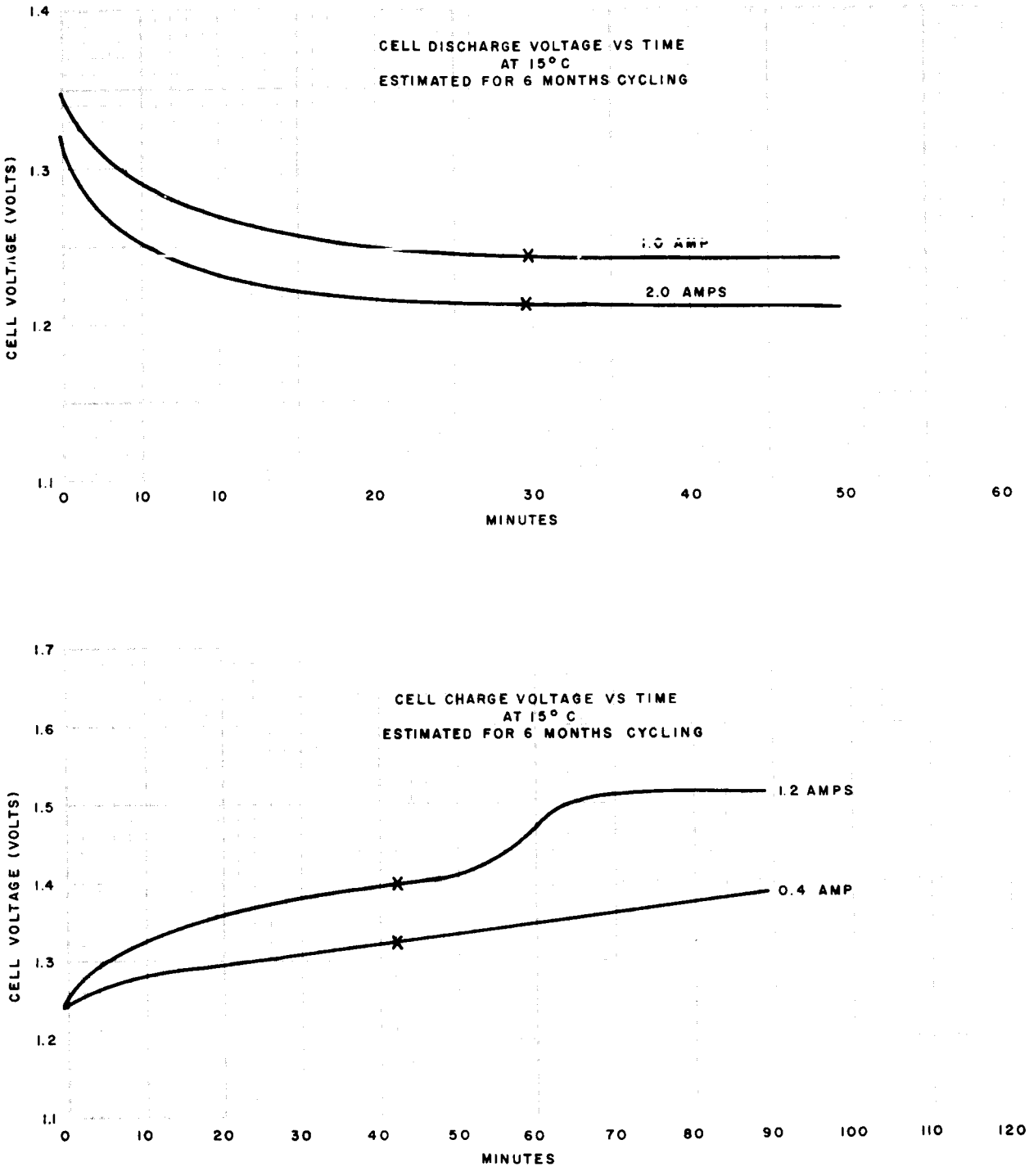
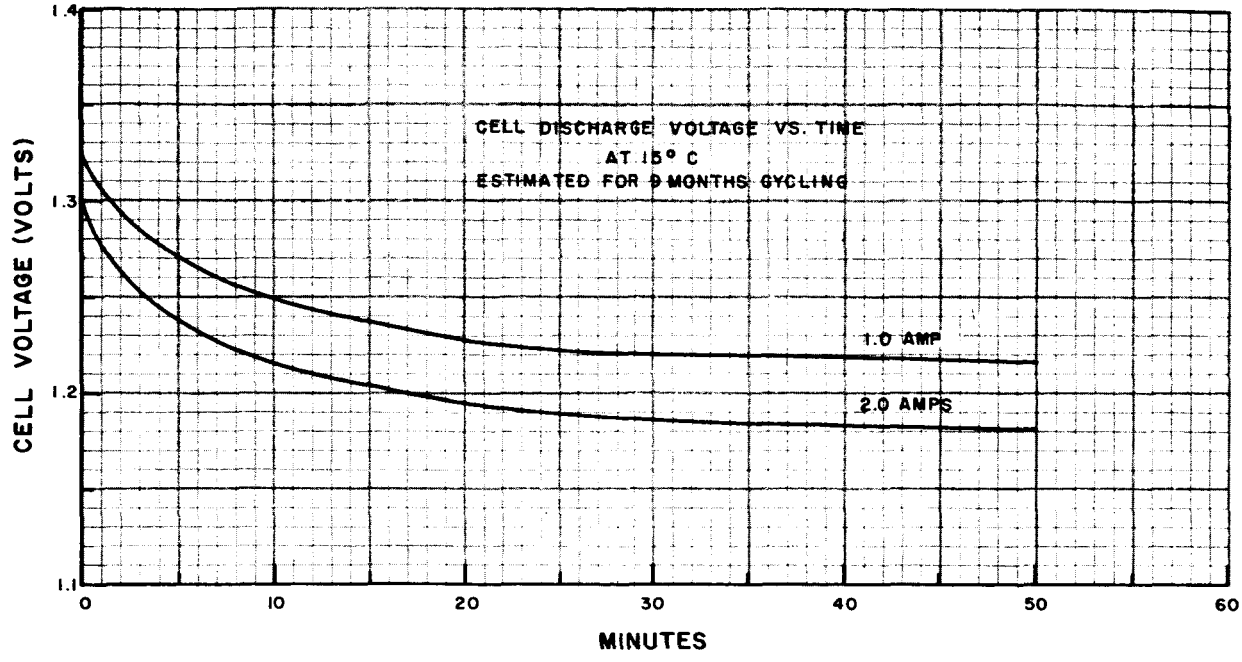


Figure 53. Cell Charge and Discharge Voltages Versus Time at 15°C, 6 Months Cycling Estimate



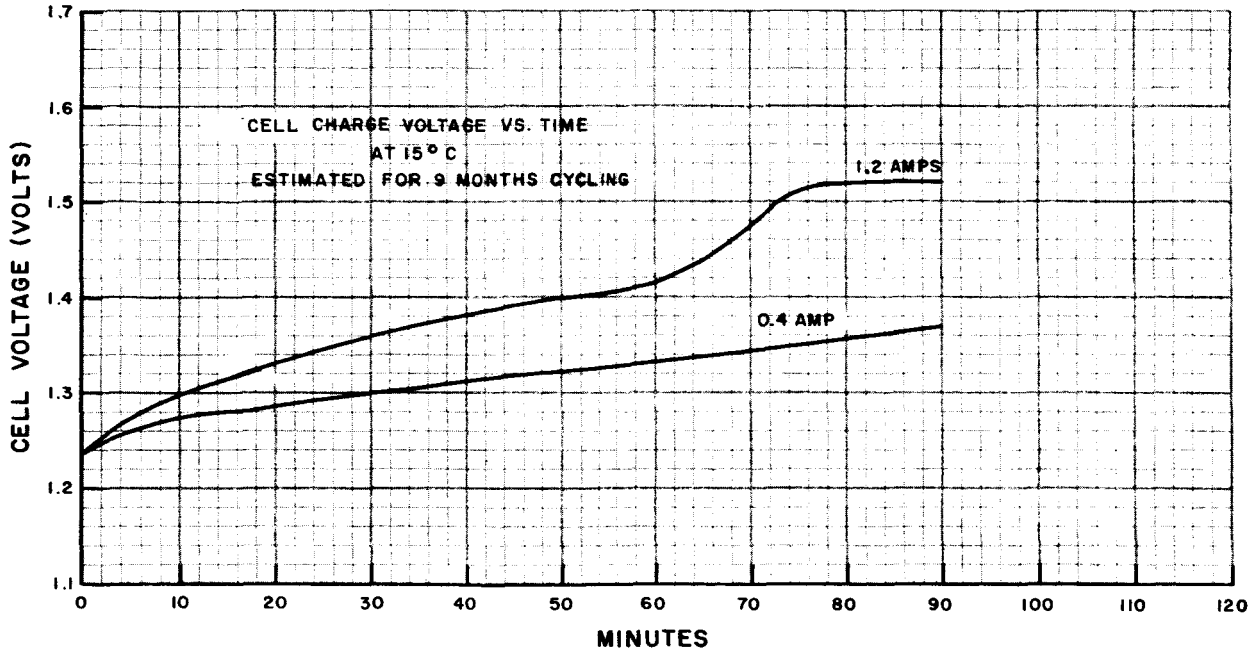
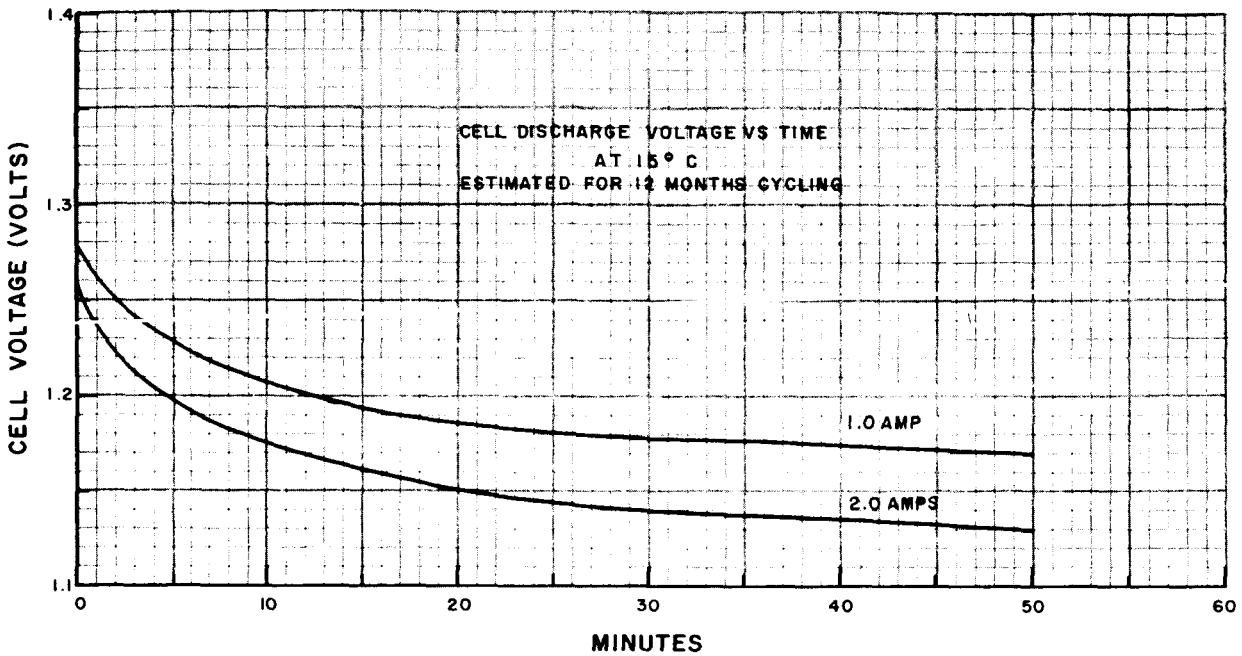


Figure 54. Cell Charge and Discharge Voltages Versus Time at 15°C, 9 Months Cycling Estimate



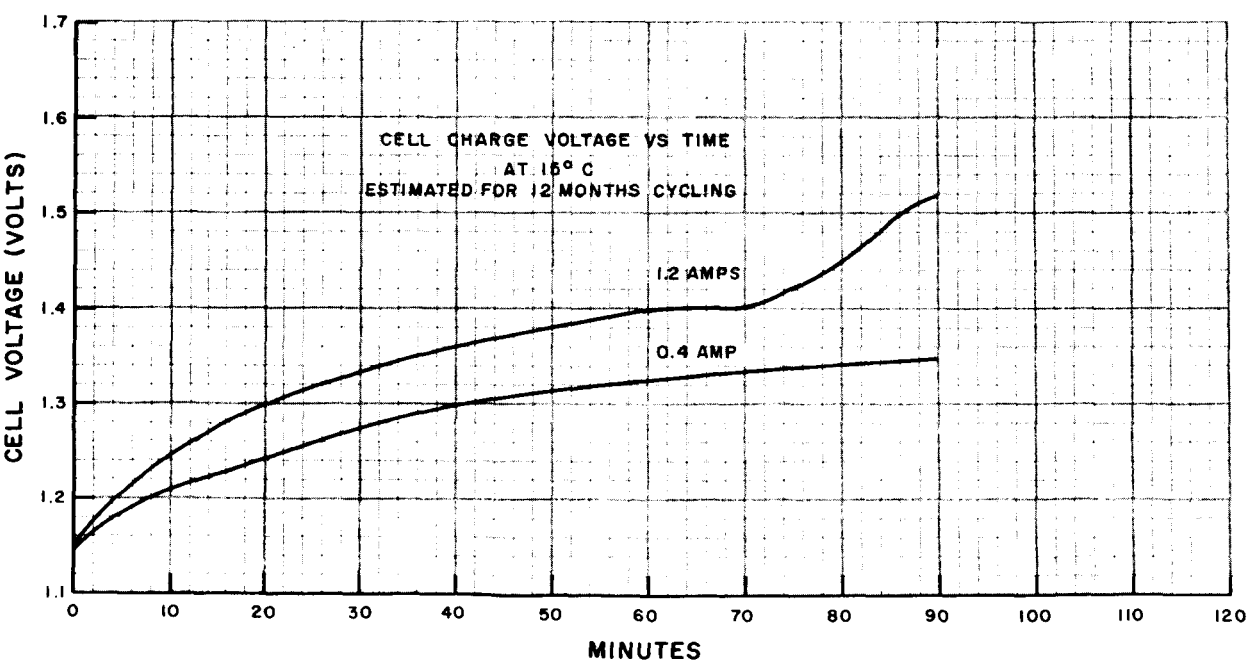
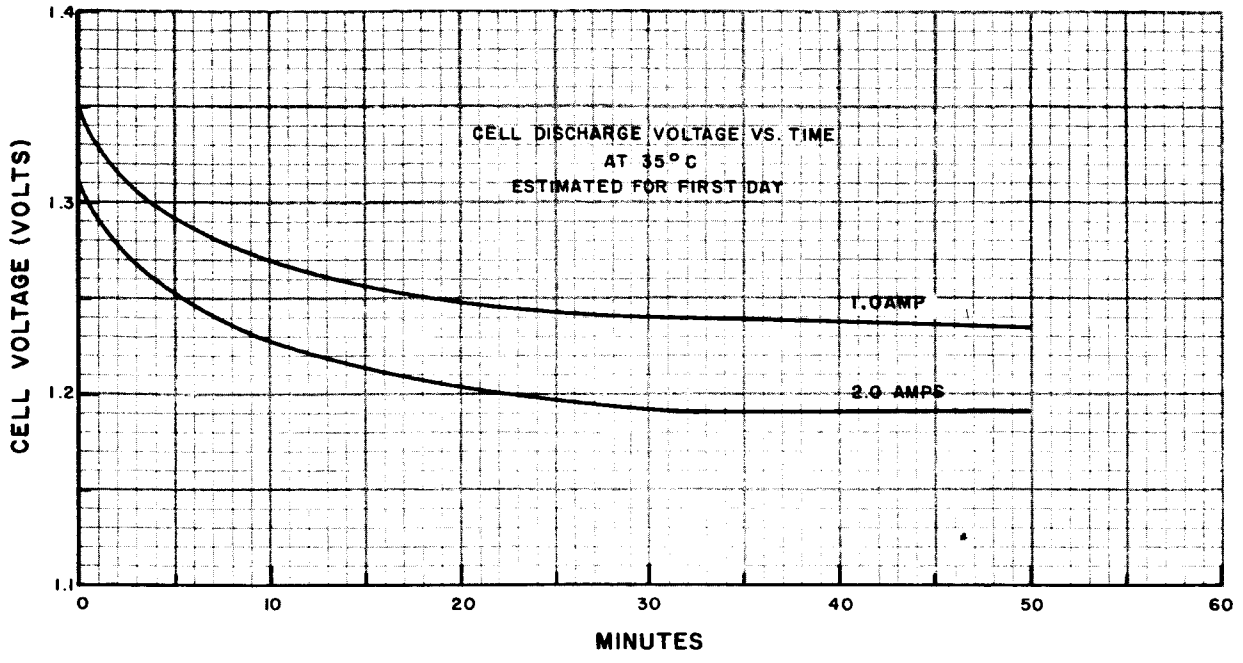


Figure 55. Cell Charge and Discharge Voltages Versus Time at 15°C, 12 Months Cycling Estimate



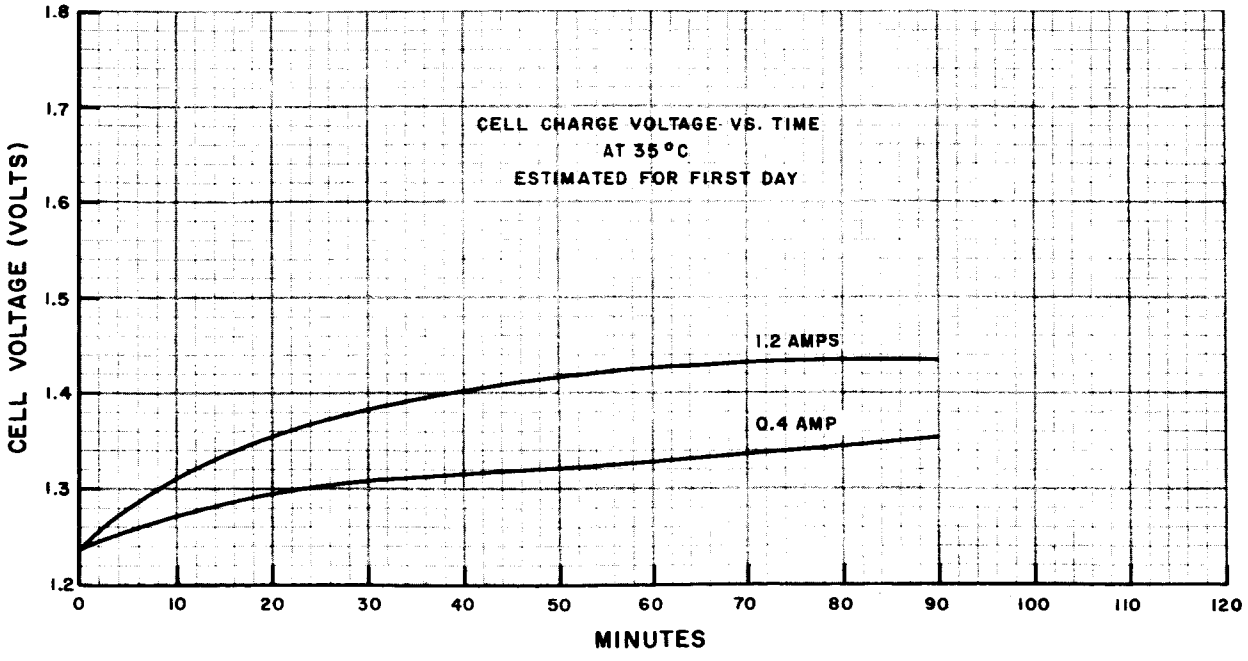
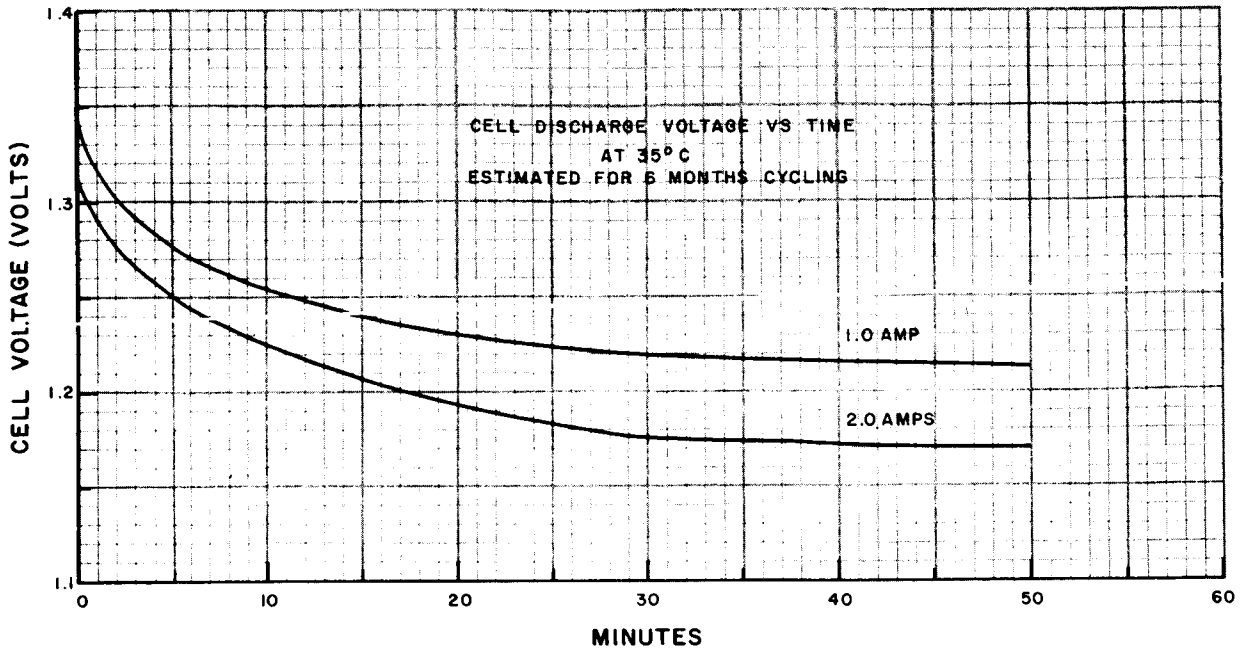


Figure 56. Cell Charge and Discharge Voltages Versus Time at 35°C, First-Day Estimate



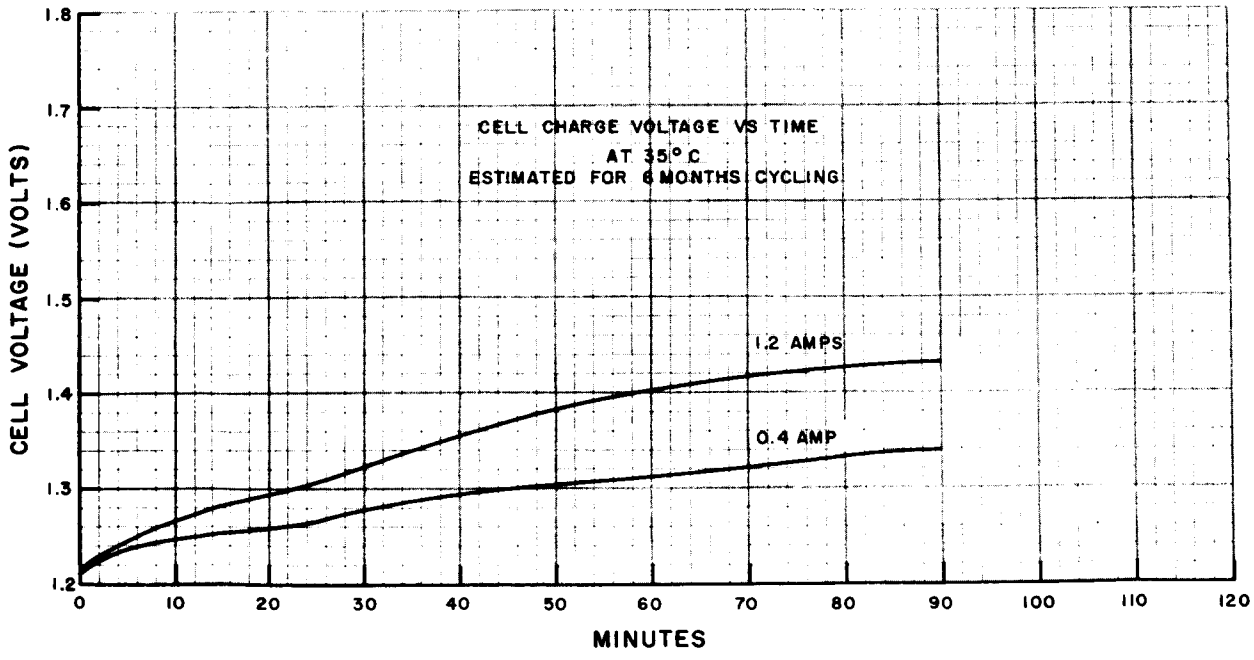
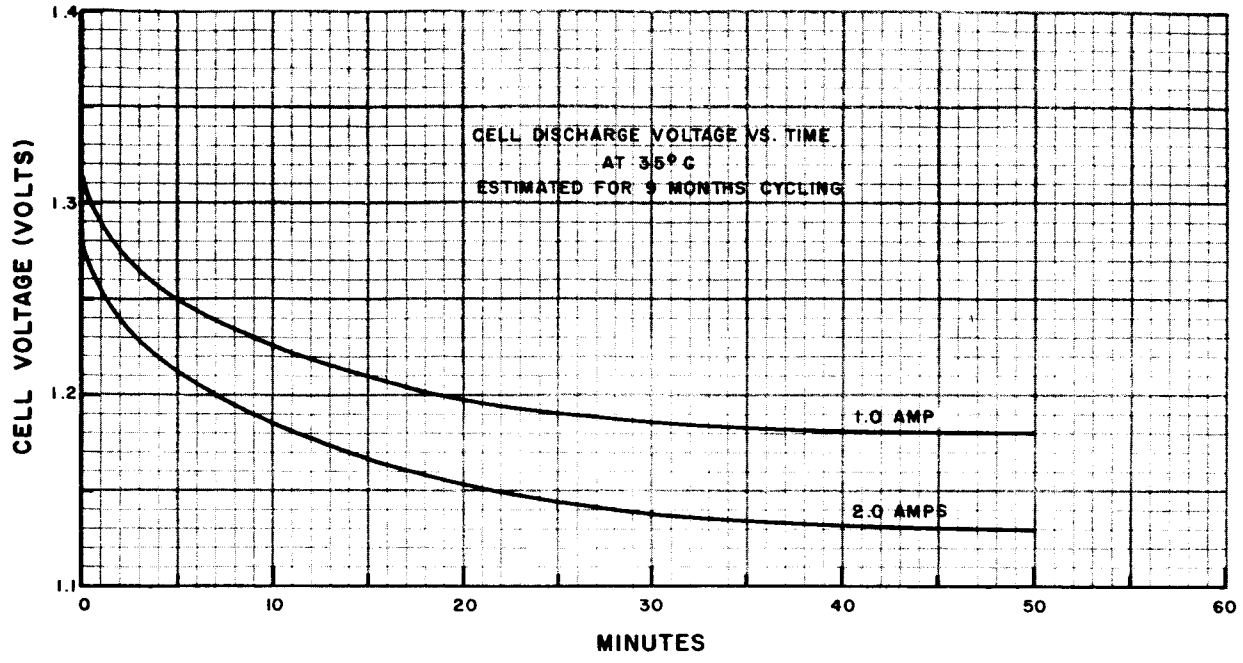


Figure 57. Cell Charge and Discharge Voltages Versus Time at 35°C, 6 Months Cycling Estimate



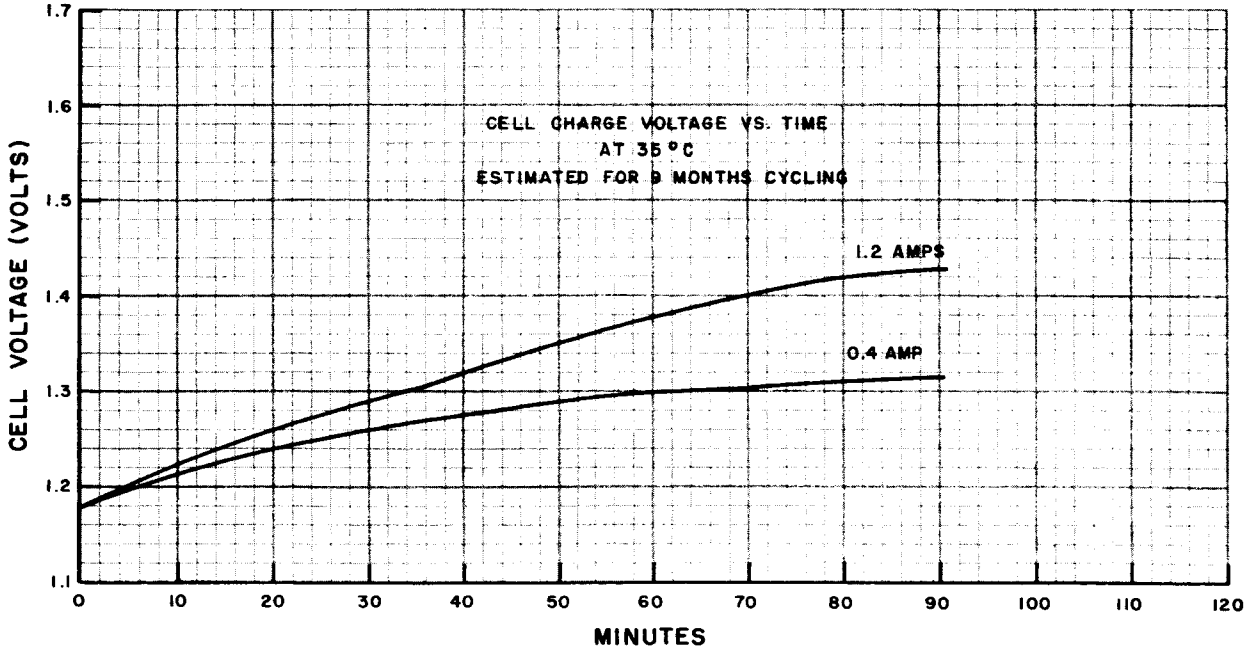


Figure 58. Cell Charge and Discharge Voltages Versus Time at 35°C, 9 Months Cycling Estimate

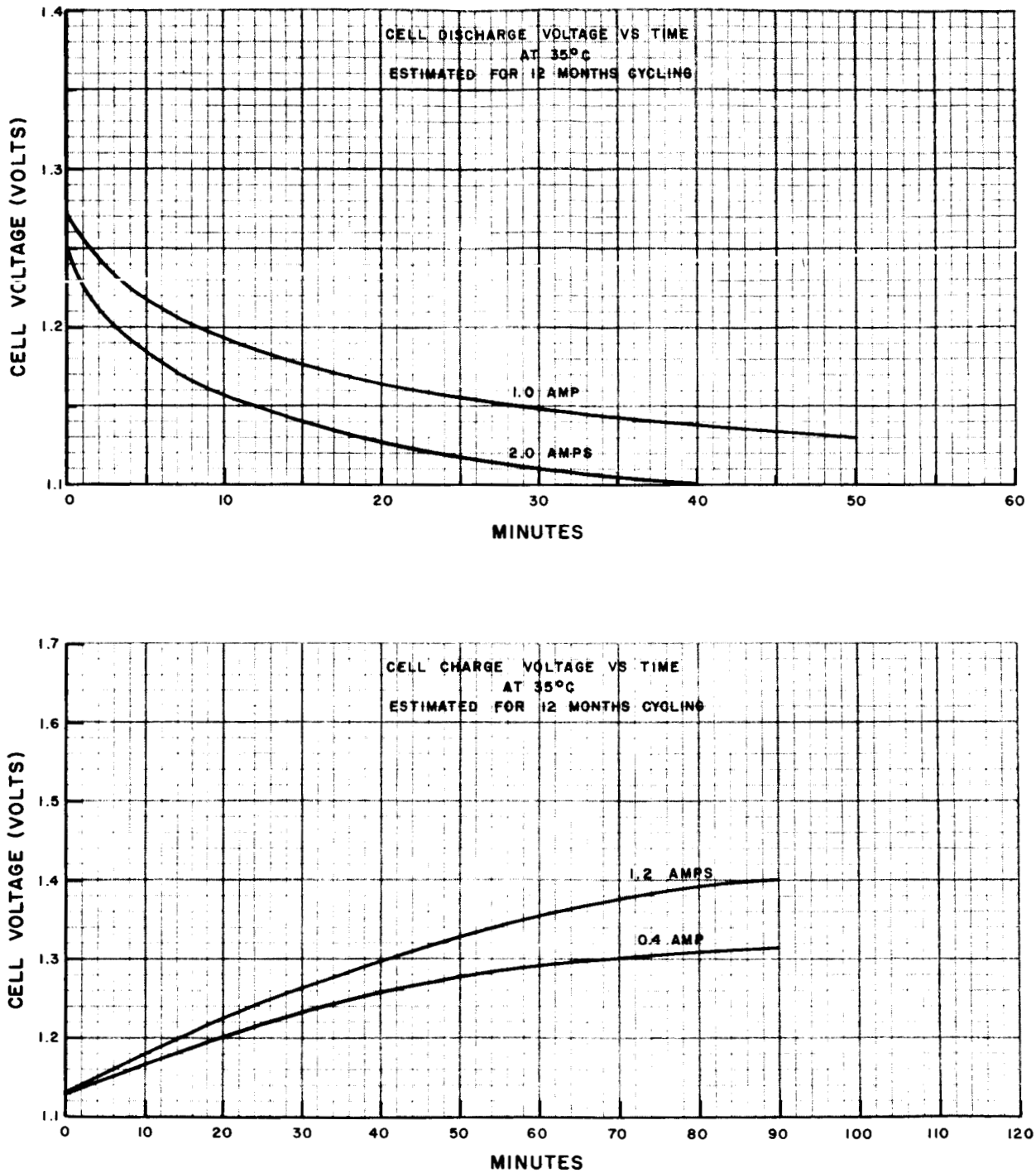
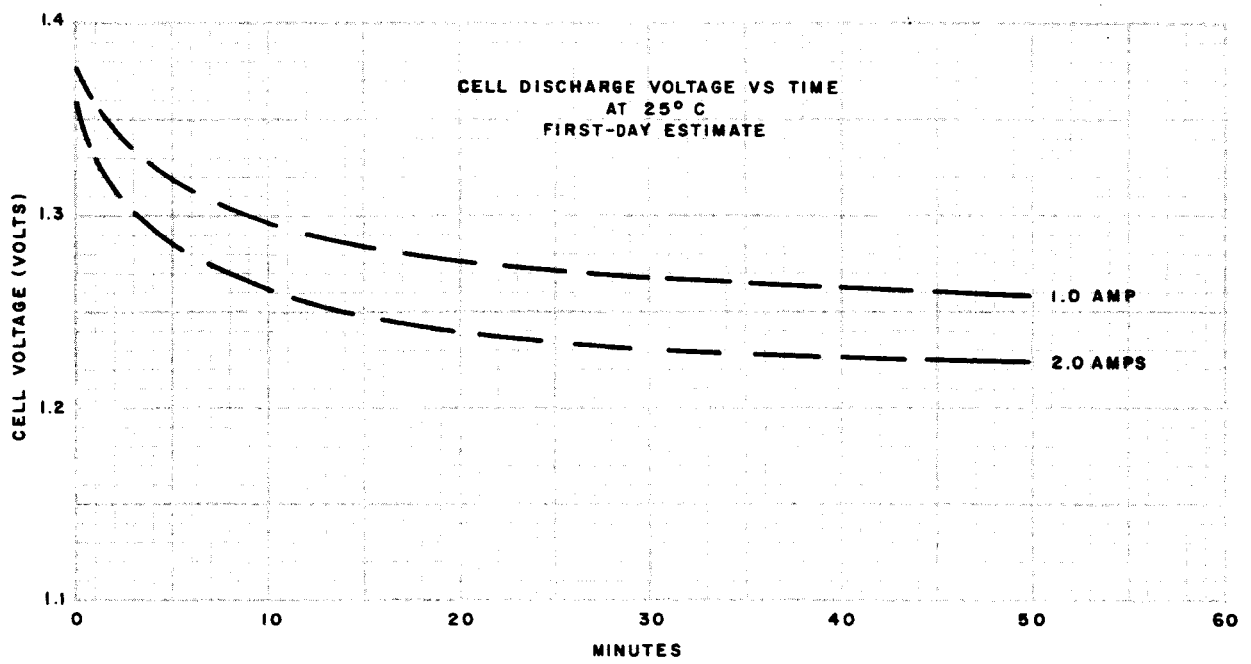


Figure 59. Cell Charge and Discharge Voltages Versus Time at 35°C, 12 Months Cycling Estimate



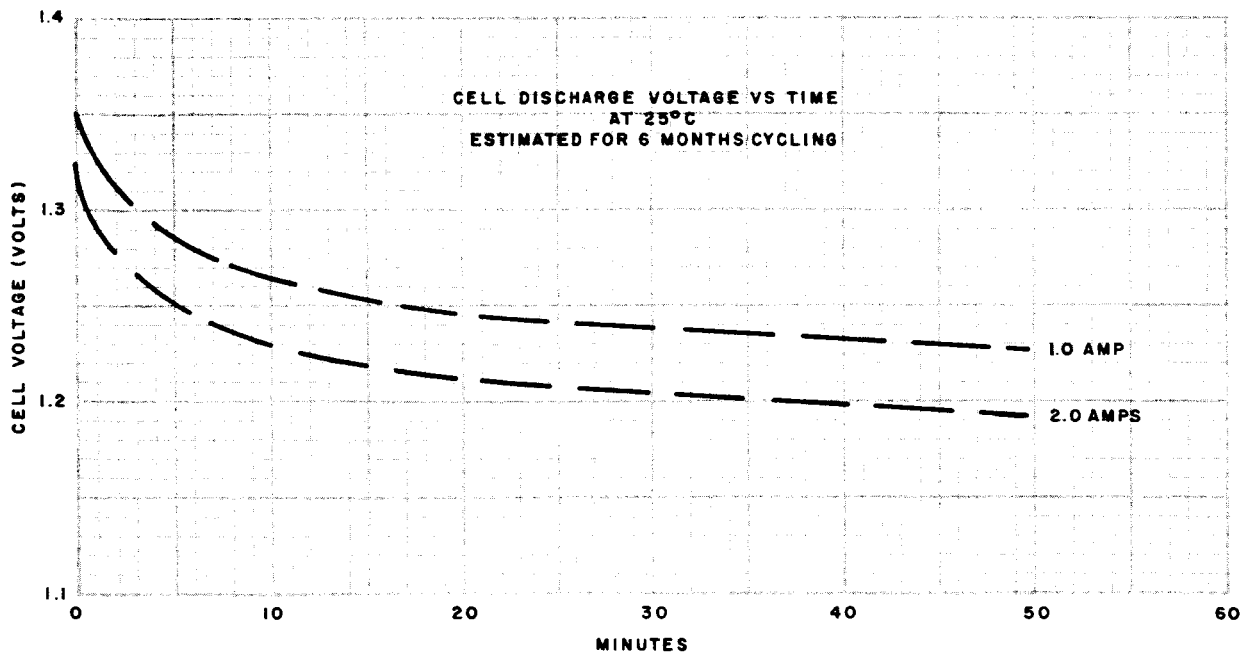
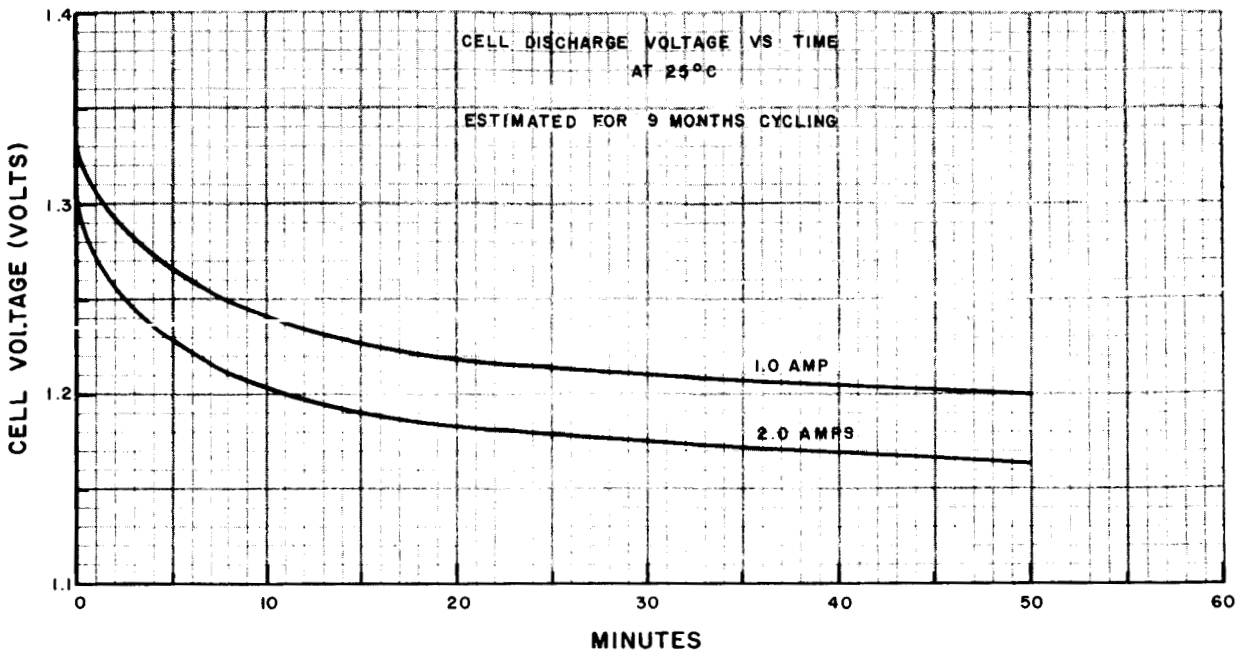


Figure 60. Cell Discharge Voltages Versus Time at 25°C, First-Day and 6 Months Cycling Estimates



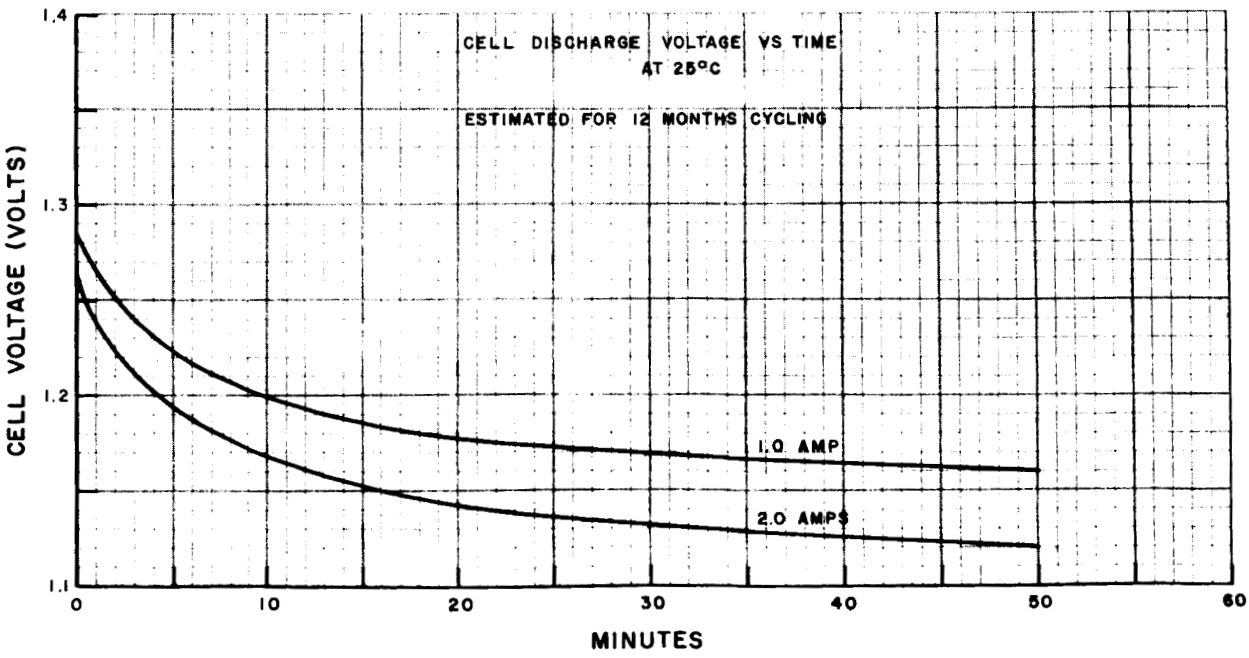


Figure 61. Cell Discharge Voltages Versus Time at 25°C, 9 and 12 Months Cycling Estimates

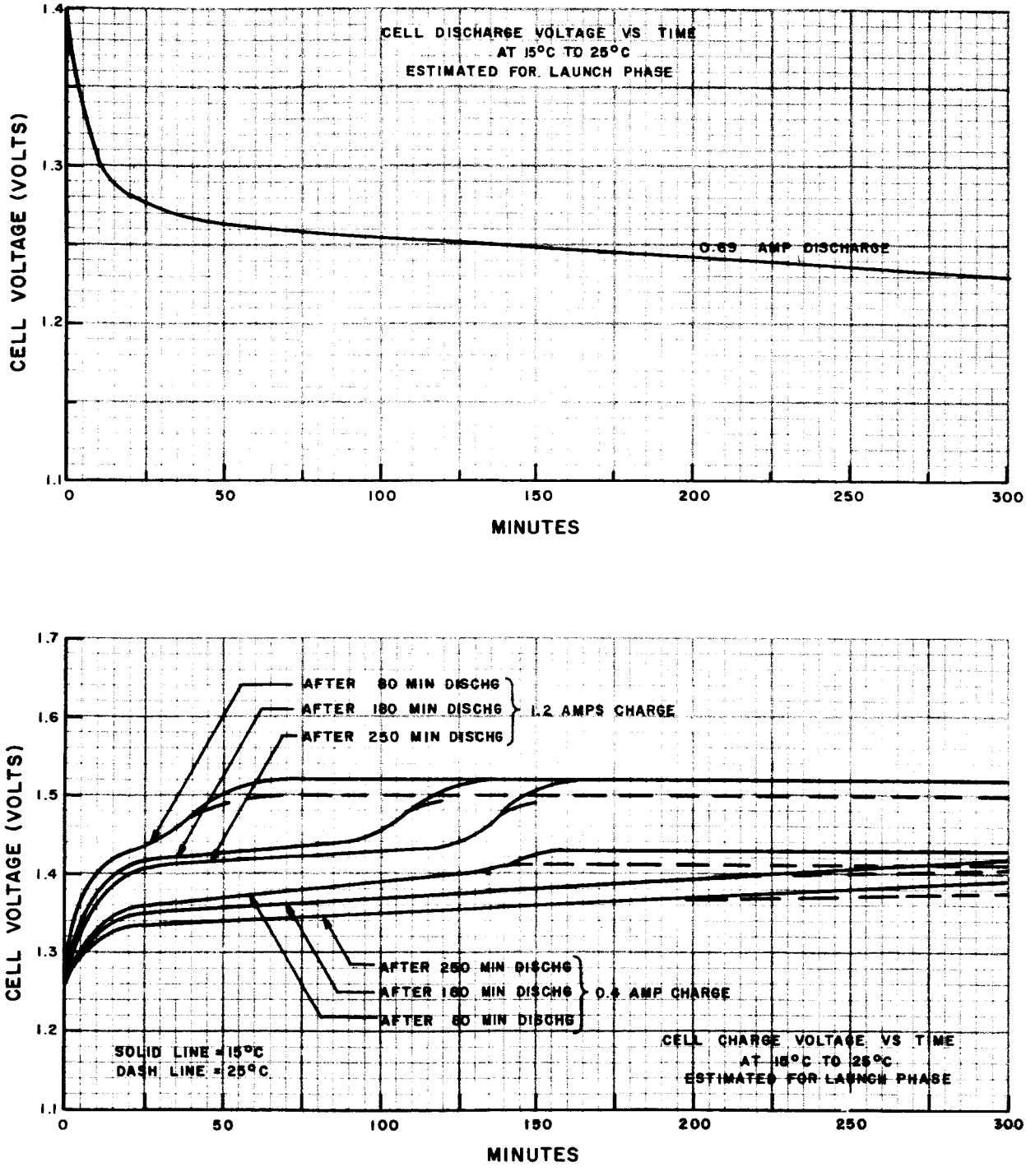


Figure 62. Cell Charge and Discharge Voltages Versus Time at 15 to 25°C, Launch-Phase Estimate

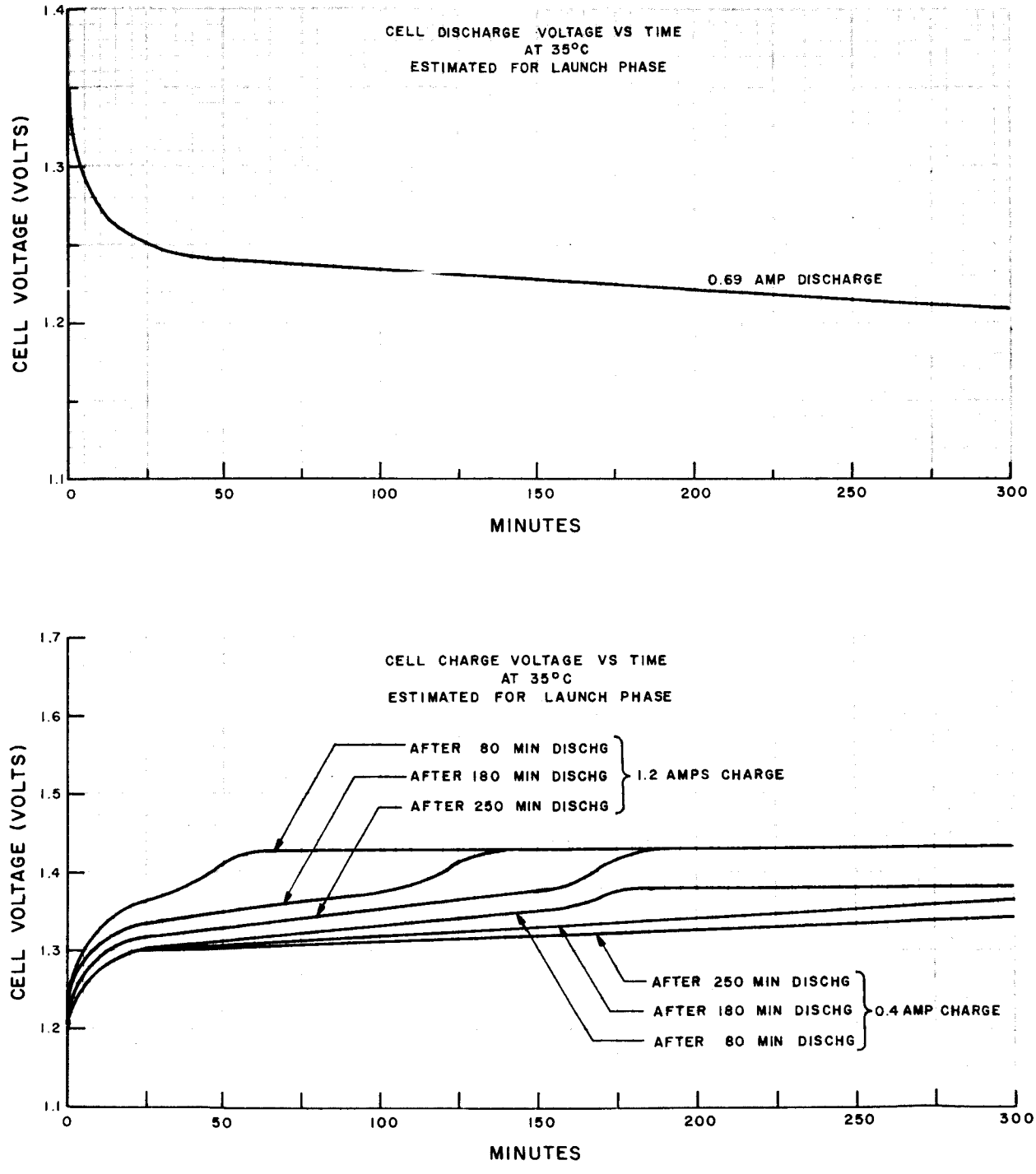


Figure 63. Cell Charge and Discharge Voltages Versus Time at 35°C, Launch-Phase Estimate

A prototype F-3 Nimbus battery module was used for this special test. The cell wiring and the connectors of this module are similar to those planned for the Nimbus-B battery module. The storage cells in this test module were 4.0 ampere-hour Sonotone cells. The module was let-down and then charged for 6.0 hours at 0.8 ampere before being connected in the test circuit shown in Figure 64. The open-circuit battery voltage just prior to the start of the test measured 32.1 volts. The battery was subjected to a series of discharge tests. The disconnect fuses limited each discharge to less than 5 milliseconds. The disconnect fuses were made of 1/8-inch lengths of 0.006-inch Pyrofuse wire. During each discharge test, the battery voltage, load voltage, and discharge time were measured with a dual-trace Textronix oscilloscope. These and other results of each test are summarized in Table 10.

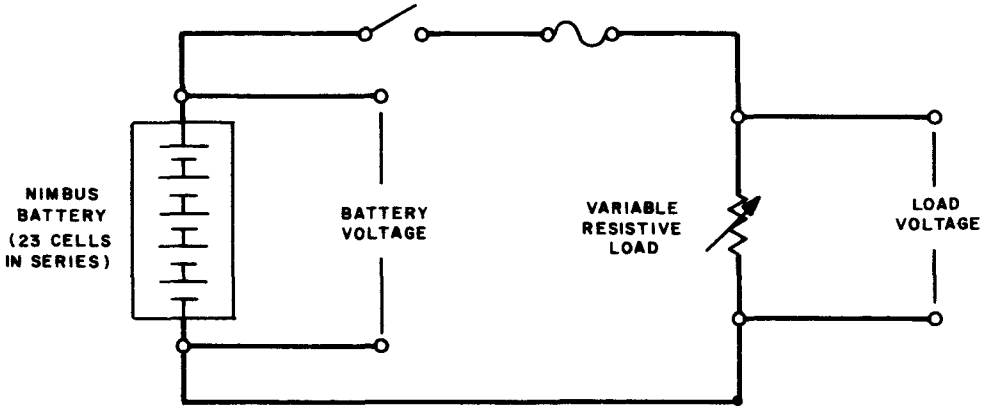


Figure 64. Battery Module Special Test Circuit

TABLE 10. SUMMARY OF BATTERY MODULE SPECIAL TEST RESULTS

Load Current (Amps)	Load Resistance (Ohms)	Fuse Resistance (Ohms)	Average Cell Voltage (Volts)	Discharge Time (Milliseconds)
35	0.638	0.012	1.00	4.5
40	0.540	0.010	0.98	4.2
43	0.490	0.010	0.93	3.5
55	0.330	0.013	0.83	2.0
56	0.288	0.013	0.76	1.6
59	0.236	0.012	0.70	1.3
54	0.186	0.013	0.55	1.1

F. BATTERY MODULE PACKAGING DESIGN

1. Mechanical Design

a. GENERAL

The new Nimbus-B battery module assembly consists of the original Nimbus battery module housing and corresponding related parts designed under contract NAS 5-943 as a contractual requirement. These parts are furnished (GFE by NASA) as salvaged from Nimbus-C battery module assemblies. A new, internal, electronic heat-sink assembly and module circuit-board assembly have been redesigned to meet new system requirements. Thermal protective finish, both internal and external, shall remain the same as that used on the original Nimbus program. In all instances of redesign, simplicity, and ease of fabrication and assembly have been improved over the original assembly.

The structural configuration, interface, and envelope limitations are shown in Figure 65. Figure 66 is the electronic circuit upon which the packaging concept is based.

b. BATTERY CELL

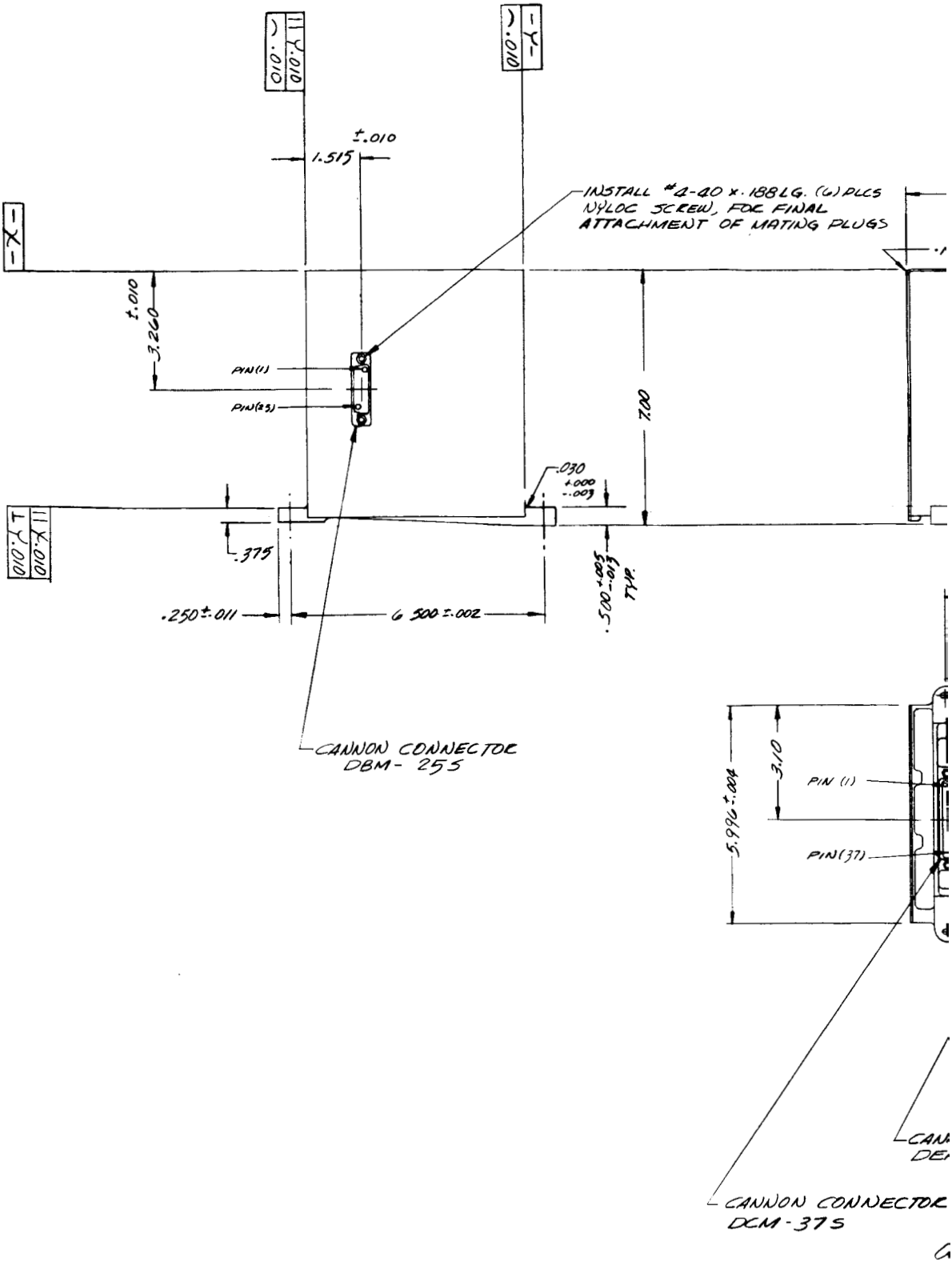
The battery cell design (Figure 67) is structurally superior to the previous battery cell. It consists of a 304-ST/STL can with a thicker bottom and an integral mount stud and inverted terminal head. It has successfully withstood pressure tests in excess of 2000 psi with no indication of leakage in the cell can or head.

c. ELECTRONIC BOARD ASSEMBLY

A single, double-sided (5.50" x 5.88") printed-circuit board is mounted to an adapter bracket which picks up existing mounting holes in the module side plate. The single module board simplifies the board assembly over the previous five boards used in the Nimbus module. The adapter mount requires the riveting of spacers to modify the side plate. The spacers and adapter mount further stiffen the relatively "soft" side plate.

d. ELECTRONIC HEAT-SINK ASSEMBLY

A single heat-sink assembly replaces the three pieces previously used. Because of the increased power dissipation requirements for the Nimbus B subsystem and the internal rearrangement of the circuit board and harness assembly, a new heat-sink bracket was designed, using existing mounting holes in the front face of the battery module. The completed assembly is shown in Figure 68.


-X-
-Y-
.010 Ⓜ X Y
.010 Ⓜ X Y
±.010
1.515
INSTALL #4-40 x .188 LG. (6) PLCS NYLOC SCREW, FOR FINAL ATTACHMENT OF MATING PLUGS
±.010
3.260
PIN(1)
PIN(63)
7.00
.030 +.000 -.003
.375
.250±.011
6.300±.002
.500 +.005 -.013 TYP.
CANNON CONNECTOR DBM-25S
5.990±.004
3.10
PIN (1)
PIN(37)
CANNON CONNECTOR DCM-37S

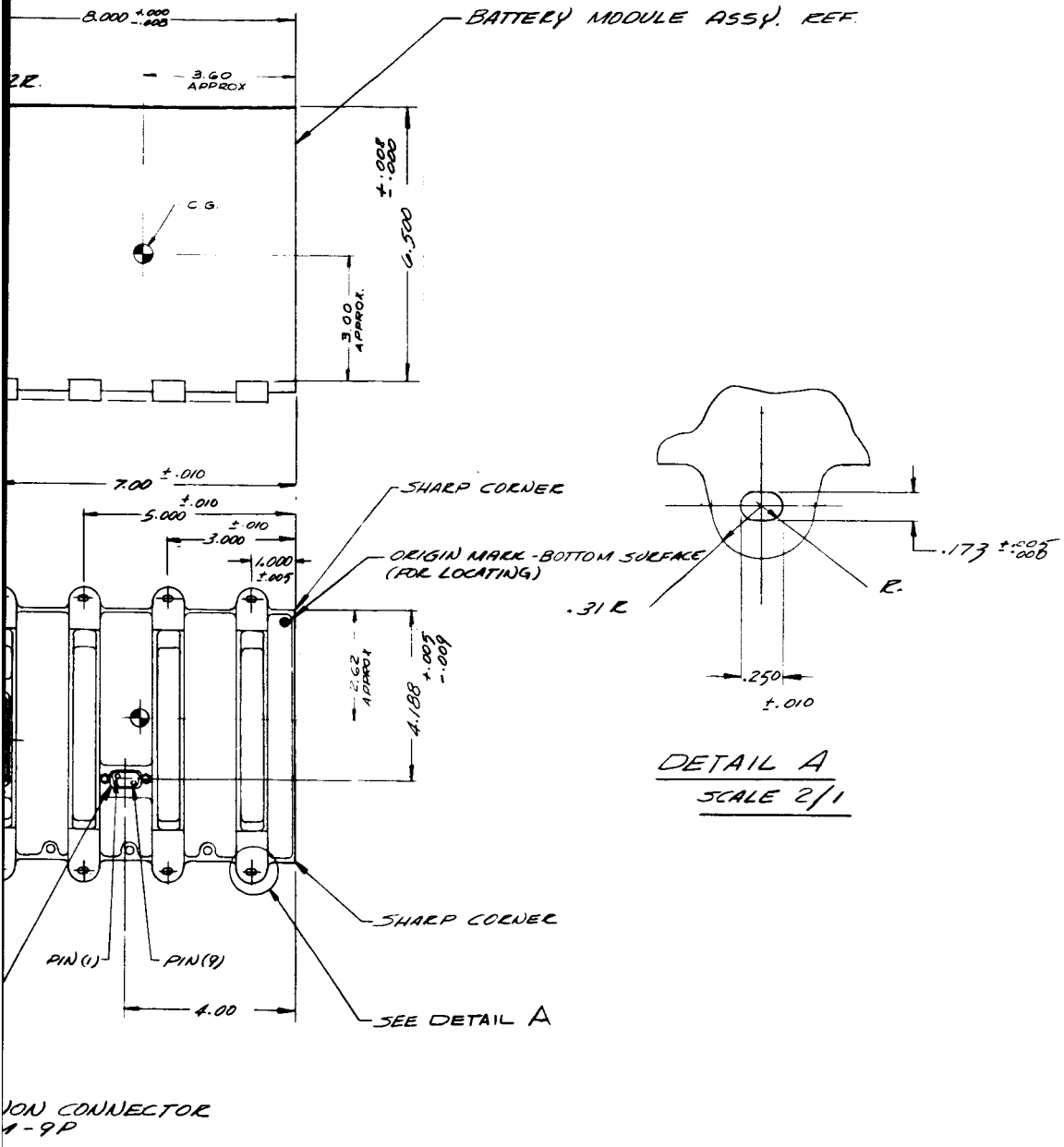
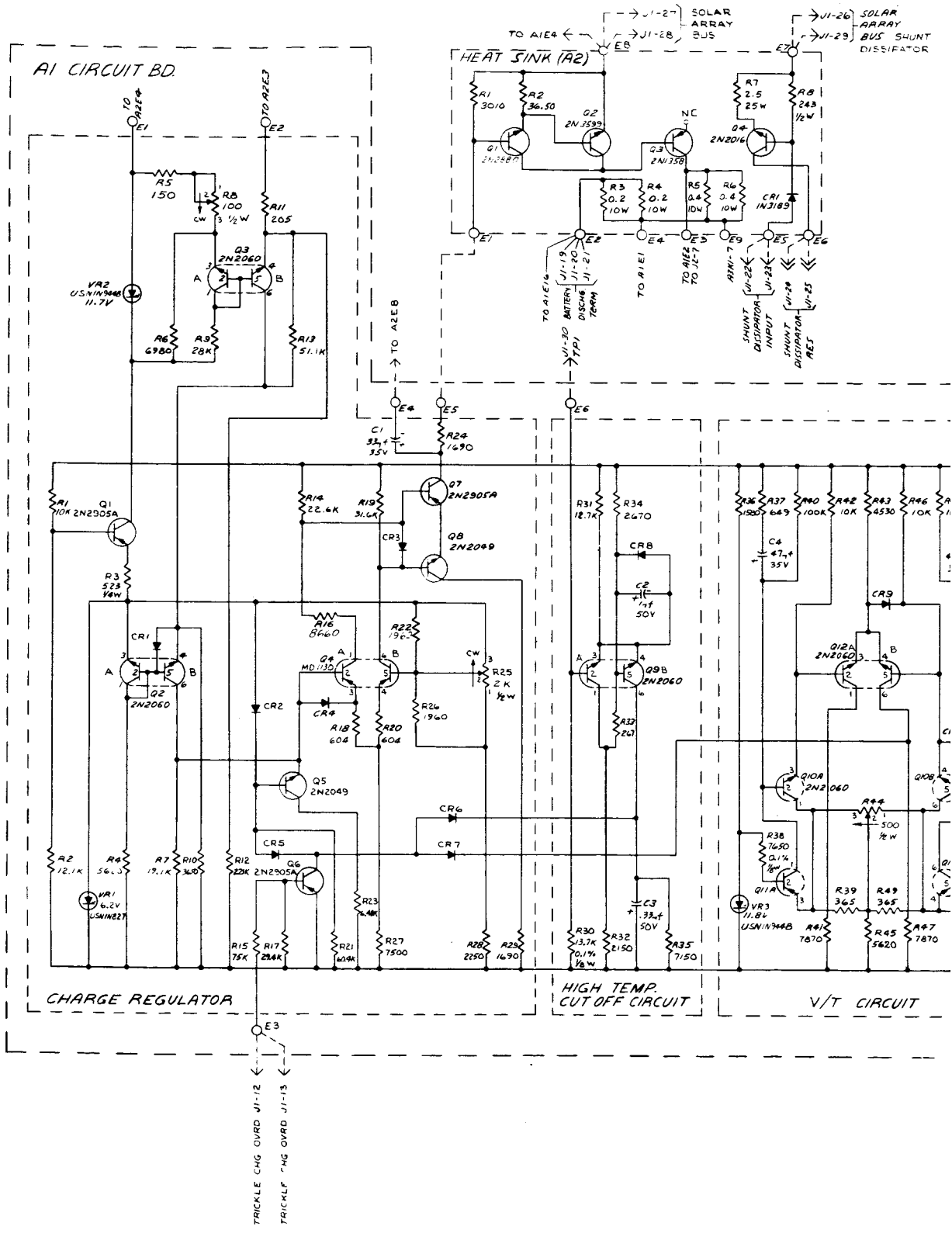


Figure 65. Nimbus-B Battery Module Structural and Interface Drawing (RCA Dwg. No. 1849618)


A1 CIRCUIT BD.
HEAT SINK (A2)
CHARGE REGULATOR
HIGH TEMP. CUT OFF CIRCUIT
V/T CIRCUIT
SOLAR ARRAY BUS
SOLAR ARRAY BUS SHUNT DISSIPATOR
TO A1E4
TO A2E3
TO A2E4
TO A2E8
TO A1E6
TO A1E1
TO A1E2
TO J2-7
TRICKLE CHG OVRD J1-12
TRICKLE CHG OVRD J1-13
Q1 2N2905A
Q2 2N2060
Q3 2N2060
Q4 MD1130
Q5 2N2049
Q6 2N2905A
Q7 2N2905A
Q8 2N2049
Q9B 2N2060
Q10A 2N2060
Q11A
Q12A 2N2060
VR1 6.2V USN1827
VR2 USN1944B 11.7V
VR3 11.8V USN1944B
CR1 IN3189
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, 1/8 WATT
2. ALL DIODES ARE JAN1N645

107

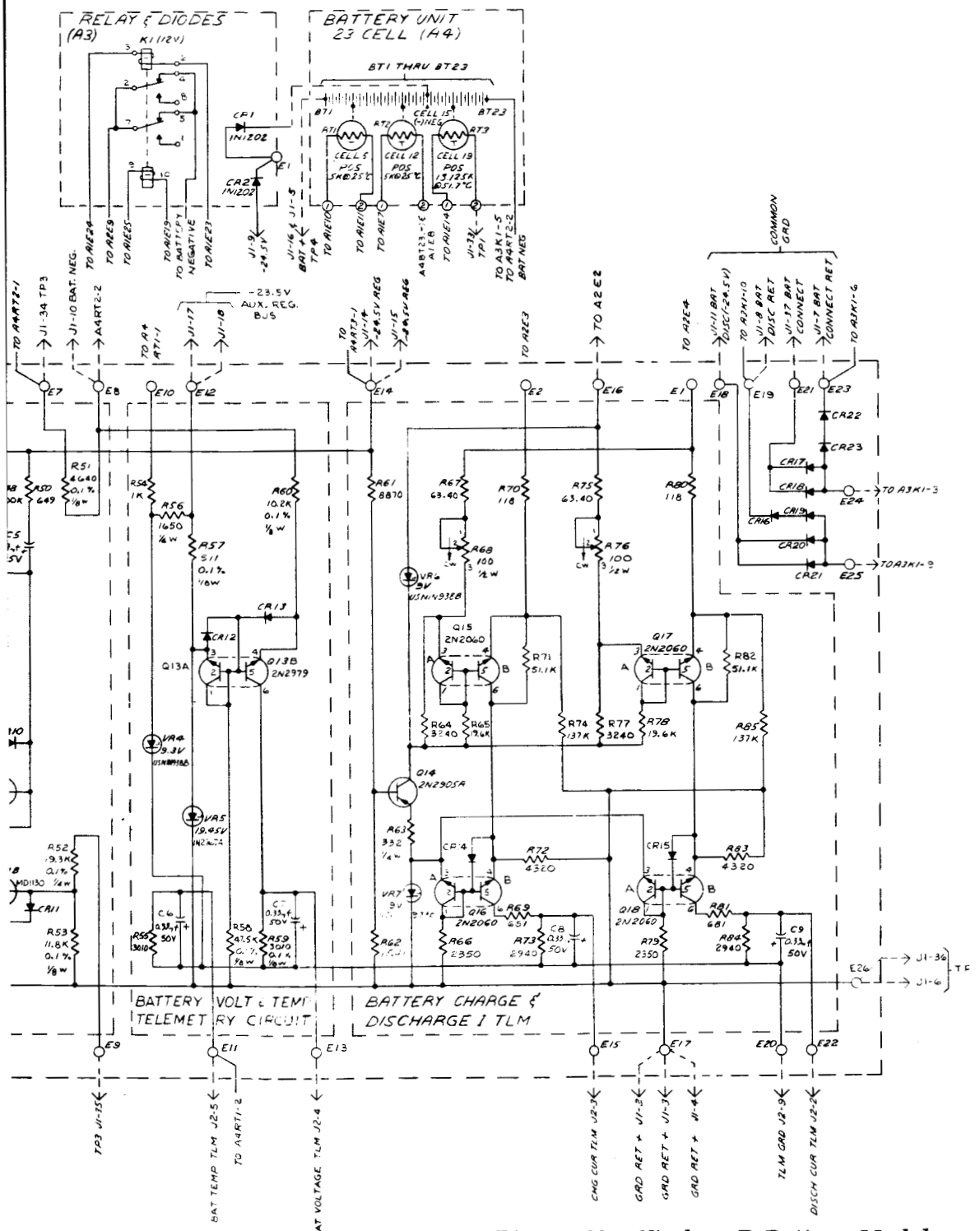
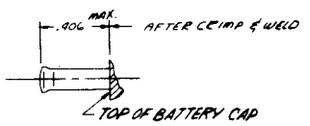
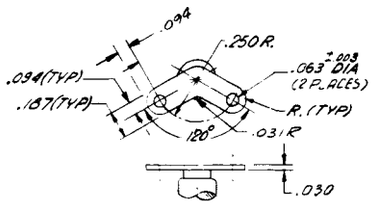


Figure 66. Nimbus-B Battery Module Schematic Diagram (RCA Dwg. No. 1759588)



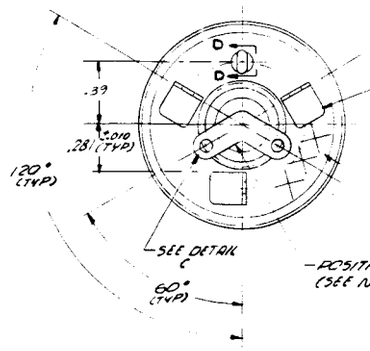
SECTION D-D

FILL TUBE DETAIL



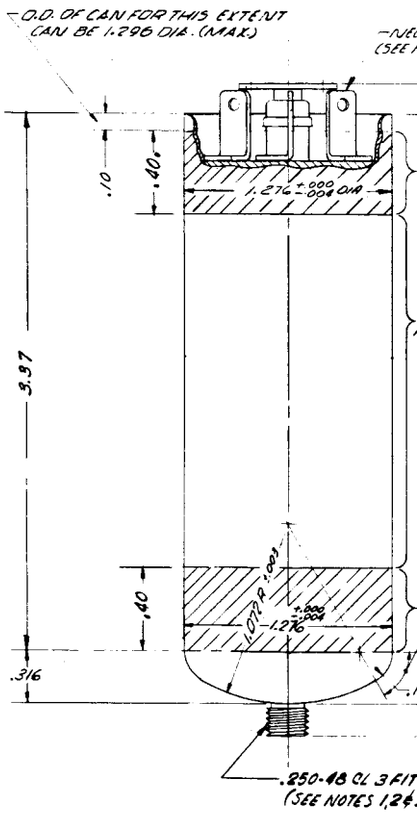
DETAIL C

POSITIVE TERM.



NOTES:

1. THE DIAMETER (1.276 +.000 -.004) OF THE UPPER AND LOWER SHADED AREAS OF BATTERY SURFACE MUST BE CONCENTRIC TO EACH OTHER AND WITH PITCH DIAMETER OF STUD THREAD WITHIN .006 T.I.R.
2. STUD MUST BE CAPABLE OF WITHSTANDING AN AXIAL TENSIONAL FORCE OF 225 LB WITHOUT PERMANENT DEFORMATION TO CAN.
3. STUD MUST BE CAPABLE OF WITHSTANDING 45 IN-LBS MIN TORQUE WITHOUT SEPARATION.
4. NEGATIVE TERMINALS MUST BE CAPABLE OF WITHSTANDING A PULL TEST ALONG THE AXIS OF THE CELL OF 75 LBS MIN. WITHOUT SEPARATION.
5. THE PLANE OF THE CIRCUMFERENTIAL WELD SHALL BE FLAT & PERPENDICULAR TO THE AXIS OF THE CELL WITHIN .010 THERE SHALL BE NO WELD WAVINESS OR SPIKES.
6. BRAZING ALLOY OF SEAL MUST BE SUITABLE FOR USE IN SPACE ENVIRONMENT AND MUST BE APPROVED BY R.C.A.
7. CELL MUST MEET ALL ELECTRICAL & ENVIRONMENTAL CHARACTERISTICS AS OUTLINED IN RCA SPEC. 1750976
8. THE TOP & SIDE SURFACES OF THE WELD AREA AT THE TOP OF THE CELL SHALL NOT BE FILED OR MACHINED.
9. ALL WELDED JOINTS TO BE HOMOGENEOUS, THERE ARE TO BE NO VOIDS.
10. SERIAL NO. TO BE MACHINE ETCHED IN AREA SHOWN APPROX. .13 HIGH.
11. FOR VIBRATION USE FIXTURE 1704132-501 AND LOCKNUT 1174496-2. TORQUE THE LOCKNUT TO 12±1 IN-LBS TO SECURE CELL IN FIXTURE. DO NOT VIBRATE UNLESS ALL CAVITIES IN FIXTURE CONTAIN A CELL.
12. CELL LEAKAGE NOT TO EXCEED 9.5×10^{-7} STD. ATM. CC/SEC HELIUM AS DETERMINED BY MASS SPECTROMETER.
13. ALLOWABLE DEPTH OF SURFACE DEFECTS SUCH AS NICKS, DENTS, SCRATCHES, PITTING ROUGH SPOTS OR TOOL MARKS MUST BE WITHIN .0001 MAX. AT CORNER RADIUS AREA SHOWN AND WITHIN .0003 MAX. IN ALL REMAINING AREAS.
14. POSITIVE AND NEGATIVE TERMINALS SHALL BE TINNED WITH RCA 2010807-304, QQ-S-571, 40/60 SOLDER. THE RESULTING TERMINAL LUG CONDITION MUST BE SOLDERABLE PER RCA SPEC. 8030020 PARAGRAPH 3.2.8.2.1
15. ALL WORKMANSHIP MUST COMPLY WITH RCA SPEC. 8030020



SPECIAL THREA
MAJOR DIA.
MAJOR DIA.
MINOR DIA.
PITCH DIA.
PITCH DIA.

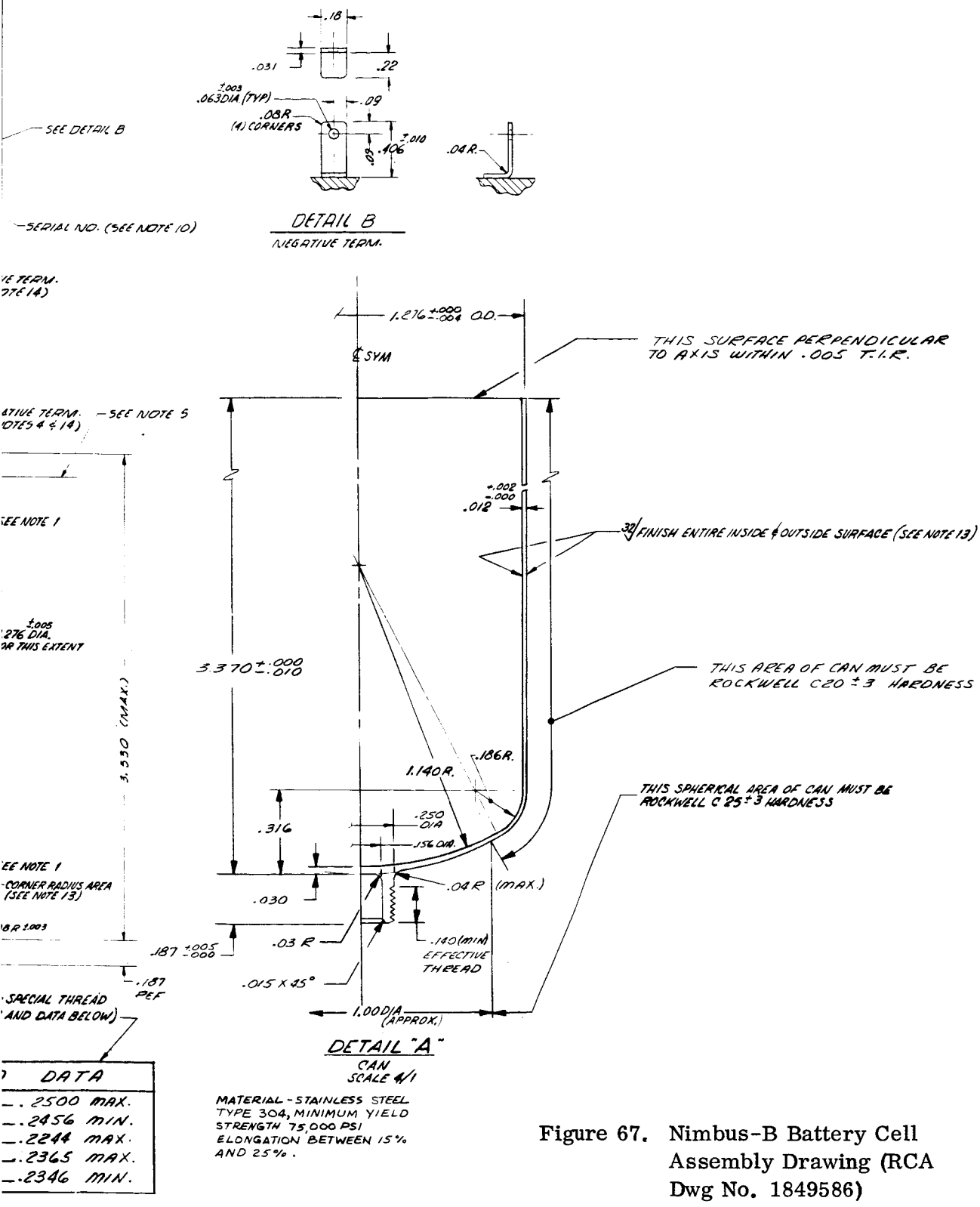
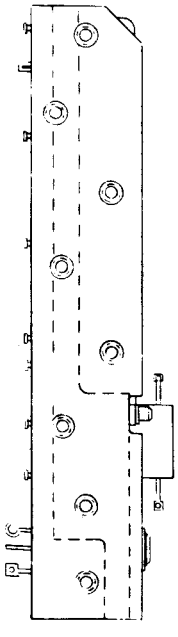
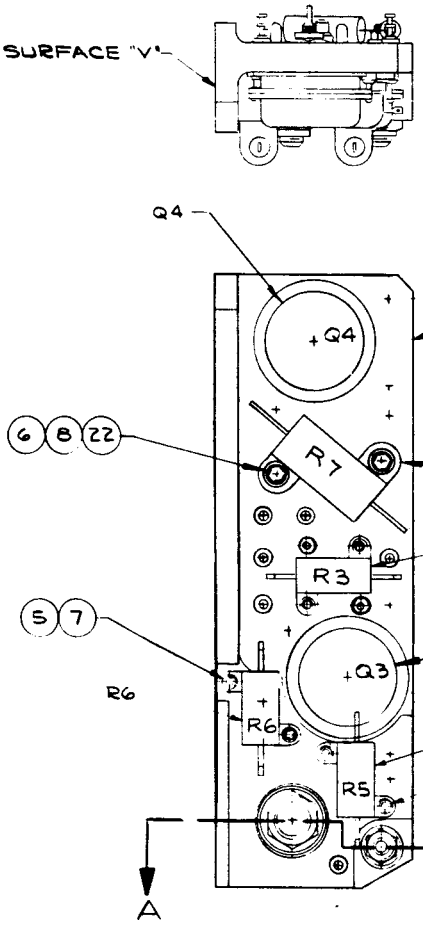
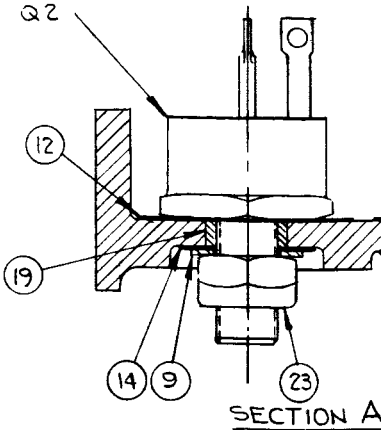


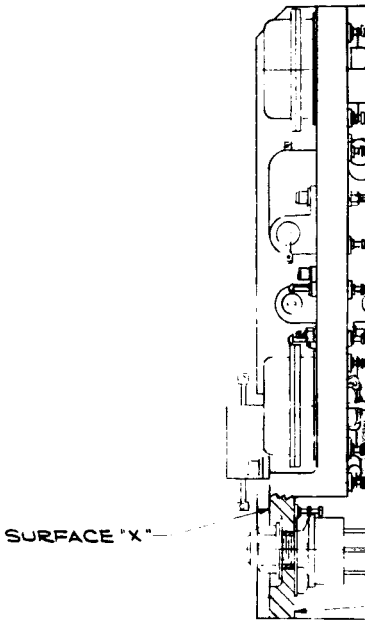
Figure 67. Nimbus-B Battery Cell Assembly Drawing (RCA Dwg No. 1849586)







SECTION A
SCALE 2



NOTES:

1- ALL FASTENING HARDWARE TO BE TORQUED PER. SPECIFICATION (ITEM 25).

2- BEFORE ASSEMBLING HEAT SINK APPLY A THIN COATING OF APIEZON GREASE (ITEM 27) TO THE FOLLOWING AREAS:

(A) TO UNDERSIDE (MOUNTING AREA) OF ALL TRANSISTORS.
(B) TO BOTH SIDES OF ALL MICA WASHERS.
(C) TO ALL AREAS OF HEAT SINK WHICH COME IN CONTACT WITH MICA PARTS OR RESISTORS AS APPLICABLE APPLY GREASE SO AS TO COMPLETELY COVER MOUNTING SURFACE ALLOWING NO ACCUMULATION. ALL EXCESS MUST BE REMOVED IMMEDIATELY AFTER ASSEMBLY

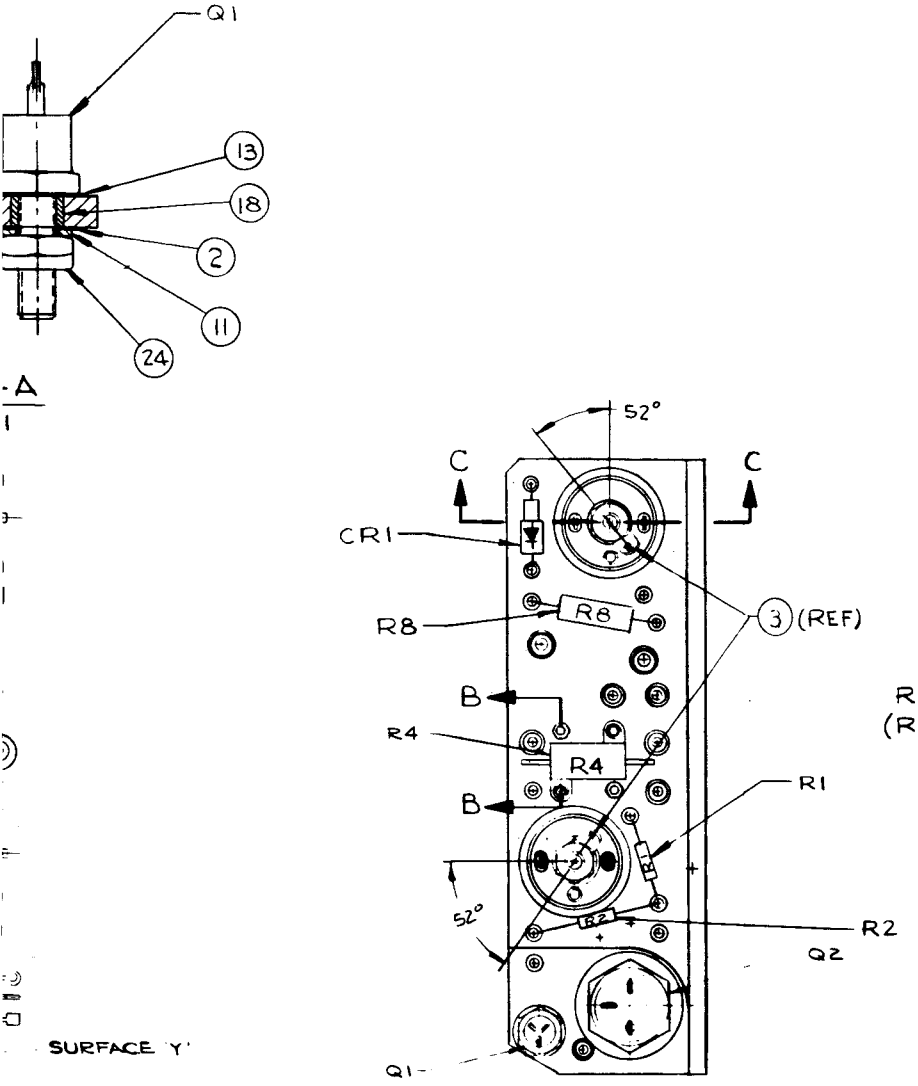


Figure 68. Nimbus-B Heat Sink Assembly Drawing (RCA Dwg No. 1849596)

e. RELAY AND HARNESS BRACKET ASSEMBLY

A ribbed-zee section bracket replaces the ell-shaped resistor mount bracket used in the original Nimbus battery module. The bracket is designed to accommodate mounting the relay, two diodes, and the harness trunk, and is not required for heat-sink purposes as in the previous design.

f. NIMBUS B BATTERY MODULE WEIGHT CONTROL

The total estimated weight of the module assembly is tabulated below; wherever possible, actual weights are listed.

Housing Assembly & Related Parts	—	2.5
Battery Cells (23)	—	10.2
Heat-Sink Assembly	—	0.9
Circuit-Board Assembly	—	0.7
Main Harness Assembly and Potting	—	0.7
Relay and Harness Bracket Assembly	—	0.5
Diodes* (for fuze protection)	—	0.2
Total Weight Estimate:		15.7 lbs

g. STRUCTURAL AND DYNAMIC ANALYSES

A review of the Nimbus-B subsystem environmental specification shows an increase of sinusoidal vibration load levels from 10g to 15g in the thrust-axis direction in the 5 to 200 cps frequency range. Loads in the other axes remain the same in accordance with the requirements of the original Nimbus contract, NAS 5-943. The increased thrust load, coupled with available transmissibility vibration data, required re-analysis of critical stress regions of the module housing. Redesign of internal structural elements also require a reassessment of the structural adequacy of the contractually required module housing. Included in the analytical study are the following areas:

(1) Bottom ribbed plate of the module housing,

(2) Egg-crate mounting of the battery cells,

(3) New module board assembly and mount bracket,

---

* Additional estimated weight of diode circuitry for fuze-protection circuit by NASA direction.

(4) Side plate,

(5) New heat-sink analysis, and

(6) Battery cell initial torque requirements.

Structural analysis to date consists of a review of the critical stress regions of the battery module housing. Re-analysis to date has shown the existing housing design to be satisfactory for the Nimbus-B program. Analysis of the heat sink and module board is complete and shows no critical stress areas. A final structural analysis report on the Nimbus-B battery module is in process.

G. THERMAL ANALYSIS

1. General

The results of a detailed thermal analysis of the Nimbus-B battery module are described herein. The same techniques that were employed in the Nimbus-A battery module thermal design were also used in this analysis. These techniques are described fully in Reference 1, and, therefore, will not be repeated in this report.

2. Module Design and Conditions

The battery module housing was specified by NASA to be the same as previously used on Nimbus A. Therefore, the wall thickness of the module was fixed.

The major heat dissipators (transistors and resistors) were mounted on a thick bracket which, in turn, was mounted directly to the front surface of the module. Grease is used to reduce the contact resistance between the bracket and front surface of the module. Mica (0.003-inch thick) and grease is used between all power transistors and metal-mounting surfaces. The mica is used to electrically insulate the transistor, while the grease reduces the contact resistance at the interfaces. Figure 69 shows the value of the major heat dissipators used in this analysis.

The entire inside of the module will be finished with a coating(s) that has a high I.R. emissivity in order to reduce temperature gradients within the modules. This coating should cover all components. The modules will be delivered to the integrator without the application of white paint on the external side of the front and bottom surfaces. This will preclude any surface damage during the integration phase. However, in this analysis, it has been assumed that the bottom surface of the module has white paint on it with a solar absorptance (a) of 0.25 and a I.R. emittance (ϵ) of 0.87.

Reference 1 - Battery Module and Components for Power Supply Subsystem, ESAR 86535-001 Volume 1, March 1963.

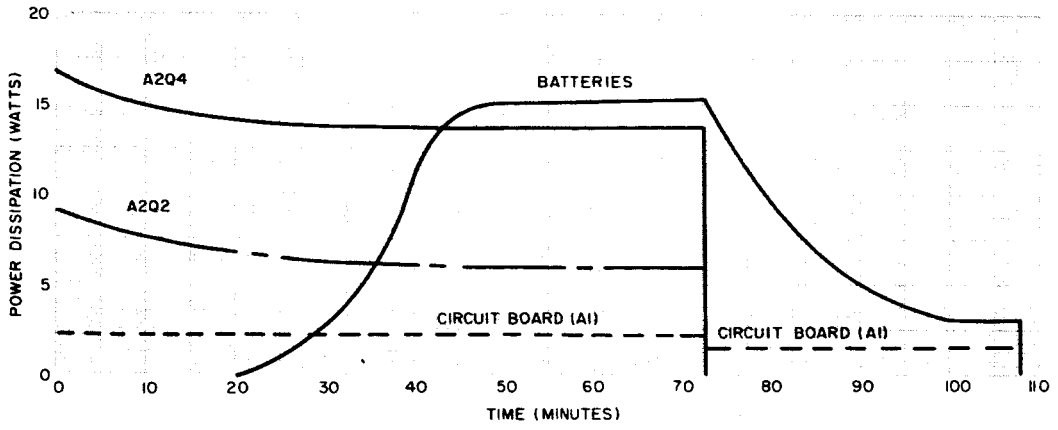


Figure 69. Major Component Heat Dissipation Versus Time, Battery Module Thermal Analysis

The design conditions used in this analysis are as follows:

(1) The battery module will be mounted to a heat sink which will be 55°C maximum and -5°C minimum;

(2) The entire front face of the module is in contact with this heat sink. Ecco-bond grease is used to reduce the contact resistance between these surfaces;

(3) The bottom face of the battery module will be open to space, and will radiate to an orbit average equivalent radiation sink of 235°K (orbit parameters are 612 nautical miles altitude, high noon, earth oriented, and sun-synchronous); and

(4) The heat dissipation in the module was computed on the basis of 475 watts being delivered from the solar-cell paddles at a maximum of 40 volts. The RTG will deliver 50 watts of power continuously, and the spacecraft will have a required minimum load of 120 watts. This represents the worse-case, total heat dissipation that can practically occur within the module.

3. Analysis and Results

For the purpose of analysis, the battery module was divided into 30 nodes, each of which is considered to be isothermal (see Figure 70). All areas of significant heat dissipation were considered as separate nodes, while the remainder of the module

was subdivided for ease of analysis. The equation used to predict the temperature of each node is as follows:

$$m_i c_i \frac{dT_i}{d\theta} = \sum_{j=1}^{n} R_{ij} (\sigma T_j^4 - \sigma T_i^4) + \sum_{j=1}^{n} K_{ij} (T_j - T_i)$$

$$+ Q_i \langle\theta\rangle + \overline{I_i} A_i \qquad (1)$$

$$- \epsilon_i A_i T_i^4$$

where:

m_i = mass of body "i"

c_i = specific heat of body "i"

T_i = temperature of body "i"

θ = time

R_{ij} = radiative coupling factor between body "i" and body "j"

K_{ij} = heat dissipation at time θ in body "i"

$\bar{I}_i$ = orbit average external input on body "i"

Equation (1) was solved on the RCA 601 Computer, and the temperature versus time for each of the 30 nodes was obtained. The results indicated that there are no temperature problems associated with the Nimbus-B battery module, even with the high dissipation used (ref. Figure 69).

Figure 71 is a plot of the results from the analysis for several of the more important nodes. Transistor A2Q4 is the hottest component in the module with a peak case temperature of 94°C. This transistor is mounted on the heat-sink bracket, and the junction-to-case temperature gradient is 18°C. Therefore, the junction temperature of A2Q4 is 112°C. Transistor A2Q2 is also on the heat-sink bracket and has a peak case temperature of 70°C, and a junction-to-case gradient of 8°C. Therefore, A2Q2's junction is 87°C. These junction temperatures are well below the desired value of 130°C.

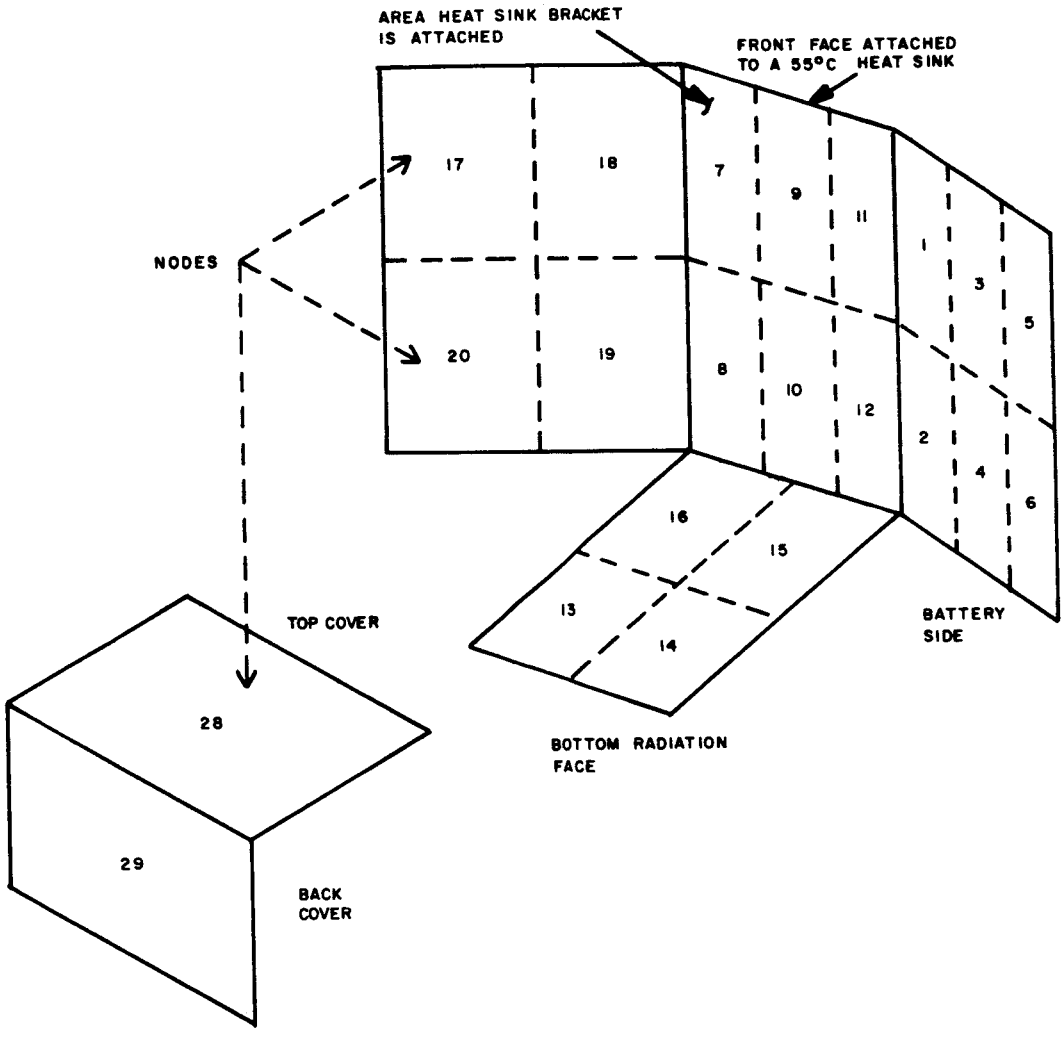


Figure 70. Identification of Nodes Used in Battery Module Thermal Analysis

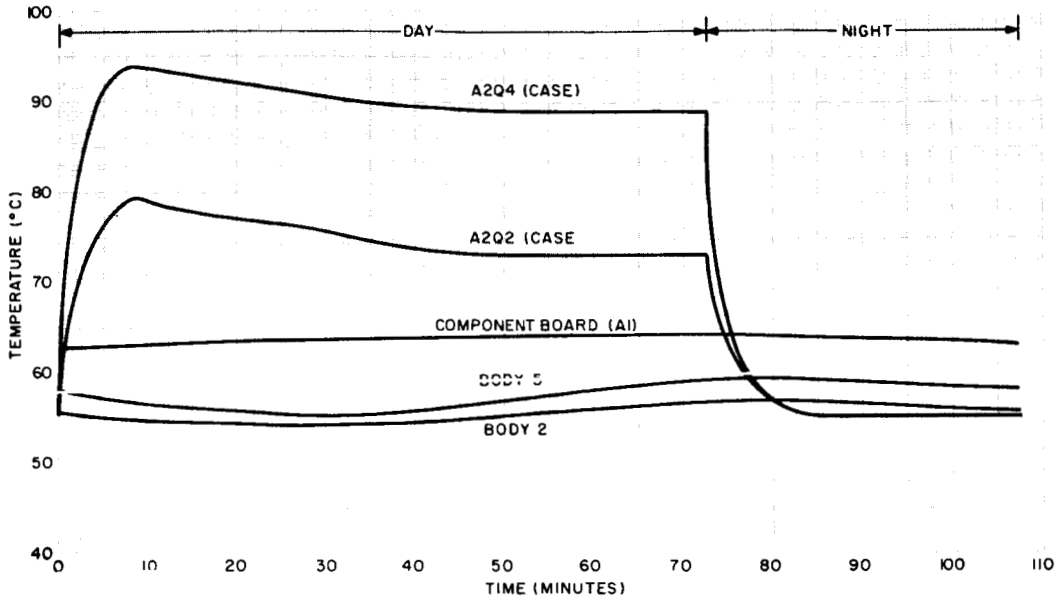


Figure 71. Temperature Versus Time for Several Nodes in Battery Module Thermal Analysis

Body 2 and Body 5 in Figure 71 represent the coolest and hottest segments of the module wall to which the batteries are attached. As can be seen in Figure 47, the maximum gradient is 2.5°C. Past experience with the Nimbus-A battery module showed that the maximum gradient from the battery cell case to the module skin was 1°C.

The temperature of the component board is also plotted in Figure 71. As can be seen, it does not vary very much in temperature over the orbit. An orbit average temperature of 63°C is obtained on the board, considering it as an isothermal body with the component heat dissipation spread evenly over the board. Some of the transistors on the board were analyzed separately based on the computer results and expected peak-power dissipation. These results are shown in Table 11 which lists all the transistors and some of the more important resistors in the module. Both the average dissipation and peak dissipation of these components are shown in Table 11, as well as the desired temperature and the calculated temperature.

4. Conclusion

Based on this thermal analysis, which utilized the worst-case environmental and worst-case power dissipation, no temperature problems are indicated. Therefore, no further analysis is necessary with respect to the existing module design. Later in the program, a thermal-vacuum test will be conducted. However, the power profile used in the test is expected to differ considerably from that used in this analysis, and therefore, the temperatures will be less than predicted in this report.

TABLE 11. CALCULATED COMPONENT DISSIPATION AND TEMPERATURE

Component	Dissipation (ma)		Temperature (°C)	
	Avg	Peak	Desired	Max Calculated
A1Q3-A (2N2060)	0.2	--	130°C Junction	Negligible
A1Q3-B (2N2060)	44	81	130°C "	82°C Junction
A1Q2-A (2N2060)	1	--	130°C "	Negligible
A1Q2-B (2N2060)	0.5	1	130°C "	"
A1Q4-A (MD1130)	3	--	130°C "	"
A1Q4-B (MD1130)	3	--	130°C "	"
A1Q6 (2N2905A)	0.55	--	130°C "	"
A1Q5 (2N2049)	0.5	1.25	130°C "	"
A1Q8 (2N2049)	13	130	130°C "	97°C Junction
A1Q7 (2N2905A)	13	130	130°C "	130°C Junction
A2Q1* (2N2880)	280	890	130°C "	76°C Junction
A2Q2* (2N3599)	8400	14400	130°C "	87°C Junction
A2Q3* (2N1358)	600		130°C "	68°C Junction
A1Q9 (2N2060)	--	--	130°C "	Negligible
A1Q12-A (2N2060)	10	--	130°C "	"
A1Q12-B (2N2060)	10	--	130°C "	"
A1Q10-A (2N2060)	5	--	130°C "	"
A1Q10-B (2N2060)	5	--	130°C "	"
A1Q11-A (MD1130)	0.5	--	130°C "	"
A1Q11-B (MD1130)	0.5	--	130°C "	"

TABLE 11. CALCULATED COMPONENT DISSIPATION AND TEMPERATURE (Continued)

Component	Dissipation (ma)		Temperature	
	Avg	Peak	Desired	Max Calculated
A1Q14 (2N2905A)	26	--	130°C Junction	Negligible
A1Q15-A (2N2060)	0.2	--	130°C "	"
A1Q15-B (2N2060)	60	120	130°C "	95°C Junction
A1Q17-A (2N2060)	0.2	--	130°C "	Negligible
A1Q17-B (2N2060)	60	120	130°C "	95°C Junction
A1Q16-A (2N2060)	1.5	--	130°C "	Negligible
A1Q16-B (2N2060)	6	6	130°C "	"
A1Q18-A (2N2060)	1.5	--	130°C "	"
A1Q18-B (2N2060)	6	6	130°C "	"
A2Q4* (2N2016)	1350	1750	130°C "	112°C Junction
A1Q1	30	--	130°C "	Negligible
A1Q13-A (2N2979)	--	--	130°C "	"
A1Q13-B (2N2979)	--	--	130°C "	"
A2R3-A*	300	--	150°C	72°C Case
A2R4-B*	300	--	150°C	72°C Case
A2R5-A*	150	--	150°C	73°C Case
A2R6-B*	150	--	150°C	68°C Case
A2R7*	750	1000	150°C	76°C Case

All remaining resistors, capacitors, diodes, and zeners are located on the component board and will be at the average board temperature, since they dissipate only a very small amount of heat.

*Mounted to "heat sink" bracket.

SECTION IV

BATTERY CONTROL AND PROTECTION CIRCUITS

A. GENERAL

A functional block diagram of the Nimbus-B battery module electronics is shown in Figure 72. The battery electronics was discussed on a block-diagram functional level in Quarterly Technical Report No. 1. This quarterly report discusses the operation of the battery electronics on a circuit level.

The major change that was made in the battery module electronics during this quarter was the elimination of the shunt-loss reducer circuit, which was discussed in the previous quarterly report. The successful operation of this circuit was based on the assumption that the solar-array voltage would decrease to zero during night. Since that time, some doubt has been raised as to the validity of this assumption.

B. CURRENT REGULATOR

Figure 73 is a schematic diagram of the current regulator. Transistor Q4, a dual PNP transistor, forms a differential amplifier which compares the reference voltage developed from zener diode V_{R1} with the voltage output from a current-to-voltage transducer. The operation of the current-to-voltage transducer (Q1, Q2, Q3, and associated components) is identical with that of the battery-charge and battery-discharge telemetry circuits. Refer to Paragraph F of this section for its theory of operation.

Transistor Q5 serves to modify the current-to-voltage transducer ratio when signal inputs are present from either the battery voltage-temperature circuit or high-temperature cutoff circuit. Transistor Q5 is operated at current saturation when no inputs are present. Injection of a signal current into the base circuit of Q5 modifies the effective load resistance of the current-to-voltage transducer, thereby directly changing its transformation ratio. Diode CR3 prevents excessive reverse biasing of the base-emitter junction of Q5.

Transistor Q4 and its associated components provide trickle-charge-override capability for the current regulator. Upon application of a minus 23.5-volt signal via ground command, transistor Q4 is driven into saturation, inhibiting any signal from the battery voltage-temperature circuit and high-temperature cutoff circuit. This prevents both circuits from placing the current regulator into a trickle-charge mode.

Relay K1 is incorporated in series with each battery so that any battery can be disconnected from the circuit via ground command.

C. BATTERY VOLTAGE-TEMPERATURE REGULATION

Figure 74 is a schematic diagram of the battery voltage-temperature circuit. The circuit consists of a differential amplifier whose inputs are: (1) a reference voltage provided by a temperature-compensated zener diode VR_1, and (2) a voltage proportional to the battery voltage and temperature derived from the R14, R15, R16, and R(T) voltage divider.

The output of the amplifier is a current proportional to the difference between the two input voltages.

Minimum drift is achieved by the use of the temperature-compensated zener diode (VR_1), dual-packaged transistors Q1, Q2, and Q3, high-stability resistors in the sensing arms, and the symmetrical arrangement used throughout, up to and including the output stage. Resistor R1 also aids in drift stabilization by matching the source impedances of the reference voltage and the signal.

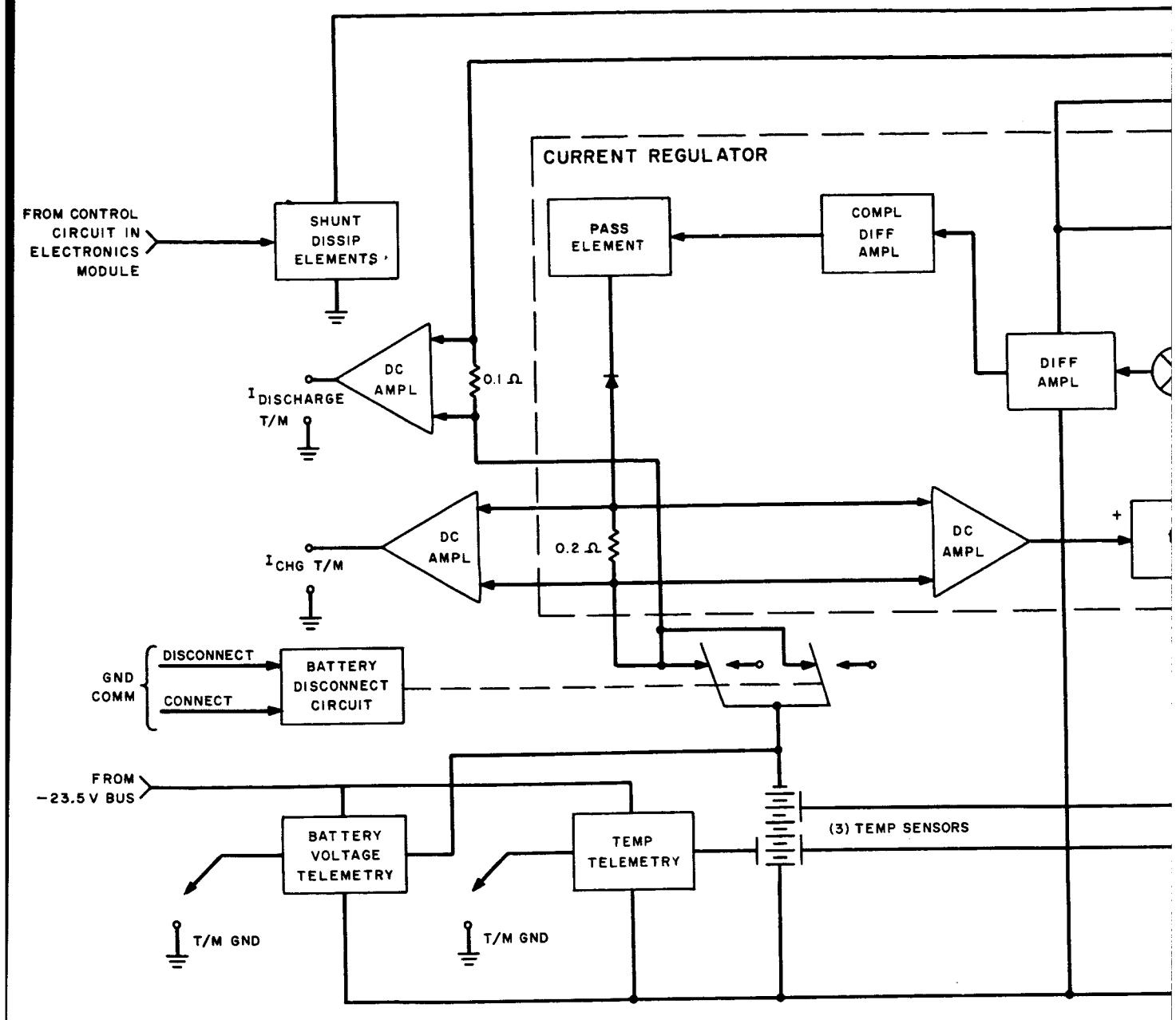
An adjustment is provided by resistor R8 to allow for initial inaccuracies due to the zener diode and resistor initial tolerances to be compensated.

Protection of the transistors against excessive reverse bias of the base-emitter junctions of Q1-A, Q2-A, and Q3-A is provided by dioses CR1, CR2, and CR3.

D. HIGH-TEMPERATURE CUTOFF CIRCUIT

Figure 75 is a schematic diagram of the high-temperature cutoff circuit.

The battery temperature is sensed by the thermistor R(T) which is mounted on battery cell No. 19. The trip level (V_T) of the Schmitt-Trigger circuit is reached at the specified battery high temperature ($51.7 \pm 2.8°C$) due to the negative temperature coefficient of the thermistor. At the trip level, the Schmitt Trigger delivers a step current to the current regulator which causes the battery current (I_B) to be reduced to the trickle-charge level. As the battery temperature decreases, V_T will decrease by an amount equal to the hysteresis of the Schmitt-Trigger. Upon reaching the lower trip level, the Schmitt-Trigger circuit will change state and allow the current regulator to charge the battery at the normal rate.


CURRENT REGULATOR
FROM CONTROL CIRCUIT IN ELECTRONICS MODULE
SHUNT DISSIP ELEMENTS
PASS ELEMENT
COMPL DIFF AMPL
DIFF AMPL
DC AMPL
0.1 Ω
I DISCHARGE T/M
DC AMPL
0.2 Ω
DC AMPL
I CHG T/M
GND COMM
DISCONNECT
CONNECT
BATTERY DISCONNECT CIRCUIT
FROM −23.5 V BUS
BATTERY VOLTAGE TELEMETRY
TEMP TELEMETRY
(3) TEMP SENSORS
T/M GND
T/M GND

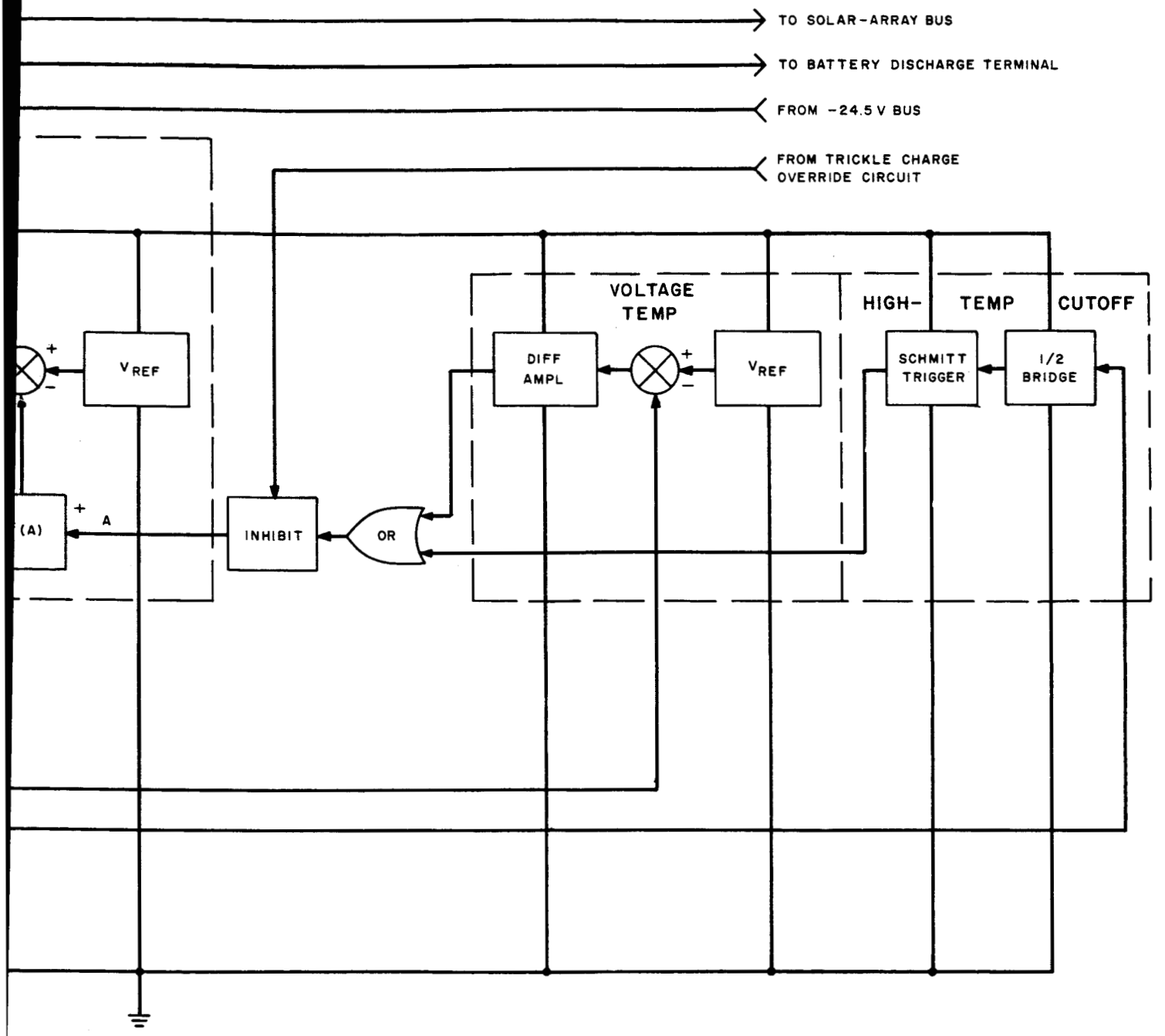


Figure 72. Nimbus-B Battery Module Electronics, Functional Block Diagram

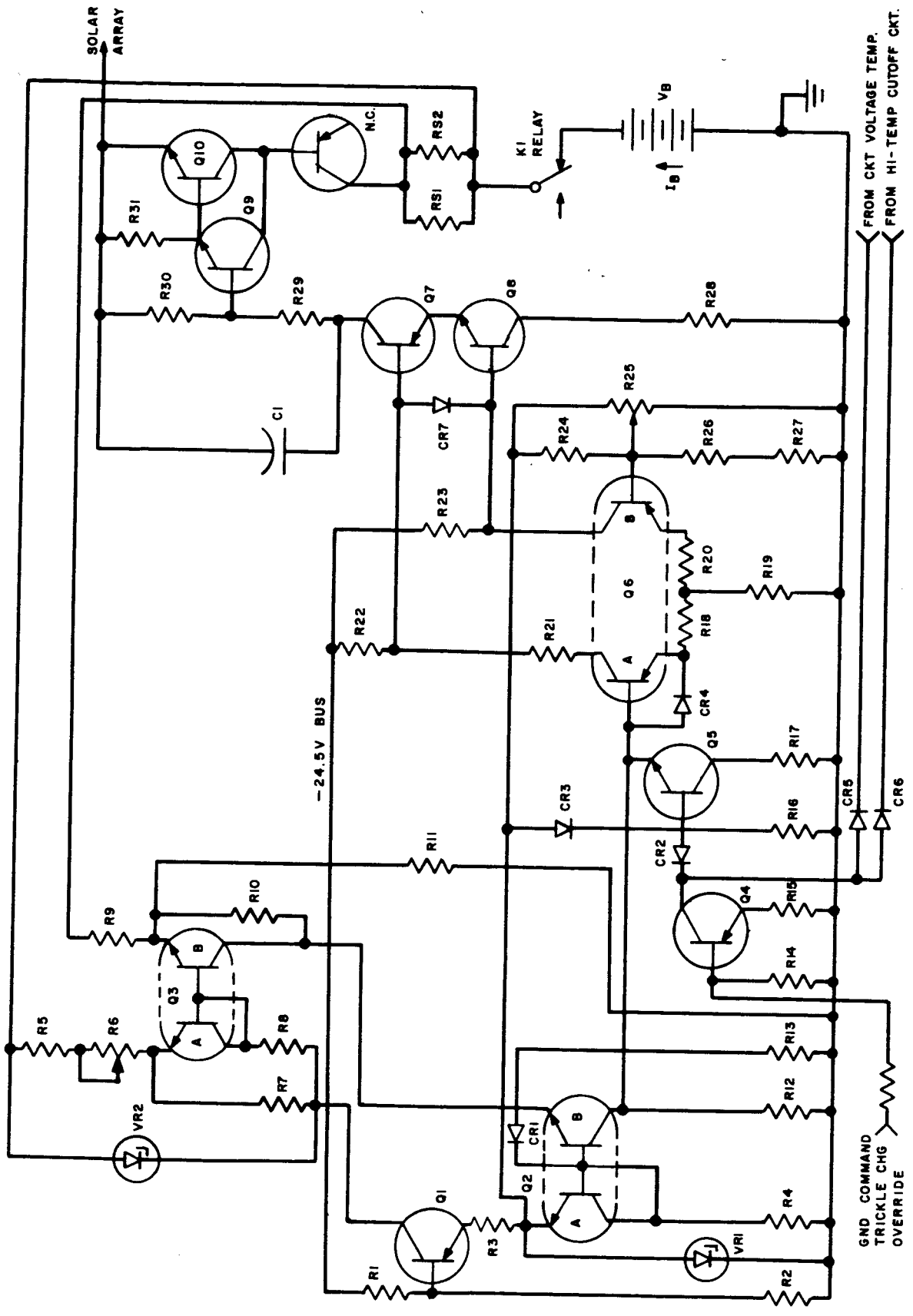


Figure 73. Current Regulator Schematic Diagram

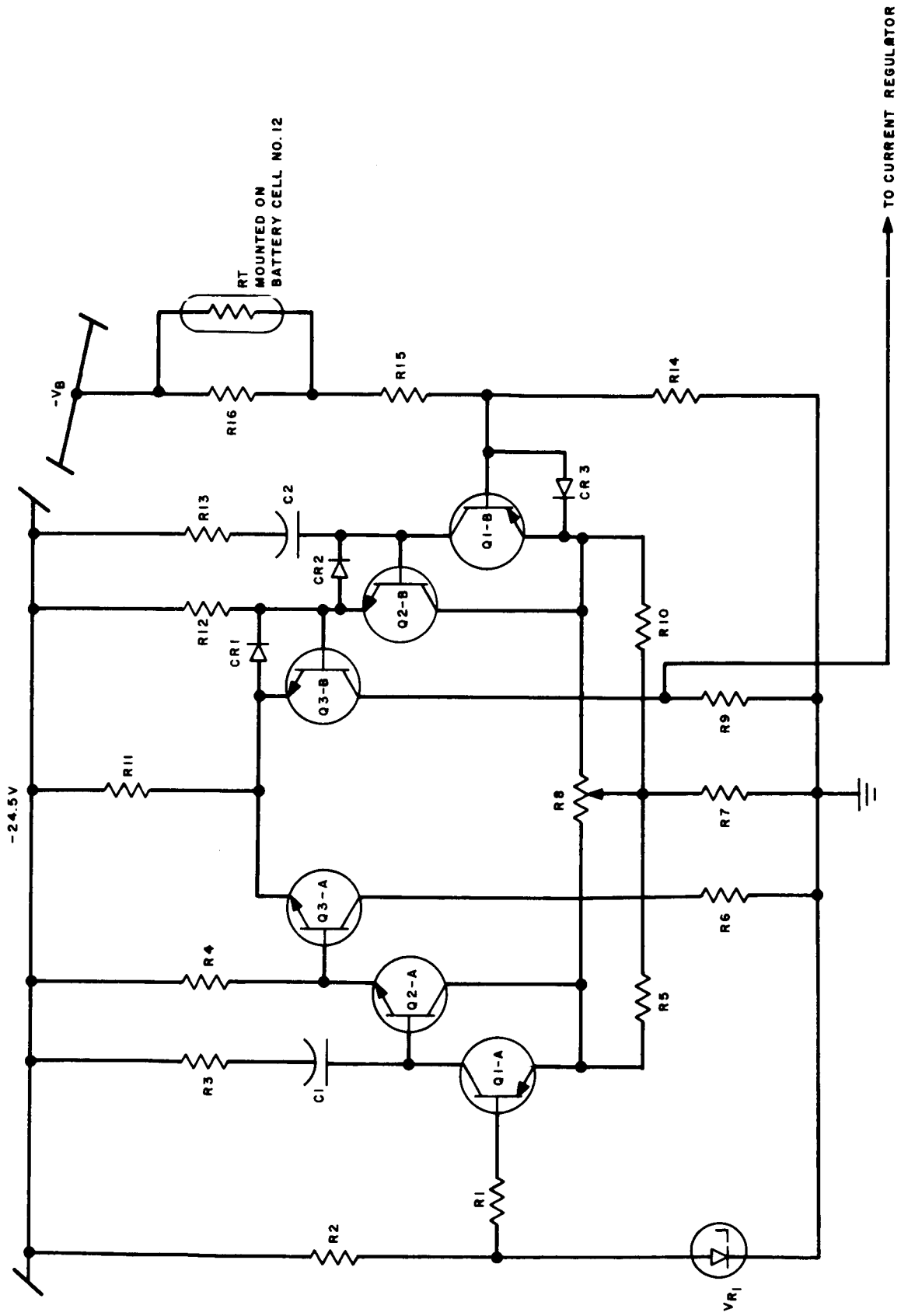


Figure 74. Battery Voltage-Temperature Regulation Circuit, Schematic Diagram

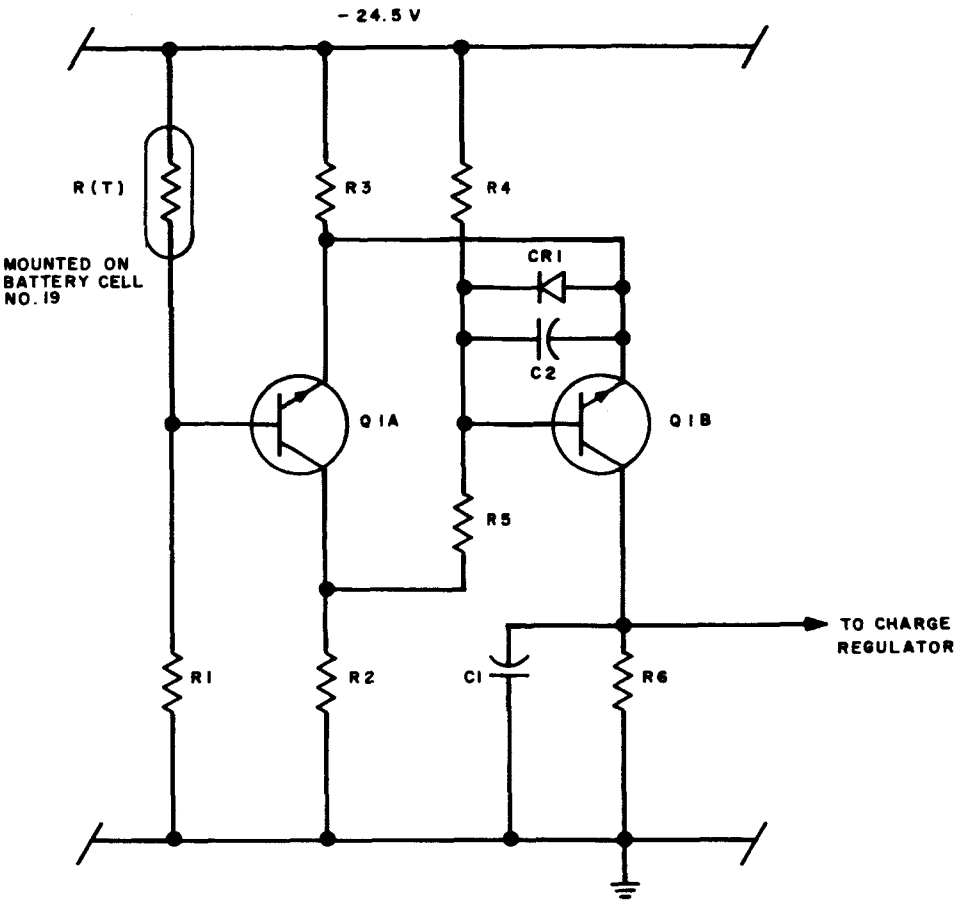


Figure 75. High-Temperature Cutoff Circuit, Schematic Diagram

E. BATTERY MODULE ELECTRONICS PERFORMANCE LIMITS

The performance limits of the battery module electronics are summarized below:

(1) Normal-charge current - 1.1 ± 0.1 amperes

(2) Trickle-charge current - 150 ± 0.05 ampere

(3) High-temperature limit - 51.7°C ± 2.8°C

(4) High-temperature detection circuit hysteresis - 2.6°C ± 2.4°C

(5) Battery voltage-temperature detection band - See Figure 76.

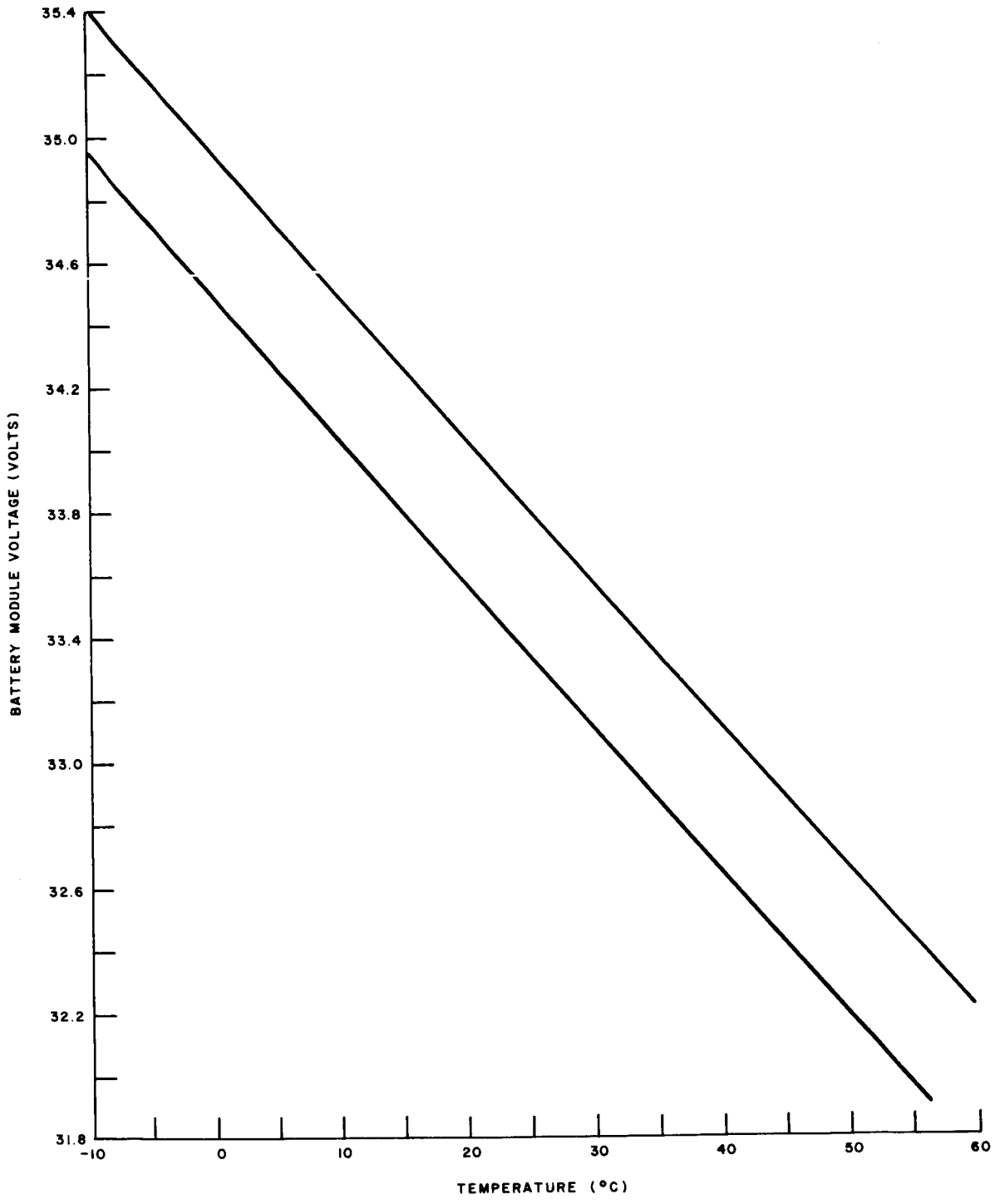


Figure 76. Recommended Voltage Limit Versus Temperature Curve

F. CHARGE AND DISCHARGE-CURRENT TELEMETRY

Figure 77 is a schematic diagram of the battery-charge current telemetry circuit. Only the charge-current telemetry circuit is discussed here, since its operation is identical with that of the battery discharge-current telemetry circuit. The circuit can be divided into three major sections:

(1) Current-sensing resistors R_{S1} and R_{S2},

(2) D-C amplifier (Q2, Q3, and associated components), and

(3) Bias source (Q1 and associated components).

The use of R_{S1} and R_{S2} in parallel reduces the probability of losing the ability to charge the batteries.

Transistor Q2-B amplifies the voltage drop developed across the current-sensing resistors R_{S1} and R_{S2} to produce a telemetry signal ranging from a nominal -0.5 volt to -6.0 volts (corresponding to 0 to 1.2 amperes charge current). Resistors R8 and R13 stabilize the voltage gain through degeneration. Resistors R14 and R9 are used to reduce the error in telemetry output voltage caused by battery-voltage variations. As can be seen from the collector characteristics of transistor Q1 (2N2060), the collector current is not entirely independent of collector voltage but tends to increase slightly with an increase in applied voltage. This effect is compensated for by modifying the bias on Q1 in a manner that reduces the collector current as collector voltage increases.

Resistor R4 aids in developing a constant voltage source at the base of Q2-B. The temperature characteristic of $Q2\text{-}B_{(V_{BC})}$ is virtually identical to that of $Q2\text{-}A_{(V_{BC})}$, resulting in the bias voltage at Q2-A tracking variations in Q2-B with changes in ambient temperature.

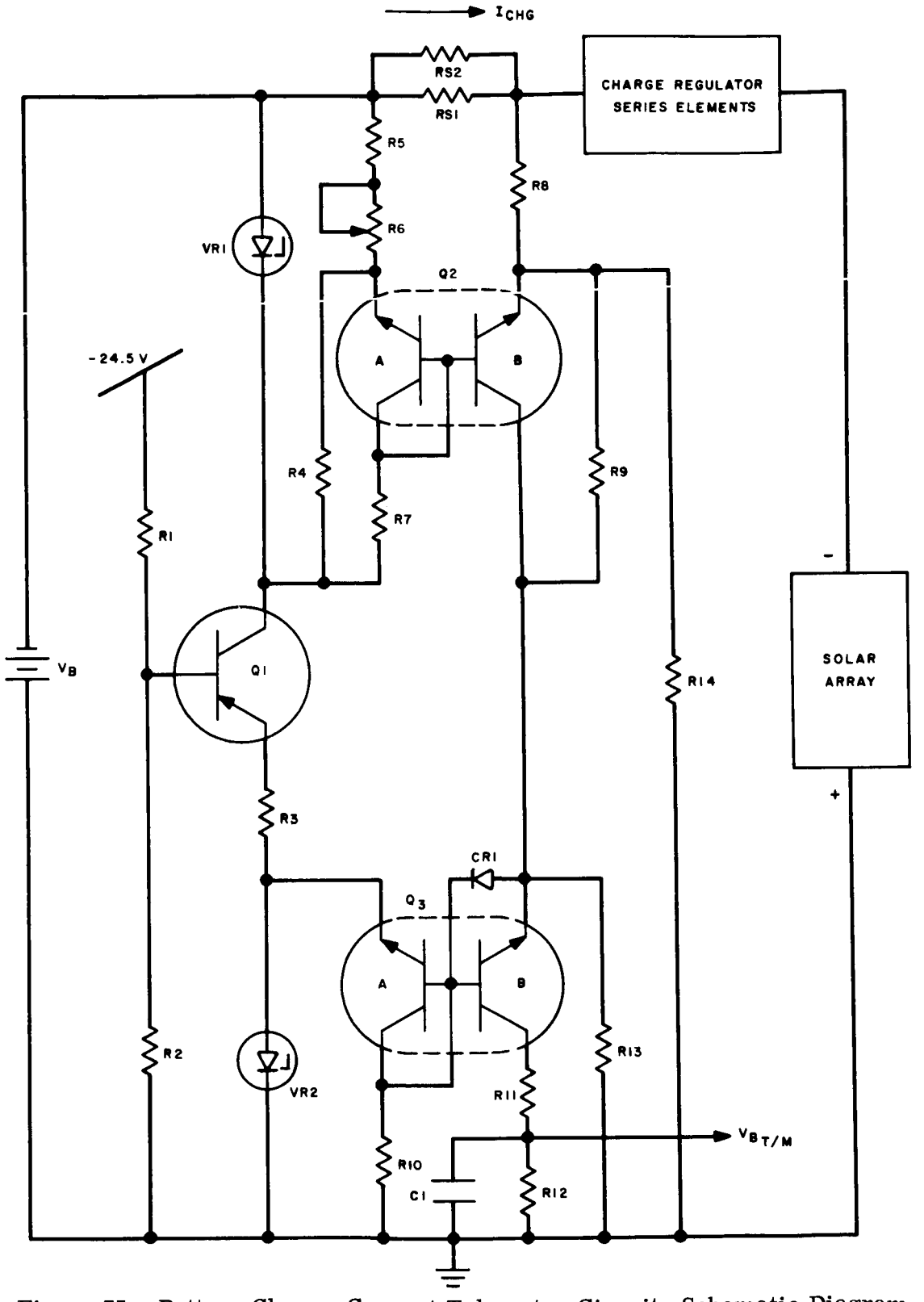


Figure 77. Battery Charge-Current Telemetry Circuit, Schematic Diagram

SECTION V
ELECTRONICS MODULE

A. ELECTRICAL DESIGN

1. General

Breadboard fabrication and testing of the electronics module circuitry was completed this quarter, together with a preliminary investigation of circuit sensitivity for electromagnetic interference problems. Design work was started on modification No. 2 to the contract which revised the regulated-bus comparator circuit to a "make-before-break" system. Nominal design for this circuit was completed and breadboard testing is in progress. Nominal design and worst-case analysis for modifications to the voltage telemetry circuits to include expanded range were completed, and breadboard testing of this circuitry is in progress.

In accordance with NASA directives, design modifications to the auxiliary regulator and shunt dissipator circuits are also in progress during this quarter. The various circuit redesign details are summarized in this section, followed by a discussion of the electronics-module power dissipation for three conditions of overall spacecraft system operation.

2. Regulated Bus Comparator

a. GENERAL

The present Nimbus-B power supply subsystem employs two pulse-width-modulated switching regulators, each with 20 amperes of load capability. One regulator supplies the total minus 24.5-volt bus load; the second is in a standby mode, only to be used in the event of a failure in the first regulator. The regulated-bus comparator (RBC) circuit is preset to sense a deviation in the -24.5 regulated bus voltage of greater than plus or minus 1.5 volts (failure mode), and by means of logic circuitry, relays, and associated driving stages, switch the standby regulator to "on-line" and the presumed-failed regulator to "off-line". A ground-command override circuit permits manual regulator switchover in the event that automatic switchover to a previously "failed" regulator occurs, or if internal failure-to-switch problems develop.

Originally developed under Contract NAS 5-3248 (AVR) and proposed for use on the Nimbus-B contract, the comparator design was based on achieving reliable switchover operation with the least number of components. Consideration was given to maintaining

the regulated bus at a minimum minus 20-volt level during the entire switchover sequence. This scheme required a 2-to-1 increase in parts count and was subsequently abandoned. From the spacecraft systems standpoint, only the clock subsystem was disturbed by momentary loss (20 to 30 msec) of the regulated bus. This problem was conveniently solved by "OR" gating auxiliary regulator power to the clock subsystem at a minus 23.5-volt level.

During recent spacecraft-system interface meetings at GSFC* (on November 5, 1965 and December 8, 1965), various new spacecraft failure modes were postulated by the momentary loss of the regulated bus during a switchover operation, either by ground-commanded or automatic operation. Of these, sporadic firing of the attitude-control gas jets was of primary concern. At this time, AED was asked to investigate a "make-before-break" scheme of achieving regulator switchover. A minimum minus 20-volt bus level is required during the switching interval.

A make-before-break scheme for switching the regulators has been incorporated and is discussed in paragraph b below, "Functional Description." In essence, the present system performs a sequential switching operation as opposed to the simultaneous switching in the previous RBC. The sequence is as follows:

(1) The standby regulator with its feedback drive inhibited is switched in parallel with the "on-line" regulator. Load current is not supplied by the standby regulator;

(2) The feedback is inhibited to the "on-line" regulator and restored to the standby regulator, which immediately supplies the total load current; and

(3) The original "on-line" regulator is switched "off-line".

The only interruption of the load under the present system is during the very brief transfer time of the flip-flop which performs the feedback inhibit switching function. The regulator output capacitor will sustain the regulated-bus voltage for this short time.

The additional circuitry required to sequentially switch the regulators consists of a flip-flop, time-delay circuits, and two relay-driving stages. The original two relays will be retained, but with the contacts connected in a manner which requires the failure of both relays to switch in order to cause catastrophic loss of the regulated bus.

b. FUNCTIONAL DESCRIPTION

With no signals appearing at the "OR" gate input, as shown in Figure 78, regulator No. 1 power transistors are connected to the energy-storage network

*Goddard Space Flight Center

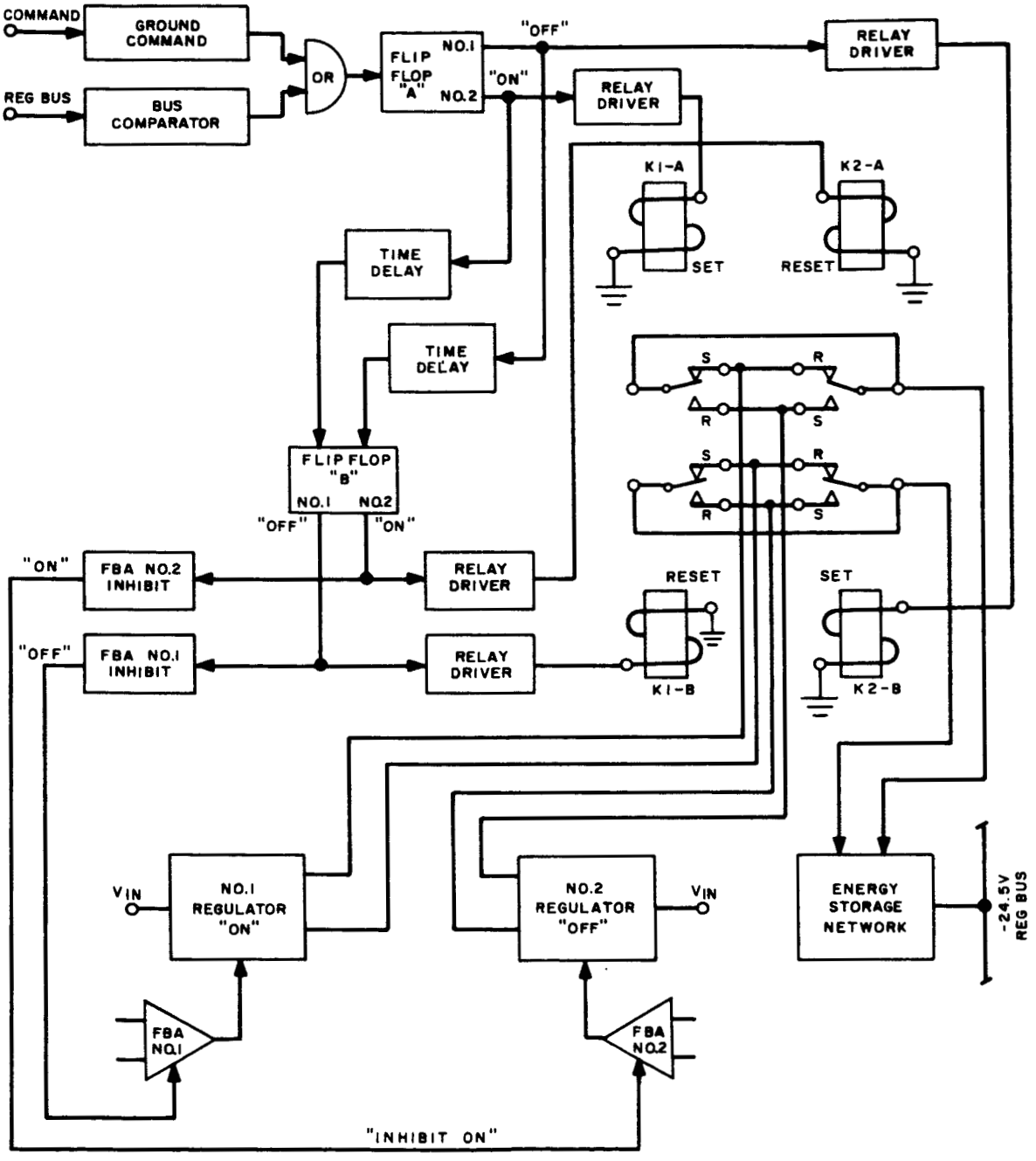


Figure 78. Regulated-Bus Comparator, Functional Block Diagram

(ESN) and the regulated bus through the K1-S and K2-R contacts, and the inhibit signal is "off" to regulator No. 1 feedback amplifier (FBA). Regulator No. 2 power transistors are disconnected and the No. 2 feedback amplifier is inhibited.

Upon receiving a signal from the "OR" gate, through either ground command or the bus comparator, the flip-flop "A" changes state and the K2-B relay coil is energized, thereby connecting the No. 2 regulator power transistors to the ESN in parallel with the No. 1 regulator. However, these transistors supply no current until the inhibit signal is removed from FBA No. 2. After a 20-millisecond time delay, which allows sufficient time for the K1 relay to switch, Flip-Flop "B" changes state and the inhibit signal is removed from FBA No. 2 and applied to FBA No. 1. Regulator No. 2 power transistors now supply the load current, and the only disruption of the load is during the transfer time of Flip-Flop "B". In effect, this is a make-before-break switching of the regulators to prevent loss of the regulated bus during changeover.

At the same time, the inhibit signals reverse, the K1-B relay coil receives power and it switches to the reset position. Regulator No. 1 transistoss are disconnected from the ESN and the system returns to normal. When a subsequent signal appears at the flip-flop "A" input, regulators Nos. 1 and 2 are switched "on-line" and "off-line", respectively.

The redundancy of the relay-contact connections, as shown in Figure 78, insures that when failure of either relay to switch, when the RBC is ground-commanded, it will not result in a loss of the regulated bus. For example, if the K2 relay contacts failed to transfer to the set position and everything else proceeded normally, regulator No. 2 would still connect to the ESN through the K1 reset contacts. If, on the other hand, the K1 contacts failed to transfer to the reset position, regulator No. 1 would remain connected to the ESN, but could not deliver current since FBA No. 1 would be inhibited. In either case, the regulated bus would remain at the minus 24.5-volt level, providing that both regulators are operating normally. In the case of both relays failing to switch and the inhibit signals transferring normally, the regulated bus would go to 0 volts, since feedback drive is inhibited to the "on-line" regulator.

3. Auxiliary Regulator

The auxiliary regulator circuit is being redesigned to accommodate the increased load requirement as per NASA direction. The modified circuit will have the following capabilities:

(1) Input voltage: -26v to -39v

(2) Load current: 0 to 1 amp

(3) Output voltage: -23.5 ± 0.5v

The basic circuit change, as shown in Figure 79, is the addition of a Darlington-connected driver transistor, Q2, to the series-pass configuration. The extra stage has the two-fold purpose of (1) reducing the input-to-ground shunt loss, since most of the driving current is delivered to the load by the collector of Q2, and (2) reducing the dissipation requirements of the low-power transistors Q3 and Q4, used in the second-stage differential amplifier.

Other circuit modifications include changes in resistor values associated with the Darlington-transistor pair and the second differential amplifier. A change in the loop stabilization is also required by the increase in loop gain due to the addition of Q2.

4. Shunt Dissipator

The shunt dissipator circuit has been designed to limit the solar-array bus voltage to a maximum of -38.8 volts. The threshold or turn-on voltage of the circuit is -38.0 ± 0.3 volts; this is the point at which solar-array current is just starting to be shunted. Since the threshold voltage may be as low as -37.7 volts, and the trans-conductance characteristic as high as 14-amperes per 0.1-volt charge in the solar-array bus, the current-handling capability of the shunt dissipator is 14 amperes at a voltage of -37.8 volts with a seven-module system. On the other hand, the power-handling capability of the circuit must be considered under the conditions of the maximum solar-array bus voltage of -38.8 volts and 14 amperes excess array current or 543 watts.

The shunt-dissipating elements, as shown in Figure 80, are being modified per NASA direction to include relay switching of the power-transistor collectors and emitters in the event of a transistor failure. The relay contacts in the emitter circuit permit removal of a shorted transistor to prevent continuous shunting of solar-array current. The relay contacts in the collector circuit allow the collector load to be applied across the solar-array bus as required. The relays and the power resistors will be remotely located from the battery modules, together with the two-voltage divider telemetry resistors which measure shunt-dissipator current as a function of the voltage across the collector load. Manipulation of the relays via ground command will enable the shunt regulator to maintain voltage limiting capability of the solar-array bus even with one or more shunt-dissipator transistor failures.

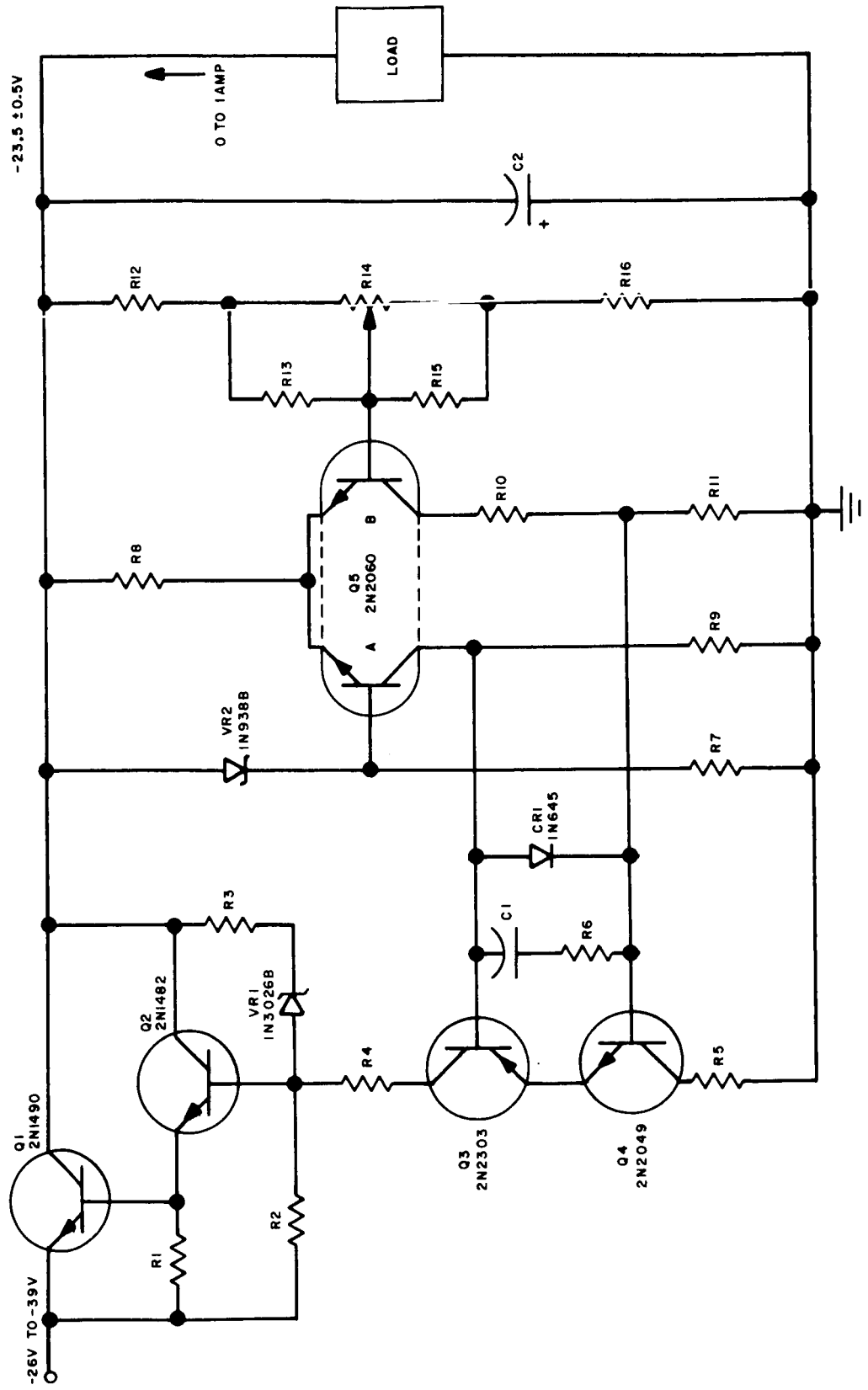


Figure 79. Auxiliary Regulator Circuit, Schematic Diagram

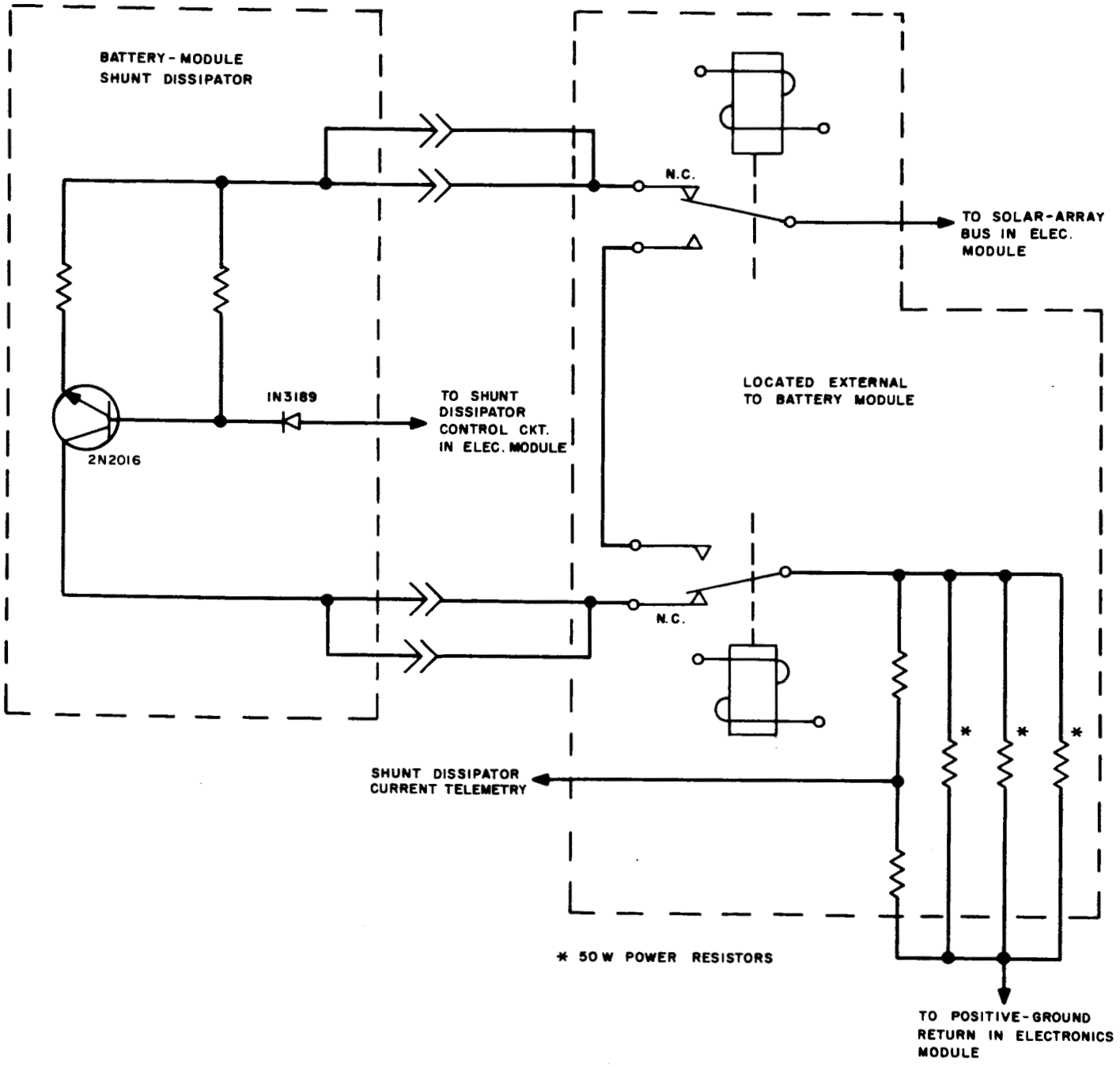


Figure 80. Shunt Dissipator Circuit, Simplified Schematic Diagram

5. Power Dissipations and System Efficiencies

The power losses in the electronics module have been estimated, from a combination of measured data and circuit calculations, for three conditions listed below:

a. Condition No. 1

(1) Solar-array at full capability (529 watts),

(2) Solar-array voltage input to electronics module at 37.5 volts,

(3) Spacecraft loads of 185 watts continuous at the -24.5-volt regulated bus, and

(4) All batteries accepting full-charge current.

b. Condition No. 2

(1) Solar-array at reduced capability,

(2) Solar-array voltage input to electronics module at 35 volts, and

(3) Spacecraft loads of 349 watts at the -24.5-volt regulated bus.

c. Condition No. 3

(1) Solar-array at full capability (529 watts),

(2) Solar-array voltage input to electronics module limited at 38.8 volts,

(3) Failure of -24.5-volt Bus (both -24.5-volt regulators inoperative),

(4) Spacecraft loads of 17.3 watts (total) at the -23.5-volt auxiliary-regulated bus, and

(5) No battery charge current.

The electronics module power dissipations and system efficiencies for the three conditions are listed in Table 12. The module system efficiency is defined as the ratio of power delivered to spacecraft loads, external to the power subsystem, and to the power into the electronics module at the solar-array input terminals (excluding power dissipated in the shunt-dissipator driver stage).

TABLE 12. ELECTRONICS MODULE POWER DISSIPATIONS AND SYSTEM EFFICIENCIES

Condition	Solar-Array Bus Voltage (volts)	Power In (watts)	Power Out (watts)	System Efficiency (Percent)	Regulator Dissipation (watts)	Shunt Driver Dissipation (watts)	Total Electronics Module Dissipation (watts)	Power to Storage Modules, (watts)
No. 1	38.6	220.3	185	84	28	--	28	7.3
No. 2	35	400.9	349	87	44.6	--	44.6	7.3
No. 3	38.8	49.1	17.3	35	28.6	23	51.6	3.2

B. MECHANICAL DESIGN

1. General

Revisions to the electronics-module packaging concept were made during this quarter due to revisions in the circuitry, inclusion of an electromagnetic inteference (EMI) control plan recommendations, and a review of the general manufacturing problems involved in unit fabrication and assembly. The module will consist of a single machining from a 6 x 8 x 13-inch aluminum section, rather than one formed by joining two 4 x 6 x 13-inch machined sections. With this exception, together with a rearrangement of components in the EMI compartment, the location and configuration of components within the module (see Figure 81) remains as presented in Quarterly Technical Report No. 1.

2. Printed-Circuit Boards

Board layouts, tape masters, and assembly drawings for the shunt dissipator, regulator control, auxiliary regulator, and regulated bus-comparator circuits (based on nominal circuit design) have been completed. An additional board was included to incorporate parts required for the "make-before-break" circuit design on the regulated-bus comparator. Design of the fuse boards has been delayed pending selection of fuses. Fuse selection must be based on specific system load requirements. All board drawings will be completed when changes due to modification No. 3 (auxiliary regulator and minus 24.5-volt regulator protection circuitry changes) have been resolved and incorporated.

3. Connectors and Wiring

Based upon tentative electronics module connector assignments presented in the last quarterly report, an interconnection list for all units in the power subsystem was prepared and submitted to NASA. At the present time, connector assignment and electronics module internal wiring is being revised to incorporate modification No. 2 wiring changes.

4. Electromagnetic Compatibility

An electromagnetic interference (EMI) control plan to be used during the design and development of the electronics module was completed this quarter. This document was forwarded to NASA under separate cover. Electronics module packaging concepts have been modified to include recommendations set forth in the EMI control plan. An EMI test plan which will indicate test conditions, test setup, and required related data is presently in preparation.

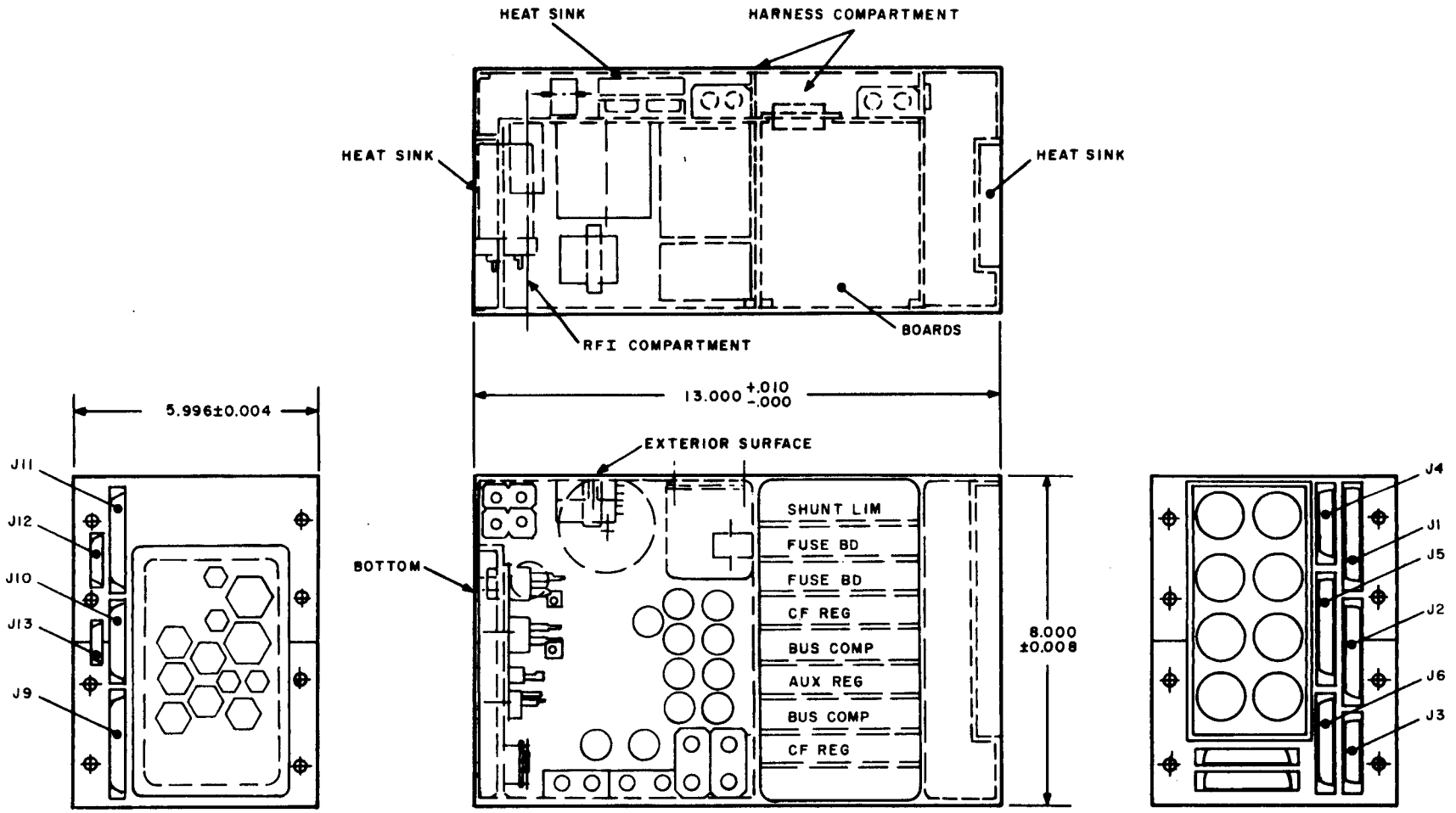


Figure 81. Proposed Nimbus-B Electronics Module Configuration

5. Weight

The total estimated weight of the electronics module at the present time is 19.22 pounds. This is broken down as follows:

(1)	Housing, covers, and brackets	5.39 lbs
(2)	Board assemblies, including components (8)	4.33 lbs
(3)	Harness-board assembly, connectors, harness, and miscellaneous electronic components	5.05 lbs
(4)	Heat sink assembly, including components (2)	2.20 lbs
(5)	Miscellaneous electronic parts and EMI filters	2.25 lbs
	Total Weight:	19.22 lbs

The reduction in weight from the 20 pounds previously reported is due to a reduction in the unit estimated weight for each of the 12 EMI filters.