FINAL TECHNICAL SUMMARY REPORT

1 JULY 1964 TO 25 FEBRUARY 1966

Advanced Telemetry System with Adaptive Capability

Contract NAS 8-5110, TP 2-831815

Prepared for George C. Marshall Space Flight Center, Huntsville, Alabama, and submitted by Lockheed Missiles & Space Company of Lockheed Aircraft Corporation, Sunnyvale, California.

Prepared by: H. N. Massey

Date: 25 February 1966

FOREWORD

This report describes work performed by Lockheed Missiles & Space Company under Contract NAS 8-5110 entitled "Advanced Telemetry System with Adaptive Capability" for George C. Marshall Space Flight Center, National Aeronautics and Space Administration, Huntsville, Alabama. This report is for the period 1 July 1964 through 25 February 1966, and covers work performed on the second and third experimental flight packages. Also, the retrofit of the first experimental flight package is covered. Seven (7) previous summary reports, (LMSC/657617, A035672, 664229, 8-39-65-1, 8-29-65-3, 8-39-66-2, and 669224), cover other work completed prior to or concurrent with the work reported in this report.

CONTENTS

Section 1

INTRODUCTION AND SUMMARY

The basic function of a vehicle borne telemetry system is to make measurements aboard the vehicle and transmit the results to a ground receiving station for display, recording, or entry into data processing equipment. These measurements are normally made in a manner which conveys an amplitude vs. time history of the quantities being monitored. Because of the large number of measurements required, it is impractical to provide the capability of continuously monitoring each measurement. For a majority of measurements, it has been found to be satisfactory to sample each measurement at some minimum rate which permits reconstruction of an amplitude vs. time history of the quantity with suitable accuracy and resolution. This makes it possible to time division multiplex a large number of measurements into a composite wavetrain for transmission over a common communication channel. However, as the number of measurements and the problems of providing sufficient bandwidth over greater distances associated with space vehicles increase, the need for improvements in techniques continues.

Investigations of telemetry data from space vehicles have confirmed that most of the data is redundant. In particular, it was found that time division multiplexed data contained a high degree of redundancy. It was reasoned that, if a system could be devised which examines the data for redundant

properties and transmits only the information actually required for reproducing the data variations, a significant reduction in bandwidth requirements could be achieved. A system, known as a telemetry data compressor, has been devised to accomplish this operation.

The general approach to the vehicle-borne system design was to add the redundancy removal capability to an existing PCM telemetry system to minimize new equipment development. Redundancy removal was implemented with logic based on the prediction that the next data sample value will be equal, within specified tolerance limits, to the last sample value transmitted. (This is also referred to as zero-order, floating-aperture logic.) To minimize the probability of buffer memory overflow, a method was devised for increasing the tolerance limits as a function of buffer occupancy.

The work under Contract NAS 8-5110 has been accomplished in six phases and has included tasks from conceptual and feasibility studies through the production of three experimental flight systems. Most of this work has been covered in previous reports.

During the first twelve months, work on Contract NAS 8-5110 was completed through Phase IV and reported in Reference 1. This included a conceptual study, design and construction of a non-flyable prototype system, test and evaluation of the prototype, and the formulation of specifications for the design and development of a flyable system.

Under Phase V, reported in Reference 2, improvements to the system were investigated and a revised performance specification was formulated. The feasibility of a reference memory with a capability of both DRO and NDRO storage was investigated and a workable solution was obtained. Sources of suitable memory cores were located and circuit development of driving and sense circuits was accomplished. System performance implications resulting from the use of a "large" buffer memory was investigated. System and circuit designs were accomplished to incorporate a "large" (1,024 word) buffer memory into the system. Performance specifications were revised to reflect these memory changes and other changes to performance requirements.

Under Phase VI, reported in Reference 3, the system and circuit design of the Data Compressor were revised to meet the requirements established during the Phase V work. Mechanical and packaging design of an experimental flight package was completed. The first experimental flight package was built and tested for operation within space vehicle environments.

Test results obtained with the first experimental flight package were used in making design corrections. Then, a second and third experimental flight package were built and tested for operation over the temperature range. Also, the first experimental flight package was retrofitted to have a reference memory of 480 words (for economy, 240 active and 240 dummy words were originally included in the reference memory of the first package).

Concurrent with the Phase VI work discussed above, additional tasks under Phase V were completed. A description of two types of digital filters,

suitable for precompression filtering, with examples and discussion, was given in Reference 4. Results of preliminary implementation studies of advanced compression algorithms were reported in Reference 5. The results of a survey of high speed digital logic circuits, for implementation of advanced compression algorithms, are given in Reference 6. An investigation, by breadboard techniques, of design improvements and techniques for implementing specific algorithms (ZVA and FVA) is described in Reference 7.

Section 2

DESIGN IMPROVEMENTS

2.1 General

During the test of the first experimental flight system, several design deficiencies were disclosed. Design changes to correct these deficiencies were made prior to fabrication of the second and third experimental flight systems. In making these design changes, an attempt was made to maintain functional and mechanical interchangeability of minor and major subassemblies of the second and third systems with those of the first system. In several instances the effort required for redesign exceeded that required to rework parts fabricated to the old design. In these instances, the "redesign" was limited to marking of blueprints to provide the necessary rework instructions.

2.2 Circuit Design Changes

Most circuit design changes were simply the incorporation of changes which were found necessary to achieve correct operation of the first system. Also, there were some changes made to improve confidence in areas where potential problems or marginal operation existed.

Within the logic subassembly, the majority of the changes were to correct for peculiarities of the Texas Instruments series 51

integrated circuits. DC loads to ground were added to all emitter-follower outputs. Also, DC loads to ground were added in several locations to lower the level of the clock input to flip-flop circuits. In a few instances the logic signals to gate inputs were revised to obtain the correct outputs. Considerable revision was made to the output circuit of the bit rate countdown counter to obtain the correct countdown and output. Also a diode-resistor network was added to eliminate reverse propagation within the bit rate counter. The output word length counter was revised to correct design errors which were present in the schematic and had been carried into the printed circuit board design.

Memory circuit changes involved sense amplifiers and regulated current drivers. In the reference memory, the NDRO sense amplifier circuit was revised to achieve improved threshold characteristics. In both memories, decoupling was added to all sense amplifier outputs to reduce the susceptibility of the sense amplifiers to noise due to cross coupling within the interconnecting wiring. All tunnel diodes used in sense amplifier circuits were changed to a type made from silicon material (during tests of the first system, gallium arsenide tunnel diodes were found to be unreliable). To eliminate false triggering of current drivers within both memories, resistor values were changed in the input circuits of the drivers.

2.3 Mechanical and Packaging Design Changes

Mechanical and packaging design changes were made to accommodate circuit changes, to correct deficiencies disclosed during work on the first system, and to improve ease of fabrication or assembly.

Changes to accommodate circuit revisions involved modification of printed circuit board designs. Only selected logic circuit boards were revised (all other logic boards were changed, if necessary, by reworking boards produced from the original design). The designs of the sense amplifier circuit boards in both memories were revised.

To correct a problem of breakage of coaxial wires, the connectors and connector brackets located at the top of both memories were eliminated. Interconnect between the logic subassembly and the top of both memories was accomplished by cabling wires directly from memory board terminals to connectors at the logic subassembly end only. The connector bracket on the logic subassembly was redesigned and connector arrangement revised to accommodate the memory/logic interface change. Wiring from external system interface connectors and the power converter, which previously went to the top of the memories, was rerouted through existing connectors at the bottom of the memories. The stabilizer frame, which straps the tops of the logic subassembly and the memory subassemblies together, was revised to reflect changes at the tops of the memories and to provide increased clearance between the frame and the equipment cover.

The reference memory design was modified to provide increased stiffness at the top and bottom of the subassembly. At the top, stiffeners were added to the bit driver circuit board and the reset driver circuit board. A rigid polyurethane foam was also added to the reset driver circuit board. At the bottom of the subassembly, stiffeners were added to the auxiliary circuit board.

Section 3

FUNCTIONAL TESTING PROBLEMS AND CORRECTIVE ACTIONS

3.1 General

Functional testing of the second and third experimental flight packages was accomplished in a way similar to that of the first package described in Section 4 of Reference 3. In addition, tests were conducted at high and low temperature extremes. Also, after retrofit work on the first experimental flight package, it was tested to verify correct operation at room temperature.

The test of each flight package will be discussed in the same order that they were tested. Problems encountered, during the construction and test of these packages, will be discussed if the problem was of special significance and has not been covered in previous reports. For example, problems with Texas Instruments series 51 circuit modules were reported in appendix A of Reference 3 and will not be repeated here.

3.2 Test of the Second Experimental Flight Package

The checkout and test of the second experimental flight package was similar to that accomplished with the first package (see Reference 3). Circuit design changes, which were made as a result of experience with the first package, were found to be effective. Replacements for the two types of diodes which were problems in the first package proved to be satisfactory. The silicon tunnel diodes, used as threshold elements

in the memory sense amplifiers in the second package, performed as desired and without the high failure rates previously experienced with gallium arsenide tunnel diodes. The high failure rate of double-junction microdiodes was found to be corrected. (These double-junction diodes are in series with logic inputs to the system to increase the maximum "0" logic level which can be tolerated.) It was found that use of the replacement double-junction diode resulted a maximum tolerable "0" logic level which was equal or exceeded the goal for all environmental temperatures of +70°C and below. Observed values of input logic levels which produced correct system operation were:

Temperature in °C	Maximum "0" in volts	Minimum "1" in volts
-20	>1.4	<2.4
+25	1.15	<2.5
+70	1.0	<2.4

The readjustment of the current pulse amplitude from the "write" current drivers in the reference memory was found necessary. (Similar adjustments had been required for the first package.) Tolerances permitted in pulse amplitude for the initial test of the "write" current drivers were incompatible with current drive requirements of the memory cores. After readjusting the "write" current amplitude, using the closer tolerances, no further difficulty was experienced with outputs from the memory cores.

During tests using the 288KC system clock rate, several marginal timing problems were disclosed. These were generally caused by the duration of one-shots and were corrected by a reduction in duration.

A major problem encountered (in terms of effort required for correction) was that of wiring shorts on the logic interconnect matrix. Shorts, between wires and wire-wrap pins, were caused by routing the wires too tightly around the sharp corners of wire-wrap pins so that the wire insulation was cut. This was principally a workmanship problem. (Very little difficulty had been experienced with the first package which had better workmanship.) A contributing cause was the ease of cutting of the wire insulation - an irradiated, modified-polyolefin. Correction of this problem in the second package was accomplished by location and correction of each short. The location of the shorts or near-shorts was by visual inspection with binocular microscope and by functional tests - including temperature cycling. A wire, for future use, with a Mylar base insulation was evaluated and found to be superior to the irradiated, modified-polyolefin insulation. For the third package, this wire with a Mylar base insulation was used.

Two other problems encountered involved the magnetic memory modules of the reference memory. Stresses produced by the epoxy conformal coating, during temperature cycling, cracked glass-cased diodes. Corrective action included removal of epoxy from around diodes, replacement of

cracked diodes, and recoating with a silicone material. A problem of corrosion, between copper conductors and a magnesium alloy plate, developed during temperature cycling. It was concluded that moisture, which condensed on the package during low temperature tests, without cover, had acted as an electrolyte between the metals. All reference memory magnetics modules were removed, inspected for damage, repaired, recoated and reinstalled. (As a protection against this sort of problem, an epoxy coating had been applied to the metal surfaces and the package is designed to contain an internal atmosphere of dry nitrogen gas.)

In addition to verification of correct performance of data handling functions, observations of input and output parameters were recorded. These were:

POWER INPUT

Input Voltage in Volts	Input Power in Watts					
	144 KC System Clock			288 KC System Clock		
	Temperature			Temperature		
	-20°C	+25°C	+70°C	-20°C	+25°C	+70°C
20.0	16.6		12.0			
23.8		12.85			17.25	
26.0		12.4			17.17	
28.0	13.73	12.6	10.9	17.37	17.25	13.17
30.0		12.6			17.4	
32.2		12.8			17.55	
35.0	14.35		11.56			

Note: For input power measurements, the data sample magnitude input contained 5 0's and 5 1's.

CPCM SIGNAL OUTPUT *

Temperature	Amplitude in volts P-P	Rise Time in microseconds
-20°C	9.5	1.5
+25°C	10	1.8
+70°C	10	2.0

* Across load of 200 ohm resistor and 0.003 microfarad capacitor in parallel.

The power input to the package and the compressed PCM signal output, as observed and tabulated above, were within the limits specified.

3.3 Test of Third Experimental Flight Package

The checkout and test of the third experimental flight package was accomplished in a manner similar to that described for the second package. The main difference was that many fewer problems were encountered with the third package. (Experience gained from work on the first and second package had been applied during construction and subassembly test of the third package.) However, several problems were encountered which are worth discussing.

Additional marginal timing conditions were disclosed when operating at the 288 KC clock rate. Corrections were made by reducing the duration of one-shots. (These were not the same one-shots discussed in paragraph 3.2 of this section.)

On checking for correct operation of the redundant sample routine, it was discovered not to be functioning entirely correctly. A wire list error had caused a wire to be mislocated. Also, it was concluded that the redundant sample routine probably had not functioned entirely correctly in the first and second package - it only appeared to work. Actually, redundant samples were accepted during the master frame period in which a new cycle of the redundant sample routine was started and this is what had been interpreted as indicating that the redundant sample routine was working correctly. The wiring error prevented storage of the redundant sample tag in the reference memory. After correction of the wiring error, proper operation was demonstrated.

A new problem of faulty components occurred with the third package. During temperature tests, it was found that the current pulse amplitude from the reference memory "write" drivers did not change properly as a function of temperature. (The current drivers are designed to have a negative temperature coefficient to compensate for a change in ferrite memory core characteristics.) The cause of this problem was traced to type VT-1/8 temperature compensating silicon resistors obtained from Vector Solid State Laboratories (Vector Department of Norden Division of United Aircraft Corporation). A separate test of this resistor type in the resistance range of 12 to 30 ohms indicated a positive temperature coefficient of considerably less than the published value of +0.7% per degree C. Also, the temperature coefficient was found to vary widely from resistor to resistor. Based on published information which implies

that the type VT-1/8 resistors are electrically equivalent to Texas Instruments type TM-1/8 resistors, LMSC procurement had chosen to buy the type VT-1/8 resistor for the third package. (Only type TM-1/8 resistors were used for temperature compensation in the first and second packages.) Corrective action was to replace type VT-1/8 resistors with type TM-1/8 resistors in the "write" driver circuits. There are type VT-1/8 resistors installed elsewhere in the third flight package which were not replaced. Replacement of these other type VT-1/8 resistors was not considered warranted because the temperature coefficient required is less critical.

After verification of correct operation at each temperature, the following observations of input and output parameters were recorded:

INPUT LOGIC LEVELS

TEMPERATURE IN °C	MAXIMUM "0" IN VOLTS	MINIMUM "1" IN VOLTS
-20	1.4	2.5
+25	1.4	2.5
+70	1.27	2.5

POWER INPUT

INPUT VOLTAGE IN VOLTS	Input Power In Watts					
	144 KC System Clock			288KC System Clock		
	Temperature			Temperature		
	-20°C	+25°C	+70°C	-20°C	+25°C	+70°C
23.8	15.48	12.5	11.4	21.1	16.8	15.95
26.0	14.82	12.5	11.44	19.75	16.8	15.87
28.0	14.84	12.46	11.5	19.6	16.8	15.96
30.0	15.0	12.46	11.56	19.5	16.8	16.2
32.2	15.13	12.58	11.6	19.97	16.9	16.44

Note: For input power measurements, the data sample magnitude input contained 5 0's and 5 1's.

CPCM SIGNAL OUTPUT *

TEMPERATURE IN °C	AMPLITUDE IN VOLTS P-P	RISE TIME IN MICROSECONDS
-20	9.2	1.5
+25	9+	1.5
+70	9	1.6

* Across load of 200 ohm resistor and 0.003 microfarad capacitor in parallel.

The input logic level limits and the compressed PCM signal output, as observed and tabulated above, were within specified limits. The maximum "0" logic level at +70°C was significantly higher than had been observed for the second package. The reason for this improvement in the third package was not determined. Except for two test conditions, the power input was within specified limits. These two test conditions were at -20°C with a 144 KC system clock with 23.8 volts input and with 32.2 volts input. For each of these conditions, the limit was exceeded by less than 0.5 watt.

3.4 Retrofit and Test of the First Experimental Flight Package

The first experimental flight package was retrofitted to provide a reference memory storage capacity of 480 words. This was accomplished by replacement of dummy parts with active parts and installation of the required additional logic. Also, improvements developed on units 2 and 3 were made so that the first experimental flight package is now functionally equivalent to the third package.

In the process of procuring the additional memory parts, it was discovered that the two-hole memory cores, for NDRO storage, were no longer available with the same specification limits as those previously obtained. Two-hole cores with slightly higher drive requirements were substituted in the added 240 words of memory. To compensate for this, the "write" current drivers, associated with these added memory cores, were adjusted to provide a correspondingly higher output amplitude. This was accomplished during boardlevel tests. No particular difficulty arises from use of these two-hole cores with higher drive requirements, other than a reduction in drive margin for the one-hole DRO cores.

During retrofit work, the disassembled logic and reference memory subassemblies were inspected for damage to internal parts resulting from previous environmental tests (shake, shock, and temperature). The only damage found was cracked glass-case diodes in the reference memory (caused by use of an epoxy material to conformal coat the diodes and temperature cycling). Corrective action was taken as described in paragraph 3.2 for the second package. For new parts added to the first package a silicone material was used for conformal coating. A check for corrosion, as had been found in the second package, revealed no evidence of corrosion - apparently prevented by a better protective coating of epoxy and less exposure to moisture.

After retrofit rework, the first package was functionally tested and no major difficulties were experienced. The following input and

output data were observed. All data were observed at an ambient temperature of approximately +25°C.

Input logic levels:

Maximum "0" of 1.4 volts

Minimum "1" of 2.5 volts

INPUT POWER

Input Voltage in Volts	Input Power in Watts	
	144KC System Clock	228KC System Clock
23.8	12.6	17.35
26.0	12.75	17.18
28.0	12.04	17.1
30.0	12.0	16.65
32.2	11.6	17.08

Compressed PCM output signal:

Amplitude = 9.5 volts peak-to-peak

Rise Time= 1.0 microseconds

The input logic level limits, power input, and compressed PCM signal output, as observed and tabulated above, were within specified limits.

Section 4

CONCLUSIONS AND RECOMMENDATIONS

The feasibility of an advanced telemetry system with adaptive capability for application in a space vehicle environment has been demonstrated. This system acquires data, examines the data for redundant properties and transmits only information actually required for reproducing data variations on the ground. The application of this system will reduce the bandwidth required to transmit the data and/or increase the amount of data that may be transmitted in a specified bandwidth.

Three experimental flight packages have been produced and tested. The ability of these flight packages to meet the performance requirements when operating in a space vehicle environment was proven by test of the first package.

An investigation has been conducted, by breadboard techniques, of design improvements and techniques for implementing of algorithms which show promise of higher compression ratios. The high-speed parts of a hybrid ZVA/FVA Data Compressor have been designed and tested at the breadboard level.

There are additional tasks recommended which are expected to lead to the successful application of advanced telemetry systems with adaptive capability aboard space vehicles. These additional tasks are as follows:

1. Determination, by experimental tests, of the detail performance criteria for a flight system. Results should be usable as a guide in programming the detail performance of the experimental flight packages.

2. The incorporation of data compression into a telemetry system aboard a space vehicle on an experimental basis. This should provide verification of or show the need for improvement upon previous simulation studies.

3. Construct additional experimental flight packages, if required, to support experimental flight evaluation of compression techniques.

4. Develop and construct additional ground data handling equipment required for reconstruction of the compressed data.

5. Conduct further investigations of techniques for implementation of compression algorithms which are shown analytically to be feasible and useful.

Section 5

REFERENCES

The following references are reports produced by Lockheed Missiles and Space Company on Contract NAS 8-5110 entitled "Advanced Telemetry System with Adaptive Capability". (Monthly progress reports are not listed.)

1. Lockheed Missiles and Space Company, Annual Technical Report - Advanced Telemetry System With Adaptive Capability, by J. A. Horton, H. N. Massey, and W. E. Smith, Report No. 657617, 30 July 1963.

2. Lockheed Missiles and Space Company, Phase V Technical Summary Report, by H. N. Massey, Report No. A035672, 20 March 1964.

3. Lockheed Missiles and Space Company, Technical Summary Report on The First Experimental Flight Package of An Advanced Telemetry System With Adaptive Capability, by J. A. Horton, H. N. Massey, and G. J. Whyte, Report No. 8-39-66-2, 7 February 1966.

4. Lockheed Missiles and Space Company, Interim Report - Phase V, Adaptive and Non-Adaptive Precompression Filtering, by W. R. Bechtold and D. R. Weber, Report No. 664229.

5. Lockheed Missiles and Space Company, Preliminary Implementation Studies of Advanced Compression Algorithms, by W. R. Bechtold and W. E. Smith, Report No. 8-39-65-1, 30 June 1965.

6. Lockheed Missiles and Space Company, Advanced Algorithm Investigation - High-Speed Integrated Circuit Survey, by W. E. Smith, Report No. 8-39-65-3, 19 August 1965.

7. Lockheed Missiles and Space Company, Summary Report - Implementation Investigations of ZVA/FVA Compression Algorithms, by H. N. Massey and W. E. Smith, Report No. 669224, 28 February 1966.

8. Lockheed Missiles and Space Company, Operation Manual, Advanced Telemetry System With Adaptive Capability (Data Compressor) Model TDC-1, by J. A. Horton and H. N. Massey, 1 November 1965, Report No. 8-39-65-4.