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A SPACECRAFT DIGITAL STABILIZATION AND CONTROL SYSTEM STUDY

by H. C. Daubert, E. W. Hoffman, and T. E. Perfitt

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ABSTRACT

A study and experimental evaluation was performed to apply digital techniques to the problem of increasing the reliability and accuracy of spacecraft stabilization and control systems, as the sophistication and duration of spacecraft missions are increased. To meet these more stringent requirements, the use of digital systems utilizing monolithic integrated microelectronics is indicated.

Of major consideration during this study were the examination of mathematical techniques for systems analysis and the investigation of problems involved in fabricating systems using integrated circuits. A specific type of loop was postulated, designed and constructed with monolithic integrated circuits. A state-space model of this system was written and programmed for computer evaluation. The mathematical model of this system is described and a comparison made between the predicted performance and actual system performance tests made on an air-bearing simulator. The design logic, fabrication problems, and a computer-aided design optimization method are described.

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A SPACECRAFT DIGITAL STABILIZATION AND CONTROL SYSTEM STUDY

1 INTRODUCTION

As the sophistication and duration of future spacecraft missions are increased, more demanding requirements of reliability and accuracy will be placed upon their stabilization and control systems. For this discussion, the term "stabilization and control" is assumed to include the pointing or aiming control of spacecraft subsystem elements as well as attitude control of the entire spacecraft structure. Examples of such subsystem elements requiring independent pointing control are solar power panels, TV cameras, communication and tracking antennae, and laser sources.

The following brief introductory discussion defines generally the problem facing the spacecraft control system designer in terms of known and anticipated reliability and accuracy requirements.

1.1 REQUIREMENTS OF SPACECRAFT CONTROL SYSTEMS

The functions of a spacecraft stabilization and control system are to:

a. measure spacecraft angular orientation with respect to specified reference coordinates, and

b. apply proper control torques to maintain a specified attitude or to change attitude in a specified manner.

For each spacecraft mission the stabilization and control system requirements are different. There is, however, a universal requirement for increased reliability and improved accuracy as mission sophistication and duration are increased.

Mission times of the order of one year are presently common for spacecraft now under development, such as AOSO and OAO. To assure an overall reliability of 0.7, the stabilization and control subsystems for such spacecraft must have a reliability of better than 0.9 for one year. For many spacecraft of the future, mission duration of several years will be a requirement with equal or better mission success assurance.

Together with this increasing demand for improved reliability is the requirement for improved accuracy of spacecraft stabilization and control systems. For the OAO Princeton experiment, a pointing accuracy of 0.1 arc second is required. This extreme accuracy is presently feasible because the axis to be controlled is nominally coincident with the reference line, i.e., it is a null seeking system. For those missions which require precise pointing -- offset with respect to a sensed reference direction -- the stabilization and control system accuracy requirements are more severe. In terms of permissible error over the range of operation, the accuracy may be expressed as a percentage. For AOSO, the control system accuracy must be better than 0.3% to maintain ± 1.0 arc minute at a 5.0 degree angular offset from the sun's center. Much improved pointing accuracies will be required to utilize lasers in space communication systems. If a hemispherical range of operation is assumed, a pointing control accuracy of 1.0 arc second over a range of ± 90 degrees would require an accuracy of 0.0003 percent.

1.2 SELECTION OF MEANS FOR MEETING REQUIREMENTS

In approaching the problem of designing a system with an accuracy of 0.001 percent and a reliability of 0.9 for 3 years as is anticipated for this general class of future spacecraft, two broad aspects must be considered - the system philosophy and the component selection. Two basic systems techniques are possible - analog and digital.

1.2.1 Analog Systems

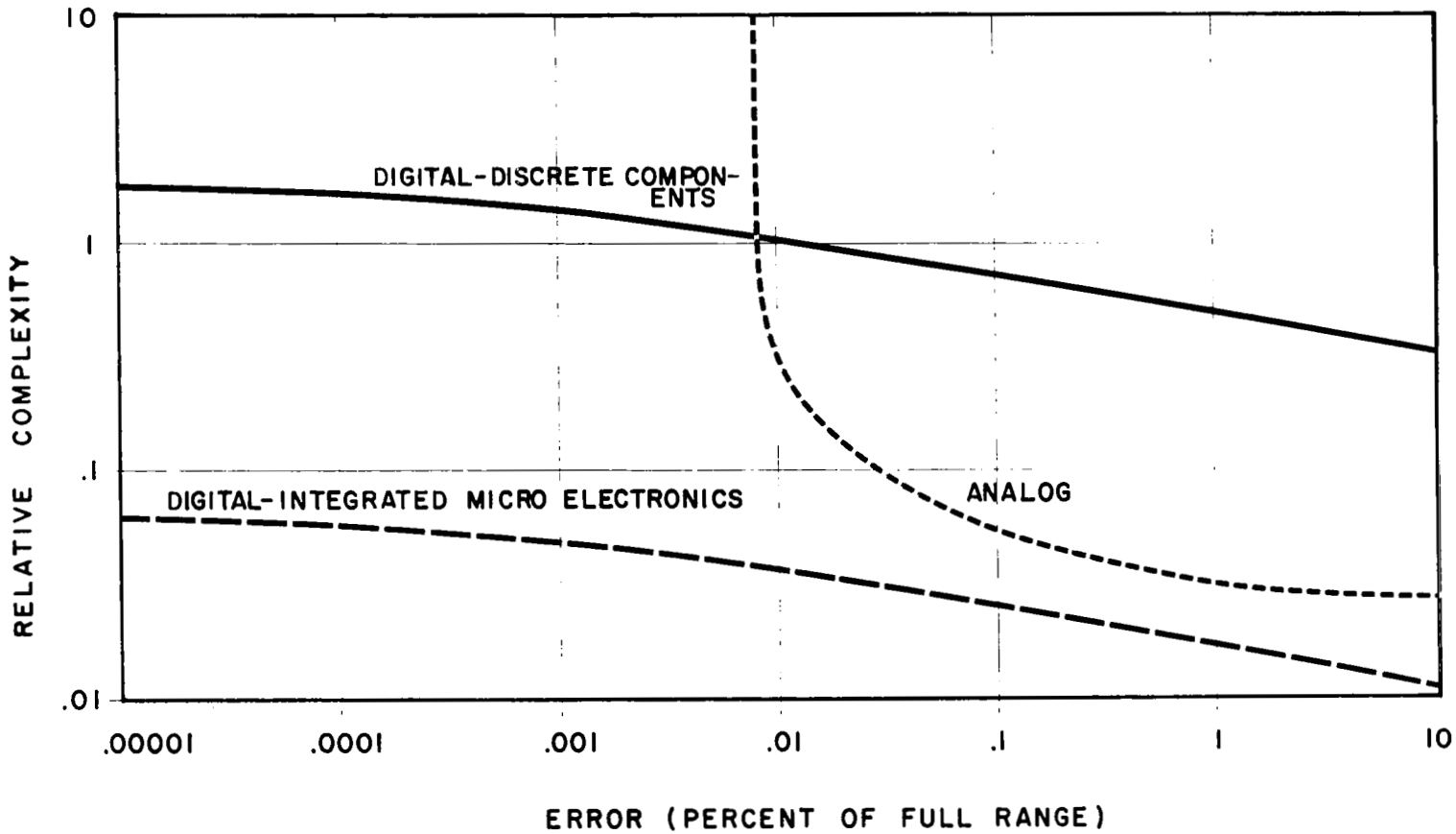
In an analog control system, physical quantities such as angles, torques, and momenta are represented by other physical quantities such as voltages, currents, shaft angles, magnetic fields, etc. Control data processing is done in terms of the substitute or analog quantities using electronic, electromagnetic, and mechanical devices. This analog approach is the one most frequently used in present spacecraft control systems and is entirely compatible with present and near future reliability and accuracy requirements.

Based on extensive production design experience with analog flight control and reference equipment, LSI has determined that there is an absolute limit to the accuracy capability of the analog approach. As the performance or accuracy requirement approaches 0.01 percent of operating range, there is a sharp increase in analog system complexity, with the ultimate possible system accuracy being only slightly better than 0.01 percent. This relation between system complexity and accuracy is illustrated by the dashed curve of Figure 1. Complexity is defined herein in terms of number of discrete components and is considered to be a good yardstick for comparison of possible system approaches, since reliability, cost, size, and weight are all directly related to complexity. Unity complexity in Figure 1 is chosen as the known complexity of an existing LSI breadboard digital control system, discussed more fully later. The explanation for the absolute limit of analog accuracy at approximately 0.01 percent lies in the fact that the components used (resistors, capacitors, inductances, mechanical elements) all have practical tolerance limits, especially over a range of temperature, radiation, vibration, and time. Sequential, operational electronic amplification stages, for instance, must maintain fixed gain characteristics over wide linear ranges (especially in early stages) if accuracies of the order of 0.01 percent are required for the entire system. There is generally a cumulative error effect due to component tolerances in an analog system.

Considering only the accuracy goal of 0.001 percent of full range postulated previously, it can be seen that a system approach other than analog must be sought.

1.2.2 Digital Systems

In a digital control system, the fundamental physical quantities (angles, torques, etc.) are measured, processed, and applied in discrete, quantized form. Data processing is done numerically. The fundamental building blocks of a digital control system are flip-flops



COMPARISON OF ACCURACY AND COMPLEXITY
FIGURE 1

and gates. These logic elements are essentially on-off devices and can tolerate wide variations (on the order of 20 percent) of operating levels and component parameters without any degradation of performance of their assigned function.

Because of the discrete nature of the digital system, variations of component tolerances within their broad operating limits do not produce a cumulative error effect as in the case of an analog system of equal accuracy requirement. Because of this non-cumulative property, system resolution, and hence accuracy, can be increased without theoretical limit by continued addition of stages. This is illustrated in Figure 1. For each binary bit (or stage) added, the system accuracy is doubled. The standard of complexity used in Figure 1 is the number of discrete components (approximately 8000) actually used in a breadboard digital stabilization and control system built by LSI prior to this study and which was used as a model for the integrated circuit controller built during this study. The observed accuracy of this system is 0. 012 percent, or 2. 64 arc minutes, at any point in the range of ± 180 degrees, as shown by the intersection of the upper solid curve (digital-conventional components) with the selected standard, or unity complexity level. Based on this proven point, digital system complexity can be predicted for system accuracy requirements both smaller and larger.

No fundamental barrier to increased accuracy exists as is the case with analog systems. The practical limitation is due only to sensor accuracy, readout resolution, and fineness of actuator torque application. It should be noted here that the information presented in Figure 1 was based on controller electronics only, and does not include either primary sensor or actuator components, which were assumed to be identical for all three curves presented. This assumption is justified if the primary sensor is considered to be a lock-on or tracking type which operates only at, or very close to, a null position -- well within the absolute angular accuracy requirement of the system. The readout of spacecraft position is then assumed to be a shaft encloder for a digital system, and an analog transducer -- such as a synchro -- for an analog system.

Likewise, the actuation means -- considered to be identical for both digital and analog systems -- is a reaction wheel-reaction jet type system.

From an accuracy standpoint alone, then, the digital approach is the only method for obtaining the previously stated goal of 0. 001 percent of full range. As can be seen from Figure 1, however, the complexity of a digital system, built from conventional components, would impose severe restrictions on meeting the reliability requirement of 0. 9 for 3 years. It should be noted, however, that the use of digital system approach in itself would permit a somewhat greater complexity, without decrease in reliability, because of the broader tolerance to discrete component parameter changes.

1.2.3 Component Selection

In designing a spacecraft stabilization and control system for future needs, the means for implementing the selected system are as important as the system approach itself. For either an analog or a digital system, two general component approaches are possible -- conventional circuitry and microelectronics.

By conventional electronics is meant discrete resistors, capacitors, transistors, diodes, inductances, etc., of the type readily available in a wide variety of tolerances and package configurations. Individual interconnections among components are necessary.

Any electronic system can be implemented with conventional components, but for operational spacecraft control systems this approach must be evaluated in terms of reliability and accuracy. Because complexity (number of individual components) is inversely proportional to reliability, a preliminary evaluation of the conventional component approach to both analog and digital systems can be made on the basis of relative complexity. Referring again to Figure 1, it can be seen that, for moderately accurate stabilization and control systems, the conventional electronic component approach is much more applicable to the analog than to the digital system. As the accuracy requirement approaches ±0.01 percent, the increase in complexity for an analog system makes the use of conventional components prohibitive.

Two forms of microelectronics are considered for implementing future spacecraft control systems: thin-film integrated circuits and semiconductor integrated circuits. Integrated circuits can be defined as those circuits in which all component parts required to perform a circuit function are fabricated on or within a single block of material.

Thin-film integrated circuits are made, basically, by the deposition of various film layers of different materials on an insulating (usually glass) substrate to form the required circuit.

Thin-film circuits have the advantage of being able to utilize a variety of materials to produce the required circuit functions. Since these are deposited upon an insulating substrate, the substrate itself does not usually contribute to the electrical characteristics of the circuit elements. Passive circuit element techniques have been fairly well developed (particularly resistors), and precision tolerances are possible which far surpass the ability of the semiconductor approach. However, to date practical active elements have not been achieved with thin-film techniques, although a number of them have been built in the laboratory. As a consequence, all practical thin-film circuits today are, in reality, hybrid combinations of thin-film passive elements and discrete component add-on devices.

Most thin-film proponents -- and in fact many of the semiconductor proponents -- believe that the day will come when all elements, both active and passive, will be fabricated by thin-film techniques directly. When and if this occurs, thin films should have all of the advantages of semiconductor circuits -- that of low cost and small size combined with high reliability. Additionally, they will be capable of providing precision tolerances such as are required for linear circuit applications and will be able to do so at a design and tooling cost that is substantially less than required for semiconductor circuits or any conventional discrete component approach, including conventional printed circuits.

Semiconductor integrated circuits, on the other hand, are formed by starting with a semiconductor substrate and then forming a multiple combination of N and P regions with their associated junctions by diffusion techniques within the substrate itself, thus forming an array of semiconductor components. Material may also be added on in some fashion (conducting films or small wires) to interconnect the various regions. Special isolation techniques are used to isolate unwanted interaction effects due to the normally conductive substrate.

The fundamental difference between the semiconductor approach and the thin-film approach is the basic material used as the starting point for the formation of the components. The advantage of using a semiconductor base is that it permits the fabrication of active elements, such as transistors and diodes. All other components, however, must also be fabricated from this same semiconductor material. While this material is highly useful in making good active elements, it is a rather poor choice when it comes to fabricating resistors, capacitors, and the other passive elements also needed in the formation of most circuits. As a result, the semiconductor approach to date has been almost exclusively restricted to the digital field, wherein broad component tolerances can be accepted.

Many efforts are being made to extend this technology into the field of linear electronics such as is required for servo amplifiers. Furthermore, in all cases the design and reduction to practice of any circuit utilizing this technique seems to be an extremely expensive process before a useful yield is obtained. Elaborate techniques have therefore been devised for using one standard combination of circuit elements to obtain a variety of circuit functions by merely changing the method of interconnection of these standard elements. Semiconductor circuits have enjoyed considerable research emphasis, based on basic transistor and diode research programs of the semiconductor industry.

The effect of integrated microelectronics on system complexity reduction on a particular system (the present LSI conventional component breadboard control system) is also illustrated in Figure 1. Based on actual component count, a reduction in discrete components from 8000 to 300 can be realized by implementing this digital controller with available semiconductor integrated microelectronics. This reduction in complexity would thus provide a reliability improvement of at least 25.

All thin-film integrated circuits which were not available at the time of this program were not considered further.

Thin-film hybrid microelectronics (thin-film passive with semiconductor chip active elements) are available but are not considered for use in digital systems because of only limited expected improvement in reliability. Improvement could be realized by using thin-film hybrid devices in an analog system, but the barrier at about 0.01 percent accuracy is still present with these devices, with only small improvement in reliability. Thin-film hybrid microelectronics do offer significant improvement in size, weight and power for analog or linear circuits. Improved resistance to radiation effects is also expected through use of thin-film techniques.

In summary, then, it may be concluded that, at present, semiconductor integrated circuits are most applicable to digital systems, and that thin-film hybrid circuits are more applicable to linear or analog applications and to moderate power applications.

All thin-film integrated circuits (with active elements) were still in the research phase, and not available. When and if such components do become available, they will be likely candidates for digital as well as analog applications.

1.2.4 Optimum System and Component Approach

From the foregoing discussion of possible system and component approaches, three major points are outstanding -

a. For system accuracy requirement better than approximately 0.01 percent, analog control systems are not technically possible.

b. Semiconductor integrated microelectronics can improve system reliability by a factor from 25 to 100 over that possible with conventional discrete components.

c. Digital systems are the most feasible application for semiconductor integrated microelectronics.

Based on these three considerations alone, the optimum approach to the reliability and accuracy problem for future spacecraft control systems is a digital system implemented with semiconductor integrated microelectronics.

1.2.5 Summary of Advantages of Selected Approach

Thus far only the accuracy and reliability considerations have been considered, and a system and component selection based on these has been discussed. There are other significant advantages which can be realized for a spacecraft stabilization and control system using the digital semiconductor microelectronics approach. All of the expected advantages are summarized as follows:

a. Reliability

Improvement over conventional electronics by a factor of from 25 to 100. The reliability considerations have been covered in detail in the previous discussion.

b. Accuracy

No fundamental limit. Accuracy of several orders better than best analog systems are presently possible. The accuracy considerations have been discussed in the previous sections.

c. Reduction in Vehicle Wiring

Data handling in serial form requires only single leads. Time sharing of leads is feasible both for signals within control system and with other on-board digital systems.

d. Compatibility with Communications System

Command information and data output information are in digital form. A digital control system will make direct tie-in to telemetry system without D/A conversion.

e. Central Computer Utilization

Digital system can use some elements for several purposes by time sharing. Consolidation of arithmetic operations can be done easily within control system or can be performed in central computer shared with other on-board systems.

f. Adaptive Control Compatibility

In a digital control system, parameters can be readily varied automatically to provide optimum spacecraft response.

g. Compatibility with Quantized Actuators

Reaction jet actuators are bi-stable devices. Pulse width modulation and/or pulse rate modulation can most easily be done digitally for stabilization and control systems of all accuracies.

h. Flexibility

With a relatively few basic system elements such as registers and gates, a variety of operations can be performed by changing inputs and re-routing signals. This is possible because all data are in a compatible numerical form. For instance, the same element can accept and process data words which in one mode may be a velocity command and in another may be a position command.

i. Redundancy Capability

In addition to reliability improvement inherent with semiconductor microelectronics, a digital system can incorporate redundant techniques easily. One space register, for instance, can be switched to many different locations as required to replace an identical unit which has malfunctioned.

j. Alternate Operation Capability

In the event of a component or element malfunction, alternate modes of operation can be commanded easily in a digital system such that a spacecraft mission can be continued with reduced accuracy or perhaps over a more limited range.

k. Size

Compared to conventional electronics, a 30-to-1 reduction in size will be realized by using semiconductor integrated microelectronics in a digital control system.

l. Weight

Compared to conventional electronics, a 6-to-1 reduction in weight will be realized by using semiconductor integrated microelectronics in a digital control system.

m. Power

Compared to conventional electronics, a 10-to-1 reduction in power requirements will be realized by using semiconductor integrated microelectronics.

1.3 THE EXPERIMENTAL SYSTEM

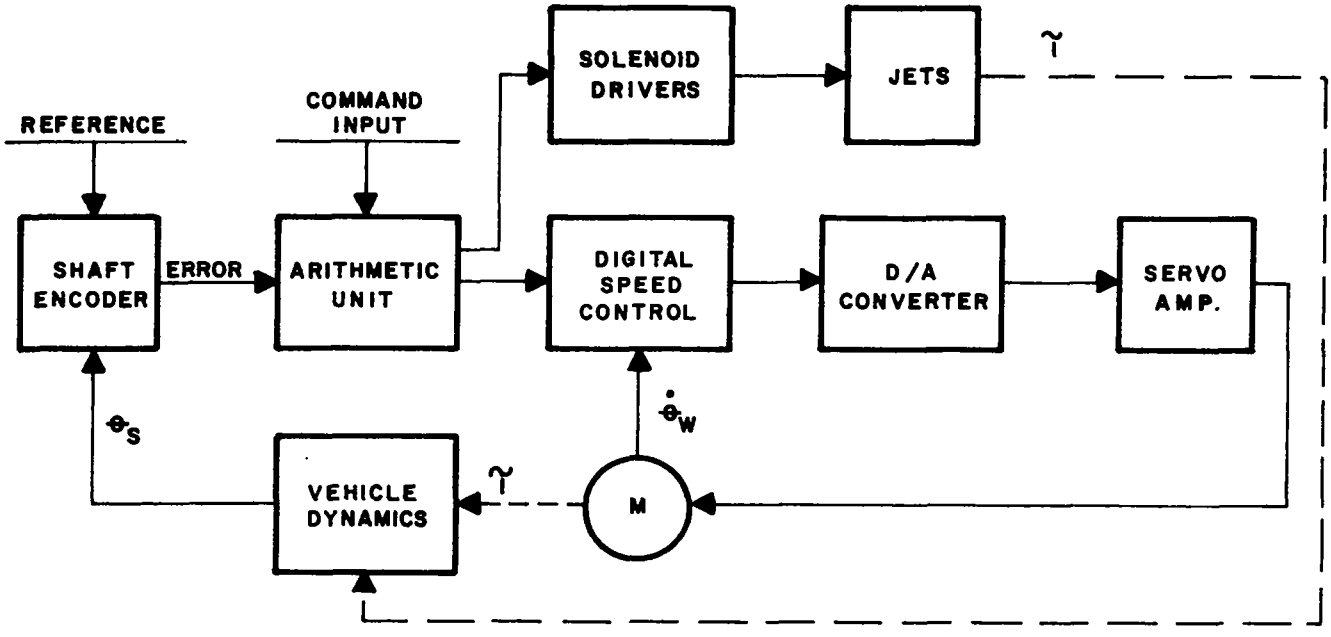
A basic integral plus proportional system was chosen as the experimental tool for this study. Since the response of such a system is well known, experimental data could be quickly evaluated as the study progressed. A block diagram of the overall system is shown in Figure 2.

This is a synchronous system utilizing an external clock for timing. The arithmetic unit accepts digital commands in either a velocity or displacement mode. In the displacement mode, the command is compared to digital displacement feedback via the encoder. The resulting error is both integrated and multiplied by a damping factor. The two results are then summed. The final number is applied to the speed control unit through an output buffer and rate multiplier which has an output pulse train of a frequency proportional to the desired wheel velocity.

The speed control unit uses operational digital techniques to compare the command frequency with a velocity feedback pulse train from the wheel. The result of this comparison is a number in the speed control register which, by digital-to-analog conversion, is applied to a servo amplifier and thence to the wheel.

Momentum dumping is achieved by observing that the number stored in the integrator register is proportional to stored wheel momentum. When a preselected number is detected in this register, reaction jet controls are actuated to dump the stored momentum.

The arithmetic unit of this system is a special purpose serial computer as shown in the detailed block diagram of Figure 12. It is designed for use with a 13 bit shaft encoder. The word length is 16 bits and consists of 12 bits for magnitude, a sign bit, a check bit, and two space bits. The basic clock is 6.25 kc/s. Negative numbers are handled in radix complement form within the unit up to the output register where they are converted to sign and magnitude.



SYSTEM BLOCK DIAGRAM
FIGURE 2

The most significant bit (MSB) of the encoder output is considered a sign bit with binary zero and binary one representing positive and negative signs respectively. The closed, finite, number system of the encoder can then be partitioned between 000 ..... 00 and 111 .... 11 so that numbers in one direction are magnitude and sign while in the opposite direction the number are radix complement and sign.

Since the machine elements are of a finite size, it is possible, during arithmetic operations, to generate numbers which exceed the capacity of some register and thus develop an overflow. Such an overflow can be detected readily by observing the sign bit. If there has been an overflow, the sign bit will be incorrect. For this reason a check bit, which duplicates the sign bit of the incoming data, was introduced at the input of the

machine. These two bits will always be the same unless there is an overflow. In the proportional register and output register any overflow is detected and used to saturate the register in either a positive or negative direction as may be indicated by the state of the check bit. In addition, the output register detects negative numbers and complements the 12 magnitude bits to obtain magnitude and sign. It should be noted that this last operation results in a diminished radix complement and is, therefore, in error by one bit. This small error is of no consequence.

Displacement data is accepted at the input of the arithmetic unit in serial natural binary form, least significant bit first. In the subtracter, feedback data is compared with command data to produce an error number. This number is routed to serial adder #1 and to the proportional register. The proportional register is a bidirectional shift register which accepts the incoming word left to right. During the two space-bit times this word is multiplied by a damping factor which, for convenience, is a power of two. This is accomplished by shifting the word left two bits.

Serial adder #2 and the associated register form an integrator which operates at a sampling rate of approximately one cps. The error number, applied to adder #2, is added continuously to the integrator register contents and the new sum entered into the register. The integrator register thus contains a momentum history of the reaction wheel at any given word time. As has been previously noted it is possible to saturate this register due to its finite size as compared to word lengths which might occur at its input. Since this register and its associated adder form an integrator, control would be lost if the register were allowed to saturate. For this reason the integrator input is limited so that large errors can not possibly fill up the register before the system has reached null.

The contents of the integrator and proportional registers are summed in adder #3 with the sum passing through adder #4 to be entered in the output register. In the displacement mode, adder #4 contributes nothing to the sum since alternate input is zero. The contents of the output register is, therefore, proportional to the desired wheel velocity.

Both the integrator register and the output register are right shift registers. Their contents are, therefore, constantly changing except during space-bit times. The output register, for this reason, can not be used to control parallel level inputs of the rate multiplier. To overcome this, the output register content is gated in parallel into the buffer register each word time.

The binary rate multiplier, sometimes known as a binary operational multiplier, is designed to accept a pulse train at one input, a numeric code at the other, and have as its output a new pulse train containing a number of pulses equal to the product of the two inputs.

In this system, the buffer register output is the numeric code input to the rate multiplier while the other input is a frequency of 12.5 kc/s based on the relation:

f = number of feedback pulses on wheel x maximum wheel rps

The output of the arithmetic unit is then a pulse train with direct scalar relationship to desired wheel velocity.

The speed control unit for the system consists of the logic shown in Figure 16. The command input comes from the rate multiplier and the sign input from the sign bit of the buffer register, both in the arithmetic unit, while the feedback pulse train comes from the reaction wheel.

The anti-coincidence circuitry provides one-bit temporary storage for both the feedback and command pulse trains. The two synchronizers are controlled by the clock such that one is out of phase with the other in passing on incoming data. Since the clock operates the synchronizer output flip-flops at a 100 kc/s rate while incoming data will be at a maximum of 12. 5 kc/s data pulses cannot be lost and possible coincidence of the two inputs is overcome.

The direction control acts simply as a DPDT switch to connect the inputs to the up or down sides of the following counter as directed by the sign bit.

The bidirectional counter acts as a summer to produce, through a weighted resistor D/A converter, an analog voltage of sufficient magnitude to drive the wheel at a speed such that the two input frequencies are exactly the same.

The D/A converter output is unipolar. Therefore, the chopper of the following servo amplifier must be biased to the mid-point of the D/A converter output range to provide bi-directional phasing for the reaction wheel.

It should be noted that the speed control unit is a complete closed-loop system by itself and, as such, has many other applications where precise control of rotary machine velocity is required.

2 DESIGN METHODOLOGY

2.1 OBJECTIVE

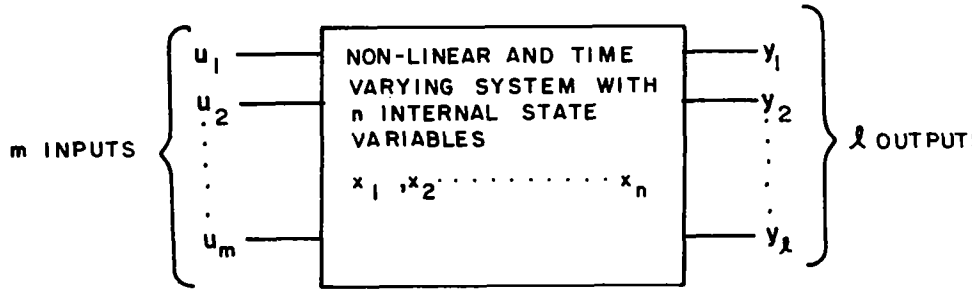
Previous LSI studies had revealed that conventional modeling techniques based on the LaPlace transform were inadequate to describe accurately the performance of the LSI spacecraft simulator. The major objective of the design methodology study, then, was to determine a more accurate modeling technique which would account for the discontinuities, sampling and low-level saturation that was present in the digital control system. If such a model could be obtained, it would be used as a design tool in evaluating the performance of the spacecraft under any proposed control scheme.

This objective was fulfilled. The modeling technique and digital computer simulation are explained in Sections 2.2 and 2.3. In addition, a means of determining the best control, in a restricted sense, was developed for future spacecraft control systems design. A description of this technique is presented in Appendix B.

2.2 THE STATE MODEL

Conventional LaPlace transform techniques approximate each component of a given system by a single n^{th} order linear differential equation. These differential equations are transformed to the s domain and manipulated algebraically to obtain an overall system transfer function. This resulting transfer function is an s domain representation of a single, high-order linear differential equation relating the system output derivatives to the system input and input derivatives. Rather than express the relationship between input and output as a single n^{th} order differential equation, it is often desirable to convert this representation to n first order simultaneous differential equations. Furthermore, if these differential equations are obtained by manipulating the component equations in the time domain, no restriction need be placed on the linearity or time independence of the component models.

This set of simultaneous differential equations with an accompanying set of algebraic equations (output equations) is called the state model and forms the core of the so-called modern control theory.



BASIC SYSTEM MODEL
FIGURE 3

In the general non-linear, time varying case with multiple inputs and outputs (Figure 3, above), the state model will be of the form:

$$\frac{d}{dt}\begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_n \end{bmatrix} = \begin{bmatrix} f_1\,(X_1,\ X_2\ ---\ X_n,\ U_1,\ ---\ U_m,\ t) \\ f_2\,(X_1,\ X_2\ ---\ X_n,\ U_1,\ U_2\ ---\ U_m,\ t) \\ \vdots \\ f_n\,(X_1,\ X_2\ ---\ X_n,\ U_1,\ U_2\ ---\ U_m,\ t) \end{bmatrix}$$

$$\begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_n \end{bmatrix} = \begin{bmatrix} g_1\,(X_1,\ X_2\ ---\ X_n,\ U_1,\ U_2\ ---\ U_m,\ t) \\ g_2\,(X_1,\ X_2\ ---\ X_n,\ U_1,\ U_2\ ---\ U_m\ t) \\ \vdots \\ g_n\,(X_1,\ X_2\ ---\ X_n,\ U_1,\ U_2\ ---\ U_m,\ t) \end{bmatrix}$$

or in shorthand column matrix (vector) notation,

$$\dot{\underline{X}} = f(\underline{X}, \underline{U}, t)$$

$$\underline{Y} = g(\underline{X}, \underline{U}, t)$$

If the system of Figure 3 is linear and time stationary (hence LaPlace transformable) with a single input and output, the state model reduces to the form:

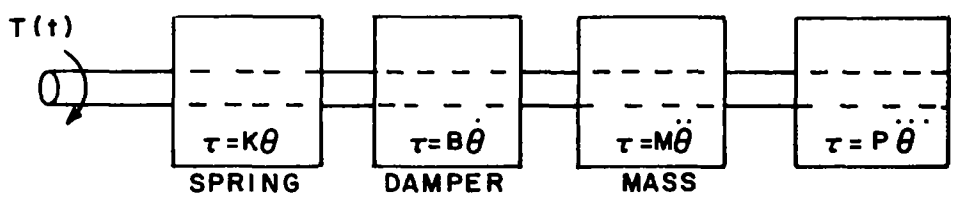
$$\dot{\underline{X}} = \underline{A}\underline{X} + \underline{B}u_1$$

$$Y_1 = \underline{C}\underline{X} + \underline{D}u_1$$

where A, B, C, and D are constant matrixes. In this form, the state model offers little advantage over conventional s domain transfer functions in obtaining analytical solutions. Frequency response, stability, etc. are obtained with about the same facility in the time domain as in the s domain.

Example 1

Consider the following linear, time stationary system:



LINEAR, TIME STATIONARY SYSTEM
FIGURE 4

where

θ = shaft position

τ = torque

K, B, M and P = constants (time stationary)

T(t) = applied torque

The single differential equation describing this system is:

$$P\dddot{\theta} + M\ddot{\theta} + B\dot{\theta} + K\theta = T(t)$$

Solving for the highest order derivative;

$$\dddot{\theta} = \frac{T(t)}{P} - \frac{M\ddot{\theta}}{P} - \frac{B\dot{\theta}}{P} - \frac{K\theta}{P}$$

Let:

$$x_1 = \ddot{\theta} = \frac{d^2\theta}{dt^2}$$

$$x_2 = \dot{\theta} = \frac{d\theta}{dt}$$

$$x_3 = \theta$$

then,

$$\frac{dx_1}{dt} = \frac{T(t)}{P} - \frac{Mx_1}{P} - \frac{Bx_2}{P} - \frac{Kx_3}{P}$$

$$\frac{dx_2}{dt} = x_1$$

$$\frac{dx_3}{dt} = x_2$$

Rewriting this in matrix form and selecting the output y as the shaft position,

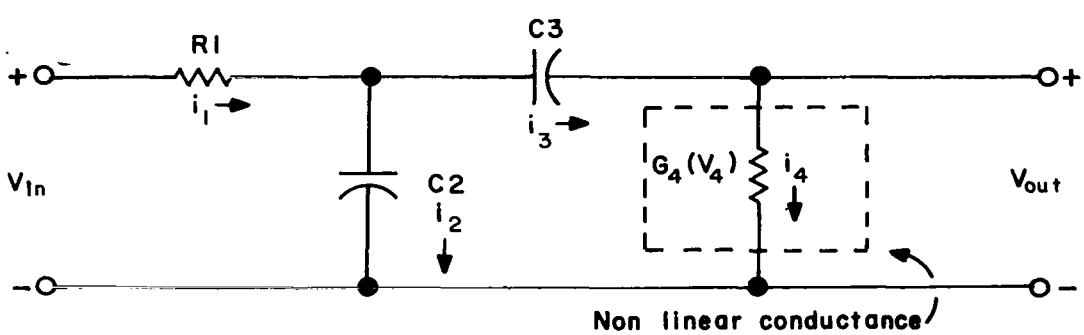
$$\frac{d}{dt}\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} -\frac{M}{P} & -\frac{B}{P} & -\frac{K}{P} \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} \frac{1}{P} \\ 0 \\ 0 \end{bmatrix} T(t)$$

$$y = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}$$

This is a state model of Figure 4.

Example 2

Consider the following non-linear electrical network:



$$i_1 = \frac{V_1}{R_1}$$

$$i_4 = G_{4a} V_4 + G_{4b} V_4^2$$

$$\frac{dV_2}{dt} = \frac{1}{C_2} i_2$$

$$\frac{dV_3}{dt} = \frac{1}{C_3} i_3$$

Substituting;

$$i_2 = i_1 - i_4 = \frac{V_1}{R_1} - G_{4a} V_4 - G_{4b} V_4^2$$

$$i_3 = i_4 = G_{4a} V_4 + G_{4b} V_4^2$$

$$V_1 = V_{in} - V_2$$

$$V_4 = V_2 - V_3$$

Therefore,

$$\frac{dV_2}{dt} = \frac{1}{C_2} \left[\frac{V_{in} - V_2}{R_1} - G_{4a} (V_2 - V_3) - G_{4b} (V_2 - V_3)^2 \right]$$

$$\frac{dV_3}{dt} = \frac{1}{C_3} \left[G_{4a} (V_2 - V_3) + G_{4b} (V_2 - V_3)^2 \right] .$$

The complete state model (for Example 2) is:

$$\frac{d}{dt}\begin{bmatrix} V_2 \\ \\ V_3 \end{bmatrix} = \begin{bmatrix} \frac{-1}{C_2}\left[\frac{V_2}{R_1} + G_{4a}(V_2 - V_3) + G_{4a}(V_2 - V_3)^2\right] \\ \\ \frac{1}{C_3}\left[G_{4a}(V_2 - V_3) + G_{4b}(V_2 - V_3)^2\right] \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{C_2 R_1} \\ \\ 0 \end{bmatrix}$$

$$V_{out} = V_2 - V_3 = \begin{bmatrix} 1 & -1 \end{bmatrix} \begin{bmatrix} V_2 \\ V_3 \end{bmatrix}$$

. . .

It is always possible to obtain a state model from a transfer function. The converse is true if the system is linear and time stationary. For any transfer function,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a_n s^{n-1} + a_{n-1} s^{n-2} \cdots\cdots a_1}{s^n + b_n s^{n-1} \cdots\cdots\cdots\cdots b_1} + K,$$

one equivalent state model is given by:

$$\frac{d}{dt}\begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_{n-1} \\ x_n \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 & 0 \\ 0 & 0 & 1 & \cdots & 0 & 0 \\ \vdots & & & & & \vdots \\ 0 & 0 & 0 & \cdots & 0 & 1 \\ -b_1 & -b_2 & -b_3 & \cdots & b_{n-1} & -b_n \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \\ x_{n-1} \\ x_n \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \\ 0 \\ 1 \end{bmatrix} V_{in}(t)$$

$$V_{out}(t) = \begin{bmatrix} a_1 & a_2 & \cdots & a_{n-1} & a_n \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \\ x_{n-1} \\ x_n \end{bmatrix} + KV_{in}(t)$$

The reverse operation is accomplished by simply taking the LaPlace transform of the state model and performing the necessary matrix algebra.

Classical and modern control theory differ primarily in the manner by which the corrective feedback signal is generated. Classical theory requires linear feedback; modern theory does not. In many instances a non-linear controller is far superior to any linear counterpart, as for example, the time optimal "bang-bang" controller. Since the transfer function representation of the plant (fixed components) does not permit the evaluation of non-linear feedback, a state model of the plant is invaluable in investigating <u>all</u> types of feedback.

A number of other advantages of the state model are considered here;

a. The initial conditions of the dynamic elements appear explicitly in the model.

b. The model is in a form that is amenable to either analog or digital computation.

c. The physical structure of the system is apparent from the model.

d. Sampling may be included by converting the differential equations to difference equations.

e. The general modeling technique is not restricted to time stationary, linear systems.

f. The general form of the model is directly applicable to Liapunov stability studies.

2.3 LSI SPACECRAFT SIMULATION MODEL

The s domain block diagram of the LSI spacecraft simulator (with zero initial conditions) is given in Figure 5. This model, as was pointed out earlier, does not adequately describe the system performance. It does, however, serve as an excellent vehicle for explanation.

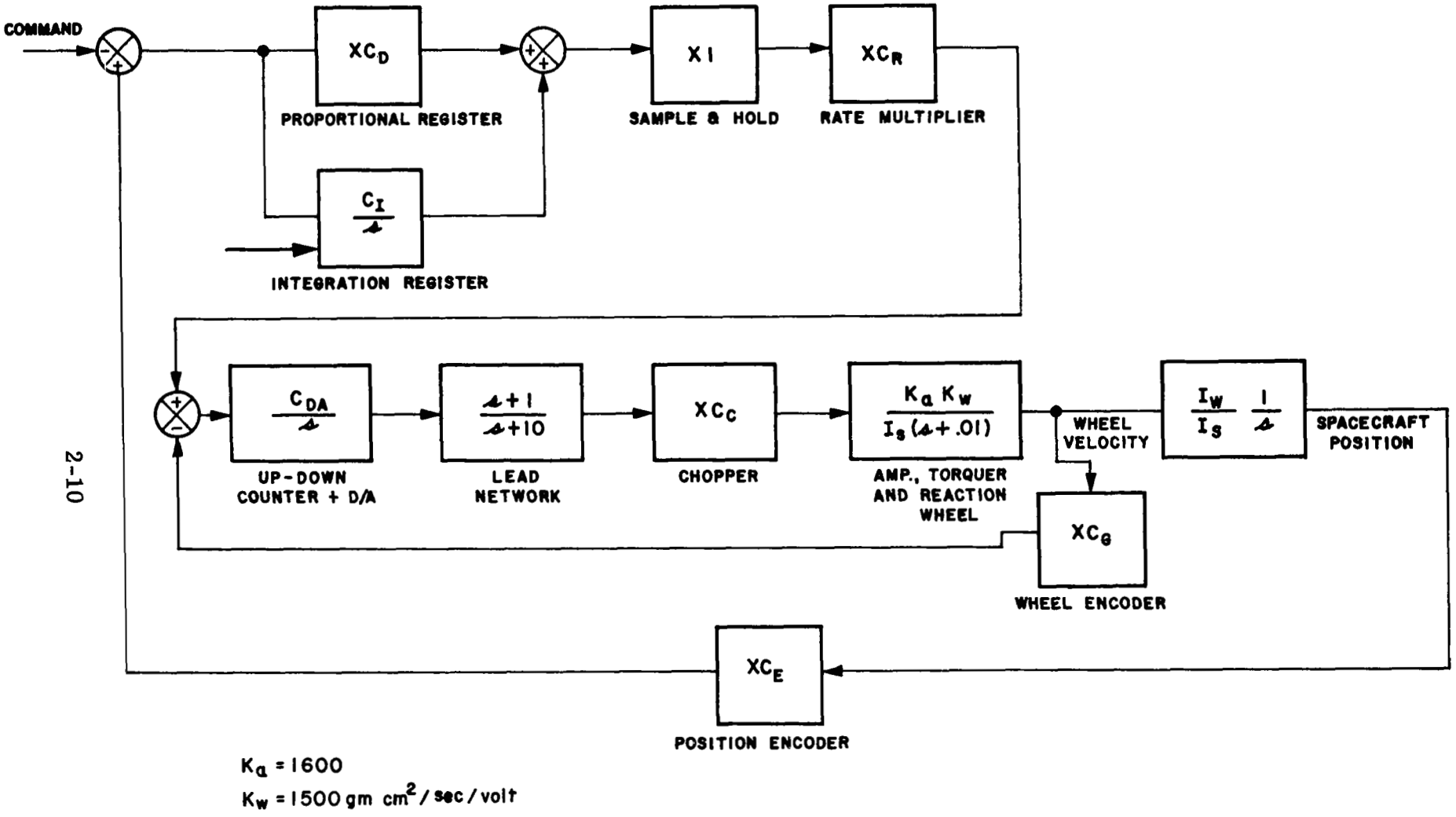
Figure 6 shows the time domain, non-linear state model corresponding to the approximate transfer functions given in Figure 5.

After performing the algebraic substitution indicated by the interconnection of the components, the following non-linear system model was obtained:

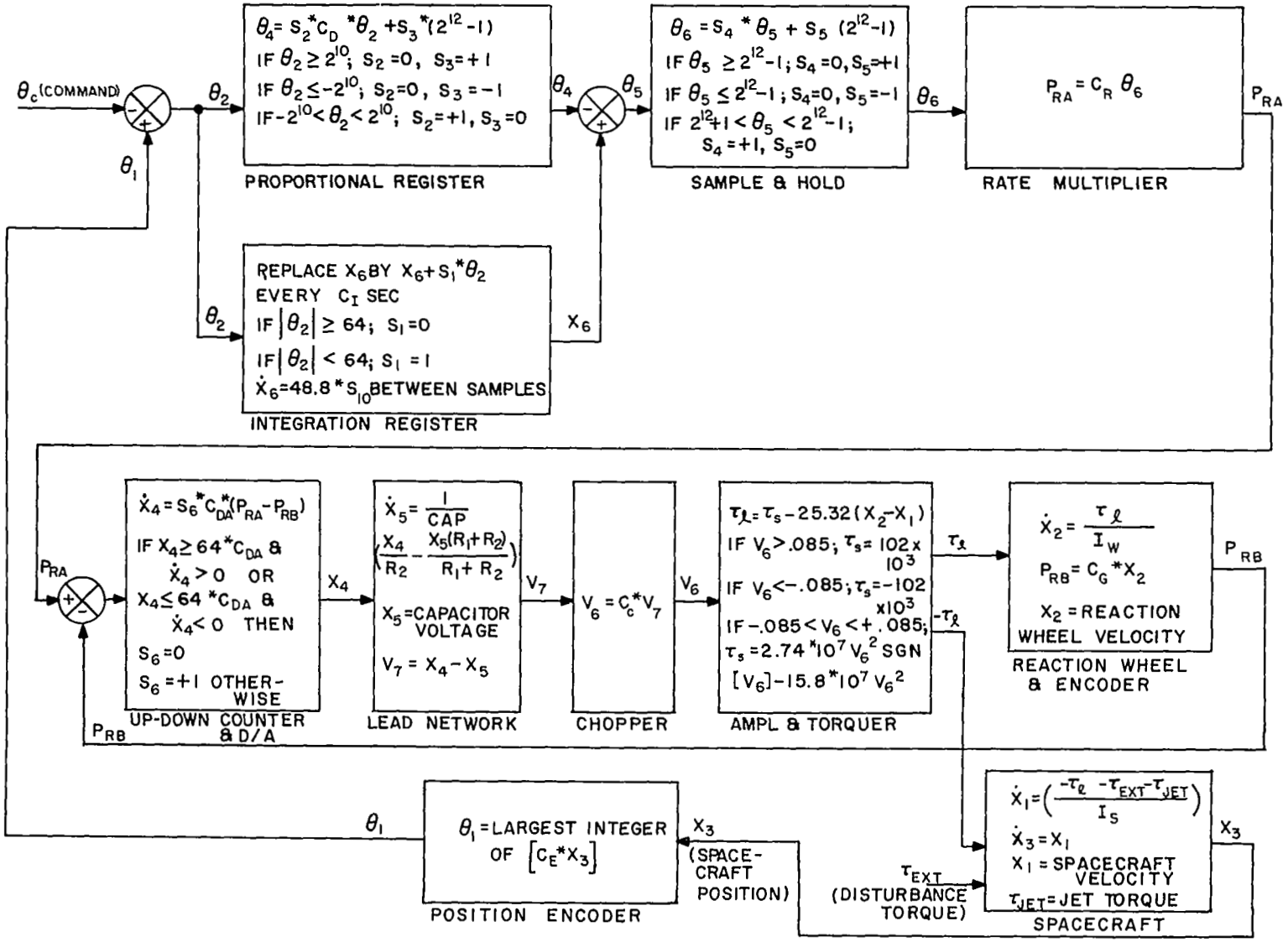
$$\frac{d}{dt}\begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \\ X_6 \end{bmatrix} = \begin{bmatrix} \frac{1}{I_S} - T_L - T_{EXT} - S_7 \frac{I_W C_R 48.8}{C_G} \\ \frac{1}{L_W} (T_L) \\ X_1 \\ S_6 C_{DA} (PRA - PRB) \\ \frac{X_4}{R_2 C} - \frac{X_5}{C} \frac{R_1 + R_2}{R_1 R_2} \\ S_{10} 48.8 \end{bmatrix}$$

where

$$T_L = S_8 \left\{ 2.74 \times 10^7 \left[C_c (X_4 - X_5) \right]^2 \operatorname{sgn} \left[C_c (X_4 - X_5) \right] - 15.8 \times 10^7 \left[C_c (X_4 - X_5) \right]^3 \right\} + S_9 (102. \times 10^3) - 25.32 (X_2 - X_1)$$



S-DOMAIN BLOCK DIAGRAM - LSI SIMULATOR SYSTEM
FIGURE 5



TIME-DOMAIN, NON-LINEAR MODEL - LSI
SIMULATOR SYSTEM
FIGURE 6

$$PRA = C_R \left\{ S_4 \left[S_2 \; C_D \; (C_e^* \; X_3^* - \theta_c) + S_3 (2^{12} - 1) + X_6 \right] + S_5 (2^{12} - 1) \right\}$$

$$PRB = C_G \, X_2 .$$

The above equation is defined for $t = \tau + n C_I$ where $n = 0, 1, 2, \ldots\ldots$ and $0 < \tau < C_I$. At $t = n C_I$, the integrator register output X is modified in accordance with the following difference equation:

$$X_6 \Big|_{t = n C_I +} = X_6 \Big|_{t = n C_I -} + S_1^* (C_E^* \; X_3^* - \theta_C).$$

where

X_1 = spacecraft velocity

X_2 = reaction wheel velocity

X_3 = spacecraft position

X_4 = digital speed control output = $S_{13} \int \dot{X}_4 \, dt + S_{14} \; (64 \; C_{DA})$

X_5 = capacitor voltage of lead network

X_6 = integrator register output

$\text{sgn} \left[C_c \; (X_4 - X_5) \right]$ = sign of $C_c \; (X_4 - X_5)$

$C_E^* \; X_3^*$ = largest integer in $(C_E \; X_3)$

T_{EXT} = external torque (must be specified)

θ_c = spacecraft position command

C_c = $\frac{1}{2\sqrt{2}}$ volts/volt, chopper gain

C_R = 3.05 bits/sec/bit, rate multiplier gain

C_G = 7.962 bits/rad, wheel pickoff gain

I_S = 3330×10^4 gm-cm^2, spacecraft inertia

I_W = 3670 gm-cm^2, wheel inertia

C_{DA} = 0.033 volts/bit, D/A converter gain

C_D = 4 bits/bit, shift register gain

C_E = 1304 bits/radian, encoder gain

C = 6 μfd, lead network capacitance

R_1 = 180K ohms, lead network resistance

R_2 = 20K ohms, lead network resistance

C = 0.763 second, integrator sampling period

S_1 = 0 for $|\theta_2| \geq 64$; where $\theta_2 = (C_E^* \; X_3^* - \theta_c)$

S_1 = +1 for $|\theta_2| < 64$

S_1 = 0 whenever system is operated in velocity mode

$$\left.\begin{aligned} S_2 &= 0 \\ S_3 &= +1 \end{aligned}\right\} \quad 2^{10} \leq \theta_2$$

$$\left.\begin{aligned} S_2 &= 0 \\ S_3 &= -1 \end{aligned}\right\} \quad \theta_2 \leq -2^{10}$$

$$\left.\begin{aligned} S_2 &= 1 \\ S_3 &= 0 \end{aligned}\right\} \quad |\theta_2| < 2^{10}$$

$$\left.\begin{array}{l} S_4 = 0 \\ S_5 = +1 \end{array}\right\} \quad \left(2^{12} - 1\right) \leq \theta_5$$

where $\theta_5 = X_6 + D_2 \; C_D \; \theta_2 + S_3 \; (2^{12} - 1)$

$$\left.\begin{array}{l} S_4 = 0 \\ S_5 = -1 \end{array}\right\} \quad \theta_5 \leq -2^{12} + 1$$

$$\left.\begin{array}{l} S_4 = +1 \\ S_5 = 0 \end{array}\right\} \quad \left|\theta_5\right| < 2^{12} - 1$$

$S_6 = 0 \qquad X_4 \geq (64 \; C_{DA})$ and $(PRA-PRB) < 0$

$S_6 = 0 \qquad X_4 \leq (-64 \; C_{DA})$ and $(PRA-PRB) > 0$

$S_6 = +1$ otherwise

where $PRA = C_R \left[S_4 \; \theta_5 + S_5 \; (2^{12} - 1)\right]$

$PRB = C_G \; X_2$

$S_7 = +1$ If: $|\theta_2| < 64$ and $|X_4| < (64 \; C_{DA})$ and $X_6 \geq 3072$. When this condition is satisfied, S_7 will remain +1 until $|\theta_2| < 64$ and $|X_4| \leq (64 \; C_{DA})$ and $X_6 = 0$, at which time $S_7 = 0$.

$S_7 = -1$ If: $|\theta_2| < 64$ and $|X_4| \leq (64 \; C_{DA})$ and $X_6 \leq -3072$. When this condition is satisfied, S_7 will remain -1 until $|\theta_2| < 64$ and $|X_4| < (64 \; C_{DA})$ and $X_6 = 0$, at which time $S_7 = 0$.

$S_7 = 0$ otherwise.

$$\left.\begin{array}{l} S_8 = 0 \\ S_9 = +1 \end{array}\right\} \quad .085 \leq C_c \; (X_4 - X_5)$$

$$\left.\begin{array}{l} S_8 = 0 \\ S_9 = -1 \end{array}\right\} \quad C_c \; (X_4 - X_5) \leq -.085$$

$$\left.\begin{array}{l} S_8 = +1 \\ S_9 = 0 \end{array}\right\} \quad \left| C_c \ (X_4 - X_5) \right| < .085$$

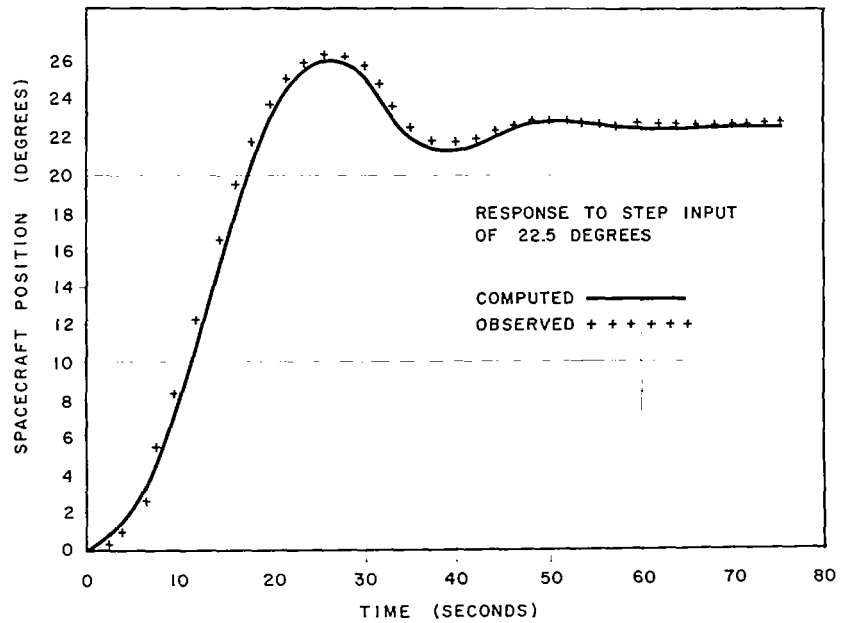
$S_{10} = +1$ If: $|\theta_2| \geq 64$ and $|X_4| \leq (64\ C_{DA})$ and $\theta_2 > 0$ <u>or</u> $|\theta_2| \leq 64$ and $|X_4| \leq (64\ C_{DA})$ and $X_6 < -3072$. If this second condition is satisfied, S_{10} will remain +1 until $X_6 = 0$ or until $|X_4| \geq (64\ C_{DA})$.

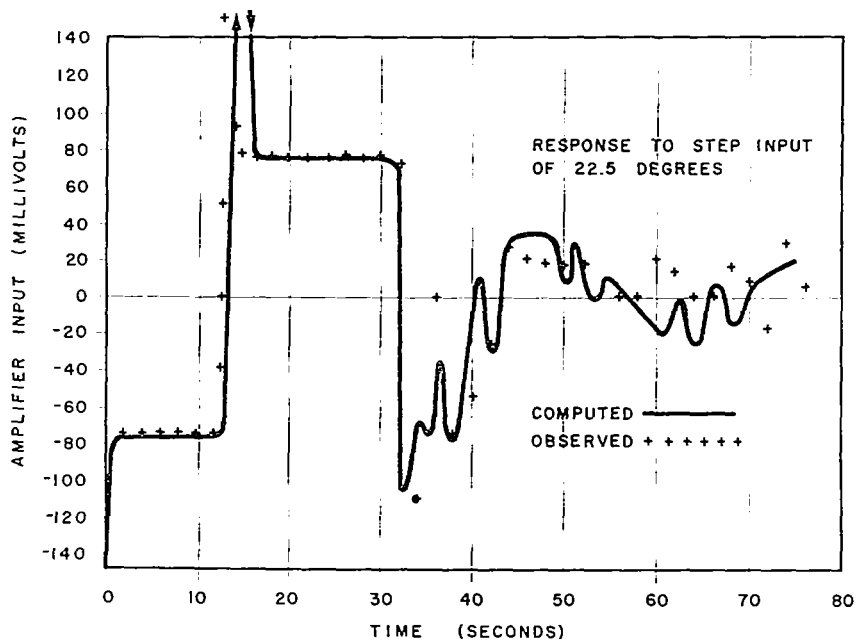
$S_{10} = -1$ If: $|\theta_2| \geq 64$ and $|X_4| \leq (64\ C_{DA})$ and $\theta_2 < 0$ <u>or</u> $|\theta_2| \leq 64$ and $|X_4| \leq (64\ C_{DA})$ and $X_6 \geq 3072$. If this second condition is satisfied, S_{10} will remain -1 until $X_6 = 0$ or until $|X_4| \geq (64\ C_{DA})$.

$S_{10} = 0$ otherwise.

These non-linear equations were solved on an IBM 1620 computer using a fourth order Runge-Ketta numerical integration technique. The logic chart and Fortran computer program are included in Appendix C.

The accuracy of the simulation has been verified by numerous comparisons with the actual performance of the LSI air bearing simulator. Figure 7 displays the results of one typical comparison.





DIGITAL CONTROLLER RESPONSE - COMPUTED AND OBSERVED
FIGURE 7

2.4 SYSTEM LOGIC DESIGN

Given a general system data flow diagram (Figure 8) and the functional arithmetic requirements, the first decision to be made was whether to use serial or parallel arithmetic. In this case, the selection was not difficult. The system time constants were relatively long, so high speed computation was not required. Serial computation uses less hardware than parallel methods; this made the serial mode of operation an obvious choice.

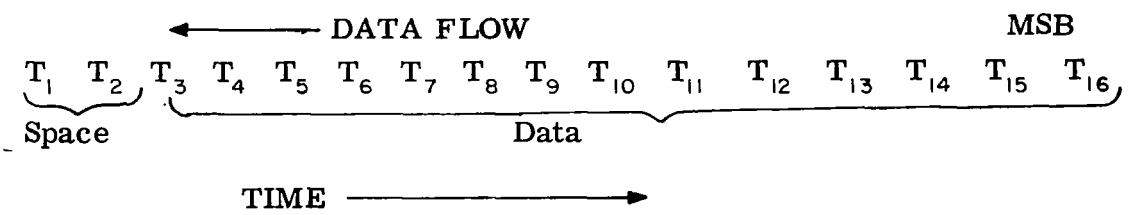
2.4.1 Word Length and Rate

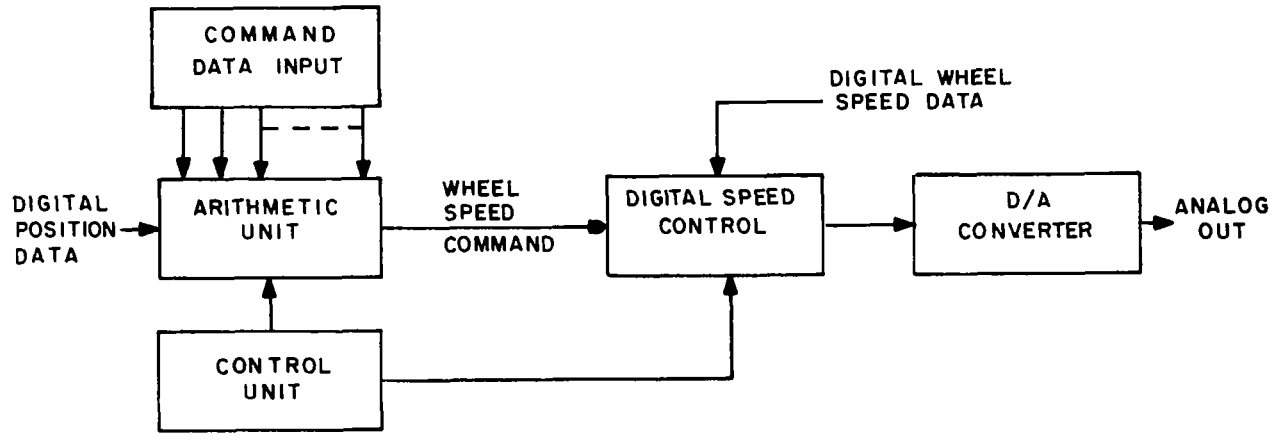
A word length was next determined. The encoder data was 13 bits in length. The most significant bit would be used as a sign with binary "1" being negative and binary "0" positive. This choice of sign definition automatically provided radix (2's) complement data from the encoder for negative numbers and greatly simplified arithmetic functions. As all registers are of finite length, the possibility of overflow exists whenever two numbers are added, subtracted, or multiplied. A simple means of detecting an overflow is to duplicate the sign bit from the encoder and the command register, calling it a check bit. This check bit can be carried along as the most significant bit and be compared continuously with the next most significant bit (sign). If these two bits ever differ, an overflow has occurred and appropriate action may be taken to correct the register content. This technique was used for the sytem. With the data length determined as 14 bits, the system word length was set at 16 bits to provide two bit times for overflow detection and correction, multiplication by left shifting, parallel data transfer at input and output, and such other operations as might be found necessary.

Without regard for optimization, a word rate of 400 cps was chosen as approaching continuous system operation. Using a 16-bit word length, the clock frequency for a 400 cycle word rate would be 6400 cycles. With a 100 kc/s master clock available, 6.25 kc/s was chosen as the nearest count-down frequency to the desired 6.4 kc/s. A four-stage binary divider, Figure 9, was used for this frequency countdown.

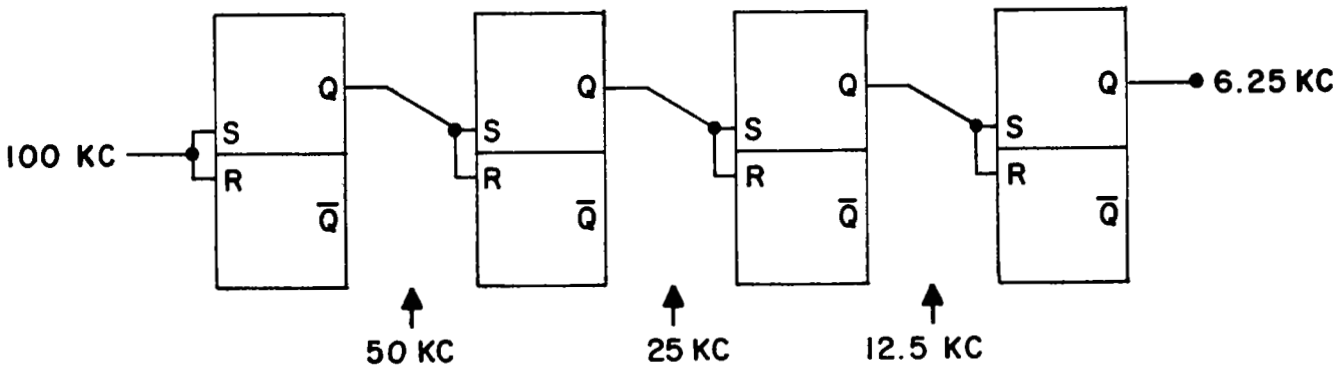
2.4.2 Control Unit

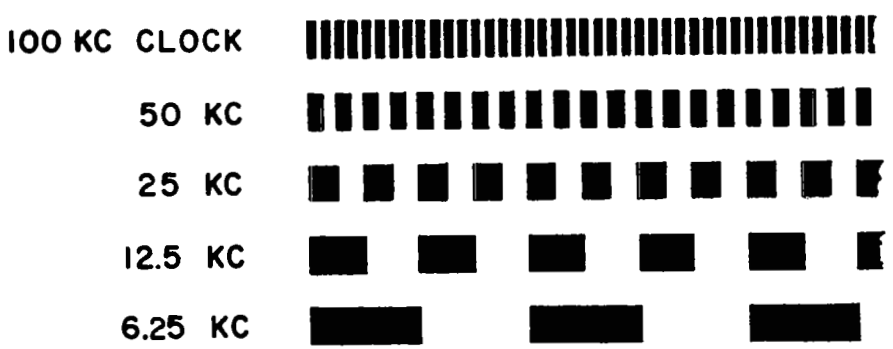
The 16-bit word format was now defined for use in logical design of the control unit and labeled T_1 through T_{16} in this manner:





GENERAL DATA FLOW DIAGRAM
FIGURE 8





MASTER CLOCK DIVIDER AND TIMING
FIGURE 9

This unit actually programs the flow of data, serially, through the system in a repetitive cycle. The system can thus be considered as a special-purpose, serial, stored-program computer.

For control purposes, T_3 through T_{16} must be available to shift data; T_1 and T_2 must be available for gating operations; T_{16} must be available as an end of data indicator; and a gating level which will be ON from T_1 through T_2 time and OFF during T_3 through T_{16} time should be available. The inversion of these control signals might also be required as the system logic develops.

Choice of a 16-bit word length was fortuitous in that a four-stage Modulo 16 index counter could be used as a basis for the control unit. Such a counter with truth tables and Vietch diagrams is shown in Figure 10 where T is the bit time of a word. Strictly from a logic standpoint, the interest was in times T_1, T_2, and T_{16} as separate pulses, while T_3 through T_{16} were to be grouped in a burst for shifting data. The conventional truth table of Figure 10b, when entered in a Vietch diagram, lead to rather complicated gating for T_1, T_2, and T_{16}. Without changing anything physically, a simple redefinition of counter states with regard to T times, as shown in Figure 10c, placed the states of interest in the center of the Vietch diagram and thus permitted simpler logical expressions.

From the later Vietch diagram, it can be seen that T_1 lies in $\bar{A}BCD$ while T_2 lies in ABCD. That is -

$$T_1 = \bar{A}(BCD)$$

$$T_2 = A(BCD).$$

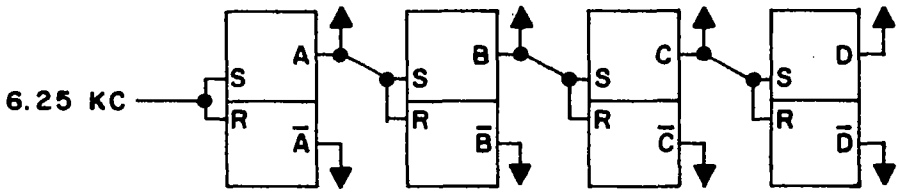
It can also be seen that the parenthesized term BCD covers only the squares containing T_1 and T_2. Therefore, the inversion of this term, $\overline{BCD}$, must cover all other squares, i.e. T_3 through T_{16}, since logically, by DeMorgans Theorem,

$$\overline{BCD} = \bar{B} + \bar{C} + \bar{D} \triangleq T_3 \longrightarrow T_{16} .$$

That this is true can readily be verified by noting, in the truth table, that either B or C or D is zero for all T's from 3 through 16,

T_{16} requires the logical expression

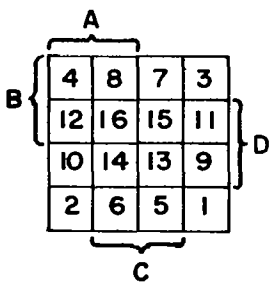
$$T_{16} = A\bar{B}CD = A\bar{B}(CD)$$



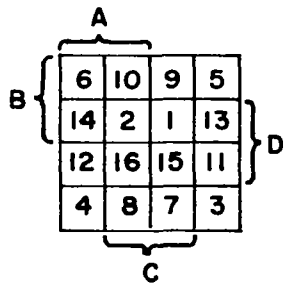
(a)

T		D	C	B	A
1		0	0	0	0
2		0	0	0	1
3		0	0	1	0
4		0	0	1	1
5		0	1	0	0
6		0	1	0	1
7		0	1	1	0
8		0	1	1	1
9		1	0	0	0
10		1	0	0	1
11		1	0	1	0
12		1	0	1	1
13		1	1	0	0
14		1	1	0	1
15		1	1	1	0
16		1	1	1	1

T		D	C	B	A
1		1	1	1	0
2		1	1	1	1
3		0	0	0	0
4		0	0	0	1
5		0	0	1	0
6		0	0	1	1
7		0	1	0	0
8		0	1	0	1
9		0	1	1	0
10		0	1	1	1
11		1	0	0	0
12		1	0	0	1
13		1	0	1	0
14		1	0	1	1
15		1	1	0	0
16		1	1	0	1



(b)

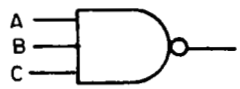


(c)

INDEX COUNTER WITH TRUTH TABLES
AND VIETCH DIAGRAMS
FIGURE 10

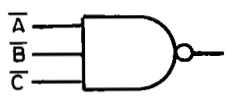
where CD is parenthesized to emphasize that it is a common term in all the gating expressions.

NAND (Sheffer Stroke) logic was chosen to mechanize this system. Typically a NAND (not AND) gate performs the function of an AND gate followed by an inverter such that with, say, three inputs A, B and C, the logical function may be drawn:



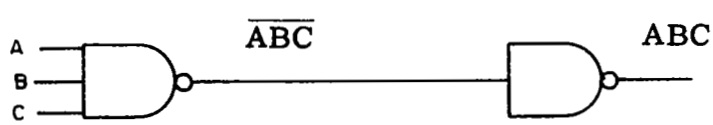
$$X = \overline{ABC} = \bar{A} + \bar{B} + \bar{C}.$$

Observe that, if the inversion of the input variables is available, the OR function is generated; that is,



$$X = \overline{\bar{A}\,\bar{B}\,\bar{C}} = A + B + C.$$

To obtain the AND function, two NAND gates are required:



The second gate effectively removes the bar from the first NAND function. A single input NAND gate, therefore, can be used as an inverter.

Implementation of the control unit gating functions using NAND gates started with the observation that the expression CD appeared in all gating expressions as noted here:

$$T_1 = \bar{A}\left[B(CD)\right]$$

$$T_2 = A\left[B(CD)\right]$$

$$T_{16} = A\left[\bar{B}(CD)\right]$$

$$T_{3\rightarrow 16} = \overline{B\ (CD)}$$

This term, then, would have to be obtained only once since all other expressions could be developed from this term as shown in Figure 11 (where C_p is the 6.25 kc/s clock and LS is a 12.5 kc pulse train from the clock divider, gated with the T_1 term, to provide two left shift pulses during T_1 time).

Using the arithmetic unit logic block diagram of Figure 12 as a guide, other logic elements could now be developed.

2.4.3 Adder/Subtracter

Four serial adders and one subtracter are indicated in the diagram. There are several standard forms of serial adder. With NAND logic the most straightforward technique is to implement the cannonical sum and carry equation:

$$\text{Sum} = A\,\bar{B}\,\bar{C} + \bar{A}\,B\,\bar{C} + \bar{A}\,\bar{B}\,C + A\,B\,C$$

$$\text{Carry} = AB + BC + CA$$

where

A = augend

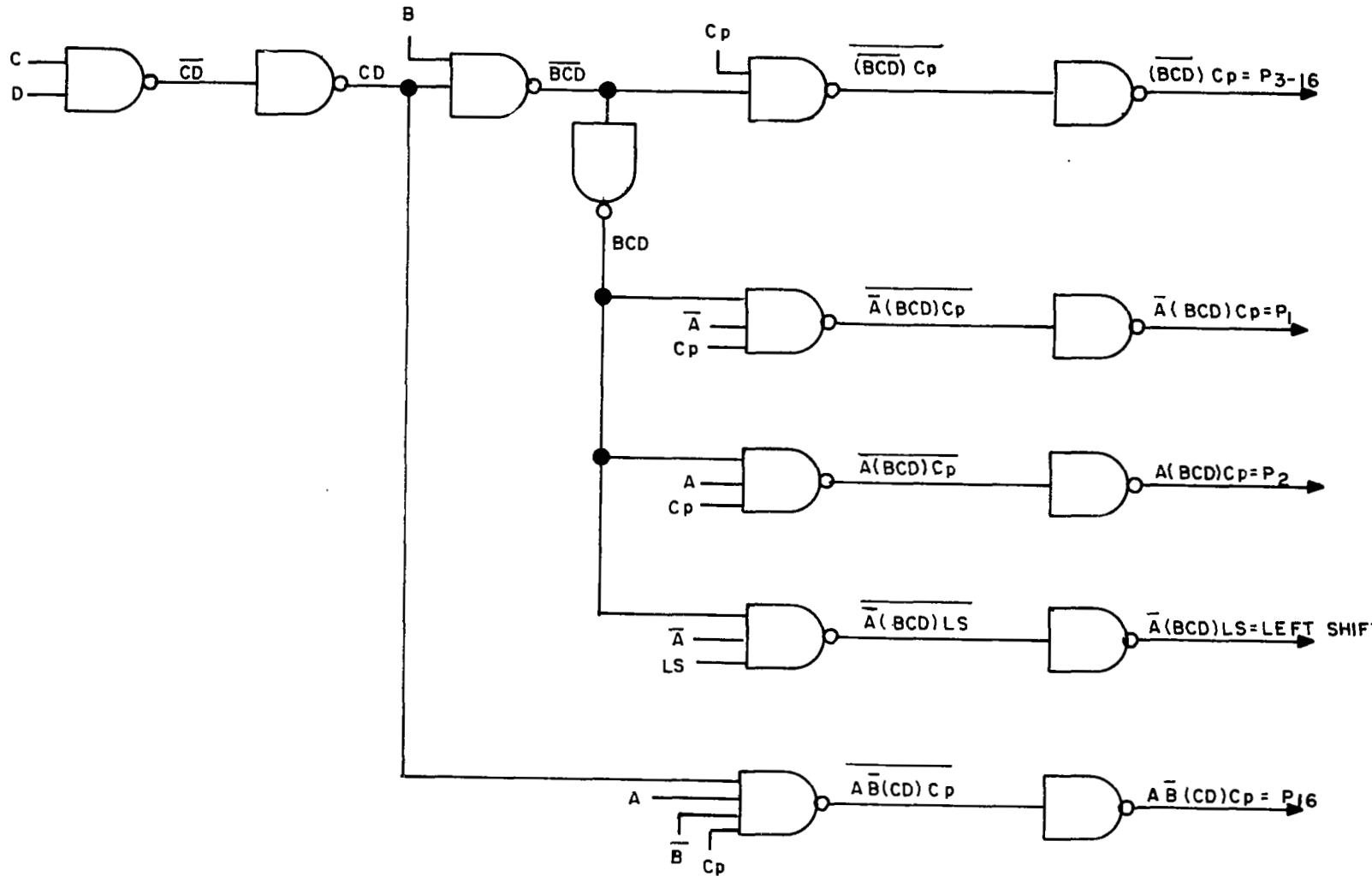
B = addend

C = carry from previous bit additions as shown in Figure 13,

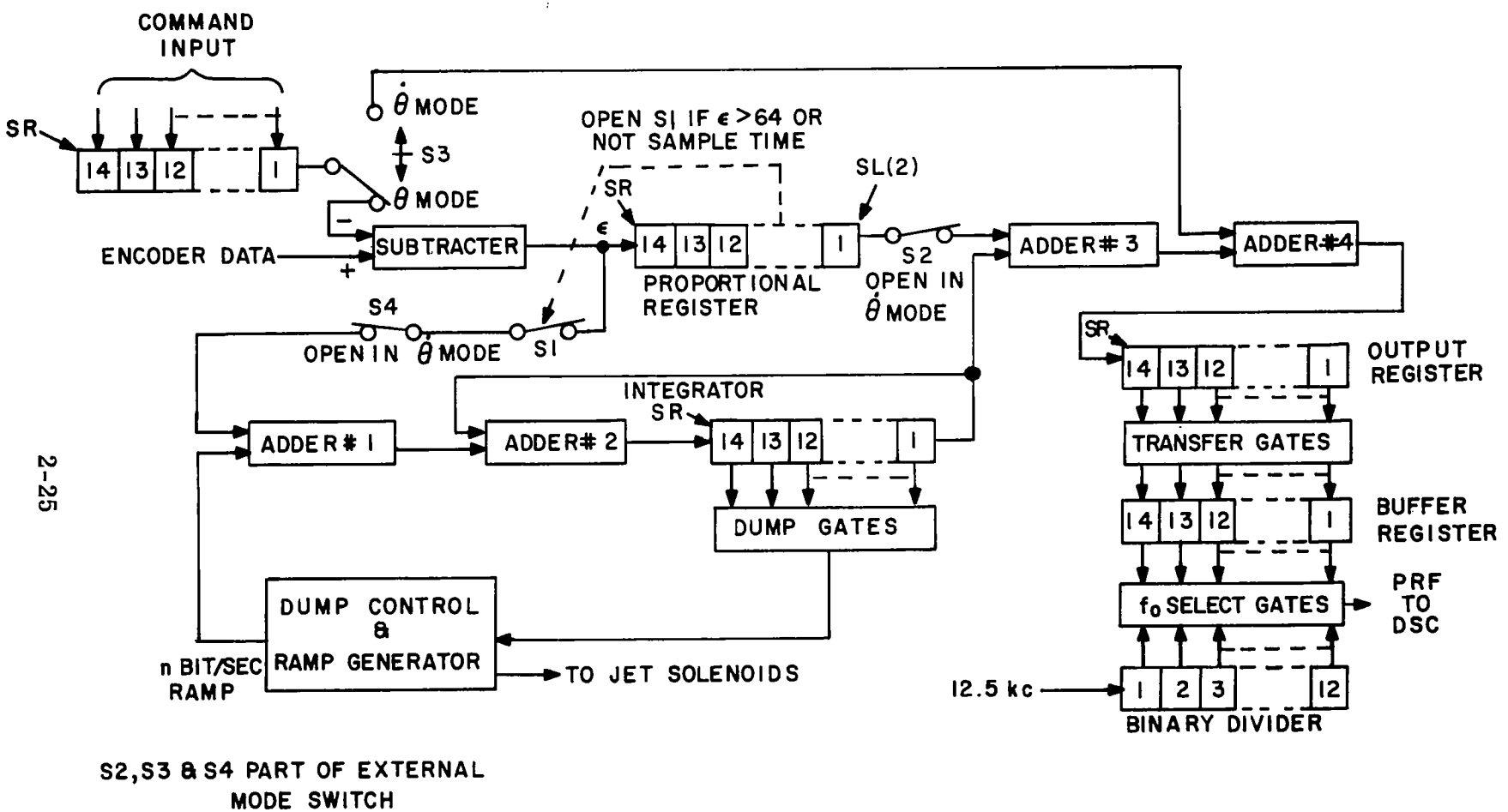
A subtractor differs from an adder only in implementation of the borrow. The difference equation is exactly the same as the sum equation. By proper connection of the X line in the logic of Figure 13, the logic will either add or subtract.

For subtraction, let:

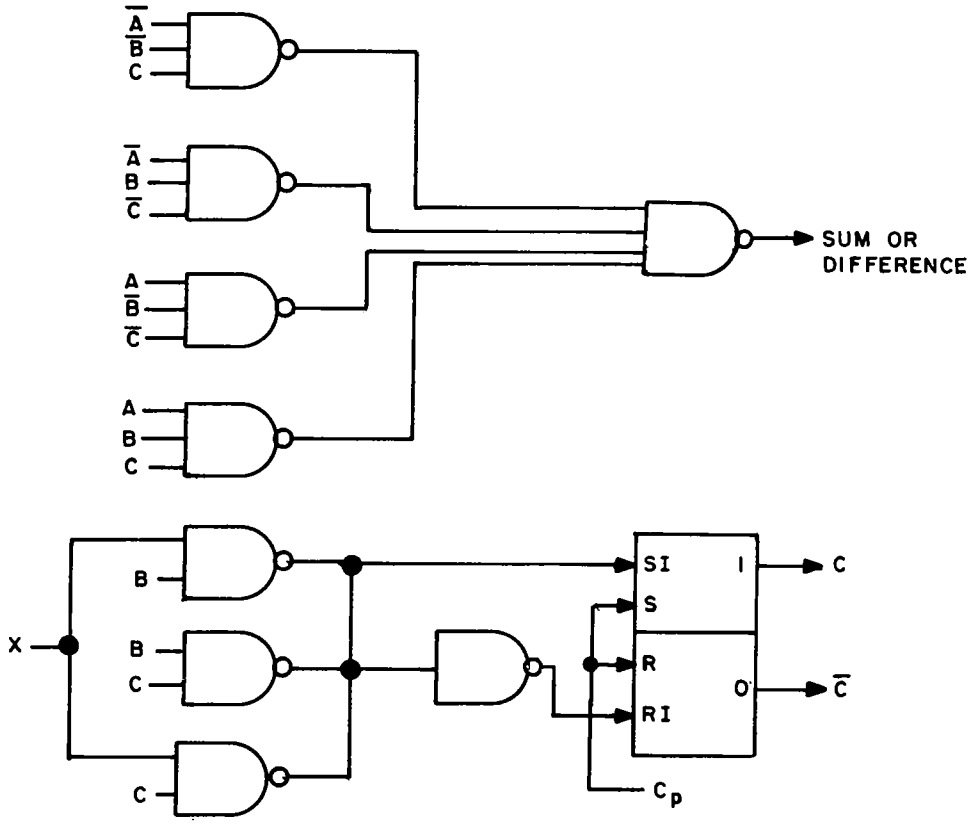
A = minuend,



CONTROL LOGIC DIAGRAM
FIGURE 11



ARITHMETIC UNIT LOGIC BLOCK DIAGRAM
FIGURE 12



FOR ADDER

A = AUGEND

B = ADDEND

X = A

C_p = CLOCK PULSE

C = CARRY (n-1)

FOR SUBTRACTER

A = MINUEND

B = SUBTRAHEND

X = $\overline{A}$

C_p = CLOCK PULSE

C = BORROW (n-1)

SERIAL ADDER/SUBTRACTER LOGIC DIAGRAM
FIGURE 13

B = subtrahend, and

C = borrow.

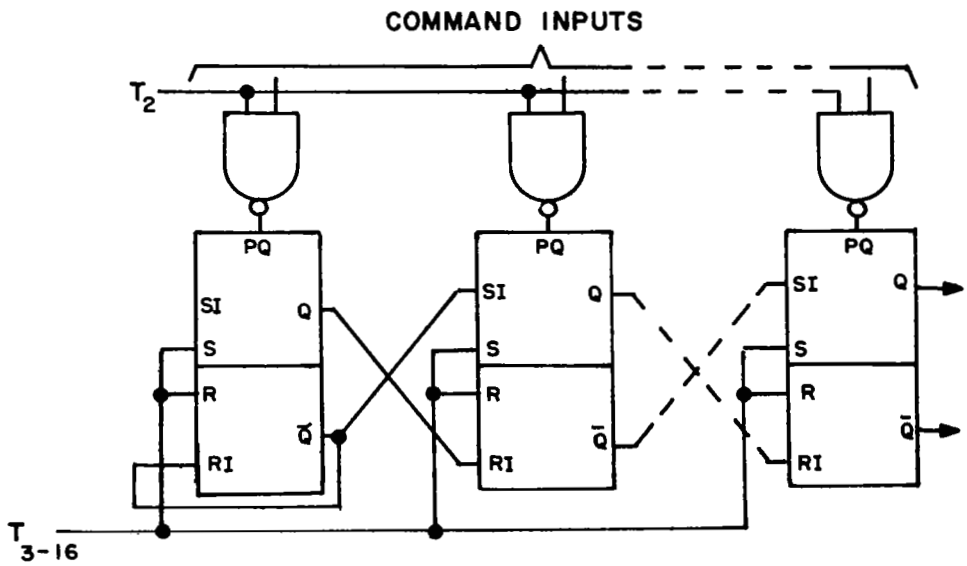
Then the borrow equation will be:

$$\text{Borrow} = \bar{A}B + \bar{A}C + BC$$

This circuit was used to implement the five adder-subtracter blocks of the system.

2.4.4 Command Register

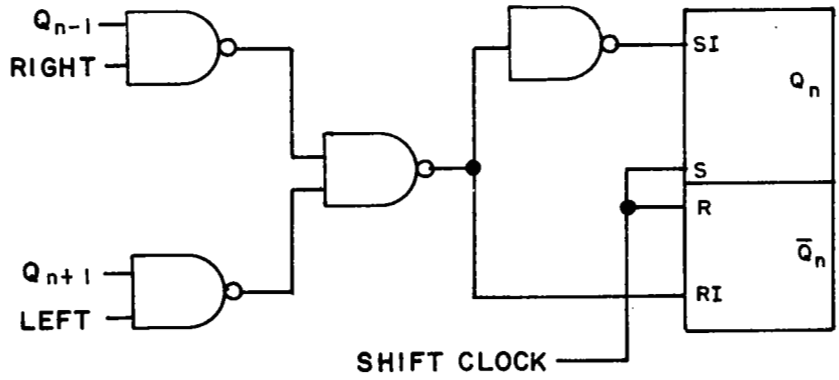
This is a parallel-in, serial-out shift register using the usual $\bar{R}\ \bar{S}$ T flip-flop connection and clocked by the $T_{3 \rightarrow 16}$ pulse burst. Parallel loading is done at T_2 time by gating the "preset" inputs of the flip-flops. By arranging for the most significant flip-flop to shift zeros into itself during the serial output time, the register is cleared to zero during each word time and it is only necessary to set in 1's of the command data as shown below:



2.4.5 Proportional Register

This is a serial-in, serial-out register with provision for left shifting the contents two places (multiply by 4) during T_1 through T_2 time.

During left shift time the sign and check bits are compared continuously. If there is a difference, the magnitude bits are set to all ones or zeros depending upon the check bit state. The sign bit is also changed to match the check bit. A bi-directional shift register requires gating between stages to control the shift direction. A typical stage with its gating looks like this:

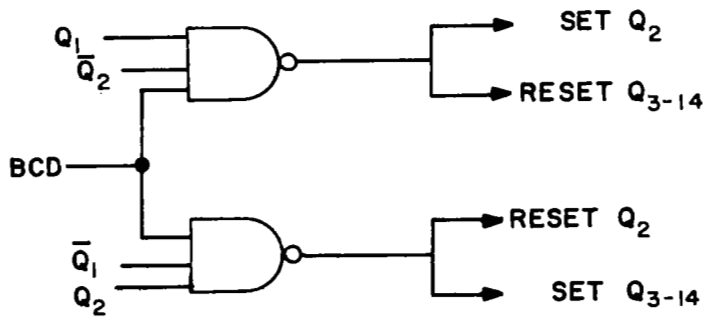


so that with right level up, data from the preceding stage is selected and with left level up, data from the succeeding stage is selected. These control levels were available from the system control logic as:

$$\text{Right Level} = \overline{BCD}$$

$$\text{Left Level} = BCD.$$

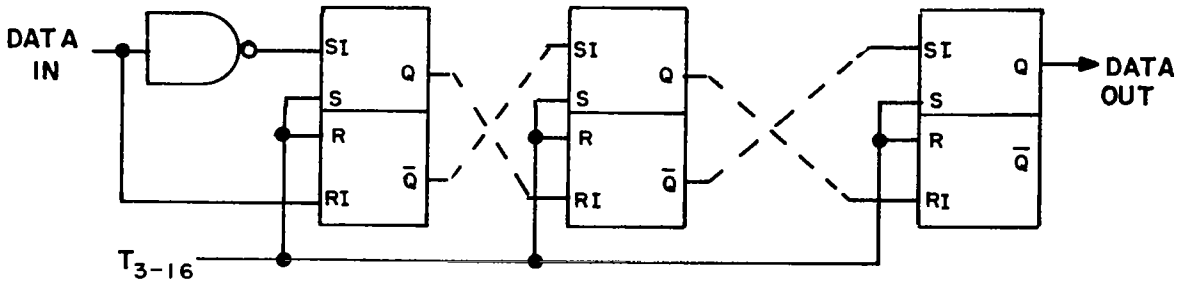
Overflow detection and correction was implemented with two NAND gates in the following manner:



Where Q_1 is the check bit, Q_2 is the sign bit, and Q_3 through Q_{14} are magnitude bits in the register.

2.4.6 Integrator Register

This is a straightforward right shift register of the form:



which is well covered in the literature and requires no detailed description here.

2.4.7 Output Register

While this is, basically, a right shift register, several operations which required gating had to be included. These operations are overflow detection and correction, and conversion of negative numbers from 2's complement to magnitude and sign.

The desired end result was a number in magnitude and sign format so the process of overflow detection was reduced to sign bit correction and the setting of all magnitude bits to one. Positive numbers (sign = 0) would already be in sign and magnitude form so only negative numbers had be considered for this additional operation.

The simplest conversion to magnitude and sign is by use of a 1's complement since this technique requires only that all magnitude bits be "toggled." That is to say, if a bit is a 1, make it a 0 and vice-versa. The resulting number will be in error by 1 bit but such an error is of small significance and can be neglected.

The logic for these operations could now be stated as:

a. If sign and check bit differ, set sign bit to match check bit and set all magnitude bits to 1;

b. If sign is negative, complement all magnitude bits,

c. With the constraint that both operations cannot occur at the same time.

Logic equations could now be written. Letting:

A = check bit

B = sign bit

C = a magnitude bit

PQ = direct set

$P\bar{Q}$ = direct reset

R = initial reset

T_i = clock pulse

Then, for the sign bit overflow correction,

$$PQ_B = A\,\bar{B}\,T_i$$

$$P\bar{Q}_B = \bar{A}\,B\,T_i$$

And for a magnitude bit under all conditions,

$$PQ_C = A\,\bar{B}\,T_i + \bar{A}\,B\,T_i + A\,B\,\bar{C}\,T_i$$

$$P\bar{Q}_C = A\,B\,C\,T_i\,.$$

Since the overflow logic automatically complements the register content, selection of clock times for these operations was important. If the overflow occurred on a negative number, we would have -

$$PQ_B = A\,\bar{B}\,T_i$$

where the second term becomes $A\,B\,T_{i+1}$ and all magnitude bits are 1 after the correction. Now ABT_i appears as part of each of the Q_C equations and this would cause complementing of the magnitude bits to all zeros, creating a large error. Obviously overflow detection had to be

done last so the equations were rewritten with initial reset, R, included:

$$PQ_B = A\,\bar{B}\,T_2$$

$$P\bar{Q}_B = \bar{A}\,B\,T_2 + R$$

$$PQ_C = A\,\bar{B}\,T_2 + \bar{A}\,B\,T_2 + A\,B\,\bar{C}\,T_1$$

$$P\bar{Q}_C = A\,B\,C\,T_1 + R$$

and noting that some form of the combination ABT_1 occurred in each equation, the implementation could be made as shown in Figure 14. It can be seen in this figure that the inversion of the equation is used. This is because the logic elements used required a 1 to 0 transition for direct set and reset inputs. One set of six gates, shown shaded in Figure 14 is required for each magnitude bit of the register.

2.4.8 Buffer Register

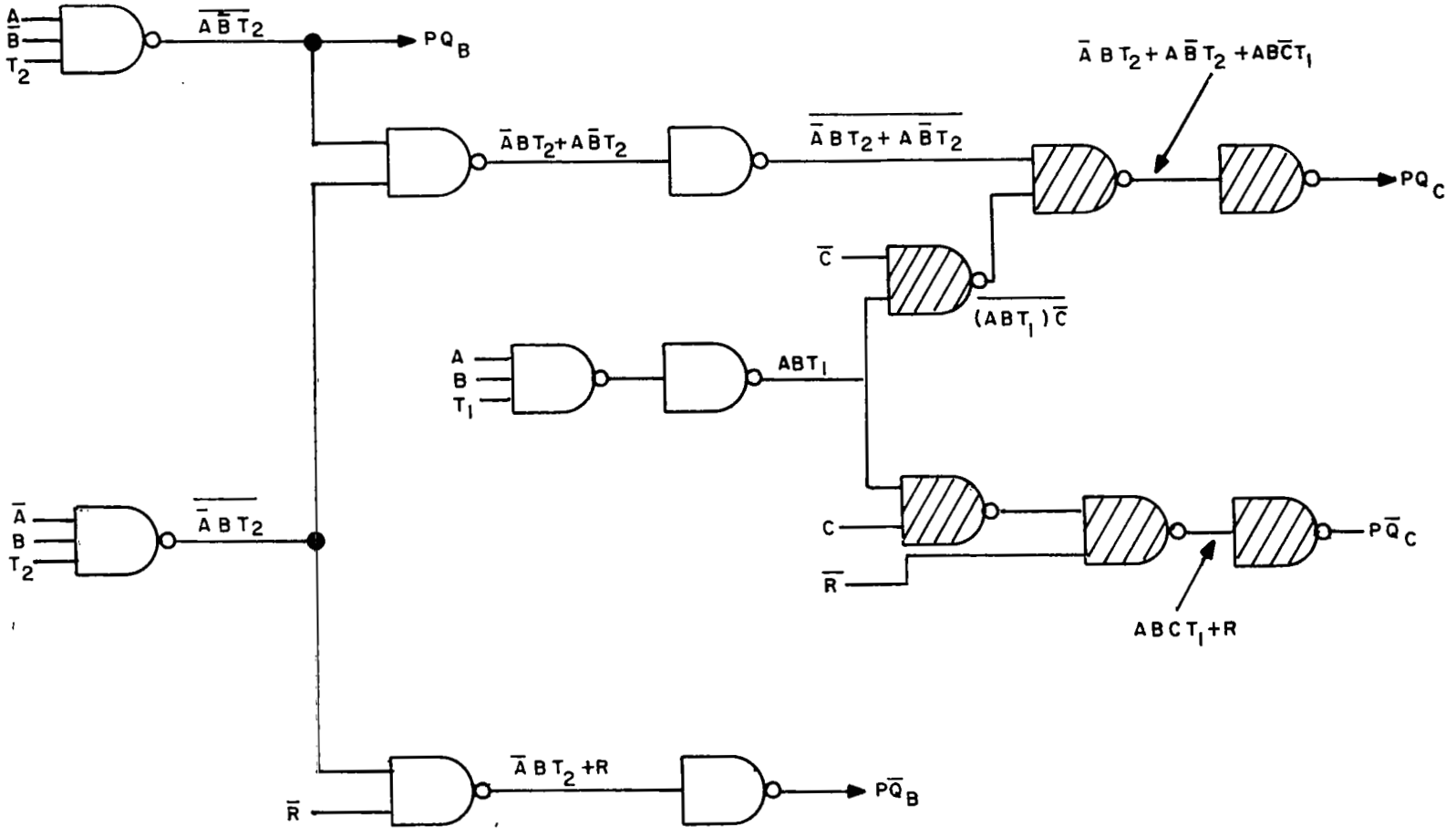
This register acts as a zero-order hold and is parallel loaded from the output register each T_2 time. The check bit is dropped in this transfer because no overflow is possible. The flip-flop of this register are connected in type "D" configuration so only one data line per flip-flop is required. Data is transferred by clocking the register with only the T_2 clock pulse.

2.4.9 Rate Multiplier

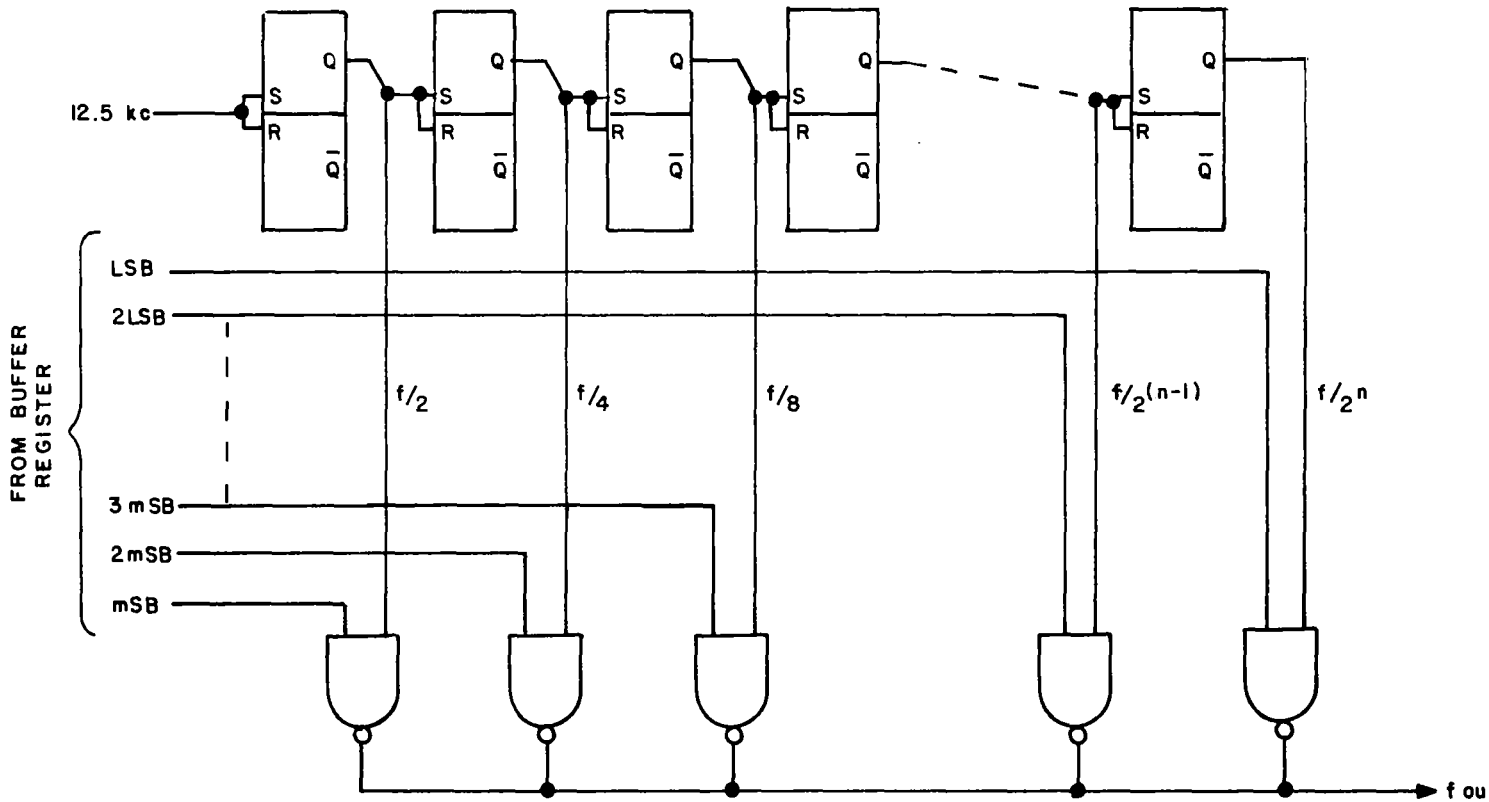
The buffer register data, a binary number, must be converted to a pulse train which has a frequency proportional to the desired reaction wheel velocity. This pulse train becomes a command to the digital speed control unit. The rate multiplier or binary operational multiplier is described in some literature, particularly in the field of numerical control of machine tools. It is a logic circuit which accepts a pulse train at one input, a numeric code at the other, and has as its output a new pulse train containing a number of pulses equal to the product of the two inputs. Figure 15 shows the common method of constructing this logical element. In this system, with 50 pulses on the reaction wheel and a desired maximum rps of 250, the input pulse train to the rate multiplier has a frequency of:

$$50 \times 250 = 12{,}500 \text{ cps}$$

which was available from the clock divider. To maintain a proper phase relationship with the 6.25 kc arithmetic unit clock, the 12.5 kc was taken



OUTPUT REGISTER CONTROL LOGIC
FIGURE 14



BINARY RATE MULTIPLIER
FIGURE 15

from the zero or NOT side of the clock divider's 3rd stage. This assured that a differentiated rate multiplier output pulse could occur during the "1" time of the 6.25 kc clock.

2.4.10 Digital Speed Control

The speed control unit consists of the logic shown in Figure 16. This control, developed in-house prior to 1962, gives a demonstrated control accuracy limited only by the stability of the command pulse train frequency. The command input comes from the rate multiplier, and the sign input from the sign bit of the buffer register, both in the arithmetic unit, while the feedback pulse train comes from the reaction wheel.

The anti-coincidence circuitry provides one-bit temporary storage for both the feedback and command pulse trains. The two temporary storage flip-flops are controlled by the clock such that one is out of phase with the other in passing on incoming data. Since the clock operates the flip-flops at a 100 kc/s rate while incoming data will be at a maximum of 12.5 kc/s, data pulses cannot be lost and possible coincidence of the two inputs is overcome.

The direction control acts simply as a DPDT switch to connect the inputs to the up or down sides of the following counter as directed by the sign bit.

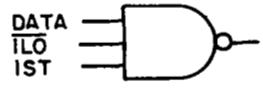
The bi-directional counter acts as a summer to produce, through a weighted resistor D/A converter, an analog voltage of sufficient magnitude to drive the wheel at a speed such that the two input frequencies are exactly the same.

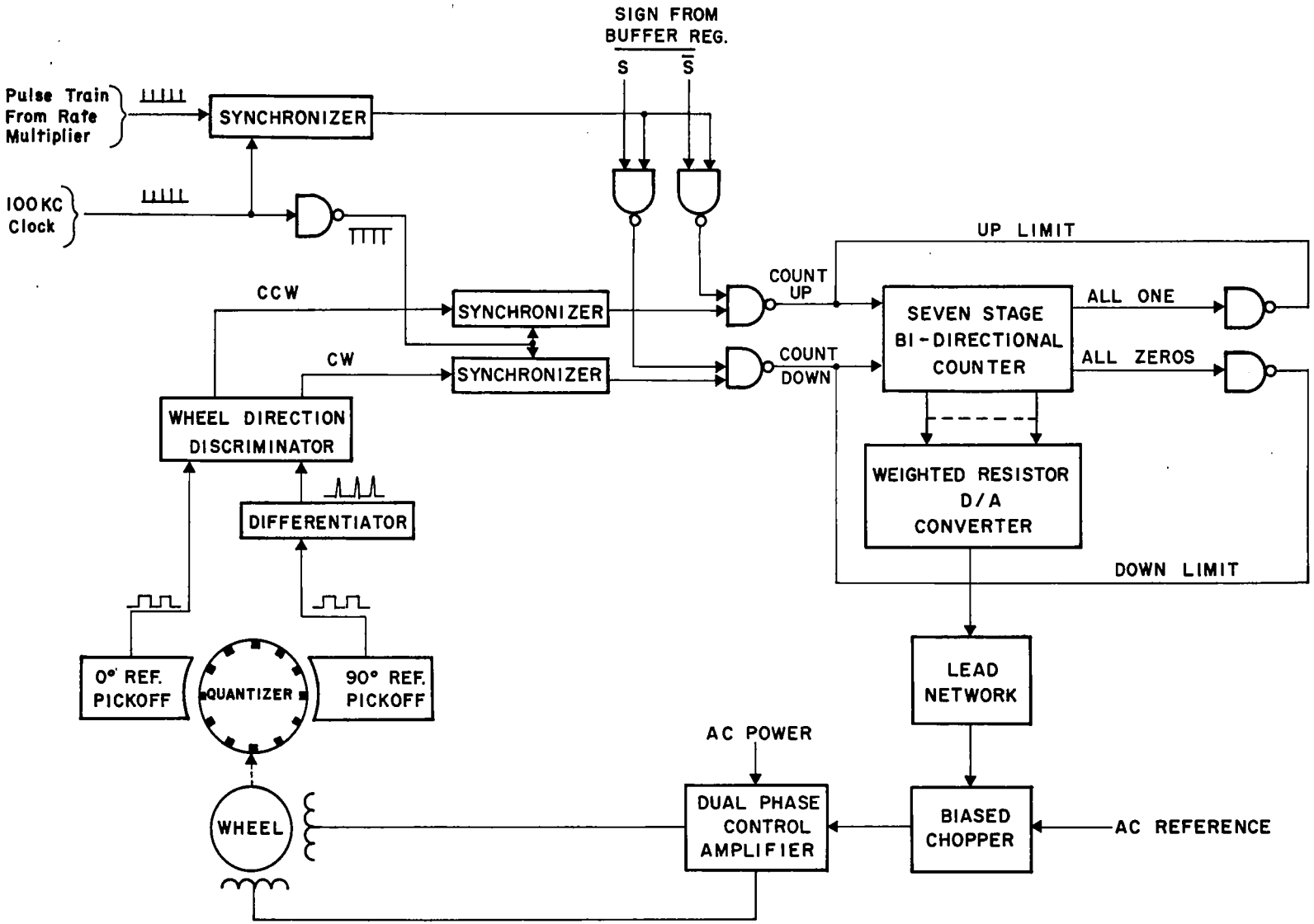
The D/A converter output is unipolar. The chopper of the following servo amplifier is biased to the mid-point of the D/A converter output range to provide bi-directional phasing for the reaction wheel.

It should be noted that the speed control unit is a complete closed-loop system by itself and, as such, has many other applications where precise control of rotary machine velocity is required.

2.4.11 Integrator Lockout

This function is shown schematically as S1 in Figure 12. This switch is a NAND gate with three inputs:





DIGITAL SPEED CONTROL-LOGIC BLOCK DIAGRAM
FIGURE 16

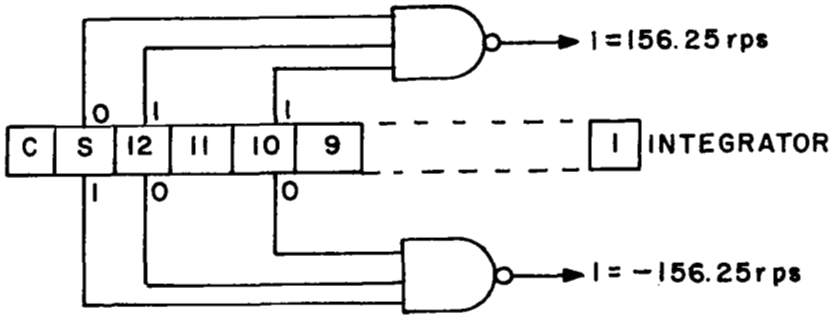
where $\overline{ILO}$ indicates NOT Integrator Lockout and IST indicates Integrator Sample Time. Integrator lockout goes to zero and inhibits the gate whenever the proportional register content is greater than ± 64 to prevent integrator saturation. IST is normally zero and goes to "1" for one word time every 1024 words. This sets the integrator gain at 0.763 or a sample rate of slightly less than 1 per second. Data can pass through this gate only when $\overline{ILO}$ and IST are both in the 1 state.

2.4.12 Momentum Dumping

Stored momentum due to external disturbance torques is indicated in the steady state by integrator content. A number in this register could, therefore, be used to initiate momentum dumping. The number in any register can be related to wheel velocity in this manner:

4096	=	1/2 max. rps
2048	=	1/4 max. rps
1024	=	1/8 max. rps
↓		↓
1	=	1/4096 max. rps.

so that 5120 decimal = 00101000000000 binary equals 5/8 x 250 = 156.25 rps. Examination of the reaction wheel torque-speed curve indicated that this velocity would represent a reasonable set-point for dumping. Since the actual trip point is not critical, a very simple gating circuit could be used to detect the desired set-point within a practical range. Only the sign bit, MSB and 3MSB, of the integrator need be observed. A simplified diagram of the required gating looks like:



When a level is detected on either gate, and the digital speed control is not saturated and the integrator lockout is not activated, a flip flop is gated so as to fire a jet. This mass expulsion would normally cause an offset in a direction so as to run the integrator content down and thereby reduce wheel velocity. But the jet torque is deterministic and in this application a ramp, with a slope equal to jet torque, is injected into the integrator so as to eliminate this offset. The ramp is turned on by the same integrator content detection gates. Both jet and ramp are turned off when the integrator changes sign upon passing through zero. The ramp is in discrete or staircase form and is a single bit entered directly into the integrator adder network after the lockout gate. The rate of injection, in bits per second, i. e. the ramp slope, can therefore be changed to match a wide range of jet torques.

The ramp generator performs another function in this system. There is a possibility, in making wide angle maneuvers, that the digital speed control might become stabilized before the error has dropped within the integrator non-lockout range. That is, the wheel velocity may actually reach the instantaneous commanded velocity and settle out. The system would then be "lost" because the integrator could not operate to reduce the offset error. With the ramp generator available, it is practical to detect the combined states of integrator locked out, not dumping and digital speed control not saturated. If this occurs, the ramp is injected into the integrator with the same slope as the error sign and forces the vehicle to approach zero error at a constant velocity until the integrator unlocks and takes over. All possibility of getting "lost" is thus eliminated.

As can be seen, the logical design of this system utilizes textbook elements with such gating as may be required to perform specific tasks related to this particular system. In essence, this is the approach to any problem in logic design. More detailed information can be obtained from References 1 through 4 listed at the end of this report.

3 ELECTRONICS UNIT DEVELOPMENT

3.1 COMPONENT SELECTION

There are probably as many ways to select a particular integrated microelectronic module as there are applications and users. The art is in such a state of flux that today's selection may well be obsolete tomorrow. For this reason, the selection process is difficult to define.

In this program, the following factors relating to the overall system were considered to be of prime importance. Logic level swing should be large to permit digital-to-analog conversion without the use of amplifiers. Fan-out capability should be high enough to minimize module count and to increase reliability. The number of input leads per gate, and gates per module, should be such as to minimize module count and number of connections required in a circuit. Cost should be reasonable for the application. Power dissipation should be low, relative to switching speed. The modules should be of the monolithic circuit type for minimum internal connections.

Within these bounds, selection was begun by surveying all potential vendors of integrated microcircuits. This survey consisted of examination of manufacturers' literature, corrrespondence, telephone conversations, and personal meetings. From the data obtained, a group of four manufacturers was selected whose microcircuit logic modules were considered to be suitable for this system. Final selection was based upon a quantitative evaluation scheme wherein each vendor's line was logically designed into one of the typical system elements (a shift register) and then rated according to these parameters:

a. Logic swing,
b. Number of interconnections,
c. Power,
d. Fan-out, and
e. Cost.

Each of these parameters was considered to have equal weight and each was normalized to the highest numerically valued vendor. The sum of normalized parameter values, for a vendor, became his rating value. As a result of this evaluation, Siliconix, Incorporated, of Sunnyvale, California was selected for use in this study program.

3.2 PACKAGE DESIGN

A hypothetical application was postulated for the system: stabilization and attitude control of a scientific satelite having a life of three to five years.

This hypothesis implied high reliability and limited field maintainability, small size, and minimum weight. Resistance welding was chosen for module attachment to printed circuit boards. To keep the number of inter-board wired connections at a minimum, it was decided to use three boards; each board was to be epoxy glass and 6" x 8" x 3/32" in size. Plated through-holes would be used for intra-board connections. Input and output connections would be through type DB25 and DA15 connectors, respectively.

Although the modules were to be welded, the discrete components used in the D/A converter and the inter-board wiring were to be soldered. Cladding for the circuit boards was selected so as to be compatible with both methods of attachment. Based on previous in-house experiments, a plating of tin-nickel alloy over copper was chosen, the art work laid out, and boards ordered.

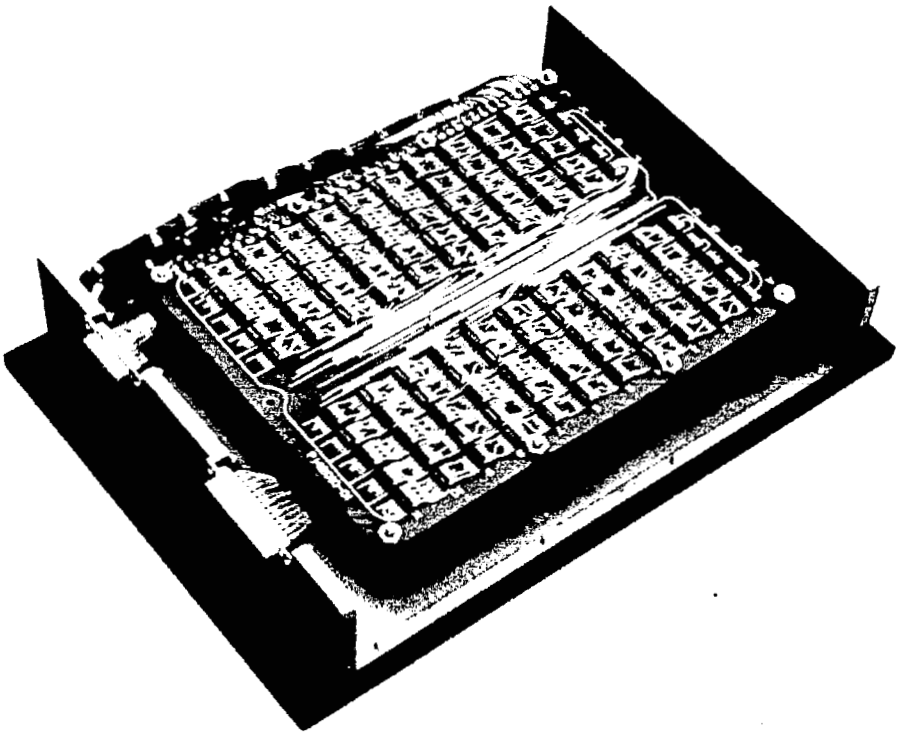
The enclosure for final assembly of the three stacked boards was next designed. Photographs of a typical board and the final assembly are shown in Figure 17.

3.3 FABRICATION AND ASSEMBLY

When fabrication began, it became apparent that the printed circuit boards had faulty plating and would neither weld nor solder properly. A new set of boards was ordered using gold flash over nickel plating on copper clad material while an analysis of the tin-nickel alloy plating problem was begun. At the conclusion of LSI's investigation into the tin-nickel alloy plating problem, it was determined that adequate control of plating thickness had not been achieved. To assure trouble-free welding and soldering, this plating must be limited to a maximum of 0.0005 inches in thickness. Failure to specify such a maximum thickness was the sole cause of the problem.

Assembly was then repeated, using the alternate set of boards. A weld schedule was determined and modules welded to the printed circuitry. It became apparent during welding operations that variations in module lead thickness and surface finish were troublesome as evidenced by weld blow-out which damaged either module leads or printed circuit lands or both. Such blow-outs were repaired by soldering while a study of weld schedule set up was made. As a result of this study, future welding operations will have schedules prepared in a manner similar to that which is detailed in Chapter 3 of NASA Technology Handbook, "Welding for Electronic Assemblies," NASA SP-5011.

Inter-board wiring was next completed and input-output connectors were affixed. The completed board and harness assembly was now ready for electrical test and debugging. Results of testing, debugging, and final test are detailed in the next section of this report.



TYPICAL CIRCUIT BOARD AND FINAL ASSEMBLY
FIGURE 17

4 DEBUGGING AND TESTING

The electronic unit was connected to the LSI simulator through interface level changers which were required because the simulator logic levels were 0 and -6 volts while the electronic unit logic levels were 0 and +6 volts. A test number was entered into the control unit and traced through the arithmetic section. Several sections were inoperative. Debugging was begun with a check of supply voltage and ground circuits. Several open lands were found in this part of the printed circuitry. These opens resulted from weld blow-outs. Solder bridging was used to correct the faults. A permanent solution to this problem was detailed in Section 3. 3.

Continued testing revealed race problems brought about primarily by the trigger characteristics of the flip flops used in this system. These flip flops change state on the leading edge of the clock and when their output was sampled by the input logic ambiguous control inputs would result. To correct this problem logic changes were made so as to use only the true output line of a flip flop in its input logic equations. By eliminating the complement output from these equations race conditions were impossible. If more application data had been on hand at the time of initial logic design these problems certainly would have been minimized.

Interboard wiring inductance proved to be a problem in one counter register. Pulse degradation along a 16-inch length of wire was sufficient to make the counter erratic. Capacitive tuning, in parallel with a pull-up resistor, was used at the input end of this line to reshape the pulse. In any new design a line driver module could be used to solve this problem and thus eliminate the discrete components.

During the debugging process a number of modules were found to be inoperative due to broken packages. An all-glass type package was being used by the vendor at the time this lot was purchased. This package is relatively fragile and careful handling is required to prevent damage. In a production run such module packaging would cause prohibitive scrap rates and cannot be recommended even for future breadboard use. This particular vendor has recently converted to a 14-lead Kovar package which appears to be an excellent solution to this problem. The location of such circuit faults was difficult due to the continuous circuitry used in this design. In future designs provision should be made for break-in, by means of jumpers, so that any register or other arithmetic element may be isolated for test purposes. While no provision for A. G. E. test points was made in this design the breakin provision could well be included in the A. G. E. test cable wiring.

With debugging completed, testing was begun using the recording equipment and techniques described in the next two sections.

4.1 TEST EQUIPMENT

The system was connected in a closed loop single axis configuration as shown in Figure 2. Figure 18 is a photograph of this setup. A reference line for displacement measurement was provided by the simple analog sun sensor which can be seen atop the spacecraft simulator. A Baldwin Model 232 shaft encoder provided 13-bit digital displacement feedback while a size 23 gimbal mount CX synchro supplied an analog output for curve tracing. Reaction wheel velocity was taken as the analog of spacecraft velocity by imposing initial conditions of stored momentum such that the wheel could not go through zero speed during a maneuver. This provided better velocity resolution for recording purposes. The simulated spacecraft floats on an air bearing and has an inertia about 10^4 times that of the wheel. The air bearing, although spherical, was restricted in pitch and roll for this test series. Reaction jets, controlled by electromagnetic valves and using CO_2 as the thrust medium, were provided for momentum dumping. The response of this system to step displacement commands was recorded using the following equipment:

a. Sanborn Strip Chart Recorder with,
   #154-100B Recorder,
   #150-1200 Servo Monitor Pre-amplifier,
   #150-400 Power Amp.

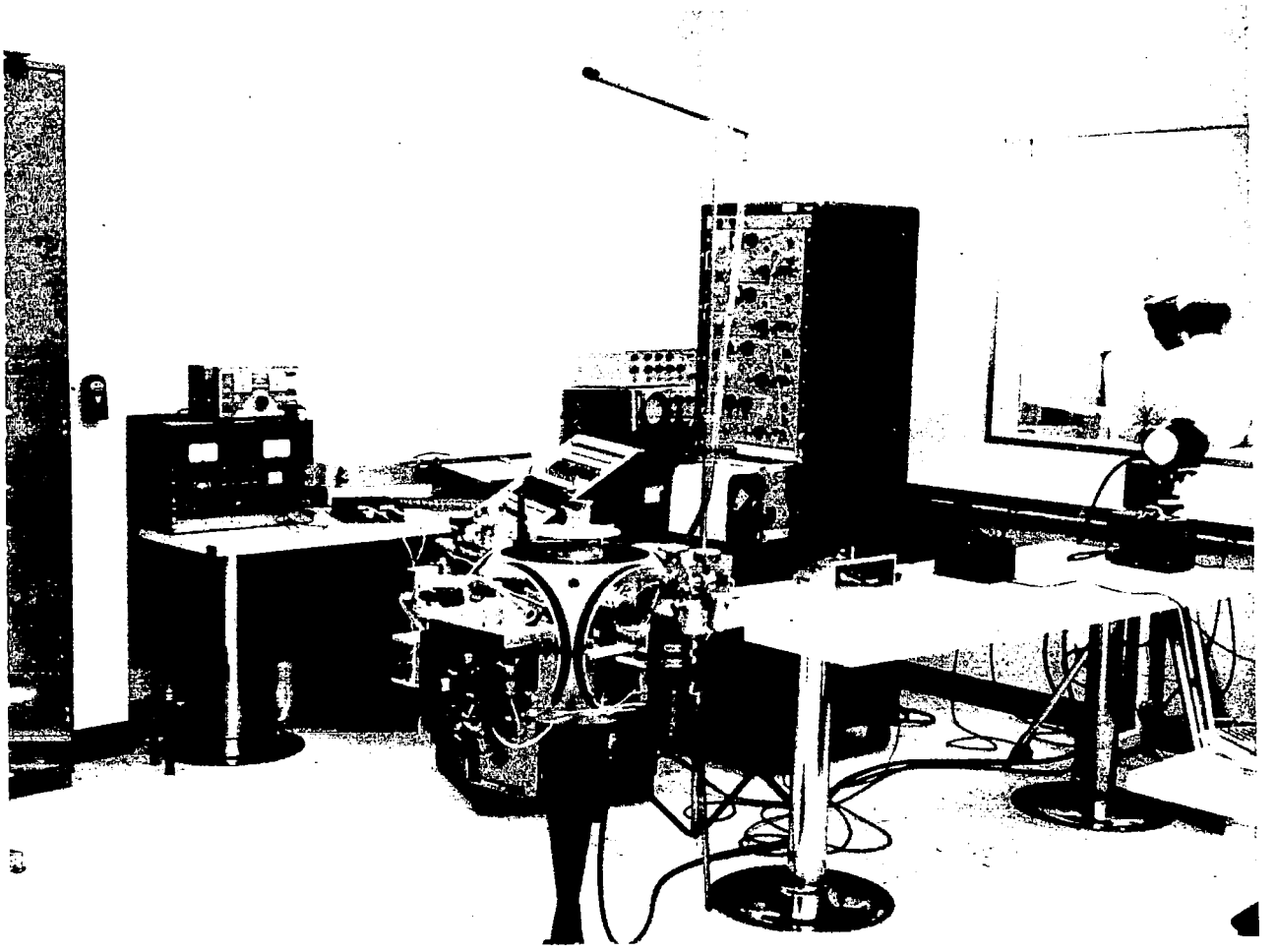
b. Moseley Model 2D X-Y Recorder,

c. Vidar Model 322 Frequency-to-Voltage Converter,

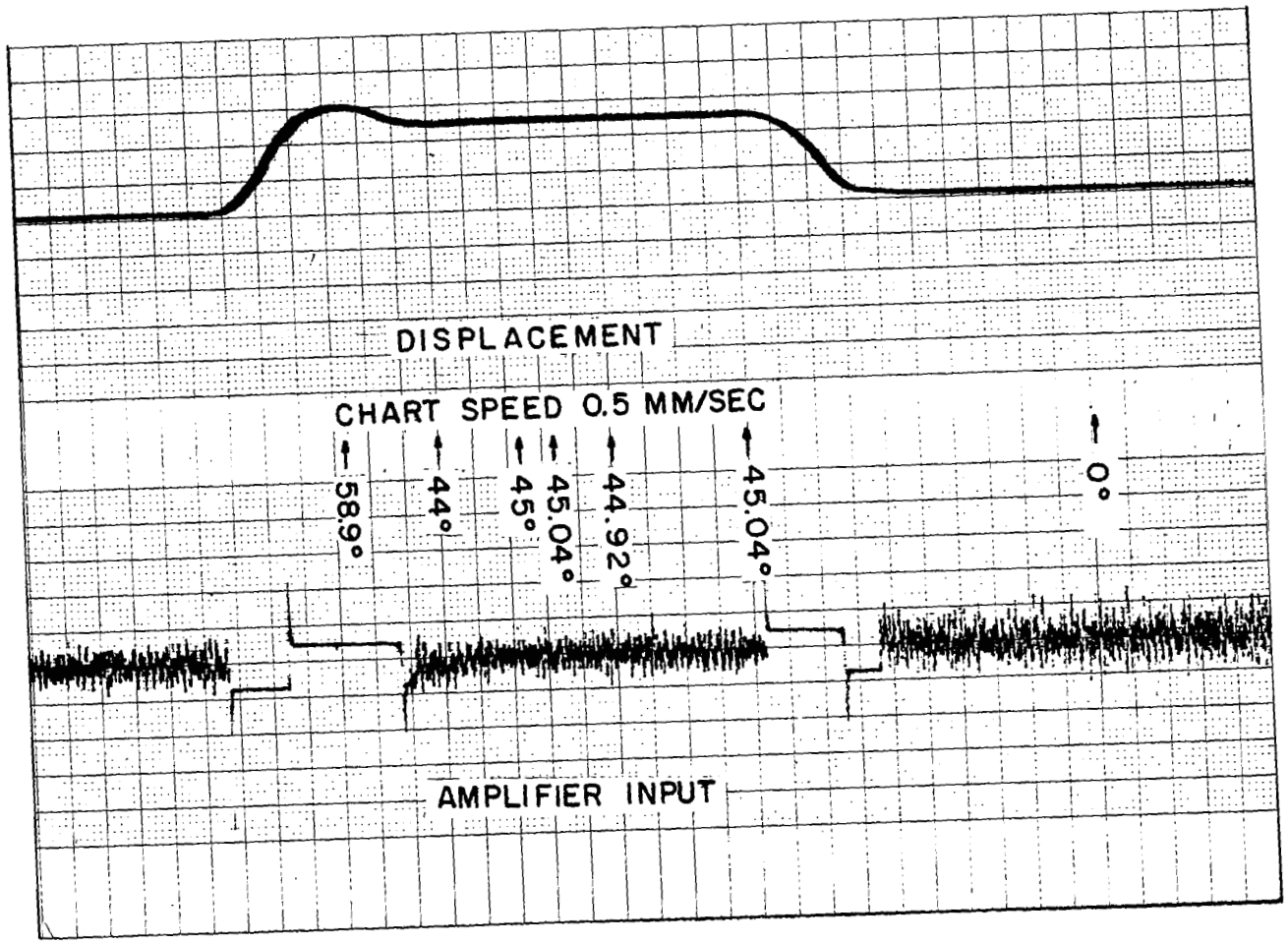
d. LSI Digital Display Unit.

4.2 TEST RESULTS

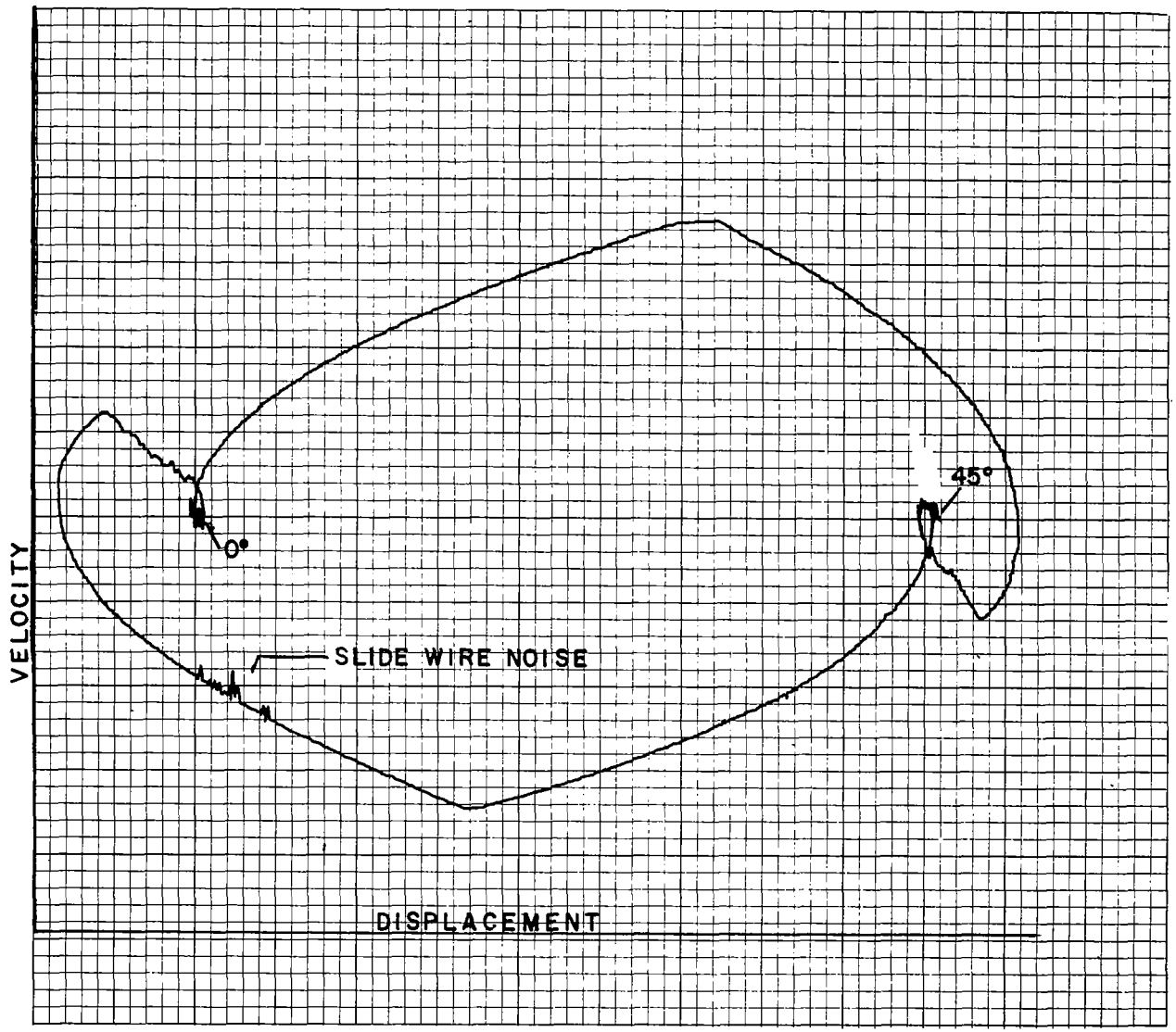
The system response to step displacement commands is shown in Figures 19 through 22. The strip chart recordings display spacecraft displacement and servo amplifier input voltage vs time. Amplifier input voltage was selected for recording because it can be considered as the electrical analog of torque in this system. The synchro displacement signals were demodulated by phase sensitive servo monitor preamplifiers prior to recording. For phase plane plots the demodulated displacement signal was fed to the X-axis of an X-Y recorder and the



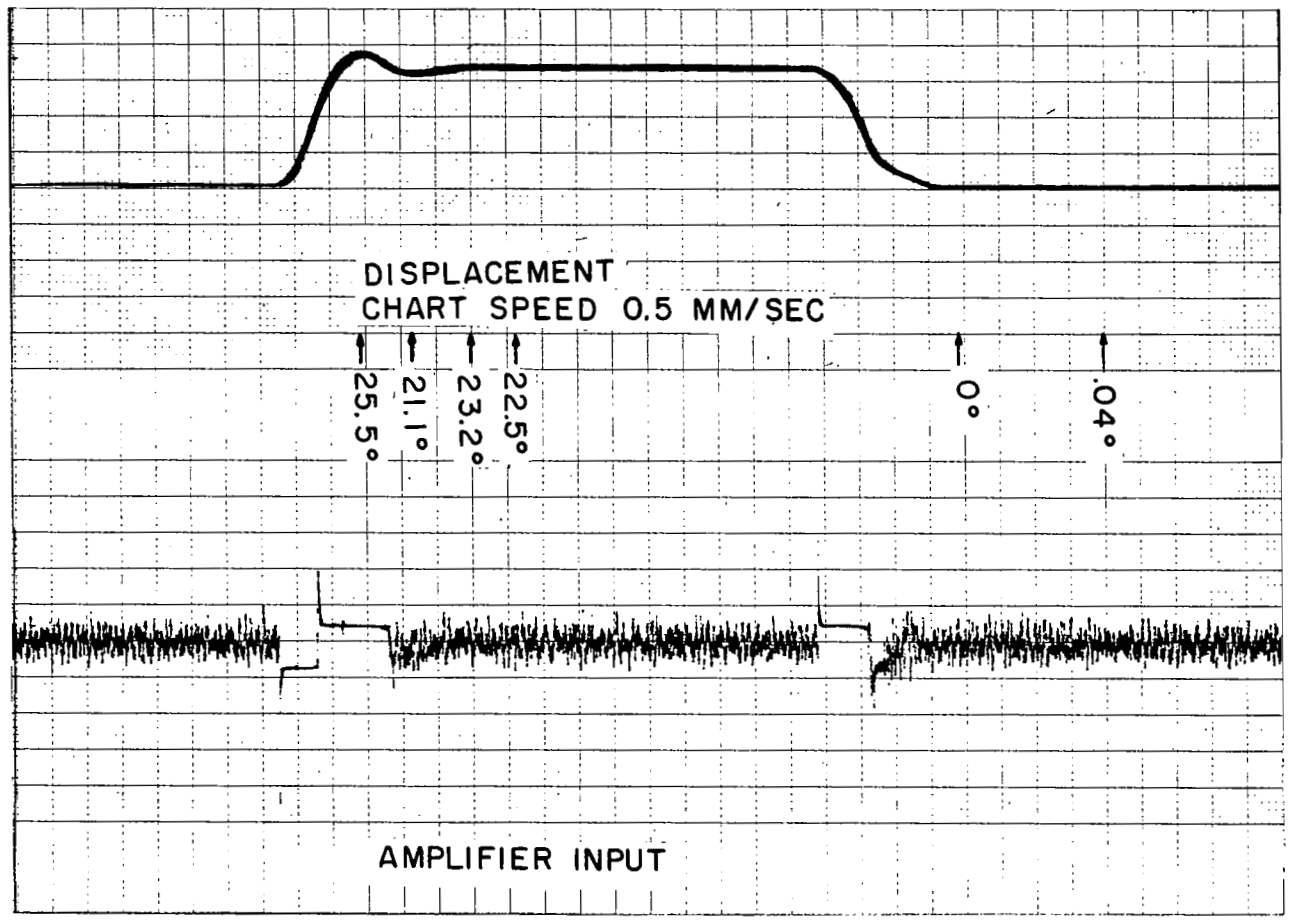
TEST SET-UP
FIGURE 18



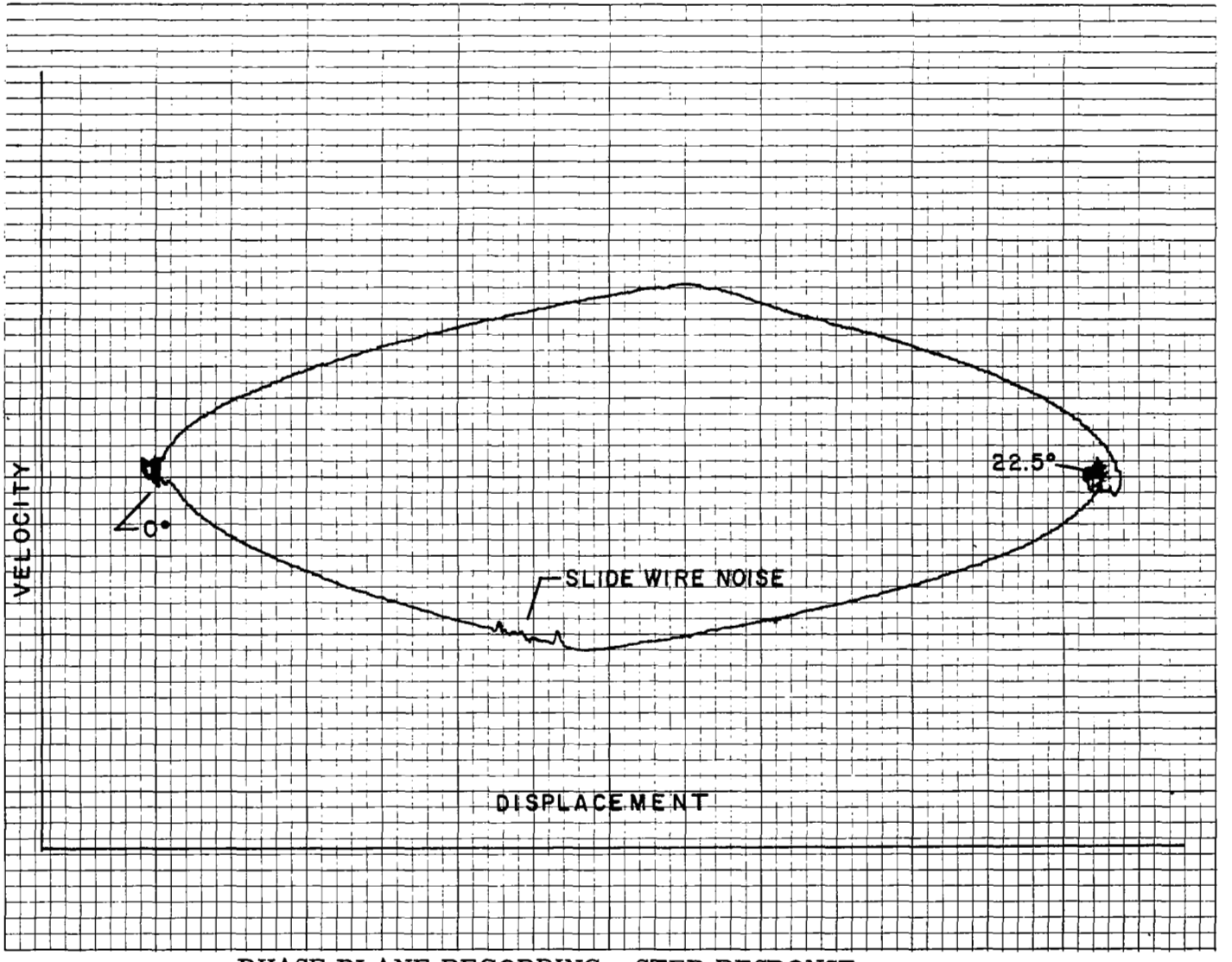
STRIP CHART RECORDING - STEP RESPONSE
45° COMMAND
FIGURE 19



PHASE PLANE RECORDING - STEP RESPONSE -
45° COMMAND
FIGURE 20



STRIP CHART RECORDING - STEP RESPONSE -
22.5° COMMAND
FIGURE 21



PHASE PLANE RECORDING - STEP RESPONSE -
45° COMMAND
FIGURE 22

reaction wheel feedback pulse train fed through a frequency-to-voltage converter to the Y-axis of the same recorder. Displacement readings, taken visually from a digital readout which displayed shaft encoder output, were logged and annotated on the strip chart recordings. Comparison of test data with a computer simulation is shown in Figure 7.

The results obtained indicate that the design procedures and modeling techniques used for this single axis system are adequate and sufficiently accurate to design and produce a digital controller which will meet a specified requirement. Refinements of these methods can be extended to the three-axis case and, from the results obtained here, clearly warrant further study.

5 SUMMARY AND RECOMMENDATIONS

The state space technique was established as a powerful tool for both the analysis and design of the over-all system. To illustrate this, a non-linear system state model of the LSI spacecraft simulator was developed in Section 2. 3. The accuracy of the state model was verified by comparing the actual simulator performance to a numerical solution of the model. It is felt that this modeling technique should be used for the design of any future digital control systems since it appears to offer new possibilities for the optimization of the digital controller. In addition, it provides a convenient means of accurately simulating important digital system characteristics such as sampling and low-level limit cycling.

The particular technique used for the logic design of the digital controller of the LSI simulator has been described in detail in Section 2. 4. Special attention was given to the application of NAND logic for the implementation of equations derived by switching algebra.

The feasibility of an on-board digital spacecraft attitude controller has been verified by the actual fabrication of an integrated microelectronic controller. Five major problems were encountered in the construction and testing of this controller. These problems and their solutions were discussed in Sections 3 and 4 and are summarized here.

a. Welding - Damage to both the printed circuit lands and the integrated logic was experienced during welding. It is recommended that future welding schedules duplicate those described in Chapter 3 of NASA Technology Handbook, "Welding for Electronic Assemblies," NASA SP-5011.

b. Inductance - The self-inductance of the interboard wiring caused significant degradation of some of the pulse trains. The problem was solved by capacitive loading.

c. Race conditions - A number of logic circuits in the initial microelectronic controller had to be altered to eliminate critical time races. It is felt that more complete application information on the integrated logic modules would have prevented this condition.

d. Fault location - Troubleshooting problems were compounded by the inability to isolate various registers from the rest of the logic circuitry. Future designs should include numerous jumper wires that may be disconnected for this specific purpose.

e. Microelectronic packaging - Glass packaging was used for the microelectronic modules and was found to be too fragile for this application. A material that is more durable should be used for future designs.

A reliability test program was developed for this program based on step-stress methods. It is felt that this technique provides meaningful results in the least amount of time and at minimum cost.

The problems that were encountered in this program were not basic to digital control systems. It appears that the only limiting factor in digital spacecraft attitude control is the accuracy that can be achieved with state-of-the-art sensors, actuators, and encoders. At the present time, shaft encoders limit pointing resolution to approximately one part in 2^{18}.

Although not specifically discussed in the body of this report, certain interesting developments in the semiconductor industry point toward monolithic integrated circuit modules which contain entire shift register elements of from 4 to 16 bits in a single package. It is recommended that these developments be closely watched, and assisted where practicable, since the use of such elements would reduce parts count and thereby tend to increase mechanical reliability. Their use would also reduce size, weight and, probably, power requirements of any digital system.

It is recommended that the experience that was obtained in this program, especially in the area of state-space techniques and optimal digital control, be applied to the design and fabrication of a three-axis reaction wheel control system.

APPENDIX A

RELIABILITY TEST PLAN

FOR

SPACECRAFT CONTROL SYSTEMS

APPENDIX A

RELIABILITY TEST PLAN FOR SPACECRAFT CONTROL SYSTEMS

A1 TRADE-OFF STUDY

A reliability test method is required to assure that a spacecraft digital control system will remain operational during the mission life of the spacecraft. Because of the limited time available for testing purposes, this method must be designed to produce the required data in a reasonable amount of time. It should simulate both the flight hardware and flight conditions as accurately as possible. In addition, it should be very versatile so that the results of this program can be applied accurately and quickly to any similar program which may be required in the future.

Basically, there are two types of tests which can be performed. The first (Type A) is to test the equipment under environmental conditions which duplicate, as closely as possible, those expected in operation. The second (Type B) is to test the equipment under high stress conditions until it fails, and then find some factor which relates its life under high stress conditions to its life under normal conditions.

Each of these two types can be broken down into three methods. The first (Method 1) is to test each of the basic components (resistors, capacitors, microcircuits, etc.) separately, determine their failure rate, and then add up each of the failure rates to obtain the failure rate of the system. The second (Method 2) is to test some basic subassembly of the system which has been chosen to be equivalent to a known fraction of the system. After its failure rate is determined, the failure rate of the complete system can be calculated. The third (Method 3) is to test the system as a whole, until its failure rate is known.

Each of these types and methods of testing is listed in Table AI along with the advantages and disadvantages of each test program.

In spite of the disadvantages, Test B2 is considered to be the most advantageous of all those studied. Methods were developed to minimize the effect of the disadvantages.

The first problem that arises is to define a representative subsystem. The sample unit must consist of the components used in the system,

TABLE A-I

TEST TYPE AND METHOD	ADVANTAGES	DISADVANTAGES
A1	1. Samples are inexpensive 2. Some data are available from manufacturer	1. Much test equipment is needed 2. Many samples are needed 3. Results are not necessarily valid for system 4. Test valid for given flight profile only 5. Test relatively long
B1	1. Samples are inexpensive 2. Some data are available from manufacturer 3. Results can be used for any flight profile 4. Test relatively long	1. Much test equipment is needed 2. Many samples are needed 3. Results are not necessarily valid for system 4. Different failure mechanisms might exist
A2	1. Samples quite representative of system 2. Simple test equipment needed 3. Not many samples required 4. Provides fairly accurate results	1. Samples relatively expensive 2. Test valid for given flight profile only 3. Test relatively long 4. A representative subsystem must be found
B2	1. Samples quite representative of system 2. Simple test equipment needed 3. Not many samples required 4. Most system parameter tested 5. Results valid for any flight profile 6. Test relatively short 7. Provides fairly accurate results 8. Test valid for most systems	1. Samples relatively expensive 2. Different failure mechanisms might exist 3. A representative subsystem must be found
A3	1. Very accurate results 2. Simple test equipment needed 3. Few samples required 4. All system parameters tested	1. Samples very expensive 2. Test relatively long 3. Test valid for given profile only 4. Test valid for given system only
B3	1. All system parameters tested 2. Simple test equipment 3. Test relatively short 4. Test valid for any flight profile	1. Samples very expensive 2. Many samples needed 3. Test valid for given system only 4. Different failure mechanism might exist

mounted in the same manner, etc. It must be as inexpensive as possible and yet complex enough so that statistically significant results will be obtained. In addition, it should provide simple failure detection and fault isolation capabilities.

A study of various digital systems revealed that registers, adders, and gates form the basic units of any digital system. These three units were combined to form a simple system fulfilling all of the above requirements. The configuration of the unit chosen is explained in more detail in a subsequent section. It will consist of about 50 microcircuit modules mounted on a single printed circuit board and will include about 700 welded connections. This number of parts will provide a statistically significant number of failures for each sample unit tested.

Since this unit is still relatively expensive, the test chosen must be very efficient so that all of the data possible are obtained from each failure. These data must also be available in the shortest possible time. A search through various sources, including IDEP*, revealed that the test method designed for ADVENT would provide failure data in a short time. If this method were to be combined with a factorially designed experiment, the maximum amount of information would be obtained from each failure.

In designing this type of test, the stresses thought to be most important in determining the life of the equipment must be chosen. In addition, any interrelation between stresses which might have an effect on the life must be tested. The following environments are considered to be the most instrumental in determining life:

a. Vibration
b. Shock
c. Acceleration
d. Temperature
e. Voltage
f. Radiation
g. Temperature cycling

It is also considered that the interrelationship between the following conditions would be important:

a. Vibration and temperature
b. Pressure and voltage
c. Voltage and temperature
d. Radiation and vibration (sequential)
e. Radiation and voltage

*IDEP REPORT NO. 347.50.00.00 - E1-03, LONG LIFE HIGH RELIABILITY PART EVALUATION, March 15, 1963.

Most of these tests are designed to check the assembly of microcircuits, connections, and printed circuit boards under various conditions since it was felt that the life of the microcircuits themselves was known from manufacturers' data. Any defect, however, whether inside the microcircuit or outside, will be detected and counted as a system defect.

A2 TEST PLAN

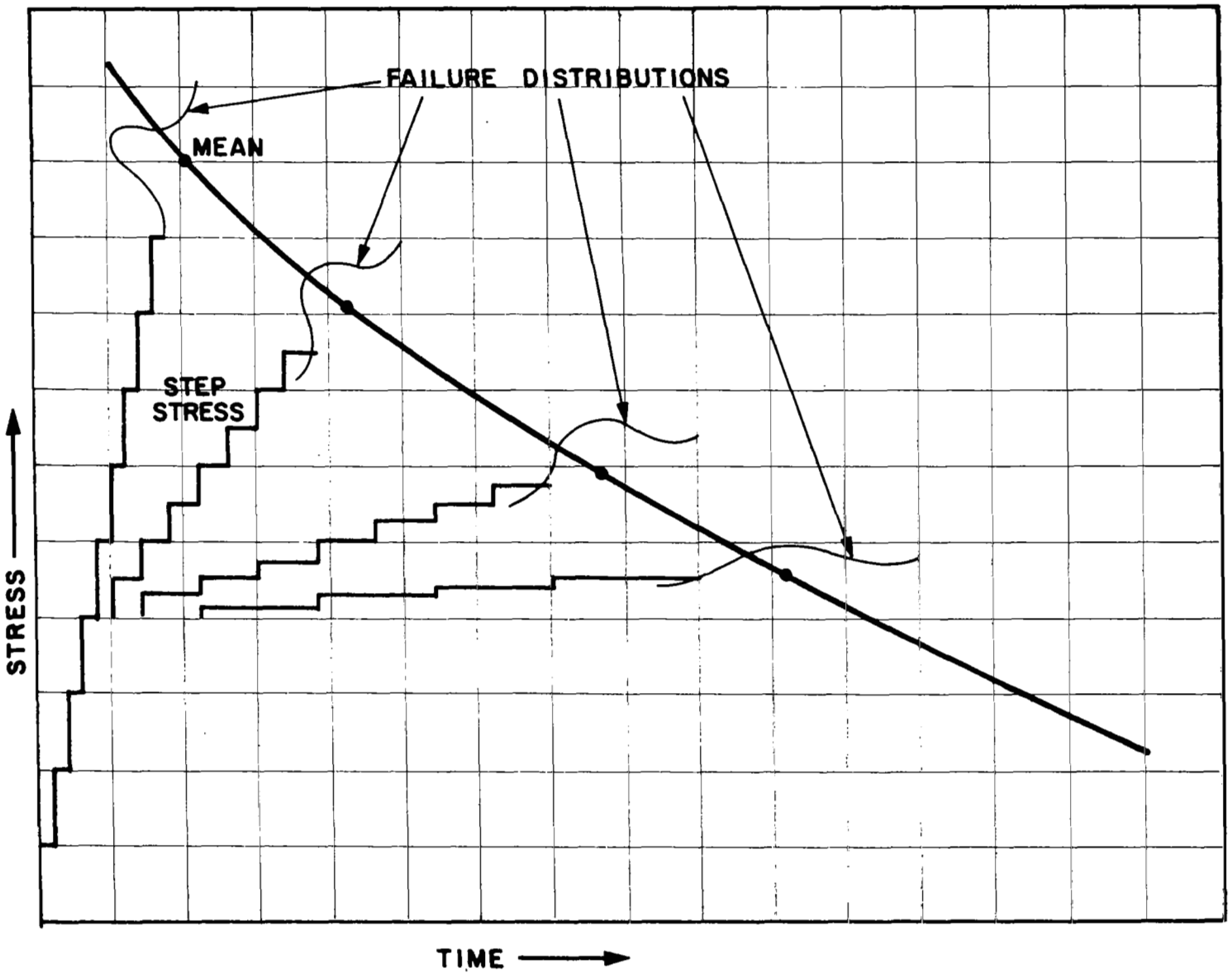
A number of sample units will be built for the testing program. All of the units being tested at one time will be connected together as described later. The tests being performed, however, do not have to be related. The reason they will be interconnected is to simplify the test monitoring equipment.

For each environmental stress to be studied, four sample units will be required. The first will be subjected to a stress of one quarter of its rating for one hour. The stress will then be raised to one half rating, then three quarters, and so on, with one hour of constant stress between each step. This will be continued beyond its ratings until the unit fails. The failure will be repaired and the step stress procedure continued until it fails again. This will continue until a statistically significant number of failures has occurred. When a failure has occurred and has been repaired, this portion of the unit will no longer be considered as part of the sample under test. That is, if it fails again, it will not be counted as a failure nor will it be counted as a success if it doesn't fail again.

The same procedure will be followed for the second unit, up until maximum rating is obtained. From there on, the steps will be half the size previously used and the sustained stress between steps will be twice as long. The third and fourth units will be similarly tested with the steps one half the height of the previous test and the length of constant stress doubled. The actual height and length of each step may be changed if it is felt that quicker or better results would be obtained in this way.

The result of this program will be a plot similar to Figure A-1. A curve through the mean of each failure distribution, extrapolated to the anticipated environmental stress, will give an estimate of the MTBF of the equipment. Each of the types of stress to be studied will produce curves similar to this.

A similar set of tests will be performed to determine the interaction between types of stresses. For each of four levels of the independent



TYPICAL PLOT OF STEP STRESS VS. TIME TO FAILURE
FIGURE A-1

stress (temperature and radiation) a step stress of the dependent stress will be performed. The levels of the independent stress will be zero, maximum anticipated in use, maximum rated, and twice maximum rated unless other factors dictate the choice. The result of this set of tests will be a family of curves similar to Figure A-2.

Some means must now be provided to assure the validity of extrapolating the curve to a point where no experimental evidence has been obtained. One way of determining this is to find some underlying mathematical relationship describing the failure mechanism. This formula should then be reduced to a form where it will plot as a straight line on a certain type of graph paper -- log-log, semi-log, log normal, Weibull, etc. If the experimental points also follow a straight line of similar slope, the extrapolation is valid as long as the same failure mechanism is predominant at the lower stress level.

Some of these mathematical relationships are known. For example, the relationship of temperature to the rate of chemical reactions, known as the Eyring Model, is:

$$R = A, T e^{-\frac{B}{KT}} e^{S\left(C + \frac{E}{KT}\right)}$$

where

R = rate of reaction

K = Boltzman's constant

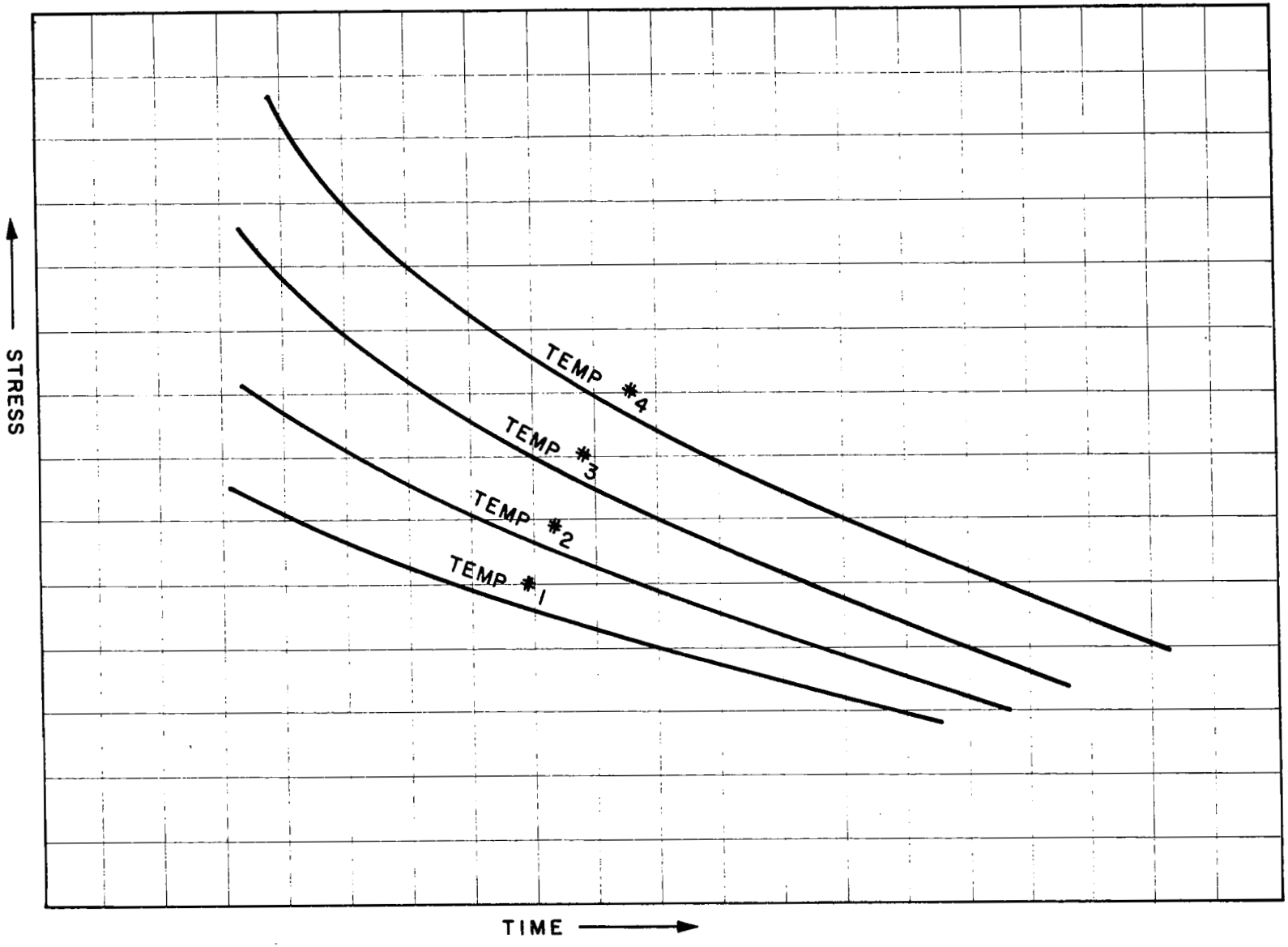
T = absolute temperature

S = some function of the applied stress

A, B, C, and E = constants

This equation can be modified to:

$$D = A_2 T e^{-\frac{B}{KT}} e^{S\left(C + \frac{E}{KT}\right)} t$$



TYPICAL PLOT OF STRESS INTERACTION
FIGURE A-2

where

D = degradation of the unit

t = time

Another model is available which relates the fatigue of meter parts with the number of stress cycles applied to the parts. This differs from the above equation in that the plot of stress vs. number of cycles is known to be asymptotic. That is, below a particular stress no failure will occur even though the stress were to be applied an infinite number of times. The study of any stress-producing metallic fatigue will be designed to reveal this asymptote so that it will be known when the stress applied during an actual flight exceeds this amount.

If this study shows that it is valid to assume that the effect of stress is cumulative and degrades the part in a known manner before failure occurs, a plot of acceleration factors can be made. If the effect of stress on part degradation is linear, this plot can be made in the following manner.

a. From the previously obtained plot of stress vs. life, find the life at the minimum anticipated stress (L_M)

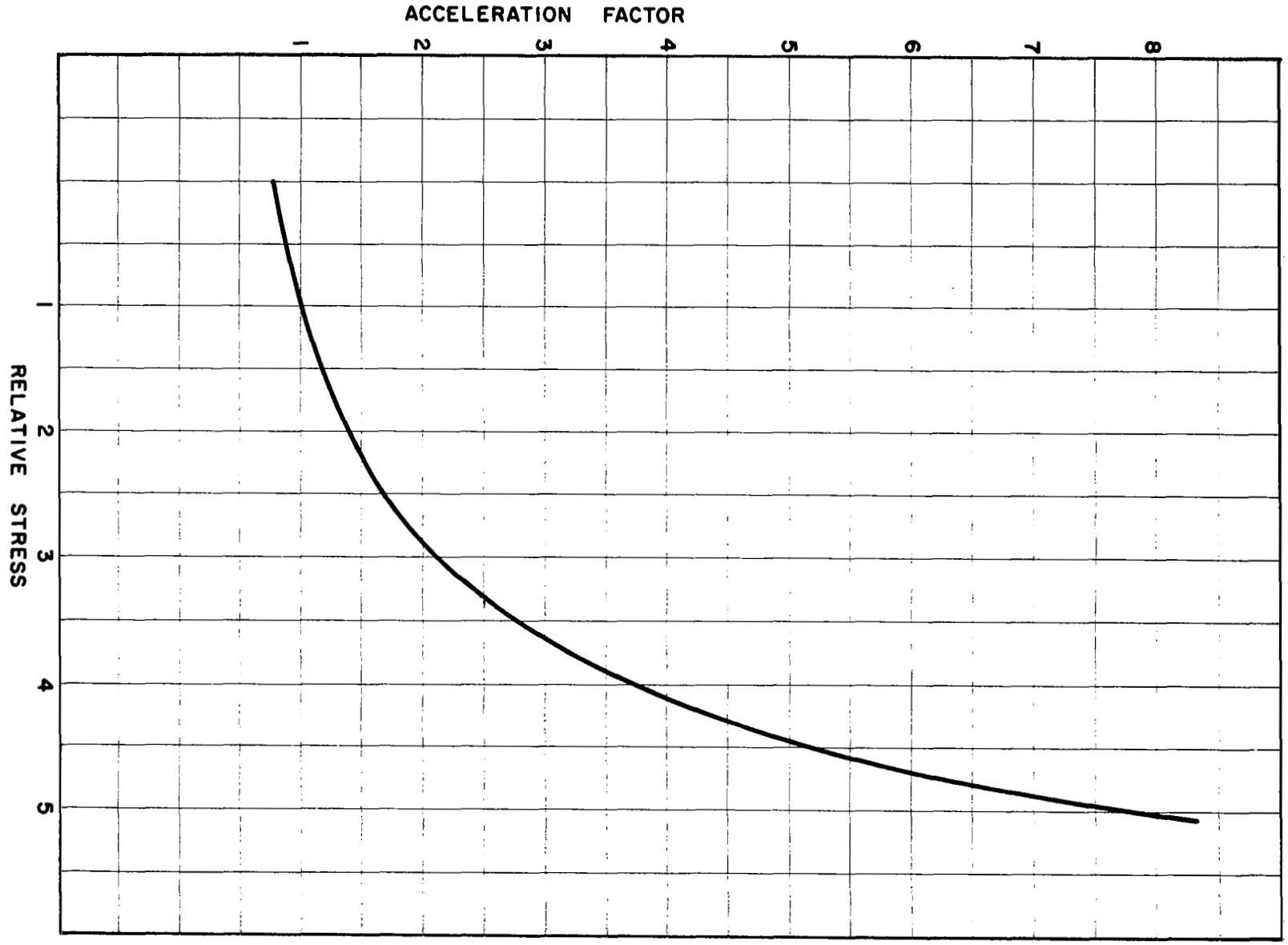
b. From the same plot, list life at a number of different stress levels (L_S)

c. Calculate the acceleration factor (A) for each stress level according to the equation:

$$A = \frac{L_M}{L_S}$$

d. Plot the points obtained in c. on a graph of stress vs. acceleration factor.

This procedure will produce a curve similar to that shown in Figure A-3. From this information, an estimate can be made of the expected life under any mission profile. The mission can be broken into various segments such as prelaunch, boost, orbit, re-entry, etc., each of which has a set of constant stresses. The time the unit is subjected to each stress multiplied by the acceleration factor is equivalent to a certain time under minimum stress conditions. By adding up each of these time



TYPICAL ACCELERATION CURVE
FIGURE A-3

segments, the equivalent operating time under minimum stress conditions can be obtained. Comparing this to the mean time to failure for minimum stress conditions, the probability of a successful mission can be obtained.

The information obtained in this study can easily be extended to almost any digital microelectronic system. The sample units were selected to include all of the basic building blocks of a typical system. To apply the information obtained in this study, determine how many of each of these blocks are present in the system then, if exponential failure rates are assumed, add up the failure rates for each of these blocks. If the failure rate is known to be non-exponential, other methods are available to determine the failure rate of the system.

Because of cost considerations, only the environments and combinations of environments felt to be most important were included in this study. Much more information can be obtained during this program if more samples are used to study additional stress interactions.

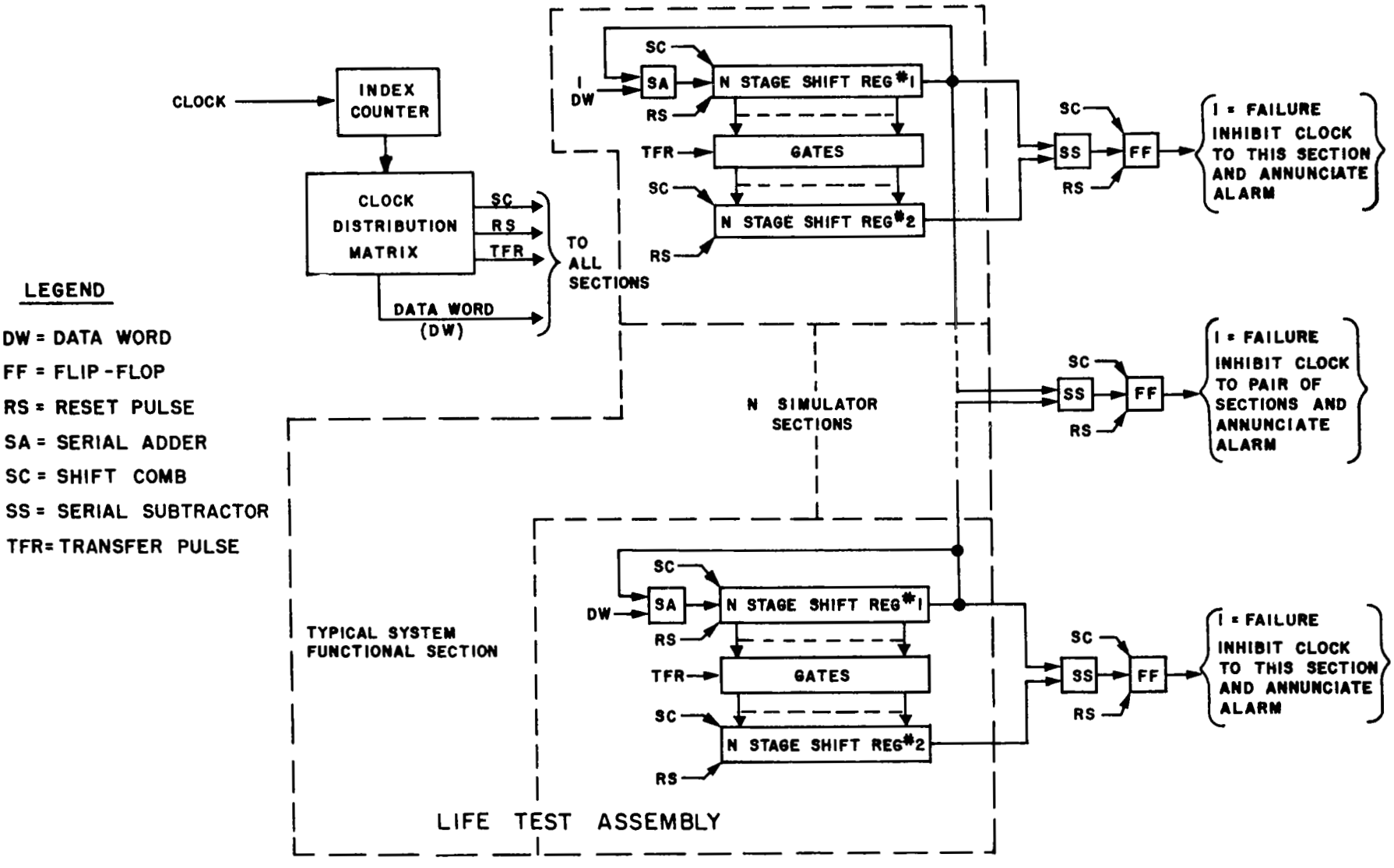
A3 DESCRIPTION OF SAMPLE

A generalized block diagram of the test sample unit to be considered for this reliability program is shown in Figure A-4. It is designed to include all the functions normally used in a digital control system and to exercise the logic elements in a manner duplicating system operation.

The sample unit consists of a serial adder, two shift registers, and a number of transfer gates.

Operation of a sample unit would be as follows:

> A data word, numerically equal to one, would shift, serially, into shift register Number 1. By parallel transfer, data from shift register Number 1 would be entered into shift register Number 2. Both registers now contain the same data.
>
> A new data word, equal to one, enters the adder and, due to the recirculation loop, is added to the previous content of shift register Number 1. During this same shift data from register Number 2 is subtracted from the initial data in register Number 1. If a difference occurs, failure is indicated and a failure alarm flip-flop is set. If no error has occurred, the cycle continues with register content increasing by one, each word time. When an overflow occurs, the registers are set to zero and the entire program repeats.



SAMPLE UNIT BLOCK DIAGRAM - DIGITAL SYSTEM RELIABILITY TEST
FIGURE A-4

All sample units under test, even though each is undergoing a different test, get the same data word at the same time, shift in synchronism, and transfer data at the same time. All registers, then, should contain the same number at the end of any word time.

Failure detection within a unit has been described above. The same method would be used to detect differences between any one unit and another. The comparison could be cascaded to cover all possible combinations, although this appears to be impractical.

Failure is thus defined as erroneous data in any one or more registers at the end of any word time.

Each unit, under test, would be provided with individual elapsed time indicators. In event of failure the fail indicate flip-flop would stop the faulty unit, or units, and the associated elapsed time indicator(s).

Indicator lights on all registers and fail flip-flops could be used for fault location and correction.

All indicators, serial subtractors, fail flip-flops, master clock index counter, and distribution matrix would be remote from the test environment.

A4 SUMMARY

Consideration of various approaches to reliability testing of digital systems leads to the conclusion that step-stress methods offer the greatest opportunity for obtaining meaningful results in the least amount of time and at minimum cost. A reasonable means of selecting a test sample has been determined which may be applied to the majority of digital systems.

Certain assumptions have been made with regard to the application of step-stress testing for which no rigorous justification can be found within the state-of-the-art. This is particularly true in the area of extrapolation of short-time data to long-time operation through the derivation of acceleration factors. Further study is required to establish confidence in such a hypothesis. The advantages of the step-stress method, however, clearly warrant such continued study to either prove or disprove the theory.

APPENDIX B

GENERAL DESIGN PROCEDURE

FOR

SPACECRAFT CONTROL SYSTEMS

APPENDIX B

GENERAL DESIGN PROCEDURE FOR SPACECRAFT CONTROL SYSTEMS

B1 DESIGN TECHNIQUE

The following is a description of a design technique that applies to any linear, stationary sampled system. A reaction-wheel controlled spacecraft simulator is used as an example of the technique. While this technique can be applied to a controller such as was built under contract NASw 1004, it has been expanded here for the more general case of proportional plus integral plus rate control.

B2 PLANT MODEL

The system is divided into two parts -- the plant and the controller, (see Figure B-1). The plant is defined as that part of the system which cannot or will not be altered during the design. The object, then, is to design a controller that provides the best control of the plant according to some specified criteria.

The first step in the design procedure is to obtain the normal form (State Model) of the plant (see References 6 and 7). For this design procedure, it will be assumed that the output of the plant is a state variable and that the plant inputs are separated into control and disturbance inputs.

The general form of the state model will then be:

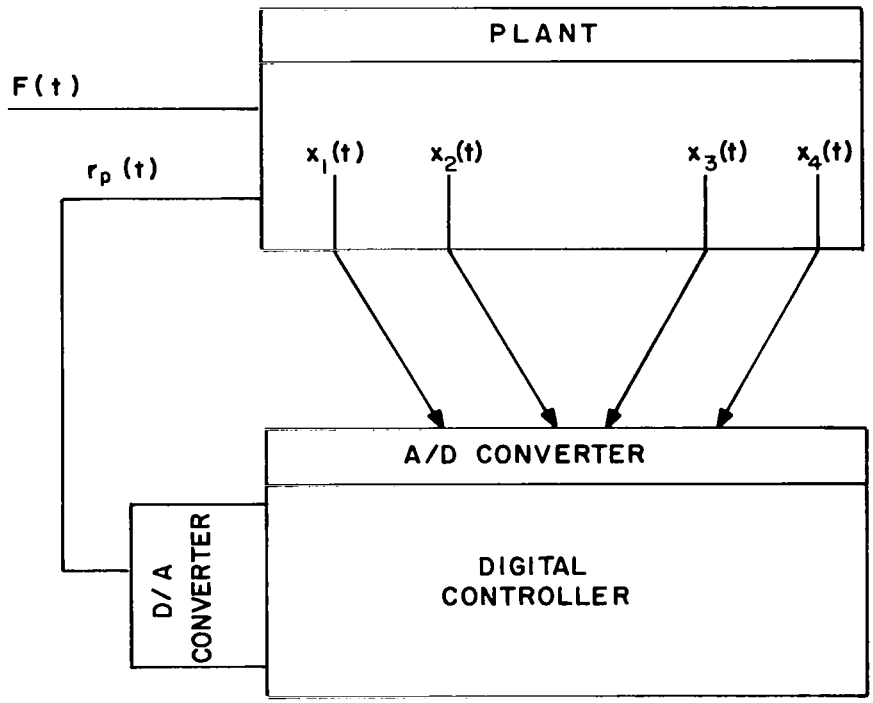
$$\frac{d}{d_t} \underline{X}_p (t) = \underline{A}_p \underline{X}_p (t) + \underline{B}_p \underline{r}_p (t) + \underline{U}_p \underline{F} (t) \qquad \text{Eq. B-1}$$

where

$\underline{X}_p (t)$ = an n dimensional vector

$\underline{A}_p, \underline{B}_p, \underline{U}_p$ = constant matrices

$\underline{r}_p$ = the plant input that will be supplied by the controller, and



GENERAL MODEL OF SAMPLED SYSTEM
FIGURE B-1

$\underline{F}$ (t) = the external disturbance.

The spacecraft, the reaction wheel and motor, and the amplifier are defined as the plant. The model is obtained as follows:

Reaction Wheel: $$\frac{dw_w}{d_t} = \frac{L_w}{I_w} \qquad \text{Eq. B-2}$$

Spacecraft: $$\frac{dw_s}{d_t} = \frac{L_s}{I_w} \qquad \text{Eq. B-3}$$

Torque Motor: $$L_m = Bw_m + KV_6 \qquad \text{Eq. B-4}$$

where

W_w = reaction wheel velocity

L_w = reaction wheel torque

I_w = reaction wheel inertia

= $0.367\ (10^4)$ gm-cm^2

W_s = spacecraft velocity

L_s = spacecraft torque

I_s = spacecraft inertia

= $0.333\ (10^8)$ gm-cm^2

L_m = motor torque

B = damping

= 25.32 dyne-cm/rad/sec

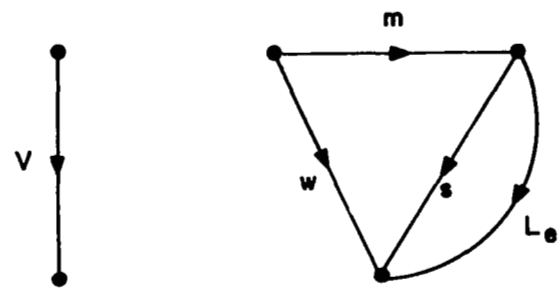
K = gain (including amplifier)

= $0.424\ (10^6)$ dyne-cm/volt

V_6 = amplifier input

and the values given are those for an experimental spacecraft simulator that was available for laboratory use.

The terminal graph of this plant is



where L_e is the external disturbance torque.

Now, from conservation of momentum:

$$I_w (W_w) + I_s (W_s) + \int_{-\infty}^{t} L_e \, dt = 0 \qquad \text{Eq. B-5}$$

$$W_w = -\frac{I_s (W_s)}{I_w} - \frac{1}{I_w} \int_{-\infty}^{t} L_e \, dt$$

or

$$\frac{d}{d_t} (W_w) = \left(-\frac{I_s}{I_w}\right) \left[\frac{d}{d_t} (W_s)\right] - \frac{L_e}{I_w} \qquad \text{Eq. B-6}$$

From Equation B-2 and the terminal graph,

$$\frac{d}{d_t} (W_w) = -\frac{L_m}{I_w} = -\frac{B (W_m) - KV_6}{I_w}$$

and with the approximation that $W_m \approx W_w$,

$$\frac{d}{d_t}(W_w) = -\frac{B(W_w) - KV_6}{I_w} \qquad \text{Eq. B-7}$$

From Equations B-6 and B-7

$$\frac{d}{d_t}(W_w) = \left(-\frac{I_s}{I_w}\right)\left[\frac{d}{d_t}(W_s)\right] - \frac{L_e}{I_w} = -\frac{B(W_w) - KV_6}{I_w}$$

or

$$\frac{d}{d_t}(W_s) = \frac{1}{I_s}\left[B(W_w) + KV_6\right] \frac{-L_e}{I_s}$$

$$= \frac{1}{I_s}\left\{B\left[-\frac{I_s(W_s)}{I_w} - \frac{1}{I_w}\int_{-\infty}^{t} L_e\, dt\right] + KV_6\right\} - \frac{L_e}{I_s}$$

$$= -\frac{B}{I_w}(W_s) + \frac{KV_6}{I_s} - \frac{B}{I_s I_w}\int_{-\infty}^{t} L_e\, dt - \frac{L_e}{I_s}$$

Eq. B-8a

Let

$$f(t) = +\frac{B}{I_s I_w}\int_{-\infty}^{t} L_e\, dt + \frac{L_e}{I_s} \qquad \text{Eq. B-8b}$$

$$\alpha = \frac{B}{I_w}, \text{ and}$$

$$\frac{d}{dt}(\theta_s) = W_s \qquad \text{Eq. B-9}$$

where

θ_s = spacecraft position

Thus, Equations B-8a and B-9 may be written as

$$\begin{bmatrix} \frac{d}{dt}(W_s) \\ \\ \frac{d}{dt}(\theta_s) \end{bmatrix} = \begin{bmatrix} -\alpha & 0 \\ \\ 1 & 0 \end{bmatrix} \begin{bmatrix} W_s \\ \\ \theta_s \end{bmatrix} + \begin{bmatrix} \frac{K}{I_s} \\ \\ 0 \end{bmatrix} V_6 + \begin{bmatrix} -1 \\ \\ 0 \end{bmatrix} f(t) \qquad \text{Eq. B-10}$$

which is in the form required by Equation B-1.

B3 DISCRETE PLANT MODEL

The continuous plant model is next converted to a system of linear difference equations that provide information only at the sampling instants.

The general solution to Equation B-1, subject to the initial conditions,

$$\underline{X}\Big|_{t = t_o} = \underline{X}_{t_o}$$

and that

$$\underline{F}(T) = \underline{F}_{t_o} \quad \text{and} \quad \underline{r}(T) = \underline{r}_{t_o} \quad \text{for } t_o \leq \underline{T} < t$$

can be written as

$$\underline{X} = e^{\underline{A}_p (t - t_o)} \underline{X}_{t_o} + \int_{t_o}^{t} e^{\underline{A}_p (t - T)} \left[\underline{B}_p \underline{r}(T) + \underline{U}_p \underline{F}(T) \right] dT$$

Eq. B-11

where

$$e^{\underline{A}_p (t - t_o)} = \underline{U} + \underline{A}_p (t - t_o) + \frac{\underline{A}_p^2 (t - t_o)^2}{2!} + \frac{\underline{A}_p^3 (t - t_o)^3}{3!} + \ldots$$

$$\ldots + \frac{\underline{A}_p^n (t - t_o)^n}{n!} + \ldots\ldots$$

The matrix, $e^{\underline{A}_p (t - t_o)}$ and the convolution integral of Equation B-11 can be evaluated by functions of matrices (see Reference 8). The general form of the results are given by the vector equation

$$\underline{X}_p (k + 1) = \underline{A}_p^* \underline{X}_p (k) + \underline{B}_p^* \underline{r}(k) + \underline{U}_p^* \underline{F}(k) \qquad \text{Eq. B-12a}$$

where

$\underline{X}(k) = \underline{X}_{t_o}$

$\underline{r}(k) = \underline{r}_{t_o}$

$\underline{F}(k) = \underline{F}_{t_o}$

$\underline{X}(k+1) = \underline{X}_{(t_o + h)}$

h = the sampling period.

Replacing k by k-1 in Equation B-12a gives

$$\underline{X}_p(k) = \underline{A}_p^* \underline{X}_p(k-1) + \underline{B}_p^* \underline{r}(k-1) = \underline{U}_p^* \underline{F}(k-1) \quad . \qquad \text{Eq. B-12b}$$

For the particular plant given in Equation B-10, the eigenvalues of $\underline{A}p$ are determined as the roots of the following equation.

$$\det \begin{bmatrix} -\alpha & -\lambda & 0 \\ 1 & 0 & -\lambda \end{bmatrix} = 0$$

or

$$\lambda(\lambda + \alpha) = 0 \qquad \text{Eq. B-13}$$

From Equation B-13, the eigenvalues are determined as

$$\lambda_1 = 0$$

$$\lambda_2 = -\alpha$$

Therefore,

$$f(\underline{A}_p) = \underline{Z}_{11} f(\lambda_1) + \underline{Z}_{21} f(\lambda_2) \qquad \text{Eq. B-14}$$

where $\underline{Z}_{11}$ and $\underline{Z}_{21}$ are constituent matrices.

Let

$$f(\underline{A}_p) = (\underline{A}_p - \lambda_2 \underline{U})$$

then

$$(\underline{A}_p - \lambda_2 \underline{U}) = \underline{Z}_{11}(\lambda_1 - \lambda_2) + \underline{Z}_{21} \cdot 0$$

and solving for $\underline{Z}_{11}$ gives

$$\underline{Z}_{11} = \frac{1}{\lambda_1 - \lambda_2} \left[\underline{A}_p - \lambda_2 \underline{U} \right] = \frac{1}{\alpha} \begin{bmatrix} -\alpha + \alpha & 0 \\ 1 & 0 + \alpha \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \frac{1}{\alpha} & 1 \end{bmatrix}$$

Eq. B-15

Since $\underline{Z}_{11} + \underline{Z}_{21} = \underline{U}$ (see Reference 6),

$$\underline{Z}_{21} = \underline{U} - \underline{Z}_{11} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{\alpha} & 0 \end{bmatrix}$$

Therefore,

$$e^{\underline{A}_p (t - T)} = \begin{bmatrix} 0 & 0 \\ \frac{1}{\alpha} & 1 \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ -\frac{1}{\alpha} & 0 \end{bmatrix} e^{-\alpha (t - T)}$$

and

$$\int_{t_o}^{t} e^{\underline{A}_p (t - T)} dt = \int_{t_o}^{t} \left[\underline{Z}_{11} + \underline{Z}_{21} e^{-\alpha (t - T)} \right] dT$$

$$= \underline{Z}_{11} (t - t_o) + \underline{Z}_{21} \left[\frac{1 - e^{-\alpha (t - t_o)}}{\alpha} \right]$$

With $\underline{r}$ (T) and $\underline{F}$ (T) constant for $t_o \leq T < t$ and with $t = t_o + h$, Equation B-11 can be written as

$$\underline{X}(t_o + h) = \left(Z_{11} + Z_{21}\, e^{-\alpha h}\right) \underline{X}_{t_o} + \left[\underline{Z}_{11}\, h + \underline{Z}_{21}\left(\frac{1 - e^{-\alpha h}}{\alpha}\right)\right]\left[\underline{B}_p\, \underline{r}(t_o) + \underline{U}_p\, \underline{F}(t_o)\right] \qquad \text{Eq. B-16}$$

In detail, with

$$\underline{X}(t_o + h) = \underline{X}(k),$$

$$\underline{X}(t_o) = \underline{X}(k-1),$$

$$\underline{r}(t_o) = \underline{r}(k-1), \text{ and}$$

$$\underline{F}(t_o) = \underline{F}(k-1)$$

the difference equations describing the plant given in Equation B-10 are written as

$$\begin{bmatrix} W_s(k) \\ \theta_s(k) \end{bmatrix} = \left\{\begin{bmatrix} 0 & 0 \\ \frac{1}{\alpha} & 1 \end{bmatrix} + \begin{bmatrix} e^{-\alpha h} & 0 \\ \frac{-e^{-\alpha h}}{\alpha} & 0 \end{bmatrix}\right\} \begin{bmatrix} W_s(k-1) \\ \theta_s(k-1) \end{bmatrix} +$$

$$\left\{\begin{bmatrix} 0 & 0 \\ \frac{h}{\alpha} & h \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ \frac{-1}{\alpha} & 0 \end{bmatrix}\left(\frac{1 - e^{-\alpha h}}{\alpha}\right)\right\}$$

$$\left\{\begin{bmatrix} \frac{K}{I_s} \\ 0 \end{bmatrix} V_6(k-1) + \begin{bmatrix} -1 \\ 0 \end{bmatrix} f(k-1)\right\}$$

which, after some manipulation, may be written:

$$\begin{bmatrix} W_s\ (k) \\ \theta_s\ (k) \end{bmatrix} = \begin{bmatrix} e^{-\alpha h} & 0 \\ \dfrac{1-e^{-\alpha h}}{\alpha} & 1 \end{bmatrix} \begin{bmatrix} W_s\ (k-1) \\ \theta_s\ (k-1) \end{bmatrix} +$$

$$\begin{bmatrix} \dfrac{K}{I_s} & \dfrac{1-e^{-\alpha h}}{\alpha} \\ \dfrac{K}{I_s}\left(\dfrac{h}{\alpha} - \dfrac{1-e^{-\alpha h}}{\alpha}\right) \end{bmatrix} V_6\ (k-1) + \begin{bmatrix} -\dfrac{1-e^{-\alpha h}}{\alpha} \\ -\dfrac{h}{\alpha} + \dfrac{1-e^{-\alpha h}}{\alpha^2} \end{bmatrix} f\,(k-1)$$

Eq. B-17

which is in the form of Equation B-12b.

B4 CONTROLLER MODEL AND INTERCONNECTION

The general form of a digital controller is assumed as

$$\underline{X}_c\ (k) = \underline{A}_c\,\underline{X}_c\ (k-1) + \underline{B}_c\,\underline{U}_c\ (k) \qquad \text{Eq. B-18a}$$

$$\underline{V}_c\ (k) = \underline{C}_c\,\underline{X}_c\ (k) + \underline{D}_c\,\underline{U}_c\ (k) \qquad \text{Eq. B-18b}$$

where

$\underline{X}_c\ (k)$ = controller state vector

$\underline{U}_c\ (k)$ = controller input vector

$\underline{V}_c\ (k)$ = controller output vector

A , B , C and D = constant matrices that are to be determined for the best control of the plant.

As can be seen from the model, the controller storage (state) $\underline{X}_c(k)$ is determined by a linear combination of the previous storage (state) and the present inputs. It is assumed that the controller and plant will be interconnected in the feedback configuration of Figure B-2. Thus,

$$\underline{U}_c(k) = \underline{R}(k) - \underline{X}_p(k)$$

For the plant given in B-17, the simplest controller that provides proportional, rate and integral control is selected. The state model of this controller is

$$X_3(k) = X_3(k-1) + \begin{bmatrix} P_4 & P_3 \end{bmatrix} \begin{bmatrix} U_1(k) \\ U_2(k) \end{bmatrix} \qquad \text{Eq. B-19a}$$

$$V_c(k) = X_3(k) + \begin{bmatrix} P_1 & P_2 \end{bmatrix} \begin{bmatrix} U_1(k) \\ U_2(k) \end{bmatrix} \qquad \text{Eq. B-19b}$$

where

$X_3(k)$ = the content of a storage register

P_1, P_2, P_3, and P_4 = constants to be determined

$U_1(k)$ and $U_2(k)$ = inputs

With $\underline{R} = 0$, Figure B-2 provides

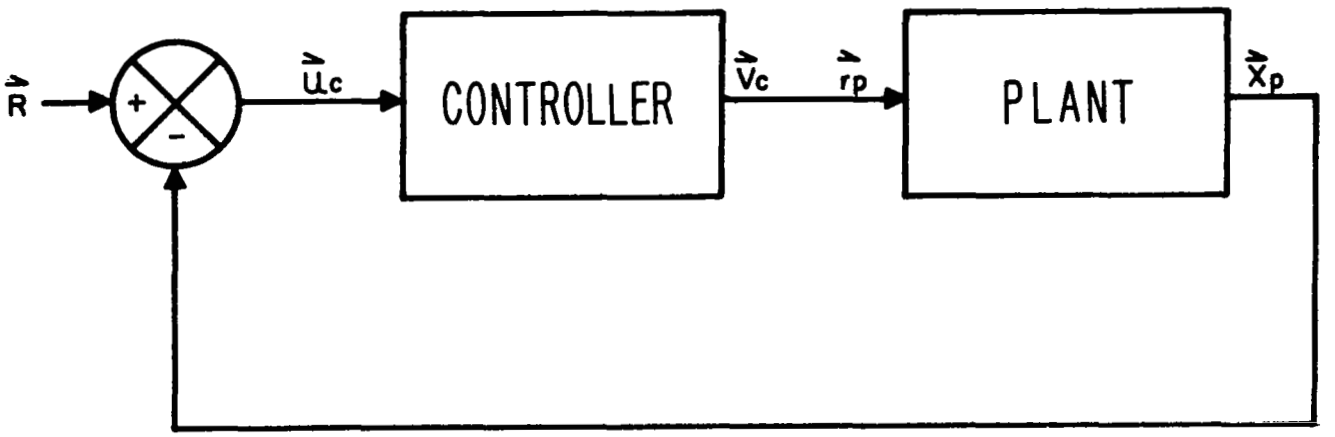
$$U_1(k) = -W_s(k)$$

$$U_2(k) = -\theta_s(k)$$

The matrices of Equation B-18 are

$$\underline{A}_c = 1 \qquad \text{Eq. B-20a}$$

$$\underline{B}_c = \begin{bmatrix} P_4 & P_3 \end{bmatrix} \qquad \text{Eq. B-20b}$$



SYSTEM INTERCONNECTION DIAGRAM
FIGURE B-2

$$\underline{C}_c = 1 \qquad \text{Eq. B-20c}$$

$$\underline{D}_c = \begin{bmatrix} P_1 & P_2 \end{bmatrix} \qquad \text{Eq. B-20d}$$

B5 COMPOSITE SYSTEM EQUATIONS

With the conditions

$$\underline{R} = 0, \ \underline{U}_c = -\underline{X}_p \text{ and } \underline{V}_c = \underline{r}_p \qquad \text{Eq. B-21}$$

Equations B-12b and B-18 may be written as

$$\underline{X}_p(k) = \underline{A}_p^* \underline{X}_p(k-1) + \underline{B}_p^* \underline{V}_c(k-1) + \underline{U}_p^* \underline{F}(k-1) \qquad \text{Eq. B-22}$$

$$\underline{X}_c(k) = \underline{A}_c \underline{X}_c(k-1) - \underline{B}_c \underline{X}_p(k) \qquad \text{Eq. B-23}$$

$$\underline{V}_c(k) = \underline{C}_c \underline{X}_c(k) - \underline{D}_c \underline{X}_p(k) \qquad \text{Eq. B-24}$$

Substituting Equation B-24 into B-22 gives

$$\underline{X}_p(k) = \underline{A}_p^* \underline{X}_p(k-1) + \underline{B}_p^* \underline{C}_c \underline{X}_c(k-1) - \underline{B}_p^* \underline{D}_c \underline{X}_p(k-1) + \underline{U}_p^* \underline{F}(k-1)$$

Eq. B-25

Writing Equations B-23 and B-25 in matrix form

$$\begin{bmatrix} \underline{U} & 0 \\ \underline{B}_c & \underline{U} \end{bmatrix} \begin{bmatrix} \underline{X}_p(k) \\ \underline{X}_c(k) \end{bmatrix} = \begin{bmatrix} \underline{A}_p^* - \underline{B}_p^* \underline{D}_c & \underline{B}_p^* \underline{C}_c \\ 0 & \underline{A}_c \end{bmatrix} \begin{bmatrix} \underline{X}_p(k-1) \\ \underline{X}_c(k-1) \end{bmatrix} +$$

Eq. B-26

$$\begin{bmatrix} \underline{U}_p^* \\ 0 \end{bmatrix} \underline{F}(k-1)$$

Since

$$\begin{bmatrix} \underline{U} & 0 \\ \underline{B}_c & \underline{U} \end{bmatrix}^{-1} = \begin{bmatrix} \underline{U} & 0 \\ -\underline{B}_c & \underline{U} \end{bmatrix}$$

then

$$\begin{bmatrix} \underline{X}_p(k) \\ \underline{X}_c(k) \end{bmatrix} = \begin{bmatrix} \underline{U} & 0 \\ -\underline{B}_c & \underline{U} \end{bmatrix} \begin{bmatrix} A_p^* - \underline{B}_p^* \underline{D}_c & \underline{B}_p^* \underline{C}_c \\ 0 & A_c \end{bmatrix} \begin{bmatrix} \underline{X}_p(k-1) \\ \underline{X}_c(k-1) \end{bmatrix} + \begin{bmatrix} \underline{U} & 0 \\ -\underline{B}_c & \underline{U} \end{bmatrix} \begin{bmatrix} \underline{U}_p^* \\ 0 \end{bmatrix} \underline{F}(k-1)$$

$$= \begin{bmatrix} \underline{A}_p^* - \underline{B}_p^* \underline{D}_c & \underline{B}_p^* \underline{C}_c \\ -\underline{B}_c \underline{A}_p^* + \underline{B}_c \underline{B}_p^* \underline{D}_c & -\underline{B}_c \underline{B}_p^* \underline{C}_c + \underline{A}_c \end{bmatrix} \begin{bmatrix} \underline{X}_p(k-1) \\ \underline{X}_c(k-1) \end{bmatrix} + \begin{bmatrix} \underline{U}_p^* \\ -\underline{B}_c U_p^* \end{bmatrix} \underline{F}(k-1)$$

Eq. B-27

From Equation B-17

$$\underline{A}_p^* = \begin{bmatrix} e^{-\alpha h} & 0 \\ \dfrac{1 - e^{-\alpha h}}{\alpha} & 1 \end{bmatrix} \equiv \begin{bmatrix} A_{P11} & 0 \\ A_{P21} & 1 \end{bmatrix}$$

$$\underline{B}_p^* = \begin{bmatrix} \dfrac{K}{I_s} \dfrac{1 - e^{-\alpha h}}{\alpha} \\ \dfrac{K}{I_s} \left(\dfrac{h}{\alpha} - \dfrac{1 - e^{-\alpha h}}{\alpha} \right) \end{bmatrix} \equiv \begin{bmatrix} B_{P11} \\ B_{P21} \end{bmatrix}$$

$$\underline{U}_p^* = \begin{bmatrix} - \dfrac{1 - e^{-\alpha h}}{\alpha} \\ - \left(\dfrac{h}{\alpha} - \dfrac{1 - e^{-\alpha h}}{\alpha} \right) \end{bmatrix} \equiv \begin{bmatrix} U_{P11} \\ U_{P21} \end{bmatrix}$$

and since

$$\underline{A}_c = 1$$

$$\underline{B}_c = \begin{bmatrix} P_4 & P_s \end{bmatrix}$$

$$\underline{C}_c = 1$$

$$\underline{D}_c = \begin{bmatrix} P_1 & P_2 \end{bmatrix}$$

then

$$\begin{bmatrix} W_s\ (k) \\ \theta_s\ (k) \\ X_3\ (k) \end{bmatrix} = \begin{bmatrix} A_{P11} - P_1 B_{P11} & -P_2 B_{P11} & B_{P11} \\ A_{P21} - P_1 B_{P21} & 1 - P_2 B_{P21} & B_{P21} \\ -P_4 A_{P11} - P_3 A_{P21} + P_1 (P_4 B_{P11} + P_3 B_{P21}) & -P_3 + P_2 (P_4 B_{P11} + P_3 B_{P21}) & 1 - P_4 B_{P11} - P_3 B_{P21} \end{bmatrix}$$

$$\begin{bmatrix} W_s\ (k-1) \\ \theta_s\ (k-1) \\ X_3\ (k-1) \end{bmatrix} + \begin{bmatrix} U_{P11} \\ U_{P21} \\ -P_4 U_{P11} - P_3 U_{P21} \end{bmatrix} f\ (k-1)$$

Eq. B-28

B6 OPTIMIZATION

The design objective is to determine the controller parameters, that is to say the values of P_1, P_2, P_3, and P_4, which will produce minimum pointing error for a specified expenditure of energy (cost), given that the plant disturbance is of a particular form, i.e.,

$$\text{ERROR} = \text{minimum}$$

$$\text{COST} = \text{specified energy}$$

This problem can be viewed as a conventional Lagrange Multiplier problem in which the function

$$Q = \text{ERROR} + W\,(\text{COST})$$

is minimized. Normally the Lagrange Multiplier, W, is determined from the partial derivatives of Q with respect to the parameters along with the constraint equations. In this procedure, however, W is treated as a pre-assigned weight and Q is minimized with respect to the controller parameters by a one-dimensional computer search. With the particular parameters that minimize Q, both error and cost are numerically evaluated. If the specified cost is then considered as the computed value of cost, the value of error will then be minimum with respect to the controller parameters subject to the specified cost constraint. The process is repeated for many values of W and a trade-off curve of error versus minimum cost is generated.

To prepare a computer program the spacecraft error function was selected as

$$\int_0^\infty \left|\text{spacecraft pointing error}\right| \, dt$$

with the integral being approximated by the trapezoidal rule. The cost function was selected as

$$\int_0^\infty \left|\text{spacecraft and acceleration}\right| \, dt$$

because of the apparent relationship between acceleration and integrated power (energy). This latter integral was approximated by the rectangular rule. The integral approximations are made over a sufficiently long, though finite, time to assure good accuracy. The external disturbance was assumed to be a torque impulse of 10^5 dyne-cm-sec applied to the laboratory spacecraft simulator immediately after a sampling instant. This "worst case" condition is accounted for by the proper specification of the spacecraft initial conditions,

$$W_s\ (t_o) = \frac{-10^5}{I_s}$$

and

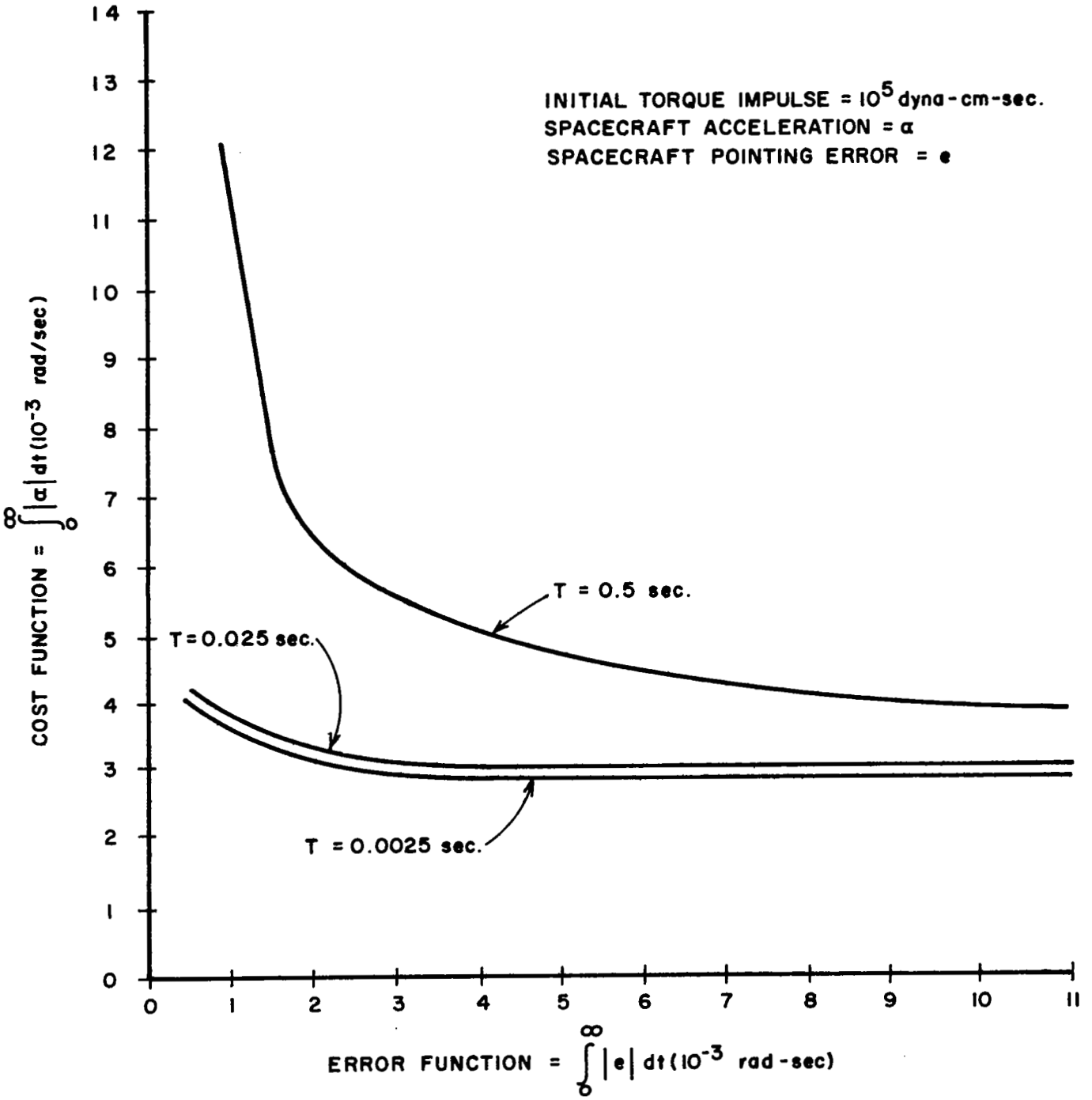
$$\theta_s (t_o) = h \left[W_s\ (t_o) \right]$$

where the initial position, $\theta_s\ (t_o)$, is equal to the initial pointing error by the conditions of Equation B-21. Also from Equation B-8b

$$f\ (t) = f\ (k) = \text{a constant} = \frac{B\ (10^5)}{I_s\ I_w}$$

During early tests of the computer program parameter P_4 was found to have little effect on the trade-off curve and hence it was set to zero. It should be noted that, with reference to a physical controller, the parameters P_1, P_2, and P_3 represent integrator gain, rate gain and proportional gain, respectively.

Figure B-3 shows a resulting family of trade-off curves for various sample periods. A listing of the computer program which generates these curves is given in Figure B-4.



COST VS. PERFORMANCE TRADE-OFFS
FOR A SINGLE AXIS SYSTEM
FIGURE B-3

```
ZZJOB 5012
ZZFORX
C       DIGITAL CONTROLLER OPTIMIZATION PROGRAM
        DIMENSION P(10),PINC(10),X(10),WX(10),A(10,10),B(10),C(10),S(10)
       1,WWX(10),EP(20),CP(20)
      2 FORMAT(1X,18HINITIAL PARAMETERS,5X,27HINITIAL PARAMETER INCREMENT)
      3 FORMAT(7X,E10.3,17X,E10.3)
      4 FORMAT(///,14X,8HWEIGHT =,E10.3,/)
      5 FORMAT(///)
      6 FORMAT(1X,14HINITIAL COST =,E10.3)
      7 FORMAT(1X,15HINITIAL ERROR =,E10.3,//)
      8 FORMAT(/,1X,11HINITIAL Q =,E10.3)
      9 FORMAT(1X,2HQ=,E10.3)
     10 FORMAT(7X,10HPARAMETERS,18X,9HTOLERANCE)
     11 FORMAT(///,1X,19HFINAL VALUES FOR W=,E10.3,/)
     12 FORMAT(1X,6HCOST =,E10.3)
     13 FORMAT(1X,7HERROR =,E10.3,//)
     14 FORMAT(16I5)
     15 FORMAT(8E10.3)
     16 FORMAT(1X,7HWEIGHT=,E10.3)
     18 FORMAT(1X,16HNUM IS TOO SMALL)
     19 FORMAT(34X,3HH =,E10.3,//)
     20 FORMAT(8E10.3)
    110 FORMAT(25X18HSAMPLING PERIOD = E10.3)
        CALL CENTER
        CALL DATE
        CALL CENTER
     21 READ 15,W,WDIV,WMIN,H,DAMP,WI,GAIN,SI,PULSE,HEFF
        READ 15,NORD,NPAR,NDIV,NUM,ISTOP
        KZ=1
        READ 15,(P(I),I=1,NPAR)
        READ 15,(PINC(I),I=1,NPAR)
        PUNCH 19,H
        PUNCH 110,HEFF
        CALL CENTER
        DO 17 JJ=1,NPAR
        C(JJ)=0.
     17 S(JJ)=PINC(JJ)
     60 KK=1
        GO TO 200
     25 PUNCH 4,W
        PUNCH 2
        DO 26 I=1,NPAR
     26 PUNCH 3,P(I),PINC(I)
        PUNCH 4,W
        COST=H*CST
        ERROR=H*ERR
        QMIN=QTEST
        PUNCH 8,QMIN
        PUNCH 6,COST
        PUNCH 7,ERROR
    100 DO 39 K=1,NDIV
    101 DO 43 I=1,NPAR
     27 P(I)=P(I)+PINC(I)
        KK=2
        GO TO 201
     28 IF (QTEST-QMIN) 29,30,30
     29 QMIN=QTEST
        COST=H*CST
        ERROR=H*ERR
```

DIGITAL CONTROLLER OPTIMIZATION PROGRAM
FIGURE B-4 (1 of 3)

```
      C(I)=1.
      GO TO 27
   30 P(I)=P(I)-PINC(I)
      IF(C(I))31,31,43
   31 P(I)=P(I)-PINC(I)
      KK=3
      GO TO 201
   32 IF(QTEST-QMIN)33,34,34
   33 QMIN=QTEST
      ERROR=H*ERR
      COST=H*CST
      C(I)=1.
      GO TO 31
   34 P(I)=P(I)+PINC(I)
   43 CONTINUE
      SUM=0.
   35 DO 36 J=1,NPAR
   36 SUM=SUM+C(J)
      IF(.1-SUM)44,44,37
   44 DO 45 J=1,NPAR
   45 C(J)=0.
      GO TO 101
   37 PUNCH 9,QMIN
      PUNCH 10
      DO 38 J=1,NPAR
      PUNCH 3,P(J),PINC(J)
   38 PINC(J)=PINC(J)/4.
   39 CONTINUE
      DO 50 J=1,NPAR
   50 PINC(J)=PINC(J)*4.
      IF(ABSF(1.-DCST/CST)-.0005)51,51,52
   51 IF(ABSF(1.-DERR/ERR)-.0005)53,53,52
   52 PUNCH 18
   53 PUNCH 11,W
      PUNCH 9,QMIN
      PUNCH 12,COST
      PUNCH 13,ERROR
      KZ=KZ+1
      PUNCH 10
      DO 40 I=1,NPAR
   40 PUNCH 3,P(I),PINC(I)
      IF (W-WMIN)300,41,41
   41 W=W/WDIV
      DO 42 I=1,NPAR
   42 PINC(I)=S(I)
      PUNCH 5
      IF(KZ-1-ISTOP)60,300,300
C     PLANT EQUATIONS START HERE
  200 ALPHA=DAMP/WI
      X(1)=-PULSE/SI
      X(2)=HEFF*X(1)
      X(3)=0.
      FOFT=PULSE*DAMP/(WI*SI)
      AP11=EXPF(-ALPHA*H)
      AP21=(1.-EXPF(-ALPHA*H))/ALPHA
      AP22=1.
      BP11=AP21*GAIN/SI
      BP21=(H-AP21)*GAIN/(ALPHA*SI)
      UP11=-AP21
      UP21=-(H-AP21)/ALPHA
```

DIGITAL CONTROLLER OPTIMIZATION PROGRAM
FIGURE B-4 (2 of 3)

```
C       PLANT EQUATIONS END AND SYSTEM EQUATIONS START HERE
  201 A(1,1)=AP11-BP11*P(1)
      A(1,2)=-BP11*P(2)
      A(1,3)=BP11
      A(2,1)=AP21-BP21*P(1)
      A(2,2)=1.-BP21*P(2)
      A(2,3)=BP21
      A(3,1)=-P(3)*AP21+P(1)*P(3)*BP21
      A(3,2)=-P(3)+P(2)*P(3)*BP21
      A(3,3)=1.-P(3)*BP21
      B(1)=UP11*FOFT
      B(2)=UP21*FOFT
      B(3)=-P(3)*UP21*FOFT
      DO 202 II=1,NORD
  202 WX(II)=X(II)
      CST=0.
      ERR=0.
      BETA=(GAIN*P(1)/SI)+ALPHA
      DELTA=GAIN*P(2)/SI
      GAMMA=GAIN/SI
      ACC=-BETA*WX(1)-DELTA*WX(2)+GAMMA*WX(3)-FOFT
      CST=ABSF(ACC)
      DO 205 LL=1,NUM
      DWX2=WX(2)
      DO 206 II=1,NORD
  206 WWX(II)=0.
      DO 203 II=1,NORD
      DO 203 JJ=1,NORD
  203 WWX(II)=WWX(II)+A(II,JJ)*WX(JJ)
      DO 204 II=1,NORD
  204 WX(II)=WWX(II)+B(II)
      DERR=ERR
      DCST=CST
      ACC=-BETA*WX(1)-DELTA*WX(2)+GAMMA*WX(3)-FOFT
      ERR=ERR+ABSF((DWX2+WX(2))/2.)
      CST=CST+ABSF(ACC)
C       SYSTEM EQUATIONS END HERE
  205 CONTINUE
      QTEST=H*ERR+W*H*CST
      GO TO (25,28,32),KK
  300 CALL EXIT
      END
*DATA
OPTIMIZATION - SPACECRAFT CONTROL SYSTEM

 40.       2.        .625      .5        25.32     3670.     4.24E+05  3.33E+07
 100000.   .0025
 3.        3.        4.        90.       7.
158.7      8.112     .1698
 10.       2.        .3

ZZZZ
```

DIGITAL CONTROLLER OPTIMIZATION PROGRAM
FIGURE B-4 (3 of 3)

APPENDIX C

COMPUTER PROGRAM DATA

- Program Listing
- Program Flow Chart
- Program Description
- Program Symbol Table

APPENDIX C

COMPUTER PROGRAM DATA

C1 STATE MODEL COMPUTER PROGRAM

The state model of the system developed for this study contract was programmed for an IBM 1620 computer using FORTRAN II-D language. This particular computer is rather slow and a review of the program flow chart (Figure A-1) will show that a great amount of computation time was saved by using logical decisions to implement all saturation functions instead of calculating these functions directly.

Numerical integration is carried out by use of a fourth order Runge-Kutta technique which integrates in discrete steps. This method has the advantage that no special computations are needed to start the solution and the error is of the order of h^5, where h is the interval of integration. Consider the equation

$$dy/dx = f(x, y);$$

then the increment for advancing the dependent variable can be found from:

$$y = 1/6\,(k_1 + 2\,k_2 + 2\,k_3 + k_4)$$

where

$$k_1 = h\,f(x_0, y_0)$$

$$k_2 = h\,f(x_0 + h/2, y_0 + k_1/2)$$

$$k_3 = h\,f(x_0 + h/2, y_0 + k_2/2)$$

$$k_4 = h\,f(x_0 + h, y_0 + k_3).$$

Now, setting $x_1 = x_0 + h$ and $y_1 = y_0 + \Delta y$ the process is repeated as required. The program version of this technique can be found in the listing (Figure C-1) beginning at statement 100 and continuing through statement 112. Temporary working values of the state variable (XW) are initialized in statements 5 and 6.

Provision was made in this program to vary the interval of integration (h = DT) so that transient output of the rate network could be observed. In statements 200, 402 and 403 a test is made of the rate of change of voltage across the lead network capacitor and if the slope is greater than a specified value (DVC) the interval of integration is divided by 10. The interval is set back to its normal value as soon as DXDT (5) is less than the test value.

This program was written directly from the block diagram of Figure 6 in the Section 2-3 of this report. Comparison of the program flow chart with this block diagram will show the correspondence. Because of certain limitations placed on the use of characters in the FORTRAN language, however, certain variable symbols used in the block diagram do not appear explicitly in the computer program. A complete listing of the program variables and their definitions appears in Table C-1.

Although this program applies to a specific system and is therefore not of general use the state variable model has proved to be a powerful tool in systems design and analysis. The technique can readily be applied to any systems problem for which a state model can be prepared.

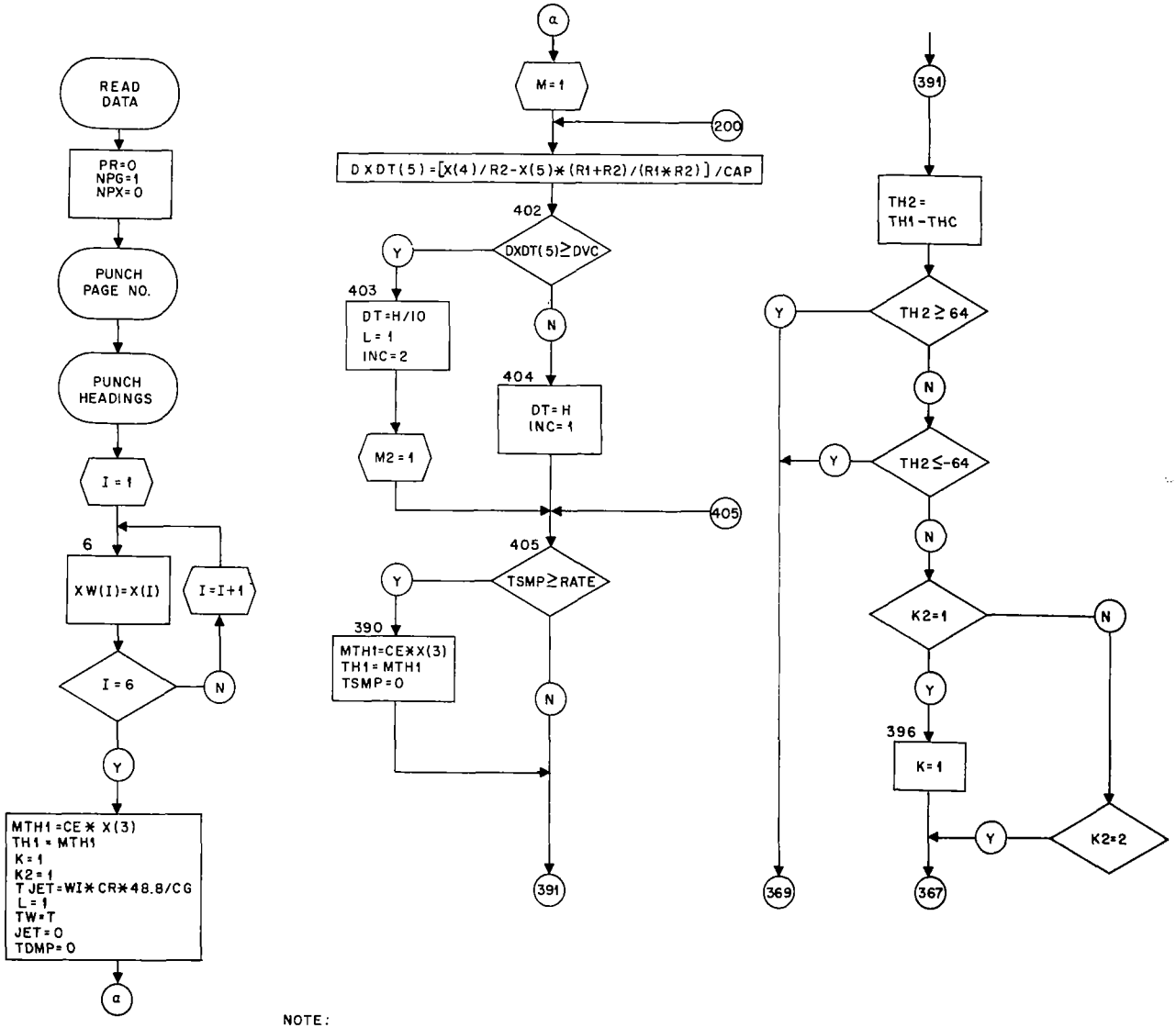
TABLE C-1
PROGRAM SYMBOL TABLE
Page 1 of 4

Program Variables	Definition
CE	Encoder gain, bits/radian
CD	Damping register multiplier
CI	Integrator gain, seconds
CR	Rate multiplier gain, pulses/bit
CG	Reaction where gain, pulses/radian
CDA	D/A converter gain, volts/bit
R1	Lead net series resistor, ohms

Program Variables	Definition
R2	Lead net shunt resistor, ohms
CAP	Lead net capacitor, farads
CC	Chopper gain, $1/2\sqrt{2}$
SI	Spacecraft inertia, gm-cm^2
X(I), I = 1, 2 . . . 6	State variables
WI	Wheel inertia, gm-cm^2
T	Real time, seconds
TI	Test increment, used to assure that integrator will not sample until error value has been tested
THC	θ_c, Spacecraft position, radians
TQE	External disturbance torque, dyne-cm
RATE	Sampling rate set point, seconds
TSMP	dt accummulator
DVC	Runge-Kutta variable increment switch
DPR	Output print interval control
N	Number of state vector calculations
PR	Output print counter
NPG	Output page number
NPX	Page line counter
I	Index variable
MTH1	Largest integer value in spacecraft position data. This is used to simulate real encoder data since fractional values are not available.

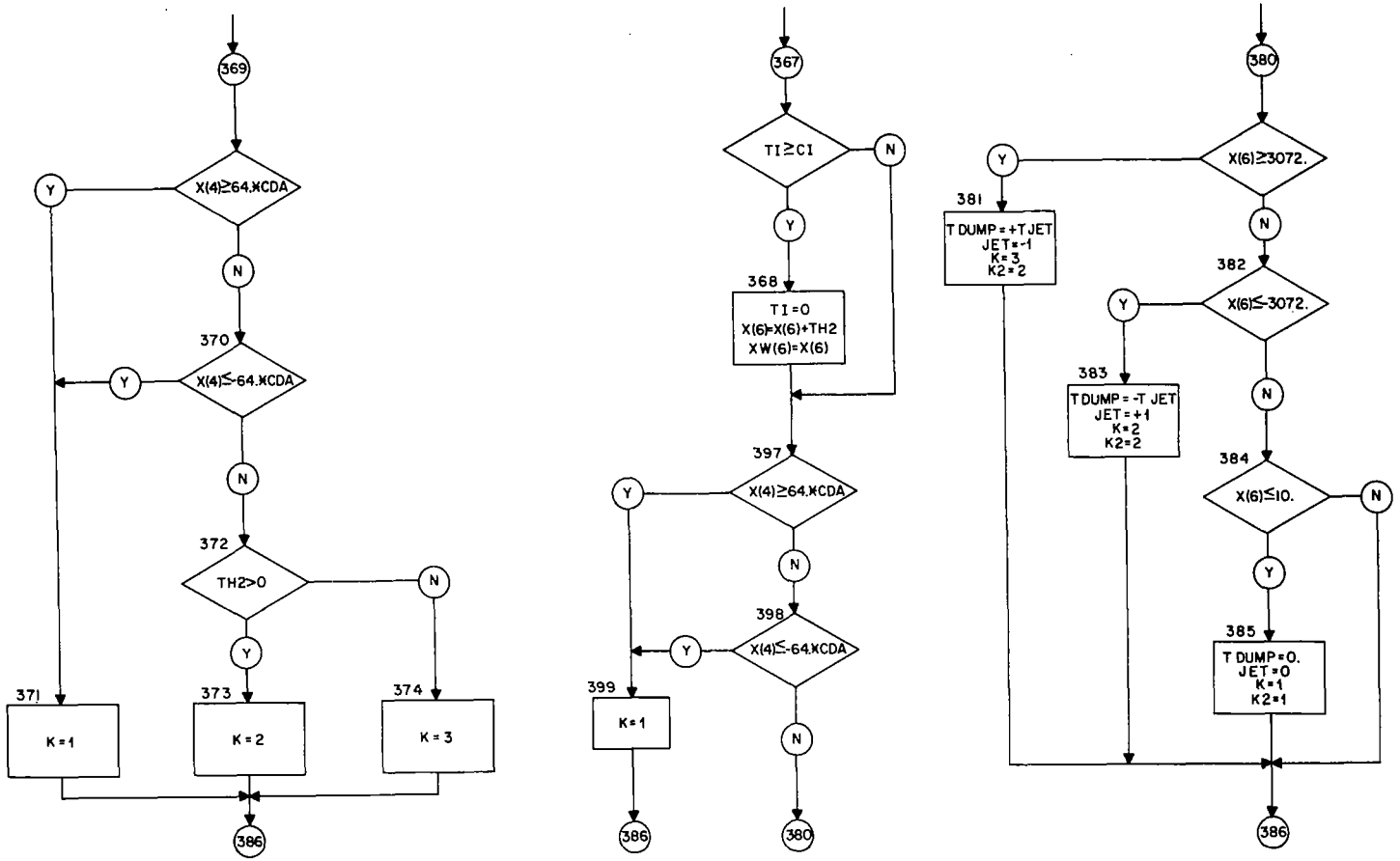
Program Variables	Definition
TH1	Floating point value of MTH1
TJET	Jet torque, for momentum dumping
L	Runge-Kutta flag
JET	Jet on-off indicator
TDUMP	Dump offset correction torque
DI	Time increment
INC	Runge-Kutta variable increment flag
TH5	Sum of proportional and integrator register contents
PRA	PRF of rate multiplier
V7	Lead network output
SV	Sign flag for V6
TL	Load torque
J	Index variable
DEGI	Spacecraft velocity, degrees/sec
DEG3	Spacecraft position, degrees
XW	Runge-Kutta working value of state variables
H	Interval of integration, equal to DT
K	Index variable
K2	Index variable
TW	Runge-Kutta working value for time
M	Index variable

Program Variables	Definition
M2	Index variable
TH2	Error data input to proportional and integrator registers
TH4	Proportional register content
TH6	Buffer register content
PRB	PRF of reaction wheel quantizer
S6	Speed control saturation flag
V6	Amplifier input
TS	Stall torque
IRPS	Reaction wheel velocity, RPS

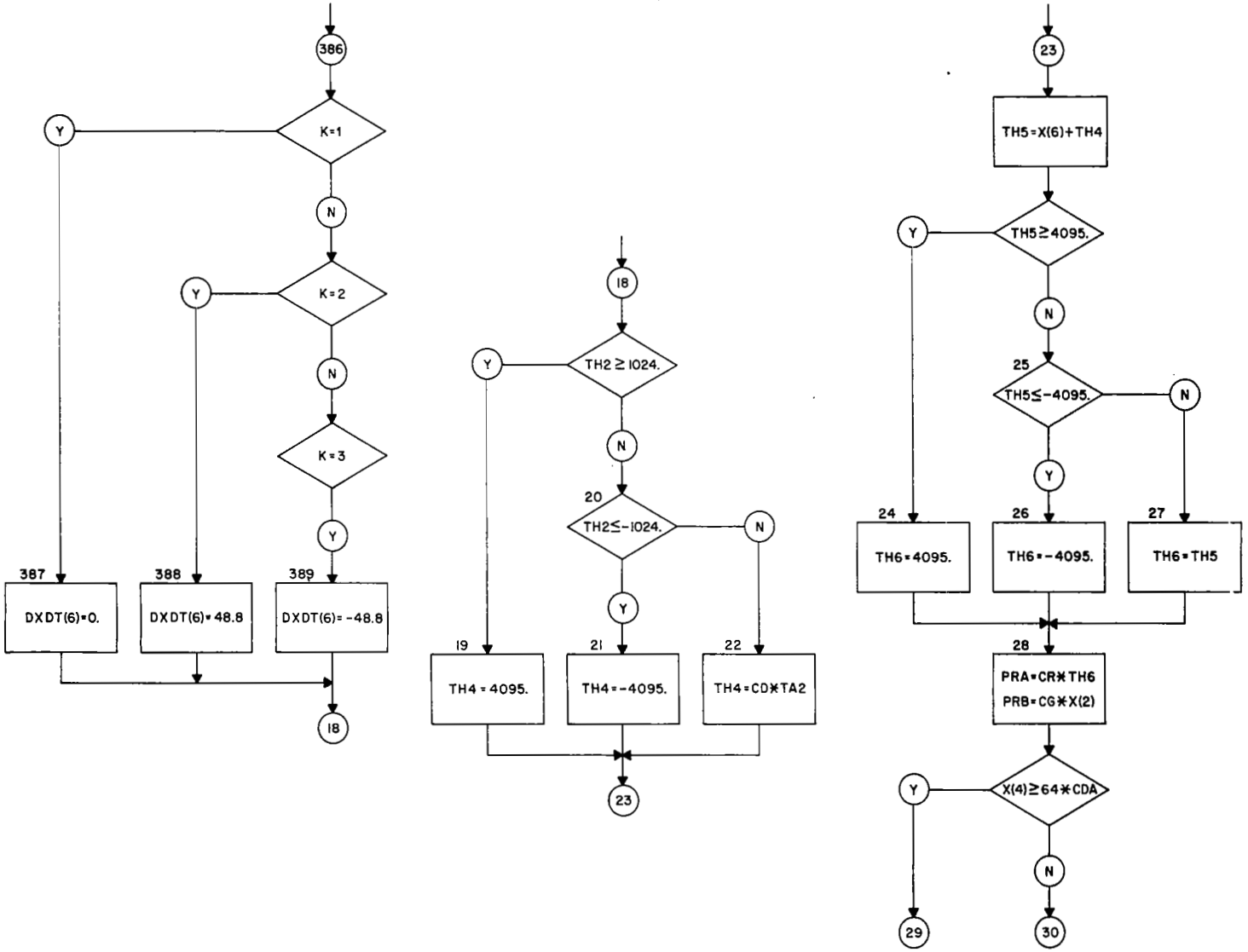


NOTE:
NUMBERS ON CHART ARE STATEMENT NUMBERS.

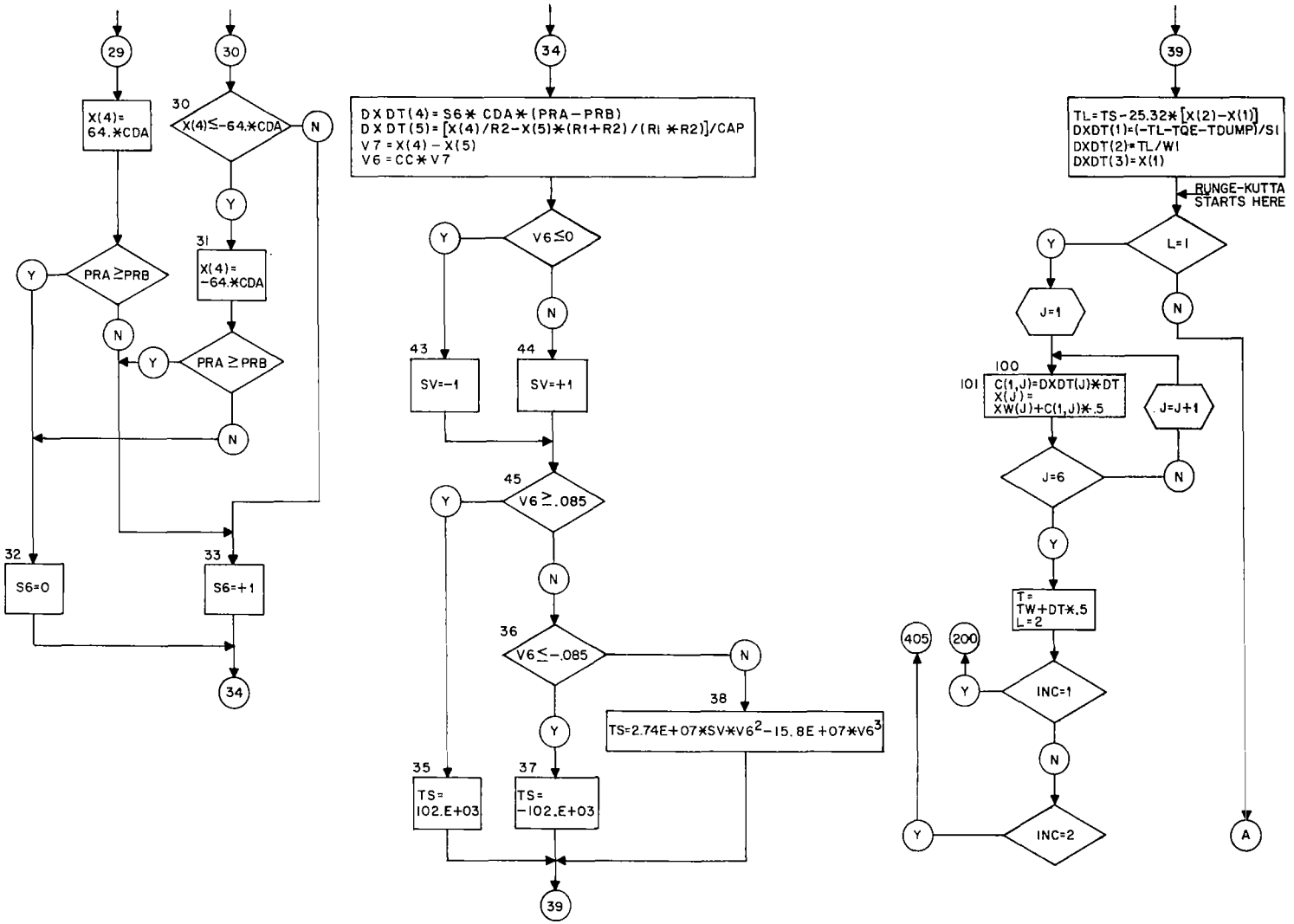
SYSTEM MODEL COMPUTER PROGRAM FLOW CHART
FIGURE C-1 (1 of 6)



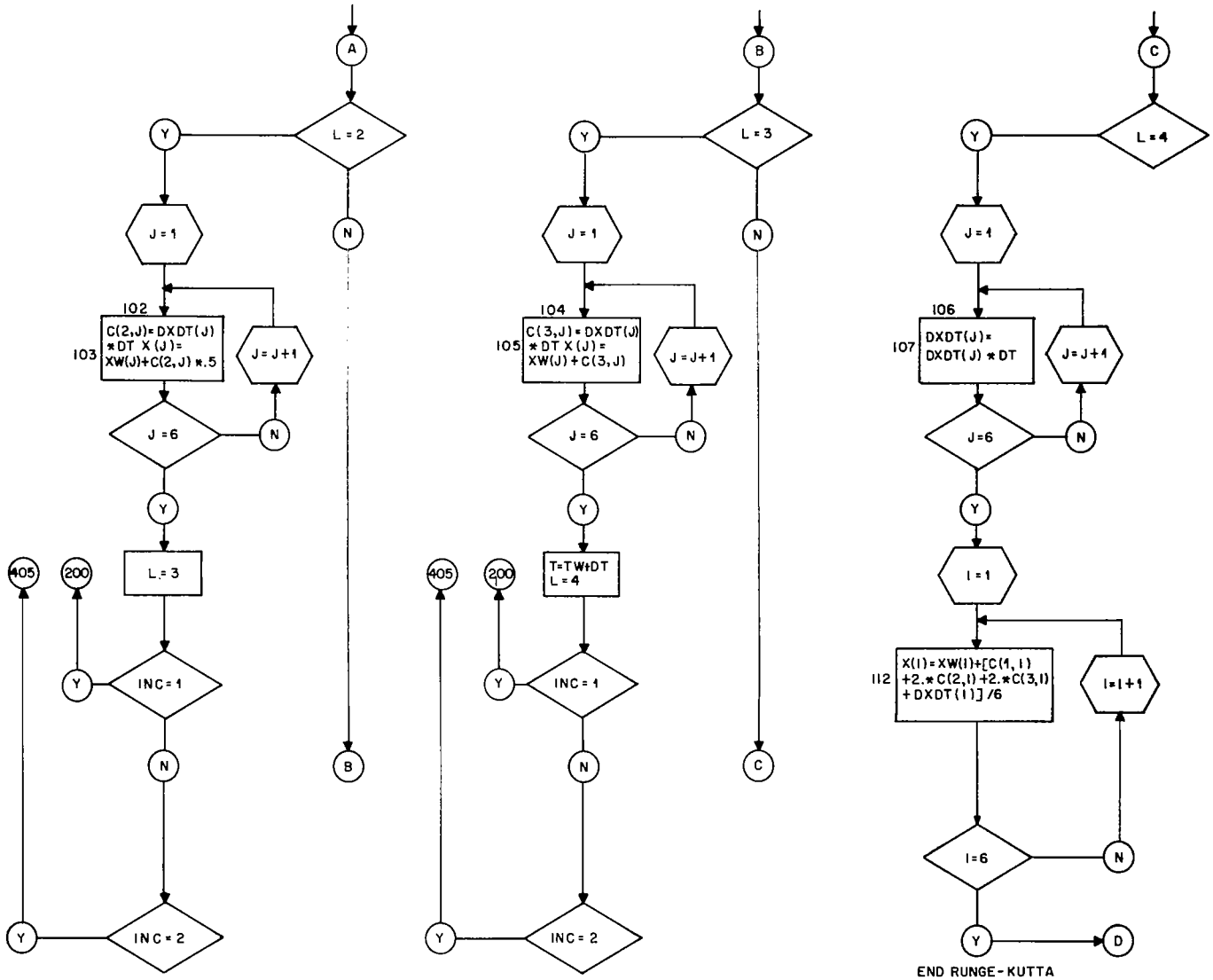
SYSTEM MODEL COMPUTER PROGRAM FLOW CHART
FIGURE C-1 (2 of 6)



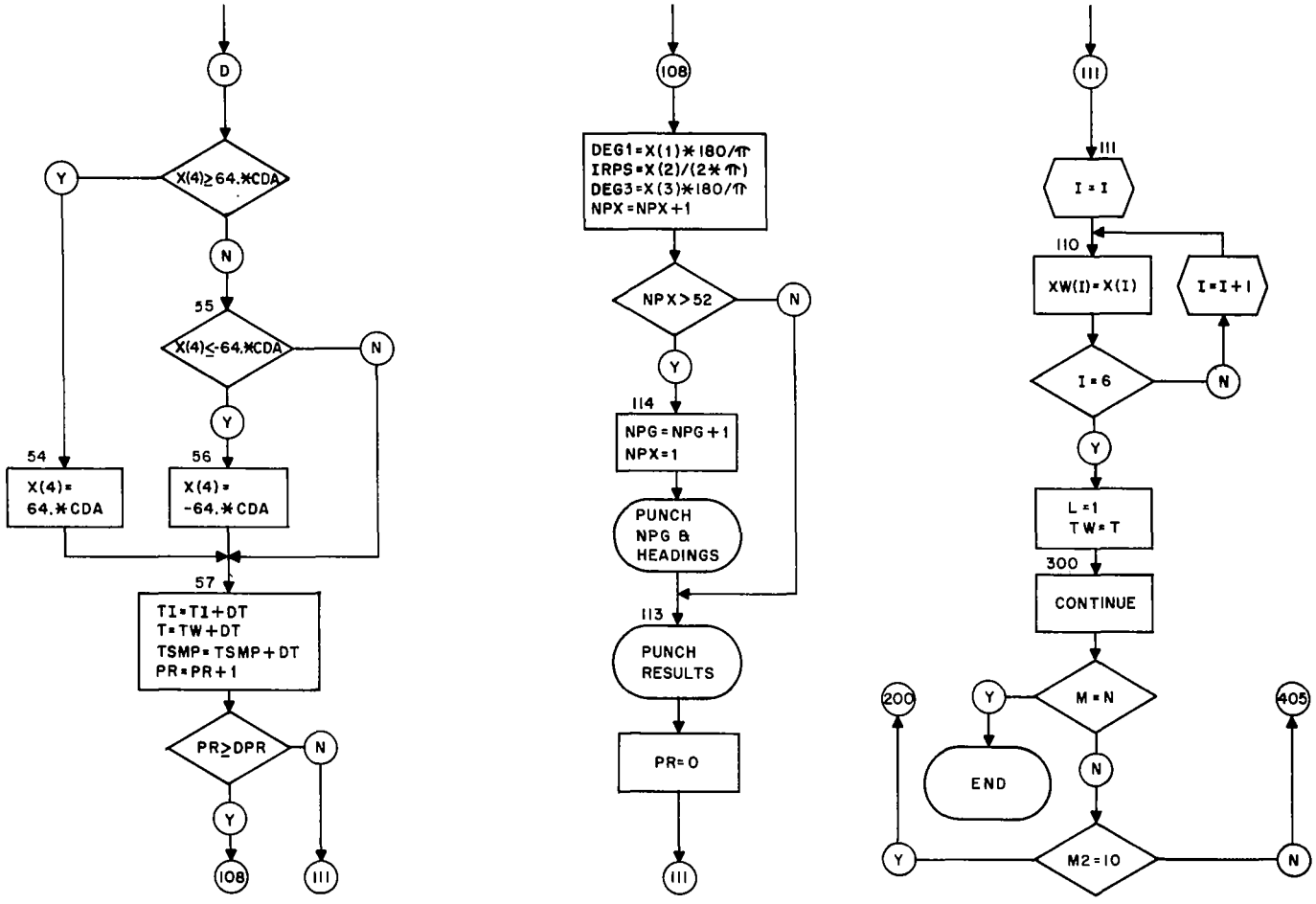
SYSTEM MODEL COMPUTER PROGRAM FLOW CHART
FIGURE C-1 (3 of 6)



SYSTEM MODEL COMPUTER PROGRAM FLOW CHART
FIGURE C-1 (4 of 6)



SYSTEM MODEL COMPUTER PROGRAM FLOW CHART
FIGURE C-1 (5 of 6)



SYSTEM MODEL COMPUTER PROGRAM FLOW CHART
FIGURE C-1 (6 of 6)

```
C       DIGITAL CONTROLLER SYSTEM MODEL * LSI SIMULATOR
        DIMENSION X(6),XW(6),C(3,6),DXDT(6)
      1 FORMAT(4X,4HTIME,4X,7HSC VEL.,2X,10HINTEGRATOR,3X,7HSC POS.,
       14X,7HD/A OUT,4X,6HAMP IN,3X,3HJET,3X3HWHL)
      2 FORMAT(4X,4HSEC.,4X,7HDEG/SEC,5X,4HBITS,8X,3HDEG,8X,3HVDC,8X3HVAC
       110X,3HRPS//)
      3 FORMAT(E10.4)
      4 FORMAT(I5)
      7 FORMAT(40X,30X,6H PAGE ,I2///)
        READ 3,CE,CD,CI,CR,CG,CDA,R1,R2,CAP,CC,SI,WI,X(1),X(2),X(3),X(4),
       1X(5),X(6),T,H,TI,THC,TQE,RATE,TSMP,DVC,DPR
        READ 4,N
        PR=0.
        NPG=1
        NPX=0
        PUNCH 7,NPG
        PUNCH 1
        PUNCH 2
      5 DO 6 I=1,6
      6 XW(I)=X(I)
        MTH1=CE*X(3)
        TH1=MTH1
        K=1
        K2=1
        TJET=WI*CR*48.8/CG
        L=1
        TW=T
        JET=0
        TDMP=0
        DO 300 M=1,N
C       INCREMENT SELECTION STARTS HERE
    200 DXDT(5)=(X(4)/R2-X(5)*(R1+R2)/(R1*R2))/CAP
    402 IF(DVC-DXDT(5)*DXDT(5))403,403,404
    403 DT=H/10.
        L=1
        INC=2
        DO 300 M2=1,10
        GO TO 405
    404 DT=H
        INC=1
C       INCREMENT SELECTION STOPS HERE
    405 IF(TSMP-RATE)391,390,390
    390 MTH1=CE*X(3)
        TH1=MTH1
        TSMP=0.
    391 TH2=TH1-THC
        IF(TH2-64.)366,369,369
    366 IF(TH2+64.)369,369,395
    395 GO TO (396,367),K2
    396 K=1
    367 IF(TI-CI)397,368,368
    368 TI=0.
        X(6)=X(6)+TH2
        XW(6)=X(6)
    397 IF(X(4)-64.*CDA)398,398,399
    398 IF(X(4)+64.*CDA)399,399,380
    399 K=1
        GO TO 386
    369 IF(X(4)-64.*CDA+1.E-04)370,370,371
    370 IF(X(4)+64.*CDA-1.E-04)371,371,372
```

SYSTEM MODEL COMPUTER PROGRAM,
FORTRAN PROGRAM LISTING
FIGURE C-2 (1 of 4)

```
371 K=1
    GO TO 386
372 IF(TH2)374,374,373
373 K=2
    GO TO 386
374 K=3
    GO TO 386
380 IF(X(6)-3072.)382,381,381
381 TDMP=+TJET
    JET=-1
    K=3
    K2=2
    GO TO 386
382 IF(X(6)+3072.)383,383,384
383 TDMP=-TJET
    JET=+1
    K=2
    K2=2
    GO TO 386
384 IF(X(6)*X(6)-100.)385,385,386
385 TDMP=0.
    K=1
    JET=0
    K2=1
386 GO TO(387,388,389),K
387 DXDT(6)=0.
    GO TO 18
388 DXDT(6)=48.8
    GO TO 18
389 DXDT(6)=-48.8
 18 IF(1024.-TH2)19,19,20
 19 TH4=4095.
    GO TO 23
 20 IF(TH2+1024.)21,21,22
 21 TH4=-4095.
    GO TO 23
 22 TH4=CD*TH2
 23 TH5=X(6)+TH4
    IF(4095.-TH5)24,24,25
 24 TH6=4095.
    GO TO 28
 25 IF(4095.+TH5)26,26,27
 26 TH6=-4095.
    GO TO 28
 27 TH6=TH5
 28 PRA=CR*TH6
    PRB=CG*X(2)
    IF(64.*CDA-X(4))29,29,30
 29 X(4)=+64.*CDA
    IF(PRA-PRB)33,33,32
 30 IF(64.*CDA+X(4))31,31,33
 31 X(4)=-64.*CDA
    IF(PRA-PRB)32,33,33
 32 S6=0.
    GO TO 34
 33 S6=+1.
 34 DXDT(4)=S6*CDA*(PRA-PRB)
    DXDT(5)=(X(4)/R2-X(5)*(R1+R2)/(R1*R2))/CAP
    V7=X(4)-X(5)
    V6=CC*V7
```

SYSTEM MODEL COMPUTER PROGRAM,
FORTRAN PROGRAM LISTING
FIGURE C-2 (2 of 4)

```
      IF(V6) 43,43,44
   43 SV=-1.
      GO TO 45
   44 SV=+1.
   45 IF(.085-V6) 35,35,36
   35 TS=102.E+03
      GO TO 39
   36 IF(.085+V6)37,37,38
   37 TS=-102.E+03
      GO TO 39
   38 TS=2.74E+07*SV*V6*V6-15.8E+07*V6*V6*V6
   39 TL=TS-25.32*(X(2)-X(1))
      DXDT(1)=(-TL-TQE-TDMP)/SI
      DXDT(2)=TL/WI
      DXDT(3)=X(1)
C     RUNGE-KUTTA STARTS HERE
      GO TO (100,102,104,106),L
  100 DO 101 J=1,6
      C(1,J)=DXDT(J)*DT
  101 X(J)=XW(J)+C(1,J)*.5
      T=TW+DT*.5
      L=2
      GO TO (200,405),INC
  102 DO 103 J=1,6
      C(2,J)=DXDT(J)*DT
  103 X(J)=XW(J)+C(2,J)*.5
      L=3
      GO TO (200,405),INC
  104 DO 105 J=1,6
      C(3,J)=DXDT(J)*DT
  105 X(J)=XW(J)+C(3,J)
      T=TW+DT
      L=4
      GO TO (200,405),INC
  106 DO 107 J=1,6
  107 DXDT(J)=DXDT(J)*DT
      DO 112 I=1,6
  112 X(I)=XW(I)+(C(1,I)+2.*C(2,I)+2.*C(3,I)+DXDT(I))/6.
C     RUNGE-KUTTA STOPS HERE
      IF(64.*CDA-X(4))54,54,55
   54 X(4)=+64.*CDA
      GO TO 57
   55 IF(64.*CDA+X(4))56,56,57
   56 X(4)=-64.*CDA
   57 TI=TI+DT
      T=TW+DT
      TSMP=TSMP+DT
      PR=PR+1.
      IF(PR-DPR) 111,108,108
  108 DEG1=X(1)*180./3.1416
      IRPS=X(2)/6.2832
      DEG3=X(3)*180./3.1416
      NPX=NPX+1
      IF(NPX-52)113,113,114
  114 NPG=NPG+1
      NPX=1
      PUNCH 7,NPG
      PUNCH 1
      PUNCH 2
  109 FORMAT(1X,F8.3,1X,E10.4,1X,E10.4,1X,E11.5,1X,E9.3,1X,E9.3,2X,I2
```

SYSTEM MODEL COMPUTER PROGRAM,
FORTRAN PROGRAM LISTING
FIGURE C-2 (3 of 4)

```
   13X,I4)
113 PUNCH 109,T,DEG1,X(6),DEG3,X(4),V6,JET,IRPS
    PR=0.
111 DO 110 I=1,6
110 XW(I)=X(I)
    L=1
    TW=T
300 CONTINUE
    END
```

SYSTEM MODEL COMPUTER PROGRAM,
FORTRAN PROGRAM LISTING
FIGURE C-2 (4 of 4)

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