LMSC 8-39-66-2

TECHNICAL SUMMARY REPORT
ON
THE FIRST EXPERIMENTAL FLIGHT PACKAGE
OF
AN ADVANCED TELEMETRY SYSTEM WITH ADAPTIVE CAPABILITY

1 JULY 1963 THROUGH 15 FEBRUARY 1965

CONTRACT NAS 8-5110, TP 2-831815

Prepared for

George C. Marshall Space Flight Center,
Huntsville, Alabama

and submitted by

Lockheed Missiles & Space Company
of
Lockheed Aircraft Corporation,
Sunnyvale, California

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Date: 7 February 1966

FOREWORD

This report describes work performed by Lockheed Missiles & Space Company under Contract NAS 8-5110 entitled "Advanced Telemetry System with Adaptive Capability" for George C. Marshall Space Flight Center, National Aeronautics and Space Administration, Huntsville, Alabama. This report is for the period 1 July 1963 through 15 February 1965, and covers work performed on the first experimental flight package. A previous report, LMSC 657517, covers work performed prior to 1 July 1963.

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LIST OF FIGURES AND TABLES

Section 1
INTRODUCTION AND SUMMARY

During the first twelve months, work on Contract NAS 8-5110 was completed through Phase IV and reported in LMSC 657617[1]. This included a conceptual study, design and construction of a non-flyable prototype system, test and evaluation of the prototype, and the formulation of specifications for the design and development of a flyable system. Discussion of the details of this earlier work will not be repeated here. Also, for a general introduction to this subject refer to LMSC 657617.

During the period covered by this report, additional study and development was accomplished. However, the major task was that of design, construction, and design proof test of an experimental flight package.

The functional design of the flyable system is, in general, based upon the earlier non-flyable prototype. However, to meet the requirements of operating over a wide temperature range and at higher speeds, improvements were required in circuit and logic design. Additional improvements were made to achieve revised performance requirements and to simplify the construction and reprogramming of the system. Where necessary to obtain or prove the solution to specific circuit problems, breadboards were constructed and tested over the temperature range. Details of functional design improvements are discussed further in Section 2. A general description, specifications and interface details, principles of operation, and programming instructions, are covered in the Operation Manual, LMSC 8-39-65-4[2].

The packaging design of the system groups similar components, related to a system function, into a subassembly. For example, all integrated circuits performing logic functions are included within a logic subassembly and conventional components, including magnetics, are included in three (3) additional subassemblies -- reference memory, buffer memory, and power converter.

These four (4) subassemblies are mounted to a baseplate, interconnected and enclosed with a cover. This arrangement of subassemblies results in advantages in design, fabrication and test. Details of the packaging design are given in Section 3.

The system was constructed and debugged at room temperature to correct functional design and fabrication errors and faulty components. This was followed by tests at high and low temperature to locate and correct additional problems with system operation. These temperature tests were followed by other environmental tests.

The system was subjected to vibration tests with monitoring transducers attached to internal structural members and system operation was monitored. After rework and retest to lower amplification factors of structural members, the system was subjected to shock and monitored as during vibration tests. The environmental tests were concluded by a combination high temperature-altitude test to verify adequate heat transfer by thermal conduction to the baseplate and to test for possible damage to the system enclosure because of internal pressure.

Conclusions from test results are that the system, with design corrections as incorporated in the unit under test, will perform correctly within environments specified in MSFC test method 50M60005 with two exceptions. These two exceptions are: 1) correct performance of the system was proven at temperatures up to +70°C (goal was +85°C), and 2) the maximum "false" logic level at system inputs degraded from 1.3 volts at room temperature to 0.85 volts at +85°C (goal was 1.0 volt maximum at +85°C). (See Appendix B for detailed specifications of performance requirements.)

Section 2
FUNCTIONAL DESIGN IMPROVEMENTS

2.1 General

Following the evaluation of the feasibility breadboard system, improvements were made in the system and circuit design to achieve desired performance of the experimental flight package. Each area where significant revisions and improvements were made will be discussed. Where basically similar problems were solved, the discussion of two or more areas will be grouped together to minimize repetition.

The following list is a summary of changes and improvements made:

a) To meet requirements for operation at higher rates, over a wide temperature range, and to get around peculiarities of the integrated logic circuits employed, all counters and shift registers were changed.

b) The programmable control logic was expanded.

c) A new method of controlling the acceptance of redundant samples from near static data channels were devised and implemented.

d) NDRO storage capability was added to the reference memory. By use of this NDRO storage capability, the organization of the reference memory was changed to simplify programming for specific multiplexer configurations.

e) The buffer memory was redesigned to provide a larger storage capacity.

f) Synchronization and command logic was changed to incorporate improvements and to meet new requirements.

g) The transmission of a code word to indicate the occupancy of the buffer memory was substituted for the previous delay measurement code.

h) To identify each multiplexer main frame, a code word is transmitted to identify each main frame, (this replaces the previous combination of master frame identification code word and the "new frame" bit).

2.2 Counters

Each counter circuit in the system was changed or deleted and some new ones added. The primary reasons for these changes were to achieve new performance requirements and/or to get around problems due to peculiarities of Texas Instruments, Inc., series 51 integrated circuits (see Appendix A for information relative to these peculiarities).

2.2.1 Event Programmer

This counter and associated circuits provide timing outputs to initiate logical operations which are repeated for each data sample. It is required to provide a division of 20 and to count at the highest system clock rate of 288 KC. Also, it must be synchronized with the multiplexer. It was found that this could not be achieved by the earlier circuit configuration because of the problem of presetting with the circuit modules used (see Appendix A, paragraph 1(a)).

A circuit arrangement was devised to achieve a division of five without the use of the preset input of the flip-flops. By preceding the ÷5 with a ÷4, a ÷20 was achieved capable of counting at a rate in excess of 500 KC, as loaded, over the temperature range of -35 to +85°C. To maintain equal loading on all flip-flops of the counter and to provide for fan-out, inverter circuits using conventional components were used. Synchronization with the multiplexer is achieved

by application of a preset pulse, to all stages of the counter, for a duration of four system clock periods and at a time when the outputs of the counter are not used.

The states of the ÷20 counter are detected by NAND gates as necessary to derive the necessary timing outputs. However, during transitions of the counter states, troublesome noise spikes appear at the output of the NAND gates. Direct use of the outputs of the NAND gates was not feasible. This problem was solved by use of an interface flip-flop, for each timing output, which is controlled by the NAND gate output and the system clock. The outputs of these interface flip-flops were then used. This achieved the desired "filtering". Also, well-defined timing outputs are produced. The details of the event programmer are shown in Fig. 2-1.

2.2.2 Channel Address Counters

These counters provide the complete address of the data sample which is being processed by the data compressor. Changes to these counters were:

a) The ÷2 was changed to provide for programming it for ÷2 or ÷4.

b) The ÷3, ÷10, and ÷30 were each changed to provide for a preset duration of at least 17 system clock pulse periods. (The preset inputs to the flip-flops are used in obtaining the desired countdown of each counter.) Also, associated with the preset inputs of the flip-flops, an improvement was made for synchronization with the multiplexer.

2.2.3 "K" Counter

The "K" counter is employed in the implementation of limits for each data sample. It is required to count at the system clock rate and to repeat a counting sequence for each data sample. The change in this counter was in the preset duration. The preset duration is now equal to six system clock periods.

2.2.4 Output Rate Countdown

This is actually two counters which provide a countdown from the system clock to establish the output bit rate from the system. The m counter is used to establish the interlace of buffer read operations such that reading is allowed to occur at odd system clock times (m=2) or at alternate odd system clock times (m=4). A choice of m=2 or m=4 is made when programming the system. This counter was added because the event programmer, as modified, is stopped during synchronization with the multiplexer. (On the breadboard the function of this m counter was performed by the event programmer.) The first stage of the m counter is synchronized with the first stage of the event programmer when the event programmer is counting.

The n counter was made programmable for ÷2 through ÷17. A choice of countdown is established by connection of selected flip-flop preset inputs to receive a preset pulse. The preset pulse generation circuit for this counter was revised to provide a duration of either 3 (for m=2) or 6 (for m=4) system clock pulses. As a further precaution, to avoid preset problems, the clock input to the first stage of the n counter is inhibited during the preset pulse. A diode and resistor network was added to correct a problem of reverse propagation in the n counter.

2.2.5 Bits Per Word Counter

This counter counts the number of output register shift operations and provides a signal to indicate when new data should be loaded into the output register. This counter was modified to permit programming for a countdown of either 16 or 17, corresponding to the desired output word length.

2.2.6 Master Frame Counter

This counter was added to provide a count of multiplexer master frames. A total count of 16 is provided. For each sequence of 16 master frames, an output initiates the insertion of a buffer occupancy code word into the buffer memory.

2.2.7 Buffer Memory Address Counters

These two counters were added to continuously monitor the occupancy of the buffer memory. The "read" counter indicates the current address of the memory "read" sequencing circuitry. Similarly, the "write" counter indicates the address location of the "write" sequencing circuitry. Each of these counters is a 10 stage simple ripple-through counter. Primary use of the outputs from these counters is for inputs to a parallel subtractor. An output from the 2^5 stage of the "read" counter is also used to initiate the insertion of the PCM word sync code into the system output.

2.3 Registers

The use and design of registers in the flyable system remained essentially the same as for the non-flyable feasibility breadboard. Minor changes were made to correct preset and shift problems as discussed in Appendix A. The output register was arranged to permit programming for an output word length of 16 or 17 bits, as required.

2.4 Programmable Control Logic

The control logic was rearranged to accommodate additional inputs and to permit programming of the inputs in combinations to achieve the desired acceptance criteria. The additional inputs accommodated included channel sample rates, time-slot groups (or multiplexer groups), and a special inhibit signal.

2.5 Redundant Sample Control

A new method was devised for acceptance of redundant data samples which uses the difference between available transmitter bandwidth and the bandwidth required for "significant" data samples in a manner such that the maximum time between two consecutive data samples, from a near-static data channel, is minimized. The method devised establishes a recycle period during which at least one data sample is transmitted from all data channels. For active data channels, acceptance of a data sample by "normal" acceptance criteria may eliminate the need to transmit a redundant sample from those channels.

A recycle period is defined as the period required to verify that at least one data sample has been accepted from all data channels since the end of the previous recycle period. The beginning of a recycle period always coincides with the beginning of a multiplexer master frame. The recycle period will contain a variable number of multiplexer master frame periods.

The state of a tag bit in each word in the reference memory indicates if the word has been accepted within the present recycle period. A "1" in the tag bit signifies that the channel has not been accepted since the last recycle period. A "0" in the tag bit signifies that the channel has been accepted, since the last recycle period, either by the normal acceptance criteria or the redundant sample control. The tag bits are scanned and when all tag bits are "0", a new recycle period is started.

Figure 2-2 is a flow diagram of the redundant sample control method. When the reference memory is read, if the tag bit is a "1" the sense amp flip-flop (SAFF) is set to the "1" state. If it is the first time that the channel has been sampled since the start of the recycle period, the SAFF is set to the "1" state. If the SAFF is a "0" the normal acceptance criteria apply. (Normal acceptance criteria, as used here, includes all criteria employed to cause acceptance or rejection of a data sample other than the redundant sample control method under discussion.) If the SAFF is a "1" and the buffer occupancy is not within the required occupancy range for redundant data acceptance, normal acceptance criteria are applied. If the SAFF is a "1" and the buffer is within the required occupancy range for redundant data acceptance, the data sample is accepted and a "0" is written into the tag bit. If the data sample is accepted by normal criteria a "0" is written in the tag bit. If the data sample is not accepted, the state of the SAFF is written in the tag bit. If the data sample is not accepted and the state of the SAFF is a "1", the tag bit flip flop (TBFF) is set to the "0" state. The SAFF is now set to "0" and if it is not the end of a master frame, the next word is read. If it is the end of the master frame, a check is made to determine whether or not the TBFF is a "1". If the TBFF is a "1", a new recycle period is started. If the TBFF is a "0", the TBFF is set to the "1" state and the next word is read.

2.6 Reference Memory

The reference memory was improved in several ways. A capability for non-destructive readout (NDRO) of data, in combination with destructive readout (DRO), was added. Using one bit of NDRO storage for addressing purposes, a revised addressing scheme was implemented which simplified the reprogramming necessary to accommodate a change to multiplexer format. Other NDRO bits were used to improve the long-term reliability for stored limit and priority data. Circuits were added, redesigned or improved to accomplish the desired functions, including operation over the temperature range.

2.7 Buffer Memory

To achieve the best design for a significantly larger storage capacity, the buffer memory was completely redesigned. Use of linear-select addressing was abandoned in favor of coincident-current addressing to reduce addressing circuitry. New addressing circuitry was developed. Also, the required bipolar sense amplifiers were developed.

To provide buffer occupancy information, "read" and "write" address counters (also see paragraph 2.2.7), a 10 bit parallel subtractor, and programmable decoding logic, were added. (The previous method used to derive buffer occupancy information could not be used with the larger capacity and revised organization.) The outputs of the occupancy decoding logic are for use as inputs to the control logic.

2.8 Synchronization Logic

The circuitry for synchronization of the internal data compressor operations, with the multiplexer, was revised and improved in several ways. Revised internal sync requirements and the requirement for operation at the 14,400 sample per second commutation rate, (288 KC system clock rate), made it necessary to revise the synchronization logic. Changes and improvements to the synchronization logic were:

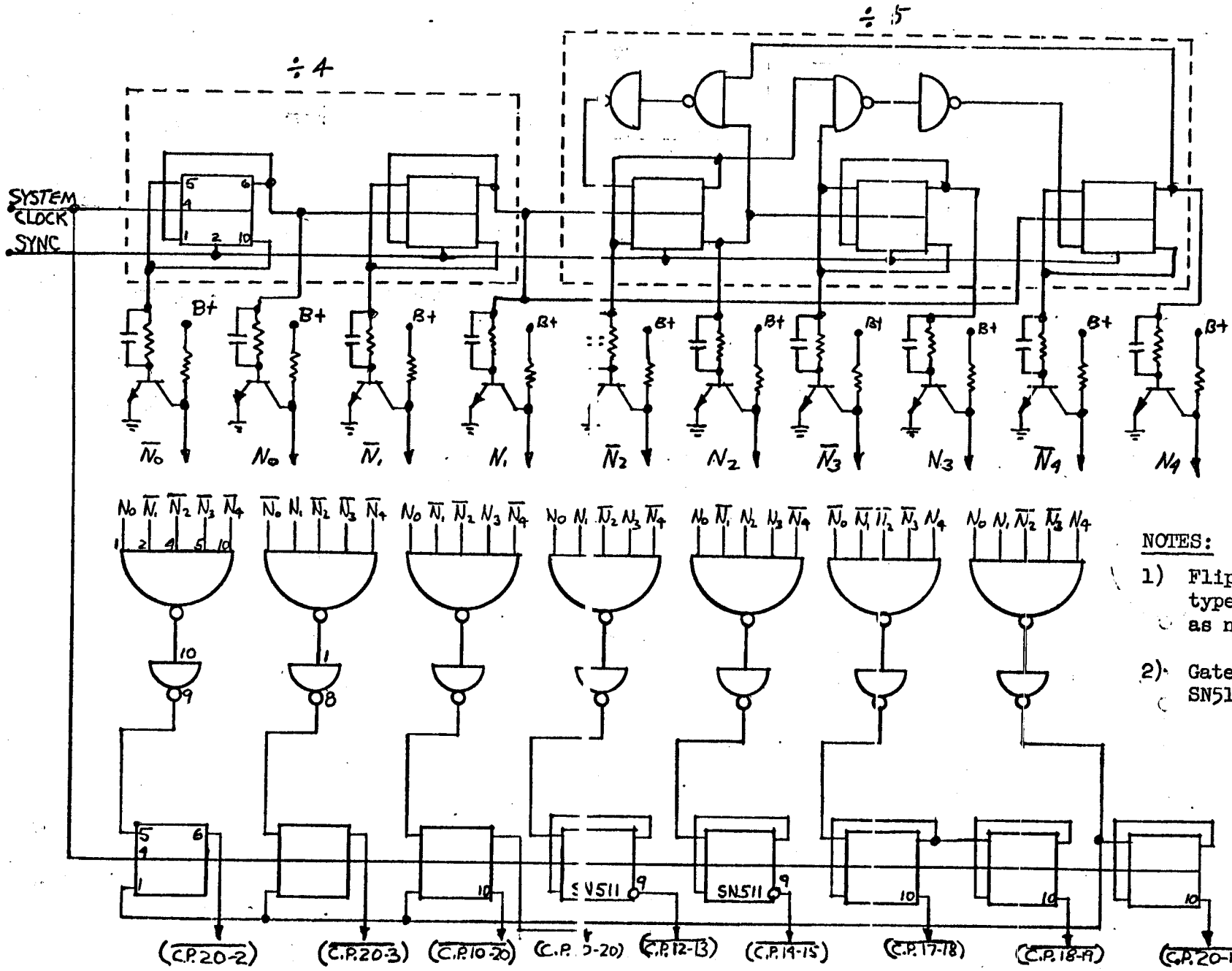
a) An interface circuit was added to provide a well defined threshold for the input amplitude required to activate the sync logic, to filter out high frequency noise, and to make the operation insensitive to input rate-of-rise.

b) Provision was made for programming the sync logic to accommodate either 144 KC or 288 KC system clock rates such that correct timing at the sync logic outputs can be obtained.

c) Two separate outputs were derived to correctly synchronize the event programmer and the channel address counters.

2.9 Command Logic

The command logic was revised to accommodate one additional address bit input, required for the commutation format related to the 14,400 sample per second commutation rate, and to provide an additional output to operate the NDRO "clear" drivers in the reference memory. Also, the number of bits input, required to signal that a valid command is ready, was reduced from two to one to maintain the total number of bits input, required for a command, at twenty (20).



NOTES:

1) Flip-flops are type SN510 except as noted.

2) Gates are SN512 or SN514, as required.

FIGURE 2-1 SCHEMATIC OF 20-COUNT EVENT PROGRAMMER

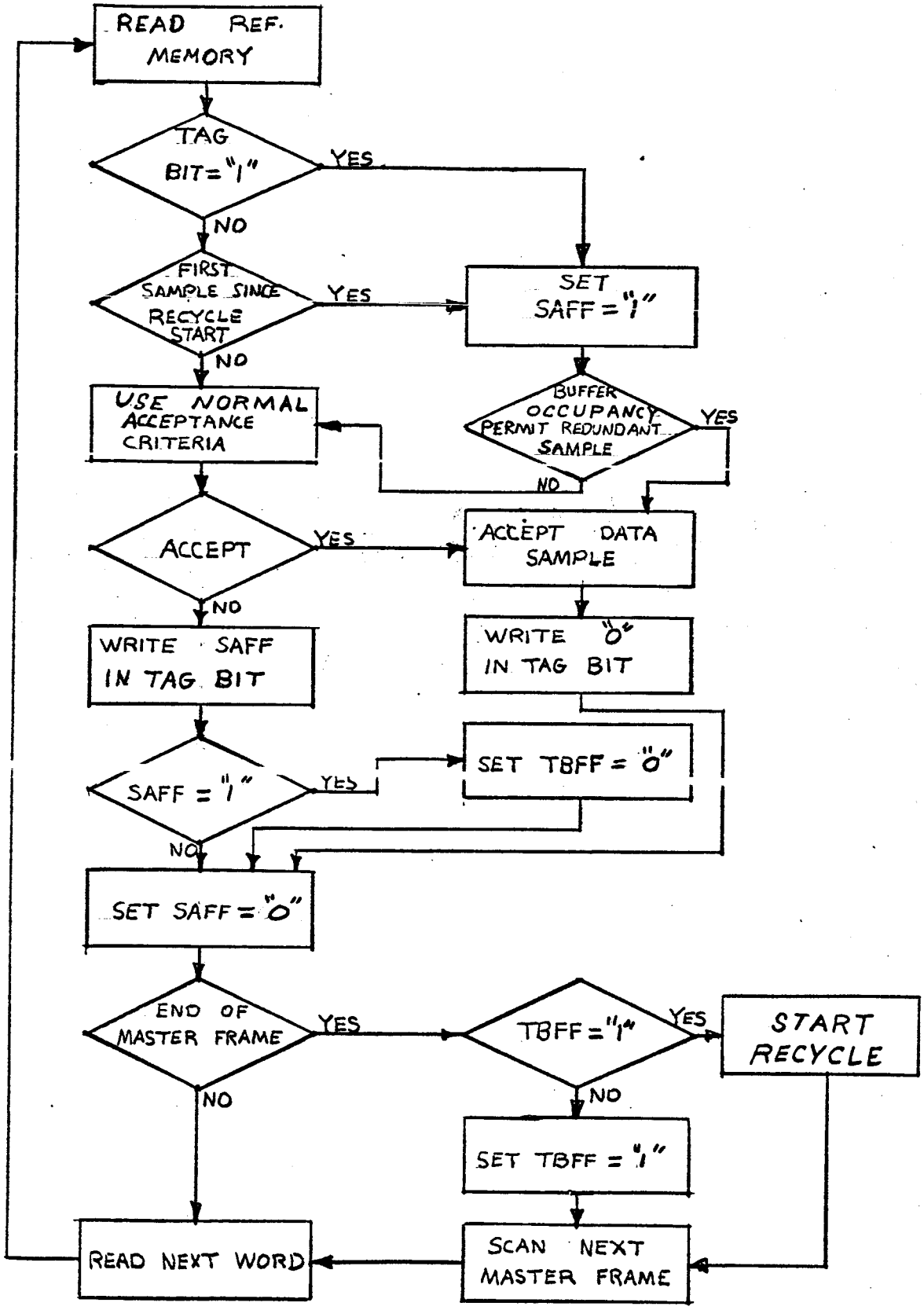


FIGURE 2-2 FLOW DIAGRAM, REDUNDANT SAMPLE CONTROL METHOD

Section 3
PACKAGING AND MECHANICAL DESIGN

3.1 Top Assembly

The Data Compressor unit consists of a base plate with attached subassemblies and wiring harness, and a removable sheet metal cover. The base plate and cover are made of 6061 aluminum alloy for high strength, light weight, and ease of fabrication. The base plate is 17.13 inches long by 15.13 inches wide, with thickness varying from .25 to .90 inches. The cover is made from a deep drawn aluminum box and has a flanged collar attached to the open side. A 4.6 inch diameter hole in one side wall of the cover permits access to the input-output connectors which are assembled to the internal structure. The total weight of the equipment with cover installed is approximately 48 pounds. Machined bosses are provided at the corners of the base plate to provide attachment points for mounting the equipment in a space vehicle. Four bolt holes of 3/8 inch diameter are provided in the mounting bosses. The cover may be removed without disturbing the base plate bolts, thus permitting test and repair while the equipment is mounted.

The input-output receptacles are Bendix Pygmy types. (PT07 series). The connectors are attached to a flanged receptacle plate with jam nuts and O ring gaskets. The receptacle plate is supported by brackets attached to the equipment structure and base plate. Rubber grommet connections permit the receptacle plate to float slightly relative to the brackets. The receptacle plate is supported with sufficient rigidity to permit exterior cables to be plugged into it when the cover is removed. The float action permits the plate to be drawn tightly against the inside of the cover by screws, after the cover is installed. An O ring gasket seals the receptacle plate to the cover.

A combination E.M.I. and pressure sealing gasket is recessed into a groove which extends around the periphery of the base plate. This gasket seals the base plate to the cover flange. The unit is purged by flowing dry nitrogen at 5 psi gage pressure into the filler valve on the side of the cover. The pressure of

the gas causes a relief valve, mounted on the top of the cover, to open. The open relief valve permits a continuous flow of dry gas through the equipment, thereby forcing out humid air. When the nitrogen source is disconnected, the relief valve closes and dry nitrogen at a slight positive pressure is retained inside the equipment. The presence of the dry gas resists the inflow of contaminated air, and prevents moisture from condensing inside, when the equipment is subjected to low ambient temperature. The Top Assembly is shown in Fig. 3-1.

3.2 Installation of Subassemblies

The reference memory, buffer memory, power supply and logic sections are each fabricated as separate, independent subassemblies. The lower surface of each subassembly is bolted to the base plate. The upper ends of the reference and buffer memories and logic section are bolted to a common structural member; the stabilizer frame. Each subassembly is provided with input and output connectors. An interconnecting wire harness plugs into all subassemblies.

3.3 Logic Subassembly

The logic circuits are packaged in the UES format, which is a standard modular system developed by LMSC. The circuit components are attached to double sided etched circuit boards 5.12 inches long by 1.73 inches wide and 1/32 inch thick.

A 66 pin male connector is attached to one edge of each circuit board. Two board subassemblies are fastened with screws to a "U" shaped metal frame; a polyurethane foam pad is compressed between the boards. Twenty-four such frame assemblies are plugged into an array of female contacts swaged to a perforated metal plate (matrix). A wire-wrap shank is attached to each female contact and extends to the rear of the plate. Interconnection of the frame assemblies is accomplished by wiring between pins on the rear of the plate. The wires are connected by the Gardner-Denver Wire Wrap technique.

The interconnect area is enclosed by a sheet metal cover. Silicone rubber foam is expanded in place between the cover and the matrix and fills all the voids between the wires and pins. The foam supports the wires and provides

resistance to vibration damage. If changes to the interconnect pattern are required, the soft foam can be easily removed to expose the wrapped connections. Rails, extending from the matrix plate, contact bosses on each of the frame assemblies. The frame assemblies are securely attached to the rails by captive screws at the ends of each frame.

The matrix, with its frame assemblies, is supported by two post structures which extend vertically from the equipment base plate. All the frame assemblies are accessible from the side of the equipment when the equipment cover is removed.

3.4 Reference Memory

The reference memory employs six identical magnetic modules packaged in a flat form factor. These modules are 8.48 inches long by 7.13 inches wide by .31 inches thick, and consist of two printed circuit boards supported by plastic frames. The center section of each module contains the magnetic memory cores and their associated matrix of drive and sense wires. The right and left sections of each module contain diodes and switch core assemblies. The memory Read/Write Drivers, sense amplifier, and bit driver circuits are packaged in a flat form factor in modules of the same dimensions as the magnetics. All modules are stacked with the flat sides parallel, and are separated by hollow spacers. The stack is fastened together by threaded rods, which pass through the modules and spacers. The modules are interconnected by jumper wires soldered to terminations along the edges of the module circuit boards. The Read/Write driver circuits are in the lower two modules of the stack, and are thermally coupled to the equipment base plate. Heat dissipated in the transistors of these modules is conducted through metal clips into aluminum heat sink rails. The rails form the side walls of these modules and are in contact with the base plate.

3.5 Buffer Memory

The buffer memory system is a stack of flat modules each of which is approximately 4.5 inches square. The memory core stack consists of five circuit boards containing cores, one printed circuit interconnect board, and a wiring support

board. The memory core stack is 1.0 inches high. The various driver and sense amplifier modules are each approximately .38 inches high. The buffer modules are separated by spacers and are fastened together with four threaded rods. Interconnections are made by jumper wires at the edges of the circuit boards.

The Read/Write driver module is in contact with the base plate to provide a low resistance heat transfer path. The transistors of this module are installed in clips similar to those in the reference memory.

3.6 Power Supply

The power supply contains four flat modules similar in construction to those used in the memories, but of smaller size. These modules are stacked, and clamped to a small aluminum chassis by four screws. The electronic components which dissipate a significant amount of heat are mounted on the chassis. A flanged sheet metal cover is bolted to the chassis, and serves as a combined E.M.I. shield and support for the input-output connector. The chassis area is 4.24 inches by 2.74 inches. Each module is 3.53 inches long by 2.05 inches wide by approximately 0.4 inches thick.

3.7 Structural and Environmental

The structure of a flight package must be designed to resist the stresses imposed by vibration and shock environments. The vibration response of a structure is determined by the stiffness-to-weight ratio of its members, and the amount of damping present. The natural (resonant) frequency becomes higher as the stiffness of a structural member is increased and its weight is decreased. Ideally, the natural frequency should be higher than the highest excitation frequency of the environment to avoid resonance conditions. This situation is difficult, if not impossible, to achieve in a complex electronic package such as the Data Compressor. However, raising the natural frequency as high as possible by stiffening all structural parts tends to decrease the stress level in these parts. In the Data Compressor, extensive use is made of the stiffening effect of ribs and flanges on the base plate, logic posts, and stabilizer frame.

The etched circuit boards are stiffened by the addition of ribs and frames.

The vibration amplification factor of a structure is determined by the damping present within the structural parts, and at the interface between parts. The internal hysteresis damping effect is small for most materials used for structural parts and etched circuit boards. Additional damping is provided in the Data Compressor by inserting polyurethane foam compression pads between the circuit boards of all modules, and by extensive use of riveted and bolted joints. Slight relative motion at the interface of such joints provides damping through the mechanism of sliding friction.

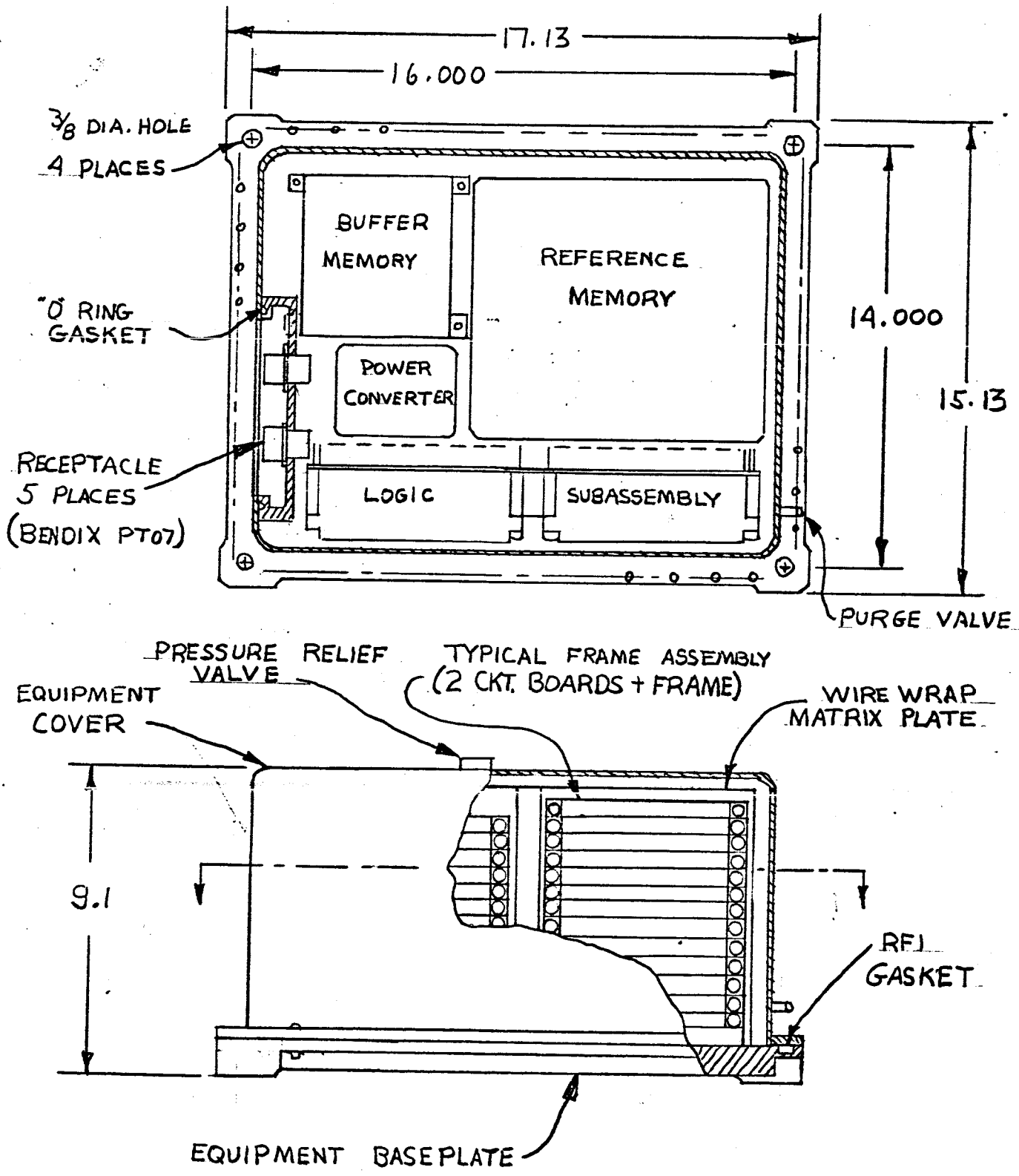


FIGURE 3-1 VIEWS SHOWING ARRANGEMENT OF MAJOR SUBASSEMBLIES AND OTHER DESIGN FEATURES.

Section 4
FUNCTIONAL TESTING

4.1 General

In this section, the tests conducted to debug the system of design and fabrication problems will be discussed. The purpose of this discussion is to state what and how tests were conducted and to state the results obtained. In most instances, the details of problems encountered and corrections made are not stated. This discussion will be limited to those tests conducted prior to beginning environmental tests of the entire system. Also, for parameters which are temperature dependent (power input and limits for input logic levels), discussion and results will be included in Section 5.

4.2 Test of Subassemblies

As the fabrication of each minor and major subassembly was completed, tests were made where possible, to determine the functional status of the subassembly.

4.2.1 Test of Logic Subassemblies

Each logic circuit board, after assembly of logic modules and other components, was tested. Inputs were applied to exercise each circuit on the board and observations made to verify that operation was as intended. Corrections were made where necessary by changing the circuit on the board (the replacement of an entire board was not warranted). Where it was necessary to change the etched circuit pattern, traces were cut and new conductors added with formvar insulated copper wire (magnet wire). After test at the board level, all logic boards were assembled onto the interconnect matrix assembly. Further tests were made of the entire logic subassembly. Correct operation of all counters, except for the buffer "read" and "write" counters, was verified. Also, correct operation reference memory addressing circuits was verified. However, because it was impractical to generate all inputs to fully simulate the memory subassemblies, additional tests were limited.

4.2.2 Test of Memory Subassemblies

Each circuit board of both memory subassemblies was tested after fabrication. Regulated current driver circuits were checked for correct output amplitude and pulse shape. Adjustment of the value of emitter resistors was made where necessary to obtain the correct amplitude. Sense amplifiers were tested for threshold levels and the strobe current-setting resistors were adjusted to obtain the desired threshold level. Address sequencing core-diode circuits were checked for correct sequencing and for correct steering of input current to the outputs. Memory core arrays were tested for correct wiring and correct performance of each memory core. After board level tests, the major memory subassemblies were completed and tested. At this stage a problem of seven (7) broken memory cores in the reference memory was detected which was not corrected. (Apparently these cores were broken accidentally after the previous test and prior to completion of final assembly work on the reference memory magnetics modules.) The immediate replacement of these broken cores was not considered justified because they would not prevent the completion of the remaining tests of the system to prove the flight worthiness of the design.

4.2.3 Test of Power Converter Subassembly

Tests of the power converter was started after the assembly of all components and wiring of the complete subassembly. After adjustment for correct output voltages, noise on input and outputs was measured. Also, regulation against input voltage and load changes was checked. Results were:

OUTPUT	TOTAL CHANGE FOR WORST COMBINATION OF INPUT AND LOAD CHANGE		NOISE IN VOLTS PEAK-TO-PEAK (MAX AT 100% LOAD)
	VOLTS	%	
+ 6 volt	0.26	4.3	0.19
+30 volt	0.40	1.3	0.14
+60 volt	0.92	1.5	0.12

NOTE: Input voltage change was from 23.8 to 32.2 volts and load change was 30% to 120% of nominal.

INPUT NOISE: Approximately 25 milliamperes peak-to-peak

4.3 Test of System

4.3.1 General

To test the system, it was programmed such that the operation of functional features of the complete system could be observed. The programming of each functional area of the system was selected to exercise as many functional parts as possible. For example, the reference memory was programmed for an assumed multiplexer format which required the use of a maximum number of words in the reference memory. Also, combinations of input signals were applied to establish system operation which permitted the operation of each functional area to be verified.

4.3.2 Test Set-up For Functional Tests

The test set-up for functi nally testing the system consisted of input signal generating equipment, as shown in Fig. 4-1, and output monitoring equipment as shown in Fig. 4-2.

Simulated data was provided to the system in the form of a triangular waveform of variable rate from a laboratory function generator and as a variable DC level. Each of these sources was connected to an input on the A-D converter and timing unit. The 144 KC/second system clock and master frame sync pulse "B" from the timing unit were used to clock and synchronize the system during the tests. Commands, to change NDRO stored information and to force a data sample, were provided from the command and test point box. This box provides switched channel addressing capability and command generating circuits along with test jacks connected to the system test points. The command output consists of 20 bits in parallel; 13 address bits, 3 limit bits, 1 priority bit, 1 command ready bit, and 2 function select bits. Adjustable logic levels are provided for the outputs to determine the maximum "0" and minimum "1" conditions for the system. For detailed evaluation of the data acceptance conditions and memory operations the 10 bits of simulated data were provided from 10 toggle switches on the signal simulator panel connected directly to the data inputs of the system. This provided control of each individual data bit.

The compressed PCM data output from the system was connected to the output monitoring equipment. This equipment can monitor and display any 2 data channels, 1 data channel and 1 code word, or 2 code words. The addresses of the data channels and/or code words desired are selected by means of toggle switches. The digital data is displayed by lights located on the panel and is also converted to an analog signal for display on an oscilloscope or analog recorder. Figure 4-2 is a simplified block diagram of the output monitoring equipment showing the input register, two programmable address decoders, two holding registers and D-A converters, in addition to the synchronizing circuitry.

Basically, the synchronizing circuits consist of a main frame sync code decoder used to advance the divide-by-3 and divide-by-10 counters and a master frame sync decoder to reset the counters when the presence of the first main frame of each master frame is detected.

4.3.3 Test of Complete System, Less Buffer Memory

Prior to tests of the complete system, tests were conducted with all subassemblies, except the buffer memory, interconnected. The buffer memory was not installed in order that the back side of the logic interconnect matrix be accessible for test monitoring.

By observation of the time relationship between the master frame sync signal on J2 pin D and the channel address agreement signal on J5 pin N, for specific settings of the command address switches on the command and test point box, correct synchronization of the event programmer and the channel address counter was verified. Also, correct sequencing of the channel address counter was verified.

Correct execution of commanded operations was verified. Next, the loading of the NDRO stored address bit information into the reference memory was accomplished via the command input. The procedure given in paragraph 4.8.3 of the Operation Manual, LMSC 8-39-65-4, was followed. While loading the address bit

information, zeros were loaded for the NDRO stored limits and priority information.

The transfer of new data into the input "A" register and correct shifting of the data in the register was verified by application of fixed combinations of new data bits to the system input connector. Also, correct storage and readout of the reference data sample from the reference memory -- including shifting of the "B" register was verified. Next, limit information was loaded into the reference memory and correct limit decisions by the comparator was verified.

4.3.4 Test of Complete System

After assembly and interconnection of the complete system, tests were conducted to verify the overall operation of the system.

By programming the address decoders (see Fig. 4-2), the last 10 bits of the output codes (see Table 2-7 of LMSC 8-39-65-4) were displayed with lights and verified to be correct. With this method of display, only part B of the word sync code may be observed. Therefore, part A of the word sync code word was verified by observing the serial bit stream with an oscilloscope. Since, for all except the word sync code, this test involved temporary storage of information in the buffer memory, a partial check on the memory operation was achieved.

By programming the address decoders, the 10 bit sample magnitude of a data channel was displayed. Prediction tolerance limits of ± 0.1% were commanded for the channel observed. Fixed combinations of data sample magnitude bits were applied at the system input and the displayed output was verified to be identical to the input. Input combinations of all "1"s, all "0"s, all possible combinations of 9 "1"s, and all possible combinations of 9 "0"s were used. This procedure complemented the output codes verification test such that complete verification of the buffer memory input, storage, and output functions were made.

Correct synchronization of the buffer memory "read" and "write" counters with the corresponding core-diode address circuits was verified.

Dynamic operation of the system was observed with a clipped triangular signal applied as shown in Fig. 4-1. By assignment of prediction tolerance limits and adjustment of the signal generator frequency, the occupancy of the buffer was caused to vary over its entire range. With this input condition, several functions of the system were verified by analysis of the analog outputs of the monitoring equipment (see Fig. 4-2).

By display of the analog signals corresponding to a selected data channel and the buffer occupancy, correct prediction tolerance limits and the adjustment of tolerance limits, as a function of buffer occupancy, was verified (see Fig. 4-3 of LMSC 8-39-65-4). In addition to the comparator, reference memory, and programmable control logic, the correct operation of all buffer memory circuits was necessary for this test -- including the "read" and "write" address counters, the parallel subtractor, and occupancy decoding logic.

With the system operating, as discussed above for dynamic tests, the operation of the redundant sample control logic was observed. The operation appeared to be correct. (It was discovered later, during retrofit work, that an incorrect location of a wire connection on the logic subassembly prevented the operation from being completely correct. The wiring was later corrected as a part of system retrofit rework and correct operation was then verified.)

Observations were made of input logic level limits, compressed PCM out signal rise time and amplitude, and system input power. All of these parameters were within specified limits.

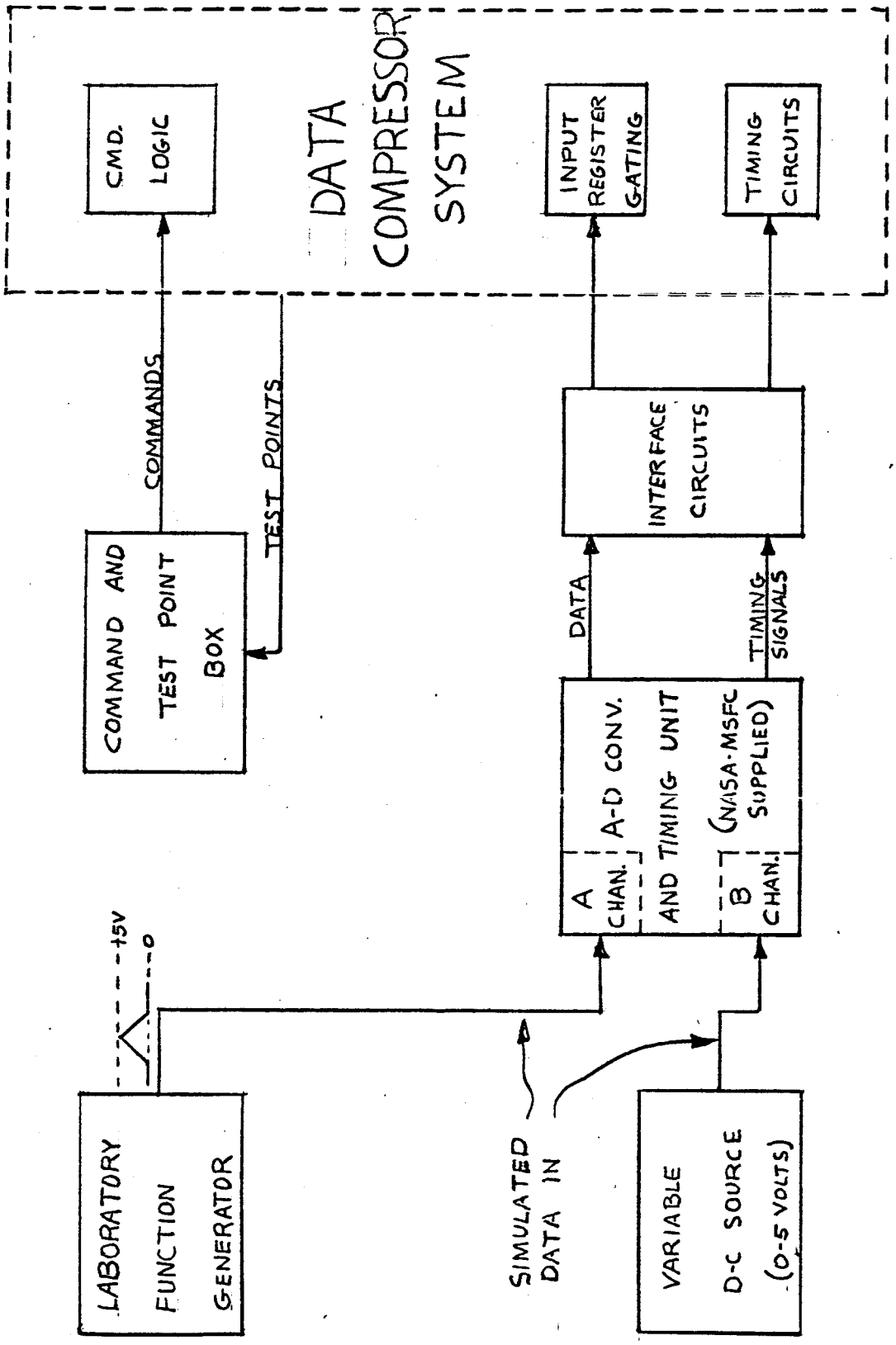


FIGURE 4-1 SYSTEM TEST SET-UP — INPUTS AND MONITORING TEST POINTS.

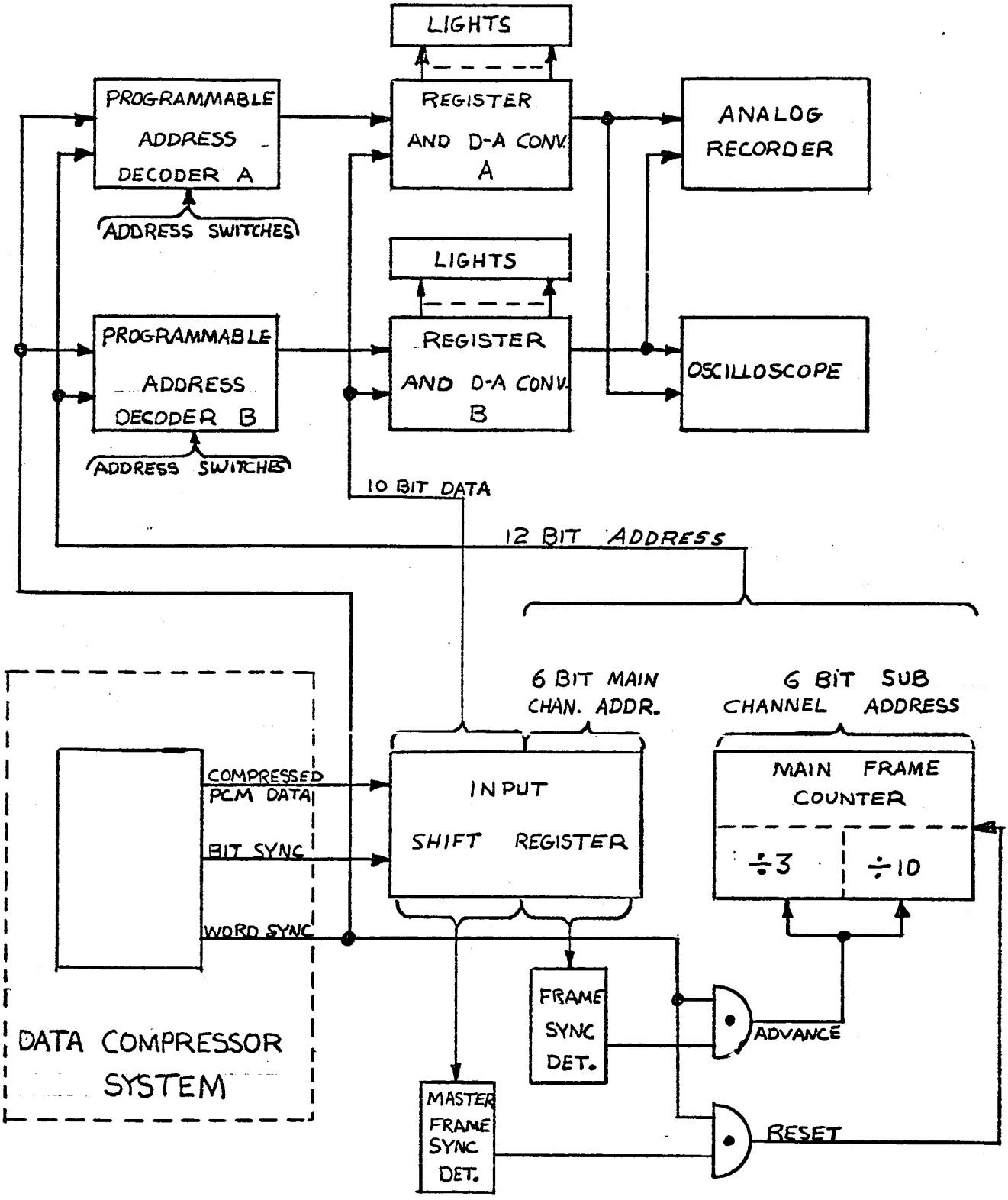


FIGURE 4-2 SYSTEM TEST SET-UP, OUTPUT MONITORING

Section 5
ENVIRONMENTAL TESTING OF FIRST EXPERIMENTAL FLIGHT PACKAGE

5.1 General

Tests were conducted to verify the suitability of the design for application in space vehicle environments. The guide used in conducting these tests was test standard 50M60005 issued by NASA-George C. Marshall Space Flight Center. Detailed checks of the system performance were made for the temperature environment. Less detailed checks were made for the other environments.

The test set-up for functional tests described in this section was similar to that described in paragraph 4.3.2. For convenience, during temperature tests, temporary monitoring connections, in addition to the J5 test connector, were made to selected points of the system and brought out through the temperature chamber wall. This permitted a more direct check of certain areas, such as the comparator, and aided in the interpretation of the system output.

Environmental tests were conducted in the same order that they are discussed in this section.

5.2 High and Low Temperature Tests

The following functional tests were conducted under both elevated and reduced temperatures to verify proper operation of the system: The temperature range used was $-20^{\circ}C$ to $+85^{\circ}C$ except where noted.

1) Synchronization of the system with the master frame sync pulse "B" was checked by verifying channel address counter states relative to the sync pulse.

2) Data acceptance, as a function of buffer memory fullness, was verified at all temperatures between $-20^{\circ}C$ and $+85^{\circ}C$ as noted below.

(a) D-A output for several channels was checked periodically.

(b) Correct function of the comparator was verified -- including correct readout of information from the reference memory.

(c) Buffer memory fullness was modified, by varying the input data rate, and the conditions for data acceptance (i.e., 2X limits, 4X limits, reject, redundant sample control, priority, and force data) were observed and verified to be correct.

3) Commands -- "Force One Sample", and "Change Stored Limits" were inserted and checked for proper execution at a number of points over the temperature range. Operation of the time-slot inhibit function was checked at -20°C and +85°C.

4) Non-destructive bits (limits, address, priority) retention and readout was verified as follows:

"K" limits

a) Loaded at 25°C readout verified at +85°C
b) Loaded at +70°C readout verified at -20°C
c) Loaded at -20°C readout verified at 25°C

Address Bit

The correct pattern of "1"s and "0"s was verified to exist by observing the states of the address bit sense amplifier flip-flop during the last main frame of the master frame.

Priority Bit

The priority bit was written into the reference memory and checked for proper control of data acceptance, at the same temperatures noted for the "K" limits (with the programming used, the priority bit affected only the time slot-II channels).

5) Output codes were verified to be correct by periodically checking for their presence and observing the light patterns on the output monitoring equipment. Output codes verified were:

(a) Word Sync Code (32 bits)

(b) Frame Sync Code (including all states of ÷3, ÷10)

(c) Fullness code (this indication also used to verify control of data acceptance)

6) Output signal parameters were measured at the temperature extremes of -20°C and +70°C.

(a) CPCM Data and code output amplitude and rise time were verified to be within specified limits. The observed values were:

Temperature	P-P amplitude in volts	Rise and Fall times in μsec
-20°C	9.6	less than 1.0
+70°C	10	approx. 1.0

NOTE: Data was observed across a load of a 0.003 microfarad capacitor and a 200 ohm resistor in parallel

(b) Command acceptance pulse was not measured directly during temperature tests but its presence was verified by observing the monitor light on the test and command box after each command.

7) Power supply input voltage was varied at the temperature extremes while proper operation of the system was checked by observing conditions for data acceptance. The voltage variation at +70°C and -20°C was from 22.0 VDC to 32.5 VDC. These were the limits of variation for the laboratory supply used. No change in system operation was noted over this range of supply voltage.

Power consumption at temperature extremes was as follows:

System Input Power

Temperature in degrees Celsius	System clock of 144 Kc		System clock of 288KC	
	Input Current in MA.	Input Power in watts	Input Current in MA.	Input Power in watts
-20°C	550	15.4		
+25°C	480	13.4	640	17.9
+85°	380	10.6W		

Conditions: a) Data input to system was a combination of 5 "1"s and 5 "0"s.

b) Input voltage was 28.0 volts.

8) A test for the limit of input logic level variation was made on the command input to determine maximum "0" and minimum "1" at -20°C, +25°C, and +70°C. Results were:

Temperature	Max. "0" in volts	Min. "1" in volts
-20°C	1.35	2.5* V
+25°C	1.3	2.5*
+70°C	0.85	2.5*

* Limit of variable input source

9) Sequencing of the reference memory was verified with the correct readout of "K" limits and address bit as noted in 4) above.

During the temperature tests, there were problems of system malfunction. Several of these problems were related to the limitations and peculiarities of the integrated circuit logic modules used (see Appendix A). There were some component failures. None of the component failures were the result of bad circuit design or the operation of the components beyond rated limits. Two components, a double junction microdiode and a Gallium Arsenide tunnel diode, had failure modes and rates which make their reliability doubtful. Failures of double junction microdiodes were opens, which were apparently a result of a manufacturing problem with that specific device type. Tunnel diode failures included shorts, opens, and high valley current. The parts lists and assembly drawings were changed to omit these two diode types and to specify diodes which are considered more reliable for future units.

There were three other types of problems encountered during the temperature tests which caused malfunction of the reference memory. It was found that the NDRO sense amplifiers were not sufficiently stable with temperature. To correct this, the NDRO sense amplifier design was changed. Also, it was found that the lower limit allowed for the current pulse amplitude output from the "write" address drivers was too low. As a result of this low amplitude, the NDRO memory cores were not "primed" sufficiently to permit an acceptable "1" output during "read" operations. This was corrected by establishing new limits for "write" current pulse amplitude and revision of component values to obtain outputs within the new limits. Another problem was the false triggering of "read", "write", and "reset" current drivers. This was exhibited at the high temperature and was associated with increased transistor gain at high temperature. Correction was to reduce the triggering sensitivity of these circuits by changing component values.

All of the problems discussed above did not occur at temperatures of +70°C and lower. Performance data were recorded at +70°C prior to rework to make some of the corrections stated. Following vibration and shock tests, corrections were completed. Although detail performance data was not recorded, a test at +85°C for a duration in excess of three hours was conducted and the problems of malfunction at high temperature were proven to be corrected. Also, during the altitude test heat was supplied to the base plate of the unit such that the base plate temperature was above +70°C for more than one hour and was at +85°C for a brief period. Continuous monitoring verified correct operation during this test. Thus, adequate heat transfer to permit correct function of all circuits was proven.

5.3 Vibration Test

5.3.1 Test Set Up

Vibration tests were performed with a Ling-Temco electro-dynamic vibration machine of 7500 pound force rating. The Data Compressor was attached to the vibration table with bolts through each of the four mounting lugs on the equipment base plate. Transducers (Accelerometer type) were attached to points within the Data Compressor to detect the response of the equipment structure and circuit boards to input vibratory motion. A transducer on the vibration table detected the input acceleration level. All acceleration data were recorded on photographic paper strip charts by a light beam galvanometer oscillograph. The envelope of traces on the strip chart represents the peak acceleration values detected by the transducers. Original input and response acceleration data were recorded in g units (32.2 ft/sec^2). The amplification factor, Ar, was computed for each transducer location within the equipment box.

The response amplification factor is defined as the ratio of the response acceleration, at a particular point in the equipment, to the input acceleration at the equipment/vibration table interface.

$$Ar = \frac{Gr}{Gi}$$ where Gr = response acceleration
Gi = input acceleration

A summary of input and response data (major resonances only) appears in Table 5-1. References to equipment axes refer to axes as defined by Fig. 5-1.

The Data Compressor was monitored while being vibrated to determine if any variation from normal operation occurred. Strip Chart recordings were made of the reconstructed analog data output of one channel and of the buffer fullness as indicated by the fullness code word. An oscilloscope was used to monitor the address bit in the last main frame, and periodically, various other test points.

5.3.2 Preliminary Tests

Runs 1 through 6 were exploratory runs at 1/2 g peak amplitude input for the purpose of detecting points in the equipment which produced resonant amplification. The input wave form was sinusoidal with frequencies varying logarithmically with time from 10 to 2000 cps. Very high amplification was observed in the reference memory bit driver and reset driver circuit boards when the input acceleration was in a direction perpendicular to the plane of these circuit boards (Y axis input). Values of Ar of 76 to 100 were observed, the higher value being for the bit driver board. Amplification of 16 to 20 occurred in the reset driver board when the input acceleration was parallel to the plane of the circuit board. (X and Z axes.)

After run 6, the reset and bit driver modules were modified by the addition of stiffening ribs. Also, the surface of the reset board was covered with a 5/16 inch thick layer of rigid polyurethane foam. The foam was expanded in place and firmly adhered to the circuit board.

Run 7 was made to test the effects of the previously described modifications. Three transducers were mounted on the bit driver board, two on the reference memory sense amplifier board, one on the upper magnetic memory module, and one on the reset driver board. Values of Ar of 12.6, 22.4 and 11.0 were obtained, in run 7, on the bit driver. The input level was 1/2 g, permitting direct

comparison with the results of previous 1/2 g runs. The modification reduced the amplification of the bit driver to approximately 1/2 to 1/9 of the previous values (depending on the position that was monitored).

The input level was increased in steps of 1/2 g in each of runs 8 through 11. Ar changed only slightly during the later runs for points on the bit driver and magnetic modules. The values of Ar for the reset driver remained practically constant at approximately 16, during runs 10 and 11. The data for this module, when compared with that obtained before the modification, shows that Ar decreased to approximately 1/5 of its previous value. (No such comparison can be made for the magnetic and sense amplifier modules as data was not recorded prior to the modification.)

After run 11, an additional modification was made to the reference memory. An aluminum reinforcing plate and two stiffening ribs were attached to the auxiliary circuit board at the bottom of the reference memory subassembly. In run 12, the value of Ar for the reset module was 3.8. This represents an additional reduction by approximately a factor of 4. The combined effects of all the modifications reduced the amplification factor of the reset module to 1/20 of the initial value. (From 76 in run 3 to 3.8 in run 12). Data obtained in run 12 for several other points in the Data Compressor indicated a similar reduction in Ar. It is thought that the high response amplitude of the reference memory circuit boards propagated disturbances through the equipment structure into adjacent subassemblies. When the reference memory response was controlled by appropriate design modifications, other points in the equipment received less propagated energy, resulting in an apparent reduction in Ar at these points.

Typical transducer response records for the reference memory reset driver are shown in Fig. 5-2. On the left, is the response curve from run 3, prior to modification of the reference memory. On the right is the record after modification, (Run 12).

5.3.3 Random Vibration

The results of run 12 apparently indicated that the major resonant amplification problems had been eliminated. The largest value of Ar produced was 5.0 on the side of the buffer memory stack (X axis), and this magnitude was not considered objectionable. The unit was then tested for response to Gaussian random vibration (Runs 13, 14 15). The tests were essentially the same as "Test Method B", described in NASA test standard 50M60005, except for the bandwidth. "Test Method B" specifies a bandwidth of 10 to 2000 cps; the actual bandwidth in the test was 20 to 2000 cps because of limitations of the existing test equipment. The input acceleration levels were:

20 g. rms for a period of 4 seconds, followed by
10 g. rms for 180 seconds.

The peak values of input and response acceleration were measured directly by the transducer-recorder system; these values are tabulated in Table 5-1. The rms level of the input acceleration was not directly measured by a transducer. In these tests it was determined by initial adjustment of the noise source.

The peak acceleration during the 4 second period ranged from 51 to 59 g in runs 13, 14, 15. During the 180 second period the average peak value was 27 to 28 g, with occasional spikes ranging up to 34.6 g, in these same runs. A sketch of a typical strip chart record is shown in Fig. 5-3.

Theoretically, the peak acceleration values in true Gaussian random motion range from zero to infinity. In a real physical system, the peak acceleration never becomes infinite, being limited by damping in the test object and available power to drive the vibration table. Typically the peak acceleration values range from approximately 3 to 10 times the rms value. During the 4 second periods of runs 13, 14 and 15, the ratios of peak to rms acceleration were 2.55, 2.90 and 2.94, respectively. During the 180 second periods of these same runs, the ratios were 3.3, 3.26 and 3.46.

The amplification factors during these runs were quite low. The highest value observed was 1.3 on the reference memory reset driver circuit board when the input was in the Y axis direction. The lowest value observed was 0.185 at the logic support post when the input was along the Y axis. Most of the values observed were less than unity indicating that the input acceleration was actually attenuated within the equipment structure.

5.3.4 Sinusoidal Vibration

After the successful random vibration tests, sinusoidal vibration tests were conducted to evaluate the safety margin of the Data Compressor mechanical design. The input amplitude was increased in 1 g steps in successive runs to a maximum of 5 g. The procedure was similar to that of NASA "Test Method A", except that the cross-over frequency was altered to permit smooth blending of the constant displacement inputs and constant acceleration inputs. The NASA method specifies a constant displacement of 0.28 inch double amplitude from 10 to 30 cps. At the upper frequency of 30 cps, 0.28 inch amplitude is equivalent to 13 g acceleration. If cross-over from the displacement mode to a 5 g constant acceleration mode were to be made at 30 cps, an abrupt discontinuity in input g level would result. To permit evaluation of the equipment response at discrete input levels, it was desirable to maintain a constant input amplitude over the major part of the frequency spectrum. For each selected input acceleration level, the cross-over frequency was chosen to permit smooth transition from the 0.28 inch constant amplitude mode. For the 5 g input runs, the cross-over frequency was 18 cps.

The equipment was vibrated along the X axis in the first 5 g test (Run 16). Excessively high resonant response occurred on the side of the buffer memory. A transducer aligned with the X axis detected a response acceleration greater than 112 g*, corresponding to an Ar greater than 22. The equipment cover was removed and several loose screws were found. It was suspected that the modules of the buffer memory were slipping relative to one another, causing

* The amplifier saturated and the maximum value is unknown.

high X axis response. Several Z axis runs were made to test this hypothesis, as both the Z and X axes are parallel to the interface between modules. Runs of 2 g and 3 g input produced vibration response levels which were low. A 4 g input run produced response accelerations with greater than proportional increase over the response of previous runs. Two runs of 5 g input (runs 19 and 23) were made. The peak Z axis response acceleration of the buffer memory was 49 g, corresponding to Ar = 9.8. These results tended to confirm the buffer module slip hypothesis with slip occurring when the input exceeded 3 g. An unusual impact type response was observed in run 19. Z axis transducers on the reference memory and on one of the logic posts detected momentary accelerations as high as 82.5 g. These responses occurred when the sweep frequency was between 15 and 20 cps, coinciding with the cross-over frequency.

Prior to the next series of runs, additional torque was applied to the buffer memory tie rods. The reference memory through bolts and the screws attaching the buffer to the stabilizer frame were also tightened. A 3 g input Z axis run (#25) resulted in successful electrical operation, and no excessive resonances occurred. In run 26, the input was 4 g along the X axis. Complete operational failure occurred soon after the start of the run and the frequency sweep was terminated at 20 cps. Impact type response was again detected by the Z axis transducers on the reference memory and logic post. A peak value of 122 g was recorded. Examination of the equipment cover indicated that the side walls were slightly warped and were not perpendicular to the mounting flange by .078 to .125 inch. The clearance between the inside of the cover and the equipment structure was adversely affected by the distortion of the cover. It was thought that the impact responses observed in runs 19 and 26 were due to either of two causes: contact between the cover and equipment structure, or slipping of the reference memory stack on the base plate.

Several modifications were made to the equipment before the next series of runs. Notches were cut in the edge of the stabilizer frame to increase the

clearance between it and the internal ribs of the cover. A support plate was added to the assembly, spanning the interface between the bottom of the reference memory and the equipment base plate. The purpose of this new part was to more securely connect the memory to the base plate, thus preventing slip. Several X axis runs were then made with input amplitudes ranging from 2 g to 5 g. The power input to the vibration table was manually reduced at several resonant frequencies to prevent possible damage to the equipment from excessive response amplitude. The normal input level was restored after the sweep had passed beyond each of the resonant frequencies. By this procedure, it was determined that critical resonances occurred in the buffer memory at 137 to 150 cps (direct X axis response) and at 380 cps (Y axis "cross talk" on the top buffer circuit board). No operational problems occurred during these runs.

A series of Z axis runs with input amplitudes of 4 g to 5 g was made with no problems occurring. This series was concluded with run 33 at 5 g input. The resonant responses were similar to those of runs 19 and 23, except that impact type responses did not occur in run 33.

Several Y axis runs with inputs ranging from 2 g to 4 g were made. The Ar values of these runs were compared with those of run 12. All values in these runs had increased over the corresponding values in run 12. Values of Ar six times greater than those of run 12 were observed in run 38 at the top of the buffer and reference memories. A 5 g input Y axis run was made with reduced inputs at several resonant frequencies. The response amplitudes were high.

The above comparison of run 12 and the later Y axis sinusoidal runs indicated that the Y axis vibration response had deteriorated. An additional Y axis random vibration test was made (run 40) and the results were much different than those of the previous random test. In run 13 all values of Ar were close to, or less than unity, indicating attenuation. In run 40, many

values were greater than unity, indicating amplification occurred within the equipment. The top of the buffer memory and the reset module displayed Ar values greater than four times the corresponding values in run 13. One more Y axis sinusoidal test was performed (run 41). The input level was 2 g. The response amplitudes were high on the side and top of the buffer memory and at the reference memory reset driver.

5.3.5 Results and Conclusions, Vibration Tests

The vibration testing of the Data Compressor was completed with run 41. The equipment is potentially capable of satisfactory performance when subjected to random vibration, as indicated by the successful runs; 13, 14 and 15. Modifications made to the equipment during the sinusoidal tests altered its Y axis behavior. Excessive resonant response amplitudes occurred in several places during Y axis sinusoidal and random vibration. The buffer memory X axis response amplitude is higher than is desirable. It appears that the addition of the support plate, and the increase in torque of the reference memory tie rods, resulted in more rigid coupling and decreased damping within the equipment structure.

After several of the runs, loose screws were found. In all cases, the screws were plain machine screws which had been erroneously installed. Self-locking screws were installed in the unit and will be used in following units to prevent recurrence of this problem.

During some of the vibration tests, the Data Compressor failed to continue to function correctly. The main cause of failure was broken coaxial wires. These broken coaxial wires failed because of fatigue induced by vibration and by handling prior to vibration tests (several of these wires were broken and repaired prior to vibration tests). These coaxial wires were inadequately supported at the connector. An improved method of support and strain-relief should eliminate this problem in the following flight packages. Broken wires,

other than coaxial type, were due primarily to handling prior to vibration tests and did not indicate a design deficiency. Broken wires occurred mainly in the reference memory which had been partially disassembled several times during previous temperature tests to correct problems.

None of the functional failures, except for the broken coaxial wires discussed above, experienced during vibration tests were due to deficiencies in the mechanical and packaging design of the system. Because of the exploratory nature and the necessity to retest after design corrections, the vibration tests far exceeded the required duration. The mechanical and packaging design, as modified as a result of these tests, is considered adequate to insure that functional performance of future units will not be altered when subjected to the required vibration environment. (This conclusion was further supported by later observations made when the reference memory was disassembled for retrofit rework. Although the observed acceleration of structural members of the reference memory, during the vibration tests, were higher than desirable, there was no evidence of damage caused by vibration or shock.)

5.4 Shock Test

5.4.1 Test Set-up and Method

The Data Compressor was bolted to a fixture plate and was suspended by four vertical cables. A pivoted hammer was struck against the edge of the fixture plate to provide the input shock pulse. The pulse shape, duration, and amplitude were detected by a transducer on the plate and recorded by an oscilloscope and camera. The responses of the internal equipment structure and circuit boards were monitored by the same transducers used in the preceding vibration tests. The responses were recorded on strip charts by a high speed oscillograph. Operation of the equipment was monitored during the shock test by the same techniques as were used in the vibration tests.

5.4.2 Results

One impact was applied to the equipment in each of two directions, along each of three axis. Each impact was an approximate half sine wave pulse of 50 g peak amplitude and 11 milliseconds duration. The maximum response amplitude was 65 g and occurred on the reference memory reset circuit board when the input was along the negative Y axis. A summary of input and response data is contained in Table 5-2. There was no apparent damage or malfunction caused by the shock test.

5.5 Moisture Resistance Test

The ability of the equipment to resist entry of humid air at elevated temperature depends upon the integrity of the gasket seals. As long as the seals do not leak, and a slight positive internal gas pressure is maintained, humid air cannot penetrate to the interior of the equipment. A simple elevated temperature leak test was deemed sufficient to prove the moisture resistance ability of the equipment.

Prior to the test, the valve mounting nuts, and the cover mounting screws and nuts were tightened. Dry nitrogen, at a pressure of 7.4 inches of mercury, was flowed into the unit through the filler valve. A soap suds solution was applied to all seams and joints except the relief valve core and connector inserts. No leaks were detected. A test chamber was pre-heated to +85°C. The equipment was then placed in the chamber and allowed to remain for approximately 30 minutes. A soap solution test was performed while the equipment was hot. No leaks were detected. The equipment was allowed to cool to room temperature and was allowed to remain in the laboratory for two days. At the conclusion of this time, the relief valve core was depressed and gas flowed out. Retention of pressure for this period of time after temperature cycling, indicated that the unit was satisfactorily sealed.

5.6 Altitude Test

To determine if the Data Compressor would be damaged by low pressure when operating on a vehicle at high altitude and to verify that the thermal design was adequate, a combination altitude-temperature test was performed. This combination of low pressure and high temperature was chosen to prove that both mechanical and thermal design was adequate.

The equipment was placed in a sealed chamber and the chamber pressure was gradually reduced by a vacuum pump. At the same time, heat was supplied to the chamber to raise the equipment to the test temperature of $+70^{\circ}C$. The equipment temperature was measured by 5 thermocouples mounted on the base plate. The total elapsed time of the test was six hours. For a period of slightly more than one hour, the chamber pressure was 10^{-4} mm of mercury and the equipment temperature ranged from $+70^{\circ}C$ to $+85^{\circ}C$. At the conclusion of the one hour test period, the chamber pressure and temperature were gradually returned to normal room ambient conditions. The unit was then visually inspected and it was verified that no damage had incurred from the test.

The equipment was operating continuously during the test and was monitored in the same manner as in the vibration test. No variation from normal, correct operation occurred during or after the test.

TABLE 5-1 ENVIRONMENTAL TEST D

RUN NO.	AXIS	FREQ BAND	TIME DURATION	RESONANT FREQ (CPS)	PEAK G_1 INPUT (g UNITS)	G_R
1	X	10-2000	10 MIN	200	1/2	-
↓	↓			450		-
↓	↓					REF MEM
2	Z	10-2000	10 MIN	200	1/2	-
↓	↓			600		-
↓	↓			1400		-
↓	↓					←
3	Y	10-2000	10 MIN	182	1/2	
↓	↓			520		
↓	↓					←
4	Y	10-2000	10 MIN	200	1/2	
↓	↓					←
5	Y	10-2000	10 MIN	190	1/2	42
↓	↓					REF MEM BIT DRVR
6	Y	10-2000	10 MIN	188	1/2	
↓	↓					
7	Y	10-2000	10 MIN	190	1/2	11.2
↓	↓					REF MEM BIT DR.
8	Y	10-2000	10 MIN	200	1.0	20.6
↓	↓					←
9	Y	10-2000	10 MIN	185	1.5	35
↓	↓					←
10	Y	10-2000	10 MIN	200	1.5	34
↓	↓					←
11	Y	10-2000	10 MIN	175 TO 200	2.0	44
↓	↓					←
12	Y	10-2000	10 MIN	200	2.0	10
↓	↓			420		
↓	↓					SIDE OF BUFFER
13	Y	20-2000 RANDOM	4 SEC	N/A	58	39
↓	↓		180 SEC	N/A	27 AVG. 33 MAX.	9.5 AVG. 20 MAX.
↓	↓					←
14	Z	20-2000 RANDOM	4 SEC	N/A	51	< 20
↓	↓		180 SEC	N/A	28 AVG. 32.6 MAX.	APPROX. 8.9
↓	↓					←
15	X	20-2000 RANDOM	4 SEC	N/A	59	< 45
↓	↓		180 SEC	N/A	AVG. ? 34.6 MAX	APPROX 13 APPROX 42.
↓	↓					←

.P.U. MODEL DATA COMPRESSOR-SUMMARY OF VIBRA

TRANSDUCER CHANNELS (ALL G_R = 0 TO PEAK VALUE

	5		6		7	
A_R	G_R	A_R	G_R	A_R	G_R	A_R
	-		-		8	16
			6	12	8	16
Z AXIS	BUF MEM	Z AXIS	BUFFER	Y AXIS	REF MEM RESET DR	Y AXIS
	-		1	2	10	20
	-				12	24
					7	14
SAME TRANSDUCER POSITIONS AS RUN #1						
			7	14	38	76
	3 TO 5	6 TO 10			12	24
SAME TRANSDUCER POSITIONS AS RUN #1						
					40	80
SAME TRANSDUCER POSITION →					REF. MEM DRIVER	BIT BOARD
84	15	30	7	14	50	100
Y AXIS	REF MEM BIT DRVR	Y AXIS	BUFFER	Y AXIS	REF MEM BIT DRVR	Y AXIS
			5	10	20 (?)	40
			LOGIC CARD	Y AXIS	LOGIC CARD	Y AXIS
22-4	6.3	12.6	TRANSDUCER BROKE LOOSE		10	20
Y AXIS	REF. MEM BIT DR.	Y AXIS	REF MEM SENS AMP	Y AXIS	TOP MAG MODULE	REF
20.6	11.2	11.2			15.3	15.3
SAME TRANSDUCER POSITIONS AS RUN #7						
23.3	19.5	13			23	15.3
SAME TRANSDUCER POSITIONS AS RUN #7						
	19.5	13			23	15.3
SAME TRANSDUCER POSITIONS AS RUN #7						
22	27.2	13.6	-	-	31.5	15.7
SAME TRANSDUCER POSITIONS AS RUN #10						
5.0	NEGLIGIBLE		7.5	3.8	5	2.5
	NEGLIGIBLE				4.3	2.14
Y AXIS	SIDE OF BUFFER	Z AXIS	REF. MEM RESET	Y AXIS	TOP OF BUFFER	Y AXIS
0.67	14.6	0.25	60	1.04	51	0.88
0.35 0.67	6.6 AVG.	0.24	33 AVG. 43 MAX	1.22 1.30	22.5 AVG 30 MAX.	0.83 0.91
SAME TRANSDUCER POSITIONS AS RUN 12						
< 0.39	< 20	< 0.39	33,4	0.66	59	1.15
APPROX. 0.32	14 AVG. 21 MAX	0.5 AVG. 0.64	11.2 AVG 19.2 MAX	0.40 0.59	22 AVG 32.5 MAX	0.79 0.99
SAME TRANSDUCER POSITIONS AS RUN 12						
< 0.76	< 31	< 0.53	33.5	0.57	50.5	0.86
APPROX. 1.23	APPROX 9 APPROX 14	APPROX. 0.4	11.2 AVG 18.4 MAX	- 0.53	21 AVG 31.5 MAX	- 0.91
SAME TRANSDUCER POSITIONS AS RUN 12						

5-17-2

TION TEST DATA

8		9		REMARKS
G_R	A_R	G_R	A_R	
-		7	14	INCREASING FREQ SWEEP
2.5	5	3	6	NO TRANSDUCERS WERE ALIGNED
LOGIC POST	Z AXIS	LOGIC POST	Z AXIS	WITH INPUT AXIS (ALL RESPONSE IS CROSSTALK)
7	14	7	14	
				INCREASING FREQ SWEEP
			→	
		10.5	21	INCRREQ SWEEP
		5	10	VERY HIGH RESPONSE #7 TOP
			→	CkT. BOARD OF REFERENCE MEM.
				INCREASING FREQ SWEEP
← SAME AS RUN #1			→	#7 TRANSDUCER MOVED TO BIT DRIVER BOARD HIGH RESPONSE
10	20	5	10	INCREASING FREQ SWEEP #4. 5. 9 MOVED
LOGIC POST	Z AXIS	STABILIZER FRAME Y AXIS		BIT DRIVER SHOWS HIGH RESPONSE
				INCREASING FREQ SWEEP. #6 7 ~~MOVED TO SURFACE OF LOGIC CARDS~~ #7 RECORDS SHOW HIGH NOISE CONTENT
11	22	5.5	11	INCREASING FREQ SWEEP. 1ST RUN ~~AFTER MODIFICATION TO REF. MEM~~
REF MEM SENS AMP	Y AXIS	REF MEM BIT DR.	Y AXIS	BIT DRIVER AND RESET DRIVER
15	15	10.5	10.5	INCREASING FREQ SWEEP . SAME
			→	AS RUN 7 EXCEPT HIGHER INPUT
25	16.6	19.5	13	INCREASING FREQ SWEEP. SAME
			→	AS RUN #7 EXCEPT HIGHER INPUT.
25	15.3	24.5	16.3	INCREASING FREQ SWEEP. SAME AS
	→	REF.MEM RESET DR	Y AXIS	RUN 9 EXCEPT #9 TRANSDUCER MOVED
31	15.5	33.2	16.6	INCREASING FREQ SWEEP. SAME AS
			→	RUN 10 EXCEPT HIGHER INPUT
NEGLICIBLE		NEGLICIBLE		INCREASING FREQ SWEEP. 1ST RUN ~~AFTER REWELDING. PLATE ADDED~~
NEGLICIBLE		NEGLICIBLE		TO AUX CKT. BOARD.
SIDE OF REFERENCE	Z AXIS	LOGIC POST	Z AXIZ	TRANSDUCERS RELOCATED
11.4	0.2	11	0.19	VALUES INDICATED 'MAX' ARE FOR
6 AVG. 7.7 MAX.	0.22 0.23	5 AVG.	0.185	OCCASIONAL SPIKES PROJECTING
			→	BEYOND AVERAGE DATA ENVELOPE
				~~ELECTRONIC OPERATION OK FOR~~ DURATION OF TEST.
32.2	0.63	26.5	0.5	MAX & AVG. SAME MEANING AS PREVIOUS RUN. #4 & 5 CHANNELS
12 AVG 14.2 MAX	0.43 0.44	10.8 AVG	0.33	INDISTINCT RECORD; VALUE
			→	ESTIMATED ELEC. OPERATION OK
14.2	0.24	17.8	0.3	MAX AND AVG. SAME AS BEFORE
6.2 AVG 7.7 MAX	0.22	6 AVG 10.8 MAX	0.31	INPUT RECORD FUZZY, CAN'T DETERMINE AVG. VALUE.
			→	#4 & 5 CHANNELS INDISTINCT, VALUE EST. ELECTRONIC OPERATION OK

TABLE 5-1 ENVIRONMENTAL TEST

RUN NO.	AXIS	FREQ BAND	TIME DURATION	RESONANT FREQ (CPS)	PEAK G_1 INPUT (g UNITS)	G_R
16	X	10-2000	5 MIN UP	15 CPS UP	5	50
↓	↓		5 MIN DWN	150 UP 185 DWN		112 *
				206		
				350		
				373		
				~ 500		
↓	↓					←
17	Z	10-2000	5 MIN UP		2	
↓	↓		5 MIN DWN			
↓	↓					←
18	Z	300-600-300				
19	Z	10-2000	10 MIN	12 CPS	5	
↓	↓			21		
				60		
				130		17
				200		
				400		
				880		25
				1000		
↓	↓					←
20	Z	10-2000	5 MIN		2	
↓	↓					
↓	↓					←
21	Z	10-2000	5 MIN		3	
↓	↓					
↓	↓					
22	Z	10-2000	5 MIN		4	
↓	↓					
↓	↓					←
23	Z	10-2000	5 MIN UP	12 CPS	5	
↓	↓		5 MIN DWN	30		
				40 TO 80		
				130		14.4
				200		
				420		
				880		23
				1000		
↓	↓					←

D.P.U. MODEL DATA COMPRESSOR-SUMMARY OF VIBRA

TRANSDUCER CHANNELS (ALL G_G = 0 TO PEAK VAI

4	5		6		7	
A_R	G_R	A_R	G_R	A_R	G_R	A_R
10	CABLE LOOSE					
> 22	NO DATA		16.5	3.3	15	3
			31.8	6.4	15	3
			30	6		
					47.5	9.5
					50	10
	SAME TRANSDUCER POSITIONS AS RUN 12					
	APPARENT HIGH OUTPUT OF ~~DUBIOUS VALIDITY~~					
	SAME TRANSDUCER POSITIONS AS RUN 12					
	NO RESPONSE					
	10	2				
	21	4.2				
	30	6				
3.4						
	26.6	5.3	14	2.8	10	2
	42	8.4				
5					30	6
			25	5		
	SAME TRANSDUCER POSITIONS AS RUN 12					
	SAME TRANSDUCER POSITIONS AS RUN 12					
	SAME TRANSDUCER POSITIONS AS RUN #12					
	SAME TRANSDUCER POSITIONS AS RUN #12					
	18	3.6				
	26.5	5.3				
	27	5.4				
2.9					8	1.6
	42	8.4	13.6	2.7	13.6	2.7
	49	9.8				
4.6					35	7
			24	4.8		
	SAME TRANSDUCER POSITIONS AS RUN 12					

5-18-2

TION TEST DATA

LMSC 8-39-66-2

.UE) 8 G_R	8 A_R	9 G_R	9 A_R	REMARKS
↑		↑		TWO SWEEPS 5 MIN. EACH
				*AMPLIFIER SATURATED
				VALUE IS ESTIMATED
10-15	2-3	~ 15	~ 3	INTERMITTANT ELECTRICAL
↓		↓		OPERATION. RETURNED TO
				NORMAL AFTER TEST.
				LOOSE SCREWS FOUND AFTER TEST.
				#4 TRANSDUCER IS BONDED TO TWO
			→	ORTHOGONAL SURFACES. IMPROPER INSTALLATION.
				UNIT OPERATED SATISFACTORILY
				THRU BOTH SWEEPS. APPARENT
			→	HIGH RESPONSE ON #5. DRIFTING AND FUZZY IN APPEARANCE
				BRIEF RUN TO CHECK TRANSDUCERS
				UNIT FAILED TO OPERATE ABOUT
20 ⊡	4	82.5 ⊡	16.5	20 CPS. BECAME OPERATIVE AFTER
				TEST. FUZZY TRACES ON #5 FROM
				60 CPS UP. FUZZY TRACES AND
32	6.4	56	11.1	SPIKES ON #9 FROM 20 CPS UP.
				⊡ SHARP PEAKS BETWEEN 15-20 CPS
		27	5.4	#8 AND 9 EXACT CORRESPONDENCE
				OF PEAKS
			→	INCREASING FREQUENCY SWEEP.
				A FEW RESONANCES OF LOW
				MAGNITUDE. ELECTRICAL
				~~OPERATION OK. UNIT WELL BEHAVED~~ MECHANICALLY
			→	INCREASING FREQUENCY SWEEP
				A FEW RESONANCES OF LOW
				MAGNITUDE. WELL BEHAVED
			→	ELECTRICALLY & MECHANICALLY. INCREASING FREQ. SWEEP
				#5 TRANSDUCER SHOWS 1ST RESPONCE
				AT 18 CPS. GENERALLY HIGH
				RESPONSE UP TO 25 G OVER A BAND
				OF FREQUENCIES 40 TO 800 CPS.
				DEFINITELY HIGHER THAN LINEAR
				INCREASE OVER RUN 21.
				ELECTRICAL OPERATION OK.
			→	INCREASING FREQUENCY SWEEP
				ELECTRICAL OPERATION OK ON UP
				SWEEP FAILURE OCCURED ON DOWN
				SWEEP. REF. MEMORY FAILED
17	3.4	17.8	3.56	~~ABOVE 1000 CPS. POWER SHORT~~
34	6.8	36.5	7.3	AT 20 CPS. RESONANCE PATTERN
				RESEMBLES THAT OF RUN 19 EXCEPT
				THAT HIGH AMPLITUDE SPIKES AT
		8.7	1.74	~~15-TO 20 CPS. DID NOT OCCUR IN~~ THIS RUN. LOOSE SCREWS AND BROKEN
				WIRE. LOOSE WASHER FREE IN BUFFER.
			→	

5-18-3

TABLE 5-1 - ENVIRONMENTAL

RUN NO.	AXIS	FREQ BAND	TIME DURATION	RESONANT FREQ (CPS)	PEAK G_1 INPUT (G UNITS)	4 G_R
24	Z	10-2000			?	
25	Z	10-2000	5 MIN UP		3	
↓	↓		5 MIN. DWN			←
26	X	10-20	SHORT	< 20	4	LOW
↓	↓					
↓	↓					←
27	X	10-2000	5 MIN	137*	4	60
↓	↓			248		20
↓	↓			327		22
↓	↓			400		
↓	↓			930		
↓	↓					←
28	X	00 TO 2000			2	
↓	↓					←
29	X	10-2000			5	
↓	↓					
↓	↓					←
30	X	10-2000	5 MIN.		5	
↓	↓					
↓	↓					←
31	Z	10-2000	5 MIN		4	
↓	↓					
32	Z	10-2000	5 MIN		4	
33	Z	10-2000	5 MIN UP	131	5	7.9
↓	↓		5 MIN DWN	210		
↓	↓			376		
↓	↓			800		38.5
↓	↓					←
34	Y	10-2000	5 MIN	199	3	23.2
↓	↓			315		
↓	↓			967		
↓	↓					←
35	Y	10-2000	5 MIN	200	4	30.2
↓	↓			355		
↓	↓					←
36	Y	10-2000	5 MIN.			
↓	↓					
↓	↓					
37	Y	100-400		230	3	
↓	↓					
↓	↓					
↓	↓					

TEST D.P.U. MODEL DATA COMPRESSOR-SUMMARY OF

	TRANSDUCER CHANNELS (ALL G_R = 0 TO PEAK VA					
	5		6		7	
A_R	G_R	A_R	G_R	A_R	G_R	A_R
SAME TRANSDUCER POSITIONS AS RUN 12						
	LOW		LOW		LOW	
SAME TRANSDUCER POSITIONS AS RUN 12						
15	↑		13.4	3.35	15.9	3.96
5	NO		35.3	8.8	15.4	3.85
5.5	DATA					
					48	12
	↓				15.4	3.95
SAME TRANSDUCER POSITIONS AS RUN 12						
SAME TRANSDUCER POSITIONS AS RUN 12						
SAME TRANSDUCER POSITIONS AS RUN 12						
SAME TRANSDUCER POSITIONS AS RUN 12						
1.58	↑				13.6	2.72
	NO				15.4	3.1
	DATA				13.6	2.72
7.7	↓		26.6	5.3	40.2	8.05
SAME TRANSDUCER POSITIONS AS RUN 12						
7.3	NO		48.5	16.2	35	11.7
	DATA		24.7	8.25	40	13.3
					16.8	5.6
SAME TRANSDUCER POSITIONS AS RUN 12						
7.6	NO		61.6	15.4	50	12.5
	DATA				50	12.5
SAME TRANSDUCER POSITIONS AS RUN 12						
					47	15.6

5-19-2

VIBRATION TEST DATA

LMSC 8-39-66-2

LUE)				
8		9		REMARKS
G_R	A_R	G_R	A_R	
				INPUT TRANSDUCER OUT OF CALIBRATION
				ELECTRICAL OPERATION OK
			→	NO EXCESSIVE RESONANCES
122		33.5		COMPLETE ELECTRICAL FAILURE TEST
				STOPPED AT 20 CPS. CRUSHED WIRE
			→	~~UNDER REF. MEMORY. LOOSE PIECES~~ OF WIRE INSIDE REF. MEMORY.
10.4	2.6	9.8	2.45	INCREASING FREQ. SWEEP
16.3	4.1	19.5	4.87	INPUT g REDUCED 137 TO 200 CPS
			→	
				INPUT g REDUCED AT SEVERAL
			→	RESONANCE POINTS
				INCREASING FREQUENCY SWEEP.
				INPUT g REDUCED AT RESONANCE
			→	~~BUT NOT INCREASED SOON ENOUGH~~ THEREAFTER. NO VALID DATA
				INCREASING FREQ. SWEEP. INPUT
				g REDUCED AT 137 CPS, RESTORED
			→	TO FULL LEVER AFTER. ELECTRICAL OPERATION OK
ERATIC				INCREASING FREQ SWEEP
RESPONSE				BROKEN SHIELD IN #8 CABLE
				INCREASING FREQ SWEEP
22.2	4.44	20.7	4.15	ELECTRICAL OPERATION OK
39.3	7.85	39.6	7.9	
19.2	3.85	18.3	3.66	
			→	
11.6	3.87	APPROX 10	3.33	INCREASING FREQ SWEEP
				ELECTRICAL OPERATION OK
			→	
14.5	3.62	12.2	3.05	INCREASING FRRQ. SWEEP
				ELECTRICAL OPERATION OK
			→	
				TEST VIBRATION TABLE FOR
				RESONANCE DATA COMPRESSOR
				REMOVED. NO RRSONANCE
				VELOCITY PICKUP TRANSDUCER
				USED TO MONITOR TABLE. PURPOSE
				WAS TO CHECK CONTROL SYSTEM.

5-19-3

TABLE 5-1 ENVIRONMENTA

RUN NO.	AXIS	FREQ BAND	TIME DURATION	RESONANT FREQ (CPS)	PEAK G_1 INPUT (g UNITS)	G_R
38	Y	10-2000	5 MIN	200	2	17.
↓	↓			370		7.9
↓	↓			800		5.3
↓	↓					←
39	Y	10-2000	5 MIN UP		5	
↓	↓		5 MIN DWN			
↓	↓					
↓	↓					
↓	↓					←
40	Y	20-2000	4 SEC	N/A	36.5	73
↓	↓	RANDOM	180 SEC	N/A	21.3 AVG 25.3 MAX	32.8 AVG 67.5 MAX
↓	↓					←
41	Y	10-2000	10 MIN	212	2 g	26
↓	↓			428		
↓	↓			484		
						SIDE OF BUFFER

L TEST D.P.U. MODEL DATA COMPRESSOR-SUMMARY OF VIBR

· TRANSDUCER CHANNELS (ALL G_R = 0 TO PEAK VALUE

	5		6		7		8
A_R	G_R	A_R	G_R	A_R	G_R	A_R	G_R
8.55	NO		50.5	25.5	30.3	15.2	11.6
3.95	DATA				30	15	
2.65					15	7.5	
		SAME TRANSDUCER POSITIONS AS RUN 12					
		SAME TRANSDUCER POSITIONS AS RUN 12					
2.0	NO		169	4.63	137*	> 3.75	34.2
1.54 2.67	DATA		93 AVG 162 MAX	4.36 6.4	78 AVG 100 MAX	3.66 3.95	17.4 AVG 18.2 MAX
		SAME TRANSDUCER POSITIONS AS RUN 12					
13			52	26	NOT		NOT
					RECORDED		RECORDED
			21	10.5			
X AXIS	SIDE OF BUFFER	Z AXIS	REF MEM RESET	Y AXIS			

5-20-2

	9		REMARKS
A_R	G_R	A_R	
5.8	11	5.5	INCREASING FREQ. SWEEP
		↓	
			INPUT g REDUCED AT APPROX.
			200 CPS & 350 CPS. ELECTRICAL
			OPERATION OK DURING UPSWEEP
			ONE DISCONTINUITY DURING
		↓	DOWN SWEEP
0.94	31.7	0.87	* APPROX AS AMPLIFIER SATURATED
0.82 0.72	16.5 AVG 26.3 MAX	0.77 1.02	ELECTRICAL MALFUNCTION
		↓	
	34	17	INCREASING FREQ SWEEP
	29	14.5	TRANSDUCERS MOVED TO NEW
			POSITIONS. WIRE BROKE
	TOP OF BUFFER	Y AXIS	DURING TEST

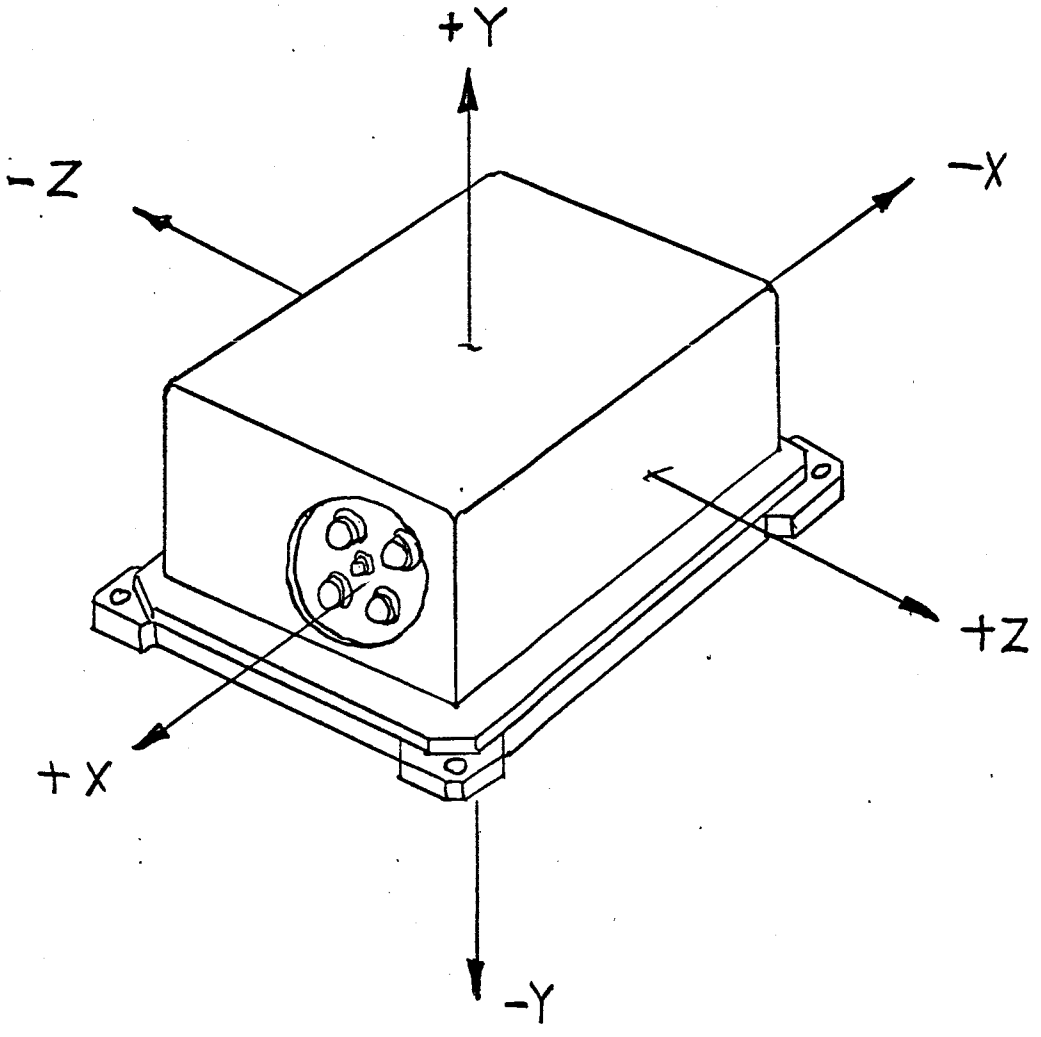
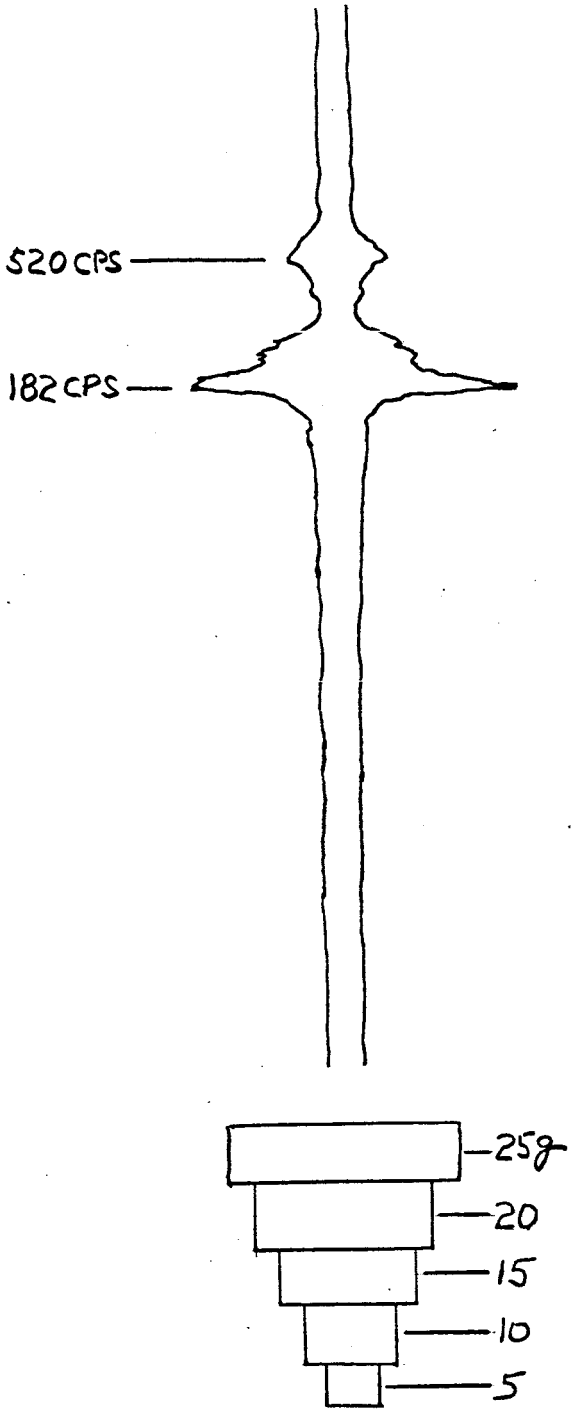


FIGURE 5-1 DIRECTION OF AXES

RUN 3, CHANNEL 7
Y AXIS ½ g INPUT



RUN 12, CHANNEL 6
Y AXIS 2 g INPUT

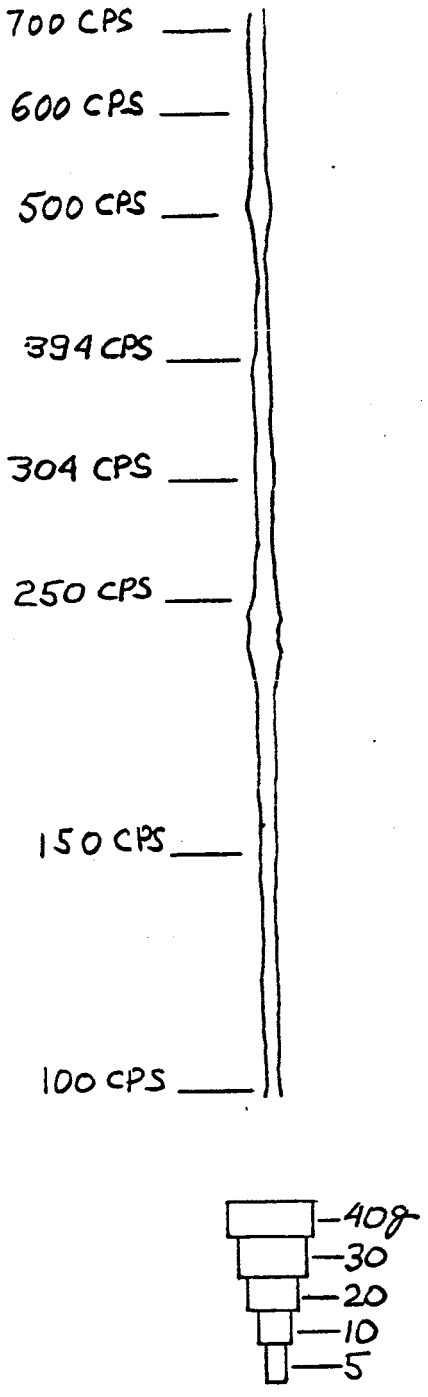


FIGURE 5-2 RESPONSE RECORDS OF RESET MODULE BEFORE & AFTER MODIFICATION (DIFFERENT SCALE FACTORS & CHART SPEEDS)

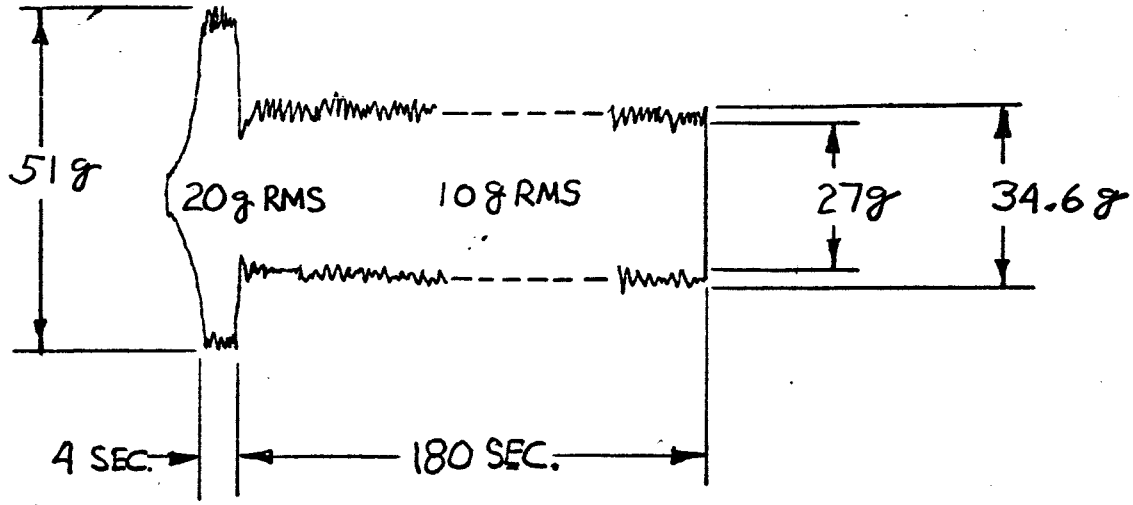


FIGURE 5-3 RANDOM VIBRATION INPUT

Table 5-2 Shock Test Data

RUN	AXIS	INPUT PEAK g	INPUT TIME (MILLISEC)	PEAK RESPONSE ACCELERATION (g) REF.MEM RESET Y AXIS	TOP OF BUFFER Y AXIS	SIDE OF BUFFER X AXIS	SIDE OF BUFFER Z AXIS	SIDE OF REFERENCE MEMORY Z AXIS	LOGIC POST Z AXIS	REMARKS
S1	+X	50	11	LOW	LOW	52.5	LOW	NO DATA	NO DATA	Electrical operation OK
S2	-X	50	11	LOW	LOW	58	LOW	NO DATA	NO DATA	Electrical operation OK
S3	-Z	50	11	NO DATA	LOW	NO DATA	LOW	54	47.5	Electrical operation OK
S4	+Z	50	11	NO DATA	LOW	NO DATA	LOW	~50	60	Electrical operation OK
S5	+Y	>50	11	52	48	LOW	32	NO DATA	NO DATA	>50 g Bounce of Fixture Electrical operation OK
S6	-Y	(?) SCOPE CAMERA FAILED TO RECORD		65	57	26.3	43.5			Electrical operation OK
S7	-Y	50	12	NO RECORD	NO RECORD	LOW	NO RECORD	NO DATA	NO DATA	Electrical operation OK - 3 recorder channels produced records that could not be read

NOTE: Run S7 was repeat of Run S6 because of failure of camera to record input shock pulse.

Section 6
CONCLUSIONS AND RECOMMENDATIONS

The functional, packaging and mechanical design was accomplished and proven by test to meet all established goals and requirements with two exceptions. These two exceptions are:

1) Correct performance of the Data Compressor was proven over the temperature range of -20°C to +70°C. Goal was for performance up to +85°C.

2) Maximum "false" logic level at the Data Compressor inputs was 0.85 volt when subjected to the high temperature environment. Goal was for a maximum "false" logic level of 1.0 volt or greater over the entire temperature range of -20°C to +85°C.

These two exceptions to the intended performance are not expected to result in any difficulty in the actual use of the Data Compressor in a space vehicle telemetry system. Also, if the additional effort is warranted, the circuit design can be improved to meet all of the established performance goals.

By application of information obtained from test results of the first experimental flight package, additional flight packages can be produced which will meet the established requirements.

On the design and test of the first experimental flight package, much effort was required to design around the limitations of the Texas Instruments, Inc. Series 51 integrated circuits. It is recommended that the precautions stated in Appendix A, in addition to those recommended by the circuit manufacturer, be observed whenever these circuits are employed in new designs.

The advantage of a combination of destructive and nondestructive storage in the reference memory was apparent. The use of this technique in the first experimental

flight package permitted a significant reduction in the complexity of reprogramming to accommodate multiplexer format change. It is recommended that, where long term reliability of data storage is required, a method of nondestructive readout be employed. When both temporary and semipermanent data are to be stored in the same memory, a choice must be made between all DRO, all NDRO, or a combination of DRO and NDRO storage. The combination of DRO and NDRO is capable of high long term reliability for storage of semipermanent data and lower cost than for all NDRO storage. For the application of a reference memory within a data compressor system, the combination of DRO and NDRO storage is recommended.

Section 7
REFERENCES

1. Lockheed Missiles & Space Company, Annual Technical Report, Advanced Telemetry System With Adaptive Capability, by J. A. Horton, H. N. Massey, and W. E. Smith, Report No. 657617, 30 July 1963

2. Lockheed Missiles & Space Company, Operation Manual, Advanced Telemetry System With Adaptive Capability, (Data Compressor), Model TDC-1, by J. A. Horton and H. N. Massey, Report No. 8-39-65-4, 1 November 1965

APPENDIX A

Problems and Precautions in the Application of Texas Instruments, Inc. Series 51 Circuit Modules

Experience gained in the design and debugging a system, which employs Texas Instruments, Inc., Series 51 Circuit Modules, has resulted in an awareness of several limitations which are not clearly evident from the circuit manufacturer's data sheets. General statements of these limitations will be made to indicate the nature of the problem. Detail analysis of the circuit modules, to relate fabrication or circuit details to the limitation, is not stated here. Also, it is recognized that some circuit modules may not exhibit the problem described and that in many applications the described circuit module limitation may not result in a system malfunction. However, each of the problems described here have been encountered. Suggestions are given for correction or avoidance of these problems. (No claim is made that the problems stated here define the extent of the limitations for these circuit modules.)

1. Flip-Flops (SN510)

   a) Preset duration -- When connected as a binary element, with both clock and preset inputs used, the circuit may not respond correctly to preset inputs of short duration. An example is the case where the preset follows immediately after a clock pulse. In this example, the final state of the circuit may not correspond to the preset state if the preset pulse duration is too short. Experimentally, it has been observed that incorrect operation of the binary element may result with a preset duration of 2 μseconds or less at room temperature and 6 μseconds or less at + 85°C. Proper operation can generally be expected at high temperature when a preset duration exceeding 10 μseconds is employed. Suggested design rules to avoid this problem are: (1) avoid use of preset input if possible; (2) avoid presetting immediately after a clock input; and (3) if (1) and (2) cannot be achieved, use a preset duration of at least 10 μseconds and preferably much longer.

b) Coupling from output to preset input -- This problem may be observed with both binary and shift register connections of the module. When connected as one stage of a multi-stage shift register, with the preset input of all stages driven from a common source, undesired presetting of some of the stages may result. This is caused by current flow from the preset input of the offending module to preset inputs of the other modules whenever the state of the offending module is changed. Similar results can be observed when these modules are connected as binary stages of a counter with preset inputs driven from a common source. Also, even when the offending module is operated individually as a binary element, the rise time of the output on pin 6 may be degraded. Suggested design rules to avoid this problem are: (1) if the preset is used, provide a low DC resistance path to logic ground; (2) if the the preset input is not used, connect the preset input directly to logic ground.

c) Coupling from output to clock input, binary connection -- When connected as a binary stage, changing the state of the flip-flop while the clock input is high produces negative-going noise at the clock input. Also, when negative-going noise is applied to a high collector output, with the clock input high, negative-going noise at the clock input will be produced. This effect has been found to be sufficient to result in the amplification of noise in a ripple counter in the reverse direction to normal signal flow. Also, when the ripple counter has several stages, noise produced by presetting the last stage has been amplified to the extent of causing the third or fourth stage, prior to the last, to flip. Again, it must be remembered that a required condition to produce this undesired reverse propagation is that the clock input be driven from the collector of a preceding stage which is in the high voltage state. Suggested design rules to follow to avoid this problem are: (1) avoid presetting a

c) Continued
stage of the ripple counter when the above condition exists for preceding stages; (2) if (1) cannot be followed, provide a diode-resistor decoupling network between the clock input and the collector of the preceding stage to prevent reverse propagation.

d) Internal coupling to clock input and clock input sensitivity, shift register connection -- When several modules are employed in a shift register, with a common source for the shift clock, the combination of internal coupling to the clock input and the sensitivity to small voltage swings at the clock input can produce false shifting of some stages. This is especially true if the states of some of the stages are changed when the shift clock line is in the high voltage state. Also, when the state of several stages change, as a result of the fall of the shift clock pulse, a small positive pulse occurs on the shift line immediately following the fall of the shift clock pulse. This small positive pulse has the effect of another clock pulse for the more sensitive modules -- especially at high temperature and when 10 or more modules are driven from the same source. Suggested design rules to reduce these problems are: (1) arrange for the shift clock line to be low whenever the state of any register stage is changed by means other than the clock input; (2) use a clock source which can provide drive in both directions, such as a SN517 "clock driver"; (3) split-up the shift line into two or more lines and drive each line from a separate clock source; (4) provide a low resistance path from the shift line to ground during the low state of the shift clock -- especially immediately following the fall of the clock pulse such that noise does not exceed + 0.5 volt above logic ground.

e) Clock amplitude versus logic level -- For shift registers and counters it has been observed that, to insure correct operation, the clock pulse amplitude should not exceed the level of the $\overline{S}$ or $\overline{R}$ steered inputs. This is especially troublesome with ripple

e) Continued

counters where the clock input of one stage is driven by the logic output of the preceding stage. The following design rules are suggested to avoid or minimize this problem: (1) for shift register clocking, limit the maximum clock pulse amplitude to approximately one-half (1/2) the normal high logic level; (2) if a clock input is driven from a gate collector output, provide DC loading to logic ground to lower the high level output from the gate; (3) for ripple counters, limit the clock pulse amplitude applied to the first stage to approximately one-half (1/2) the normal high logic level and maintain equal loading on all collector outputs of the counter.

2. Circuits with emitter-follower outputs (SN511 and SN513)

Difficulties have been experienced in most attempts to use the emitter follower outputs of these modules. This problem lies primarily in the fact that, for a low level out, the output is clamped to the ground through a diode plus a transistor in series. Thus, after the output falls to approximately one volt, the impedance to ground is relatively high. When several gate inputs are driven by one of these emitter-follower outputs and short (1 to 2 μseconds) duration pulses are involved, some of the gate inputs may not be sufficiently turned off. As previously indicated this type of emitter-follower output is not suitable for driving multiple clock loads such as shift registers. The following design rules are suggested: (1) where high speed in achieving the low logic level is important, use of these emitter-followers should be avoided or a DC load to ground should be connected (when DC loading to ground is used, the fan-out and module power dissipation must be checked); (2) alternate circuits, such as the SN517 "clock driver" module should be used to drive multiple clock inputs.

3. Output to Input coupling in gates (SN512, SN513, SN514 and SN515)

All types of gates listed here have been observed to exhibit signal feedback from output to input during the rise of output voltage. When the feedback is to a driven input, additional drive considerations are required. When the feedback is to an unused and ungrounded input (an input driven directly from the emitter-follower output of a SN511 or SN513 module can be considered to be in this category), the output rise time will be degraded. Suggested design rules, to avoid problems due to this output-to-input coupling, are: (1) all unused gate inputs should be connected to logic ground; and (2) when speed is important, provide a low resistance path from the input to ground when the logic level is low.

4. Sensitivity to high frequency noise at gate inputs (SN512, SN513, SN514, and SN515)

For the gates listed here, it has been observed that, when all but one input are low, a fast negative-going noise spike of approximately one volt in amplitude, at the input which is high, can produce a positive-going spike at the gate output. This occurs even though the absolute voltage at this input is never below + 3 volts above ground. (The noise spike is apparently coupled through the speed-up capacitor in the gate input circuit.) When the gate output drives the preset input of a flip-flop, undesired presetting can result. Since the fall time of the spikes required to cause malfunction is faster than the fall time produced by the series 51 modules, and the cross coupled noise within actual systems is usually less than one volt, this problem is not observed when series 51 modules are operating together. However, at each "black box" interface, there is a possibility of noise pick-up. It is expected that this problem will be avoided by normal shielding and grounding.

Appendix B

SPECIFICATIONS FOR THE DESIGN AND DEVELOPMENT OF A FLYABLE ADVANCED TELEMETRY SYSTEM WITH ADAPTIVE CAPABILITY

1.0 Scope

It is the purpose of this specification to define performance requirements for the Data Compression equipment employed in a flyable vehicle borne advanced telemetry system with adaptive capability. Although the overall system includes existing vehicle telemetry equipment, the specification for this existing vehicle equipment is not included herein. Therefore, these specifications are restricted to those requirements to be met by the equipment which provides bandwidth compression, herein referred to as the "Data Compressor". Detailed environmental specifications are not included herein.

2.0 Performance Requirements

2.1 General

The data compressor shall examine the PCM data produced by the vehicle telemetry equipment for redundant properties, and produce an output for transmission which includes only the information necessary for reproducing the data on the ground. These performance requirements shall be met when the equipment is subjected to environments typical of space vehicles. It shall be a design goal for the equipment to meet these performance requirements when tested per test standard 50M60005, issued by NASA-George C. Marshall Space Flight Center.

2.2 Inputs

The data compressor shall operate when the following inputs are provided. Unless otherwise specified, logic and synchronization input levels shall have nominal values of zero volts for "false" and +5 volts for "true". When loaded by the input circuits of a T.I. SN514 gate module or equivalent (approximately 20K shunted by approximately 60 picofarads), the maximum "false" shall be +1.0 volt and the minimum "true" shall be +3.9 volts. Logic input circuits shall not be damaged by any input level of less than +8 volts.

A. System Clock - Both 144 KC and 288 KC system clock rates shall be accommodated by appropriate preflight programming.

B. Master Frame Sync - Correct synchronization shall be maintained provided that the input master frame synchronization pulses are as follows:

1) Frequency - 4 per second (once each multiplexer master frame period).

2) Duration - In excess of 200 microseconds but less than 8 milliseconds.

3) Timing - As specified by Fig. B-1.

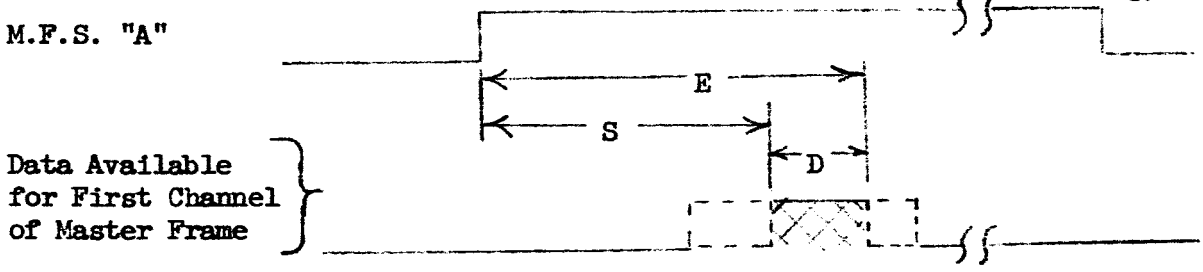
4) Rise Time - Maximum of 2 microseconds to a level of +3.2 volts.

C. Data Sample Magnitude - 10 bits in parallel form.

D. Command (from vehicle command system) - 20 bits in parallel. When loaded by the input circuits of two T.I. SN514 gate modules or equivalent (approximately 10K shunted by approximately 120 picofarads), the command input logic levels shall have a maximum "false" level of +1.0 volt and a minimum "true" level of +3.9 volts. One-bit shall signal that a valid command is available. The remaining 19 bits shall signal operations to be executed within the data compressor. Use of the 19 bits shall be:

1. Channel Address - 13 bits
2. Prediction Tolerance Limits - 3 bits
3. Priority Tag - 1 bit
4. Define Commanded Function - 2 bits

E. Programmed Inhibit - This input shall be +28 ± 4.2 volts, with reference to input power ground, whenever it is desired to inhibit processing of data related to specific time-slot group(s). Maximum current drain on this input shall be 20 milliamperes.

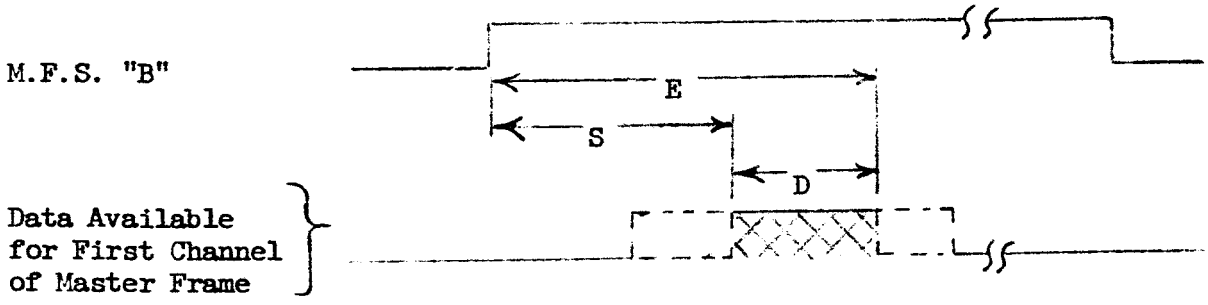


D (Minimum Duration) = 3 system clock periods (≈10.4 μsec)

E (End of Availability) = 40 system clock periods, min. (≈139 μsec)

S (Start of Availability) = 37 system clock periods, max. (≈128.5 μsec)

Part A - Relationship for 288 KC System Clock



D (Minimum Duration) = 3 system clock periods (≈20.8 μsec.)

E (End of Availability) = 20 system clock periods, min. (≈139 μsec.)

S (Start of Availability) = 17 system clock periods, max. (≈118 μsec.)

Part B - Relationship for 144 KC System Clock

Fig. B-1 -- Timing Relationships Between Master Frame Synchronization Pulses and the Availability of First Data Sample of Master Frame

F. Power - Input power shall be 15 watts maximum or 22 watts maximum for system clock rates of 144 KC and 288 KC, respectively, when operating from an unregulated power source of +28 ± 4.2 volts D.C.

2.3 Input Data Rates and Format

The Data Compressor shall process input data of the following rates and format:

A. Commutation Rate - 7200 or 14,400 samples per second corresponding to system clock rate of 144 KC or 288 KC, respectively.

B. Channel Sampling Rates - 4, 12, 40 and 120 samples per second.

C. Commutation Format - Data samples assembled in the time-division multiplex format and rates described here shall be processed by the data compressor.

1. Time-Slots - The data samples will be available for transfer into the data compressor at prescribed time-slots relative to the leading edge of a master frame sync pulse. Each time-slot has a duration of approximately 20 system clock pulses.

2. Main Frames - A main frame consists of a group of either 60 or 120 consecutive time-slots corresponding to system clock rates of 144 KC and 288 KC, respectively. Main frames occur at a rate of 120 per second.

3. Master Frame - A master frame includes a sequence of 30 main frames.

4. Time-slot Groups - The time-slots within a main frame may be considered to be grouped into time-slot groups in a manner such that the channel sampling rate(s) of data contained in each time-slot group is assignable independent of the channel sampling rate(s) assigned to data in all other time-slot groups. Time-slot grouping to accomplish this is defined by:

Group	Time-slot Position
I	(1 + 2N)
II	(2 + 2N)
III	(1 + 4N)
IV	(2 + 4N)
V	(3 + 4N)
VI	(4 + 4N)
VII	Last three of main frame

Where N includes zero and all positive integers through the highest number corresponding to the maximum number of time-slots within a main frame that may contain active data samples. The "time-slot position" referred to here is the position of a time-slot relative to the beginning of a main frame.

Time-slot Groups I, II and VII apply when a system clock rate of 144 KC is used. Time-slot Groups III, IV, V, VI and VII apply when a system clock rate of 288 KC is used. Time-slot Group VII does not contain information to be processed.

5. Combinations of Channel Sampling Rates - Each time-slot within a main frame may contain data of any one of the four sampling rates. However, all data associated with the same time-slot group must all be at 12 and/or 120 SPS rate(s) or all at 4 and/or 40 SPS rate(s).

2.4 Outputs

The data compressor shall provide outputs as follows:

A. Compressed PCM Signal - A compressed PCM output shall be provided. This output shall be in a serial "NRZ-Space" format. The output amplitude shall be a minimum 7.0 volts peak-to-peak with a maximum rise time of 3.0 microseconds (10% to 90% amplitude) when measured across a load consisting of a 200 ohm resistor and a 0.003 microfarad capacitor in parallel. The following information shall be present in the compressed PCM output:

1. PCM Data Word - The PCM data word shall include 10 bits for data sample magnitude and 6 or 7 bits, as required, which defines the time position of the data sample within a multiplexer main frame.

2. PCM Synchronization Code - The PCM synchronization code shall be present in the output once each 66 output word times. The PCM sync code shall be 32 bits long when the system clock is 144 KC and 34 bits long when the system clock is 288 KC.

3. Frame Synchronization Code - A frame sync code shall be present in the output once for each multiplexer main frame. The frame sync shall identify the specific multiplexer main frame within a multiplexer master frame sequence and identify the master frame within a sequence of 16 master frames.

4. Buffer Fullness Word - A PCM word shall be present in the output once every 16 multiplexer master frames which signals the fullness of the buffer memory at the time that the buffer fullness word enters the buffer.

B. PCM Bit Rate - The PCM output bit rate shall be preflight programmable for values given by the expression, Bit Rate = $\frac{\text{System clock rate}}{2\,n}$, where n is programmable for any integer from 3 to 16.

C. Command Acceptance Pulse - A separate pulse output, not associated with the data output, shall be provided within 500 milliseconds after receipt of a valid command which signals the execution of the command within the data compressor. This pulse shall be positive going with amplitude of at least 4 volts. This output shall be capacitively coupled from an emitter-follower stage (minimum output coupling capacitance of 50,000 picofarads). The command acceptance pulse shall have a duration of approximately 15 microseconds.

2.5 Method of New Data Acceptance

A zero-order, floating-aperture prediction criterion shall be employed to determine which data samples represent significant new information. The prediction tolerance limits shall be assigned, via the command input, independently for each data source (multiplexer input). The possible limits, in terms of percent of full scale for samples of 10-bit magnitude, shall be ±0.1% (LSB), ±0.78%, ±1.56%, ±3.13%, ±6.25% and ±12.5%.

2.6 Programmable Control Logic

Control logic shall be provided which can be programmed to control data acceptance as a function of a set of input logic signals.

A. Control Logic Inputs - The following logic signals shall be provided, within the data compressor, as inputs to the control logic:

1. Commanded (via vehicle command system) "force accept".
2. Two signals which indicate two specific combinations of stored prediction tolerance limits.
3. Stored priority tag.
4. Stored "redundant sample" tag.
5. Six inputs, each of which indicates a decoded range of buffer memory fullness.
6. Four inputs, each of which corresponds to a specific channel sampling rate. A "true" condition for each of these inputs indicates the channel sampling rate for the data sample currently being processed by the comparator logic.
7. Four inputs, each of which corresponds to the time-slot group to which the data sample currently being processed belongs.

B. Control Logic Output Functions - In response to the inputs per paragraph 2.6A and to the control logic programming, the following functions shall be accomplished:

1. Permit normal prediction and comparison to control data acceptance.
2. Increase prediction tolerance limits (aperture size) to twice normal value.
3. Increase prediction tolerance limits to four times normal value.
4. Force acceptance of a data sample.
5. Force rejection of a data sample.

C. Examples of Control Logic Programming Capability - A few of the basic programming possibilities are listed here in brief form. This list of examples is not intended to imply specific limits of control logic programming capability.

Examples:

1. An increase in prediction tolerance limits for higher levels of buffer memory fullness may be achieved. The level of fullness at which an increase in limits occurs could be made dependent upon time-slot group, channel sampling rate and/or the stored priority tag. However, data samples from data channels which are assigned prediction tolerance limits of ±0.1% will not be processed with increased limits.

2. Rejection of a data sample at higher levels of buffer fullness. Again, the fullness level at which a specific data sample is rejected could be made dependent upon the time-slot group, channel sampling rate and/or the stored priority tag.

3. Acceptance of a redundant data sample may be achieved when buffer memory fullness is low and the "redundant sample" tag is "true".

D. Fixed Programmed Functions - Certain inputs or combinations of inputs shall always produce a specific control logic output function. These fixed conditions are:

1. When the buffer memory fullness is within the lowest detected fullness range, all data samples processed shall be accepted.

2. When the buffer memory fullness is within the highest detected fullness range, all data samples processed will be rejected, except for those samples which are processed concurrent with a commanded "force accept" input per paragraph 2.6.A.1.

3. One data sample will be accepted from any data channel addressed with "force accept" command.

2.7 Commanded Functions

The data compressor shall be capable of executing the following operations when a valid input command from the vehicle command system is applied.

A. Change stored prediction tolerance limit and priority tag assigned to the addressed data channel.

B. Force acceptance of one sample from the addressed data channel.

2.8 Redundant Sample Provisions

Capability shall be provided to accept redundant data samples to prevent the buffer memory from becoming empty and to transmit confirming samples for near-static data channels. The technique employed shall utilize the difference between available transmitter bandwidth and the bandwidth required for "significant" data samples. The bandwidth available for redundant data samples shall be utilized in a manner such that the maximum time between two consecutive data samples transmitted from each data source is minimized.

2.9 Reference Memory

The reference memory, required to implement the method of new data acceptance per paragraph 2.5, shall have a basic storage capacity of 480 words (each word of storage accommodates one data source). The basic design shall permit construction of this memory, for the purpose of economy, with less than the basic capacity. A means shall be provided to program the reference memory to accommodate input data within the limits of paragraph 2.3.

2.10 Buffer Memory

To permit a constant output rate, a buffer memory shall be provided which stores data samples accepted at an irregular rate and provides outputs as required to maintain a constant system output rate.

A. Storage Capacity - The buffer memory shall have storage capacity of 1,024 words.

B. Fullness Detection - Means shall be provided to continuously detect the state of fullness of the buffer memory. A minimum of 6 fullness levels shall be detected and a logic output (for use internally only - not an output of the Data Compressor) provided for each of these 6 levels. Each of these 6 logic outputs shall have a change in logic level at one and only one level of buffer fullness. (For example, if the fullness is near empty and the logic level is "false", then as the fullness increases towards full, the logic level shall change to "true" at a specified level of fullness and remain "true" until

B. Continued

the fullness is reduced below that specified level of fullness.) The lowest fullness level detected shall be at 4 words. The remaining 5 fullness levels detected shall each be programmable independently in increments of 16 words or less.

2.11 Special Programming Capability

In addition to programming provisions described elsewhere, a capability shall be included to permit inhibiting the processing of data samples corresponding to any specific time-slot group(s). (See paragraph 2.3 for definition of time-slot groups.) The effect of this provision is to permit exclusion from the system output of all data samples corresponding to specific time-slot group(s). The data excluded from the system output shall be determined by preflight programming of the system operations. It shall be possible to exclude data related to specified time-slot group(s) for the entire duration of flight. It shall also be possible to exclude data corresponding to other specified time-slot group(s) by application of the "programmed inhibit" (Paragraph 2.2.E).