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FINAL REPORT

DESIGN GUIDELINES FOR CIRCUITRY IN A NUCLEAR REACTOR-PROPELLED SPACECRAFT

Contract NAS8-11755

by

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FOREWORD

This document is the final report for Guidelines and Design Efforts for Radiation Resistant Circuitry performed for the Astrionics Laboratory of Marshall Space Flight Center, National Aeronautics and Space Administration by the Huntsville Research & Engineering Center of the Lockheed Missiles & Space Company.

The work was performed under Contract NAS8-11755. Technical aid and direction for the Guidelines were provided by Mr. William T. White, Special Projects, Astrionics Laboratory, R-ASTR-BP, MSFC.

Technical aid and direction for the design efforts were provided by Messrs. John M. Caudle and John H. Owens, Jr., of R-ASTR-NFE, Astrionics Laboratory, Marshall Space Flight Center.

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1.0 INTRODUCTION AND SUMMARY

The effort on this contract was divided into two major phases: that concerned with the generation of a circuit designer's guidelines manual for radiation resistant circuitry; and that concerned with the design and analysis of radiation resistant power supplies.

The guidelines manual effort involved a literature search on the theory and measurement of radiation effects; the compilation of data of radiation effects on components; the testing of components for which insufficient data were available; the design, fabrication and irradiation of a 200 watt power supply and a voltage regulator as typical of the type of circuitry most adversely affected by radiation, and the generation of the manual "Design Guidelines for Circuitry in a Nuclear Reactor-Propelled Spacecraft." Because of the size of the manual and the fact that it has already been completed and delivered, it is not included with this report. Mr. William T. White, Special Projects, Astrionics Laboratory, R-ASTR-BP, MSFC, is in charge of the manual and its distribution.

The second phase involved the design and breadboarding of power supplies using the techniques indicated in the manual to minimize the susceptibility to radiation. A novel 400 Hz inverter was built after the initial design proved to be theoretically possible but required transistors with a combination of properties not yet available. A dc to dc converter was also designed. A detailed analysis of switching regulation was made to assist the circuit designer to optimize circuit performance and minimize radiation effects.

1.1 Literature Search

A literature search was initiated to obtain as much information as possible on the effects of the radiation environment on electronic circuitry. To this end letters were sent to selected system manufacturers requesting any non-classified information which could be compiled by LMSC/HREC and included in the Radiation Guidelines Manual. Although circuit information was particularly emphasized, the majority of information which was received contained only component level studies. Some microwave and TIMM circuitry information was received, but this information generally attempted to cover facility capability rather than useful data.

Most of the technical articles uncovered by this literature search which offered circuit design techniques for radiation hardening invariably confined their discussion to compensating the degradation effects of the nuclear environment on semiconductors.

1.2 Testing of "Building Blocks" and Circuits

Several circuits and "building blocks" were breadboarded by HREC and irradiated at the Georgia Nuclear Laboratory Facility in Dawsonville, Georgia. The testing and their results are described in the Guidelines except for two circuits which failed during the radiation testing. One of these circuits involved using a two-transistor equivalency for the silicon controlled switch (see Figure 1.1). The mechanization had been successfully tried as an equivalency for the unijunction transistor, but unfortunately a compensating diode which tracked the base-to-emitter voltage variations in the device was not put into the breadboard tested at Dawsonville. The results were an abrupt failure as this sensitive voltage increased. The other circuit will be discussed under a separate heading entitled: "200 Watt Power Supply."

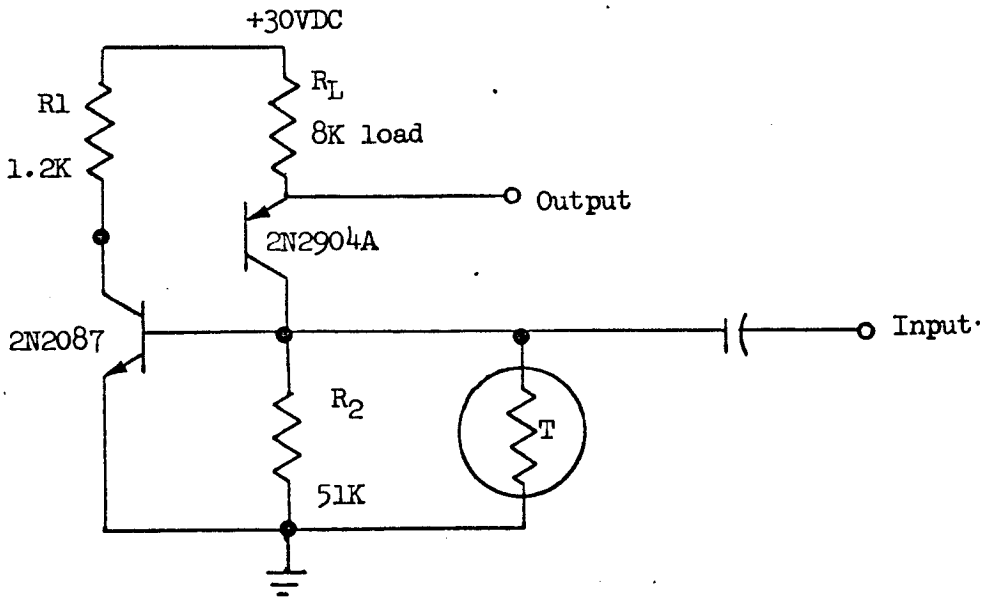

Figure 1.1

1.3 SNAPSHOT Program Conference in Sunnyvale, California

One member of the HREC/LMSC staff visited LMSC's Sunnyvale facility for the purpose of obtaining practical design guidelines from the design engineers working on the SNAPSHOT Program. This trip proved very fruitful in gaining a realistic insight into the radiation environment as viewed through the more experienced eyes of these program members. They were more cognizant of the limitations in measuring the actual radiation environment and had an excellent knowledge of the grey areas surrounding surface effects and actual permanent damage directly attributable to gamma radiation. A rough draft copy of the Guidelines Manual was reviewed by their staff and their helpful comments and criticisms increased the readability and factual content of the manual.

1.4 The Radiation Guidelines Manual

The guidelines manual consists of three sections. The first section consists of general background information in atomic and nuclear physics necessary for interpreting the results and guidelines set forth in the remainder of the text. The second section is divided into two parts. One is the careful inclusion of state-of-the-art limitations in the semiconductor family caused by the radiation environment. The reader is then invited to examine in detail some of the reasons behind the limitations and methods by which they can be circumvented. The second part of this section discusses other materials and electronic components which would be subjected to the same environment. As would be anticipated, the inescapable conclusion is that the semiconductor is the weak link in any electrical circuit subject to nuclear radiation.

The final section consists of a compendium of design guidelines and detailed derivations and formulae which are useful for designing radiation-tolerant equipment. Also included are circuits tested and qualified for the environment including actual performance curves. An appendix is included which covers the derivation of some design equations and a glossary of useful radiation terms.

1.5 The 200 Watt Power Supply

A 200 watt power supply was built for irradiation utilizing a switching/summing waveform technique (see Figure 1.2). The breadboard version was first tested at HREC/LMSC and the results indicated that satisfactory performance might be achieved if the power transistors used could continue to provide a useful gain. However, upon receipt at GNL in Dawsonville, the circuit failed to meet specifications initially, and also failed catastrophically early in the test program. Since HREC was not informed of the faulty circuit until after the testing, no attempt was made to remedy the circuit or improve the performance. This perhaps points up the need to have the design engineer available at the test site to help avert this lack of communication.

Performance data for the 200 watt Vdc power supply is as follows:

Chopper Frequency	1.6 kc
Regulation*	± 0.5% at 20% to 120% full load (see Figure 1.3)
Efficiency	83.5% at 20% full load 90% at full load
Ripple	2.0% full voltage

*No regulation under low supply voltage (24 Vdc); see text.

Figure 1.3 represents the regulation of the 200 watt power supply as given by a developmental breadboard utilizing two 2N3232 transistors in parallel rather than the 2N2125 transistors originally called out in the circuit diagram. Figure 1.2 represents the 200 watt power supply.

The output voltage did not hold up under low supply voltage (24 Vdc); however, this may be corrected by adding some turns to the secondary of the output transformer. Some rise in the output voltage under light load conditions will also occur, but this is not expected to interfere with good regulation in the 30% to 120% full load area.

1.6 Regulator Operation

The voltage applied to driver B is 180° out of phase with that applied to driver A. With no current in the bias or feedback windings, there is no delay of the applied signal through the mag-amp and therefore the output of driver B is 180° out of phase with respect to driver A. The resultant sum, which is applied to the power amplifier, is zero. As bias current is applied, the mag-amp comes out of saturation, with the resulting conditions causing the applied wave to be delayed before triggering driver B's transistors. The outputs of A & B now start to come into phase with each other, resulting in a signal to be applied to the power amplifier. At 1.6 kc, a full cycle is 625μs long. Therefore, when enough current is applied to the bias winding, the mag-amp can delay the applied signal 312.5μs (equal to 180°) resulting in full matching of drivers A & B, and full output power.

The feedback winding and sensor are arranged to force the mag-amp back into saturation and thus reduce the output power. The common base amplifier in the sensor plus the choice of operating point and load resistor (2K) provide enough gain to establish a 0.5% regulation between 20% and 120% full load.

The mag-amp is capable of delaying the applied signal longer than 312.5μs. When this happens, the power supply becomes unstable. In some cases using the sensor shown in the Sixth Monthly Progress Report, the output voltage stabilized around 30 Vdc. This condition occurred most often under heavy load

starting tests. To correct this instability, the diode-capacitor gates to the bases of driver B's transistors were added. These ensure that the output of B will never be delayed beyond maximum (in phase) matching with driver A.

With the present circuit, the bias is adjusted to provide enough delay and resulting output power to supply 120% full load. The feedback winding then regulates the output voltage for lighter loads.

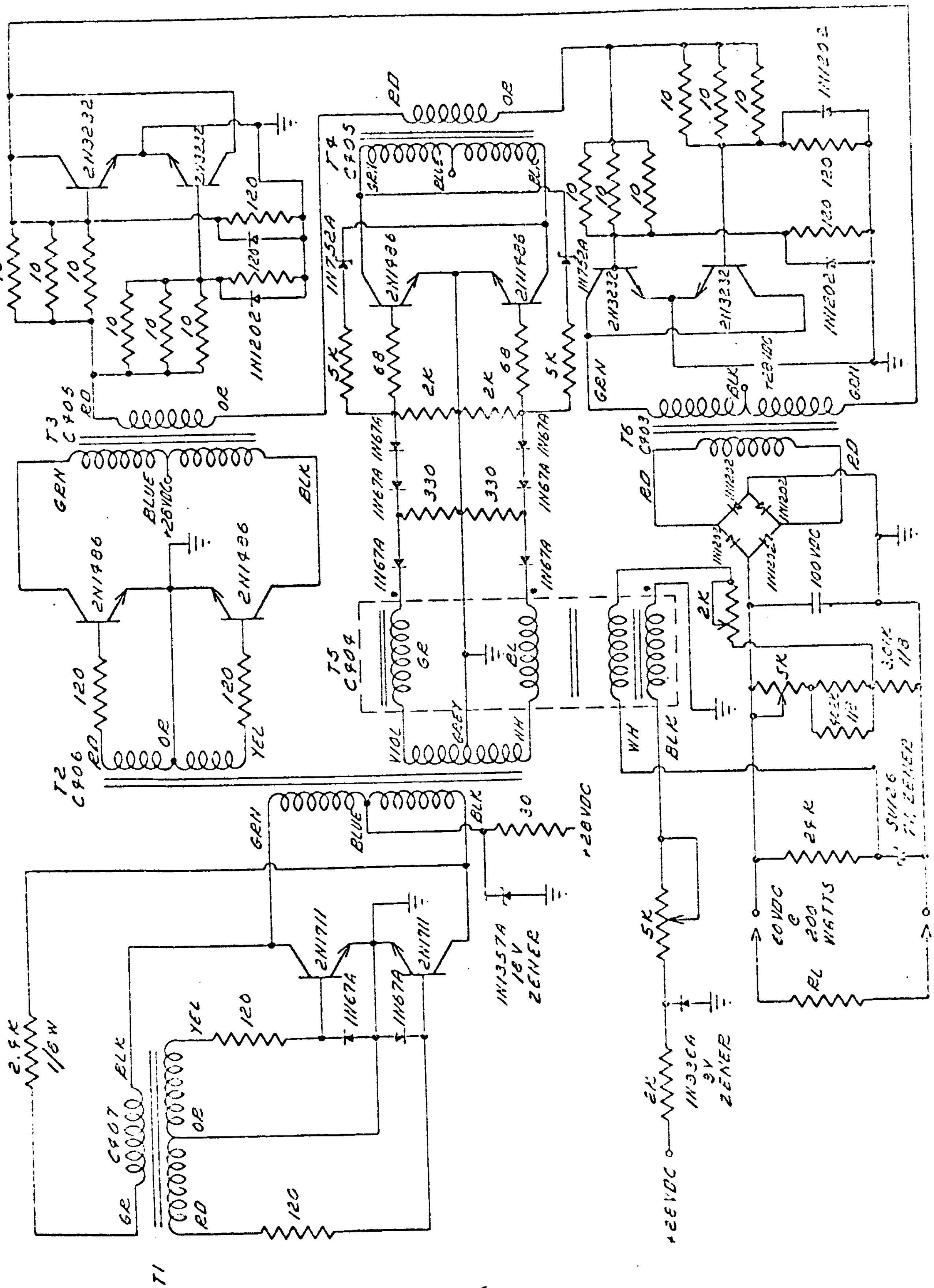
2N3232
2N1486
2N1711
1N1202
1N752A
1N67A
T1 C407
T2 C406
T3 C405
T4 C405
T5 C404
T6 C403
+28VDC
1N1357A 18V ZENER
60VDC @ 200 WATTS
RL
100VDC

FIGURE 1.2

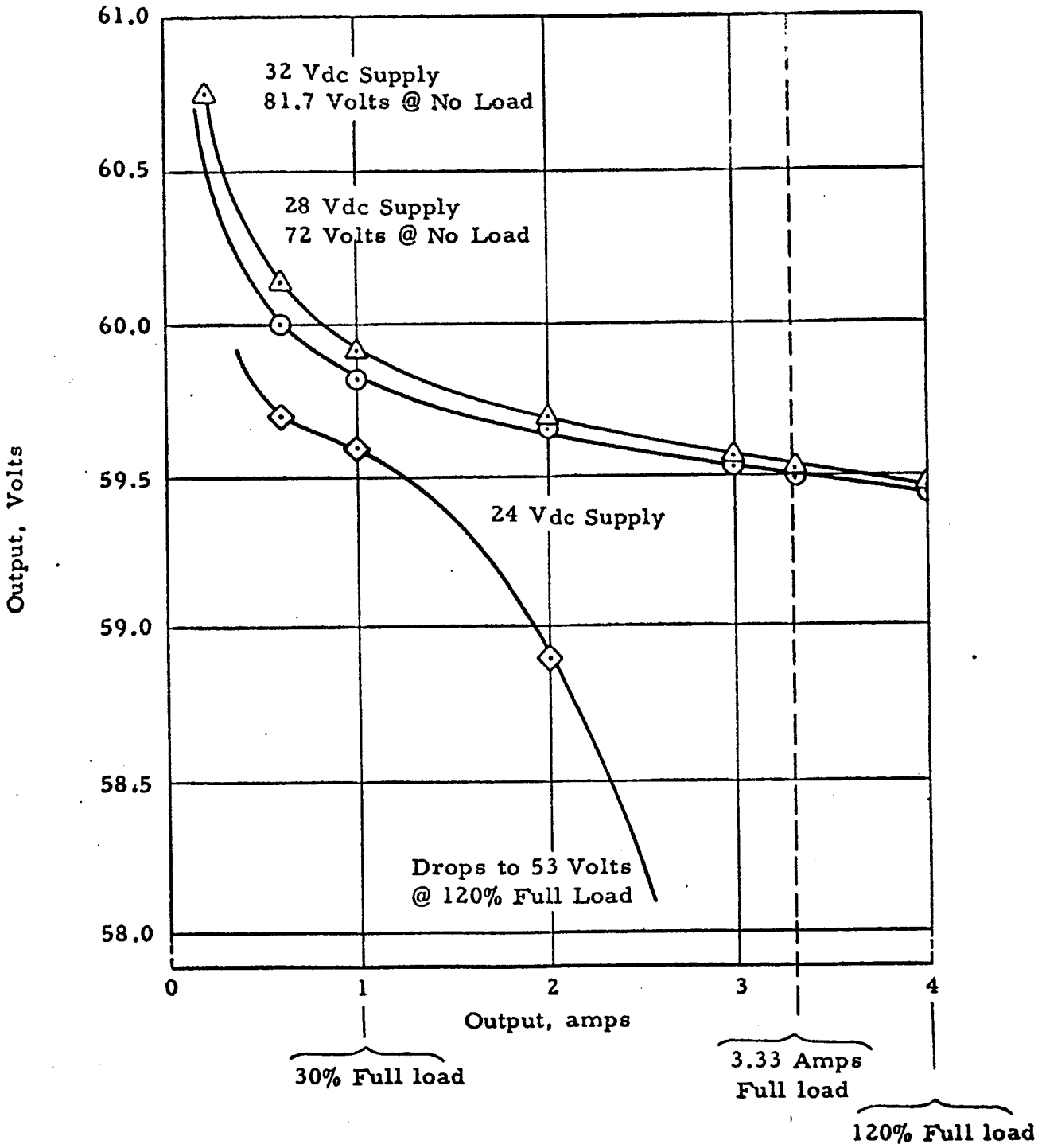

Figure 1.3 - 200 Watt, 60 Vdc, Power Supply Regulation Curve

2.0 GUIDELINES MANUAL

The "Design Guidelines for Circuitry in A Nuclear Reactor-Propelled Spacecraft" manual is the principal product of Phase I of this contract. It is intended to assist circuit designers to understand the nature of nuclear radiation, its effects on components and circuitry and the ways in which these effects can be avoided or minimized.

The manual has been delivered previously and is under the control of Mr. William T. White of the Astrionics Laboratory, MSFC.

3.0 PHASE I: CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE EFFORT IN RADIATION EFFECTS

The level of design quality for space applications has increased steadily. As a means of reducing cost, there is an increasing demand for off-the-shelf hardware as functional building blocks. State-of-the-art improvements which continuously evolve are incorporated into programs only when they can demonstrate a significant improvement with their use. However, future planning must reflect adaptability to the anticipated improvements which will appreciably alter the scope of many present programs.

It is becoming apparent in the rapidly evolving semiconductor field that those products which are now used in off-the-shelf hardware must be compatible with anticipated improvements in future space programs. The alternatives range from complete redesign of the sub-system in question to simple replacement of undesirable devices with compatible higher performance substitutes.

Many future space programs, as well as present ones, plan to subject electronic circuitry to a new environment which severely degrades semiconductor performance...the nuclear radiation environment. Much has been written on circuit design for survival in this environment, but unfortunately, there are too many disjointed, parallel efforts attempting to qualify and demonstrate component and circuit effects in many different nuclear radiation environments.

If an equivalency can be demonstrated and statistically correlated to show that the radiation tolerance of semiconductors depends upon device geometry and manufacturing processes, then the first step in unifying the multitude of test programs, either planned or in progress, would be accomplished. Further, if this equivalency can be used to predict device performance in one radiation environment by subjecting the device to another radiation environment, less expensive and readily available, then it becomes feasible to specify and design all systems to be "radiation-rated". This major increase in mission flexibility can be obtained at an insignificant increase in time and money costs.

The semiconductor device is the most seriously affected component of the electronic circuit performing in the nuclear radiation environment (see Reference 2). The very properties of the semiconductor which achieve its desired electrical response are, unfortunately, the most volatile when subjected to any external energy source. Since heat, light, and electrical fields bias and restrict semiconductor performance, it is not surprising that radiation fields having a high energy content can cause "unpredictable" and "unnatural" property changes in the device.

3.1 The Damaging Effects of Radiation on Semiconductors

Only two major effects actually impart significant performance changes to semiconductor circuits in the radiation environment. These are ionizing effect induced by the electrical charge content of the radiation flux, and the displacement effect damage produced by the "brute force" high energy impact of the radiation particle with the target material's lattice structure. The ionizing effect will cause build up, storage, or transfer of electrical charge in a semiconductor device which can be minimized by careful circuit design or removed once the energy source has been removed. In this event, the circuit can again perform at desired specifications. The displacement effect, on the other hand, causes an irreversible change in the physical properties of the materials, which will usually cause serious degradation of transistor action, increased leakage across reversed-biased junctions, and decreased conductivity in each doped substrate (see Reference 2).

3.2 Selecting Radiation-Tolerant Semiconductors

The selection of a semiconductor device for optimum performance in the radiation environment first involves careful selection of the device geometry and power requirements necessary to satisfy the system's performance requirements without compromising the necessary device capabilities. Quite often, the applications engineer will require high power, as well as low power, high frequency operation as well as audio and dc operation, and high voltage as well as low voltage capability in a system. He will quite naturally specify semiconductor devices which are rated by the manufacturer for these applications. He considers doing otherwise to be inefficient and an annoying inconvenience. On the contrary, it is important to make the applications engineer realize how different is the semiconductor's performance in a radiation environment. Thus, when transistor selection is required, any manufacturing technique which reduces the active geometry or increases the impurity doping concentration or optimizes the base-to-emitter perimeter ratio is worthy of consideration, even if it is less efficient from a purely circuit point of view (see References 3 and 6).

3.3 Limitations of Commercially Available Semiconductors

Unfortunately, the manufacturing processes spelled out by these requirements do not reliably restrict system failure due to semiconductor degradation. The fact remains that the semiconductor registration system currently employed completely ignores radiation tolerances. Therefore, transistor parameter design can be accomplished by various manufacturers under widely differing processes all meeting the registered design centers and tolerances. Radiation-induced damage thresholds on the other hand can be several orders of magnitude apart. To further complicate the picture each manufacturer states quite openly on every transistor specification sheet that he reserves the right to "improve" his product at any time without notice. Since his only restraints are the "registered" parameter design centers and their tolerance, he is free to meet these requirements with any

process which suits fancy and up-date or change the process whenever economy or change in the state-of-the-art dictates. For example, he can change the chemical composition of the epoxy seal or use different annodizing or protective coating processes. He can use large junction connections of one base metal or smaller junctions of another. He may fill the case with inert gas or plain air, or sometimes, when conditions demand, he will evacuate it. Many of these "beneficial improvements" reduce the radiation tolerance of the devices.

It therefore becomes necessary for the user to examine and select his semiconductor device on a lot-by-lot basis. He can intelligently select a device class based upon manufacturing process, power requirements, and device geometry, but he must insure that the minor construction techniques do not produce harmful side effects under radiation. From past performance of semiconductor manufacturers, he can expect that uniformly frozen manufacturing processes will be the exception rather than the rule over a long period of time so that he must expect to have to requalify his semiconductor selection lot-to-lot (see Reference 2).

3.4 The Selective Sampling Procedure

Numerous methods can be used to select a transistor from a given lot to insure that it can be reliably used for a given radiation environment. In the limit, every electrical parameter variation caused by incident high energy radiation flux can be used as a sensor for monitoring this induced damage. As the radiation flux is allowed to accumulate with time, the damage or degradation rate of the electrical parameters (h_{fe}, h_{ie}, I_{cbo}, etc.) increases. As the total integrated flux exposure on the target area increases, this changing rate may tend to level off or not, depending upon the nature of the devices under test. However, one point is assured: that increasing the total integrated flux exposure always decreases the effective transistor action.

Methods of Selection: The various rates at which the individual transistors degrade, if sensed early enough, can be used as a selection technique for identifying the more tolerant devices. Variations in the most sensitive parameter of transistor action, current gain, would be the easiest to instrument and measure (see References 1 and 2).

There is also the possibility that the devices can be irradiated through their maximum anticipated radiation environment; the most tolerant devices selected and then under carefully controlled temperature annealed to a condition approaching their pre-irradiated state. It has yet to be demonstrated that significant post-irradiation correlation will occur with previously irradiated properties. NASA/MSFC attempted to show this correlation with a number of silicon power transistors (2N2125) without success (see Reference 7).

Some evidence exists that the leakage current of a transistor group sample can be monitored and the device, which has the highest leakage levels or which exhibits the greatest leakage change during radiation, can be rejected

as a poor choice for radiation tolerance. However, because of the high impedances and extremely low-level leakage currents involved in silicon devices and the necessarily long test lines which couple the circuit in the radiation environment to the external test equipment, it is doubtful that consistently accurate data points can be recorded (Reference 1).

Since the diffusion process allows the doping density of the substrates involved to be large over the major portion of the active area, manufacturing processes involving diffusion and grading techniques should improve the transistor's tolerance to radiation. Planar and planar epitaxial processes usually employ diffusion techniques for forming at least the base and emitter and, in the latter case, all three junction areas. Since the masking, etching, and timing of the diffusion growth can be accurately controlled and reproduced, the electrical parameter variations between transistors (especially in the same lot) can be held much closer than the older techniques such as the alloy junction devices. Because of this close correlation of the physical size and geometry relationships in each transistor of the lot, more nearly uniform radiation damage from device-to-device can be anticipated as well. Thus, when a flux intensity is uniformly incident upon an entire target sample with the precise geometry and size set by the above manufacturing processes, the result should produce a reasonably uniform degradation of the entire lot (Reference 3).

Application Requirements in the Selection Process: The applications engineer must have in mind the desired response which the device will be asked to generate before he can specify and interpret a selection process. For example, a transistor for use in a high gain operational amplifier with feedback would be selected primarily for high gain. On the other hand, an open-ended amplifier would require a transistor whose gain variation was minimized over the radiation environment range. Thus, a transistor with a pre-irradiated h_{fe} of 100 and a post irradiation h_{fe} of 30 would be a better choice for the operational amplifier than one which has a pre-irradiated h_{fe} of 20 and a post-irradiated h_{fe} gain of 12. The latter, however, would be better suited for the open-ended amplifier (Reference 2).

When switching applications are desired, the designer must be aware of the current ranges being switched so that the optimum emitter-periphery ratio commensurate with device rating can be selected. For example, a transistor switching 0.2 to 1 ampere would probably be selected from a device capable of 5 amperes maximum collector current (Reference 2).

Program for Statistically Correlating Sample Sets: Before discussing the statistical program, the pertinent terms need defining and a typical selection program for a high frequency transistor class is used as an illustration of these terms:

- Samples: The significant number of devices necessary to insure that an accurate population of devices' parameter changes can be correlated.

- Sample Set: The samples in one class of device selected from one manufacturer's lot.

- Class: A particular type of semiconductor with closely correlated physical size and uniform material composition per set.

To illustrate this procedure, assume that a 2N708 high frequency, switching-type transistor manufactured by planar techniques is selected as one class of device for testing. It is calculated that the sample number necessary to provide accurate population sampling to a 90% confidence limit is 30. Therefore, for each environmental test proposed, a manufacturer's lot will provide one sample set per test. Since four radiation environments are projected, each manufacturer must provide four sample sets or a total of 120 devices purchased from each manufacturer's lot. Thus, for example, Transitron, General Electric, and Fairchild may be selected to provide the 2N708 transistors for the testing, and each would provide four sample sets of thirty for a total class sampling number of 360 devices.

The testing program is defined explicitly in the following outline:

- Three sample sets in each class will be exposed to three separate radiation environments. One sensitive electrical parameter will be monitored before, during, and after their radiation. The integrated exposure flux of each environment will exceed:

  1. for neutron flux: 10^{13} n/cm^2 (E $\approx$ 3.2 Mev)
  2. for electron flux: 10^{16} e/cm^2 (E $\approx$ 1.5 Mev)
  3. for gamma flux: until the class is destroyed

- There will therefore be nine sample sets exposed to each independent radiation environment:

Radiation Environment	Class I	Class II	Class III
Neutron	A_1, B_1, C_1	D_1, E_1, F_1	G_1, H_1, J_1
Electron	A_2, B_2, C_2	D_2, E_2, F_2	G_2, H_2, J_2
Gamma	A_3, B_3, C_3	D_3, E_3, F_3	G_3, H_3, J_3

where letter designates specific manufacturer's lot and number subscript identifies one sample set.

- Using the data from each sample set, curves of the electrical parameter degradation versus integrated radiation exposure flux will be plotted on a semi-log basis. Damage correlation between gamma, neutron and electron flux will be achieved by first fitting together the three curves corresponding to a manufactured lot. This will be accomplished by varying the logarithmic scales of two of the sample set curves. Then the equivalency should be verified by cross-checking the equivalencies determined from the other two fitted curves in the class.

- The same procedure will be used to establish the equivalency factors for the other two classes.

3.5 The Case for Radiation Equivalency

There has been effort in the past attempting to correlate electron-to-proton-to-neutron equivalency at various energy thresholds (usually 1 Mev or above). These studies have shown, for example, that one proton at 10 Mev will do as much damage as 4.2 neutrons from an unshielded reactor which does as much damage as 70 electrons at 10 Mev on a particular target material (References 4 and 5). This equivalency holds only for a particular type material (silicon solar cell) and cannot be expected to convert for other materials. However, it is entirely plausible that particular classes of semiconductors (high frequency, switching type transistor for example) can also be degraded by various radiation sources and a damage equivalency established. Of course, the semiconductor's primary permanent damage mechanization results from the displacement effect. This is directly attributable to high energy particle bombardment of the semiconductor substrate. It is the energy content of the particle which imparts the Frenkel Defect upon the lattice structure and alters the substrates physical and electrical properties.

Consider the following analogy. A child's wagon rolling down a steep hill will have little effect upon a brick wall at the bottom. On the other hand, a diesel locomotive would only slow slightly upon impact with the same wall. The same disruptive result will occur to the wall if struck by a large truck, a cannon ball, or even a hurricane. Except for the wagon, all of these devices had one property in common; each device contained high energy. The wall's physical configuration was as surely changed by each high energy impact. Since the energy content of the radiation flux is the primary, permanently-damaging mechanism and ionization, secondary emission, and radioactive decay can be classified at best as second order effects, it is reasonable to assume that permanent damage to a semiconductor will result regardless of the carrier used. Thus the semiconductor itself can be used as the sensor to "estimate" the degree of damage imparted from any given radiation flux environment. Therefore, if a class of semiconductors is selected whose physical properties are very uniform through the samples (as should result for planar devices for example), they can be irradiated under different radiation fields to an equivalent electrical parameter degradation with the integrated flux exposures of each flux field recorded.

Then for this class of device an equivalent damage correspondence can readily be formulated empirically. Once established for this semiconductor class, then only one flux field need be utilized thereafter to qualify the devices for each type environment (proton-electron for example).

Evidence exists that the electrical parameters of silicon transistors are degraded considerably in high energy, pure gamma flux fields. Both LMSC in qualifying semiconductors for their SNAPSHOT Program and the Astrionics Laboratory of NASA/MSFC for a similar semiconductor qualifying program encountered this effect (References 1 and 7). Because of the definite economic advantage as well as the testing flexibility from the numerous gamma sources available, an equivalency correlation between gamma-radiation-induced semiconductor damage and electron, proton, and neutron-induced damage will be highly attractive (see Figures 3.1 and 3.2).

Once the equivalency is established, the low cost selection technique can provide semiconductor devices for most radiations where duration of exposure and high energy fields limit the choice of semiconductors to the screened, radiation-tolerant type. Thus, job lots of commercially available semiconductors can be qualified by the manufacturer for use in most missions, including long duration space probes, nuclear-propelled boosters, Van Allen Belt and other space located radiation belts, and perhaps nuclear detonations.

3.6 Establishing the Variance of Device Parameters for Transistors

Present day manufacturing processes offer excellent control stability over the basic device geometry and most of the doping impurity densities. The planar process, for example, offers precise masking and etching techniques with carefully-timed, gaseous diffusion building at least the base and emitter substrates. However, if the current gain of each device in a lot is measured, a relatively large spread is observed. With the geometry tolerances held as tightly as they are, the major contributing factor lies in the degree of doping provided each base substrate. The base thickness is orders-of-magnitude less than that of either the collector or emitter. Since the doping is controlled by timing the gaseous diffusion of impurity atoms, this timing requires much higher precision for forming the base region than for the emitter. Therefore, a small variation in this timing will strongly affect the base area doping concentration.

One of the basic rules in transistor physics states that the degree of transistor action is controlled by the relative differences in dopant density between the base and the emitter. Therefore, the first order reason for observing the current gain variation in a large sample is due to the relative fluctuations of the base dopant density.

Displacement-effect damage, if imposed upon the same class material, will tend to impart equal damage. However, based upon the above discussion the higher gain devices in a lot will have fewer impurity atoms present in their base region than their lower gain counter-parts. Therefore, there will be a tendency for these higher gain devices to "lose" relatively more impurity

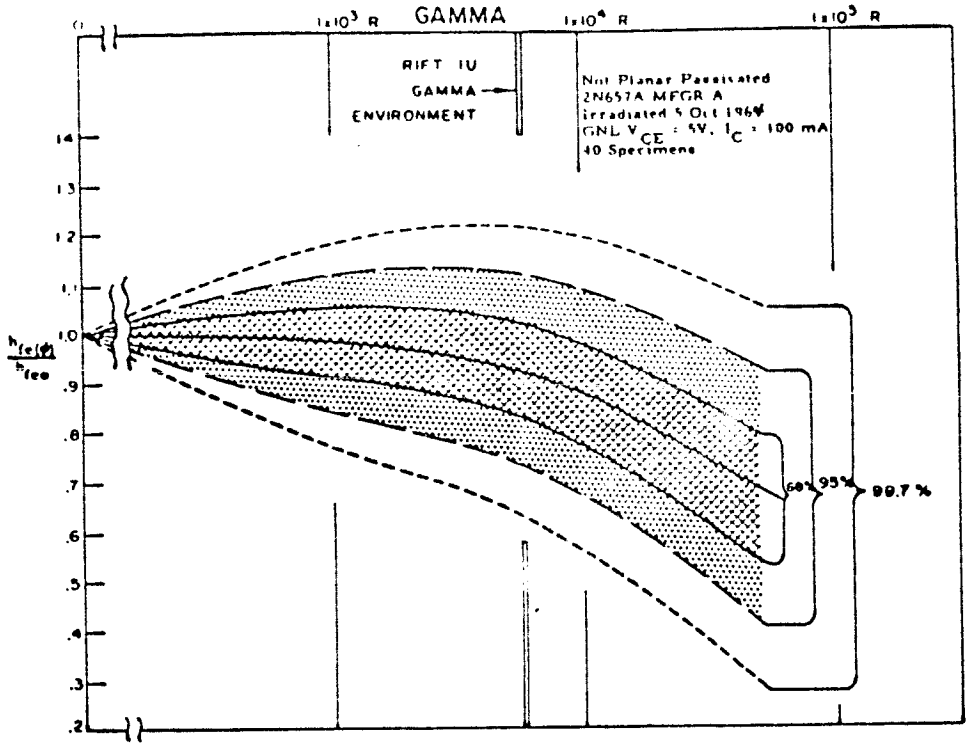

Figure 3.1 - GAIN DEGRADATION OF A NON-PLANAR PASSIVATED 2N657A TRANSISTOR DUE TO GAMMA EXPOSURE

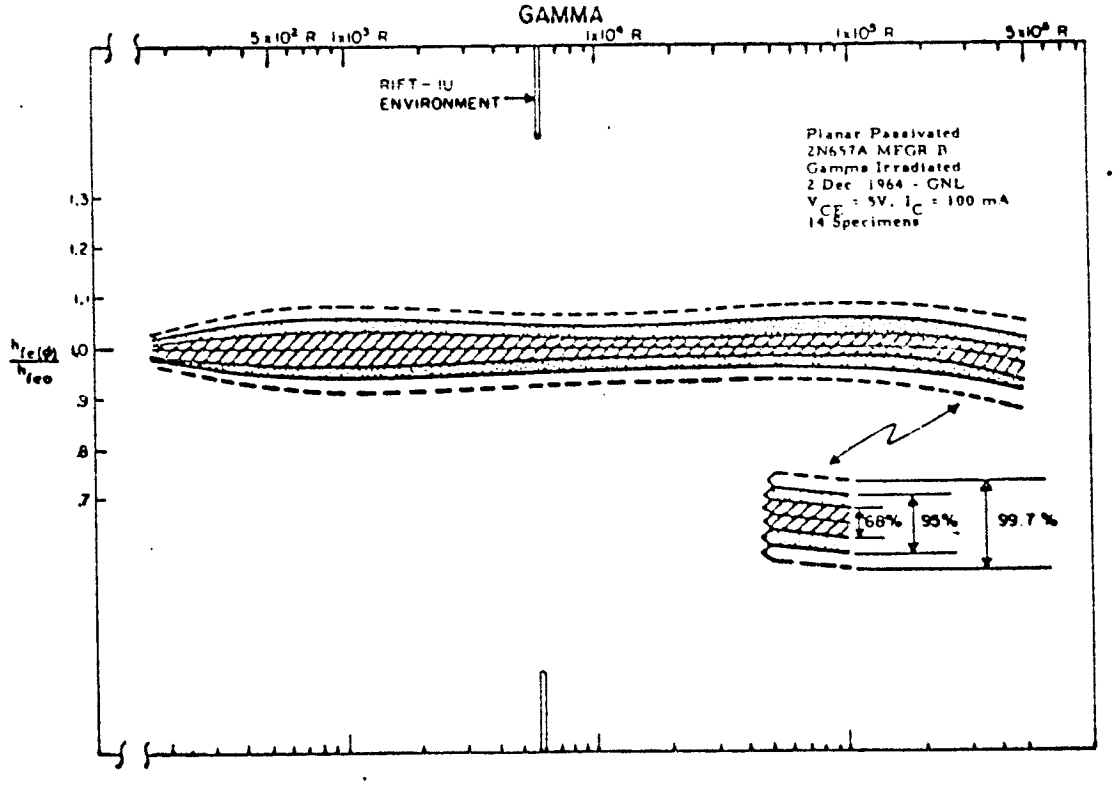

Figure 3.2 - GAIN DEGRADATION OF A PLANAR PASSIVATED 2N657A TRANSISTOR DUE TO GAMMA EXPOSURE

carriers per Frenkel Defect than the higher-doped base, lower gain devices which have a physically larger number of impurity carriers to lose.

The trend for damage change as a function of current gain was observed at the Lockheed Georgia Nuclear Laboratory where small samples of transistors were irradiated (Reference 8). It was noted that in choosing an arbitrary failure point of 50% gain degradation, many of the devices with high gain failed first, the lowest gain devices failing last. Of course, only a small number of devices (10 to 20) were tested and no significant analyses were attempted. However, many of the semiconductor testing results repeat this observation while at other times this correlation cannot be shown. It is anticipated that manufacturing defects, which can significantly alter the device electrical performance under radiation, will be observed as "unpredictable" and "unexpected" variations in a small number of lot samples which must be disqualified.

Fortunately, the manufacturer can provide a much tighter correlation of his devices at a small increase in cost. Since yields in his transistors tend to fall into selective distributions (i.e., 5000 devices in a lot of 12,000 may fall into a narrow gain strata between 55-65 h_{fe}), the manufacturer can easily select transistors lying in this high yield range. A sample distribution of these devices will inherently have a small variance and easily estimated mean. Thus, not only can this distribution be readily provided, but any statistical sampling method will necessitate fewer samples to provide equal confidence limits than a more random selection from the entire lot's sample distribution uniformly since not only are the geometry parameter tolerances small, but the doping concentrations in the base regions are similar as well. The damage or degradation changes versus total integrated flux of any high energy radiation can be correlated with confidence due to the controlled uniformity of the sampled detectors. The damage equivalency between different radiation fields can then be correlated for the particular semiconductor class.

After verifying the damage equivalency for a class at a particular current gain range, the manufacturer will be required to select a significant sample number from a lot in the low and high current gain ranges. To reduce the cost of testing, these devices will be irradiated and measured at the same time as the high yield range of devices. With this information a family of curves can be drawn so that expected current gain degradation as a function of integrated flux is shown with current gain as a parameter.

By qualifying several manufacturer's transistors of the same class and by substantiating that the equivalency can then be established for a class rather than for a particular manufacturer, this significant performance history can be used to continue qualifying and rejecting transistor lots and individual samples in the same class. Thus, the device may be qualified with only the relatively inexpensive gamma radiation.

3.7 Integrated Circuit Considerations

The integrated circuit (IC) is a relatively new device which is rapidly coming into widespread usage because of the great system flexibility it permits without compromising system reliability. As herein used, the term integrated circuit is understood to mean a monolithic, silicon, planar-epitaxial, digital circuit in either a flat-pak or TO-5 metal can. Analog integrated circuits have recently become available, but the number is still small and the availability so uncertain that it is questionable whether to include them at this time. However, the techniques described can be employed for integrated analog circuits if desired.

The first consideration is to limit the selection to the five major suppliers: Texas Instruments, Fairchild, Westinghouse, Motorola, and Siliconix, since only these companies are firmly committed to continued IC production, the others being still in the pilot-run stage and subject to abrupt withdrawal from the market. These five companies share 90% of the IC market and thus are more apt to have consistent production runs, extensive quality assurance programs, etc. Thus, the results of the recommended program are more likely to be applicable in the years immediately following.

The second consideration is the type of integrated circuit to be tested. It is recommended that a single-gate, DTL NAND/NOR be the circuit used for testing. This choice is predicated on several basic facts. A single-gate chip is somewhat less expensive and much less work to test, record, and analyze. Since multiple gates will consist of the same geometry as on the first gate, much less variation will be encountered than among the same number of gates on separate chips. Thus, a given amount of testing effort will produce more useful data if separate chips are used.

The diode transistor logic (DTL) is preferred over other types of logic for reasons of inherent tolerance of performance degradation and widespread availability. SUHL or Sylvania Universal High Level logic is a multiple-emitter configuration available essentially only from Sylvania. This lack of widespread availability severely limits its usefulness in a selective sampling program.

Emitter-coupled logic (ECL) such as Motorola produces is very high speed but achieves this speed by means of a very small signal swing. To operate over a temperature range, a temperature-sensitive threshold voltage supply must be incorporated. Thus, very little additional variation can be tolerated by the system. It is to be anticipated that this will be the logic system most susceptible to radiation damage.

The resistor-transistor logic (RTL) as employed by Fairchild Micrologic (and a similar form produced by Siliconix) is in reality an analog summing of resistor currents to bias a transistor base above or below its cutoff voltage. The resistors are formed from doped areas of the substrate and are difficult to control accurately. This, plus the inherent analog nature of the system, limits the normal fan-out to three. Any appreciable radiation-induced degradation would render the system completely unusable.

Thus the field is for all practical purposes limited to the most widespread and reliable logic of all, diode transistor logic (DTL). In this form, the logic is performed by diodes with the transistors providing power gain and signal inversion. This type of logic uses large signal swings, a current steering type of circuit and transistor overdrive. It is characterized by large fan-out and high noise rejection and thus inherently possesses a large performance degradation tolerance.

Figure 3.3 shows basic NAND gate. The input resistor, R, provides a relatively constant current which is either shunted to ground via one or more of the input diodes and the transistor of the driving circuit or is shunted into the base of transistor Q_1.

The IC equivalent of current gain is fan-out, inasmuch as the base drive is fixed. By selecting a NAND without an internal connection to the collector resistor, the total collector current is available for measurement via an external load. H_{fe} is defined as $h_{FE(sat)}$ in terms of the maximum output current which can be supplied to an external load without causing the collector-to-emitter voltage to exceed the maximum allowable saturated voltage. Except for this minor difference, the previous remarks about current gain apply to integrated circuits. Since integrated circuits are by nature small-geometry, high-speed transistors and diodes, they might be thought to be inherently radiation tolerant. However, it is not quite that simple. In addition to the logic diodes and the transistor, there are also biasing diodes and the gate resistor, each of which is affected by radiation. Thus, circuit failure is not so much a question of the transistor itself as the associated elements. Unfortunately, the diode forward voltage and the resistor both tend to increase with radiation. Both effects decrease the current available to the transistor base and thus aggravate the decreasing current gain of the transistor. Since various manufacturers use different resistor values, current levels, doping levels, etc., it cannot be predicted what the radiation resistance of a manufactured device will be until actual tests are conducted. However, it is certainly advisable to select devices capable of high fan-out and to derate this parameter considerably.

3.8 Other Advantages

Rejection of Ionization-Sensitive Devices: The gamma radiation testing program can be used to reject devices which are highly sensitive to ionizing radiation. When sample sets are exposed to shorter time durations of gamma-radiation some, or many, of the individual samples, depending upon the manufacturing techniques, will diverge rapidly from the expected class degradation curve. The precise reason for this divergence is unimportant so long as manufacturing processes are available which allow highly reliable qualification. The divergent samples are rejected as unreliable and poor risks. This method should reject many individual devices which have flaws and weaknesses which are uncovered by the punishing radiation environment. Some of these rejects will be the occasional, unexplained failure which survives the current testing methods.

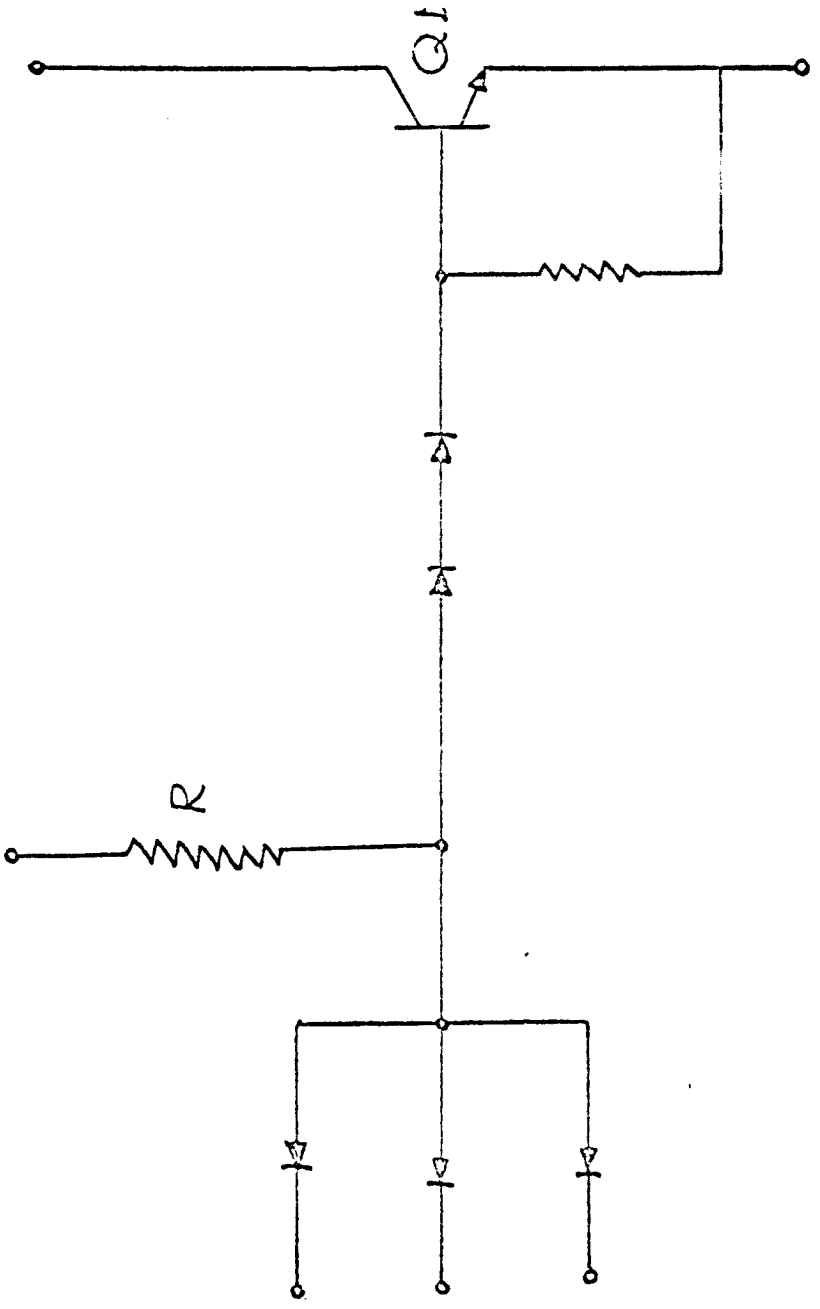

Figure 3.3 - NAND/NOR Gate

Therefore, the same class degradation curve initially qualified for radiation-equivalency correlation can be used for detecting, to a high confidence limit, devices of this class which will not only survive the radiation exposure but also select those devices whose electrical parameters can be depended upon to remain stable. This is a currently anticipated problem which will exist at the gamma flux levels encountered by the instrument unit of a spacecraft using a nuclear propelled booster.

Early Detection of Unreliable Devices: Individual samples can be rejected (when conditions demand 100% testing to assure very high confidence levels for survival) if the class damage curves are scaled with confidence levels as a parameter. Then, any particular device which falls below a minimum threshold level at a fixed lower radiation exposure will be disqualified. The integrated flux exposure will be chosen to allow significant data points but still allow a usable range of qualified radiation tolerance. The threshold will be determined from the class qualification data.

Supply of Post-Irradiated Devices for Worst Case Design: Another by-product of this testing under gamma radiation will also provide the applications engineer with irradiated transistors for proving out circuit performance. The circuits can be designed for operation before and after the total radiation exposure and the results verified by interchanging each pre-irradiated or screened device with its post-irradiated counterpart. This method will further enhance the chances of success for that circuit during the mission.

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4.0 PHASE II: DESIGN OF RADIATION TOLERANT POWER SUPPLIES

4.1 400 Hz Inverter Development

Figure 4.1 presents an amplitude modulation system similar to the existing mechanization except the voltage reference in the switching regulator is a.c. This combines the voltage regulation and power amplification functions into a single switching circuit and results in a synthesized sinusoidal output waveform. The technique has much merit but these design problems are apparent:

1. The filter on the switch output must accommodate a large dynamic swing.

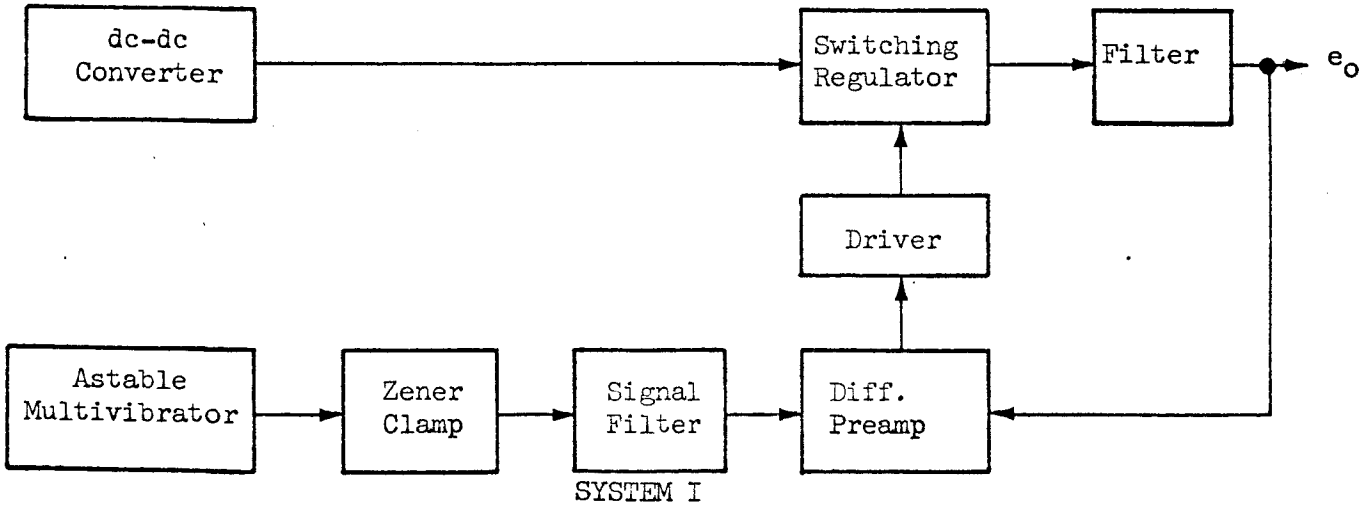
2. An additional circuit is required to establish the initial magnetization conditions on the core.

3. Proper circuit operation requires a minimum load.

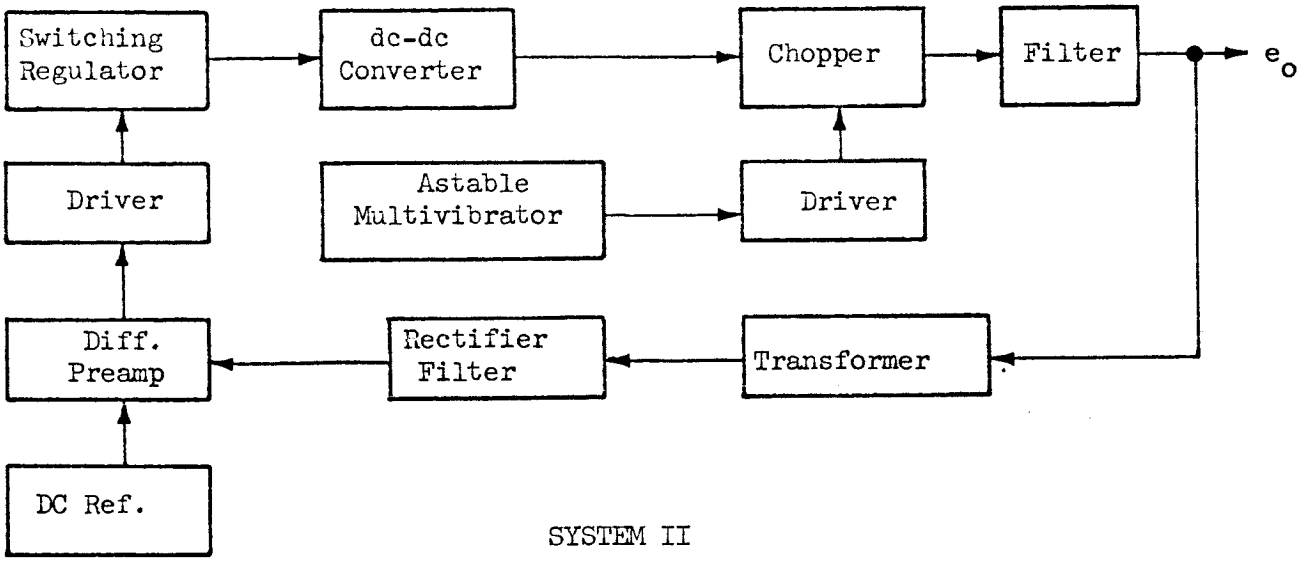
Again a size reduction may be accomplished by the addition of a dc to dc converter on the input. This would eliminate the latter two problems.

It was suggested that the amplitude modulation system with an integral dc to dc converter be used for the final design. This configuration combines design simplicity, high frequency conversion, and efficient operation.

Briefly, the proposed inverter mechanizations to be studied were:



SYSTEM I



SYSTEM II

Each of these uses a high-frequency converter to reduce transformer size as well as a switching regulator for efficiency. The mechanization difference is the utilization of an ac reference for the first system as opposed to a dc reference, thereby combining the regulator and chopper functions into a single component and reducing filter size. The primary effort has been on this system.

Before the inverter design continued, it was necessary to determine if the filter is realizable for this mechanization. To simplify the procedure, the following assumptions were made:

1. The high frequency pulses from the chopper, which are bridge-rectified and capacity filtered before the switching regulator, will be considered a firm DC voltage of $\pm$ E volts.

2. The saturation resistance of the switching transistor and the diode (which conducts when the transistor is off) are considered equal and called R. Also, the resistance of the filter inductor is lumped in this term.

3. The inductance and capacitance are considered ideal lumped parameters.

Figure 4.2 shows the circuit to be considered for analysis with its equivalent circuits for the "on" state and "off" state. Whenever the reference voltage exceeds the load voltage, the driver turns on the transistor switch. When the load voltage exceeds the reference, the switch is turned off. Thus, if a threshold voltage is assumed, it is of interest to determine the charging and discharging times of the switching regulator at various phases of the 400 cycle output voltage waveform. These charging and discharging times along with this threshold level are critical in determining system response, maximum switching speed, ripple, and regulation. The switch driver responds to any deviation from the reference level with this threshold tolerance.

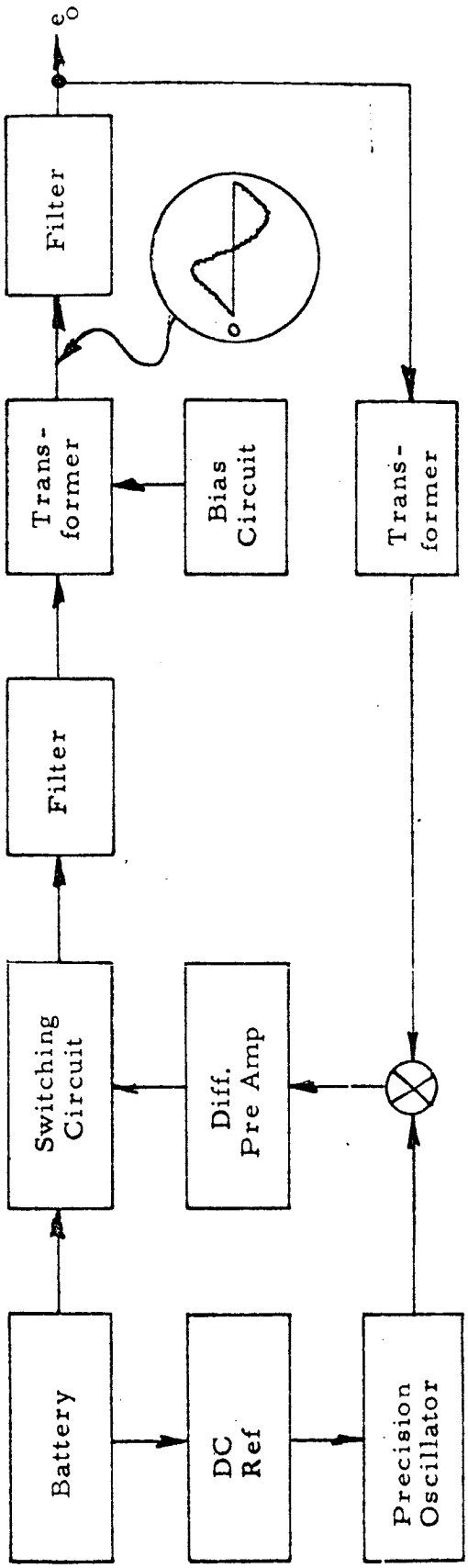


FIGURE 4.1 - AMPLITUDE MODULATION SYSTEM

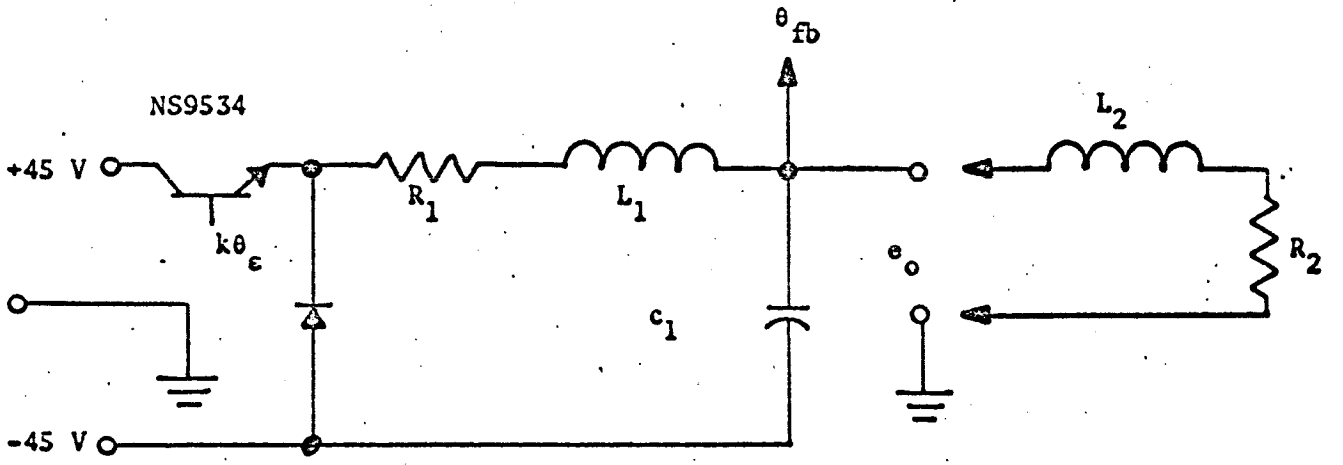
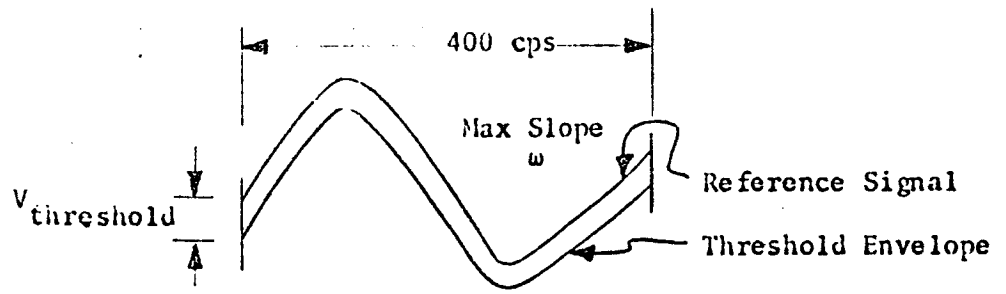


Figure 4.2- Switching Regulator and Filter

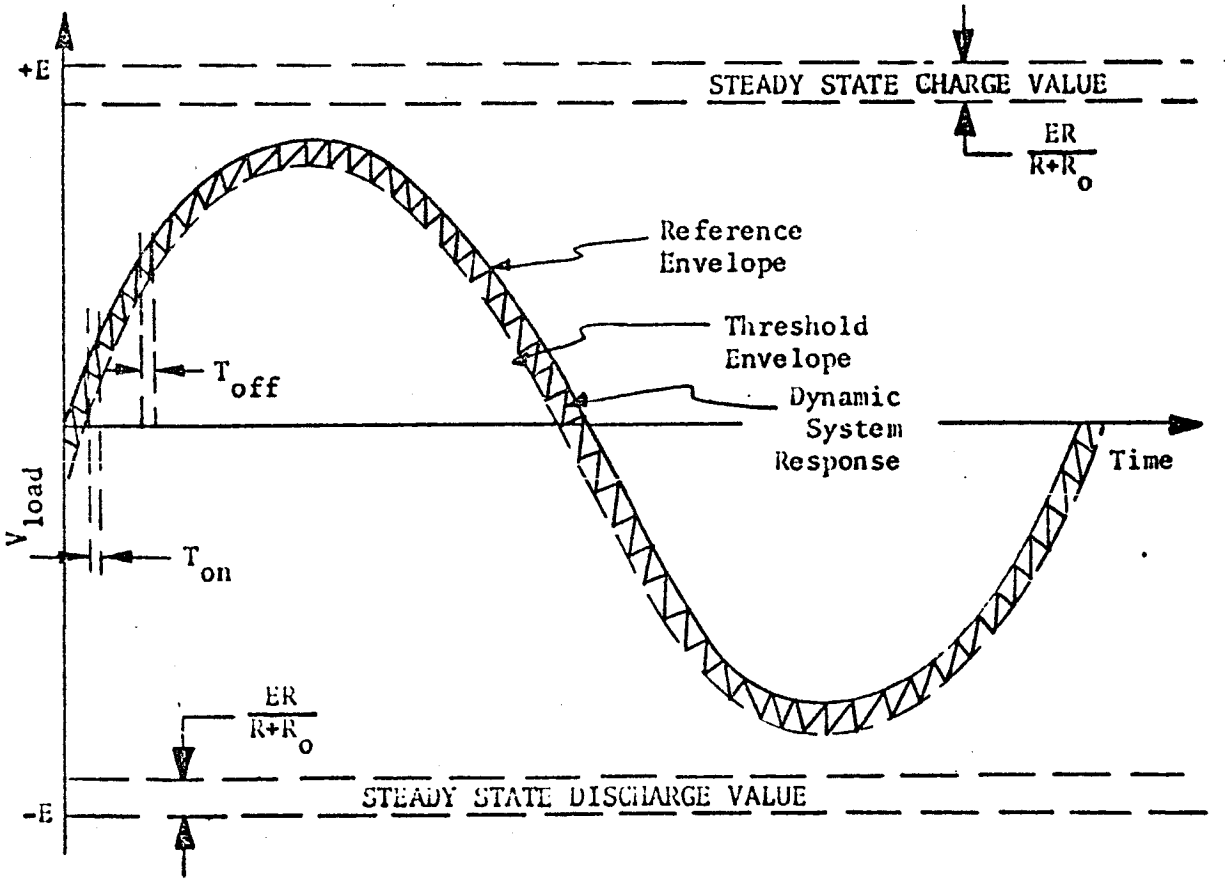
Note that the discharge and charge rates must always be greater than the maximum rate of change of the reference envelope which is $\hat{E}\omega$ (the derivative of $E \sin\omega t$ with $\omega t = 0$).



This charging and discharging rate is defined as follows:

For charging: $\dfrac{V_{L_{on}} - V_{L_{off}}}{T_{on}}$ For discharging: $\dfrac{V_{L_{off}} - V_{L_{on}}}{T_{off}}$

If an ideal system is assumed (no transport time lag), the voltage at the load is described below.



The equivalent circuit (Figure 4.3, B and C) reveals that the charging and discharging pulses are working into a biased level. To illustrate, note that when the reference envelope is at a maximum level, the system will discharge toward the steady state value of $RE/R+R_o$. The time it takes at this point to discharge through the threshold level is less than the time it takes to discharge through the threshold level on the other extreme of the envelope, the minimum voltage point. The same reasoning applies to the charging times. At the minimum value of load voltage, the system charges at a much faster rate than at the maximum voltage where the differential charging voltage is much smaller. Thus, the maximum load voltage has the lowest charging rate and the highest discharge rate while the minimum load voltage has the highest charge rate and the lowest discharge rate.

At this point, it is necessary to describe the system's dynamic response with time. For this analysis, circuit B in Figure 4.3 is used when the switch is on and circuit C when the switch is off. The initial conditions must be determined from the circuit condition preceding the time of switching. If we assume symmetrical operation, that is, that T_{on} of maximum load voltage is identical to T_{off} for minimum load voltage, and T_{off} for maximum load voltage is identical to T_{on} for minimum load voltage, then only two conditions need be evaluated as the extreme cases for our analysis. If T_{off} is chosen with maximum voltage existing across the load, the maximum charging/discharging rate can be determined with the initial conditions at this point equal to the reference envelope $\hat{E} \sin\omega t$. If the T_{off} is chosen with minimum voltage existing across the load, the minimum charging/discharging rate is determined and the initial conditions are still evaluated at $\hat{E} \sin\omega t$. For the analysis, then, it is only necessary to consider circuit C, the equivalent circuit with the switch off.

Evaluation of the Initial Conditions: As long as the system turns off when it coincides with the reference envelope $\hat{E} \sin\omega t$, a statement of the current through the filter inductor and the voltage on the capacitor at any time is sufficient. This approximation is valid as long as the threshold level is a very small portion of the load voltage as it is at the chosen points of interest.

The following equations are derived from the equivalent circuit of Figure 4.3C.

when $V_L = V_{REF}$ at that time called $t = t_o$

at $t = t_o$ $V_L = \hat{E} \sin\omega_n t_n$ where ω_n = freq. of inverter

$= (2\pi)$ (400 cps)

$= 2512$

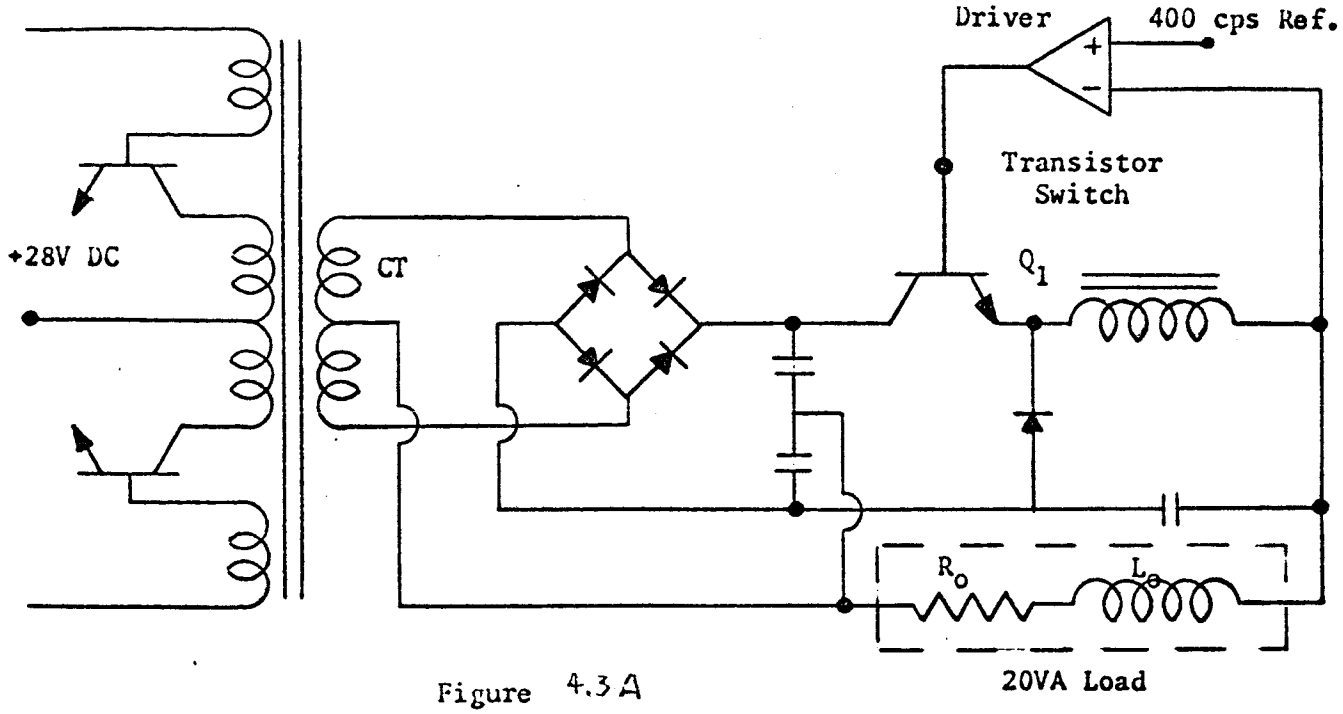


Figure 4.3A

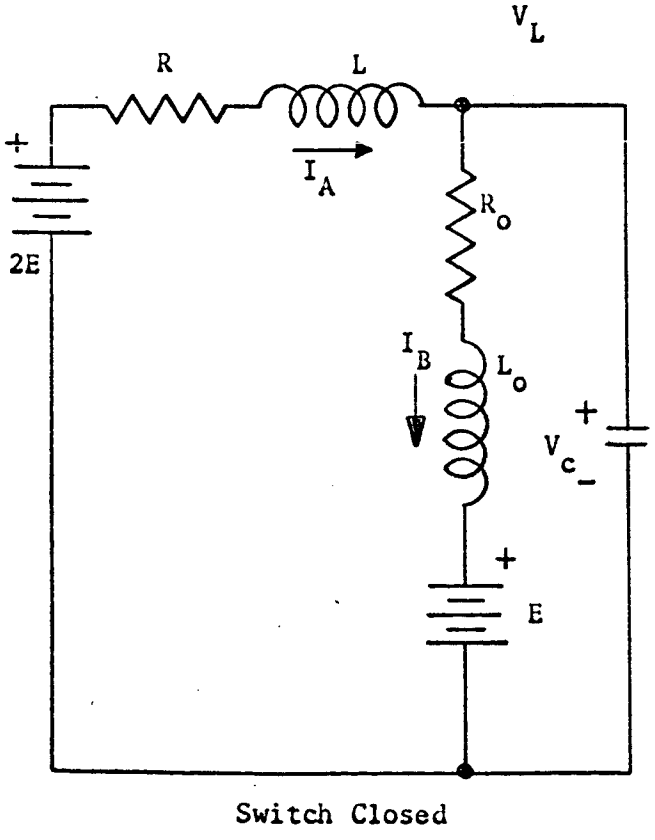


Figure 4.3B

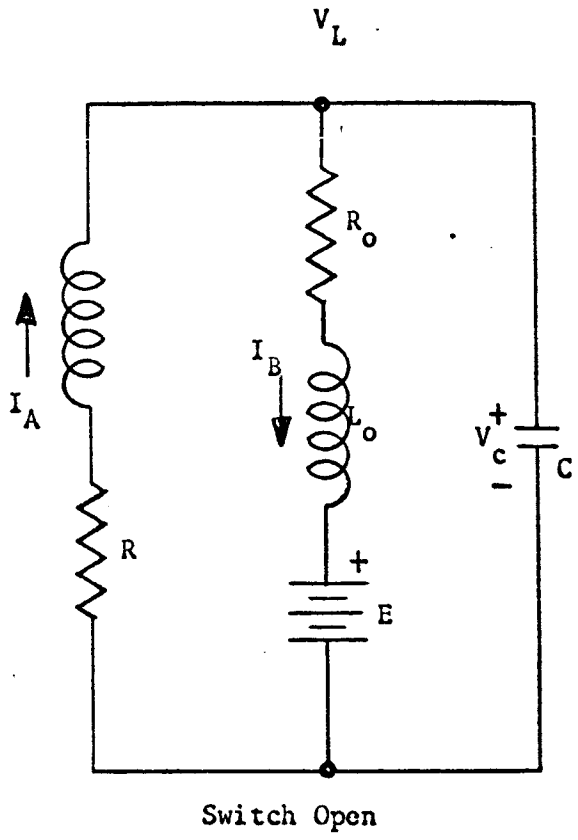


Figure 4.3C

(1) $V_c = E + \hat{E} \sin\omega_n t_n$

(2) $I_A = I_c + I_L$

$$I_L = \frac{\hat{E} \sin\omega_n t_n}{Z(\omega_n)} = \frac{\hat{E}}{|Z(\omega_n)|} \sin(\omega_n t_n - \Phi)$$

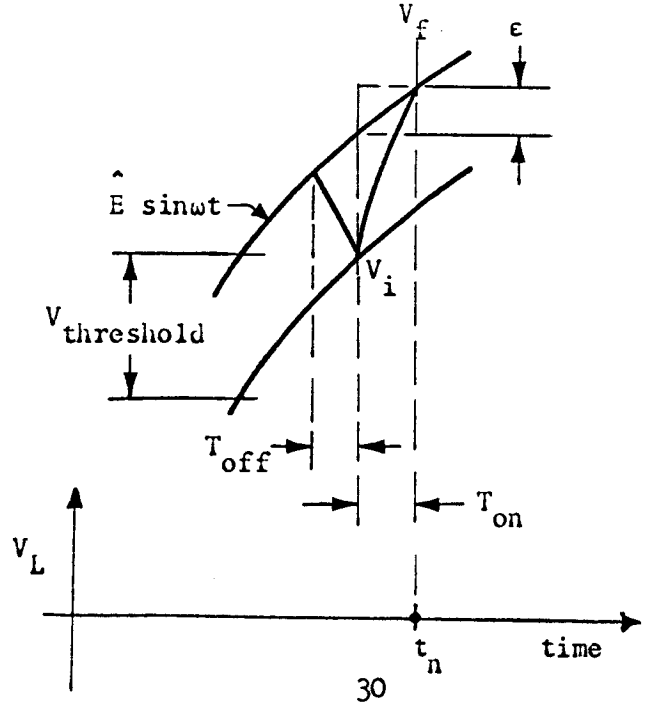
For the equivalent circuit condition:

(3) $$I_L = \frac{\hat{E} \sin\left[\omega_n t_n - \tan^{-1} \frac{\omega_n L_o}{R_o}\right]}{\sqrt{R_o^2 + (\omega_n L_o)^2}}$$

In the diagram below, note that the total increase of voltage over the threshold range during time T_{on} is defined as

$$V_f - V_i = V_T + \hat{E}\left[\sin\omega_n t_n - \sin\omega_n (t_n - T_{on})\right]$$

but $$\sin\omega_n t_n - \sin\omega_n (t_n - T_{on}) = \sin\omega_n t_n - \sin\omega_n t_n \cos\omega_n T_{on} + \sin\omega_n T_{on} \cos\omega_n t_n.$$



so that if $T_{on} << t_n$

$$\varepsilon = \hat{E}\left[\sin\omega_n t_n - \sin\omega_n t_n \cos\omega_n T_{on} + \sin\omega_n T_{on} \cos\omega_n t_n\right]$$

$$\cos\omega_n T_{on} \to 1$$

$$\sin\omega_n T_{on} \to \omega_n T_{on}$$

$$\therefore \varepsilon = \hat{E}\,\omega_n T_{on} \cos\omega_n t_n.$$

and the total voltage differential is

$$(4)\quad V_f - V_i = \hat{E}\,\omega_n T_{on} \cos\omega_n t_n + V_{th}$$

$$\frac{V_f - V_i}{T_{on}} = \frac{\Delta V_L}{\Delta t} = \hat{E}\,\omega_n \cos\omega_n t_n + \frac{V_{th}}{T_{on}}$$

$\therefore$ The current I_c through the capacitor is:

$$(5)\quad I_c = C\frac{\Delta V_L}{\Delta t} = \frac{CV_{th}}{T_{on}} + \omega_n C\,\hat{E}\cos\omega_n t_n.$$

thus the current in the filter inductor can be closely approximated from (3) and (5).

$$(6)\quad I_A = \frac{\hat{E}}{\sqrt{R_o^2 + (\omega_n L_o)^2}} \sin\left[\omega_n t_n - \tan^{-1}\frac{\omega_n L_o}{R_o}\right] + \omega_n C\,\hat{E}\cos\omega_n t_n + \frac{CV_{th}}{T_{on}}.$$

Now the initial conditions at turn-off can be estimated from equations (1) and (6). It is necessary to select the voltage of interest and estimate the turn-on time, T_{on}. If this turn-on time estimate correlates with the calculated time, it acts as an excellent check on the actual system calculations.

Derivation of the Filter's Dynamic Response: Using the equivalent circuit of Figure 4.3c, the following mesh equations are written:

$$(7)\quad -\frac{E}{S} + LI_A = \left[R + R_o + (L + L_o)S\right] I_1(S) - \left[R_o + S\,L_o\right] I_2(S)$$

$$(8)\quad \frac{E}{S} - \frac{V_c}{S} = -\left[R_o + S L_o\right] I_1(S) + \left[\frac{L_o C S^2 + R_o C S + 1}{SC}\right] I_2(S)$$

$$(9)\quad V_L(S) = \left[I_1(S) - I_2(S)\right] Z_o(S)$$

where $Z_o(S) = R_o + S L_o$

$$(10)\quad \Delta I_1(S) = \begin{vmatrix} \frac{SLI_A - E}{S} & -\left[R_o + S L_o\right] \\ \frac{E - V_c}{S} & \frac{L_o C S^2 + R_o C S + 1}{SC} \end{vmatrix}$$

$$(11)\quad \Delta I_2(S) = \begin{vmatrix} \left[R + R_o + (L + L_o)S\right] & \frac{SLI_A - E}{S} \\ -\left[R_o + S L_o\right] & \frac{E - V_c}{S} \end{vmatrix}$$

$$(12)\quad \Delta = \begin{vmatrix} \left[R + R_o + (L + L_o)S\right] & -\left[R_o + S L_o\right] \\ -\left[R_o + S L_o\right] & \left[\frac{L_o C S^2 + R_o C S + 1}{SC}\right] \end{vmatrix}$$

$$\Delta I_1 = \frac{(SLI_A - E)(L_o C S^2 + R_o C S + 1)}{S^2 C} + \frac{(E - V_c)(R_o + S L_o)}{S} \cdot \frac{SC}{SC}$$

$$= L L_o C I_A S^3 + (LCR_o I_A - E L_o C) S^2 + (LI_A - R_o E C) S - E$$

$$+ E L_o C S^2 - V_c L_o C S^2 + E R_o C S - V_c R_o C S$$

$$(13)\quad \Delta I_1 = \frac{LL_oCI_AS^3 + (LCR_oL_A - V_cL_oC)S^2 + (LI_A - R_oCV_c)S - E}{S^2C}$$

$$\Delta I_2 = \left[R + R_o + (L + L_o)S\right]\left(\frac{E - V_c}{S}\right) + \left(\frac{SLI_A - E}{S}\right)(R_o + SL_o)$$

$$\Delta I_2 = (R + R_o)(E - V_c) + (L + L_o)(E - V_c)S + S^2LL_oI_A + SR_oLI_A - EL_oS - ER_o$$

$$(14)\quad \Delta I_2 = \frac{ER - V_c(R + R_o) + \left[L(E + R_oI_A) - V_c(L + L_o)\right]S + LL_oI_AS^2}{S}$$

$$(15)\quad \Delta(I_1 - I_2) = \frac{LC(E - V_c)S^2 + \left[LI_A + RC(E - V_c)\right]S - E}{S^2C}$$

$$\Delta = \frac{\left[(L + L_o)S + R + R_o\right]\left[L_oCS^2 + R_oCS + 1\right]}{CS} - R_o^2 - 2L_oR_oS - L_o^2S^2$$

$$\Delta = (L + L_o)L_oCS^3 + \left(LR_oC + L_oR_oC + RL_oC + R_oL_oC - 2L_oR_oC\right)S^2$$

$$\frac{- L_o^2CS^3 + (RR_oC + R_o^2C + L + L_o - R_o^2C)S + R + R_o}{SC}$$

$$(16)\quad \Delta = \frac{LL_o}{S}\left[S^3 + \left(\frac{R_o}{L_o} + \frac{R}{L}\right)S^2 + \left(\frac{1}{LC} + \frac{1}{L_oC} + \frac{RR_o}{LL_o}\right)S + \frac{R + R_o}{LL_oC}\right]$$

$$I_1(S) - I_2(S) = \frac{LC(E - V_c)S^2 + \left[LI_A + RC(E - V_c)\right]S - E}{LL_oCS\left[S^3 + \left(\frac{R_o}{L_o} + \frac{R}{L}\right)S^2 + \left(\frac{1}{LC} + \frac{1}{L_oC} + \frac{RR_o}{LL_o}\right)S + \frac{R+R_o}{LL_oC}\right]}$$

$$(17)\quad I_1(S) - I_2(S) = \frac{\frac{E - V_c}{L_o}S^2 + \left[\frac{I_A}{L_oC} + \frac{R}{LL_o}(E - V_c)\right]S - \frac{E}{LL_oC}}{S\left[S^3 + \left(\frac{R_o}{L_o} + \frac{R}{L}\right)S^2 + \left(\frac{1}{LC} + \frac{1}{L_oC} + \frac{RR_o}{LL_o}\right)S + \frac{R+R_o}{LL_oC}\right]}$$

$$(18)\quad V_L(S) = \left[I_1(S) - I_2(S)\right]\left[R_o + SL_o\right]$$

$$(19)\quad V_L(S) = \frac{L_o\left\{\frac{E - V_c}{L_o}S^2 + \left[\frac{I_A}{L_oC} + \frac{R}{LL_o}(E - V_c)\right]S + \frac{E}{LL_oC}\right\}\left(S + \frac{R_o}{L_o}\right)}{S\left[S^3 + \left(\frac{R_o}{L_o} + \frac{R}{L}\right)S^2 + \left(\frac{1}{LC} + \frac{1}{L_oC} + \frac{RR_o}{LL_o}\right)S + \frac{R+R_o}{LL_oC}\right]}$$

$$(20)\quad \text{Define } D = S\left[S^3 + \left(\frac{R_o}{L_o} + \frac{R}{L}\right)S^2 + \left(\frac{1}{LC} + \frac{1}{L_oC} + \frac{RR_o}{LL_o}\right)S + \frac{R+R_o}{LL_oC}\right.$$

Then:

$$(21)\quad DV_L(S) = (E - V_c)S^3 + \left[\frac{I_A}{C} + \left(\frac{R}{L} + \frac{R_o}{L_o}\right)(E - V_c)\right]S^2 + \left[\frac{I_AR_o}{L_oC} + \frac{E}{LC} + \frac{RR_o}{LL_o}(E - V_c)\right]S + \frac{ER_o}{LL_oC}\ .$$

Assuming values for the system parameters allow the calculation of D in (20) above.

Let
$R = 2$ ohms
$R_o = 21.7$ ohms
$L = 0.50$ mh
$L_o = 10.30$ mh
$C = 1.0$ uf
$E = 45.0$ V

$$(22)\quad D = S^3 + 6.105 \times 10^3\, S^2 + 2.1 \times 10^9 S + 4.6 \times 10^{12}$$

Using synthetic division to find the real root, the expression factors into:

$$D = (S + 2.19 \times 10^3)\left[(S + 1.958 \times 10^3)^2 + (4.57 \times 10^4)^2\right]. \tag{23}$$

The numerator (21) can be combined in terms of initial conditions in the following manner:

$$DV_L(S) = E\left[S^3 + \left(\frac{R}{L} + \frac{R_o}{L_o}\right)S^2 + \left(\frac{RR_o}{LL_o} - \frac{1}{LC}\right)S - \frac{R_o}{LL_oC}\right] - V_c\left[S^3 + \left(\frac{R}{L} + \frac{R_o}{L_o}\right)S^2 + \frac{RR_o}{LL_o}S\right] + \frac{I_A}{C}\left[S^2 + \frac{R_o}{L_o}S\right]. \tag{24}$$

Knowing the initial conditions allows the S-plane evaluation of this response. The total $V_L(S)$ can be written:

$$V_L(S) = \frac{E\left[S^3 + \left(\frac{R}{L} + \frac{R_o}{L_o}\right)S^2 + \left(\frac{RR_o}{LL_o} - \frac{1}{LC}\right)S - \frac{R_o}{LL_oC}\right]}{S\,(S + 2.19 \times 10^3)\left[(S + 1.958 \times 10^3)^2 + (4.57 \times 10^4)^2\right]} + \frac{\frac{I_A}{C}\left[S^2 + \frac{R_o}{L_o}S\right] - V_c\left[S^3 + \left(\frac{R}{L} + \frac{R_o}{L_o}\right)S^2 + \frac{RR_o}{LL_o}S\right]}{S(S + 2.19 \times 10^3)\left[(S + 1.958 \times 10^3)^2 + (4.57 \times 10^4)^2\right]}. \tag{25}$$

These equations can be expanded using partial fraction expansion and the inverse LaPlace transformation taken to yield the load voltage variation in the time domain.

If the natural damping ratio for this equation is examined, it is found to be entirely too small to be useful and the circuit will oscillate near the natural frequency, since the voltage will not damp out before the next pulse appears.

$$\alpha = 1.958 \times 10^3 = 2\delta\omega_n$$

$$\delta = \frac{\alpha}{2\omega_n} = \frac{1.958}{(2)(45.7)} = .0214$$

By decreasing L and increasing C, the damping is increased.

$L = 50\ \mu h$ and $C = 10\ \mu f$..

Then:

(26) $D = S^3 + 42.1 \times 10^3 S^2 + 201 \times 10^3 S + 4.6 \times 10^8$

(27) $D = (S + 2.4 \times 10^3) \quad (S + 19.88 \times 10^3)^2 + (43.7 \times 10^3)^2$

Now the damping ratio is:

$$= \frac{19.88}{(2)(43.7)} = 0.227$$

In order to prevent the undershoot from exceeding the threshold level, the damping ratio must increase to near 0.8. This can be accomplished by allowing L = 10μh and C = 10 μ f.

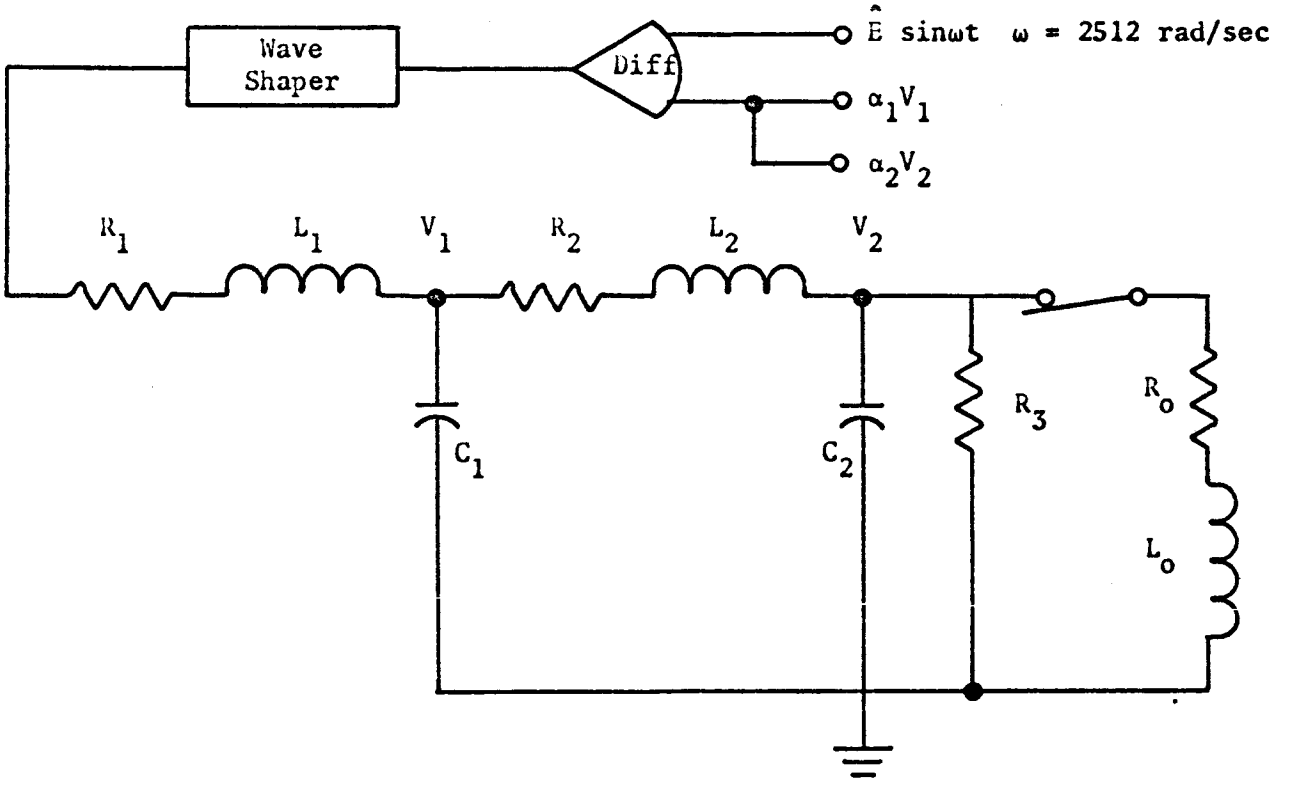
(28) $D = S^3 + 2.02 \times 10^5 S^2 + 14.21 \times 10^9 S + 2.3 \times 10^{13}$

(29) $D = (S + 1.66 \times 10^3) \quad (S + 10^5)^2 + (.622 \times 10^5)^2$

$$= \frac{1}{1.244} = 0.804$$

Since the calculations involved are very laborious and the results for switching time determination appear inconclusive because it is necessary to settle upon an optimum damping ratio which will still allow size reduction and good frequency and amplitude stability, the filter circuit was programmed on Lockheed's analog computer.

400 Hz Inverter's Computer Mechanization: The circuit below depicts the electronic equivalent programmed on the analog computer.



Current equations are used to describe this system's response. They are derived below.

Writing the node equations:

$$\frac{V_1 - V_2}{R_2 + SL_2} + \frac{0 - V_2}{(1/C_2S)} + \frac{0 - V_2}{R_3} + \frac{0 - V_2}{R_o + L_oS} = 0$$

expanding, this becomes:

$$V_1R_3 = V_2R_3 + V_2R_3C_2S(R_2 + L_2S) + V_2(R_2 + L_2S) + V_2R_3\left(\frac{R_2 + L_2S}{R_o + L_oS}\right).$$

$$V_1 = V_2\left[1 + C_2S(R_2 + L_2S) + \frac{R_2 + L_2S}{R_3} + \frac{R_2 + L_2S}{R_o + L_oS}\right]$$

$$V_1 = V_2\left[L_2C_2S^2 + \left(R_2C_2 + \frac{L_2}{R_3}\right)S + 1 + \frac{R_2}{R_3} + \frac{R_2 + L_2S}{R_o + L_oS}\right].$$

$$V_2S^2 = -\left\{\left(\frac{R_2C_2}{L_2C_2} + \frac{L_2}{R_3L_2C_2}\right)SV_2 + \left(\frac{1}{L_2C_2} + \frac{R_2}{R_3L_2C_2}\right)V_2 + \left(\frac{R_2 + L_2S}{R_o + L_oS}\right)\frac{V_2}{L_2C_2} - \frac{V_1}{L_2C_2}\right\}.$$

$$\ddot{V}_2 = -\left(\frac{R_2}{L_2} + \frac{1}{C_2R_3}\right)\dot{V}_2 - \left(1 + \frac{R_2}{R_3}\right)\frac{1}{C_2L_2}V_2 - \frac{R_2}{R_o}\left(\frac{1 + \frac{L_2}{R_2}P}{1 + \frac{L_o}{R_o}P}\right)\frac{1}{L_2C_2}V_2 + \frac{V_1}{L_2C_2}$$

Let $A'' = \left(C_2R_2 + \frac{L_2}{R_3}\right)\frac{1}{C_2L_2}$ $\qquad D'' = \frac{1}{C_2L_2}$

$B'' = \left(1 + \frac{R_2}{R_3}\right)\frac{1}{C_2L_2}$ $\qquad \frac{L_2}{R_2} = \tau_2$

$C'' = \frac{R_2}{R_oL_2C_2}$ $\qquad \frac{L_o}{R_o} = \tau_o$

Then:

(1) $$\ddot{V}_2 = -A''V_2 - B''V_2 - C'' \left(\frac{1 + \tau_2 P}{1 + \tau_o P}\right) + D''V_1$$

$$\frac{e_{in} - V_1}{R_1 + L_1 S} + \left(0 - V_1\right) C_1 S + \frac{V_2 - V_1}{R_2 + L_2 S} = 0 .$$

$$e_{in}\left(R_2 + L_2 S\right) + V_2\left(R_1 + L_1 S\right) =$$

$$\left(R_2 + L_2 S\right) V_1 C_1 S \left(R_1 + L_1 S\right) + V_1\left(R_2 + L_2 S\right) + V_1\left(R_1 + L_1 S\right).$$

$$e_{in}\left(R_2 + L_2 S\right) + V_2\left(R_1 + L_1 S\right) = \left\{C_1 L_1 L_2 S^3 + C_1\left(R_1 L_2 + R_2 L_1\right) S^2 + \left(C_1 R_1 R_2 + L_1 + L_2\right) S + R_1 + R_2\right\} V_1 .$$

$$\left\{S^3 + \frac{R_1 L_2 + R_2 L_1}{L_1 L_2} S^2 + \frac{C_1 R_1 R_2 + L_1 + L_2}{C_1 L_1 L_2} S + \frac{R_1 + R_2}{C_1 L_1 L_2}\right\} V_1 =$$

$$\frac{R_2}{C_1 L_1 L_2} e_{in} + \frac{L_2 S\, e_{in}}{C_1 L_1 L_2} + \frac{V_2 R_1}{C_1 L_1 L_2} + \frac{L_1 S\, V_2}{C_1 L_1 L_2}$$

Let $E'' = \left(\frac{R_2 L_1 + R_1 L_2}{C_1 L_1 L_2}\right) C_1$ $\qquad I'' = \frac{L_2}{C_1 L_1 L_2}$

$F'' = \frac{C_1 R_1 R_2 + L_2 + L_1}{C_1 L_1 L_2}$ $\qquad J'' = \frac{R_1}{C_1 L_1 L_2}$

$G'' = \frac{R_2 + R_1}{C_1 L_1 L_2}$ $\qquad K'' = \frac{L_1}{C_1 L_1 L_2}$

$H'' = \frac{R_2}{C_1 L_1 L_2}$ $\qquad L'' = \frac{1}{C_1 L_1 L_2}$

$$\dddot{V}_1 = - E'' \ddot{V}_1 - F'' \dot{V}_1 - G'' V_1 + H'' e_{in} + I'' \dot{e}_{in} + J'' V_2 + K'' \dot{V}_2$$

$$\ddot{V}_1 = - E'' \dot{V}_1 - F'' V_1 - G'' \int V_1 dt + H'' \int e_{in} dt + I'' e_{in} + J'' \int V_2 dt + K'' V_2 \quad (2)$$

Equations (1) and (2) are now generated on the analog computer along with an electronic switch for positive and negative e_{in} (see Figure 4.4). The reference voltage and portions of V_1 and V_2 are summed into amplifier 12 which drives the electronic switch. Table I lists the calculated values and coefficient of each pot used in the program. The amplitude and time scaling are also given in the table. Systems 3 and 5 are the third and fifth computer runs respectively with the following circuit values used.

$R_1 = 2\ \Omega$ $\quad R_2 = 0.5\ \Omega$ $\quad R_3 = 3\ k\Omega$

$L_1 = 60\ \mu h$ $\quad L_2 = 1.5\ mH$ $\quad L_o = 10.3\ mH$ } System #3

$C_1 = 0.5\ \mu F$ $\quad C_2 = 2\ \mu F$ $\quad R_o = 21.7\ \Omega$

$\alpha_1 = \alpha_2 = 0.30$

Same as System #3 except $L_2 = 0.75\ mH$, $C_2 = 4\ \mu F$ } System #5

It was found that a minimum voltage level of $\pm$ 60 VDC was needed to drive the filter sections without causing the loop to open at the high or low voltage level. The ripple shown on the computer runs was below 1/2 V peak to peak, and the regulation scaled from the no-load to full-load switching on the computer run for System #5 was below 1 per cent. There was no noticeable change in output voltage with variations in e_{in} as long as the 60 V margin was maintained.

Figure 4.5 shows the output voltage V_2 as a function of time first in the unloaded and then switched to the loaded case. Note that on all these figures, that the time t = 0 begins on the right.

Figure 4.6 shows the output ripple and indicates the system stability when a small perturbation was applied. Note the time scale change on the left. Figures 4.7 and 4.8 show the number of cycles it takes for the output to stabilize when the system is first turned on. Figure 4.7 is the no-load condition and Figure 4.8 is the loaded condition.

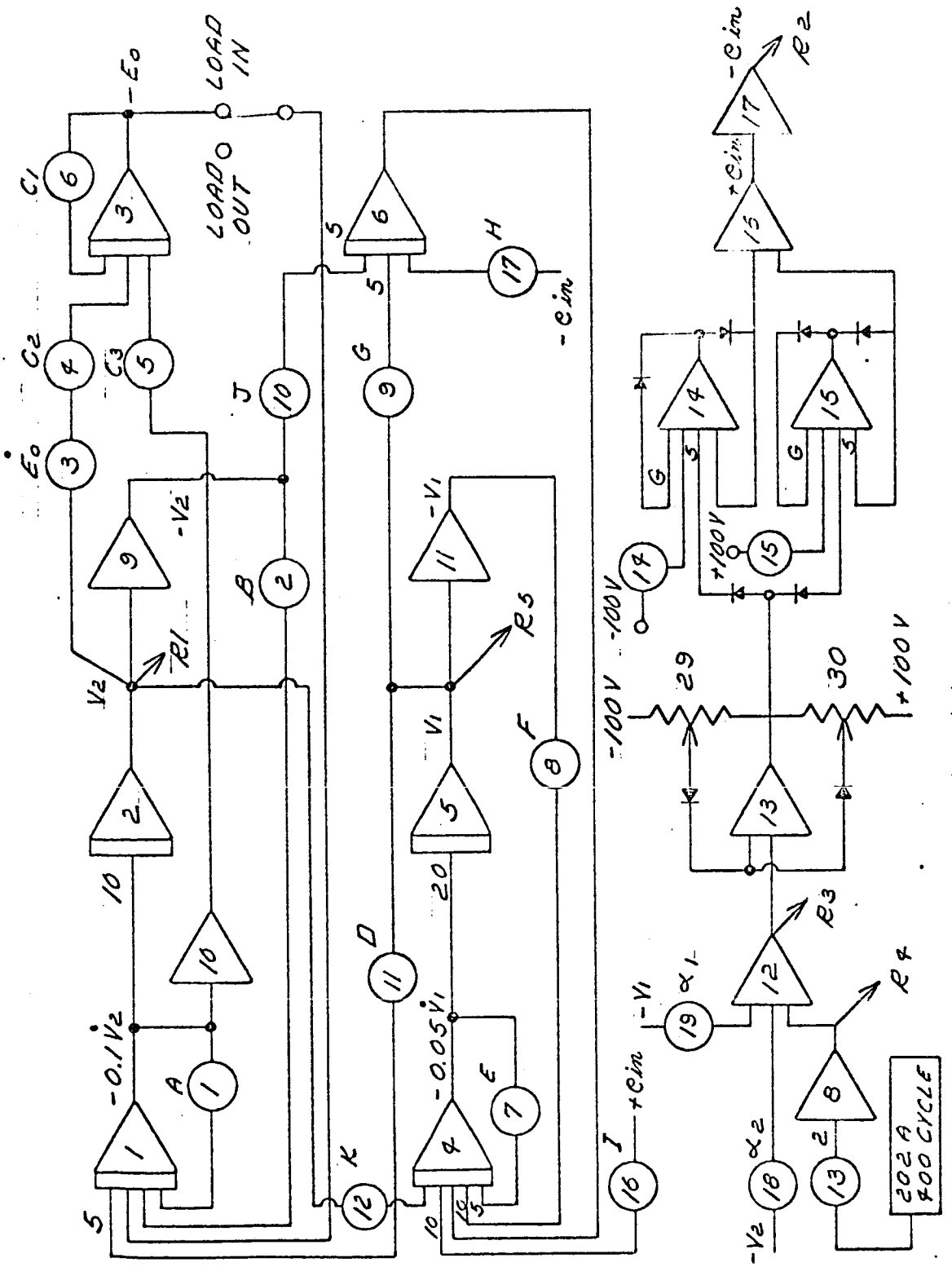

LOAD IN
LOAD OUT
-E0
C1
C2
C3
E0
-V2
V2
R1
A
B
J
G
H
-ein
D
-V1
V1
R5
F
K
E
I
+ein
-0.1 V2
-0.05 V1
10
20
5
10
-100 V
+100 V
29
30
R2
R3
R4
α1
α2
-V1
-V2
202 A
400 CYCLE

FIGURE 4.4

TABLE I

Coefficient Formula	Coefficient Value	Multiplier	Pot No.	System 3		System 5	
$A'' = \left(C_2 R_2 + \frac{L_2}{R_3}\right) D''$	0.6667^{3}	1^{-4}	1	0.5	0.05	$.75^{3}$	.075
$B'' = \left(1 + \frac{R_2}{R_3}\right) D''$	0.6668^{9}	1^{-9}	2	0.3333^{9}	0.3333	$.333^{9}$	.333
$\bar{C}_2 = \bar{C}_1 \frac{R_2}{R_0} D''$	0.003236^{13}	1^{-12}	3	0.001618^{13}	0.0162	1.63×10^{10}	.0163
$\bar{C}_3 = \bar{C}_2 \frac{L_2}{R_2}$	0.09707^{9}	1^{-8}	5	0.04854^{9}	0.4854	$.622^{7}$	.0622
$\bar{C}_1 = \frac{R_0}{L_0}$	0.21066^{4}	1^{-4}	6	0.21066^{4}	0.2107	$.2107^{4}$	.2107
$L'' = \frac{1}{C_1 L_2 L_1}$	11.1111^{12}			22.2222^{12}		4.444^{3}	
$E'' = C_1 (R_2 L_1 + R_1 L_2)'' L''$	33.6667^{3}	2^{-5}	7	33.6667^{3}	0.6733	33.66^{3}	.6733
$F'' = (C_1 R_1 R_2 + L_1 L_2)'' L''$	17.3444^{9}	0.5^{-10}	8	34.6778^{9}	0.8669	3.599^{10}	.8997
$G'' = (R_1 + R_2) L''$	27.7778^{12}	1^{-14}	9	55.5556^{12}	0.5556	11.111^{13}	.5556
$J'' = (R_1) L''$	22.2222^{12}	1^{-14}	10	44.444^{12}	0.4444	8.88^{13}	0.888
$D'' = \frac{1}{C_2 L_2}$	0.6667^{9}	2^{-10}	11	0.3333^{9}	0.0667	$1/3^{9}$	0.0667
$K'' = L_1 L''$	0.6667^{9}	0.5^{-9}	12	1.3333^{9}	0.6667	2.667^{9}	.6667
$I'' = L_2 L''$	16.6667^{9}	0.5^{-10}	16	33.3333^{9}	0.8333	3.333^{10}	.8333
$H'' = R_2 L''$	5.5556^{12}	0.5^{-13}	17	11.1111^{12}	0.5556	2.222^{13}	.5556
$B''' = 1/L_1$	1.6667^{4}	2^{-5}	22 & 23			1.667^{4}	.333
$A''' = R_1/L_1$	3.3333^{4}	1^{-5}	24			0.333^{5}	.333

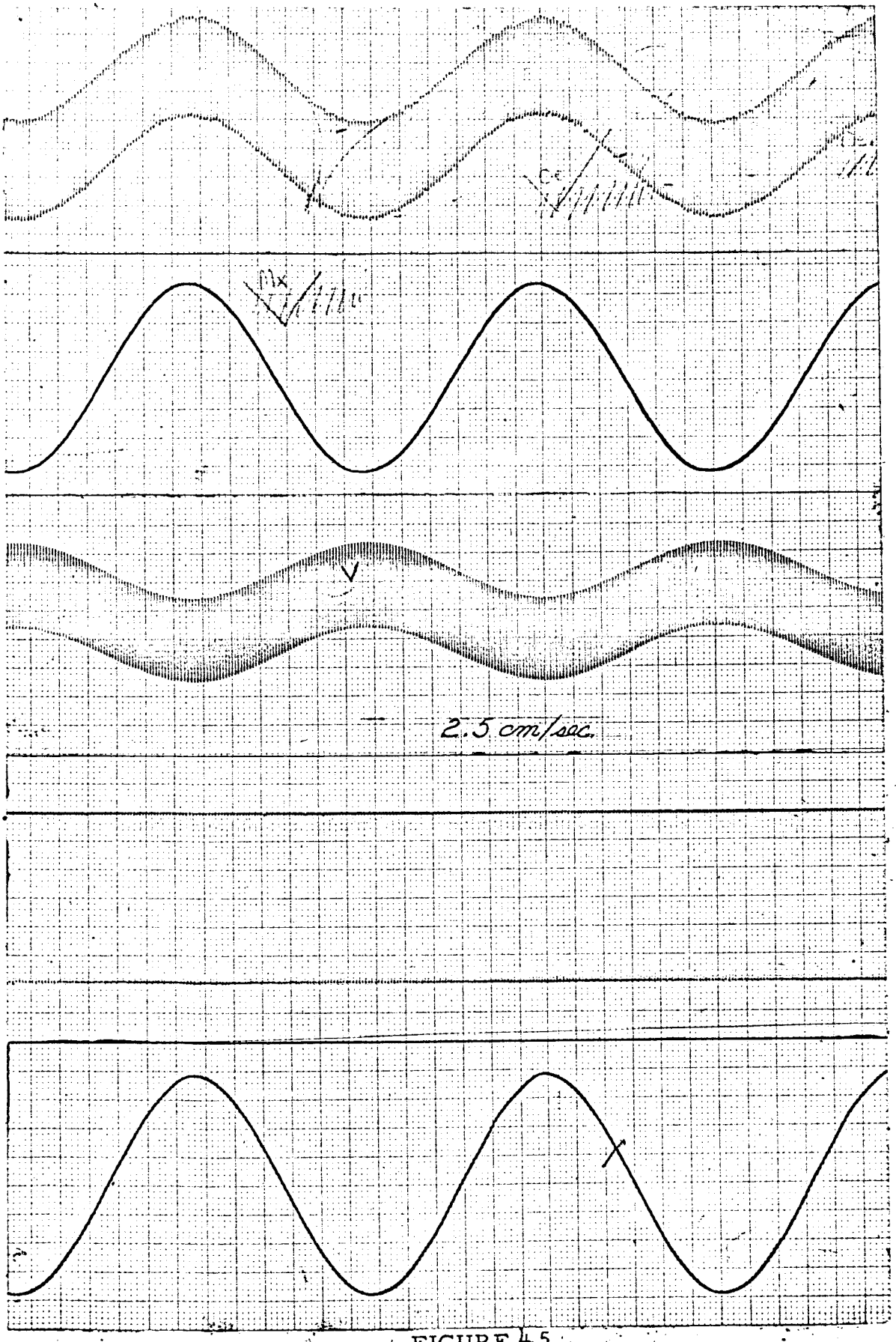


FIGURE 45

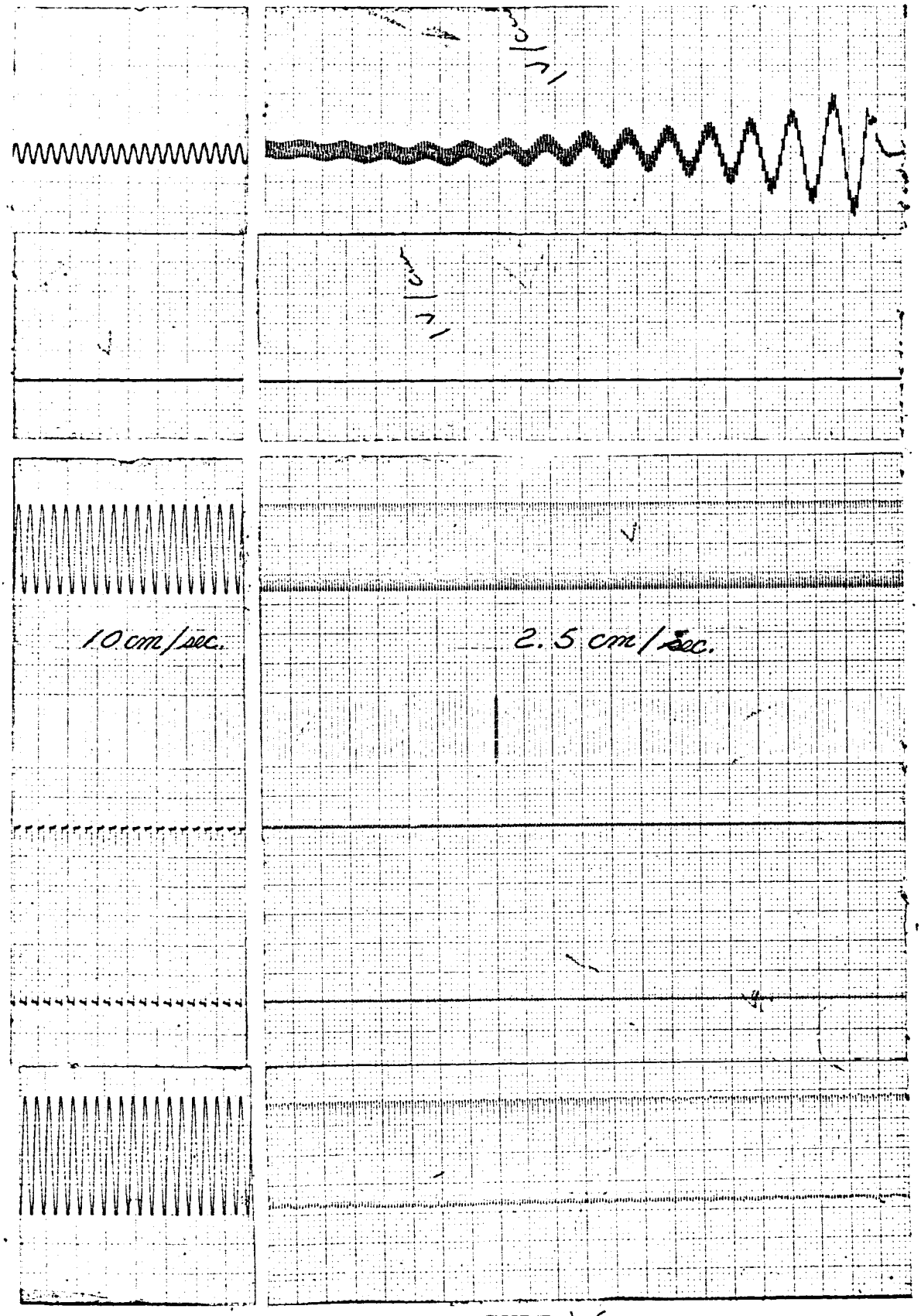

V1
50V/cm
Ref.
1V/cm
Error
20V/cm.
10 cm/sec.
2.5 cm/sec.
Driver
50V/cm
V2
1V/cm

FIGURE 4.6

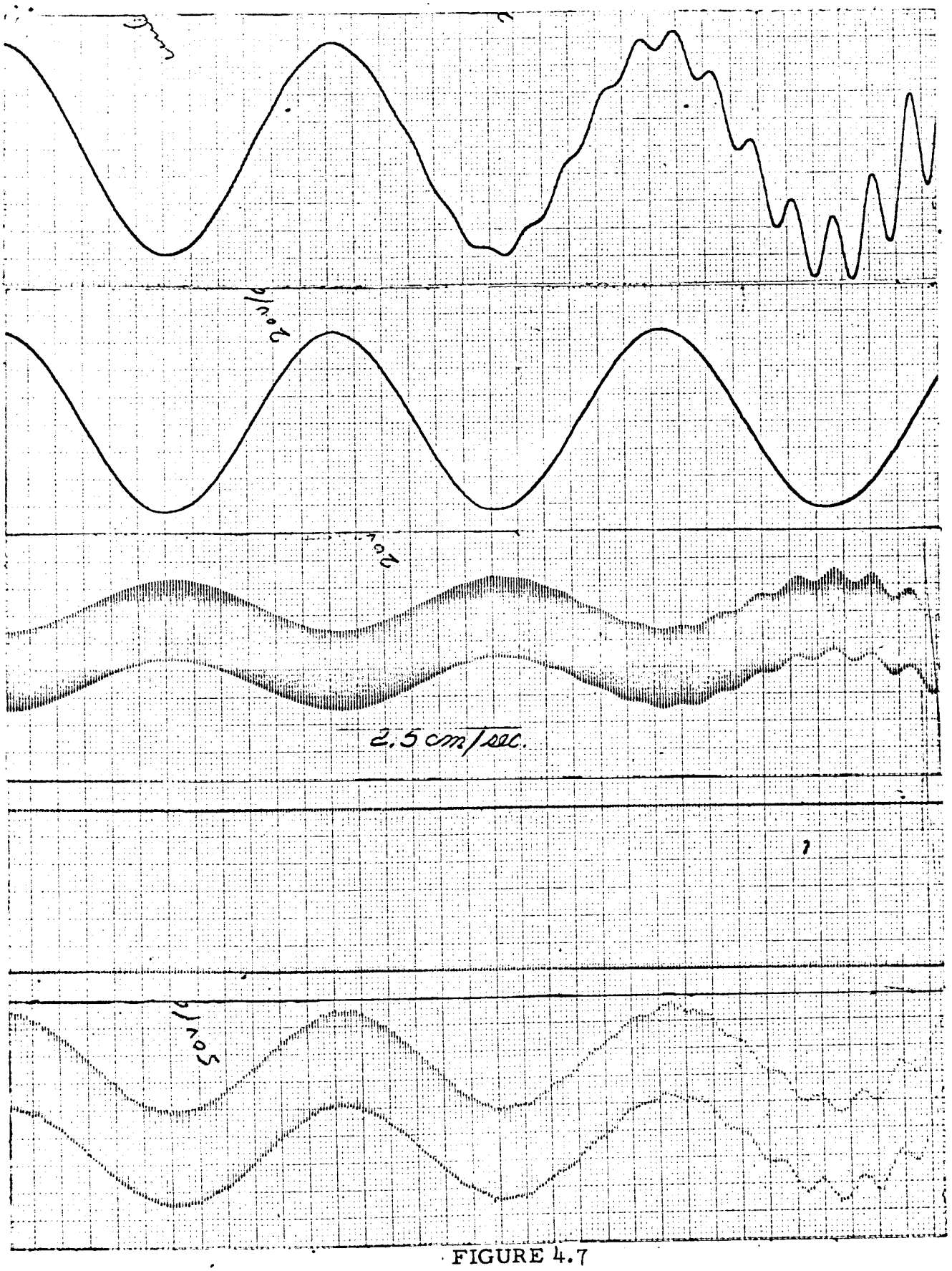

V_1
50V/cm
Ref.
20V/cm
Error
20V/cm
2.5 cm/sec.
Driver
50V/cm
V_2
20V/cm

FIGURE 4.7

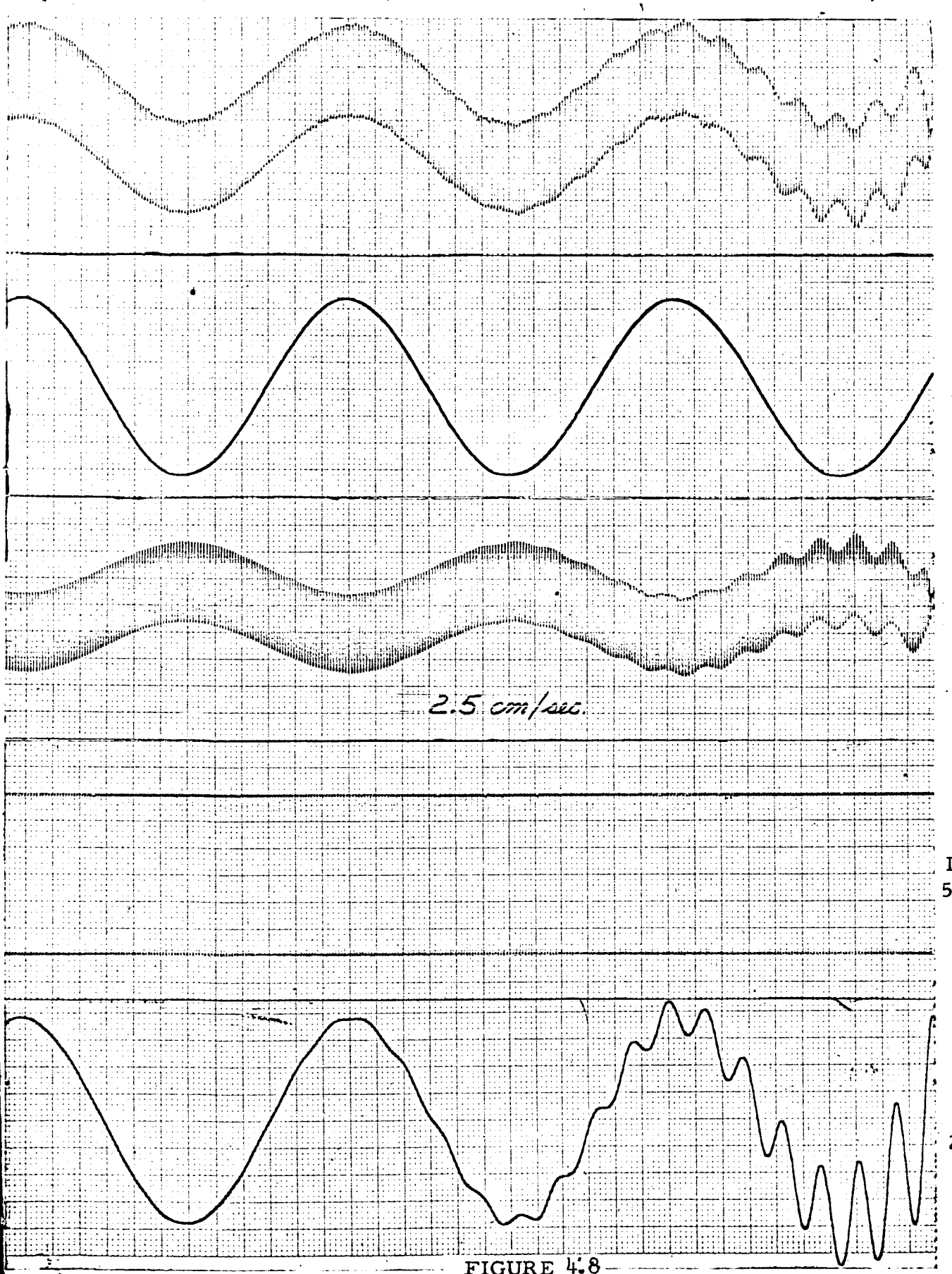

V_1
50V/cm
Ref.
20V/cm
Error
20V/cm
2.5 cm/sec.
Driver
50V/cm
V_2
20V/cm

FIGURE 4.8

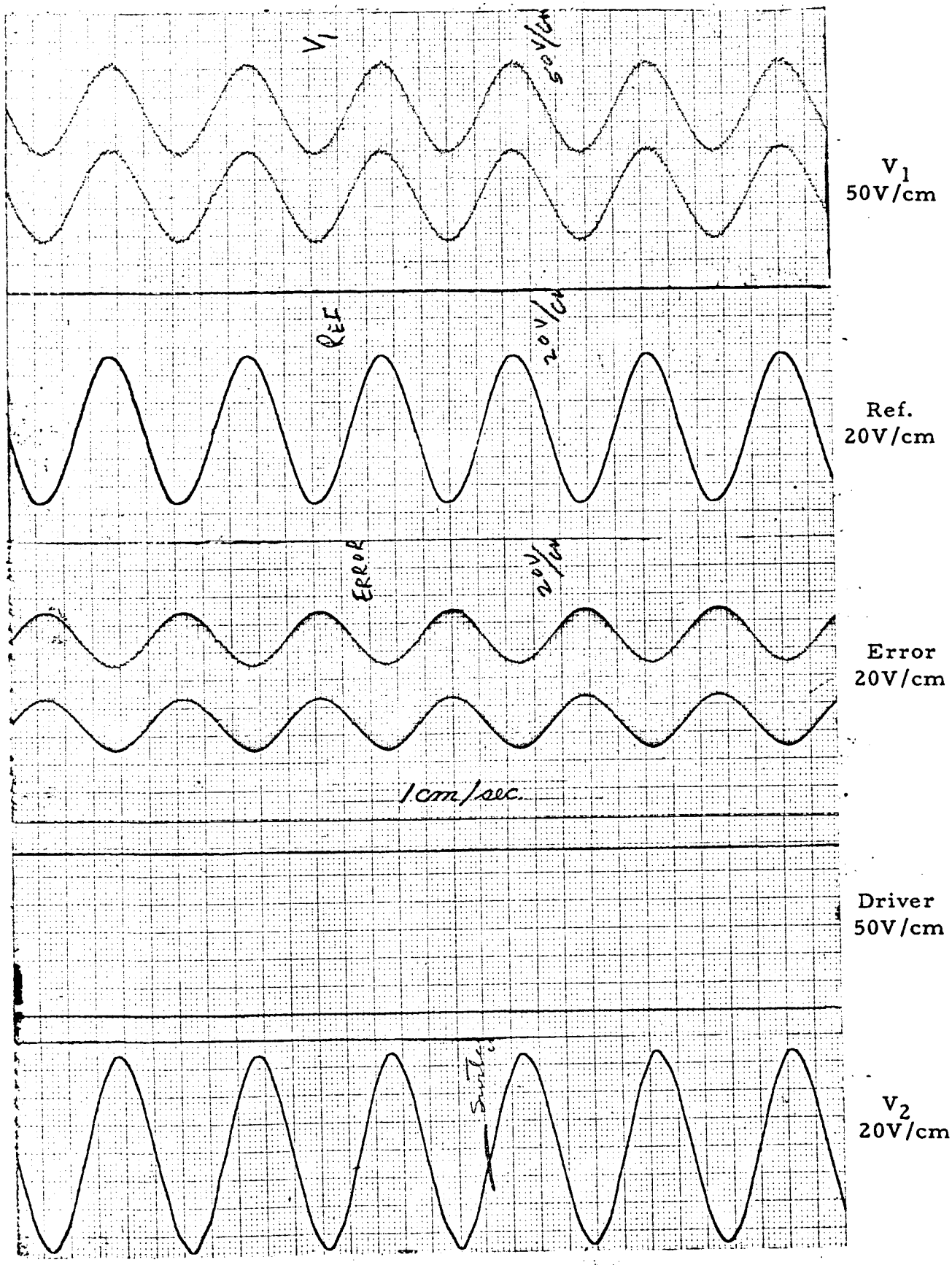

V1
50 V/cm
REF
20 V/cm
ERROR
20 V/cm
1 cm/sec
V1
50V/cm
Ref.
20V/cm
Error
20V/cm
Driver
50V/cm
V2
20V/cm

FIGURE 4.9

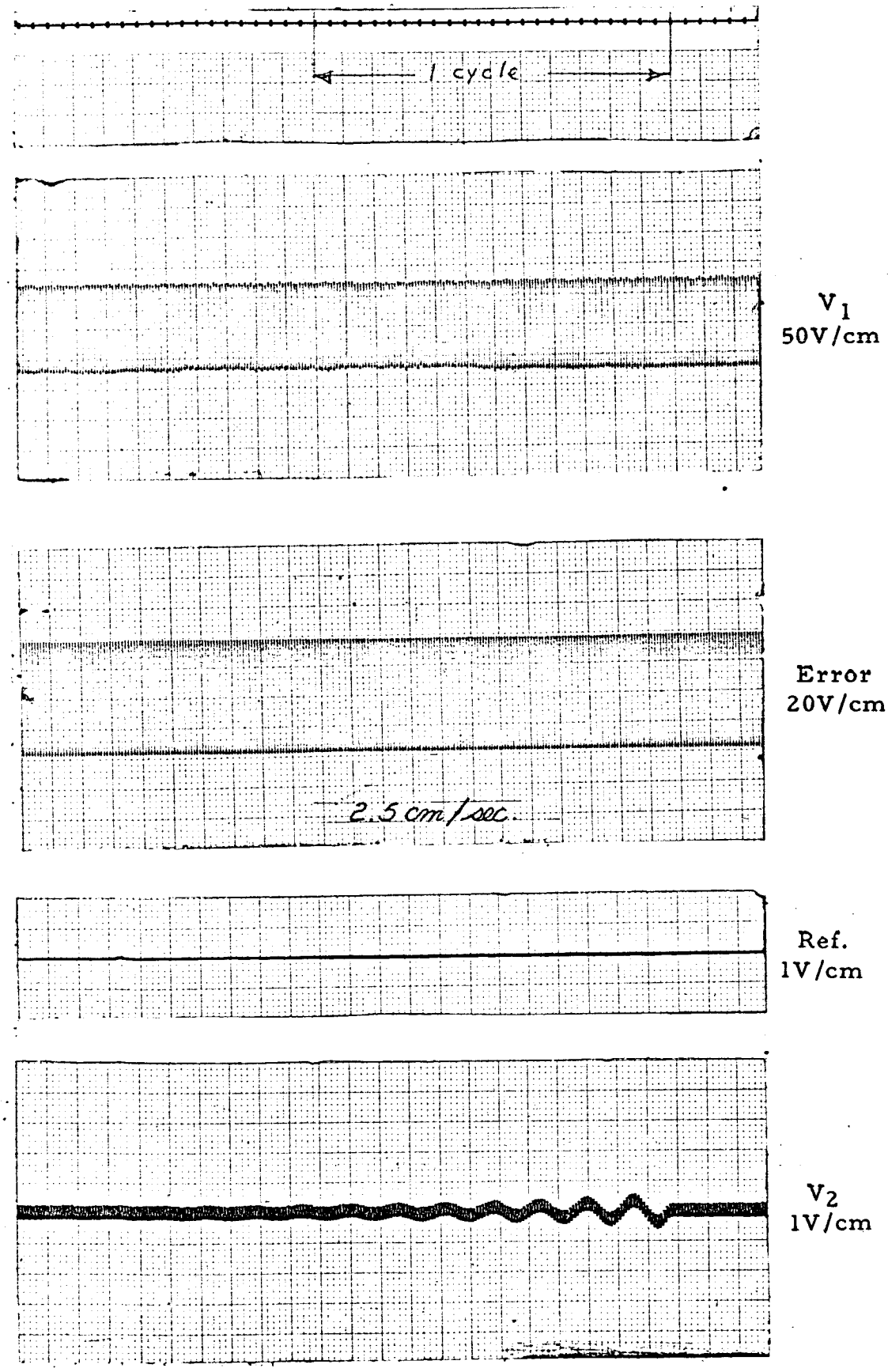


FIGURE 4.10

Figures 4.9 and 4.10 are from the fifth computer run while the previous figures were made on the third run. Figure 4.9 shows the regulation when the load is switched in and out. The slight distortion which appears on the output traces damped out after 15 cycles. Figure 4.10, again, shows the ripple and response to a small perturbation. Note the scale change to 1V/cm.

General Mechanization of the 400 Cycle Inverter: The block schematic, Figure 4.11, incorporates the filter results from the computer study with a general method for mechanization. As pointed out by Mr. Owens and verified by the computer run, a simple diode will not perform the commutating function due to the reversal of load current. It is necessary to switch from the plus to minus side of the line. A gating method was incorporated to accomplish this. Silicon-controlled switches lend themselves to this type of operation, but because of their instability under radiation and frequency, other limitation methods of gating with transistors were explored.

Driver Mechanization: Two basic forms of drivers involving both bistable and tristable circuits have been used to study the power switch characteristics. The prime requirement placed upon the driver has been to provide the fastest possible switching signal for the power switch. Basic physical properties of the power switch have delayed the development of the device.

There are many high power transistors which can withstand 150 watts. However, these transistors typically have switching times of 5-7μ sec. Laboratory tests of this circuit, with power supplies of $\pm$ volts, have developed current transients of 2 amperes with transistors which switch in 200 nsec. Hence, a 5μ sec, 150 volt short circuit cannot be tolerated.

A base driver circuit can be designed to account for a 5μ sec switching time by delaying the turn-on of the second transistor by an equal time. However, the switching circuit now under development uses a switching frequency of 50 kc. A 5μ sec storage time at this frequency would reduce the maximum possible modulation to 50%. Thus, a higher supply voltage is required in order to maintain the required current.

A lower switching frequency can be used, but this will require a larger filter-inductor and a higher supply voltage. The larger inductor will be required to support current longer during the opposite voltage cycle. The higher supply voltage will be required to provide the same initial L/R slope through the larger inductor.

Higher speed transistors rated for I_C max of 2 or 3 amperes and V_{CE} max of 180 volts are still unacceptable because they experience secondary breakdown (see Figure 4.15) when called upon to switch the inductive load.

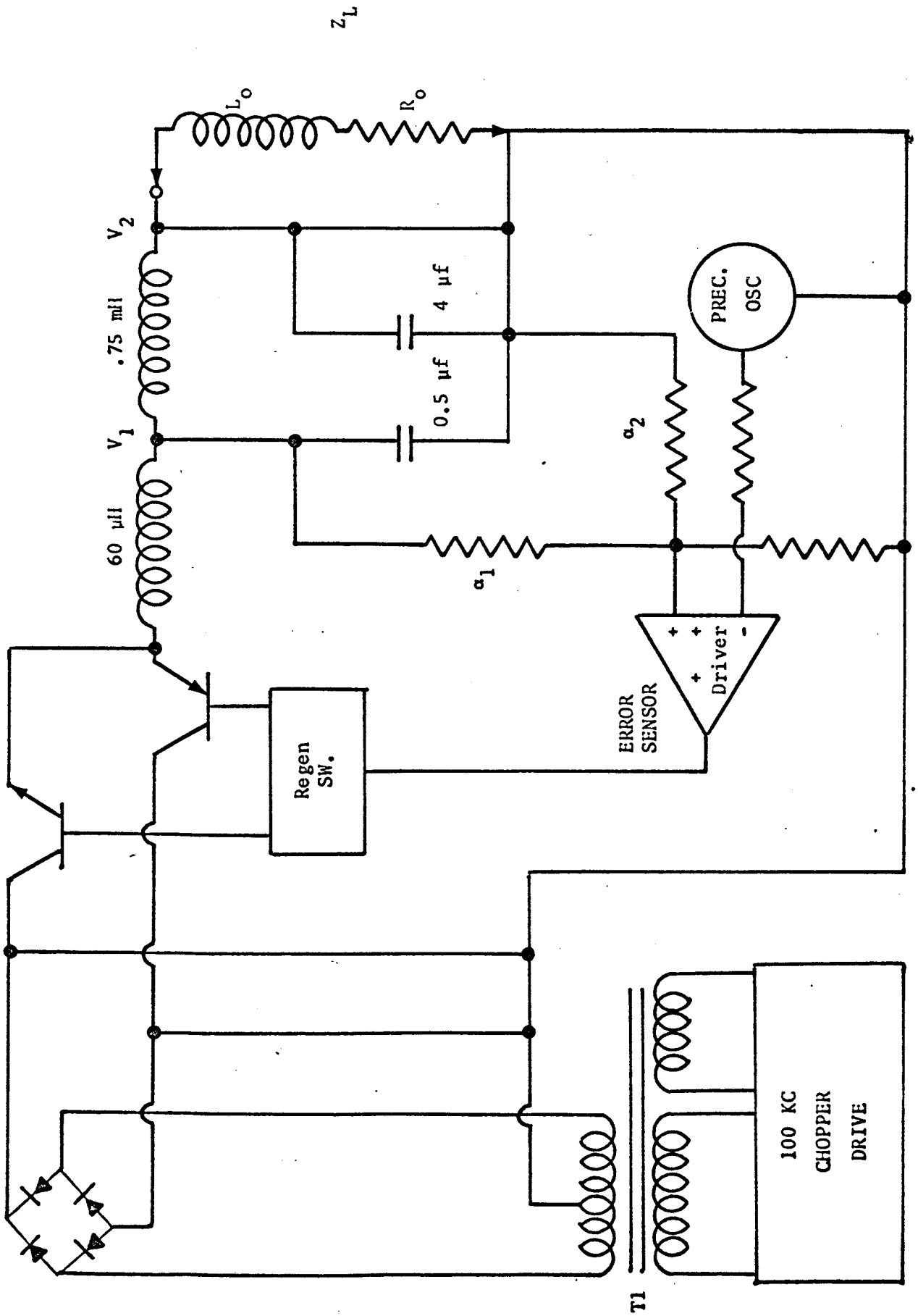

Z_L
L_o
R_o
V_2
.75 mil
V_1
60 µH
4 µf
0.5 µf
α_2
α_1
PREC. OSC
Driver
ERROR SENSOR
Regen SW.
T1
100 KC CHOPPER DRIVE

FIGURE 4.11

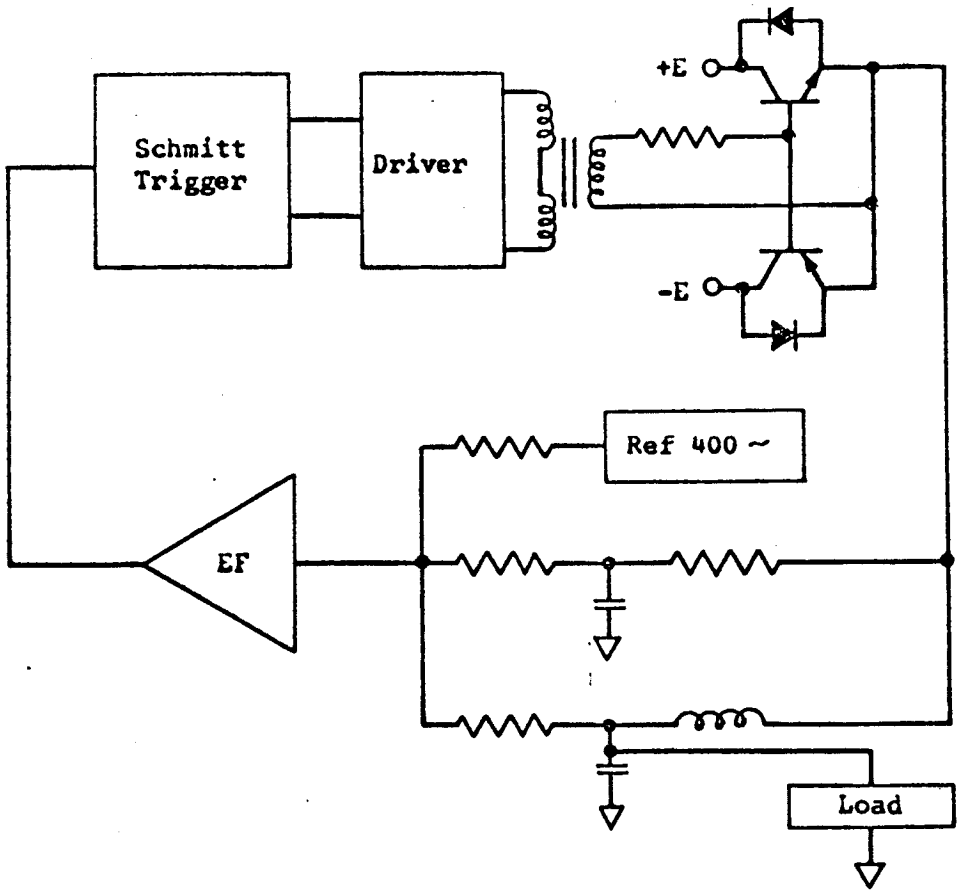


Figure 4.12

The emitter follower input provides isolation from the voltage transients seen at the Schmitt trigger input. The transformer-coupled complimentary pair are turned off by positive pulses from the Schmitt circuit and provide the required 200 mwatts for driving the power switch.

The sensor voltage will be resistively summed with the reference voltage. The resulting error voltage will modulate the integrated square wave feedback required for self oscillation.

Some minor circuit changes will be required to provide temperature compensation.

The power switch calls upon the best properties of a power transistor and a high-speed logic transistor. Referring to Figure 4.13, the transistors must have a fast switching time in order to avoid shorting the positive and negative power supplies. This implies a thin film, low base capacitance transistor.

The same transistor must turn off a maximum load current for an inductive load of about one ampere with a V_{CE} maximum of 140 volts.

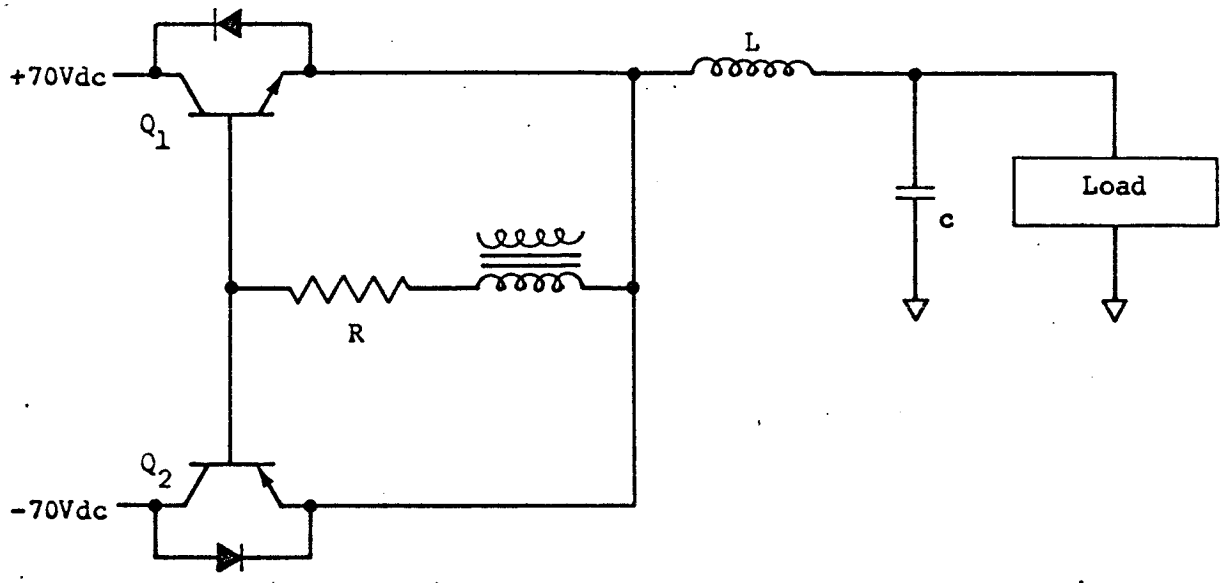


Figure 4.13

Figure 4.14 shows that the power switch must be capable of both high current and high voltage for a short duty cycle.

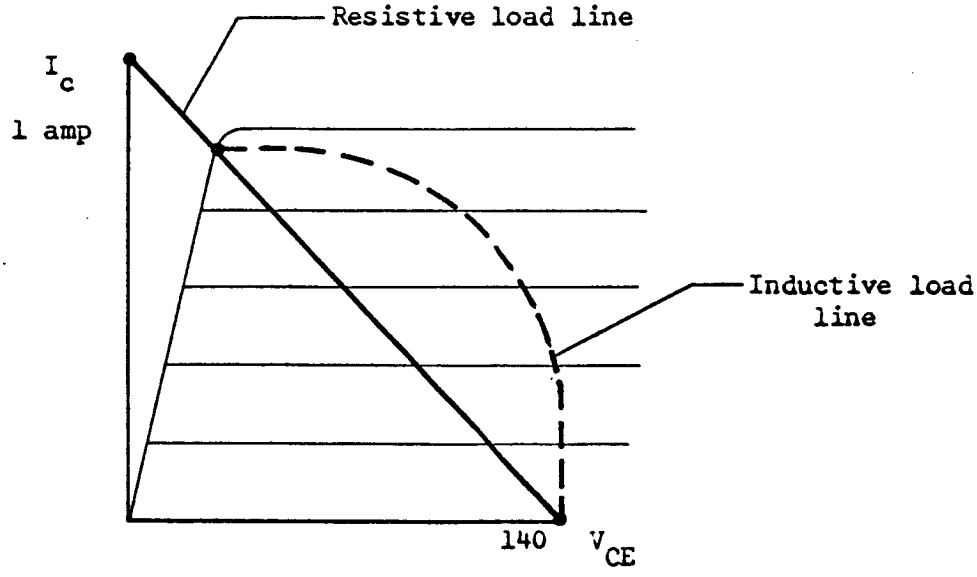


Figure 4.14

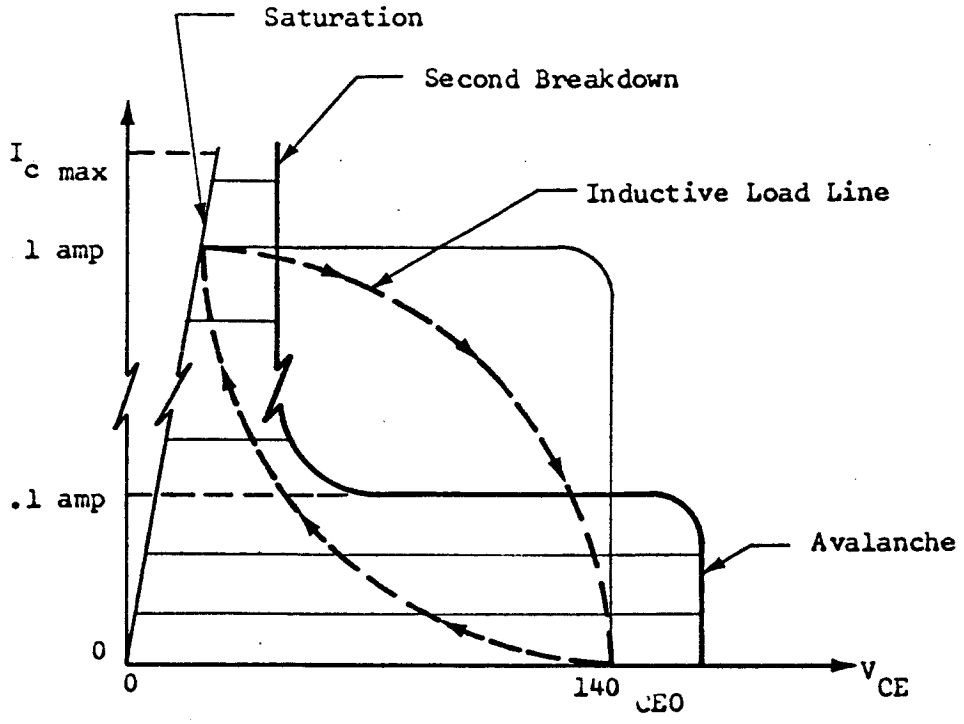


Figure 4.15

No single transistor now available can meet all the requirements for the power switch, therefore, a multiple device approach would appear the only method feasible.

A number of high current-low voltage transistors may be placed in series as in Figure 4.16.

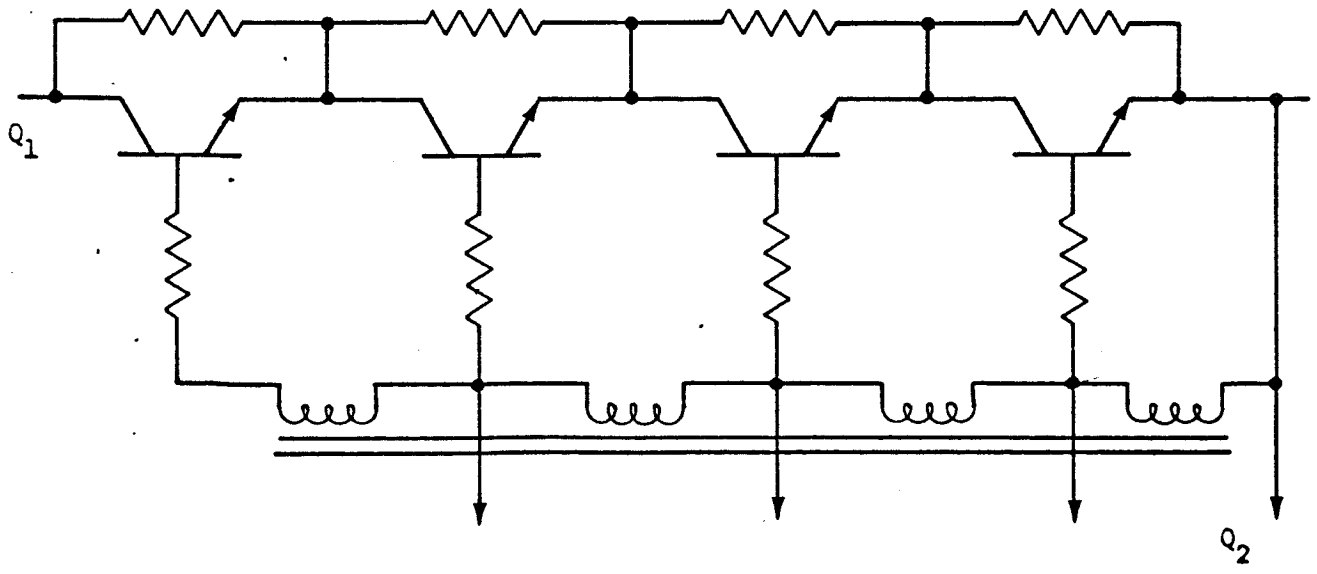


Figure 4.16

Paralleling many high speed transistors (Figure 4.17) and dividing the current between them appears to be the best solution. The transient current can be kept low and current division appears more reliable than voltage division. Secondary breakdown may also be avoided by keeping the current in each transistor below the secondary breakdown power level. However, attempts to mechanize either combination did not prove practicable. The requirement for high switching speed (i.e., low storage time) was not met for either mechanization.

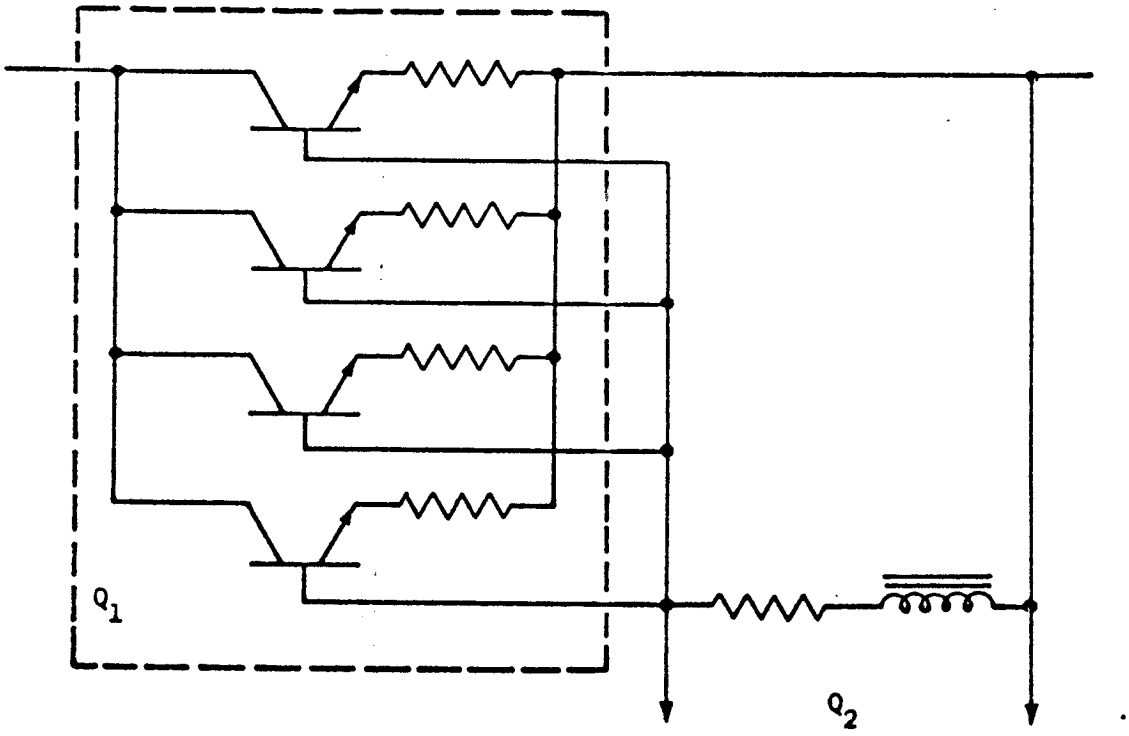


Figure 4.17

A different approach was tried. The switch problem was solved by simply using high power switching transistors and accepting the 2-5 microsecond storage time. The circuit is shown in block diagram form in Figure 4.18, and in schematic form in Figure 4.19. The system requires that each transistor be driven separately and that the turn-on of each switch is delayed until the other is off. Six to ten microseconds per cycle were allowed for the delay time. In order to achieve a high degree of modulation, the switching frequency was dropped to about 20 kc. The system functions well with a high voltage power input but because of the limited closed loop frequency response, the output was limited to 30 volts P-P.

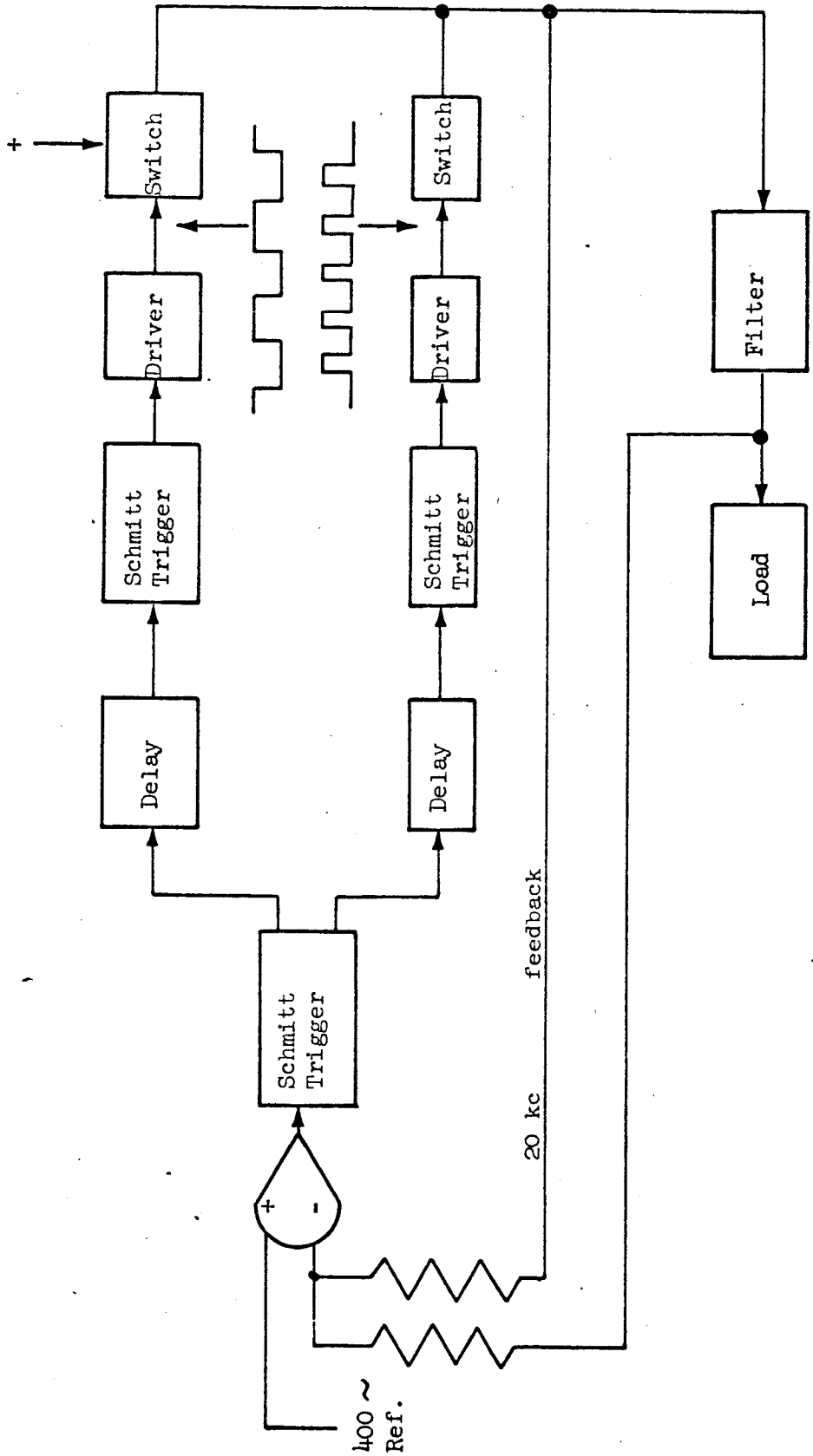


Figure 4.18 - 400 ~ Inverter, High Frequency Switch (20 kc Pulse Width Modulation)

	NAME	DATE	LOCKHEED MISSILES & SPACE COMPANY A GROUP DIVISION OF LOCKHEED AIRCRAFT CORPORATION	Page	TEMP.	PERM.
Prepared						
Checked			TITLE 400 Hz. INVERTER SWITCH CIRCUIT	Model		
Approved				Report No.		

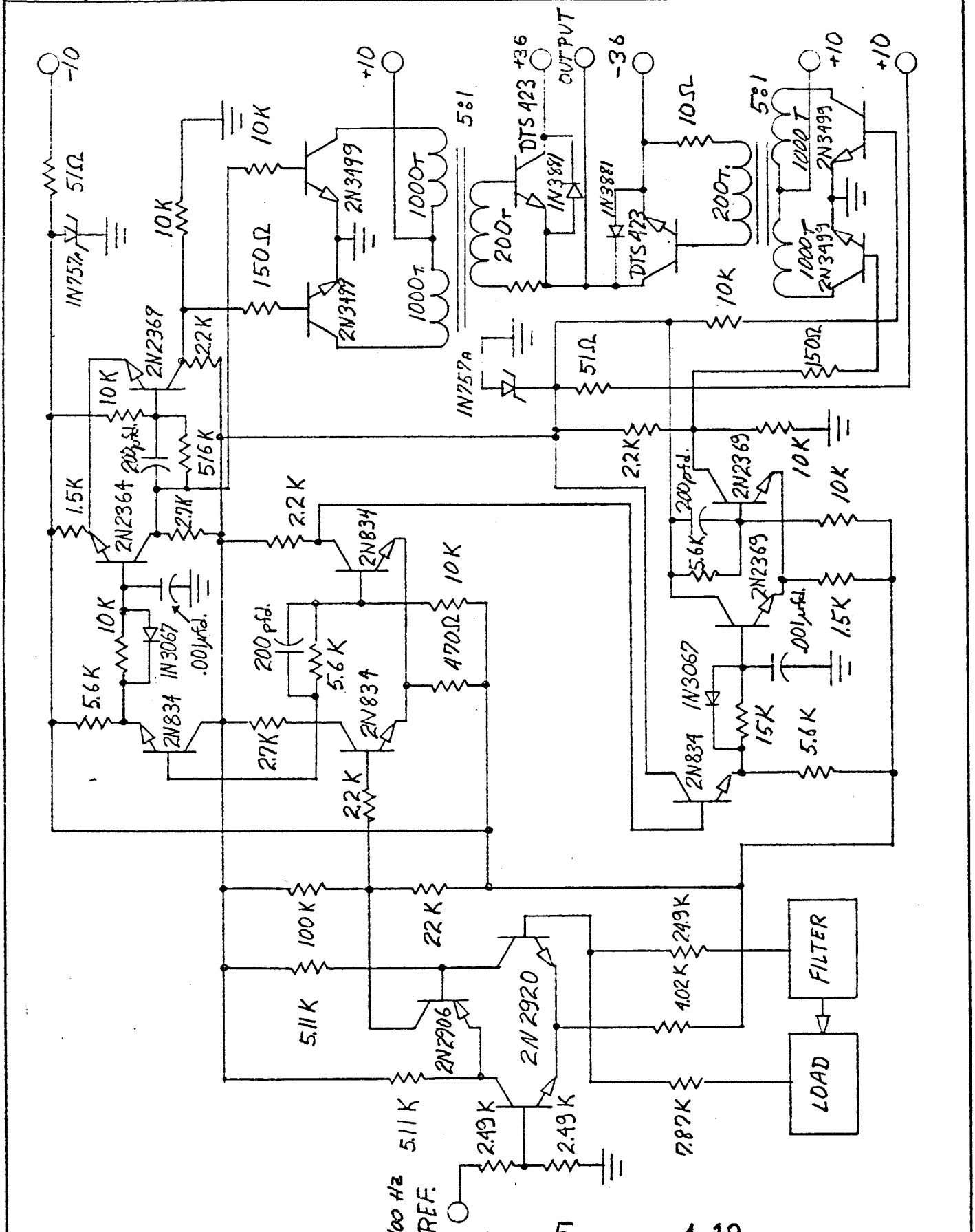


Figure 4.19

100 kc DC to DC Converter for the Inverter

The converter was mechanized utilizing a positive feedback, non-saturating output transformer for sensing when the 2N3448 transistors have turned off (stored charge removed from the saturated ON transistor) and then reversing polarity. The saturating core was used to energize the ON transistor's base until saturation; then the loss of voltage across the primary of the transformer affords a negative drive for the base, turning off the transistor. Both transistor's bases have negative bias until the output transformer switches, since the rate of change of current reverses. This is due to the increasing impedance of the ON transistor while turning OFF after removal of the storage charge. The di/dt reversal generates an opposite polarity voltage waveform.

The converter's electrical schematic is shown in Figure 4.20 and the efficiency calculations are in Table 1. Figure 4.21 shows the test setup for making the power measurements.

Results of this 400 Hz Inverter Mechanization: This mechanization finally had to be dropped. Since the switch voltage capability prevented the generation of the ± 36.8 volt peak amplitude because of the large reverse-bias requirements on the collector to base region and the operation into an inductive load causing very high power spikes during switching necessitated a reevaluation of the switching concept. The regulation requirements dictated a high gain closed loop system which required much lower corner frequencies that anticipated to stabilize the system. This then presented a sluggish response to the tracking error signal/output difference so that the high voltage output could not be achieved with necessary regulation requirements.

Final 400 Hz Inverter: The general design of this 400 Hz inverter is similar to a dc-to-dc converter with two distinct differences: (1) the error signal is held to a dynamic null by the active feedback of the difference between an externally generated 400 Hz reference oscillator and the output waveform; (2) the power is switched across a transformer at high frequency. This power is controlled on the secondary side by sensing both error magnitude and polarity of error signal synchronized with the 400 Hz reference benerated on the same secondary side of the transformer, and finally coupled to the primary side by means of a blocking oscillator. By controlling the blocking oscillator repetition rate and by the initiation of pulses, either a burst of pulses or relatively few pulses can be coupled across the power transformer by means of a unique power one-shot circuit. The duty cycle of these pulses is a direct function of the load and line demands.

Since the power transfer is accomplished in a switching mode of circuit operation, inherently high efficiency is offered with transformer size being dictated by the switching frequency. By handling the power switching on the primary side, the transformer turns ratio can be utilized to increase the voltage where necessary. Of course, the same circuit philosophy can be used to generate any arbitrary function by substituting that function for the 400 Hz reference. Natural restraints are imposed by the frequency, voltage amplitude, and power requirements.

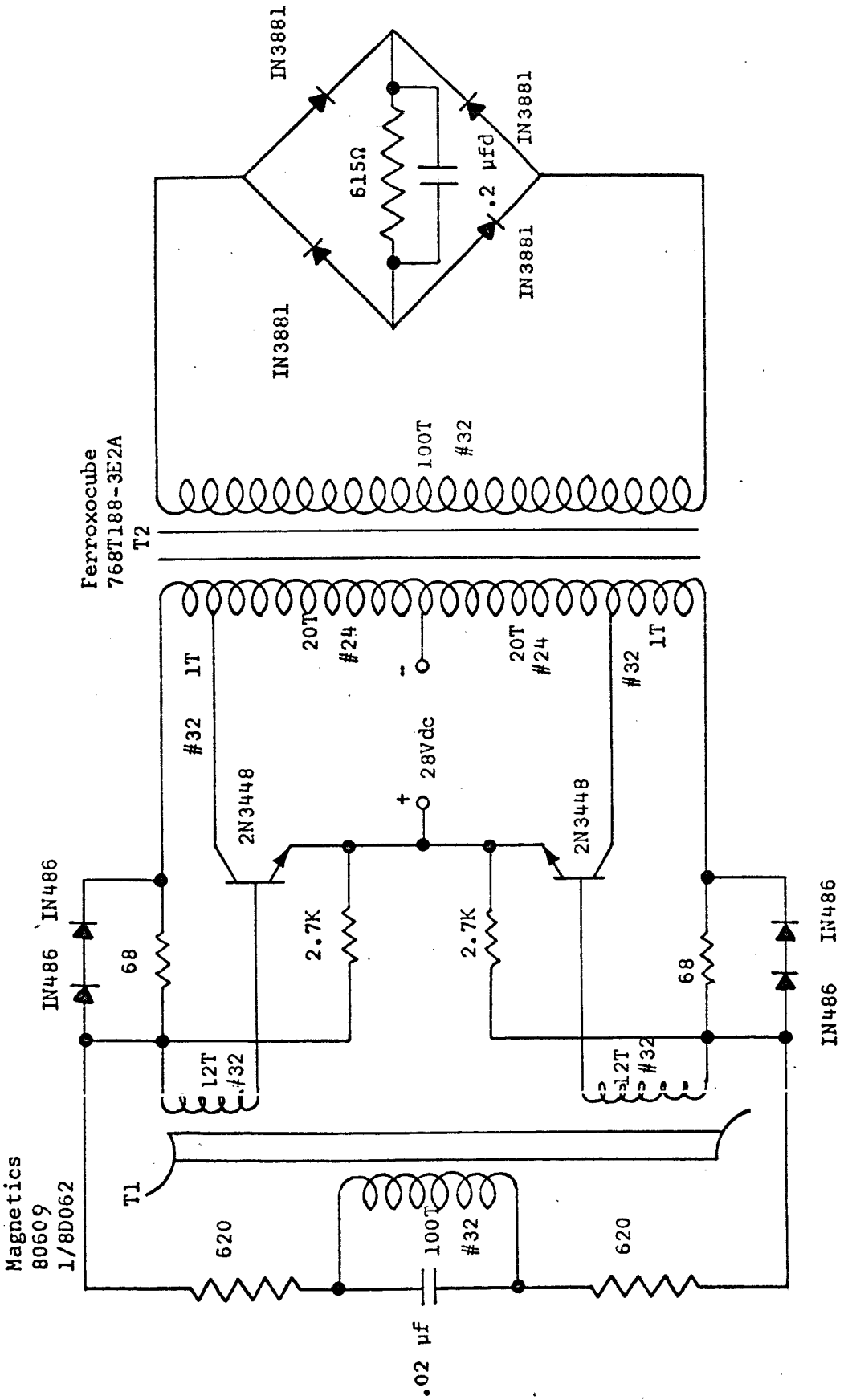


Figure 4.20 - DC-to-DC Converter

TABLE I

V_{in} (volt)	I_{in} (amp)	P_{in} (watt)	V_o (volt)	I_o (amp)	P_o (watt)	η (%)	f (kc)
23.8	1.09	25.95	116	.189	21.9	84.5	67.2
24.7	1.11	27.4	120.5	.196	23.6	86.2	68.5
25.7	1.16	29.8	125.2	.204	25.6	85.8	69.5
26.7	1.20	32.0	129.5	.211	27.3	85.1	71.5
27.65	1.22	33.75	133.6	.218	29.1	86.4	73.5
29.55	1.305	38.55	142.0	.231	32.8	85.0	75.8
31.5	1.39	43.8	150.4	.244	36.65	83.5	79.5

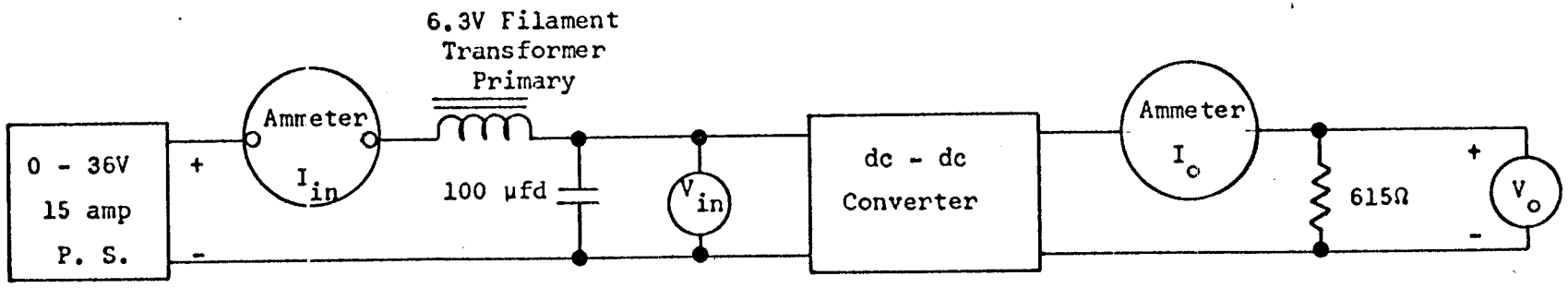


Figure 4.21- Measurement Circuit

The circuit has been laid out with the idea of utilizing presently available commercial microcircuits, both analog and digital, for substitution in most of the control and timing functions. The power switching circuitry could perhaps be manufactured in a hybrid flat-pack to reduce size and offer better matching characteristics.

Generalized Block Diagram: Figure 4.22 shows the generalized block diagram of the circuit. No attempt is made to present impedance matching and coupling circuits, but only the necessary explicit functions. Each of the functional circuits is discussed in detail.

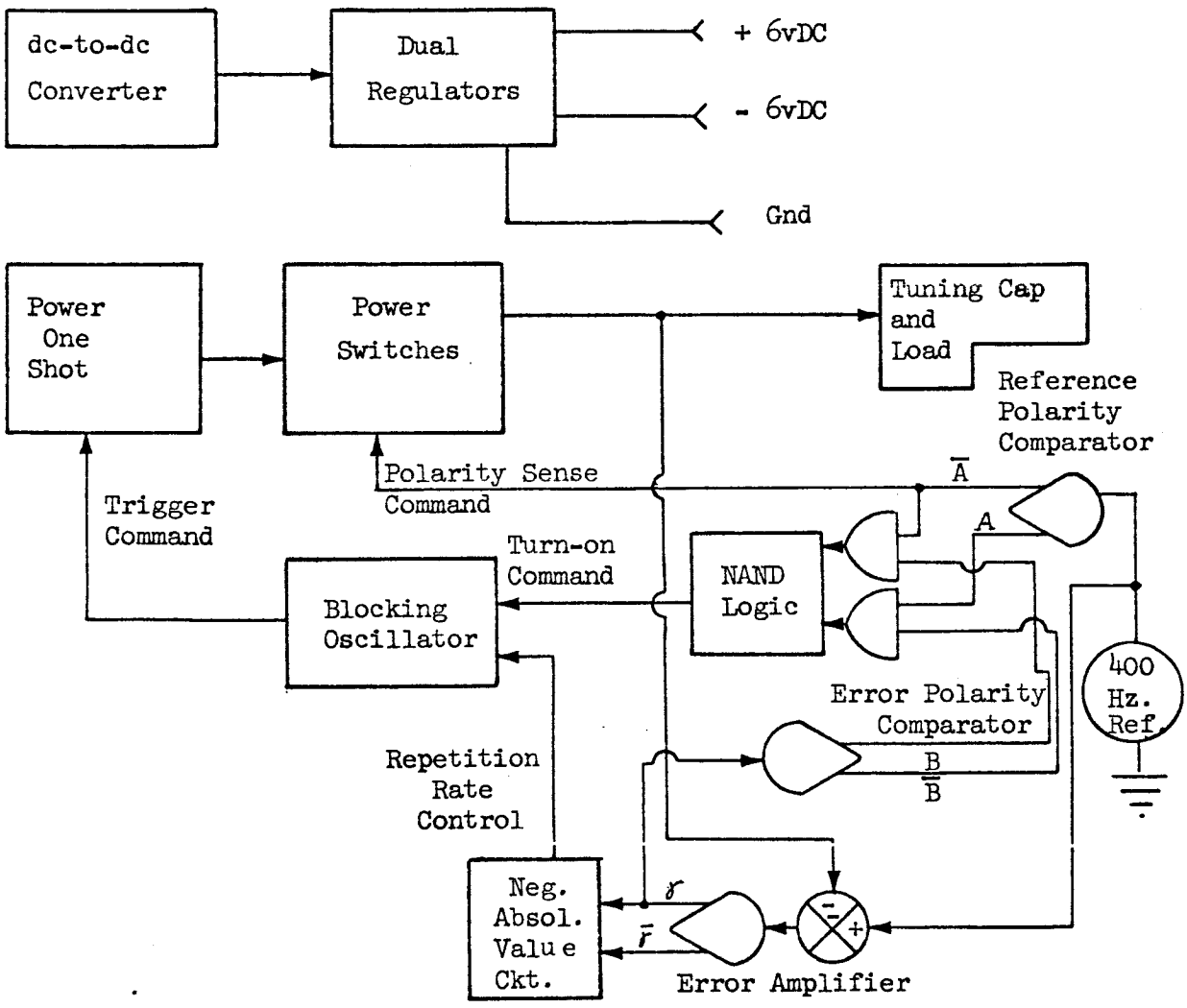


Figure 4.22

The Power One-Shot Circuit: The power one-shot circuit is shown on Figure 4.23. This circuit can best be described by explaining one complete cycle of operation. Upon command from the blocking oscillator circuit, transistor Q_5 is saturated "on" effectively connecting ground to CR7 and R9 and permitting current to flow into the base of Q2. Since the emitter of Q2 is at -V potential initially, this current is limited only by resistor R9. As the Q_2 base-to-emitter diode turns on, transistor action with heavy drive current sweeps Q_2 into saturation. Thus tap no. 16 on transformer T2 is effectively grounded and a potential of V established across primary winding 14 - 16. Simultaneously, autotransformer action establishes 2V potential at tap 12 and an even lower potential at tap 11. The initial charge across capacitor C2 is zero volts while capacitor C1 has an initial charge of V volts. As the autotransformer action pulls tap 11 negative, the zero charge across C2 transfers this negative potential to the base of transistor Q1. This response aids in holding the base-to-emitter diode of Q1 reverse-biased during this portion of the cycle. C1 meanwhile has also transferred a potential change of V plus the potential between taps 11 and 12 to the R11/C1 node. Current flows through R11 from tap 11 of transformer T2. Because the time constant of R11-C1 is 44 usec, the potential across C1 does not change appreciably during the time of interest (3 to 12 usec).

Meanwhile the emitter of Q1 is driven to -2V, the diode CR1 becomes forward biased, allowing current to flow between the emitters of Q2 and Q1 through the path, R4, T1 primary, and CR1. Energy is then transformer-coupled to the secondary side of T1 to drive the base of Q2 into saturation. This drive holds transistor Q2 in saturation until the core of T1 saturates.

The secondary of T1 connected through R1 to Q1 also holds the base of Q1 reverse-biased. Indeed, if the potential supplied by the secondary of T1 and the feedback winding of T2 (taps 11-12) are identical, no net charge will exist across C2.

As T1's core saturates, the potential which had existed across its primary and secondary windings is lost. Thus, the negative potential of -2V exists at the primary winding at the R6, C3, and R4 junction. The current is now limited by R4 alone. This increased negative potential more than overcomes the zener breakdown potential of CR4 and results in turn-on of transistor Q4. It is this drive supplied by Q4 acting through CR6 and R10 which removes the stored charge from saturated transistor Q2. Since this charge cannot be removed instantaneously, transistor Q2 remains "on" until the total charge can be removed. Therefore, current can continue through Q2 to provide the necessary energy to sustain the transformer and auto-transformer actions demanded by the load and feedback circuitry. Upon removal of this stored charge, however, the transistor action is abruptly ended. This abrupt switch opening provides a very large di/dt change in the direction to reverse all of the polarities on the windings. The major contributors to this action are the leakage reactances of T2. Note that this polarity reversal not only prevents Q2 from turning "on" but provides a positive potential to be coupled through an already positively charged capacitor C2 to forward bias Q1's base-to-emitter diode. (C2 had become positively charged during the saturation

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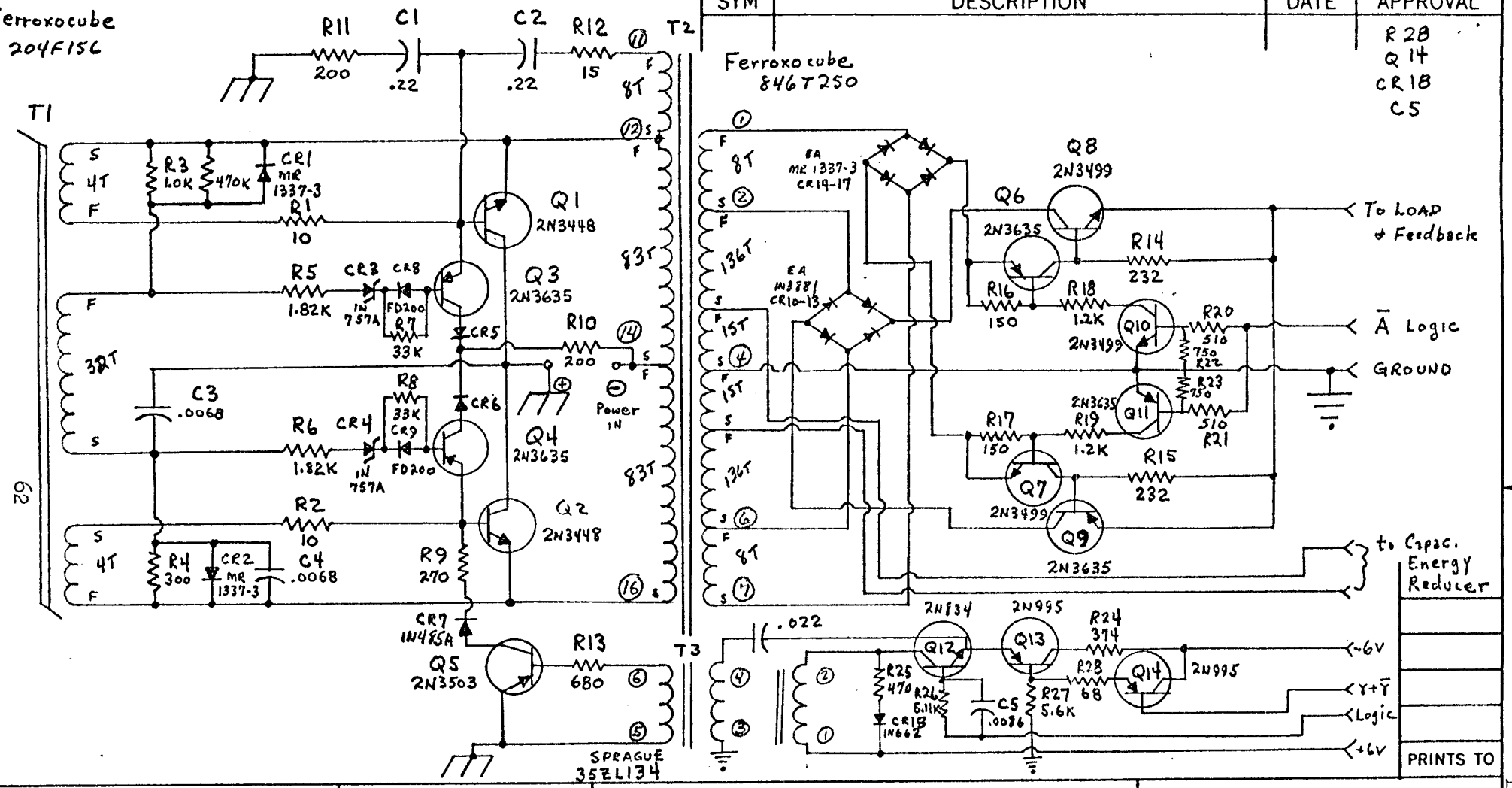
			R28 Q14 CR18 C5



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: FRACTIONS ± DECIMALS ± ANGLES ± ALL SURFACES ✓	DRAWN J. L. WESTROM	400 Hz INVERTER - Power One Shot - Power Switches - Blocking Oscillator	LOCKHEED MISSILES & SPACE CO.
	DATE 5-5-66		DIV OR DEPT
	APPD		LOCATION
	ISSUED		
MATERIAL	APPROVED / DATE		SIZE: Figure 4.23
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G-E	MFG		
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portion of the cycle when the negative potential was lost on the secondary of the drive transformer T1.) Its time constant being C2 (R1 + R12), or 11 usec.

As the autotransformer action is produced across taps 14 - 16, diode CR2 conducts, re-energizing T1 and producing voltage on the primary and secondary windings with the opposite polarity from previously. Q1 remains latched in the saturation mode until the core of T1 again saturates. Q2's base-to-emitter diode meanwhile is reversed-biased by T1's other secondary.

The second time that T1's core saturates and the voltage drive is lost produces the same type of latching action which removes the stored charge from the base region of Q1, this time through R5, CR3, and CR8 which turns on transistor Q3. Upon removal of this stored charge the switch Q1 abruptly opens, again producing the large di/dt which reverses the polarity of all windings on T2. Since there is no positive feedback winding capable of gating on Q2, the oscillation ceases. In actual practice, however, it was found that a small capacitor (C3) had to be inserted between the primary of T1 and ground to prevent regeneration of the waveform. Capacitors C4 and C5 are speed-up devices to insure rapid commutation of the switching transformer T1. C1/R11 provide load balance to the primary of T1 and a necessary load for the feedback winding of T2.

Problem Areas in the Power-One-Shot:

1. Unsymmetrical switching. Q2 is working much harder than Q1.
2. High dissipation in R11.
3. Q3 and Q4 are conducting before T1's core begins to saturate.
4. Ferrite core was used for switching core in T1. Tape wound core should provide faster switching and improved efficiency.

The Power Switches: The function of the power switches is to provide positive or negative polarity voltage to the load. The positive potential is provided by gating on Q8 by turning on the Q6 - Q10 series-connected transistors by means of a positive signal from the $\bar{A}$ signal which occurs whenever the 400 Hz reference is negative. The negative potential is provided by gating on Q9 by turning on the Q7 - Q11 series-connected transistors by means of a negative signal from the $\bar{A}$ signal which occurs whenever the 400 Hz reference is positive. The transistors operate in the saturation mode whenever they are gated "on" and are "off" at all other times. Thus, whenever the 400 Hz changes polarity, the power switches likewise switch to the opposite polarity.

Problem Areas in the Power Switches: The negative polarity portion of the power switches are not operating in the saturation mode. Instead, whenever the power one-shot fires, they are pulled into their active linear region which is a high dissipation area. This hurts the efficiency as well as reduces reliability.

The Blocking Oscillator: The blocking oscillator circuit (Figures 4.23 and 4.24) controls the initiation of the power one shot's output pulse pairs as well as the spacing between pulse pairs. The spacing between pulses or repetition rate is controlled by an analog signal coming from the "absolute value circuit" which provides only the negative portion of the amplified error signal. Thus, when a null or very small error exists, the repetition rate command receives no contribution from the absolute value circuit. However, R27 establishes a minimum repetition rate of 5kHz. Although the rate is controlled by the analog error signal magnitude, the actual triggering of the blocking oscillator is accomplished with binary NAND logic. This logic physically shorts and opens the base control of Q12 which provides the drive for the oscillation. This is shown at the R26/C5 junction. The blocking oscillator's output transformer T3 (pins 6 - 5) couple the pulse to the base of Q5. The negative going waveform saturates Q5, effectively shorting the base of Q2 to ground through CR7 and R9.

The 400 Hz Reference: American Time Products, Frequency Standard: Type 10 consists of a subminiature tuning fork made of iso-elastic material, a drive and a pickup system, a transistor and associated circuitry. An internal voltage source of 1.2 to 1.6 volts dc is supplied with 6 VDC applied across R29 and the required voltage dropped across two forward biased diodes, CR19 and CR20, which are in parallel with the 400 Hz reference input, the red terminal (see Figure 4.25). The case of the device must be grounded, and the yellow terminal supplies the reference 400 Hz output with a peak amplitude of $\pm$ 0.10 volts.

Since the current required from the output terminal exceeds 3 uamp, it is necessary to insert a 0.1 uf coupling capacitor between this terminal and the Darlington buffer amplifier. This capacitor could be eliminated and the Darlington buffer obviated by utilizing a field effect transistor as the buffer.

Reference Buffer Amplifiers: Because of their off-the-shelf availability, transistors were used in Darlington connections to provide the impedance buffer needed to prevent loading down the reference (see Figure 4.25). Also, because of the inherent high gain, the first buffer stage also provides a voltage gain of 20 to the reference amplitude. This signal is capacitively coupled to a second Darlington amplifier which impedance converts this signal to a low output impedance (less than one ohm). This signal then drives two high gain differential amplifiers, A1, the 400 Hz comparator and A2, the difference amplifier.

400 Hz Comparator: This circuit (Figure 4.26) consists of a high gain dc amplifier which in the final configuration could easily be an off-the-shelf micro-circuit. The circuit function is to provide a large voltage of opposite polarity to the 400 Hz input. Two output channels are required, the one channel being the complement of the other. For brevity these channels are noted as A and $\bar{A}$ on Figure 4.26. The A channel provides a $\pm$ 4 volt output square wave which is 180° out of phase with the reference input. The $\bar{A}$ channel is in phase with the reference input. The $\bar{A}$ channel drives the power switch,

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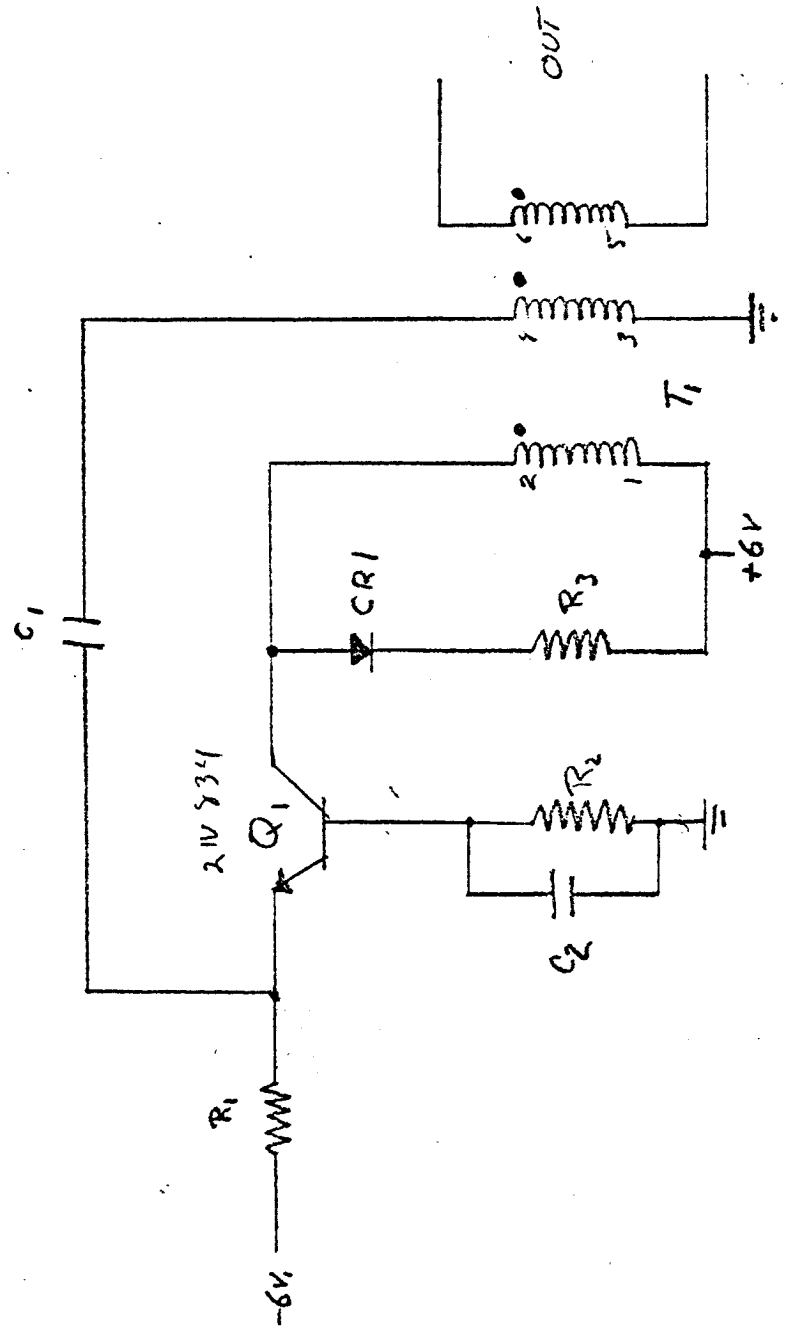
Fig. 4.24



$CR1 = 1N662$
$T_1 = SPRAGUE\ 35\#L134$

$C_1 = .02\mu F$
$C_2 = .008\mu F$
$Q_1 = 2N834$

$R_1 = 1.07K$
$R_2 = 5.11K$
$R_3 = 470\Omega$

Fig. 4.24

CR 19 - 20
Q 15 - 18
C 7 - 8
R 29 - R 43
A1 - A3
FS - 1

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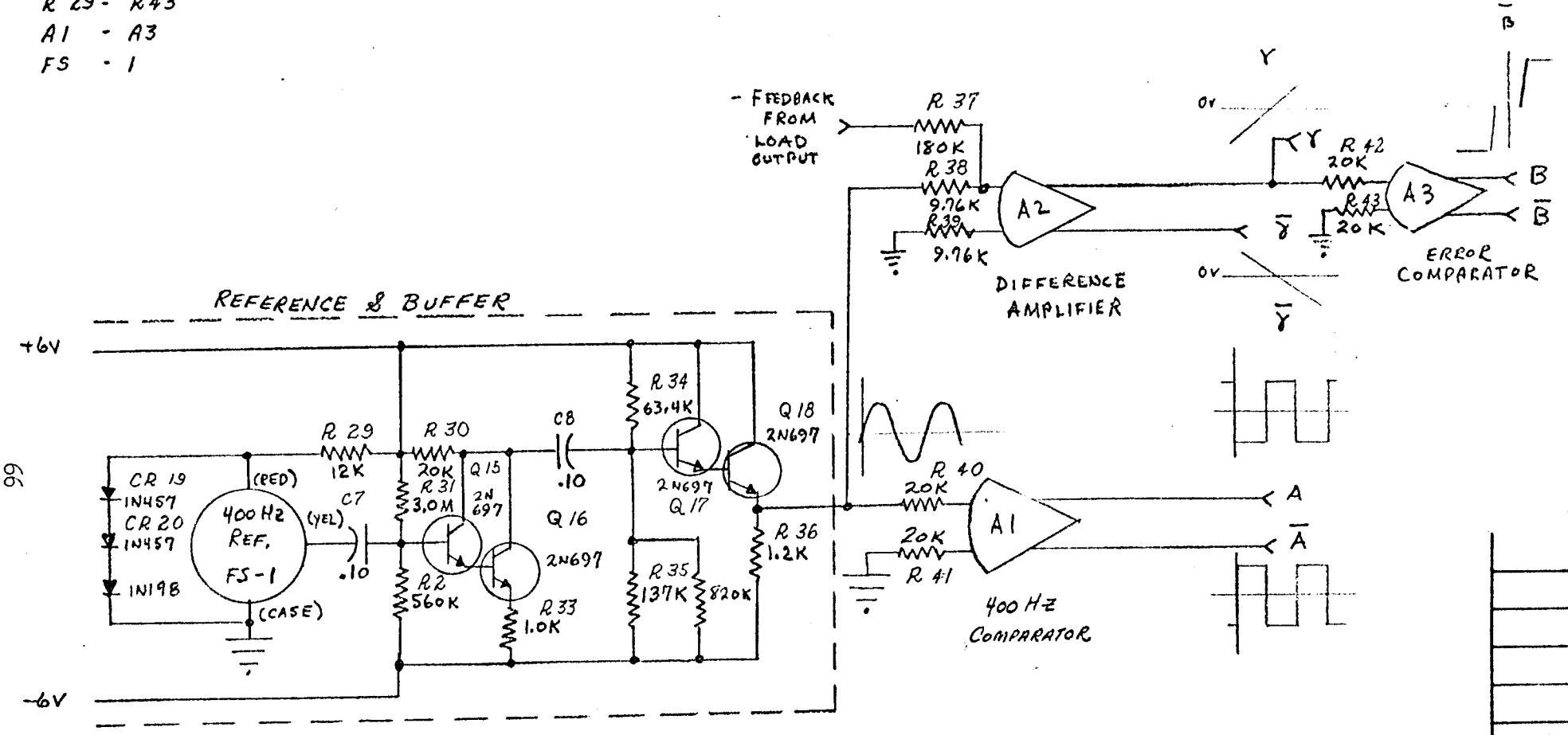

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400 Hz INVERTER REFERENCE/BUFFER AND ANALOG BUILDING BLOCK LOGIC

SCALE WT CALC ACTUAL

LOCKHEED MISSILES & SPACE CO.
DIV OR DEPT
LOCATION

SIZE Fig 4.25

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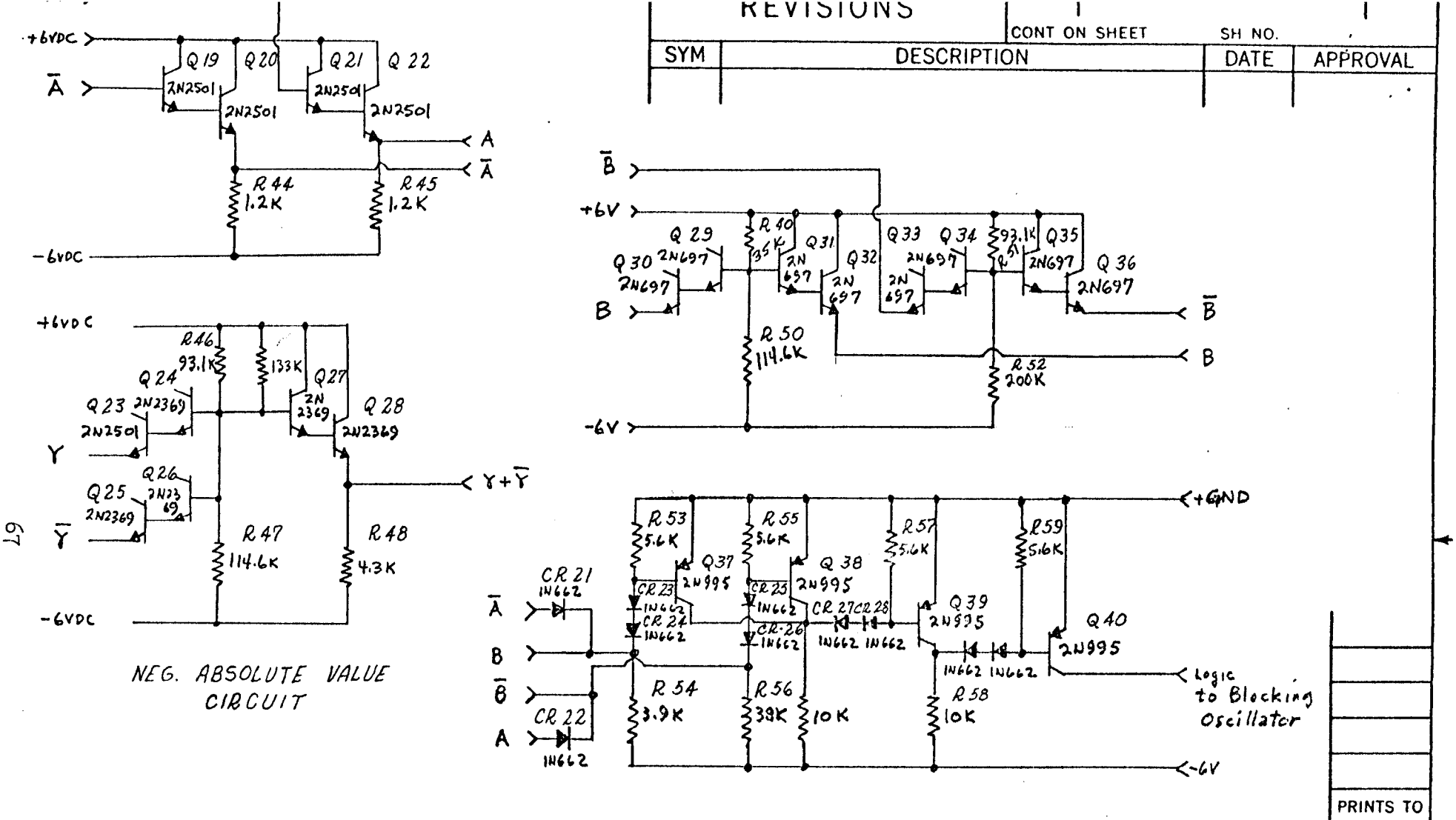

NEG. ABSOLUTE VALUE CIRCUIT

67

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400 Hz Comparator

Analog Building Block Logic Buffers & Blocking Oscillator Logic

LOCKHEED MISSILES & SPACE CO.
DIV OR DEPT
LOCATION

SIZE Fig 4.26

SCALE | WT CALC ACTUAL | CONT ON SHEET | SH NO.

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is used in the capacitive energy reducer trigger circuitry, and is used in the logic turning on the blocking oscillator trigger pulses. The A channel is used in the logic circuitry as well.

The Difference Amplifier: This circuit (Figure 4.26) also consists of a high gain dc amplifier. It could be an off-the-shelf micro-circuit. The circuit compares the difference between the reference input and the load output voltage waveform. As the output waveform deviates from the desired reference waveform, a difference error signal is generated and amplified by the difference amplifier (A2) (see Figure 4.25). Two output channels are required for use in the circuitry, one output being the complement of the other. These outputs are identified on Figure 4.25 as δ and $\bar{\delta}$. The δ and $\bar{\delta}$ outputs are used to provide the negative absolute value circuits inputs, and also for driving the error comparator (A3) (see Figure 4.25).

The Error Comparator: This circuit also consists of a high gain, dc amplifier (A3) (Figure 4.25). It could be an off-the-shelf micro-circuit. This circuit provides a large voltage ($\pm$ 4 vdc) of opposite polarity whenever an error voltage exists at the output of A2 on the δ channel. Two separate complementary channels are required for outputs on the error comparator. They are labeled B and $\bar{B}$ on Figure 4.25 and 4.26. These channels are both used in the binary logic used to trigger on the blocking oscillator. The B channel is also used in the capacitive energy reducer circuitry.

Buffers for the Analog Building Block Logic: To prevent loading down of the high gain dc amplifiers used to generate the analog logic, it was necessary to provide buffer amplifiers which are shown on Figure 4.26. In order to overcome the emitter-to-base diode offset voltages in these Darlington-connected amplifiers, it was necessary to use similar diode drops as coupling devices from the dc amplifiers to the Darlington devices. This was done on the δ and $\bar{\delta}$ and the B and $\bar{B}$ channels. The A and $\bar{A}$ channels, however, were preset by hand-selecting their output load resistors to null at the necessary off-set voltage. The first method of controlling the offset is preferable because of the relative ease of providing the match, as well as the excellent tracking accuracy and similar temperature coefficients. This entire buffer problem can be obviated by providing higher output current capability on each micro-circuit amplifier, i.e., 20 ma output current devices would be more than sufficient to drive the necessary loads without buffering.

The NAND Logic for Triggering the Blocking Oscillator: This is another area in which commercially available microcircuits can be used to advantage. Four simple NAND gates are interconnected in series/parallel combination to provide the necessary logic function for triggering the blocking oscillator. At present PNP logic is used; however, the normal NPN NAND logic can also be performed with an increase in the number of gates necessary.

To understand the performance of this logic, realize that each time the RC circuit in the base path of Q12 in Figure 4.23 is shorted to ground, a

trigger pulse is initiated. If the RC circuit remains shorted to ground, a continuous train of pulses occur at the repetition rate determined by actual analog error ($\gamma + \bar{\gamma}$). Observe in Figure 4.27 that the output waveform is superimposed upon the reference waveform with each scaled to a similar magnitude and phase. This waveform will be used to explain each logic sequence.

Assume initially that the reference waveform and the output are in synchronism. Since the error signal (γ) is zero at this point, B is also zero while A, being independent of γ, is negative. Of course each of these channels has a complement which simultaneously has inverted polarity ($\bar{A}$, $\bar{B}$ and $\bar{\gamma}$).

The reference of course is a sinusoidal function and therefore is changing magnitude as well as polarity of the course of one Hz. At this time the reference is increasing in a positive sense, while the output voltage (since it has received no energy from the power one shot) is either at zero potential or decaying toward zero potential (with respect to ground). The difference signal and its inverted output ($\bar{\gamma}$) is increasing and when this magnitude overcomes the inherent hysteresis of A3 input the B and $\bar{B}$ channels are driven from zero to their saturated positions which in this instance are a negative 4 volts for B and a positive 4 volts for $\bar{B}$. The NAND logic which commands the blocking oscillator pulse turn-on has been designed to provide the binary "on" function whenever a negative potential is presented at the input to one of the input gates. At this time, $\bar{A}$ is positive and effectively latches the $\bar{A}$ or B gate to a positive potential holding this gate "off". $\bar{B}$ however is negative once the hysteresis has been overcome. Since A is also negative its path to the gate is blocked by the series diode and prevents its interference with the logic gating. Therefore, during the portion of the reference cycle in which channel A is negative, the $\bar{B}$ channel controls the blocking oscillator pulse initiation.

Note that as full voltage occurs on the reference waveform, that the output will require no additional input energy from the power one shot. This assumption is valid only for the case of resistive load. This case is considered here to simplify the qualitative discussion. At some point past this maximum reference waveform, the energy supplied from the filter capacitor to the load will exceed the requirements expressed by the reference waveform. Here the error output channel ($\bar{\gamma}$) changes polarity and after the system deadband is exceeded $\bar{B}$ changes from zero to a positive potential. Now the $\bar{B}$ channel turns off the NAND logic with this positive potential in effect telling the power one shot that no more power is required. This same command however will turn on the capacitive energy reducer. The reducer circuit provides an additional energy sink for absorbing the filter capacitor's energy thereby allowing a more rapid RC decay. In the case of the inductive load, the energy stored in this field will also attempt to alter the output waveform. This will be discussed later.

When one half cycle has been completed by the reference, the polarity of A and $\bar{A}$ channels reverse. This reversal causes the A or $\bar{B}$ channel into the logic gates to be gated "off". The $\bar{A}$ or B channel can turn on the power one-shot only when B goes negative. From Figure 4.27 this can occur whenever the reference waveform is more negative than the output waveform. Thus, logical

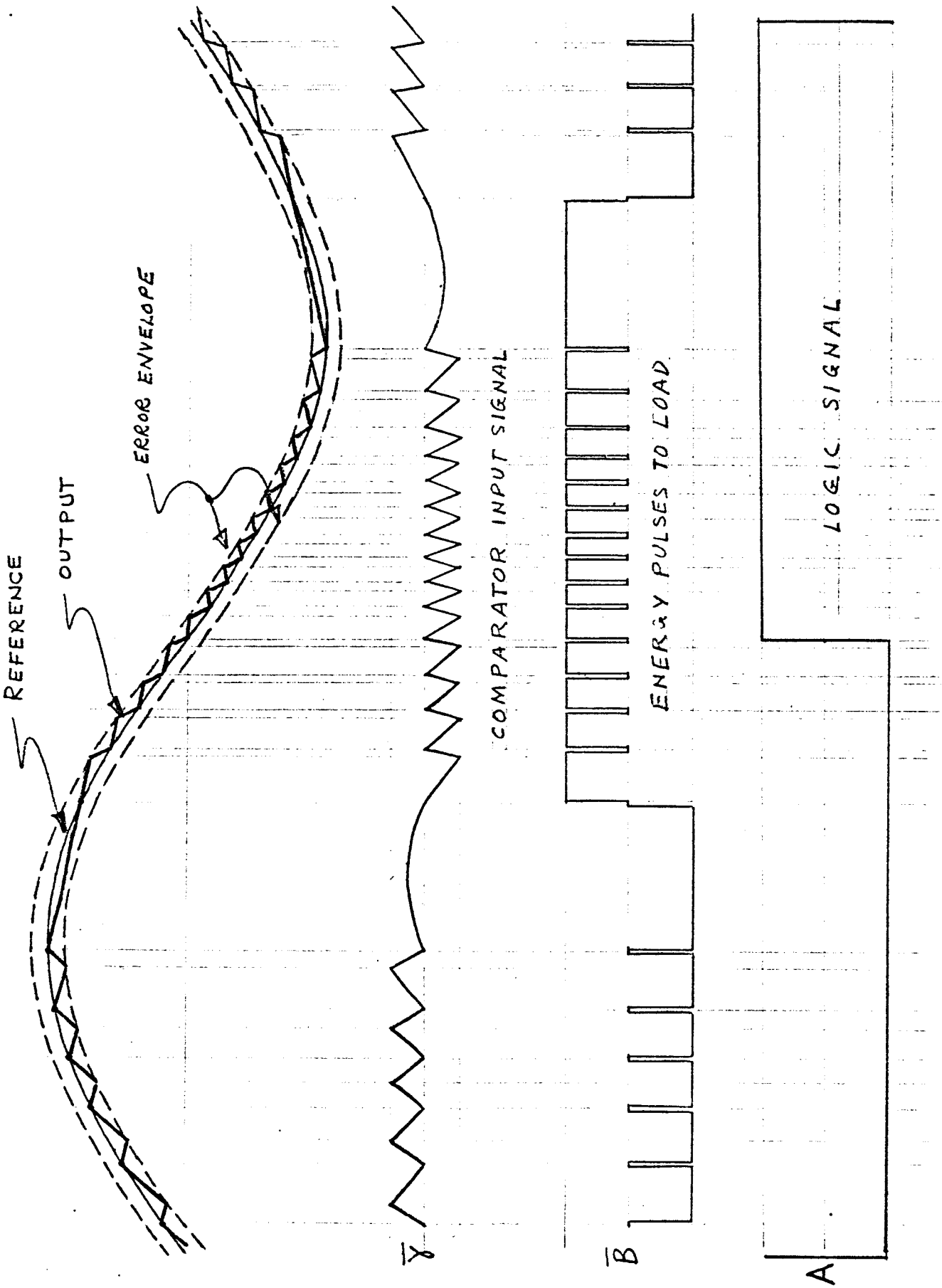

Figure 4.27 400 Hz Inverter Significant Waveforms

symmetry has been established for both polarities of the 400 Hz waveform. The waveform output again tracks the reference with the same deadband-induced ripple sensitivity apparent on the positive half-cycle. As the maximum negative magnitude is reached, the filter capacitor again discharges into the load, the error polarity changes, preventing the turn on of the power one-shot, and when B changes from negative to positive polarity, the capacitive energy reducer is again activated in rapid sequences to reduce the energy content in the filter and thereby track the reference input. This logic senses the fact of low output voltage magnitude with respect to the reference voltage in either polarity regions. When this low magnitude exceeds the system threshold, the logic commands the turn on of the power one shot, and when B changes from negative to positive polarity, the capacitive energy reducer is again activated in rapid sequences to reduce the energy content in the filter and thereby track the reference input. This logic senses the fact of low output voltage magnitude with respect to the reference voltage in either polarity region. When this low magnitude exceeds the system threshold, the logic commands the turn on of the power one shot through the blocking oscillator function.

The Capacitive Energy Reducer Function: Before observing the method of operation for the capacitive energy reducer, consider the actual requirements imposed upon the power sources by the load when an inductive component is present. These requirements are depicted graphically in Figure 4.28. The diagram assumes that power is available from the source whenever demanded.

Figure 4.29 shows the same load and filter, but the power source is switched in at a rate dependent upon the tracking deadband inherent in the reference-to-output waveform. The load current is held smooth and continuous because of the high series impedance value of the load inductance at high frequency.

When a larger-than-required filter capacitor is present, the load is no longer tuned efficiently. Not only is resistive power dissipated, but the reactive component seen by the source will hold the output voltage above the required reference waveform on the capacitive discharge portion of the cycle. If tracking is to be achieved, this additional energy must be removed. The capacitive energy reducer provides this function as shown in Figure 4.30. The electrical schematic is shown on Figure 4.31.

Figure 4.31 shows the electrical schematic of the capacitive energy reducer. This circuit consists mainly of complementary NAND logic for operating during either waveform polarity and the proper coupling gates and output drivers.

The $\overline{A}$ function provides either a positive or negative 4 volt command into the emitter-follower Q26. A positive command turns on Q23 and holds Q22 off while a negative command performs the complementary result. By turning on the gate Q23, Q21 is turned off, Q19 is turned on, which turns on Q17 thereby holding off the driver Q15. However, this logic is modified by the gate Q25. If the B channel is zero or +4 volts the logic function at Q21 is not altered. When B changes to -4 volts, this response is emitter-coupled through Q27 to the

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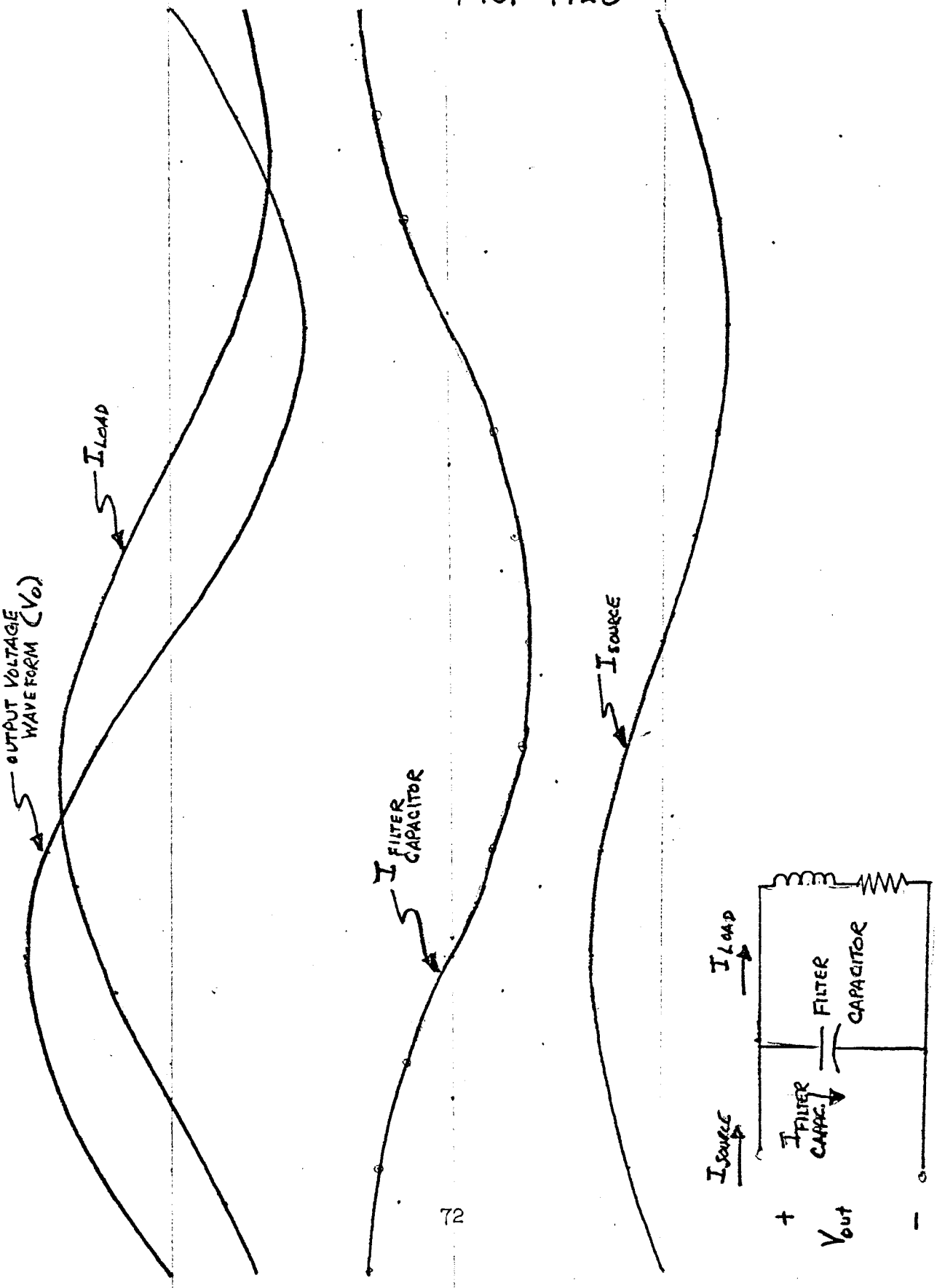
FIG. 4.28



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Checked			TITLE 400 Hz INVERTER SWITCHING EFFECTS UPON TUNED LOAD CURRENT DEMANDS	Model		
Approved				Report No.		

FIG. 4.29

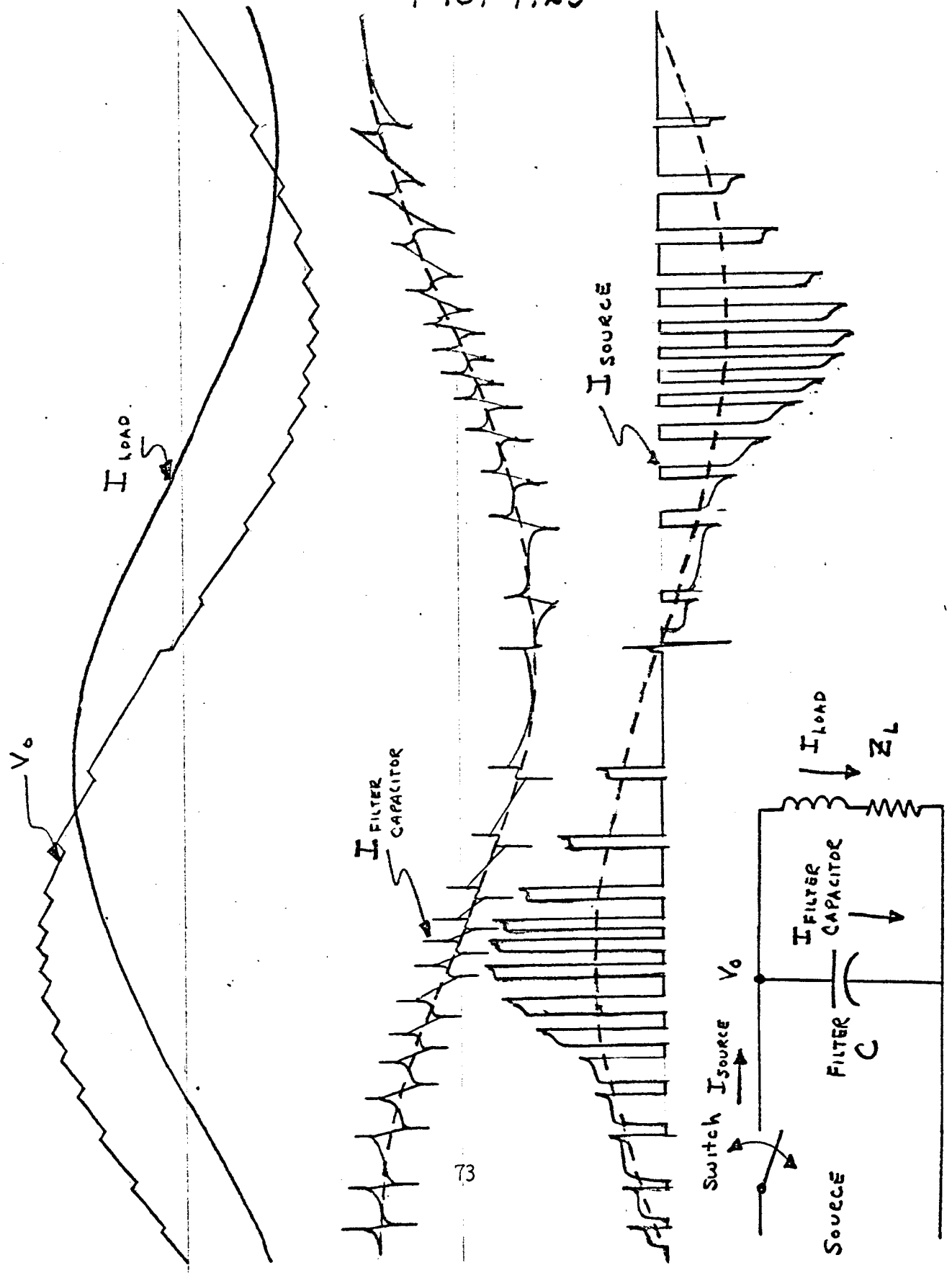

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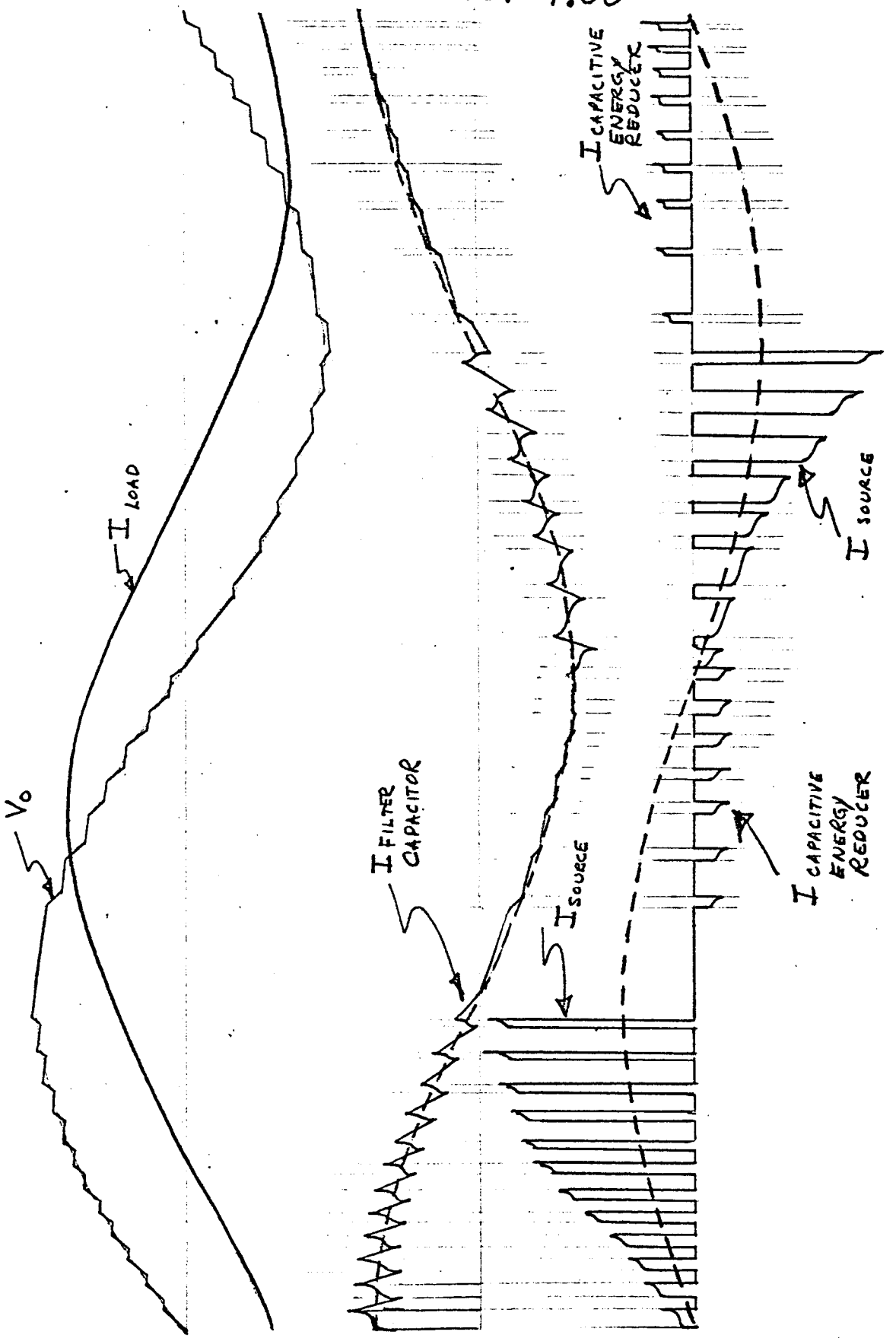
FIG. 4.30



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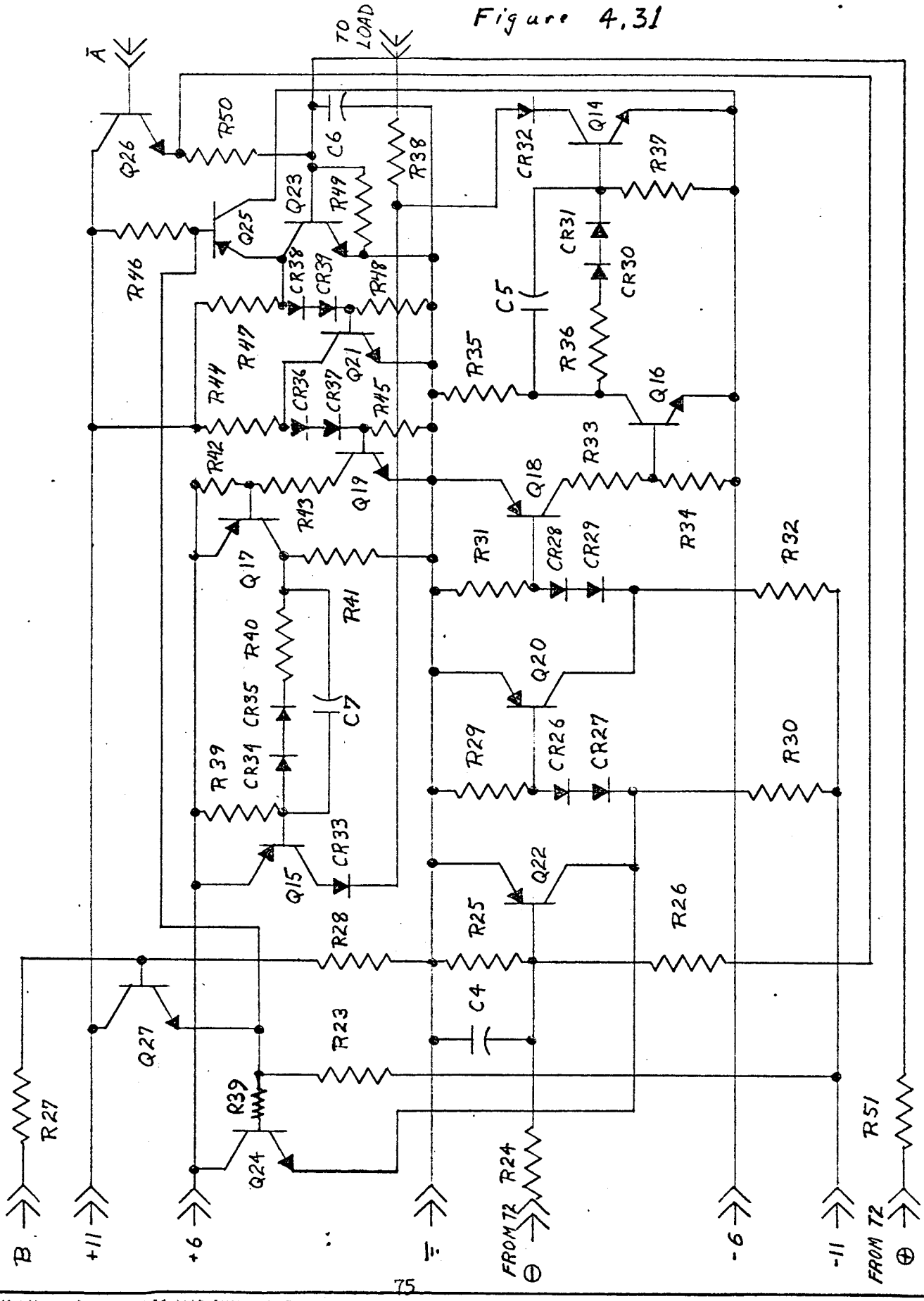
Checked			TITLE 400 Hz. CAPACITIVE ENERGY REDUCER	Model		
Approved				Report No.		

Figure 4.31



base of Q25. Since this is a pnp transistor, current will flow from the more positive emitter into the negative base region turning on a negative source at the collector of Q25. This will pull the collector of Q23 negative and current will flow through the collector base diode while the base-to-emitter diode of Q23 becomes reverse-biased. Q21 still remains held off.

When $\overline{A}$ is positive, Q22 is helf off, and the gating logic depends upon the polarity of channel B. When B is positive or zero potential, this voltage emitter coupled through Q24 holds Q20 off. This action holds on Q18 and Q16 which prevents the driver Q14 from turning on. When channel B goes negative, the logic reverses and the driver is gated on. Therefore, when $\overline{A}$ is positive and B is negative the driver Q14 is turned on; effectively shorting the output load and filter through a 200 ohm resistor (R38) to a negative 6 volt buss. Since the output is positive during this portion of the cycle, a rapid discharge of the filter capacitor's energy results. When the error voltage (δ) drops within the deadband threshold, B resumes a zero potential and the driver switch opens again.

A negative value of $\overline{A}$ holds Q23 off so that B again controls the logic necessary for energizing Q15 (driver). A negative $\overline{A}$ turns on Q22 effectively holding Q20 off regardless of the polarity of B. Otherwise, when $\overline{A}$ is negative so that Q22 has been saturated to ground, the emitter of Q24 and Q27 will not rise above -0.3 and +0.3 volts respectively, regardless of how far positive channel B goes. This would change the logic since a positive value of B is necessary to gate "on" Q21.

Performance of the Inverter: The inverter circuit has been mechanized as a breadboard model in early May of 1966. Although the attempt was to mechanize and not optimize, its operation resulted in 50% overall efficiency at nominal (28 volts dc) input voltage for a 10 watt load. Because this mechanization involved using available hardware including semiconductors, the transistors used in the power switch area (see Figure 4.23) do not exhibit an attractive h_{FE} for switching at the current levels necessary. They exhibit about a 3 to 5 gain at 500 ma collector current. As a result the drive circuitry does not provide sufficient drive to saturate them at full load. When better switches were substituted (h_{FE} of 8) the efficiency was improved to 63%. Before the circuit can be fully tested for environmental operation, a better complementary, high voltage set of switches must be found for operation at 500 ma.

4.2 DC to DC Converter

A 60 volt DC power supply was designed and breadboarded which utilized the switching regulator technique for load/line regulation. However, instead of supplying the switching type pass transistor in the secondary side of the power transformer, the dc-to-dc chopping transistors utilized for transferring the energy across the transformer windings and stepping up the voltage were also prevented from oscillating upon command from inhibit circuitry in the primary. A block diagram of this circuit is shown on Figure 4.32.

The circuit operation is as follows: at turn-on, the dc-to-dc converter gradually charges the filter. When the voltage across the load reaches a preset magnitude, the error voltage now generated is enough to turn-on the

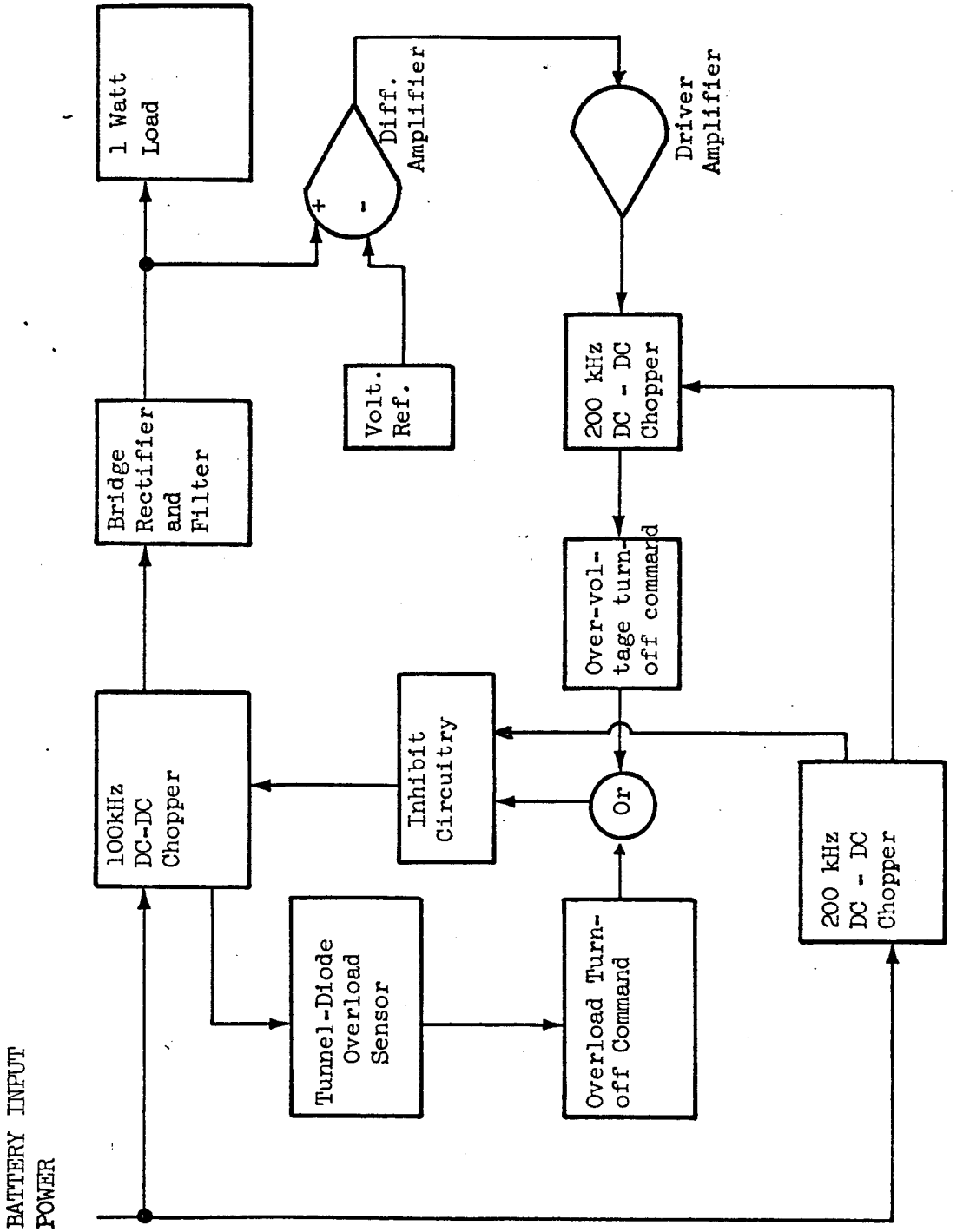


FIGURE 4.32 - Block Diagram of 60VDC Power Supply

200 kHz chopper acting through the difference amplifier and the driver amplifier. The voltage transferred back to the primary side of the circuit is filtered and rectified, supplying a DC voltage necessary to energize the inhibit circuitry thus preventing the 100 kHz chopper from oscillating until this voltage is removed.

Tunnel diode circuitry is used to sense an overcurrent condition (1N2934's). When the current exceeds 120 ma these diodes are triggered onto their higher voltage state. This voltage is enough to back-bias the base-to-emitter diodes of each of the chopping transistors, preventing oscillation and effectively shutting down the circuit. After a reasonable time delay set by an RC time constant in the overload turn-off command circuit which had simultaneously latched on, the inhibit condition is removed and oscillation allowed to continue. If the overload exists, the circuit again shuts the system down.

The general waveforms are shown in Figure 4.33 and the following Figure 4.34 shows the actual schematic of the circuitry. Although this circuit was mechanized, it was decided by NASA that the total number of cores necessary to achieve mechanization (3) reduced the desirability of the circuit from the package size standpoint. Also, because two separate bias voltages had to be supplied by one of the additional cores, it was also felt that circuit component count and thus the reliability of the system suffered needlessly when the more normal type switching regulator performance was used as a comparison. At this point the mechanization was dropped and since NASA's present 60 volt supply already utilized a switching regulator for its mechanization as did the dual power supply, it was felt that the only path open was to present a detailed analysis of the switching regulator design. This analysis is presented in the following section (4.3).

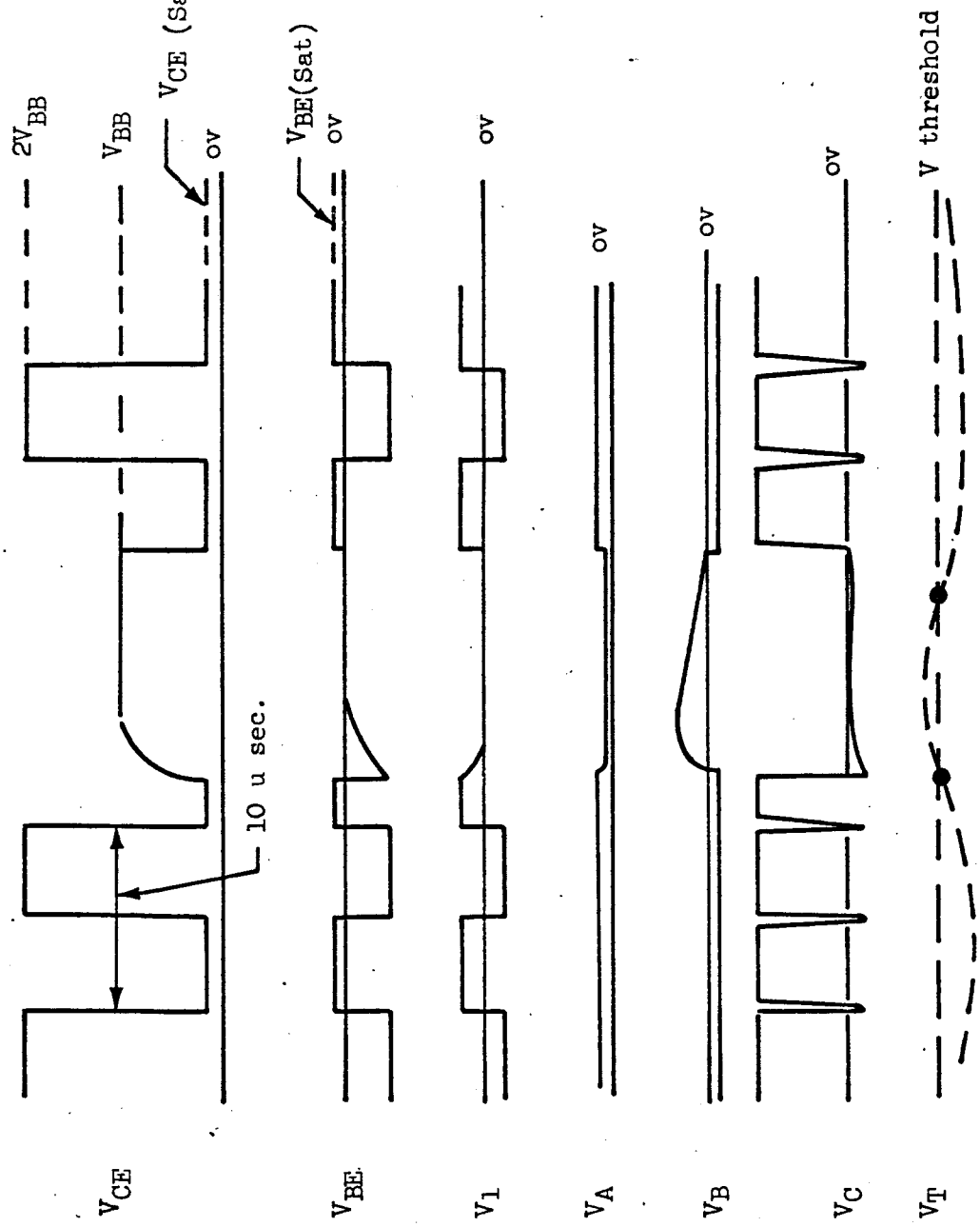


Figure 4.33 - Waveforms for Pulsed Inhibit Circuit

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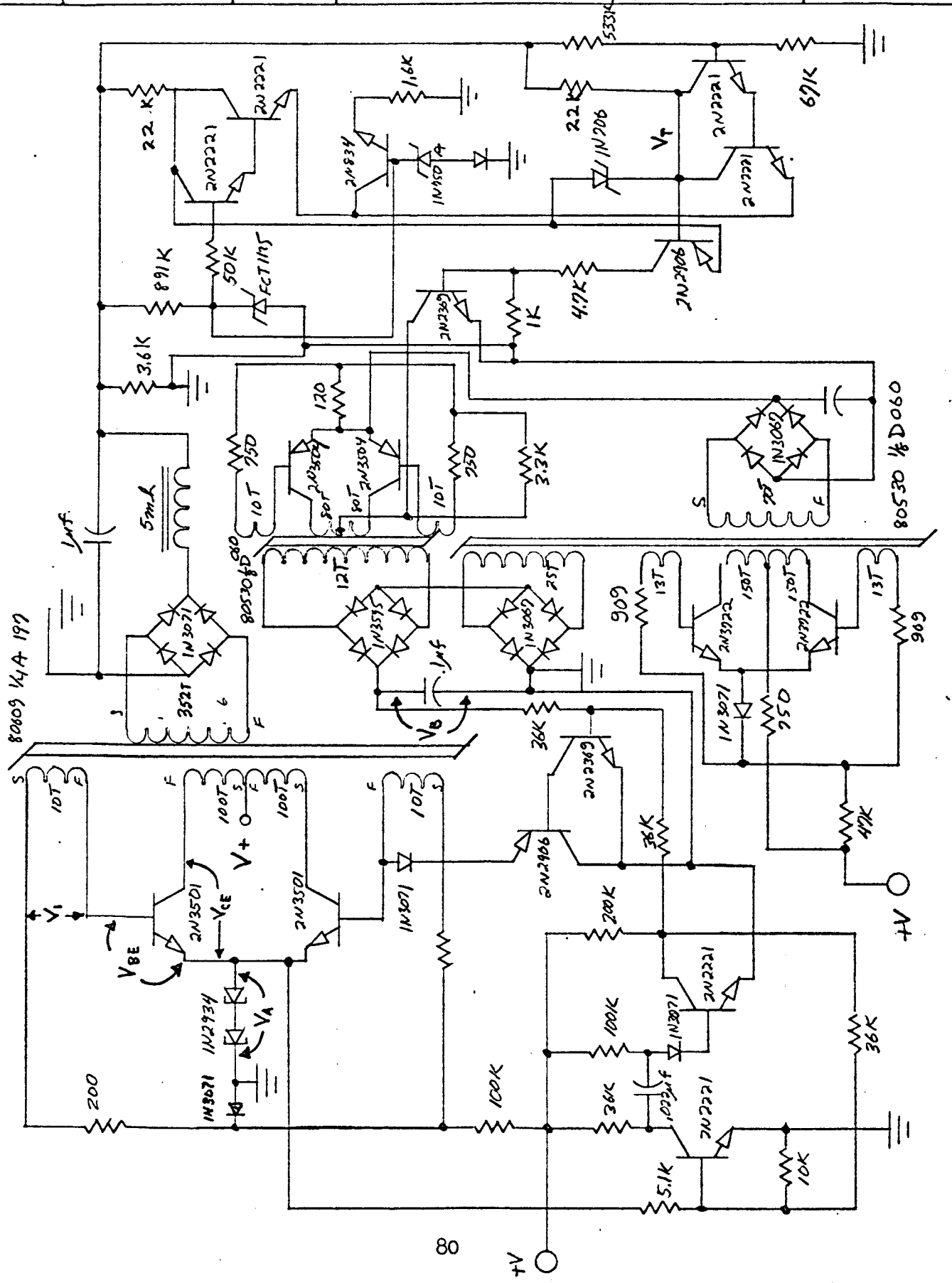

4.3 Phase II - Analysis of Switching Regulation

The switching regulator circuit involves switching the power input to an L-C filter at a rate necessary to achieve line and load regulation. The method used to achieve this regulation is to compare the filter output voltage with a reference voltage. Deviation from the reference will generate an error voltage whose sense can be used to energize or deenergize the switch. To achieve fast response to this error voltage and increase the regulator performance, a high gain difference amplifier and regenerative switch is employed. The block diagram of the closed loop system is shown below in Figure 4.35.

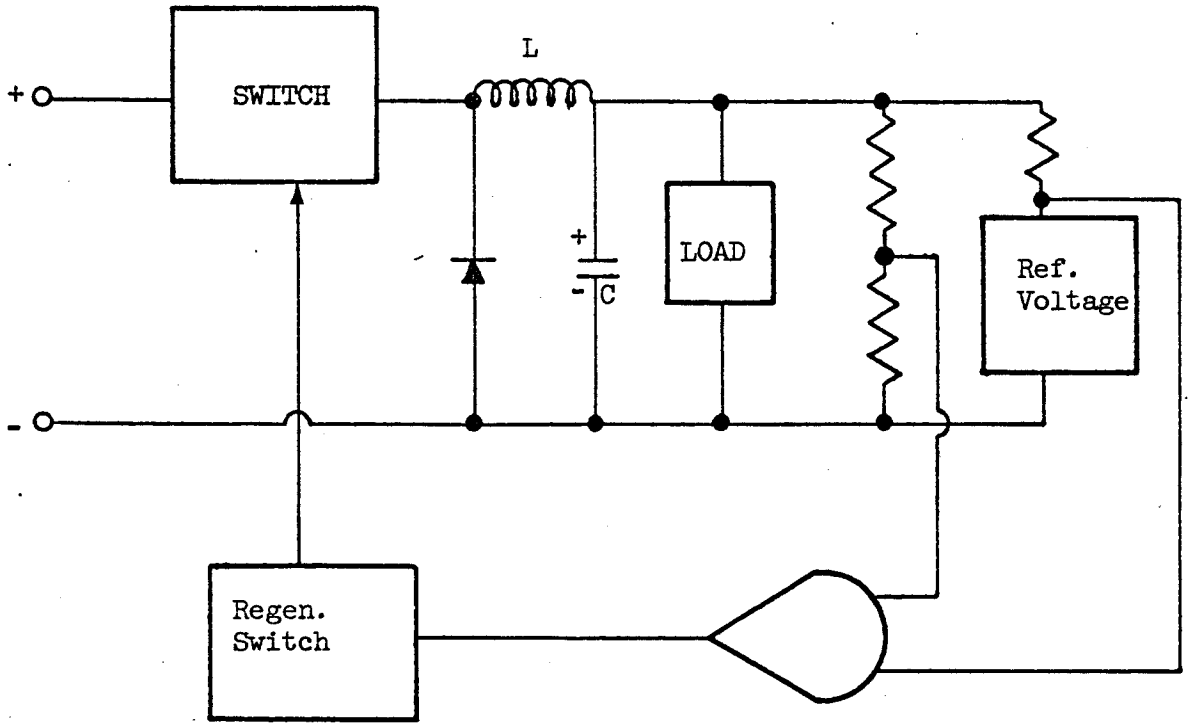

Figure 4.35 - Block Diagram of Switching Regulator

Method for Specifying the Switching Regulator Filter when Restrained by System Specifications: Restraints can be imposed upon the filter values as well as upon the switching times necessary to achieve the desired output. These restraints are implicit in the performance specifications and will be shown to necessarily limit the actual regulator's capability. In many cases the limitation results from lack of suitable components to accomplish the desired function, while in other cases specifications will conflict divergently so as to produce unrealizable circuit elements.

The instantaneous voltage and current relationships of the L-C filter will depend upon the state of the switching device, as well as upon the applied potential variation and the line/load changes. The current and voltage equations with respect to time are derived for the "on" state when energy is supplied through the closed switch to the filter, and for the "off" state when the switch is opened, allowing the collapsing field in the inductor (L) to supply the necessary energy to sustain the potential across the load demanded by the capacitor (C) (see Figure 4.36).

Derivation of Useful Equations for the L-C Filter: The instantaneous voltage and current relationships of the L-C filter will depend upon the state of the switching device as well as upon the applied potential variation and load changes. The current and voltage equations with respect to time will be derived for the "on" state when energy is supplied through the closed switch to the filter and for the "off" state when the switch is opened allowing the collapsing field in the inductor to supply the necessary energy to sustain the potential across the load and filter capacitor.

THE "ON" STATE DERIVATION

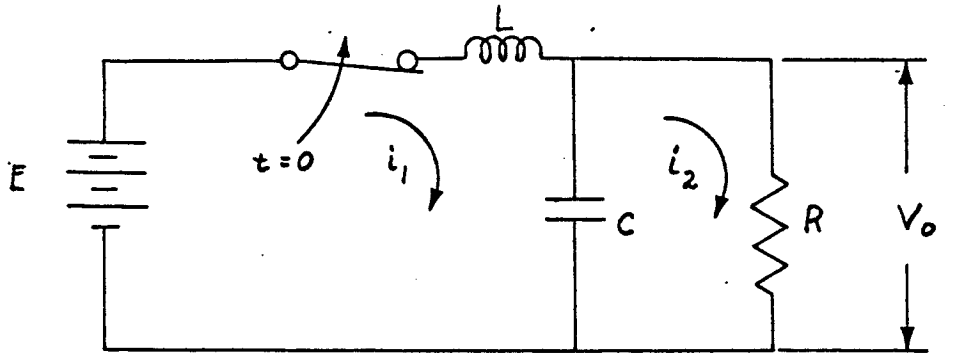

FIGURE 4.36 Equivalent Circuit for "On" State

The equivalent circuit shown above assumes that instantaneous switching occurs at t = o with no losses in the switch and the back-biased diode shown in Figure 4.35 has no leakage.

At the time t = o+, current $I_{nom.}$ is assumed to flow through L and voltage V_{min} exists across the capacitor. The defining mesh equations are:

$$E = L\frac{di_1}{dt} + \frac{1}{C}\int i_1\,dt - \frac{1}{C}\int i_2\,dt \tag{1}$$

$$0 = -\frac{1}{C}\int i_1\,dt + \frac{1}{C}\int i_2\,dt + Ri_2 \tag{2}$$

Taking the La Place transform of each equation and satisfying the boundary conditions results in:

$$\frac{E - \left(\frac{q_1(o+) - q_2(o+)}{C}\right)}{S} + L\,i_1(o+) = \left(SL + \frac{1}{SC}\right)I_1(s) - \frac{1}{SC}I_2(s) \tag{3}$$

$$\frac{q_1(o+) - q_2(o+)}{SC} = -\frac{I_1(s)}{SC} + \left(R + \frac{1}{SC}\right)I_2(s). \tag{4}$$

Define $\dfrac{q_1(o+) - q_2(o+)}{C} \equiv V_{min}$

$$i_1(o+) \equiv I_{NOM.}$$

(see Figure 4.36).

In Matrix Form:

$$\begin{bmatrix} \dfrac{E - V_{min}}{S} + L\,I_{NOM} \\ \dfrac{V_{min}}{S} \end{bmatrix} = \begin{bmatrix} \frac{1}{SC}(s^2LC+1) & -\frac{1}{SC} \\ -\frac{1}{SC} & \frac{1}{SC}(sRC+1) \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix}$$

The matrix determinant Δ is:

$$\Delta = \left(\frac{1}{sC}\right)^2 (s^2LC+1)(sRC+1) - \left(\frac{1}{sC}\right)^2$$

$$= \frac{1}{s^2C^2}\left(s^3RLC^2 + sRC + s^2LC\right)$$

$$= \frac{RL}{s}\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right) \qquad (5)$$

To find the current $I_1(S)$:

$$\Delta I_1(s) = \begin{bmatrix} \frac{E-V_{MIN}}{s} + L I_{NOM} & \left(-\frac{1}{sC}\right) \\ \frac{V_{min}}{s} & \left(\frac{1}{sC}+R\right) \end{bmatrix}$$

$$\Delta I_1(s) = \left[\left(\frac{E-V_{MIN}}{s} + L I_{NOM}\right)(sRC+1) + \frac{V_{MIN}}{s}\right]\frac{1}{sC}$$

$$\Delta I_1(s) = \left[(E-V_{min} + sLI_{NOM})(sRC+1) + V_{MIN}\right]\frac{1}{s^2C}$$

$$\Delta I_1(s) = \frac{LRCI_{NOM}s^2 + \left[(E-V_{MIN})RC + LI_{NOM}\right]s + E}{s^2C}$$

$$I_1(s) = \frac{LRC\,I_{NOM}\,s^2 + \left[(E-V_{MIN})RC + LI_{NOM}\right]s + E}{RL\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)} \cdot \frac{s}{s^2C}$$

$$I_1(s) = \frac{I_{NOM}\,s^2 + \left(\frac{E-V_{MIN}}{L} + \frac{I_{NOM}}{RC}\right)s + \frac{E/R}{LC}}{s\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)}$$

$$I_1(s) = I_{NOM}\,\frac{s^2 + \left(\frac{E-V_{MIN}}{LI_{NOM}} + \frac{1}{RC}\right)s + \frac{E}{RI_{NOM}LC}}{s\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)} \qquad (6)$$

For convenience these values can be substituted by:

$$I_1(s) = I_{NOM}\,\frac{s^2 + a_1 s + a_0}{s\left[(s+\alpha)^2 + \beta^2\right]} \qquad (7)$$

where $$a_1 = \frac{E-V_{MIN}}{LI_{NOM}} + \frac{1}{RC} \qquad (8)$$

$$a_0 = \frac{E}{RI_{NOM}LC} \qquad (9)$$

$$\alpha = \frac{1}{2RC} \qquad (10)$$

$$\beta^2 = \frac{1}{LC} - \left(\frac{1}{2RC}\right)^2 \qquad (11)$$

The inverse La Place Transform of this form is:

$$i_1(t) = \frac{a_0 I_{NOM}}{\alpha^2+\beta^2} - \frac{I_{NOM}}{\beta}\sqrt{\frac{(\alpha^2-\beta^2-a_1\alpha+a_0)^2+\beta^2(a_1-2\alpha)^2}{\alpha^2+\beta^2}}\, \epsilon^{-\alpha t} \sin(\beta t+\psi). \quad (12)$$

Where $\psi = \tan^{-1}\frac{\beta}{\alpha} + \tan^{-1}\frac{\beta(a_1-2\alpha)}{\alpha^2-\beta^2+a_0-a_1\alpha}$.

Substitution and simplification gives:

$$i_1(t) = \frac{E}{R} - \sqrt{\frac{\left(\frac{E}{C}-\frac{E+V_0+\Delta}{2R}\right)^2}{1-\chi/4} + LC\left(\frac{E-V_0+\Delta}{L}\right)^2}\, \epsilon^{-\frac{t}{2RC}} \sin(\beta t+\psi). \quad (13)$$

Where $\beta = \sqrt{\frac{1}{LC}\left(1-\frac{\chi}{4}\right)}$

$$\psi = \tan^{-1}\sqrt{\frac{4}{\chi}-1} + \tan^{-1}\frac{E-V_0+\Delta}{E-V_0-\Delta}\sqrt{\frac{4}{\chi}-1}.$$

for reliability $\chi < 4$

where $V_{MIN} = V_0 - \Delta$

$V_{MAX} = V_0 + \Delta$

Δ = Peak AC ripple

$$\chi = \frac{L}{R^2C}$$

The output voltage is expressed as:

$$E_o(s) = R\,I_2(s) \tag{14}$$

∴ solving for $I_2(s)$:

$$\Delta I_2(s) = \begin{vmatrix} sL + \frac{1}{sC} & \frac{E - V_{min}}{s} + L\,I_{NOM} \\ -\frac{1}{sC} & \frac{V_{min}}{s} \end{vmatrix}$$

$$\Delta I_2(s) = \frac{V_{min}\left(s^2LC+1\right)}{s^2C} + \frac{L\,I_{NOM}\,s + E - V_{min}}{s^2C}$$

$$\Delta I_2(s) = \frac{s^2LC\,V_{min} + L\,I_{NOM}\,s + E}{s^2C}$$

$$I_2(s) = \frac{s^2LC\,V_{min} + L\,I_{NOM}\,s + E}{s^2C} \cdot \frac{s}{RL\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)} \tag{15}$$

$$I_2(s) = \frac{\frac{V_{min}}{R}s^2 + \frac{I_{NOM}}{RC}s + \frac{E/R}{LC}}{s\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)}$$

$$\therefore\ E_o(s) = \frac{V_{min}\, s^2 + \frac{I_{NOM}}{C} s + \frac{E}{LC}}{s\left(s^2 + \frac{1}{RC} s + \frac{1}{LC}\right)} \tag{16}$$

$$= V_{min} \frac{s^2 + \frac{I_{NOM}}{V_{min} C} s + \frac{E}{V_{min} LC}}{s\left(s^2 + \frac{1}{RC} s + \frac{1}{LC}\right)} .$$

This expression is in the same form as $i_1(t)$ and its time value is the following:

$$E_o(s) = V_{min} \frac{s^2 + a_3 s + a_2}{s\left[(s+\alpha)^2 + \beta^2\right]} \tag{17}$$

where $a_3 = \frac{I_{NOM}}{V_{min} C}$ (18)

$$a_2 = \frac{E}{V_{min} LC} \tag{19}$$

$$\alpha = \frac{1}{2RC} \tag{20}$$

$$\beta^2 = \frac{1}{LC} - \left(\frac{1}{2RC}\right)^2 \tag{21}$$

The inverse La Place Transform is:

$$e_o(t) = \frac{a_2 V_{min}}{\alpha^2+\beta^2} - \frac{V_{min}}{\beta}\sqrt{\frac{(\alpha^2-\beta^2-a_3\alpha+a_2)^2+\beta^2(a_3-2\alpha)^2}{\alpha^2+\beta^2}}\, \epsilon^{-\alpha t}\sin(\beta t+\lambda) \quad (22)$$

$$\text{where } \lambda = \tan^{-1}\frac{\beta}{\alpha} + \tan^{-1}\frac{\beta(a_3-2\alpha)}{\alpha^2-\beta^2+a_2-a_3\alpha}.$$

Substitution & Simplification gives:

$$e_o(t) = E - \sqrt{\frac{\left(E-V_o+\Delta-\frac{\chi}{2}\Delta\right)^2}{1-\chi/4} + \chi\Delta^2}\; \epsilon^{-\frac{t}{2RC}}\sin(\beta t+\lambda). \quad (23)$$

$$\lambda = \tan^{-1}\sqrt{\frac{4}{\chi}-1} + \tan^{-1}\frac{\Delta\sqrt{1-\frac{\chi}{4}}}{\sqrt{1/\chi}(E-V_o+\Delta)-\frac{\Delta}{2}\sqrt{\chi}}$$

where $V_{MIN} = V_o - \Delta$

$V_{MAX} = V_o + \Delta$ $\qquad \chi = \frac{L}{R^2C}$

Δ = peak ac ripple

The "Off" Condition: The current and voltage relationships with respect to time are now developed for the filter with the switch in the "off" condition. Again, there are assumed boundary conditions for the L and C components and the ideal diode now acts like a short circuit.

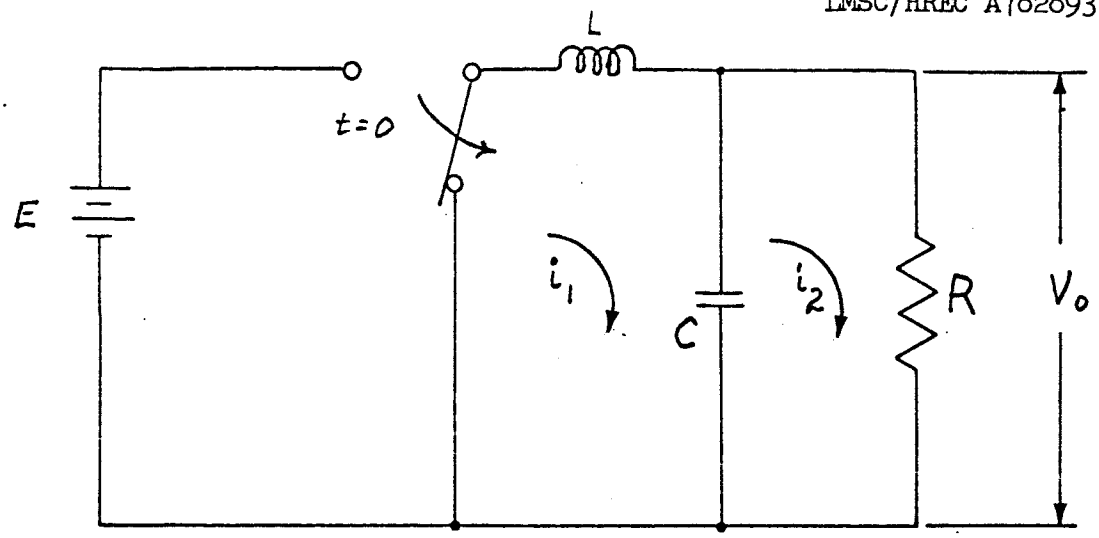

Figure 4.37 - Equivalent Circuit for "Off" State

The equivalent circuit shown above assumes that instantaneous switching occurs at t = o with no losses in the diode shown in Figure 4.35. At time t = o+ current i (o) is assumed to flow through L and voltage v (o) exists across the capacitor. The defining mesh equations are:

$$o = L\frac{di_1}{dt} + \frac{1}{C}\int i_1 dt - \frac{1}{C}\int i_2 dt. \tag{24}$$

$$o = -\frac{1}{C}\int i_1 dt + \frac{1}{C}\int i_2 dt + R i_2 . \tag{25}$$

Taking the La Place Transform of each equation and satisfying the boundary conditions results in:

$$L I_{NOM} - \frac{V_{max}}{S} = \left(sL + \frac{1}{sC}\right) I_1(s) - \left(\frac{1}{sC}\right) I_2(s) \tag{26}$$

$$\frac{V_{max}}{S} = -\left(\frac{1}{sC}\right) I_1(s) + \left(\frac{1}{sC} + R\right) I_2(s) \tag{27}$$

or in matrix form:

$$\begin{bmatrix} L I_{NOM} - \frac{V_{MAX}}{S} \\ \frac{V_{MAX}}{S} \end{bmatrix} = \begin{bmatrix} (sL + \frac{1}{sC}) & -(\frac{1}{sC}) \\ -(\frac{1}{sC}) & (\frac{1}{sC} + R) \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_L(s) \end{bmatrix}$$

The matrix determinant Δ was derived from equation (S) and is:

$$(S) \quad \Delta = \frac{RL}{S}\left(S^2 + \frac{1}{RC}S + \frac{1}{LC}\right)$$

To find the voltage $V_o'(s)$:

$$V_o'(s) = R I_2'(s)$$

$$\text{where } \Delta I_2'(s) = \begin{bmatrix} sL + \frac{1}{sC} & L I_{NOM} - \frac{V_{MAX}}{S} \\ -\frac{1}{sC} & \frac{V_{MAX}}{S} \end{bmatrix}$$

$$\Delta I_2'(s) = \frac{V_{MAX}}{S}\left(\frac{s^2LC+1}{sC}\right) + \frac{sLI_{NOM} - V_{MAX}}{s^2C} \qquad (28$$

$$= \frac{V_{MAX} LC s^2 + I_{NOM} LS}{s^2C} = \frac{V_{MAX} LC s + I_{NOM} L}{sC}$$

$$I_2'(s) = \frac{V_{MAX} LC s + I_{NOM} L}{RLC\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)} \tag{29}$$

$$= \frac{V_{MAX}}{R} \frac{s + \frac{I_{NOM}}{V_{MAX} C}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}}$$

$$V_o'(s) = V_{MAX} \frac{s + \frac{I_{NOM}}{V_{MAX} C}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}}. \tag{30}$$

The inverse La Place Transform is:

$$e_o'(t) = V_{max} \mathcal{L}^{-1}\left[\frac{s + a_4}{(s+\alpha)^2 + \beta^2}\right] \tag{31}$$

where $a_4 = \frac{I_{NOM}}{V_{MAX} C}$

$$\alpha = \frac{1}{2RC}$$

$$\beta^2 = \frac{1}{LC} - \left(\frac{1}{2RC}\right)^2$$

$$e_o'(t) = \frac{V_{max}}{\beta} \epsilon^{-\alpha t} \sqrt{\beta^2 + (a_4 - \alpha)^2}\, \sin(\beta t + \theta) \tag{32}$$

where $\theta = \frac{\beta}{a_4 - \alpha}$

Substitution gives:

$$e_o'(t) = \sqrt{\frac{(V_o + \Delta)^2 - X \Delta V_o}{1 - X/4}} \left(\epsilon^{-\frac{t}{2RC}} \right) \sin(\beta t + \theta) \tag{33}$$

where $\theta = \tan^{-1} \dfrac{(V_o + \Delta)\left(\frac{1}{n} - \frac{1}{4}\right)}{V_o}$

again letting:

V_o = rated output voltage

Δ = peak AC ripple

$V_o + \Delta = V_{max}$

$V_o - \Delta = V_{min}$

$I_{nom} = V_o/R$

To find $I_1'(s)$:

$$\Delta I_1'(s) = \begin{vmatrix} L I_{NOM} - \frac{V_{MAX}}{S} & -\frac{1}{SC} \\ \frac{V_{MAX}}{S} & \frac{1 + SRC}{SC} \end{vmatrix}$$

$$\Delta I_1'(s) = \frac{(LS I_{NOM} - V_{MAX})(1 + SRC)}{S^2 C} + \frac{V_{MAX}}{S^2 C} \tag{34}$$

$$= \frac{RCL I_{NOM} S + L I_{NOM} - RC V_{MAX}}{SC}$$

$$I_1'(s) = \frac{RLC\, I_{NOM}\, s + L I_{NOM} - RC V_{MAX}}{RLC\left(s^2 + \frac{1}{RC}s + \frac{1}{LC}\right)} \qquad (35)$$

$$= I_{NOM}\, \frac{s + \frac{1}{RC} - \frac{V_{MAX}}{L I_{NOM}}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}}.$$

The inverse La Place is:

$$i_1'(t) = I_{NOM}\, \mathcal{L}^{-1}\, \frac{s + a_5}{(s+\alpha)^2 + \beta^2} \qquad (36)$$

where $$a_5 = \frac{1}{RC} - \frac{V_{MAX}}{L I_{NOM}}$$

$$\alpha = \frac{1}{2RC}$$

$$\beta^2 = \frac{1}{LC} - \frac{1}{4R^2C^2}$$

This solution has the same form as (34):

$$i_1'(t) = \frac{V_o}{R}\sqrt{\frac{V_o + \Delta(1+X)}{XV_o(1 - X/4)}}\, \epsilon^{-\frac{t}{2RC}} \sin(\beta t + \Phi). \qquad (37)$$

where $$\Phi = \tan^{-1} \frac{\sqrt{\frac{1}{X} - \frac{1}{4}}}{1 - \frac{V_o + \Delta}{XV_o}}$$

Solving for X = the Dilemma: A restraint can be placed on X by solving $e_o(t)$ at time $t = o$. This is the voltage equation which defines the voltage decay during the time that the switch is open. By definition $e_o'(t = o) = V_o + \Delta$.

$$V_o + \Delta = \sqrt{\frac{(V_o+\Delta)^2 - X\Delta V_o}{1 - X/4}}\,\sin\theta$$

$$\text{where } \theta = \sin^{-1}\frac{\sqrt{\frac{1}{2C}\left(1-\frac{X}{4}\right)}}{\sqrt{\frac{1}{2C}\left(1-\frac{X}{4}\right) + \left(\frac{V_o}{V_o+\Delta}\cdot\frac{1}{RC} - \frac{1}{2RC}\right)^2}}$$

$$= \sin^{-1}\frac{\sqrt{1-\frac{X}{4}}}{\sqrt{1-\frac{X}{4} + X\left(\frac{V_o}{V_o+\Delta} - \frac{1}{2}\right)^2}}$$

$$= \sin^{-1}\frac{1}{\sqrt{1 + \frac{X/4}{1-\frac{X}{4}}\left(\frac{V_o-\Delta}{V_o+\Delta}\right)^2}}$$

$$(V_o+\Delta)^2 = \frac{(V_o+\Delta)^2 - X\Delta V_o}{1-X/4}\cdot\frac{1}{1+\frac{1}{4/X-1}\left(\frac{V_o-\Delta}{V_o+\Delta}\right)^2}$$

$$(V_o+\Delta)^2 = \frac{(V_o+\Delta)^2 - \chi\Delta V_o}{1-\frac{\chi}{4}+\frac{1}{4/\chi-1}\left(\frac{V_o-\Delta}{V_o+\Delta}\right)^2-\frac{\chi/4}{4/\chi-1}\left(\frac{V_o-\Delta}{V_o+\Delta}\right)^2}$$

$$-\frac{\chi}{4}(V_o+\Delta)^2+\frac{1}{4/\chi-1}(V_o-\Delta)^2-\frac{\chi/4}{4/\chi-1}(V_o-\Delta)^2+\chi\Delta V_o = 0$$

$$-\frac{\chi}{4}V_o^2-\frac{\chi\Delta V_o}{2}-\frac{\chi\Delta^2}{4}+\chi\Delta V_o = -\frac{\chi}{4}(V_o^2-2\Delta V_o+\Delta^2) = -\frac{\chi}{4}(V_o-\Delta)^2$$

$$\frac{1}{\frac{4}{\chi}-1}(V_o-\Delta)^2-\frac{\chi/4}{4/\chi-1}(V_o-\Delta)^2-\frac{\chi}{4}(V_o-\Delta)^2 = 0$$

$$\frac{1}{\frac{4}{\chi}-1}-\frac{\chi/4}{\frac{4}{\chi}-1}-\frac{\chi}{4} = 0$$

$$4-\chi-4+\chi = 0$$

$\therefore$ χ is a dependent variable which cannot be used as a restraint.

Selecting a Turn-off Time (t_{off}): In order to determine system parameters it is necessary to assume certain conditions:

$$e_o'(t = t_{off}) = V_o - \Delta$$

$$V_o - \Delta = \epsilon^{-\frac{t_{off}}{2RC}} \sqrt{\frac{(V_o+\Delta)^2 - \chi\Delta V_o}{1-\chi/4}} \sin(\beta t_{off} + \theta)$$

since $\sin(\beta t + \theta) = \sin\beta t \cos\theta + \cos\beta t \sin\theta$

$$V_o - \Delta = \epsilon^{-\frac{t_{off}}{2RC}} \left[\sin\beta t_{off} \sqrt{\frac{(V_o+\Delta)^2 - \chi\Delta V_o}{1-\chi/4}} \cos\theta + (V_o+\Delta)\cos\beta t_{off} \right].$$

because $V_o + \Delta \equiv \sqrt{\frac{(V_o+\Delta)^2 - \chi\Delta V_o}{1-\chi/4}} \sin\theta$

also $\theta = \cos^{-1} \frac{1}{\sqrt{1 + \frac{\frac{4}{\chi} - 1}{\left(\frac{V_o-\Delta}{V_o+\Delta}\right)^2}}} = \cos^{-1} \sqrt{\frac{(V_o-\Delta)^2}{(V_o-\Delta)^2 + (V_o+\Delta)^2\left(\frac{4}{\chi}-1\right)}}$

$$V_o - \Delta = \epsilon^{-\frac{t_{off}}{2RC}} \left[\sqrt{\frac{(V_o+\Delta)^2 - \chi\Delta V_o}{1-\frac{\chi}{4}} \cdot \frac{(V_o-\Delta)^2}{(V_o-\Delta)^2 + (V_o+\Delta)^2\left(\frac{4}{\chi}-1\right)}} \sin\beta t_{off} \right.$$

$$\left. + (V_o+\Delta)\cos\beta t_{off} \right].$$

$$1 = \epsilon^{-\frac{t_{off}}{2RC}}\left[\sqrt{\frac{(V_o+\Delta)^2 - \chi\Delta V_o}{(V_o-\Delta)^2 + (V_o+\Delta)^2\left(\frac{4}{\chi}+\frac{\chi}{4}-2\right) - \frac{\chi}{4}(V_o-\Delta)^2}}\sin\beta t_{off} + \frac{V_o+\Delta}{V_o-\Delta}\cos\beta t_{off}\right]$$

Assume $\frac{\Delta}{V_o} = .01$, $\chi = 2$

$$\epsilon^{\frac{t_{off}}{2RC}} = \sqrt{\frac{1.0001}{.9801 + 2.0402 - .4900S}}\sin\beta t_{off} + 1.020\cos\beta t_{off}$$

$$\epsilon^{\frac{t_{off}}{2RC}} = .63\sin\beta t_{off} + 1.020\cos\beta t_{off}$$

Since $\beta = \sqrt{\frac{1}{LC}\left(1-\frac{\chi}{4}\right)} = \sqrt{\frac{1}{LC}\left(1-\frac{1}{2}\right)} = \frac{1}{\sqrt{2LC}}$

$\chi = 2 = \frac{L}{R^2C}$ when $R = 3.6$K ohm.

$\frac{L}{C} = 2(3.6)^2 \times 10^6 = 2.592 \times 10^7$

choose $C = 10^{-8}$ f

so that $L = .2592$ h

$LC = .2592 \times 10^{-8}$

$2LC = .5184 \times 10^{-8}$ $\sqrt{2LC} = 7.20 \times 10^{-5}$

$$\beta = 1.39 \times 10^{4}$$

$$2RC = (2)(3.6) \times 10^{-5} = 7.2 \times 10^{-5} \text{ sec.}$$

$$\frac{1}{2RC} = 1.39 \times 10^{4} \text{ sec}^{-1}$$

$$\epsilon^{1.39 \times 10^{4} t_{off}} = .63 \sin 1.39 \times 10^{4} t_{off} + 1.020 \cos 1.39 \times 10^{4} t_{off}.$$

by iteration:

$$t_{off} = 6 \mu\text{sec.}$$

To calculate t_{on}:

$$e_o(t_{on}) = E - \sqrt{\frac{(E - V_o + \Delta - \frac{\chi}{2}\Delta)^2}{1 - \chi/4} + \chi \Delta^2}\, \epsilon^{-\frac{t_{on}}{2RC}} \sin(\beta t_{on} + \lambda)$$

$$e_o(t_{on}) = V_o + \Delta$$

Using the same conditions and assumptions as the t_{off} case:

$$V_o(1.01) = E - \sqrt{2(E - V_o)^2 + .0002 V_o^2}\, \epsilon^{-\frac{t_{on}}{2RC}} \sin(\beta t_{on} + \lambda).$$

or

$$1.01 = \frac{E}{V_0} - \sqrt{2\left(\frac{E}{V_0}-1\right)^2 + .0002}\; \epsilon^{-\frac{t_{ON}}{2RC}} \sin(\beta t_{ON} + \lambda).$$

if $\frac{E}{V_0} = \frac{3}{2}$

$$1.01 = \frac{3}{2} - \sqrt{1.0002}\; \epsilon^{-\frac{t_{ON}}{2RC}} \sin(\beta t_{ON} + \lambda).$$

$$1.0001\, \epsilon^{-\frac{t_{ON}}{2RC}} \sin(\beta t_{ON} + \lambda) = 0.490$$

$$\epsilon^{1.39\times10^4 t_{ON}} = \frac{\sin(1.39\times10^4 t_{ON} + \lambda)}{.490}$$

$$\lambda = \tan^{-1} 1.0 + \tan^{-1} \frac{.01\sqrt{\frac{1}{2}}}{\sqrt{\frac{1}{2}}\left(\frac{3}{2}-.99\right) - \frac{\sqrt{2}}{2}.01}$$

$$\lambda = 45^\circ + \tan^{-1} .020 = 46.15^\circ$$

$$\epsilon^{1.39\times10^4 t_{ON}} = \frac{\sin(1.39\times10^4 t_{ON} + 46.15^\circ)}{.490}$$

$\therefore t_{ON} = 51\,\mu sec.$ by iteration.

In summary a switching regulator can be designed from the following parameters:

$R = 3.6K$

$L = .259h$

$C = .010\ \mu fd$

$\frac{\Delta}{V_o} = .01$

$\frac{E}{V_o} = 3/2$

to have an ideal switching frequency of $f = \left(\frac{1}{6 + 51}\right) \times 10^6$

$f = 1.75 \times 10^4 = 17.5$ kc

A set of design curves could be generated (given sufficient time) to show the interaction of the regulation $\left(\frac{\Delta}{V_o}\right)$ and the line $\left(\frac{E}{V_o}\right)$ upon switching times with X as a parameter (see Figure 4.38 and 4.39).

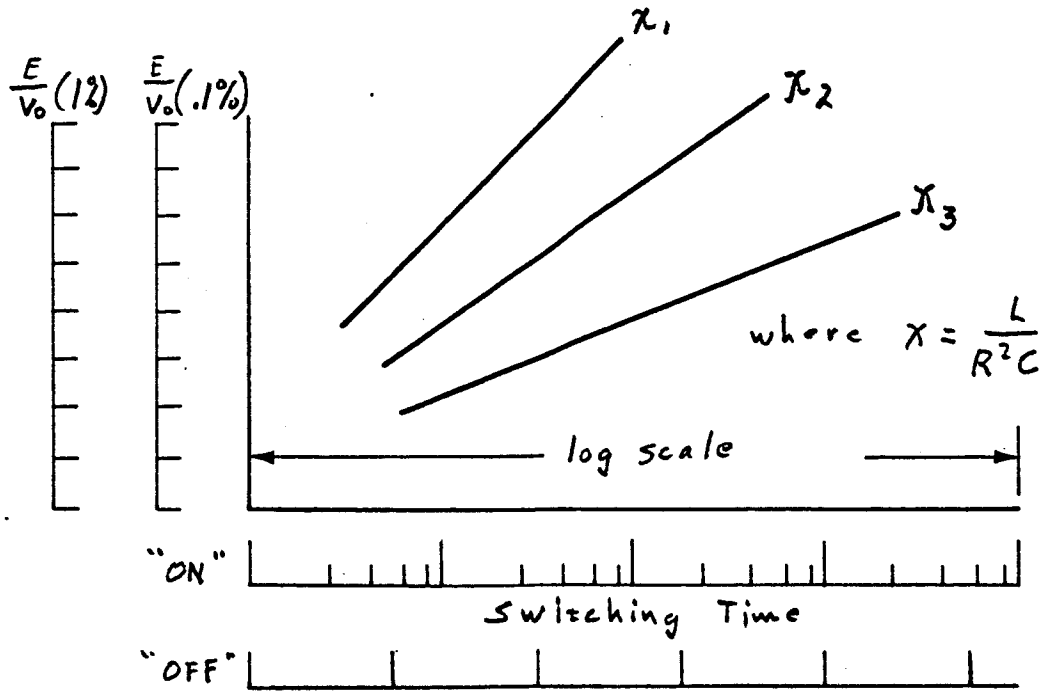

Figure 4.38

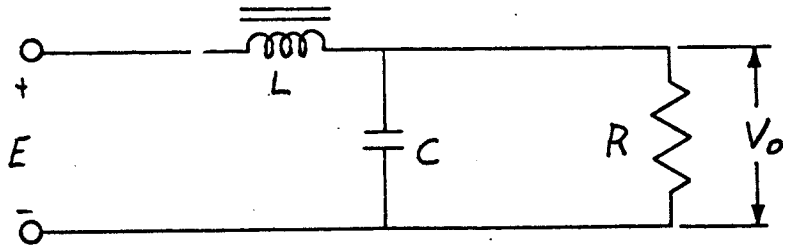

Figure 4.39

To clarify this explanation assume that the line variation is given as E_1 and E_2. The output voltage required is specified as V_o. The load variation is R_1 and R_2. Then the L/C ratio (which with the values of R_1 and R_2 specify an X_1 and X_2) can be varied to achieve reasonable turn on and turn off switching times. The variation of the X parameter of course must be held between 0 and 4 for circuit reliability ($0 < X < 4$). Thus, $\frac{E_1}{V_o}$ and $\frac{E_2}{V_o}$ when compared with X_1 and X_2 define a t_{on} and t_{off} switching time. The regulation $\frac{\Delta}{V_o}$ achieved by these values is automatically secured by using the proper $\frac{E}{V_o}$ scale. If 1% regulation is required, the $\frac{E}{V_o}$ (1%) scale is used. Thus, realizable values of switching times and L/C ratios can be determined graphically with knowledge of the load/line regulation and the required output voltage and its allowable variation.

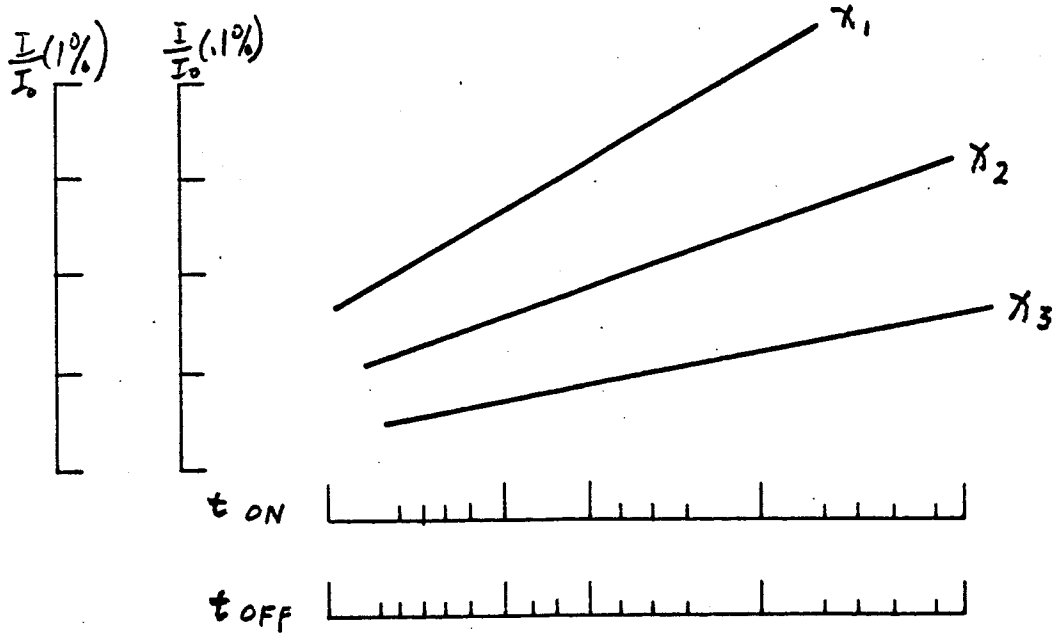

Figure 4.40

The same type of design curves could be developed to optimize the core size and magnetizing current requirements for the inductor as well as specify the peak currents necessary to achieve proper regulation. I_o is the nominal load current (V_o/R). I_1 is the peak current supplied from the energy source. The parenthesis indicate regulation requirements (1% - 0.1%, etc.).

5.0 FUTURE RECOMMENDATIONS FOR RADIATION RESISTANT POWER SUPPLIES

As a result of the success encountered in mechanizing the laboratory feasibility model of the 400 Hz inverter, it is clear that a simplified and refined version of the 400 Hz can be designed and fabricated to meet NASA's demanding environment. The proposed project is described in detail under separate cover.

Essentially, the improved version overcomes the shortcomings of the laboratory model because it will (1) generate the 400 Hz reference through the use of a crystal controlled oscillator operating at a high multiple of 400 Hz and counted down to 400 Hz via digital flip flops; (2) regulate the amplitude of the square wave by comparison with a temperature-compensated zener; (3) remove all odd harmonics via an active filter using two IC operational amplifiers and an R-C network (no even harmonics exist due to the countdown action and the resulting symmetry of the square wave); (4) the power one-shot will be greatly simplified, the timing transformer T_1 eliminated and replaced by IC digital circuits; (5) the power switch section redesigned; and (6) the logic section simplified. The result will be a high efficiency (80% to 85%), high performance inverter composed almost entirely of integrated circuits, both digital and analog, and thick film networks.