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ADVANCED DIGITAL CIRCUIT R&D EVALUATION

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Prepared for:

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FINAL REPORT
CAL Report No. UD-2002-X-1
Contract No. NAS 8-11412
3 October 1964 to 30 September 1965

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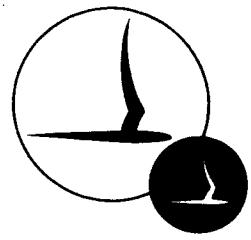

Final Report

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Prepared for:

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ABSTRACT

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A program of evaluation and testing was carried out to determine the suitability of using integrated circuits in the Saturn IB and V Launch Vehicle Data Adapter. Three digital logic lines, a thick film hybrid DTL, a monolithic integrated DTL and a monolithic integrated TTL, were evaluated in each of three applications and comparative data prepared. Evaluation was carried out over the full temperature rating of each circuit and data taken on maximum frequency of operation, noise margin, power required, and power supply tolerance.

A table was prepared to compare performance and included a comparison of circuit wiring complexity (number of connections) and circuit size (number of modules).

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1.0 OBJECTIVE OF PROGRAM

Cornell Aeronautical Laboratory (CAL) has conducted a program of advanced digital microminiature circuit evaluation for the NASA Marshall Space Flight Center, (MSFC), Huntsville, Alabama under Contract NAS8-11412.

The objective of this evaluation program was to determine if microminiature circuits might be suitable for use in the Saturn IB and V launch vehicle, in order to minimize power and weight and increase the reliability of the electronics. Integrated circuits were to be selected and evaluated along with a thick film hybrid microminiature circuit now in use in the Saturn IB Launch Vehicle Digital Computer and Data Adapter, and performance compared.

1.1 Evaluation Program

Study was made of the Launch Vehicle Data Adapter (LVDA) and the Unit Logic Device (ULD) circuits used in it. A search of available monolithic integrated circuits which would be suitable in the LVDA environment was made, and several selected which appeared best suited. Technical personnel at MSFC selected two lines of monolithic integrated circuits and these were evaluated, along with the ULD's, in applications. Unit tests and stress tests were performed on the circuits, to sort out early failures. Three digital applications were constructed and tested with each logic line, and each application evaluated at temperature extremes. Comparison was made of the operating parameters of each logic line in each application.

2.0 DESCRIPTION OF CIRCUITS TESTED

Three logic lines by three manufacturers were chosen by MSFC for evaluation after an initial study and recommendations by CAL. These are:

1) The Unit-Logic Device (ULD) thick film hybrid diode transistor logic (DTL) modules, which are now in use in the Saturn IB Launch Vehicle Digital Computer (LVDC) and Data Adapter, manufactured by IBM Corp.

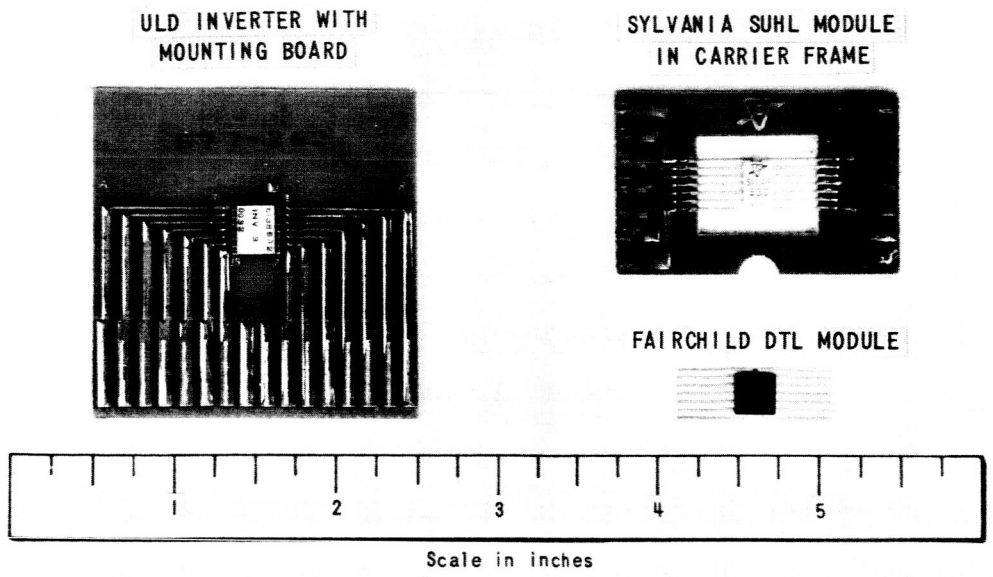
2) The Fairchild DTL monolithic integrated circuits in the militarized flat package.

3) The Sylvania Universal High Level Logic (SUHL) using Transistor-Transistor Logic (TTL) in the militarized flat package.

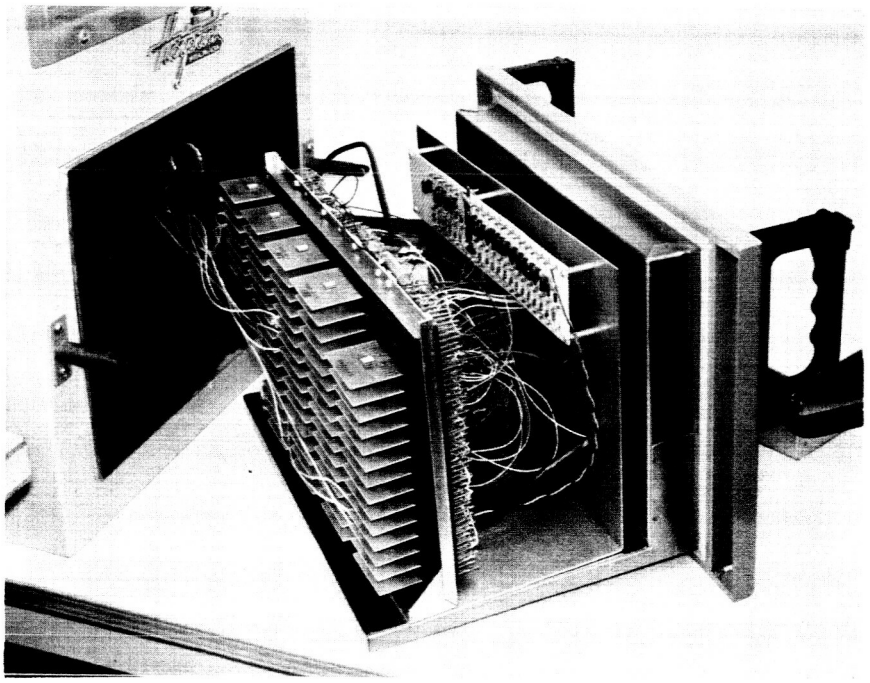
The ULD modules have been in development for over a year. The Fairchild DTL circuits have been commercially available for over a year, while the Sylvania SUHL modules became available late in 1964, and have since been superseded by a second generation of SUHL circuits.

2.1 ULD Circuits

The ULD circuits tested, those used in the Saturn Launch Vehicle Digital Computer (LVDC) and Launch Vehicle Data Adapter (LVDA),[1] can be briefly described as thick film, hybrid circuits using a straightforward DTL (Diode Transistor Logic) logic. In the Saturn LVDC and LVDA they are mounted on a special multi-layer printed circuit board, 35 to a board. Two printed circuit boards containing 35 ULD's each are mounted back to back on a special heat sink frame and this assembly is called a page. In this evaluation program each ULD module was mounted on its own printed circuit board at the factory, as shown in Figure 2.1a, and this board was plugged into a special connector block when testing of the circuit was required. The counter and shift register applications were assembled by wiring up to 10 connector blocks into the required circuits, and plugging in up to 78 printed circuit boards each containing either an INVERTER, AA or AB module as shown in Figure 2.1b. Thus it was not necessary to solder any connections to any individual ULD modules during any testing.



a. ULD, SYLVANIA AND FAIRCHILD MODULES WITH SCALE



b. THE ULD SYNCHRONOUS COUNTER TEST SETUP, MOUNTED ON THE TEST CHAMBER DOOR, IS READY TO BE SLID INTO THE TEMPERATURE TEST CHAMBER. NOTE THE ULD MODULES, EACH MOUNTED ON ITS OWN PRINTED CIRCUIT BOARD.

Figure 2.1

2.1.1 Fabrication

The ULD modules are constructed on a 0.3" x 0.3" alumina substrate. Resistor patterns are silk screened on the bottom of this chip, and conductor patterns on both top and bottom of the chip. After firing of the chip to insure adhesion of the conductors and resistors, the resistors are trimmed by air abrasion to within 1% of their desired value. Twenty-five mil square chips containing either a transistor or two diodes (back to back) are soldered to the conductor pattern using a reflow solder technique and copper balls to make contact between the conductor pattern and the chip. Thus the chip is held slightly off, and bridging over, the conductor pattern. Fourteen S-shaped clips are added to the edges of the chip to insure conduction from the conductor pattern on one side to the other side, and also to provide an electrical and mechanical mounting for the chip. Necessary varnish coatings, and a frame and lid arrangement are added to protect the resistor side and semiconductor side respectively.

The circuits found on the three types of ULD's are shown in Figure 2.2. The inverter module forms the basic building block of the ULD logic and the AA and AB modules are used to extend the diode logic input capability. All diode logic AND-OR gates feed into a base of an inverter transistor.

It will be noticed immediately that all nodes are brought out to connectors. Thus, all components-resistors, diodes, and transistors-can be tested individually, rather than requiring testing of a gate or flip flop entirely as is required in most integrated circuits. The disadvantage is two-fold: there is less circuitry per module because of pin limitations, and more connections are required for any given logical function. The results of these two factors will be more fully realized when a tabulation of modules and connections is made in section 7.

2.1.2 Use of ULD Modules

In use, the ULD inverter modules have a good deal of logical flexibility in the inputs to the inverter. In Figure 2.3 voltages have been added to show the normal operating circuit of a ULD. A three input AND

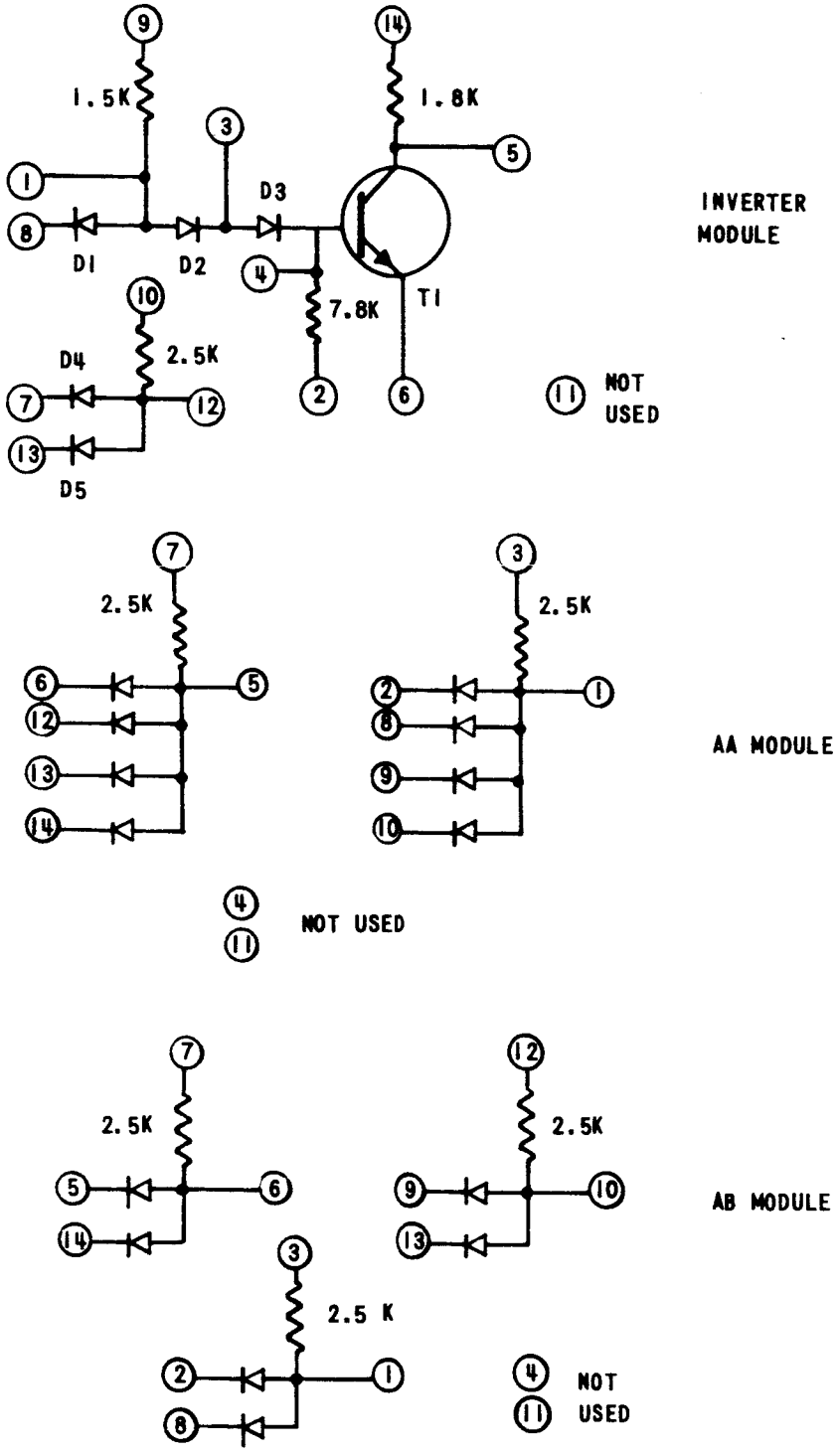


Figure 2.2 CIRCUIT AND PIN CONNECTIONS OF ULD INVERTER, AA AND AB MODULES

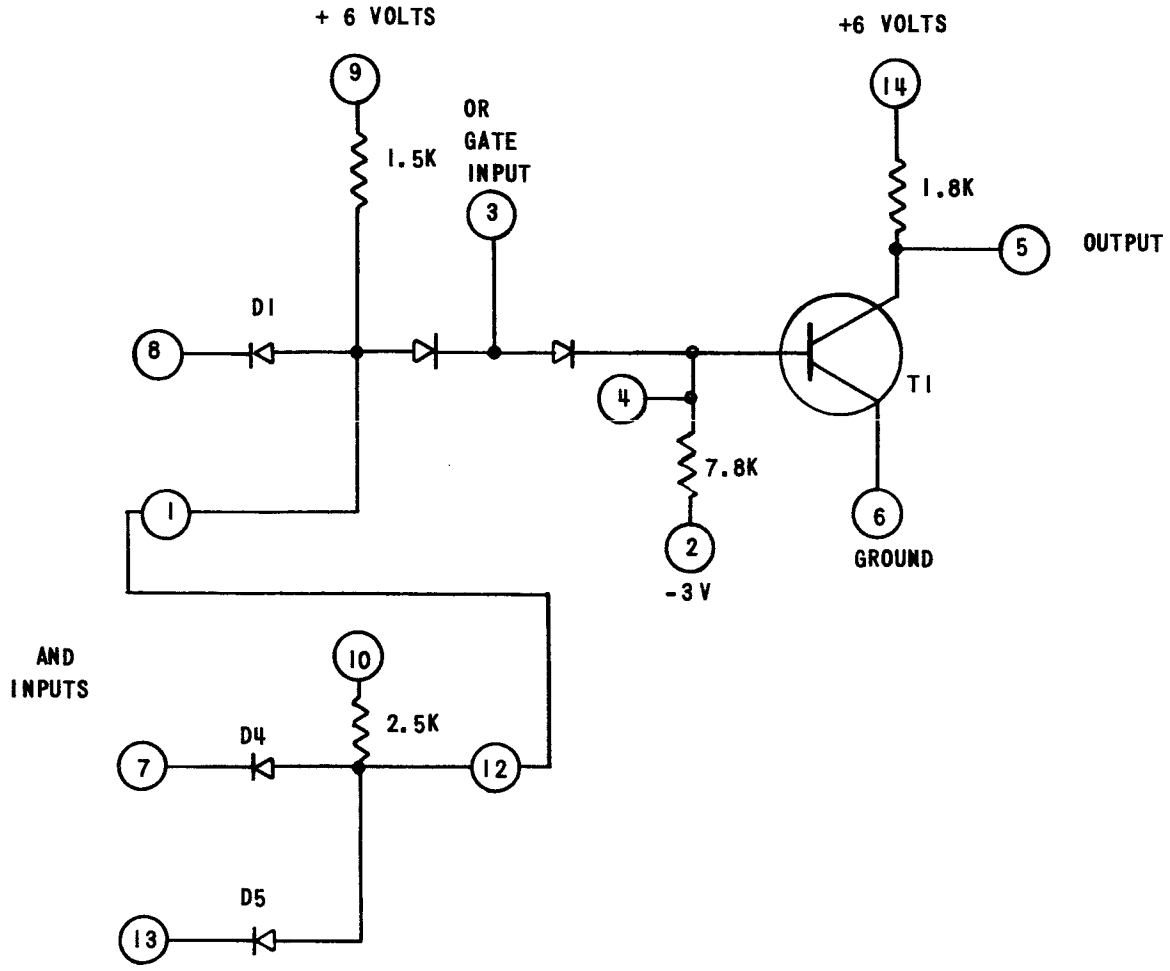


Figure 2.3 ULD INVERTER MODULE CONNECTECTED AS 3 INPUT NAND GATE

gate has been formed by connecting pins 12 and 1 together and leaving pin 10 open. The voltage at pin 9 provides base current for T1. When pins 7, 8 or 13 become grounded, the node current from pin 9 flows out to the left and no base current for T1 is available. The 7.8K resistor connected to -3 volts provides reverse base current to insure, in this case, that T1 is fully turned OFF and pin 5 goes up toward 6 volts. The gate is an AND gate for positive signals, with inversion of the logic polarity at the transistor, or what is called a NAND gate. Additional signals may also be ORed with the inputs of this gate by using pin 3 as a common OR point.

The output of the inverter can be clocked by substituting a clock voltage for the constant voltage at pin 9. The clock voltage will be +6 volts when the AND gate is active, and zero volts when the output of the AND gate is inactive.

There are two AND gate resistors used in the ULD which determine the base current to the transistor, and hence the drive or output current that the transistor can handle. Also, drive capabilities are different depending on use of a D.C. or clock voltage at the AND gate. Table 2.1 gives the fan-out rules suggested by the manufacturer for ULD modules.

TABLE 2.1

INVERTER Resistor	DRIVE Voltage	INVERTER FAN OUT "C"
1.5K	6VDC	10
1.5K	CLOCK	8
2.5K	6VDC	4
2.5K	CLOCK	3

Standard Load Definition:

$$C = N_1 + 3/5\, N_2$$

where N_1 = number of 1.5K loads

N_2 = number of 2.5K loads

Figure 2.4 shows how ULD modules would be used to construct a clocked flip-flop stage, to be used in a multi-phase clock digital system. Two inverter modules have been interconnected. When clock voltage Cp is zero volts, the cross coupling from inverter output 5 to input 8 of the opposite inverter holds the flip-flop in either a ONE or ZERO state. Assuming the condition that T1 is on, T2 off, when Cp becomes +6 volts, a ONE (+ voltage) at the set input will allow base current to reach T2. Then T2 will turn ON, grounding D1 and removing base current from T1. T1 will turn off and, if the clock voltage is removed, the two transistors will remain in the same state. It is obvious that in case there is a ONE at set and reset inputs, then both outputs will become ZERO as long as the clock voltage is present. After the clock voltage is removed, it is uncertain to which state T1 and T2 will revert.

The interconnection of four ULD inverter modules to form one stage of a shift register is shown in Figure 2.5. Clock voltage Cpx clocks the input portion of the circuit, while clock Cpy clocks the output portion.

Five ULD modules, four inverters and an AB unit, are required to construct the synchronous counter stage shown in Figure 2.6. The stage again requires a two phase clock system and includes provision for reset of the counter to zero. Reset could be provided for any arbitrary bit pattern if required.

The ULD ripple counter stage shown in Figure 2.7 requires four inverter modules, one AA module and one AB module. Provision is included for a reset and no clock pulses are required to clock the counter. The counter will count a signal used to drive the first stage.

2.2 Fairchild DTL Circuits

The Fairchild DTL Circuits evaluated in this program are fully microminiaturized monolithic integrated circuits which are packaged in a standard militarized flat package.[2] The circuits are rated by the manufacturer for operation at 5 mc over the temperature range of -55°C to +125°C.

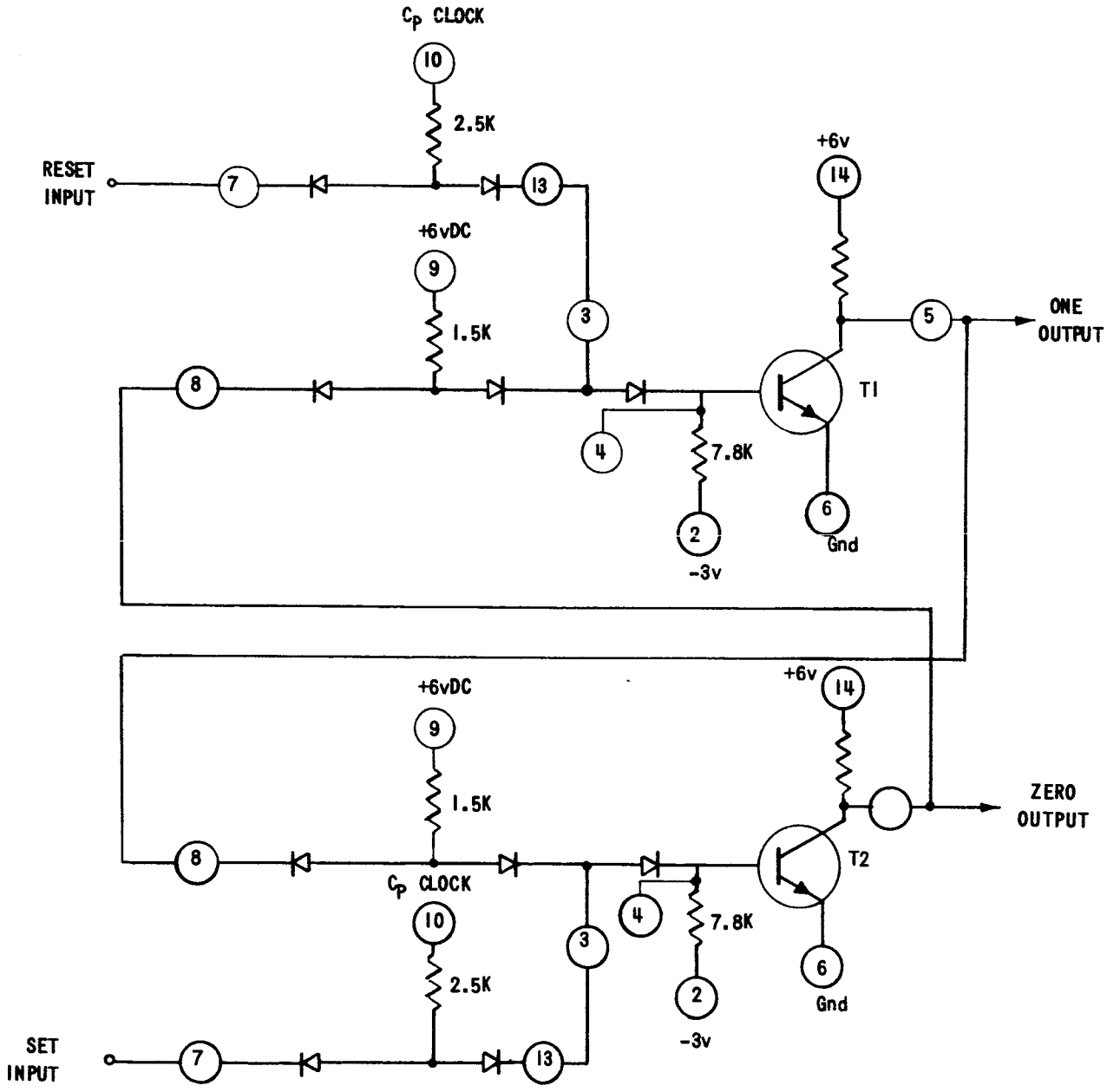


Figure 2.4 TWO ULD INVERTER MODULES CONNECTED TO FORM A TWO PHASE RS FLIP-FLOP

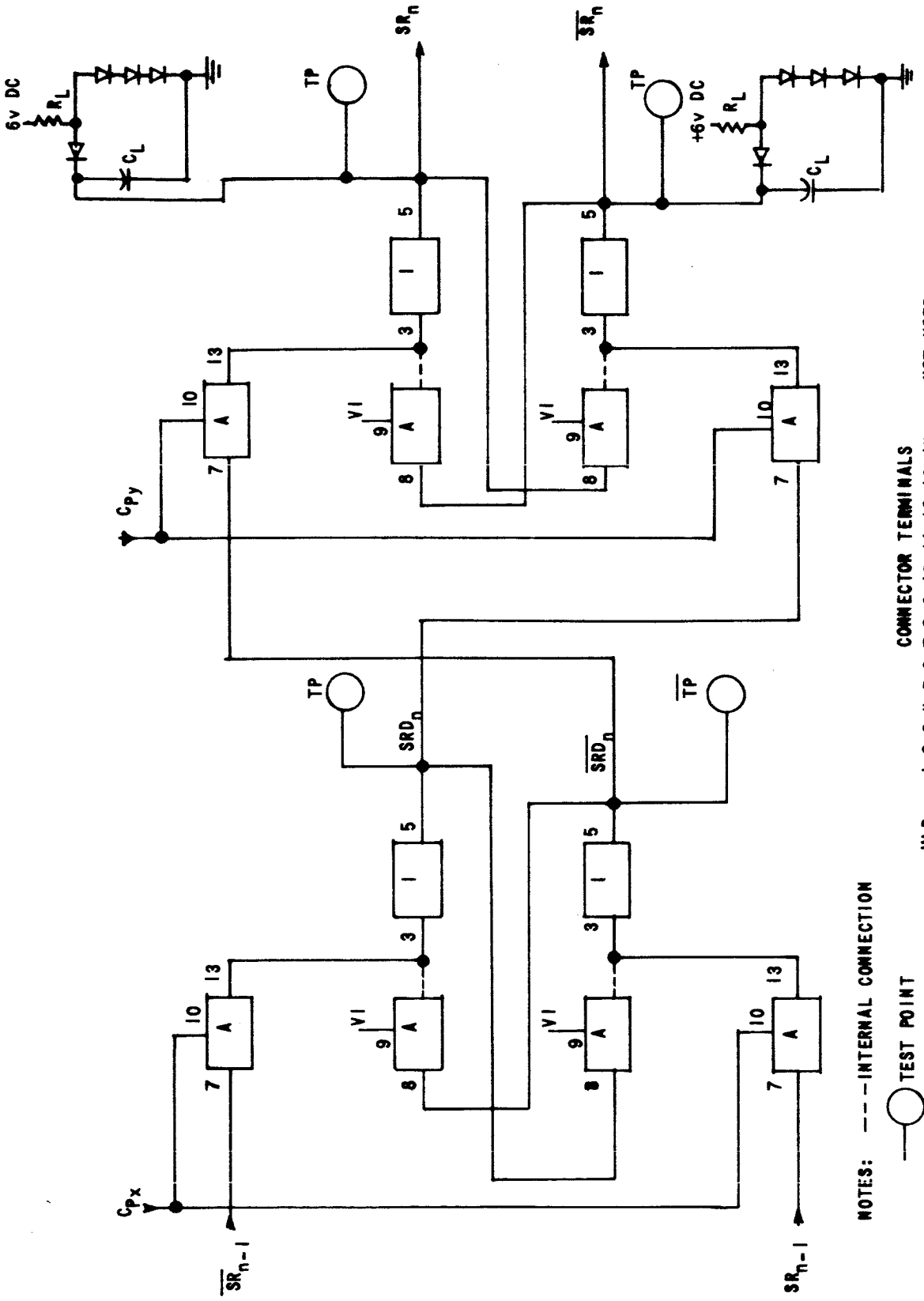


Figure 2.5 ULD SHIFT REGISTER STAGE

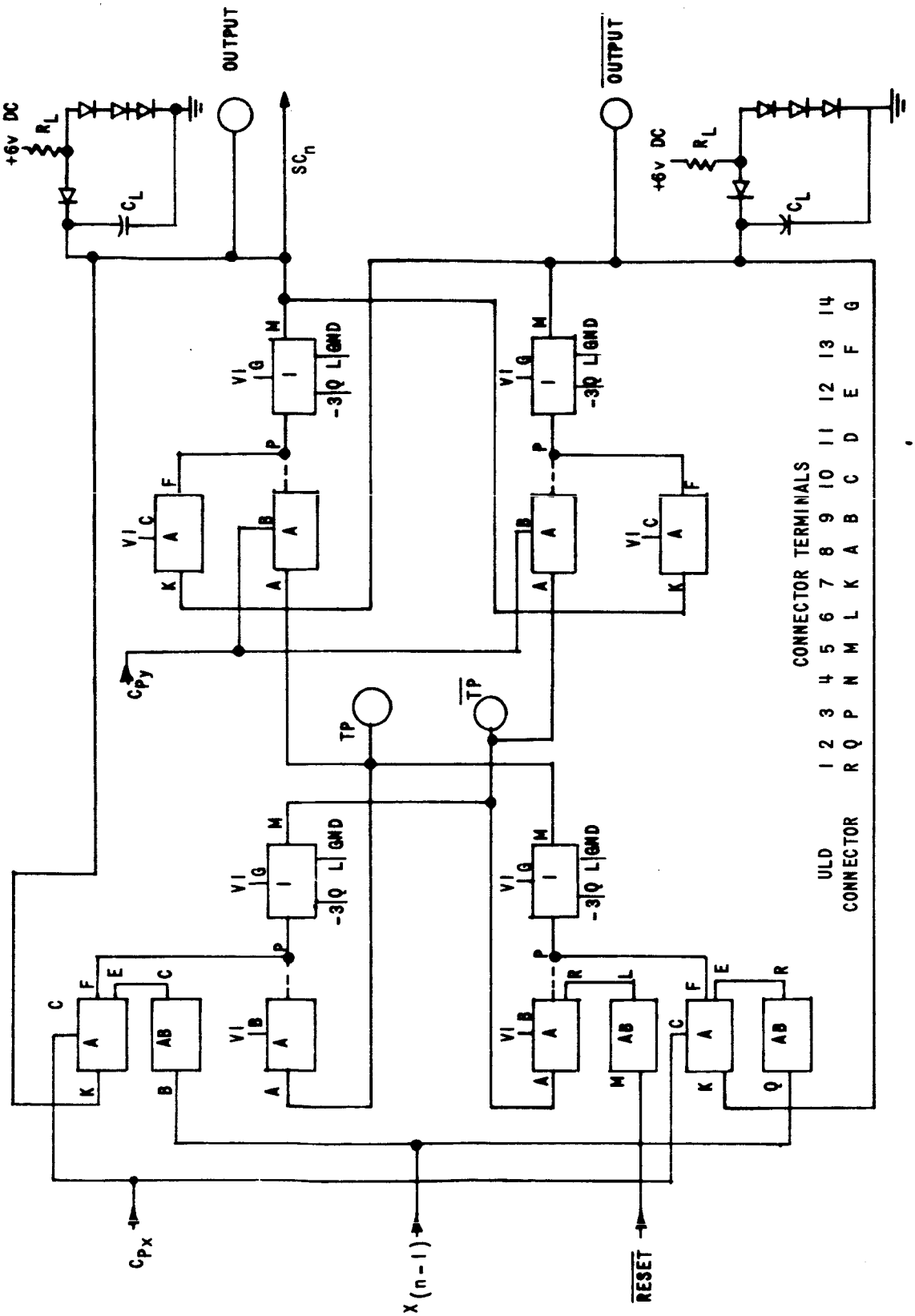


Figure 2.6 ULD SYNCHRONOUS COUNTER STAGE

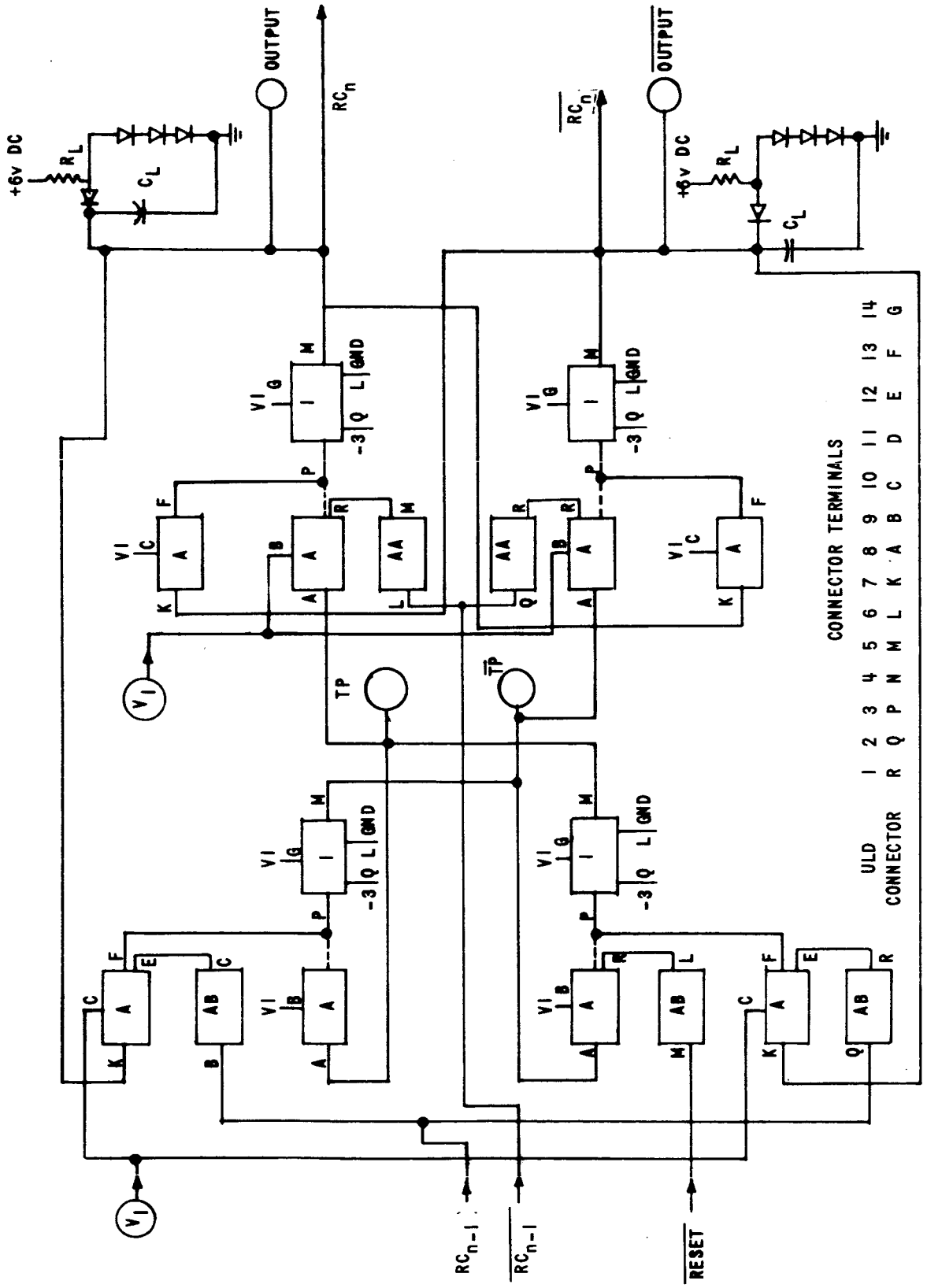


Figure 2.7 ULD RIPPLE COUNTER STAGE

The circuits selected as necessary to construct the three applications are the 930 DUAL 4 input NAND gate, the 931 single phase RS flip flop, the 932 DUAL 4 input NAND buffer and the 933 DUAL 4 input AND expander.

These circuits are all packaged in a 14 lead flat pack of .250"x .250" dimensions having the standard lead spacing of the 0.050 between adjacent leads. The case has a ceramic (alumina) base, in which the silicon circuit is bonded. A Kovar lead frame is bonded to the base and a ceramic lid is added to close the assembly. One mil aluminum wires are wedge bonded to make connection between pads on the integrated circuit chip and the lead frame.

The Fairchild DTL circuits differ from the standard DTL in that a transistor is used in place of a diode.[3] Referring to Figure 2.8a, transistor T1 replaces a diode. The collector of T1 is connected to a tap between R1 and R2. When an input diode, such as A, is grounded, the load current reflected into the output of the driving circuit is determined by the sum of R1 and R2. But, when all input diodes are back biased, the base drive current for T2 is determined by R2. Thus, a higher base drive current is obtained, and a better compromise between fan out and noise margin can be obtained.

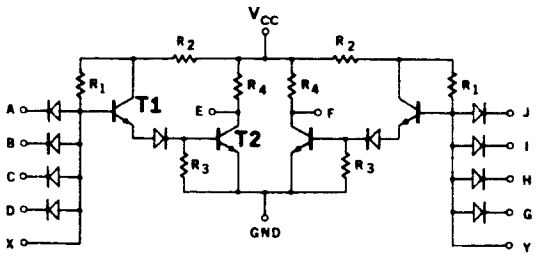
The 932 dual NAND buffer gate shown in Figure 2.8b is logically the same as the 930 but is rated for a fan out of 25. It contains a Darlington amplifier arrangement and an output pull-up transistor, similar to the Sylvania circuits, and should be capable of driving large capacitive loads.

The 933 AND gate expander shown in Figure 2.8c is a DUAL 4 input diode network which can be used to expand the AND gate inputs of a 930 or 932 gates. AND-OR gate arrangements cannot be constructed with it, nor are there connections available to use the 933 to expand the inputs of the 931 flip flop.

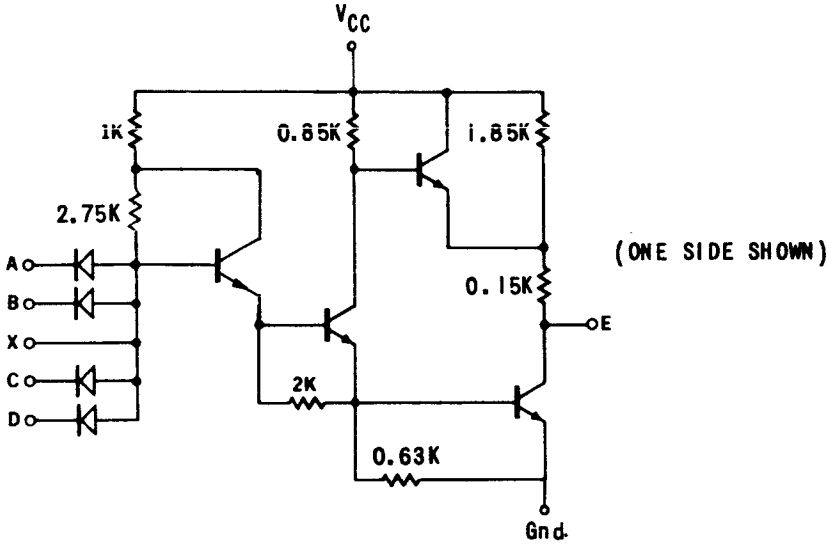
The 931 RS single phase clock flip flop contains both a master and slave flip flop and can be arranged as a complete shift register or counter stage in one module. The whole circuit is shown in Figure 2.9. Two clocked

TYPICAL RESISTOR VALUES

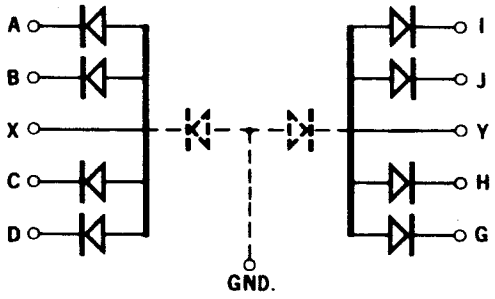
$R_1 = 2.0\ K\Omega$
$R_2 = 1.75\ K\Omega$
$R_3 = 5.00\ K\Omega$
$R_4 = 6.00\ K\Omega$



a. FAIRCHILD 930 DUAL NAND GATE

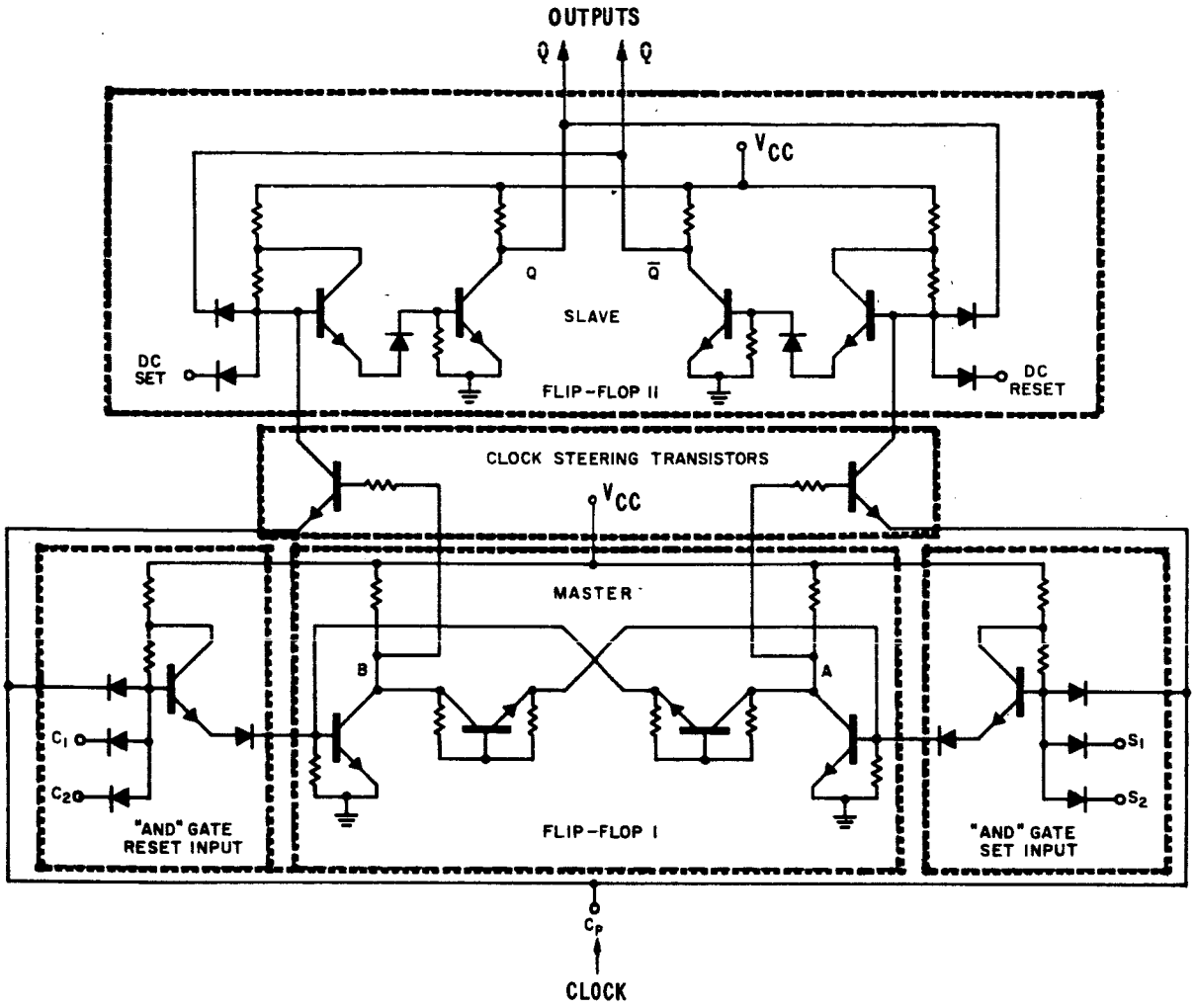


b. FAIRCHILD 932 DUAL NAND BUFFER ELEMENT



c. FAIRCHILD 933 AND EXPANDER ELEMENT

Figure 2.8



R-S MODE TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	INDETERMINATE

X - either an 0 or 1 may be present
1 - more positive than 0

Figure 2.9 EQUIVALENT CIRCUIT FOR THE FAIRCHILD 931 SINGLE PHASE CLOCKED RS FLIP-FLOP

set and two reset input gates are provided, in addition to a direct set and reset input. As the clock voltage rises from 0 to 5 volts, the clock steering transistors are biased off and the Set and Reset gates turned on. Transistor A and B respond to the input conditions, as shown in the truth table. As with the ULD and Sylvania flip flops, a ONE at both AND gate inputs is not an allowed condition. After an interval to allow flip flop I to latch up, the clock voltage will fall to zero volts. The input AND gates are turned off and the clock steering transistors turned on. The clock steering transistors override the direct input to the slave, flip flop II, and force it to the same condition as the master. During the transistion of Q to a ONE output, for example, the transistor Q will be turned off and its output rises to a one before the $\overline{Q}$ transistor is turned on and its output falls to a zero. Thus, during transition, both outputs will be one.

The direct Set and Reset inputs to the slave flip flop will be effective only during the time the clock voltage is positive. This restriction makes implementation of a reset logic for a synchronous or ripple counter impractical. A newer version of the 931, the 945, has an improved direct set and reset which should help cure some of the problems of the 931.

Aside from the reset logic, implementation of the three applications is very simple with the 931 flip flop. Figure 2.10 shows the connections used to implement one stage of the shift register. An additional set of inputs, C1 and S1, is available but not used. The synchronous counter stage is shown in Figure 2.11 with a reset logic which was instrumented to determine that it should not work. A further discussion is given on this in Section 4.3. The ripple counter connection is shown in Figure 2.12. A up counter, such as instrumented here, can be reset to only a condition of all ONES, and a down counter can be reset to all ZEROS. A general reset is not practical.

2.3 Sylvania SUHL Circuits

Sylvania SUHL integrated circuits use TTL circuits in an integrated circuit which strives for high speed, high noise immunity and high output drive capability.[4] A dual four input NAND gate, shown in Figure 2.13a shows the basic circuitry. A multi-emitter transistor T1 comprises the input, with its base resistor R1 tied to Vcc. If any of the emitters are connected to

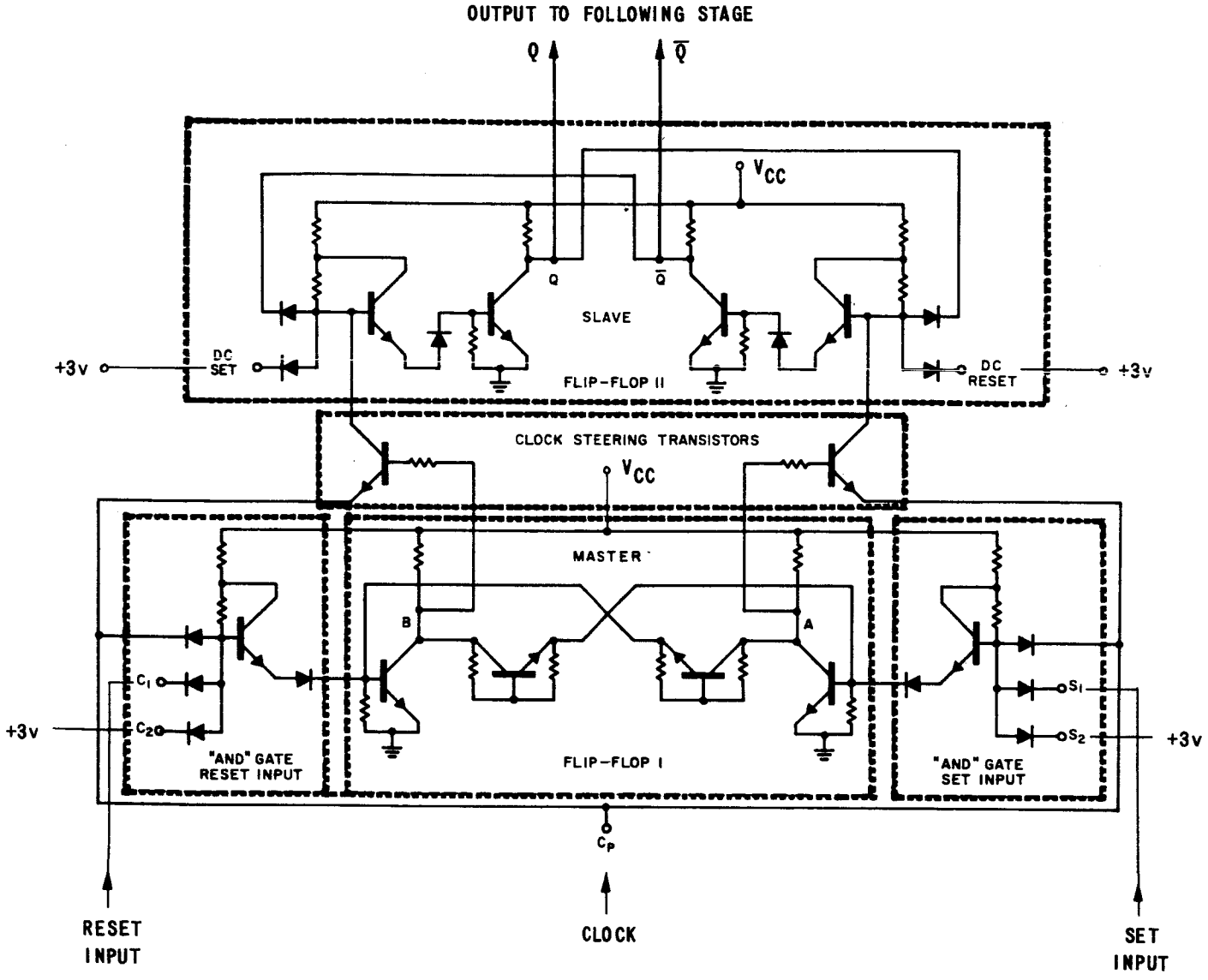


Figure 2.10 FAIRCHILD 931 FLIP FLOP CONNECTED AS A SHIFT REGISTER STAGE

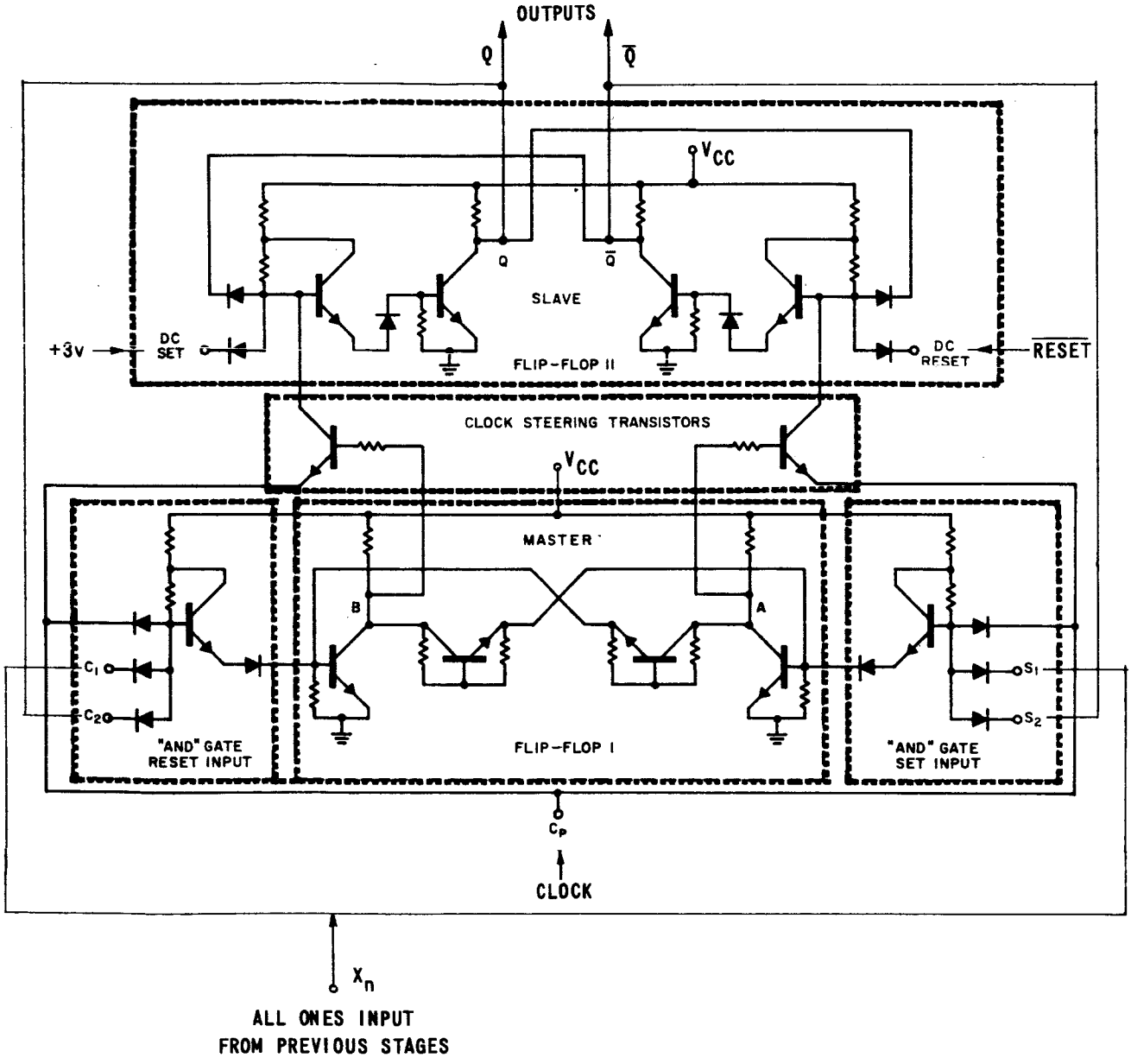


Figure 2.11 FAIRCHILD 931 FLIP FLOP CONNECTED AS A SYNCHRONOUS COUNTER STAGE

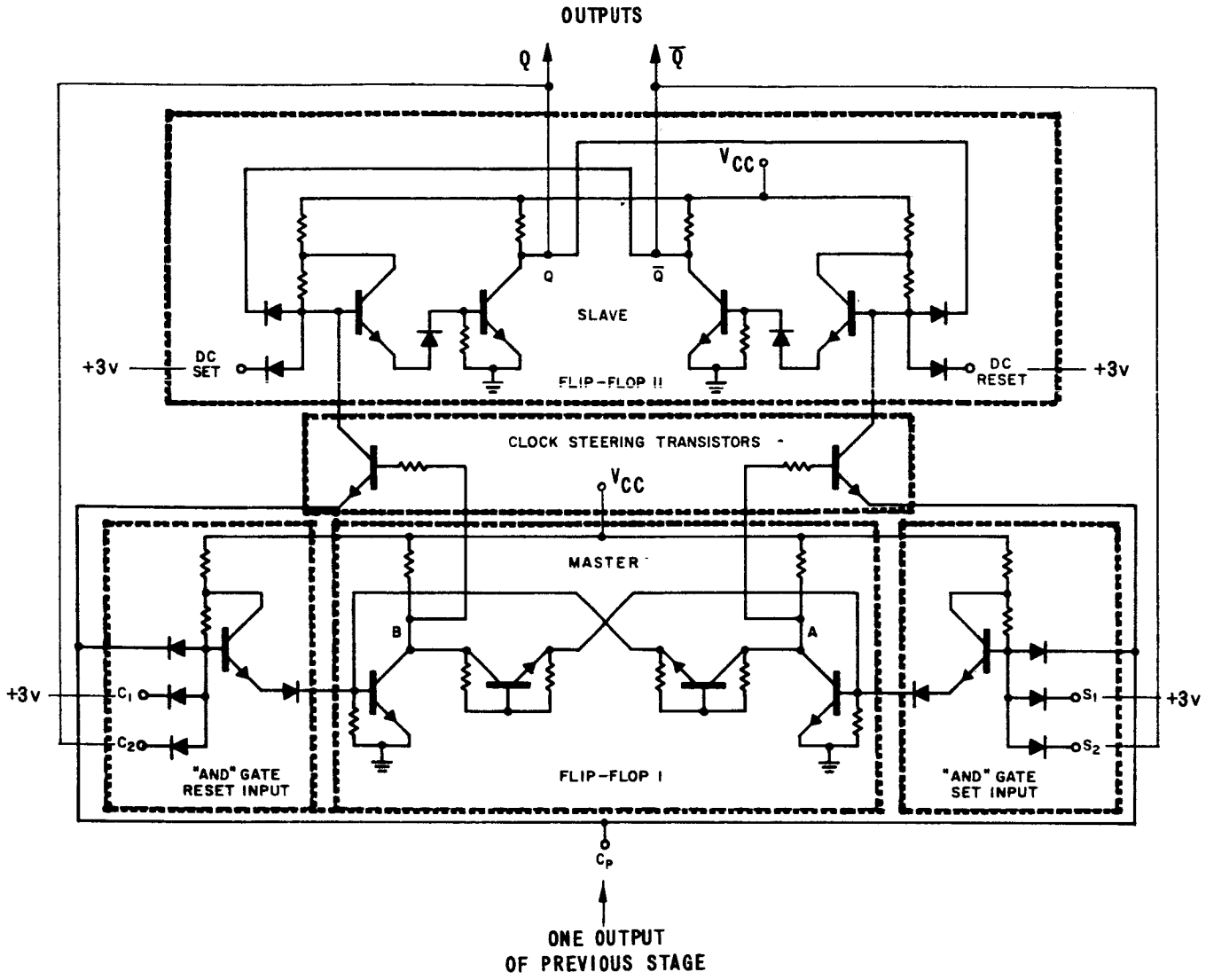
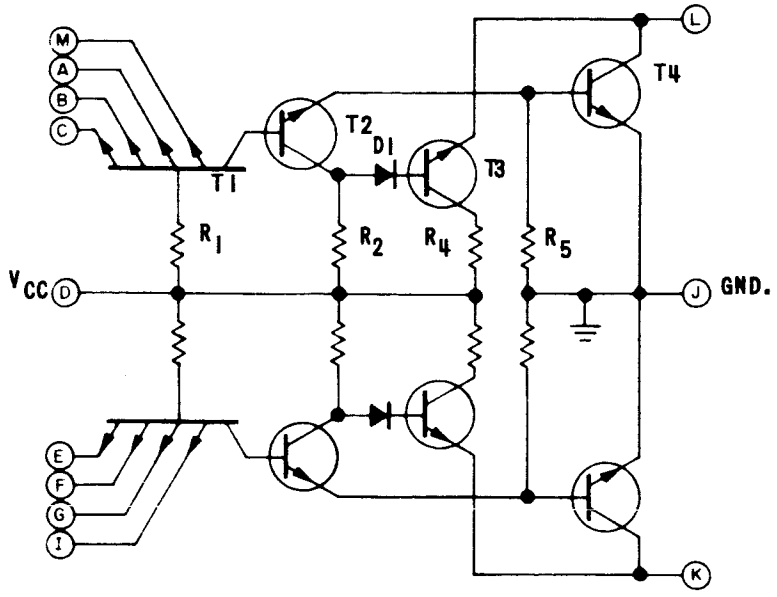
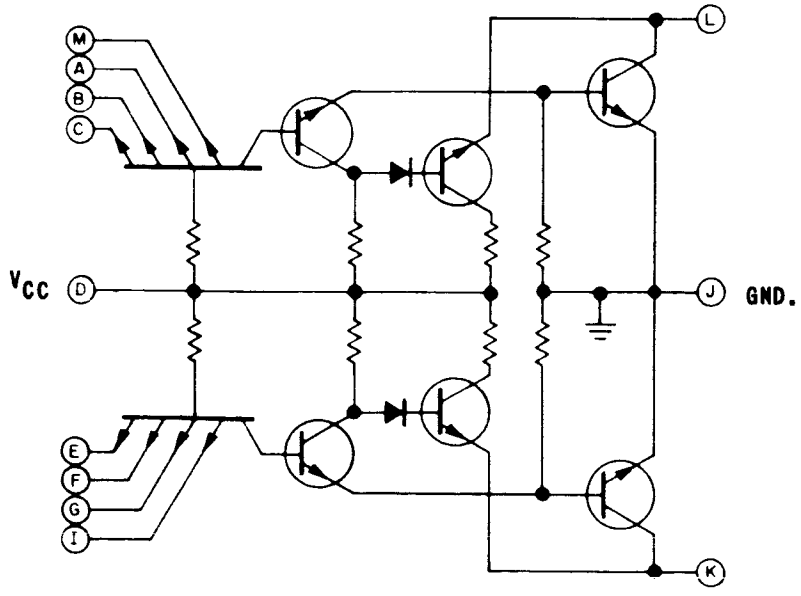


Figure 2.12 FAIRCHILD 931 FLIP-FLOP CONNECTED AS A RIPPLE COUNTER STAGE



a. EQUIVALENT CIRCUIT OF SYLVANIA SNG-14 DUAL FOUR INPUT NAND GATE



b. EQUIVALENT CIRCUIT OF SYLVANIA SNG-4B DUAL FOUR INPUT, HIGH FANOUT NAND GATE

Figure 2.13

ground (the collector of an ON transistor input), the current flowing from Vcc through R1 will be shunted to ground through that emitter. However, if all emitters are at 3 volts or higher, this current will flow to the base of transistor T2, a Darlington amplifier, and transistors T2 and T4 will conduct. How ever, when T2 and T4 are turned off, due to a grounded emitter at the input, T3 is turned on through R2 and D1 and remains on, charging a capacitive load, until the output L becomes positive enough to bias it off. Therefore R4 and T3 take the place of a pull up resistor but do not drain current when T4 is on and provide a low impedance path for charging current when T4 is off.

The SNG-4B shown in Figure 2.13 b works exactly the same but is rated for a worst case fan out of 20, where the SNG 14 is rated for a fan out of 7.

The SFF 12 two phase SR clocked flip flop, shown in Figure 2.14 uses the same type TTL circuitry, but has additional transistors for an OR function and has the cross coupling connected internally. Two input transistors, T1 and T1A, feed base current to two Darlington amplifiers, T2 and T2A, which are connected in parallel to provide an OR function. The output circuitry of T3 and T4 is exactly the same as in the SNG-14 and the fan out is 7. The feedback connection from output L to T1A is direct but all inputs and reset signals must go through the clocked input transistors. The logical problem of this arrangement will be discussed in the synchronous counter test section, where reset circuitry was instrumented.

The logical arrangement of the SFF 12 is such that if all inputs to the K side are positive (about 3 volts) and the clock signal is positive, T2 and T4 will be turned ON and the K output will be a logical ZERO. The truth table for the SFF 12 follows, where logical 0 = 0 volts and logical 1 = +3 volts.

TABLE 2.2

(I·E·F)	(A·B·M)	CLOCK	K	L
1	0	1	0	1
0	1	1	1	0
0	0	1	no change	
1	1	1	0	0 not allowed

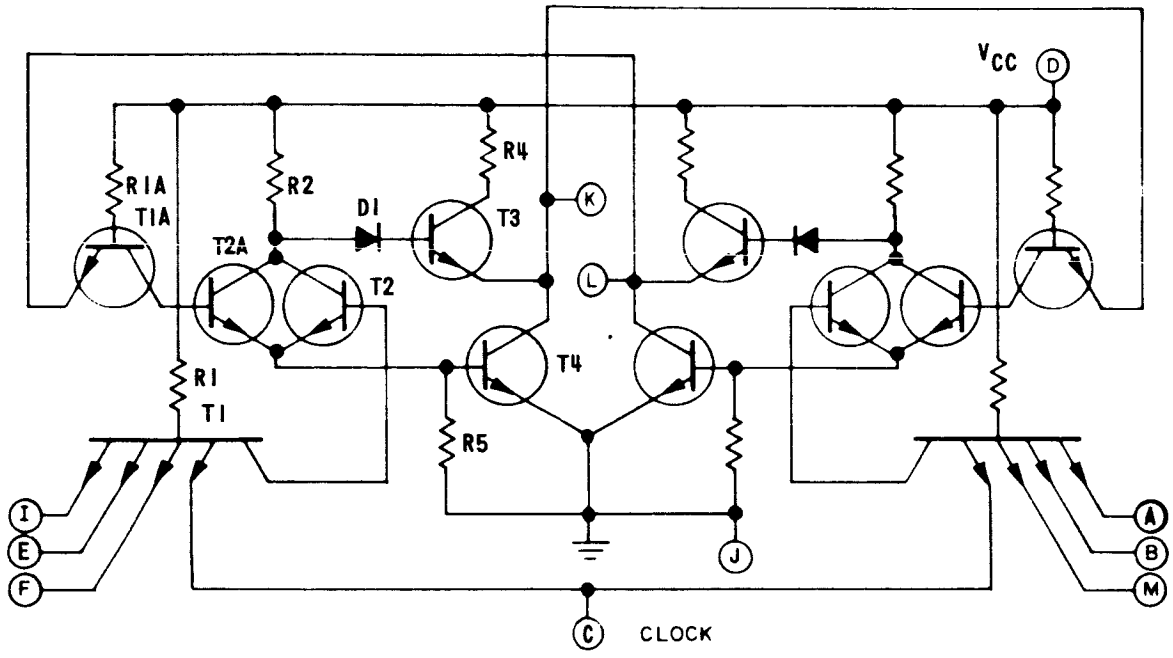


Figure 2.14 EQUIVALENT CIRCUIT DIAGRAM OF SYLVANIA SFF 12 TWO-PHASE RS CLOCKED FLIP-FLOP

The Sylvania SUHL circuits which were tested were housed in a 14 lead flat pack of .175 by .250 inch dimensions. The package is hard glass and the circuit is bonded to a kovar base plate to minimize the thermal drop to any mounting and heat sink plate. One mil aluminum wires are used to make connections from the pad on the silicon die to the package, in order to eliminate problems associated with "purple plague".[5]

The logical connection of two SFF 12 circuits to form one shift register stage is shown in Figure 2.15. The input flip flop is clocked by Cpx and the output by Cpy. Unused inputs are connected to +3 volts to eliminate their junction capacitance at the input.

The connection of two SFF 12 flip flops to form a stage of the synchronous counter is shown in Figure 2.16. The 1st or input flip flop is clocked by Cpx, and the output flip flop by Cpy in the two phase system. The input signal X_{n-1} will be a logical one (+ voltage) when all previous stages of the counter are ONE's. Then, when Cpx occurs, the input flip flop changes to a ONE, and when Cpy occurs, the output flip flop is changed to a ONE. The $\overline{\text{RESET}}$ signal at the input flip flop prevents the entry of a ONE into that flip flop when reset occurs. When Cpx occurs, either a ZERO is entered into the stage or a ONE is prevented from entering. All X_n signals are held at a logical ONE during reset so that they do not prevent gating in of reset signals.

Two SFF 12 flip flops are connected in Figure 2.17 to form one stage of a ripple counter. The input flip flop is clocked with the ONE output of the previous stage, while the output flip flop is clocked with the ZERO side. The operation is similar to the ULD ripple counter but reset is not practical with the SFF 12, since all of the inputs to either stage are controlled by the clock inputs, Since these clock inputs are the outputs of the previous stage, it is not possible to control these clock inputs as is done in a synchronous counter. Addition of a gate between stage C_{n-1} output and stage C_n clock inputs would allow gating to control this signal but would increase the delay carry problem inherent in the ripple counter and destroy the simplicity and economy of the ripple counter design.

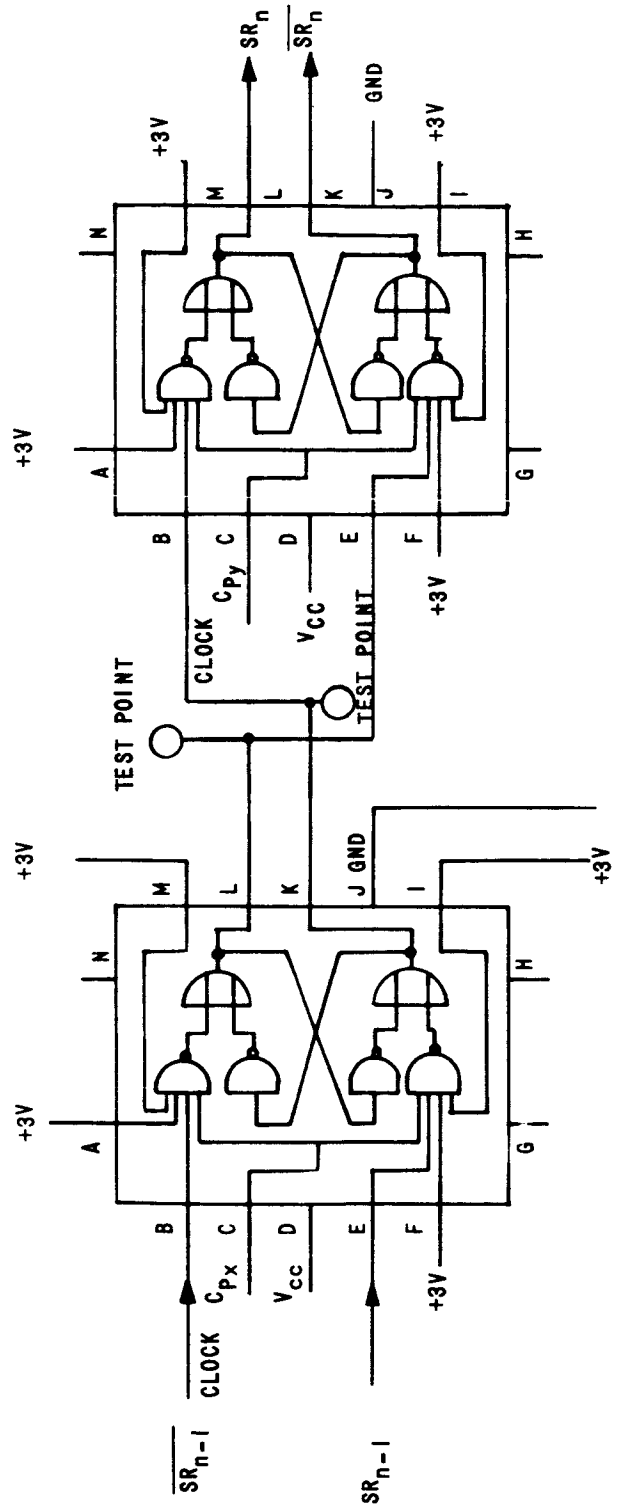


Figure 2.15 TWO SSF-12 MODULES CONNECTED TO FORM A SHIFT REGISTER STAGE

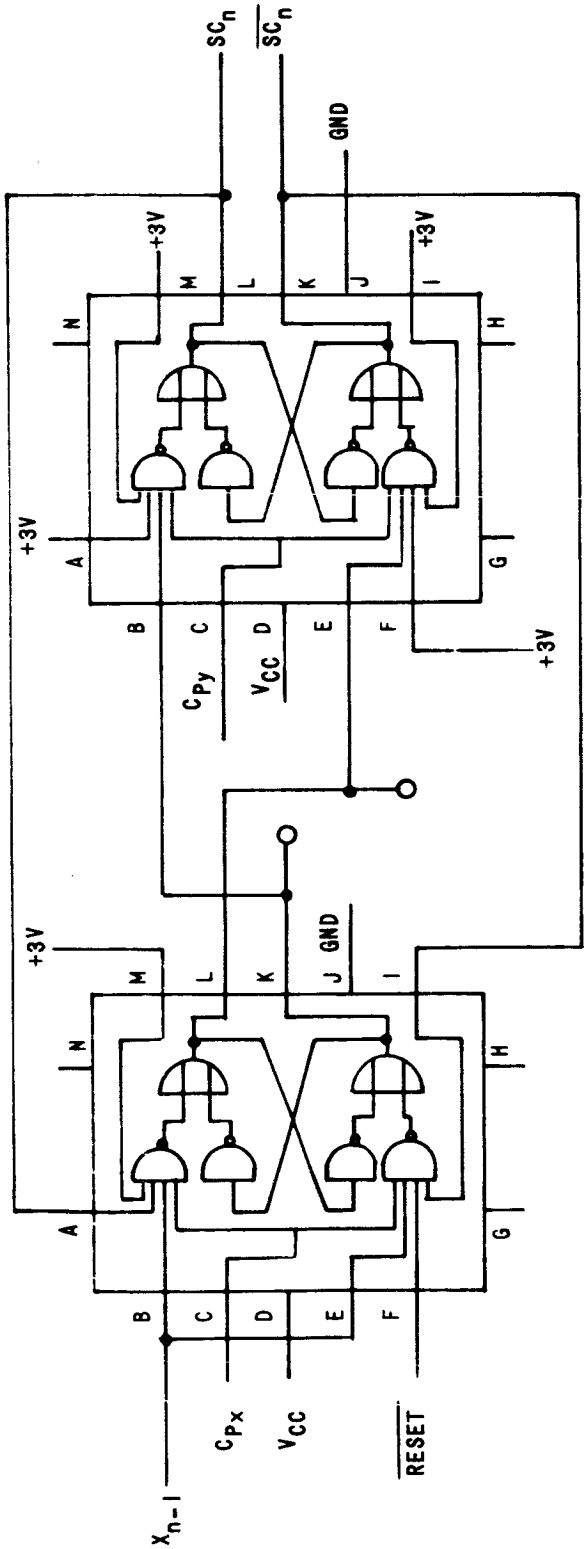


Figure 2.16 TWO SSF-12 MODULES CONNECTED TO FORM ONE STAGE OF THE SYNCHRONOUS COUNTER

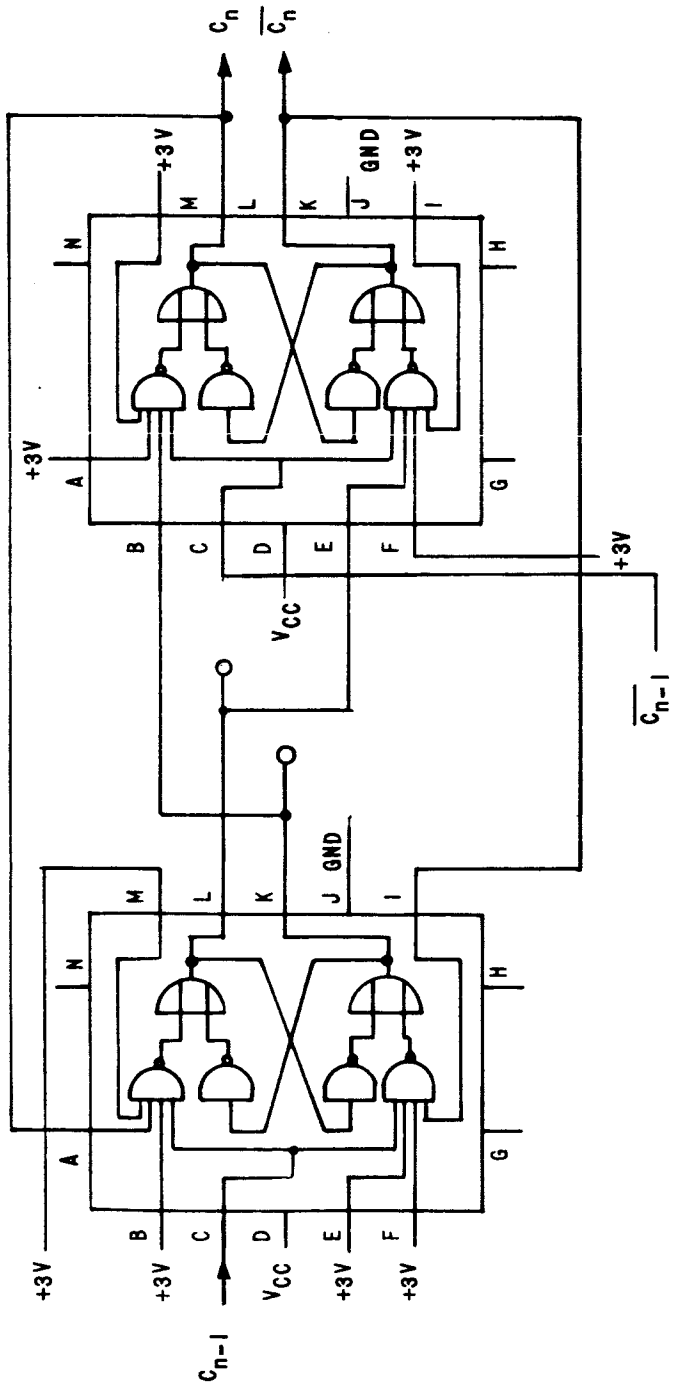


Figure 2.17 TWO SFF12 FLIP FLOPS CONNECTED TO FORM A RIPPLE COUNTER STAGE

Later versions of the SFF 12 brought out by Sylvania have direct set and reset input connections added which help cure part of the problems encountered in design of resets of counters. Referring to Figure 2.14 an additional emitter has been added to T1A and its other side counterpart, and these connections brought out.

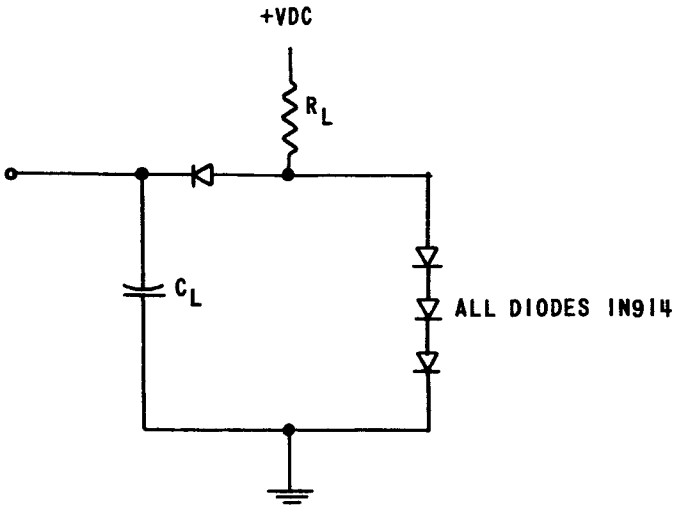
2.4 Simulated Load Circuits

The use of simulated loads is necessary in the testing of the various applications to evaluate the circuit's performance under realistic conditions. The large number of stages, and the higher fan-outs of some of the circuits tested would have required a prohibitive number of modules if actual inverters were used as loads.

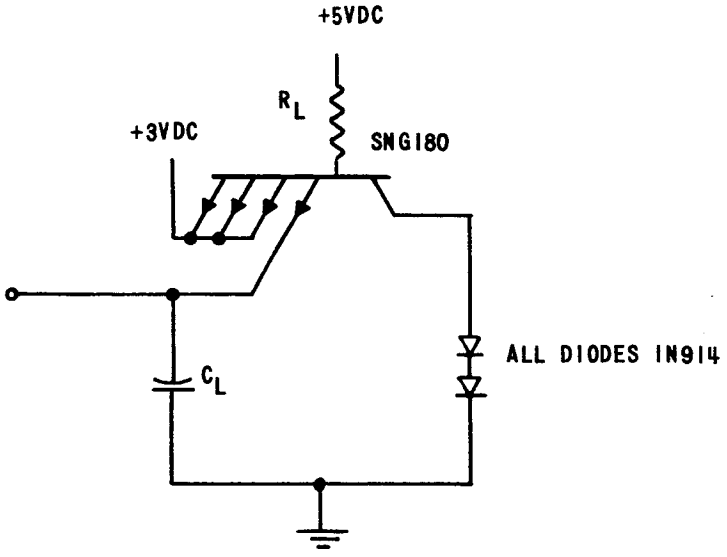
Since the ULD and Fairchild circuits are both DTL, the load circuit is the same for both. This circuit is shown in Figure 2.18a. Comparison to a standard DTL circuit such as the ULD shows that the load circuit looks like an AND-OR gate and inverter except that the base-emitter junction of the inverter transistor is replaced with a forward biased diode D4. Figure 2.19 shows a comparison curve of the static Vin-Iin curve for 3 ULD inverters and simulated load circuit for a fan-out of 3. Figure 2.20 shows the dynamic output of an ULD inverter loaded with 3 actual inverter loads and with a simulated load of 3. Similar comparisons were performed with Fairchild circuits and their simulated loads to insure that the test applications would faithfully represent actual circuitry.

Figure 2.18 b shows the simulated load for the Sylvania SUHL circuits. Here the integrated circuit, multi-emitter transistor SNG-180 was used to represent the input transistor of the TTL circuitry, since this circuit was recommended by Sylvania integrated circuitry personnel as the best circuit to simulate their loads. On Figure 2.21 the dynamic comparison is given between actual and simulated loads. The curves are so close it is difficult to see that two curves are present.

Simulated loads were computed on the basis of the worst case load presented by the input of a gate circuit. Fan-outs on all application tests

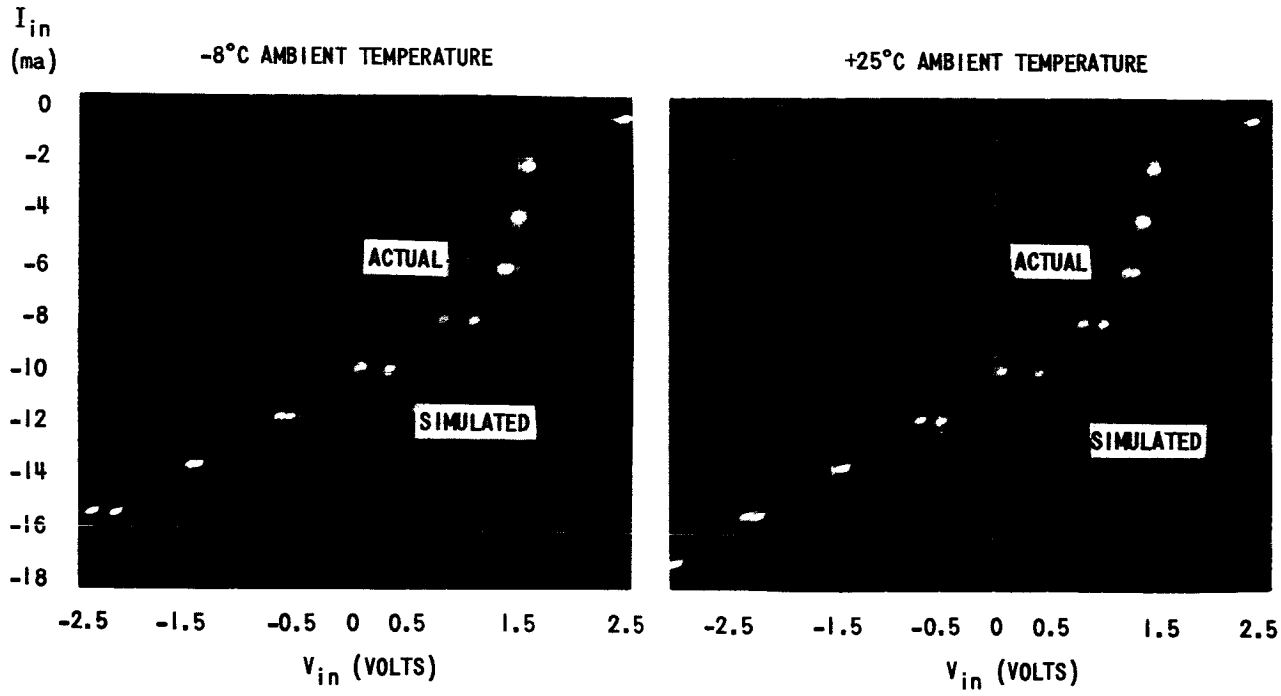


a. SIMULATED LOAD CIRCUIT FOR ULD AND FAIRCHILD DTL CIRCUITS



b. SIMULATED LOAD CIRCUIT FOR SYLVANIA TTL CIRCUITS

Figure 2.18



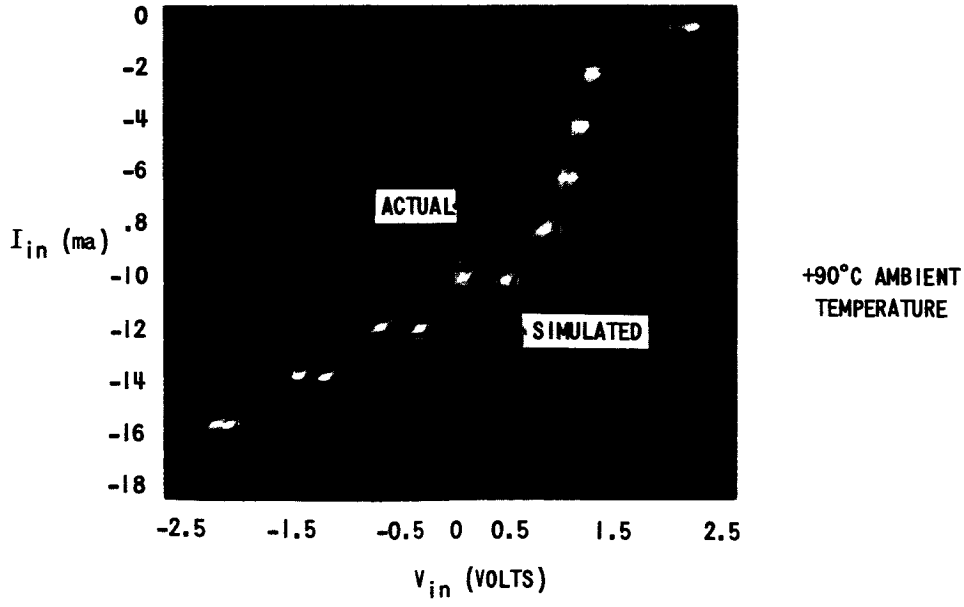


Figure 2.19 STATIC COMPARISON OF ULD ACTUAL AND SIMULATED LOADS FOR A FANOUT OF 3

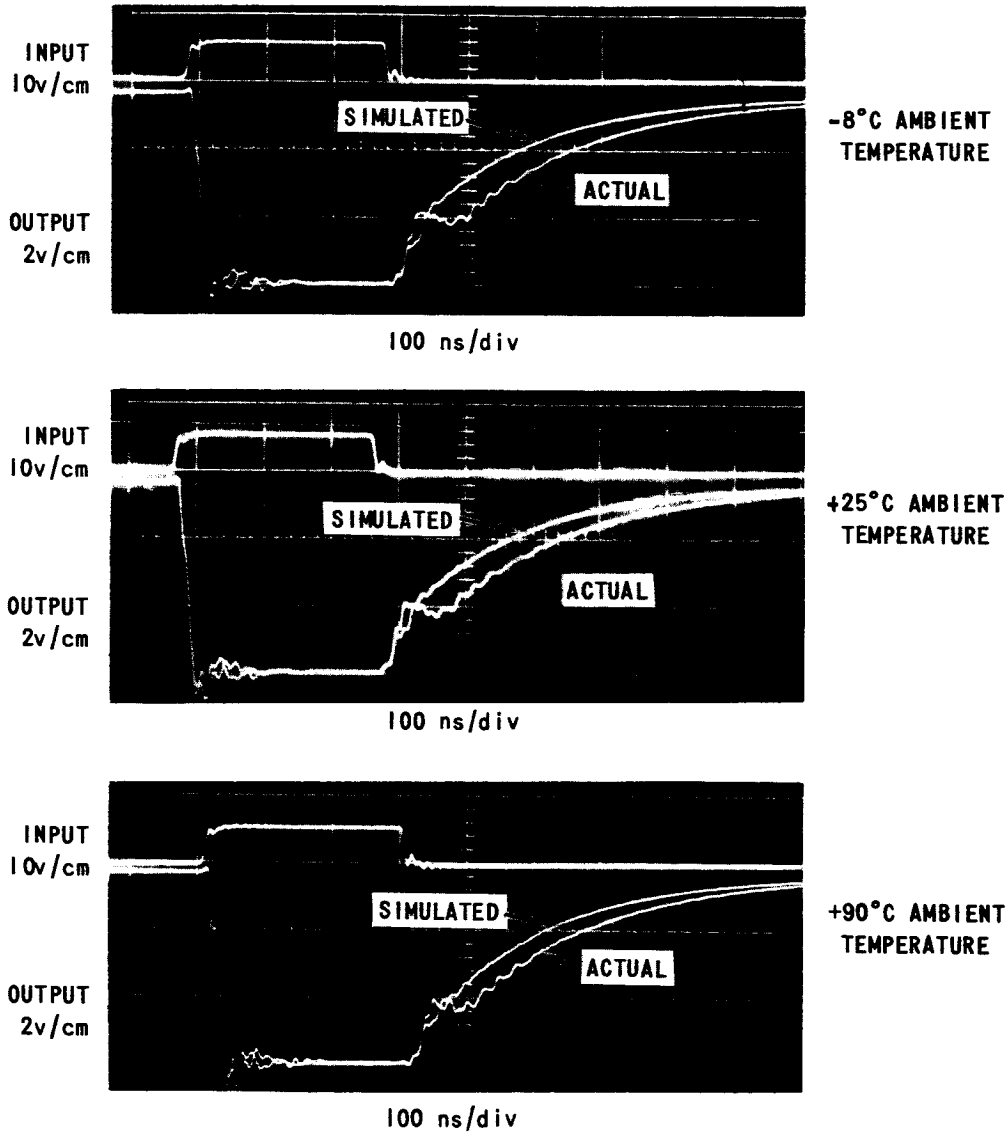
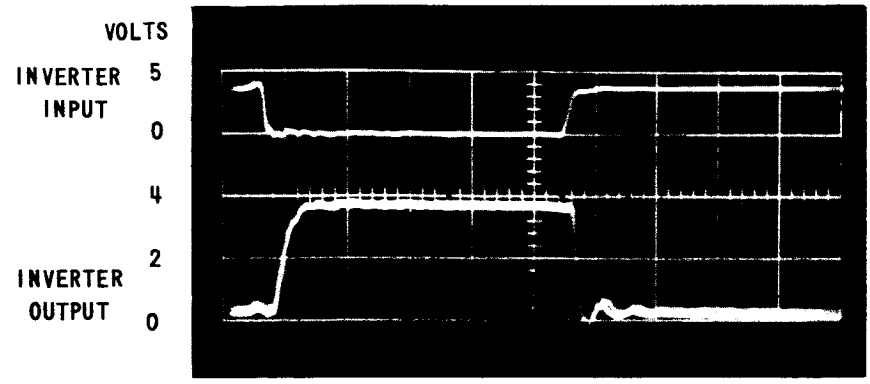
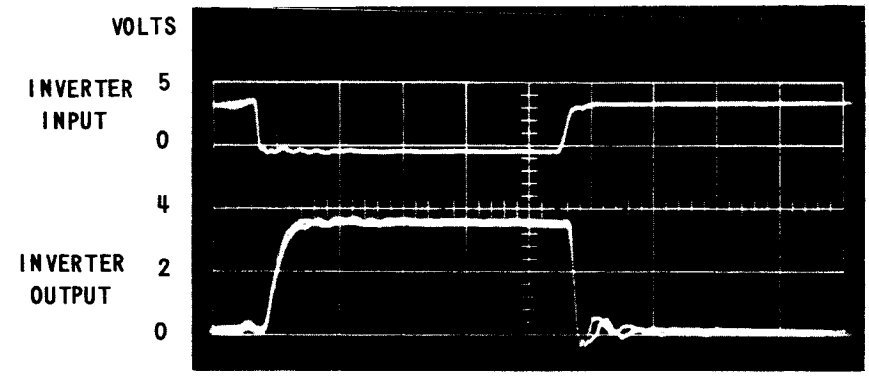


Figure 2.20 ULD INVERTER INPUT AND ULD INVERTER OUTPUT FOR ACTUAL AND SIMULATED LOADS AT FANOUT OF 3





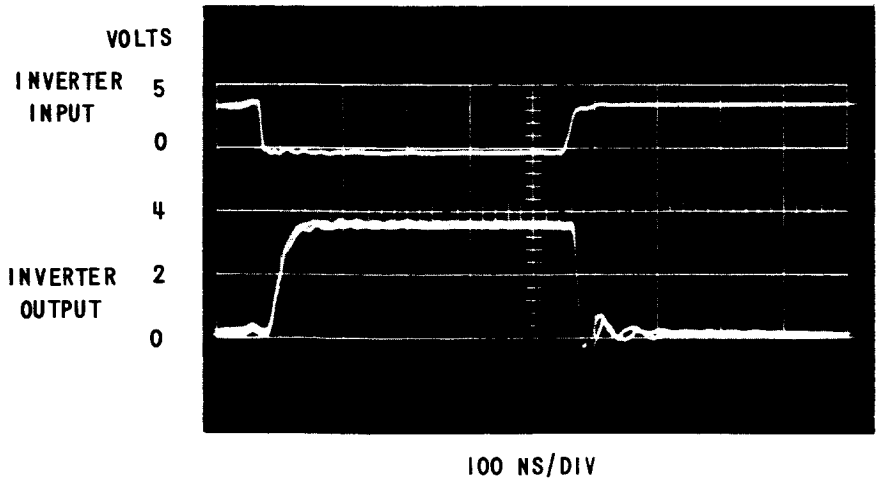


Figure 2.21 DYNAMIC COMPARISON OF SYLVANIA ACTUAL (SNG-14) AND SIMULATED LOADS FOR A FANOUT OF 4

were adjusted for the maximum fan-out as rated by the manufacturer. This loading is shown in the table in Section 2.1 for ULD inverters and was a fan-out of 7 for both Fairchild and Sylvania flip flops.

3.0 UNIT TEST SCHEDULE

The unit test schedule leading up to the network functional test was planned in three phases. The first rather straightforward phase was the acceptance test during which each unit was visually inspected for physical damage and numbered for identification. The second phase was the unit function test during which the electrical parameters of each unit were measured. Data sheets and photographs of interesting waveforms were recorded for each unit and the faulty ones were removed from the test cycle. The third and largest phase was the stress test. The first step in this phase was the non-operating bake-in in which the units were stored at maximum specified storage temperature. The bake-in was followed by the second unit functional test as a check to see if and how any parameters had varied because of the bake-in. The second step in the stress phase was the high voltage test in which the units were operated at maximum rated Vcc. A third unit functional test followed in search for signs of parameter variations. The final phase was the maximum load-high temperature test in which the units were subject to maximum operating temperatures under heavy fan-out conditions. This test was followed by the fourth and final unit functional test. The units which passed this stress phase were qualified to be used in the counter and shift register applications. Appendix A shows the progress of each unit through the test program.

3.1 Initial Unit Tests

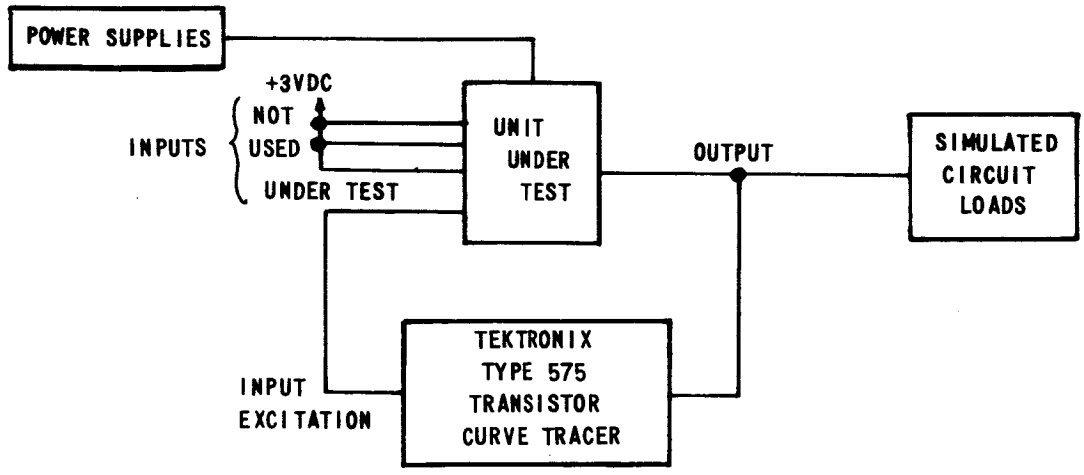
Parameters of the microminiature units were measured in the unit functional test under d-c conditions and at high frequencies. Characteristics measured were power dissipation, propagation delays, logic switching levels, and d-c noise margins. The basic test fixture included a socket and rotary switch arrangement which allowed each individual input to be sequentially selected for testing. The remaining inputs were reverse biased (connected to +3 VDC) and the output under test was connected to a load circuit to simulate actual loading or fan-out conditions. The test was conducted at room temperature (approximately 25°C) and at the optimum power supply voltages recommended in the manufacturer's specifications. Due to the variation in the logic lines,

a separate test fixture was used for each line. The fabrication and layouts of the various test fixtures were kept as similar as possible to eliminate measurement discrepancies in comparing the characteristics of the various logic lines.

3.1.1 Static Unit Tests

The unit test was conducted in two parts. The d-c characteristics were investigated in the static test and the dynamic test deals with the characteristics at 1 Mc. The equipment involved in the static test (see Figure 3.1) included regulated power supplies, the unit test fixture and a TEXTRONIX 575 transistor curve tracer. The curve tracer generates the necessary excitation waveforms and presents a CRT display of the characteristics of interest.

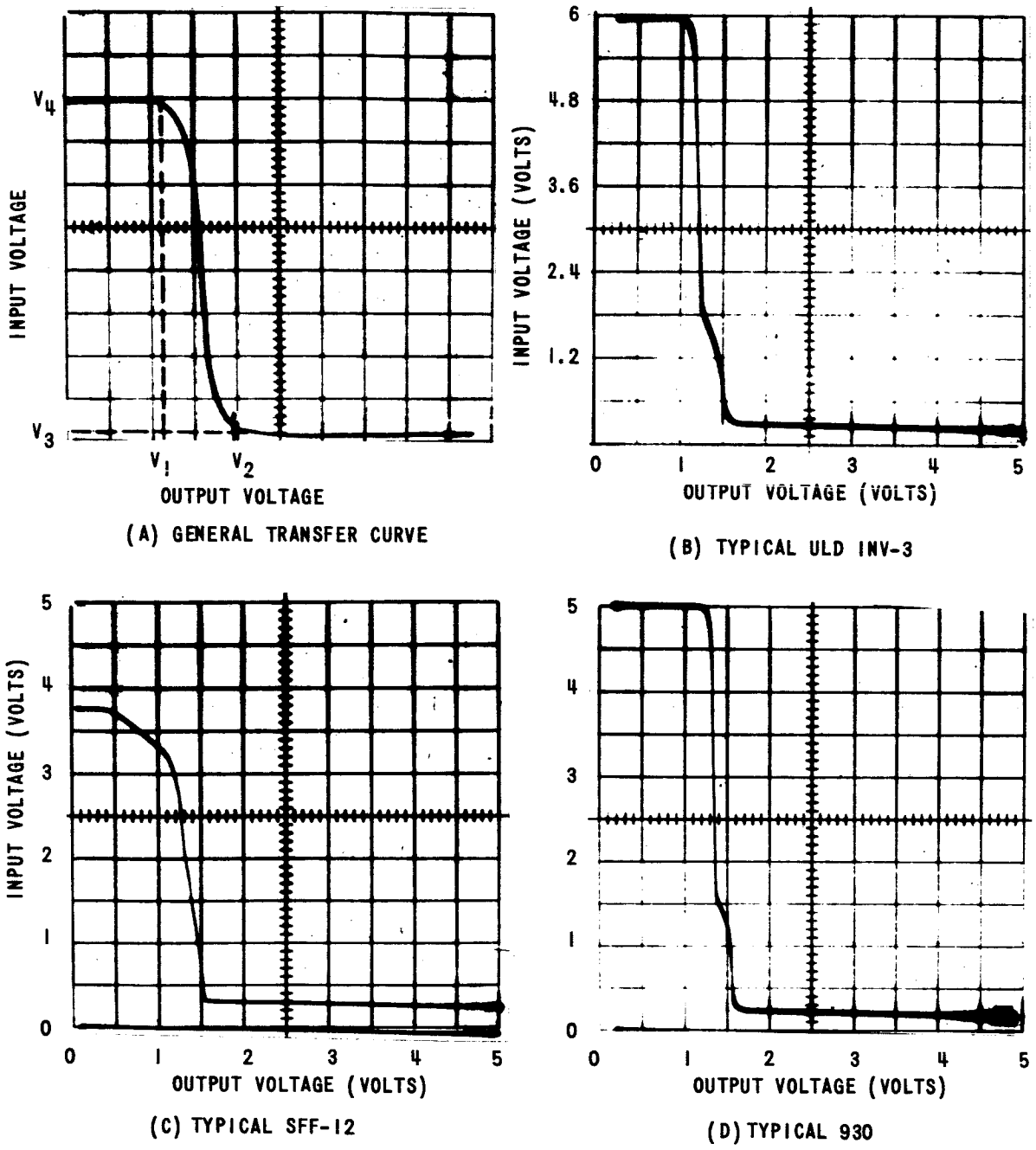
Input-output voltage transfer characteristics (see Fig. 3.2) were plotted for the ULD inverter, the Sylvania set-reset triggered flip-flop (SFF 12), dual NAND gates (SNG-4B and SNG-14) the Fairchild DTL clocked flip-flop (931), dual-gate element (930) and dual buffer element (932). The voltage transfer curve has input voltage plotted along the horizontal axis and output voltage along the vertical axis. The input sweep was a 5.0 volt peak, fullwave rectified 60 cycle sine wave generated by the collector sweep generator in the curve tracer. On Fig. 3.2A, V_1 is the maximum input voltage (ZERO logic level) for which the output voltage is a logical ONE (V_4). V_2 is the minimum input voltage (ONE logic level) for which the output voltage is a logical ZERO (V_3). This curve defines the characteristics of the unit under test at the standard test conditions and it does not reflect maximum or minimum limits. These limits can be found in the manufacturer's specifications and they serve as a guide to the performance of the unit under test.



UNIT UNDER TEST	SIMULATED LOAD		SUPPLY VOLTAGE	INPUT EXCITATION	TYPICAL RESPONSE	
	FAN OUT	CAPACITANCE LOAD			TYPE	LIMIT
ULD						
AA-3 (GATE)	-	-	Vcc 6V	.5MA/STEP 0-3MA	V_{IN}	-2.5V TO +2.5V
AB-3 (GATE)	-	-	Vcc 6V	.5MA/STEP 0-3MA	V_{IN}	-2.5 TO +2.5V
INV-3 (INVERTER)	*42MA	50 pf	Vbb -3V Vcc 6V	0-5 PEAK	V_{OUT}	+.24V TO +6V
SYLVANIA						
SNG-4B! (GATE)	15	60 pf	Vcc 5V	0-5V PEAK	V_{OUT}	+.20V TO +3.7V
SNG -14 (GATE)	7	30 pf	Vcc 5V	0-5V PEAK	V_{OUT}	+.20V TO +3.7V
SFF - 12 (FLIP-FLOP)	7	30 pf	Vcc 5V	0-5V PEAK	V_{OUT}	+.30V TO +3.7V
FAIRCHILD						
930 (GATE)	5.5	30 pf	Vcc 5V	0-5V PEAK	V_{OUT}	+.25V TO +5V
931 (FLIP-FLOP)	5	30 pf	Vcc 5V	0-5V PEAK	V_{OUT}	+.25V TO +5V
932 (GATE)	10	100 pf	Vcc 5V	0-5V PEAK	V_{OUT}	+.25V TO +5V

NOTE: * 42MA IS THE MAXIMUM COLLECTOR CURRENT ACCORDING TO SPECIFICATIONS. (F.O. ≈12)

Figure 3.1 UNIT TEST STATIC TRANSFER CHARACTERISTICS



NOTE: The Sylvania unit transfer curve has a double knee break rather than the simple curve depicted in Figure A. V_4 is considered to be at the second, or lower knee.

Figure 3.2 INPUT-OUTPUT VOLTAGE TRANSFER CHARACTERISTICS

The d-c noise margin can also be obtained from the voltage transfer curve. The d-c noise margin N is the peak noise voltage which may appear on the input, in addition to the logic level, without causing false triggering of the output. N must be specified as both positive N+ and negative N- and its magnitude is defined in the following manner.[6] Consider the case where two two-port networks with voltage transfer characteristics similar to those in Figure 3.2 are cascaded as shown in Figure 3.3. Noise generated on the input line to network B could cause false triggering of output V_0. N+ is defined as:

$$N+ = V_1 - V_3$$

Since this is the peak positive noise voltage that can be added to output V_0 and still be interpreted as a logical ZERO by the input of network B. N- is defined as:

$$N- = V_4 - V_2$$

which is the peak value of negative noise that can be added to output V_0 and still be interpreted as a logical ONE by the input of network B. Typical values found for N+ and N- are listed in Table 3.1.

TABLE 3.1

Unit Type	Typical Values	
	N+	N-
ULD		
INV-3	.9 volts	4.4 volts
Sylvania		
SNG-4B	1.0 volts	2.2 volts
SNG-14	1.0 volts	2.2 volts
SFF-12	.95 volts	2.1 volts
Fairchild		
930	1.1 volts	3.4 volts
931	1.0 volts	3.4 volts
932	1.1 volts	3.4 volts

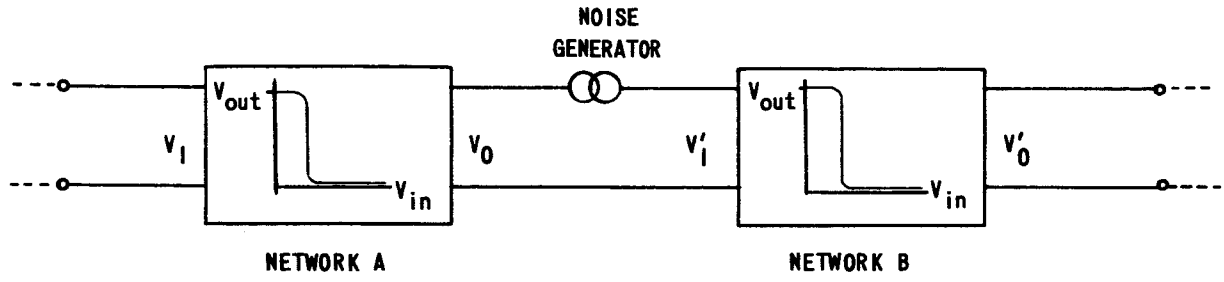


Figure 3.3 NETWORKS WITH NOISE

Input voltage-current impedance characteristic curves (see Fig. 3.4) were plotted for the ULD gates (AA-3 and AB-3) with input current along the vertical axis and input voltage along the horizontal axis. The input excitation was a .5 ma/step current waveform generated by the base step generator of the curve tracer. The slope of the curve in the region where the current is very negative is constant and equal to $\frac{1}{R}$, the reciprocal of the AND-gate resistor. The current where the curve intercepts the zero voltage axis, I_{Vo}, is of interest since this represents the load current for a ZERO logic level. This current must be supplied by the output collector resistor and therefore determines the fan-out configuration. The curve reflects the characteristics of the unit under the test conditions set forth and not the limiting values specified by the manufacturer. The typical value for R was 2.3K and I_{Vo} was 2.1 ma for both gate types.

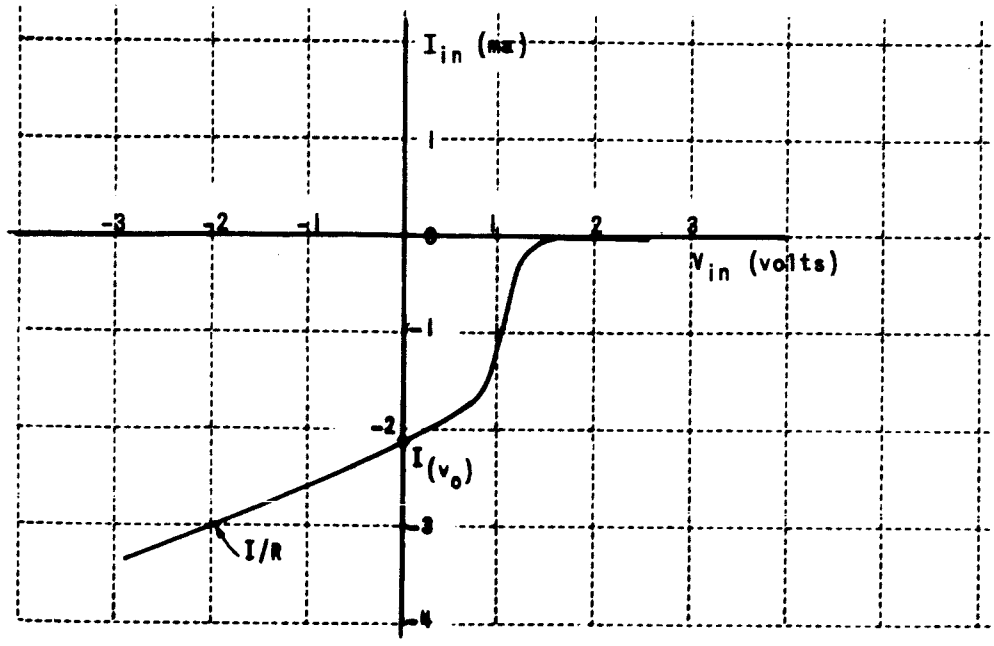


Figure 3.4 ULD INPUT IMPEDANCE CHARACTERISTICS

The simulated load used for the ULD gates (AA and AB) was three IN914 diodes in series tied between the gate output and ground, thus simulating the condition of connecting the gate output into pin 1 of the inverter. The load for the ULD inverter was 50 picofarads and a collector load current of 42 ma to ground. In testing the ULD inverter package, the additional expansion gate was ANDED with the inverter input by connecting pin 1 to 12 and pin 10 was left open. The 1.5K AND gate resistor was used during this test which left the 2.5K AND resistor untested during the unit functional test. The 2.5K gate resistor was used in the shift register and counter applications.

The Sylvania load on the output of the unit under test represented a capacitance load of 30 pf and a current load representing a maximum fan-out of 7 for the SNG-14 and SFF 12 units. A capacitance load of 60 pf and a current load representing a maximum fan-out of 15 was applied to the SNG-4B outputs.

The Fairchild simulated load represents a capacitance load of 30 pf and a current load for a maximum fan-out of 5 1/2 on the output of the 930 gate and a maximum fan-out of 5 on the flip-flop. A capacitance load of 100 pf and a current load representing a fan-out of 10 was used for the 932 gate outputs. Due to the complexity of the 931 flip-flop, the static test was restricted to the slave flip-flop section, using the preset gates as inputs and connecting the clock input to +3 VDC. Due to the simplicity of the DTuL 933 dual four-input expander, the unit functional test consisted of an ohmic measurement of forward and reverse resistance of each diode.

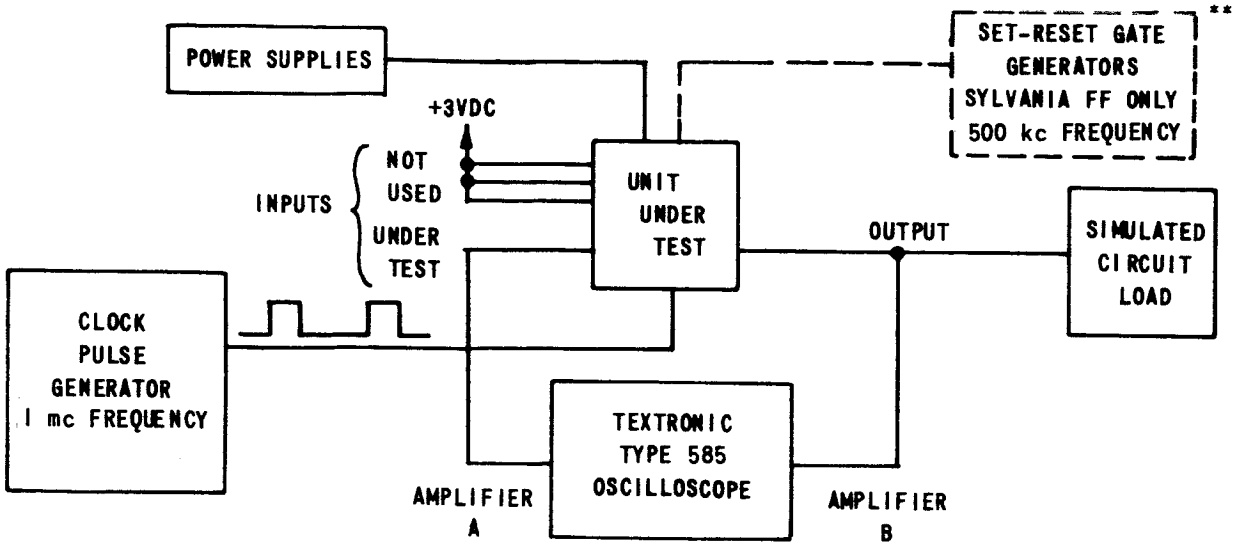
3.1.2 Dynamic Unit Tests

The dynamic unit functional test equipment (see Fig. 3.5) included regulated power supplies, a Textronix type 585 oscilloscope with a type 82 dual channel plug-in amplifier, the unit test fixture, pulse generators, clock and gate buffer circuits and digital voltmeter. The input excitation was a 1 Mc clock pulse (See Fig. 3.6).

The ULD Clock pulse generator circuit (See Fig. 3.7) was taken from a IBM document 6110915 supplied by MSFC. The pulse generator used to drive the clock circuitry was a E-H Research Laboratory Model 139. For testing, all the input diodes were connected to +3 VDC and the clock pulse was connected to Pin 9 of the inverter package.

The Sylvania clock pulse was generated by driving an SNG-14 gate with the E-H model 139 pulse generator and using the output of the gate as the clock source (See Figure 3.8). In addition, set-reset gates had to be generated to facilitate the testing of the SFF-12 flip flop. The set gate was generated by an SNG-14 gate driven from an E-H model 138 pulse generator. The set gate was then fed into another SNG-14 gate to generate its complement for the reset gate. The E-H 138 Generator was triggered from the basic clock pulse timing source, the E-H 139.

The Fairchild clock was generated by driving the input of a 930 gate with the E-H model 139 pulse generator and using the output of the gate as the clock source. To achieve the rise time needed for the clock pulse, a 620 ohm pull-up resistor was connected between the 930 gate output



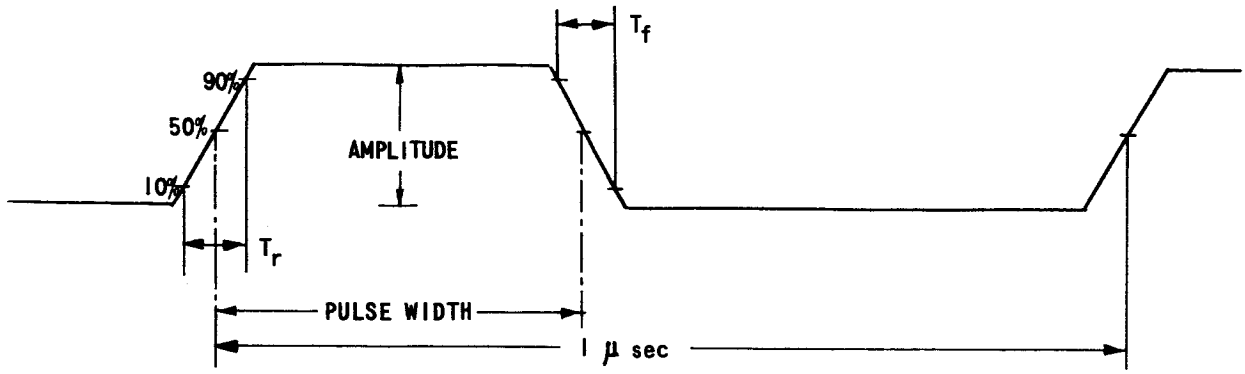
UNIT UNDER TEST	SIMULATED LOAD		SUPPLY VOLTAGE	*** CLOCK FREQUENCY	TYPICAL $\overline{Tpd}$
	FAN OUT	CAPACITANCE LOAD			
ULD					
INV-3 (INVERTER)	*42MA	50 pf	V_{bb} -3V V_{cc} 6V	1 MC	33 NS
SYLVANIA					
SNG -4B (GATE)	15	60 pf	V_{cc} 5V	1 MC	15 NS
SNG - 14 (GATE)	7	30 pf	V_{cc} 5V	1 MC	15 NS
SFF - 12 (FLIP-FLOP)	7	30 pf	V_{cc} 5V	1 MC	19 NS
FAIRCHILD					
930 (GATE)	5.5	30 pf	V_{cc} 5V	1 MC	26 NS
931 (FLIP-FLOP)	5	30 pf	V_{cc} 5V	1 MC	55 NS
932 (GATE)	10	100 pf	V_{cc} 5V	1 MC	26 NS

NOTES: * 42 MA IS THE MAXIMUM COLLECTOR CURRENT ACCORDING TO SPECIFICATIONS (F.O.≈12)

** SYLVANIA FLIP-FLOPS WERE TESTED IN SET - RESET MODE FAIRCHILD FLIP-FLOPS WERE TESTED IN J-K MODE.

*** CLOCK PULSE WAS ON FOR 400 NS AND OFF FOR 600 NS

Figure 3.5 UNIT TEST DYNAMIC TRANSFER CHARACTERISTICS



LOGIC LINE	AMPLITUDE	T_r	T_f	PULSE WIDTH
ULD	5.8 V	40 ns	20 ns	400 ns
SYLVANIA	4.0 V	11 ns	15 ns	200 ns
FAIRCHILD	3.6 V	55 ns	16 ns	150 ns

Figure 3.6 DYNAMIC UNIT FUNCTIONAL TEST CLOCK PULSE

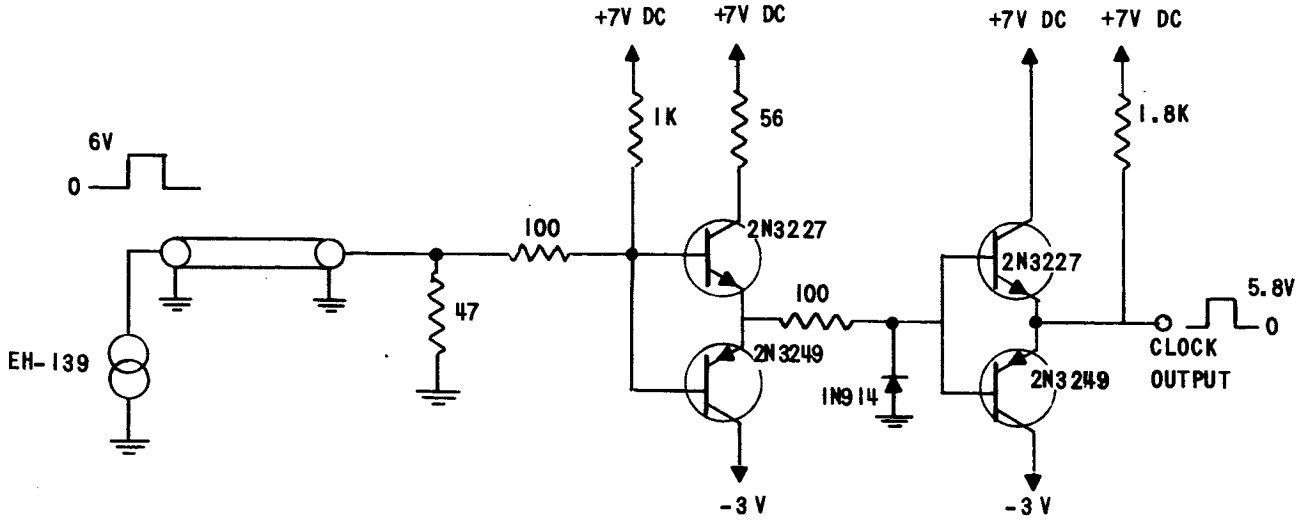


Figure 3.7 CLOCK GENERATOR CIRCUIT

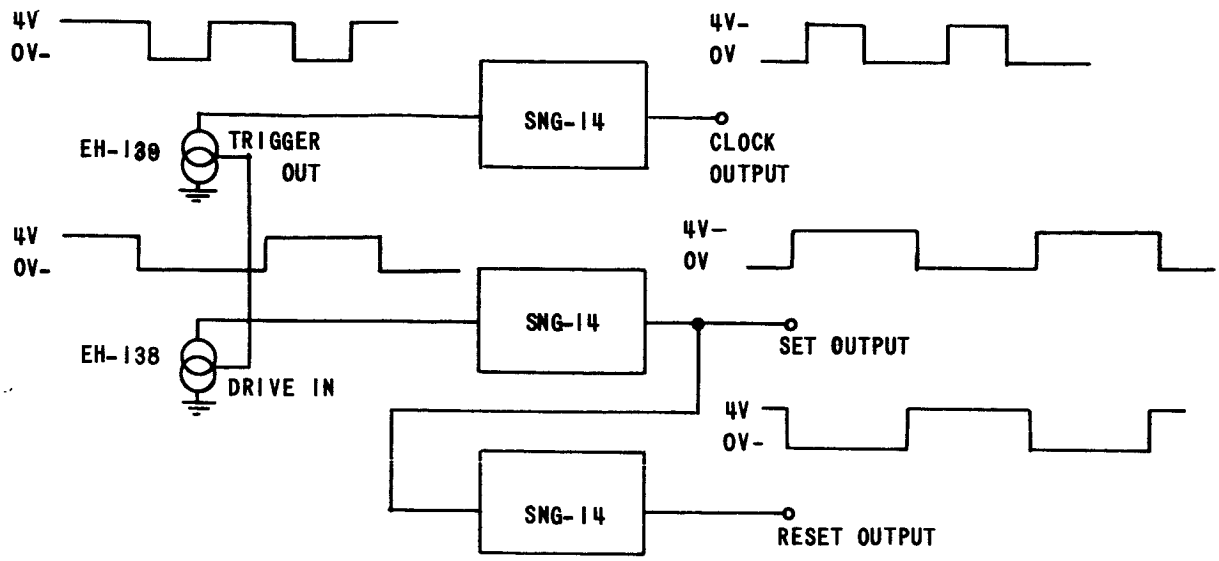


Figure 3.8 SYLVANIA CLOCK PULSE AND SET-RESET GATE GENERATORS

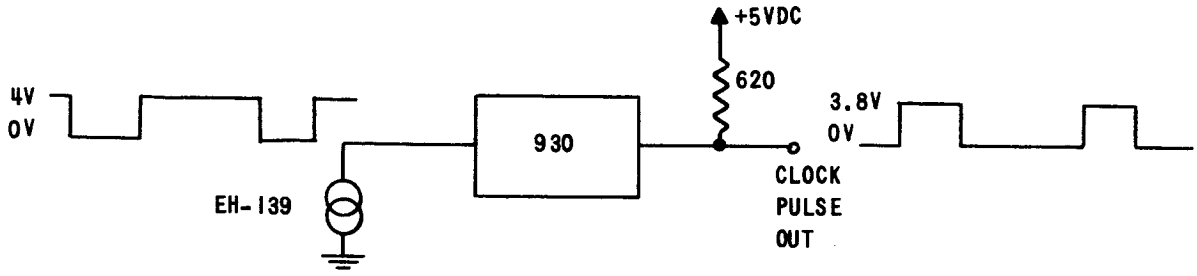


Figure 3.9 FAIRCHILD CLOCK PULSE GENERATOR

and +5 VDC supply (see Figure 3.9). The 931 flip flop dynamic test did not require additional gating as did the SFF 12 since it was tested in the J-K configuration by connecting Q back to S_1 and $\overline{Q}$ to C_1.

The average propagation delay $\overline{Tpd}$ from input to output was the primary characteristic studied in this dynamic mode. $\overline{Tpd}$ was taken to be the average of the output turn-on delay (Tpd +) and output turn-off delay (Tpd -). Tpd+ and Tpd- were measured at the 2DCD level for the ULD inverter, the 50% amplitude point for the Sylvania units and the 1.5 VDC level for the Fairchild units as recommended in the specifications. The actual Tpd+ measurement was made between clock fall and the output rise for all units. The Tpd- measurement was taken from the clock rise to the output fall for all units except the Fairchild 931 flip flop. In this case, Tpd- was taken from clock fall to output fall because the circuit configuration is such that the output switches only on the clock's falling edge. Typical values measured are listed in Table 3.2

TABLE 3.2

Unit Type	Typical Tpd+	Tpd-	$\overline{Tpd}$
UDL			
INV-3	20ns	45ns	33ns
Sylvania			
SFF-12	30ns	10ns	20ns
SNG-14	18ns	10ns	14ns
SNG-4B	18ns	10ns	14ns
Fairchild			
930	28ns	24ns	26ns
931	45ns	63ns	54ns
932	46ns	2ns	24ns

The power dissipation measurements were taken at the optimum supply voltages recommended in the specification, at the 1 Mc logic rate and at room temperature. Typical results are listed in Table 3.3

TABLE 3.3

Unit Type	Vcc	Average power dissipation per module
UDL		
INV-3*	6V	10.8 mw
	-3V	1.1 mw
Sylvania		
SNG-4B	5V	29.5 mw
SNG-14	5V	23.0 mw
SFF-12	5V	25.3 mw
Fairchild		
930	5V	17.2 mw
931	5V	33.6 mw
932	5V	67 mw

3.2 Stress Tests

The stress tests were designed to disclose early or potential circuit failures without changing the electrical characteristics of the circuits. Use of over-stress techniques to reveal failure modes would have potentially altered the characteristics of the units and materially changed the results of the application tests which followed. Thus, the circuits were operated up to, but not beyond, the limits of temperature, voltage and power dissipation specified by the manufacturer. Disruption of important application tests was considered to be less likely after eliminating most of the early failures. It is expected that any program of construction of a high reliability computer would require operation of individual units in a manner to eliminate early failures.

* Does not include clock power.

Three basic mechanisms were used to accelerate early failures in the circuits tested. These are baking, high voltage operation, and full load-high temperature operation. The failure mechanisms accelerated or detected by each test are: [7, 8]

BAKING--

a) Formation of hydrated aluminum from the aluminum conducting layer, due to excess moisture in the package.
b) Formation of hydrated aluminum accelerated by the presence of scratches or oxide steps.
c) Disappearance or absence of aluminum near bonds.
d) Formation of an electrical insulating layer between aluminum and silicon at interface of a window in the oxide.

FULL LOAD--HIGH TEMPERATURE--

a) Generally, those failures detected by baking.
b) Detection of severe scratching on conductors where the conductor can no longer handle the high current.

HIGH VOLTAGE--

a) Shorts from aluminum conductor layer to silicon through the silicon dioxide layer.
b) Shorts at pads at the edge of the die due to die scribing too close to the pad.
c) Ball bond overlapping the edge of the die.
d) Shorts between adjacent 1 mil leads connecting silicon die to the package lead frame.

3.2.1 Stress Test Procedure

The bake-in test stressed the units in an non-operating, elevated temperature environment. The test may be designed to accelerate any electro-chemical bonding or interface problems that might occur due to storing or operating the units at high temperatures. The UDL units were reverse-biased during the bake-in test. All diodes were connected between 15 VDC and the inverter transistors were biased off by applying +6 VDC

from collector to emitter and -3 VDC from base to emitter. All resistors were open circuited for this test. The UDL units were baked in an ambient 150°C environment for eight hours. The Fairchild and Sylvania units were baked with no voltages applied for eight hours at an ambient temperature of 150°C.

The high voltage stress test was conducted to insure that the units would operate at the specified maximum voltage. The test was conducted at room temperature (approximately 25°C) for two hours. The outputs of the units were monitored to insure that the units were functioning during the test. The maximum operating voltage of 8 VDC (Vcc max) was specified for the Fairchild and Sylvania units. The value for Vcc maximum used for the ULD units was derived from the maximum power dissipation figures given for the resistors. The INV and AA units were tested with Vcc at 8 VDC and AB units at 7.4 VDC. The circuit configuration for this test was similar to that of the dynamic unit function test. The standard 1 megacycle clocks generated by the unit test fixtures with the set-reset gates generated by the Sylvania fixture were used. The units were loaded with the same simulated load configurations as in the unit functional test. The ULD AA and AB gate inputs were all grounded and the AND-gate resistors were connected to Vcc.

The maximum load test was designed to insure that the units were capable of operating at extreme temperatures under heavy loading conditions. The maximum operating temperatures are specified for junction temperatures so that each rating was converted into an ambient temperature rating. The test was conducted using the same circuit configuration as the high voltage test with the following changes. Vcc for the ULD units was +6 VDC and the ambient temperature was 80°C. Vcc was +5 VDC for the Fairchild and Sylvania units while the ambient temperatures were 105°C for the Fairchild units and 110°C for Sylvania units. The test was conducted for two hours at this elevated temperature and the outputs were monitored to insure that the units were operating.

3.3 Results of Unit Stress Tests

3.3.1 Results of Unit Stress Tests on ULD Modules

The ULD modules were tested in two groups. Ten per cent of the units were put through the complete test including the 150°C eight hour bake-in. After the results of this test were known, the remaining 90 per cent of the units were put through the unit stress tests without the 150°C bake-in.

A total of 85 inverters were received. Of these there were 12 failures, all open resistors. Eight inverters were baked at 150°C and of these four developed subsequent failures. 76 inverters went through unit stress tests without being baked and of these there were eight failures. Of the units that were not baked all but one were initial failures. The one exception was a failure on the third unit test. The results shows a fifty per cent failure rate with the units that were baked and a ten per cent failure rate with the units that were not baked, and of this, the ten per cent represents approximately the initial failure rate for the units. It appears the high voltage and the maximum load tests did not significantly contribute to failures.

25 AA units were received and of these six developed failures. Five of them were initial failures and one was on the third unit test. There were five open resistors and one shorted diode in this group. Only two AA units were baked and neither of these failed so that no significant difference in failures developed between the baked units and the units that were not baked.

20 AB units were received and of these four suffered failures. Two had been selected to be baked in the first ten per cent and both of these developed failures. One was an open resistor and the other a faulty diode. The remaining two failures were both open resistors detected in the initial unit functional test.

The overall result for the AA units was that approximately 20 per cent were initial failures and with the AB units approximately 10 per cent were initial failures. It would be unwise to draw too many conclusions from the small number of units that represented in the 10 per cent

initial failures. All failures except the two noted diode failures were caused by open leads in the AND resistor or inverter collector resistor. It appears from this information and information supplied from MSFC that the leads to the resistors on the bottom of the substrate are opening up, perhaps at the S clip. No units have been opened up for detailed failure analysis by CAL.

3.3.2 Results of Unit Stress Test on the Sylvania Units

All the Sylvania units received were run through the test sequence together. The initial acceptance test showed that one SFF-12 and one SNG-14 were not properly soldered on to the test circuit board on which they were received. These connections were repaired and the units remained in the testing sequence. The initial unit functional test showed that one out of the twenty-three SFF-12 units tested was faulty. One-half of the unit, that associated with output L, was defective in that sweeping the inputs. A, B, and M did not produce a response at L. The initial unit function test also showed that one out of twenty SNG-14 units was defective. This unit appears to have an open in the Vcc connection inside the package since there was not any current drawn by the unit. The only other failure detected during the stress testing phase was one SNG-14 which would not operate under conditions of the maximum load-high temperature test. This unit does operate properly at room temperature but it was dropped from the test cycle. No problems were detected with the three SNG-4B units during the unit stress test.

3.3.3 Results of Unit Stress Test on the Fairchild Units

Two 931 units failed out of the thirteen tested. One unit does not operate under the conditions of the high-voltage test. With a Vcc of 8.0 volts, the outputs would not switch states. The second 931 failed to meet the minimum ONE logic voltage of 2.6 VDC during the dynamic unit functional test following the high voltage test. A possible explanation is that the leakage current was sufficient to keep the output transistor from switching off. All eleven 930, four 932 and three 933 units progressed through the unit test sequence without a failure.

4.0 APPLICATION TEST RESULTS

Each of the three logic lines evaluated was tested in each of the three applications. The general configuration of each application was kept logically as similar as possible, with the exceptions noted. The output portion of each counter or shift register stage was loaded to the maximum worst case fan-out as rated by the manufacturer, and the capacity to ground at each output was measured to be within 5% of 220 pf, including wiring capacity and simulated load. The standard ULD clock driver circuit, as used in the unit tests, was used to generate Cpx and Cpy. A SNG-4B and a 932 were used as clock drivers in the Sylvania and Fairchild circuits, respectively.

4.1 Shift Register Evaluation

The shift register application tested the characteristics of the flip flops rather than the gates in a logic line, and probably gives a better idea of the basic speed of the flip flop than either the synchronous or ripple counters. The general logical layout of the shift register application is shown in Figure 4.1. The input data is buffered and inverted and simply shifted down a chain of ten stages of the shift register. The external pulse pattern generator provided a pattern of "ONES" and "ZEROS" for testing of the register. The particular connections used for the ULD modules in constructing one stage of the shift register are shown in Figure 2.5. This interconnection is the same type used in the COD counter in the Launch Vehicle Data Adapter. However, the inputs to the register have been simplified to facilitate testing. The logical interconnections allow a maximum fan-out of three for this arrangement. Therefore, the simulated load circuits were adjusted so that the total fan-out of each stage of the shift register would be three. The connections of a typical stage such as the ninth stage are such that the load on one inverter would be a 1.5K resistor for cross-coupling and a 2.5K resistor input to the following shift register stage. This, according to the loading rules, amounts to a fan-out of 1 2/3. Therefore the simulated load at that point would be adjusted to look like 1 1/3 load to give a total fan-out of three. The outputs of all ten shift register stages were loaded heavily with 220 pf of capacitance to simulate the heavy capacitance loading encountered in the Launch Vehicle Data Adapter. Figure 4.2a gives a description of the noise immunity circuit

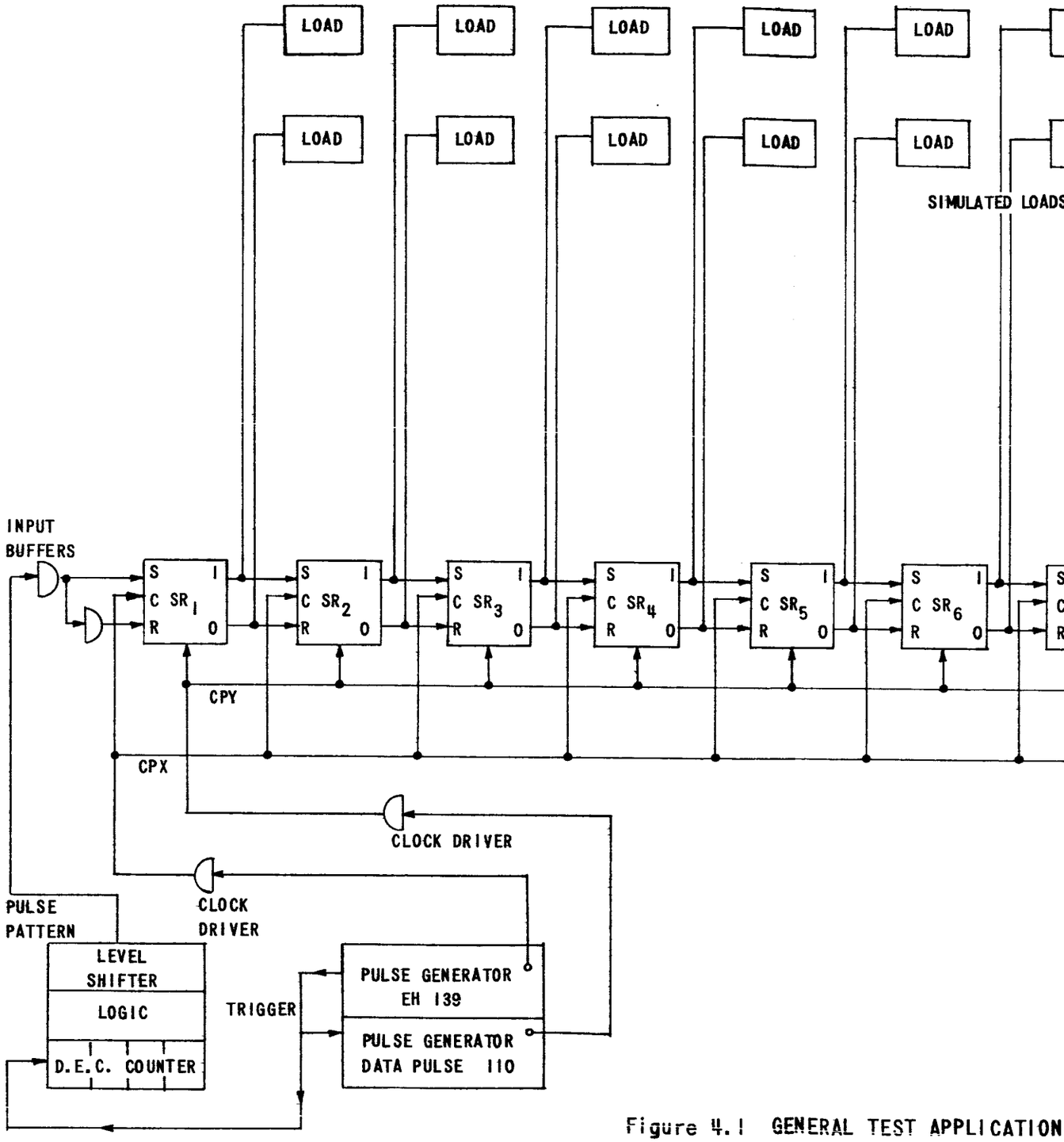
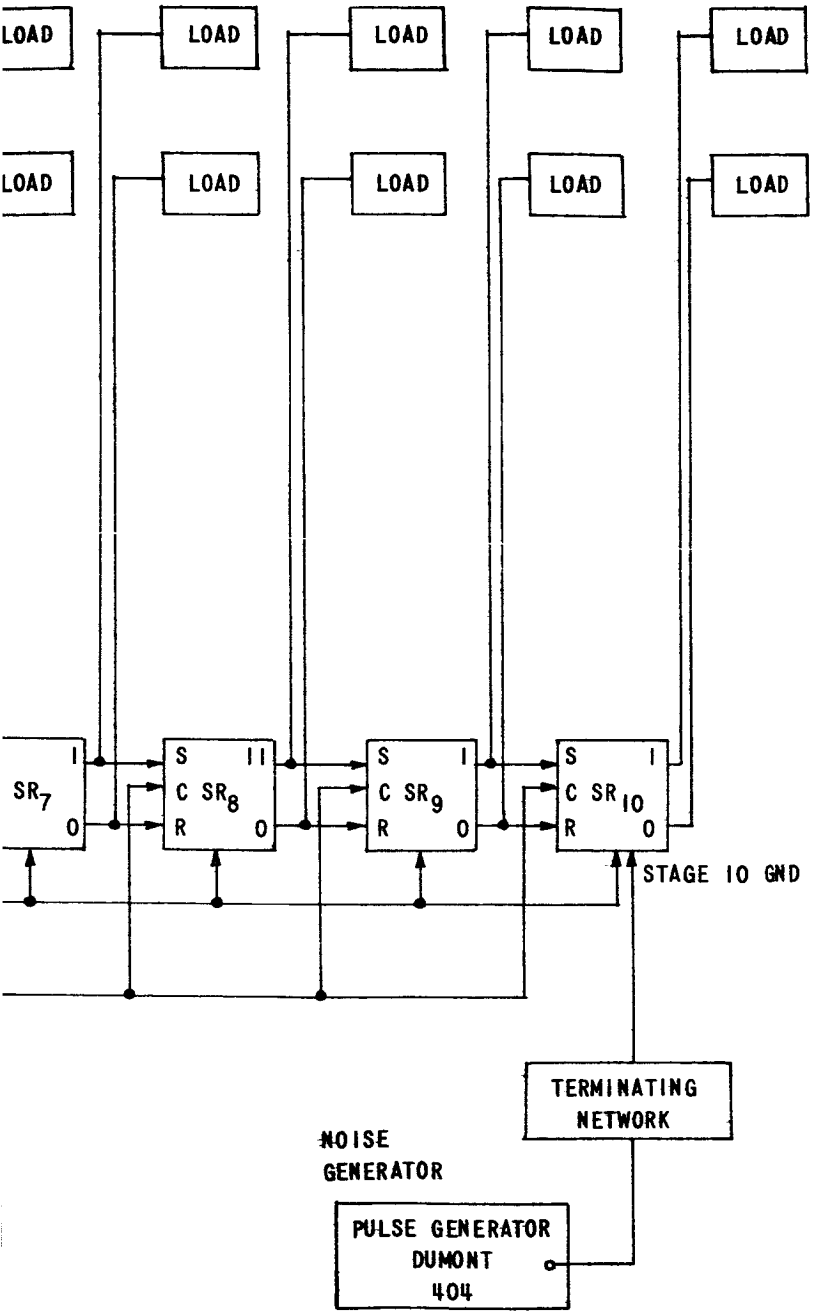
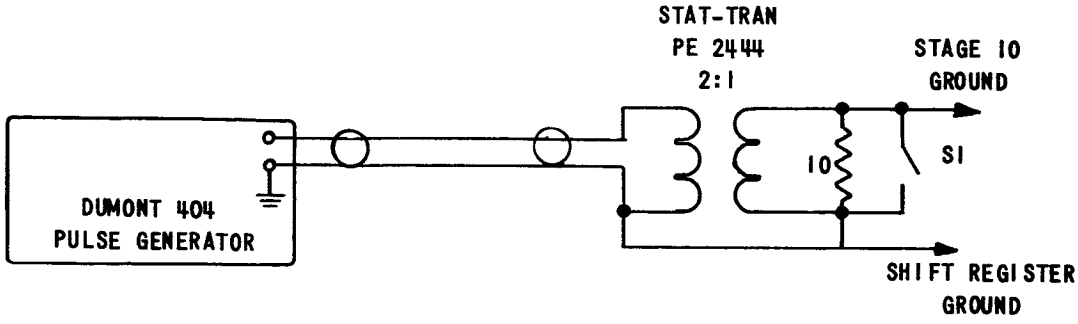


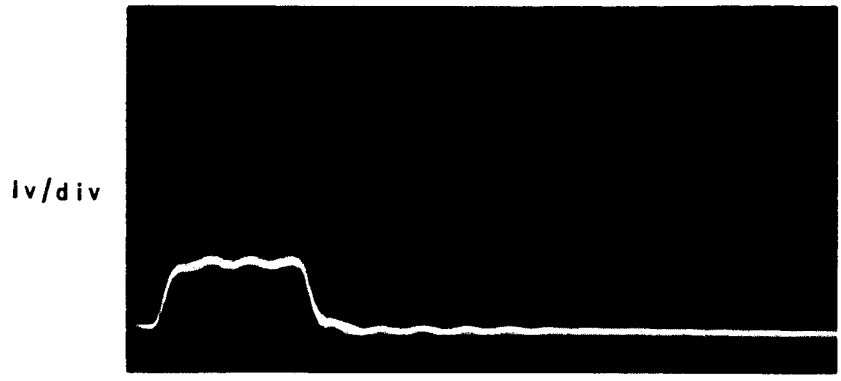
Figure 4.1 GENERAL TEST APPLICATION



, SHIFT REGISTER



a. NOISE TEST CIRCUIT USED FOR SHIFT REGISTER, SYNCHRONOUS AND RIPPLE COUNTER TESTS



100 ns/div

b. STANDARD NOISE PULSE

Figure 4.2 NOISE TEST CIRCUIT

used in testing the shift register and the counters. Here the ground on the total tenth stage of the shift register has not been connected in common with the ground of the other nine stages but rather has been tied through a pulse generator to the common ground. It is therefore possible to apply a positive or negative pulse on the ground to the tenth stage. The appearance of the standard positive pulse used to test for noise immunity is shown in Figure 4.2 b. Since noise introduced into a circuit may or may not cause trouble depending on the phasing of the noise, the polarity of the noise and the amplitude of the noise, it is necessary to run the noise generator in this test asynchronously. That is, it is not synchronized with the clock used in the system. The method of making the measurement is this: The output of the tenth stage, both sides, is examined on the 585 oscilloscope. The noise generator is turned on and the tenth stage ground switch opened so that the noise pulse will appear on the tenth stage ground. The output of the pulse generator is antenuated to give a very low amplitude pulse of either positive or negative polarity depending on the test being made. The output of the tenth stage is examined closely on the oscilloscope and the pulse generator output amplitude increased slowly until it is apparent that there is a mistriggering of the output of the tenth stage. In practice, discerning when the pattern begins to pick up the noise is much easier to see than might be expected. Noise levels as small as 1/2 db change can be detected easily. Measurement is then made of the maximum amount of noise pulse allowable without any noise pickup or mistriggering in the output of the tenth stage. This is done separately for a positive pulse and for a negative pulse. A positive pulse on the ground makes a ONE at the input of the tenth stage appear to be a ZERO when a noise level is too high. Conversely, a negative pulse on the ground of the tenth stage makes a ZERO on the input of the tenth stage appear to be a ONE. Since the positive and negative noise protection of the circuit is generally not the same it is also expected that the noise immunity of the tenth stage of the shift register would be different for positive and negative noise.

Figure 4.3 shows the output wave shape of the tenth stage of the ULD, Sylvania, and Fairchild shift registers. The ULD and Fairchild shift registers were operating at a frequency of about 3 mc, but the Sylvania was operating at

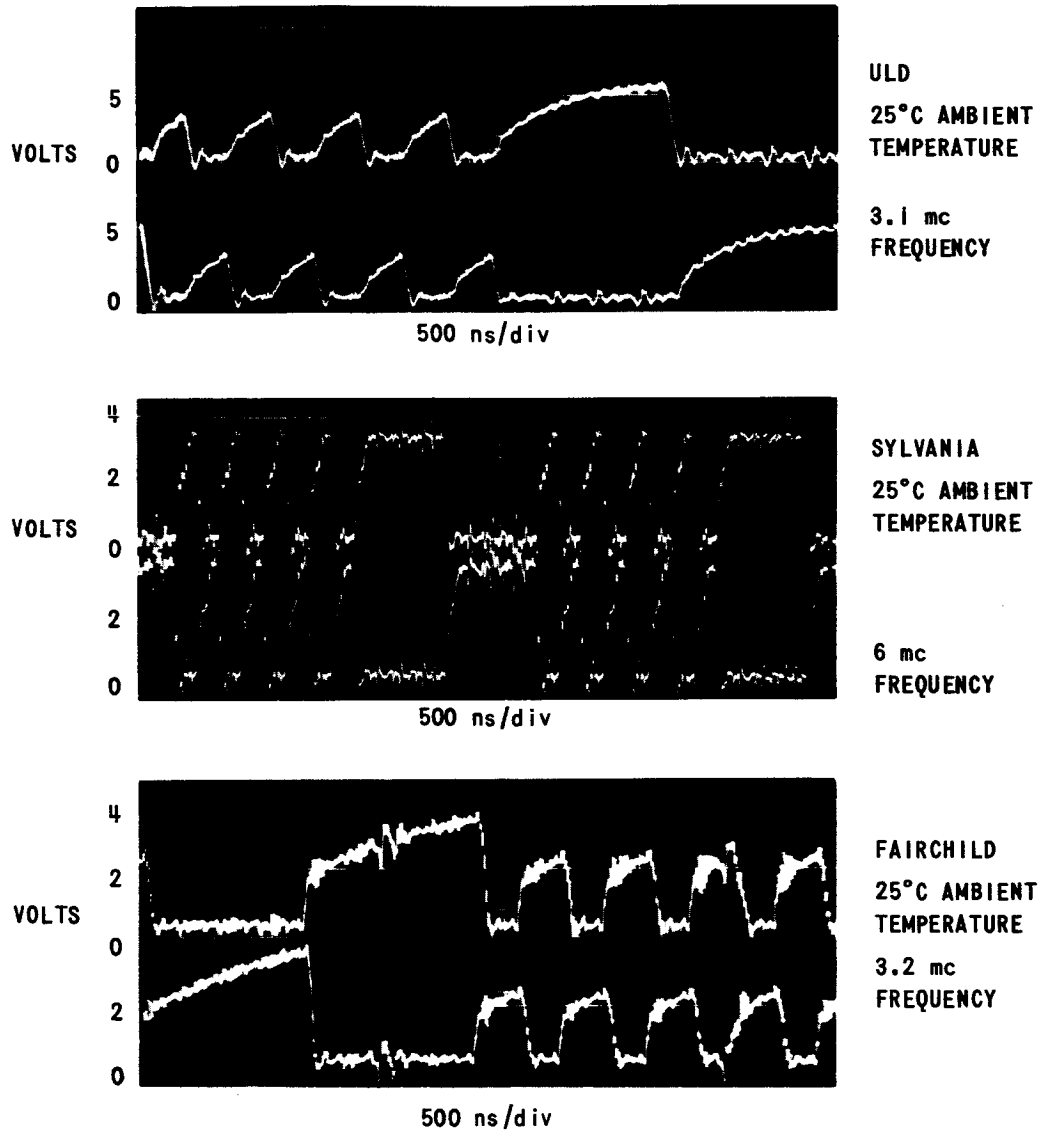


Figure 4.3 10th STAGE OUTPUT (BOTH SIDES) OF SHIFT REGISTER SHOWING WAVE SHAPES OF ULD, SYLVANIA AND FAIRCHILD FLIP FLOPS

6 mc. Standard data, such as minimum voltage and noise margins, were taken with operation at 3 mc in the shift register tests. On the rising edge of the wave shapes shown, the point that the load diodes became back biased can be seen as a break in the rising wave shape. Charging of the load capacity occurs faster before this break and slower after this break. On the Sylvania shift register the rising wave shape is much steeper because of the unique pull up transistor circuit employed.

Figure 4.4 shows curves of noise margin as a function of temperature for each logic line in the shift register test. Two curves are necessary, one for positive pulses and one for negative pulses. In practice, the lower of the two noise margin voltages would have to be the one considered in arriving at the safe margin allowable. Data for the Fairchild units at high temperature is not available due to a coaxial cable shorting in the temperature chamber during this test.

The DC power consumed in the three logic lines, at 3 MC shift rate, is shown as a function of temperature in Figure 4.5. This measured power does not include power supplied to the simulated loads. Power consumed changes no more than 12% over the temperature range.

Figure 4.6 shows curves of the minimum operating voltage as a function of temperature for each of the logic lines.

The maximum frequency of operation of the shift register is an indication of the speed of the flip-flop and hence the margin of safety, in a large system, of the timing. The frequencies shown in Figure 4.7 are maximums, above which faulty operation occurred, and are not the frequencies that could be safely used in a large digital system. The TTL circuits are three or more times faster than the DTL, while the Fairchild DTL is about 50% faster than the ULD. Determination of the maximum operating frequency, in a two phase system, can be affected by the relative periods and phasing of the two clock phases. An effort was made to standardize the clocks at 180° phase, each clock period 40% of the total period.

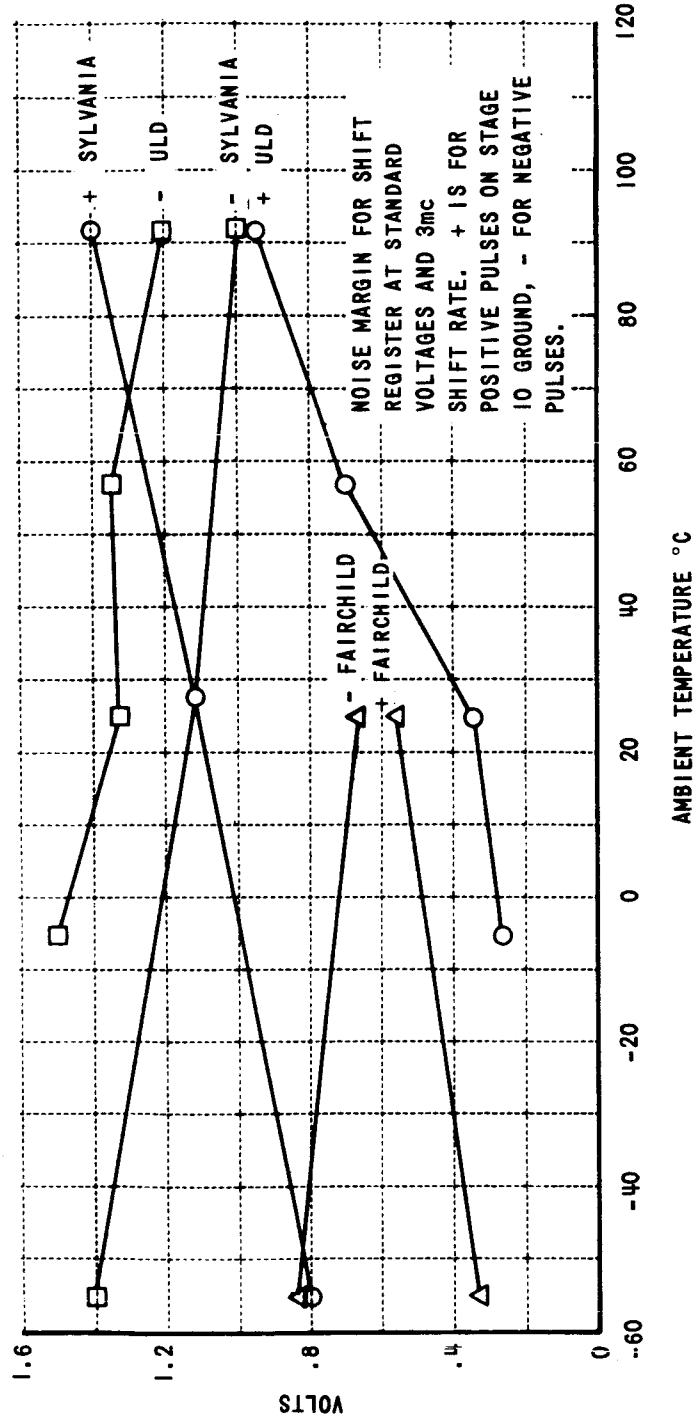

SYLVANIA + ULD -
SYLVANIA - ULD +
FAIRCHILD -
FAIRCHILD +
NOISE MARGIN FOR SHIFT REGISTER AT STANDARD VOLTAGES AND 3mc SHIFT RATE. + IS FOR POSITIVE PULSES ON STAGE 10 GROUND, - FOR NEGATIVE PULSES.
VOLTS
1.6
1.2
.8
.4
0
-60
-40
-20
0
20
40
60
80
100
120
AMBIENT TEMPERATURE °C

Figure 4.4

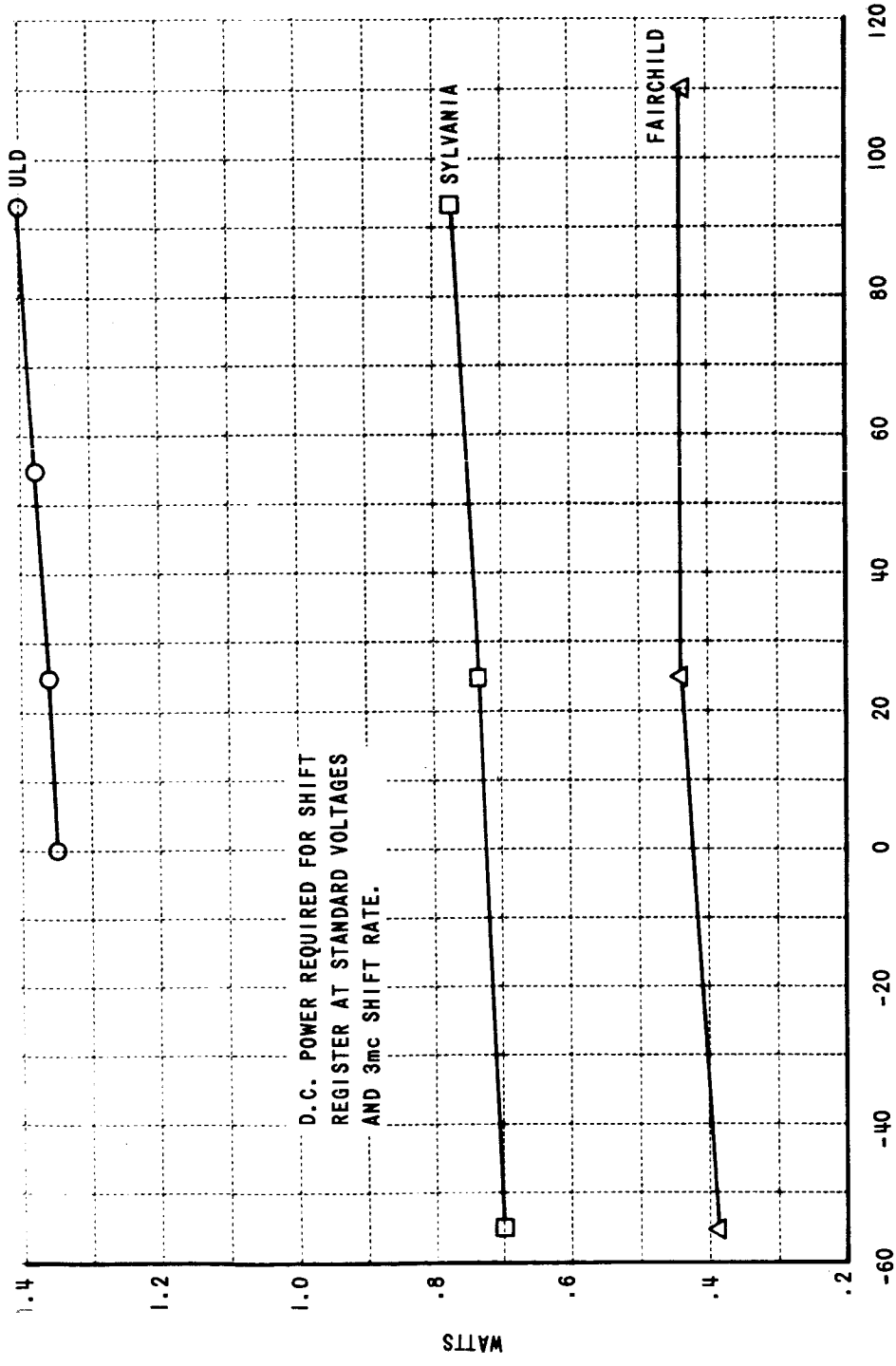

ULD
SYLVANIA
FAIRCHILD
D.C. POWER REQUIRED FOR SHIFT
REGISTER AT STANDARD VOLTAGES
AND 3mc SHIFT RATE.
WATTS
1.4
1.2
1.0
.8
.6
.4
.2
-60
-40
-20
0
20
40
60
80
100
120
AMBIENT TEMPERATURE °C

Figure 4.5

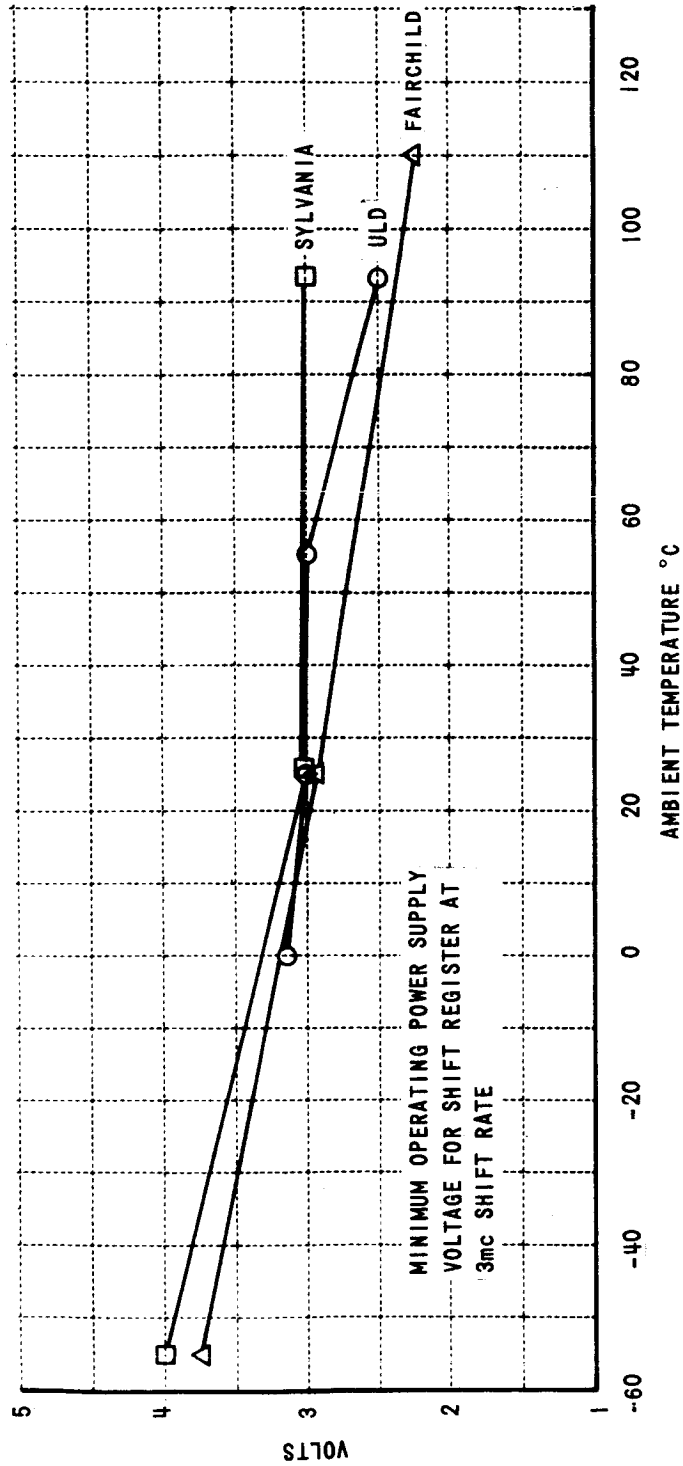

MINIMUM OPERATING POWER SUPPLY
VOLTAGE FOR SHIFT REGISTER AT
3mc SHIFT RATE
SYLVANIA
ULD
FAIRCHILD
VOLTS
AMBIENT TEMPERATURE °C
5
4
3
2
1
-60
-40
-20
0
20
40
60
80
100
120

Figure 4.6

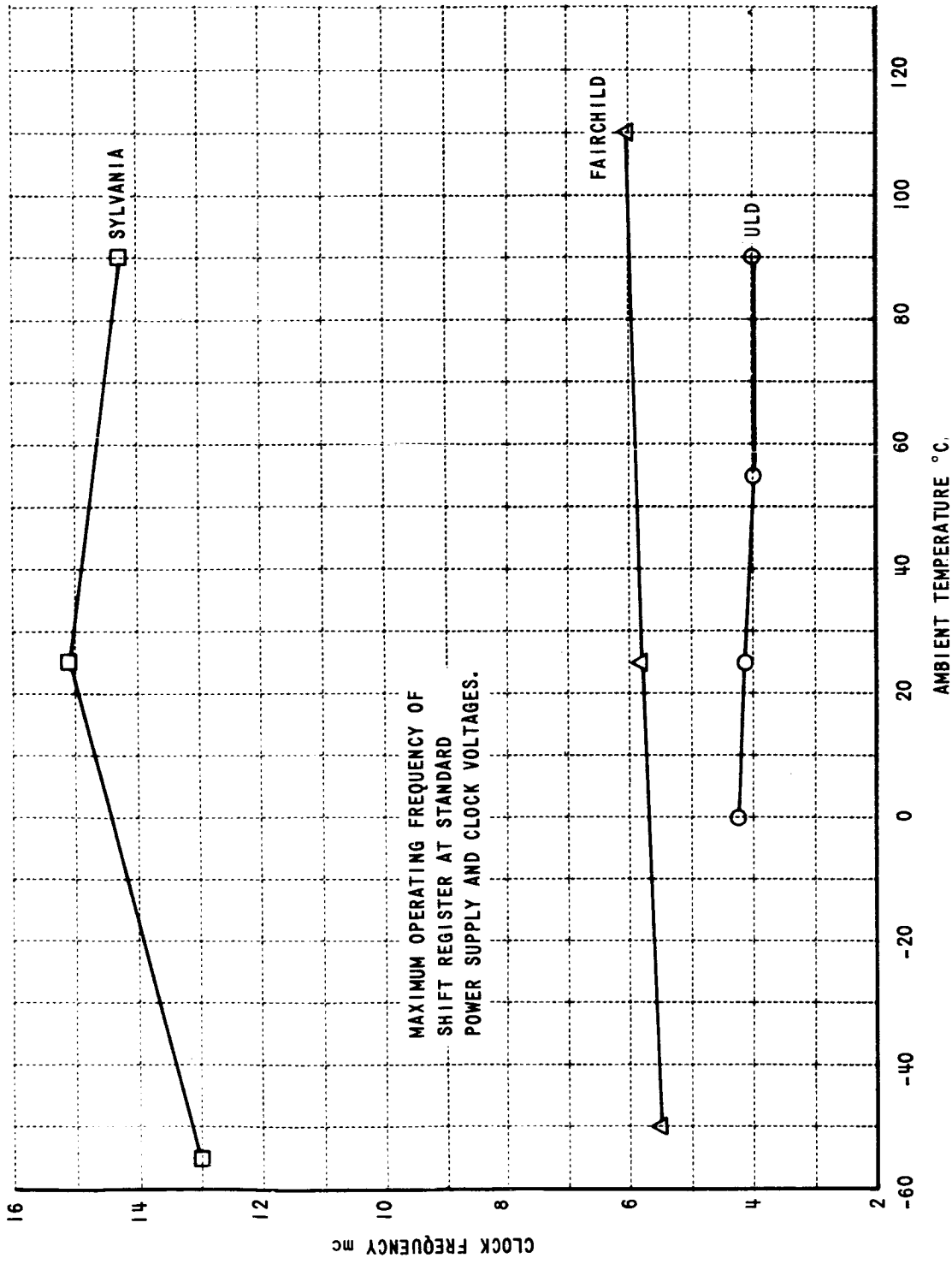

MAXIMUM OPERATING FREQUENCY OF
SHIFT REGISTER AT STANDARD
POWER SUPPLY AND CLOCK VOLTAGES.
SYLVANIA
FAIRCHILD
ULD
CLOCK FREQUENCY mc
AMBIENT TEMPERATURE °C.
16
14
12
10
8
6
4
2
-60
-40
-20
0
20
40
60
80
100
120

Figure 4.7

The Sylvania circuits show their relative greater speed in driving the high capacity loads over the DTL circuits. The output configuration of the TTL circuit, using a pull-up transistor rather than a pull-up resistor, as expected, had a greater speed driving the capacitive loads.

One effect has been noted which may be caused by low beta in the output stage of the Fairchild flip-flop. At low operating temperature, where the beta of the transistors is naturally reduced from the room-temperature beta, the outputs of stage six of the shift register had a high VCE_{SAT} of 1.4 volts. This effect was also noted on this stage during low voltage operation at room temperature and at the maximum temperatures. Of course, low operating voltage reduces the base current when the transistor is on and a low beta plus a low base current will result in the module having a very high VCE_{SAT}. The worst combination of these two effects is at low temperature and low operating voltage.

An additional effect of this high saturation voltage is that the positive noise immunity of the circuit is less under these conditions, since the difference between V_1 and V_3, as defined in Figure 3.2, is smaller.

4.2 Synchronous Counter Evaluation

The outstanding logical feature of the synchronous counter application is the long line of logic gates in cascade required to gate the flip-flops, as shown in Figure 4.8. The logic AND's the carry signal Xn with the preceding flip-flop ONE in order to gate the following counter stage. A series arrangement such as this was chosen in order to investigate the effect found with a long chain of logic gates. However, an alternate scheme, logically, is to AND the ONE output of the 1st and 2nd stages to gate the 3rd stage, and AND the ONE output of the 1st, 2nd, and 3rd stage to gate the 4th stage. The logical delay involved is then no more than one set of logic gates. The ONE output of the earlier stages is loaded heavily and the fan-in requirements of the gates becomes progressively larger. In practice, a synchronous counter would usually be constructed with a compromise of these two techniques in order to optimize fan in and loading and still prevent delays from becoming too large.

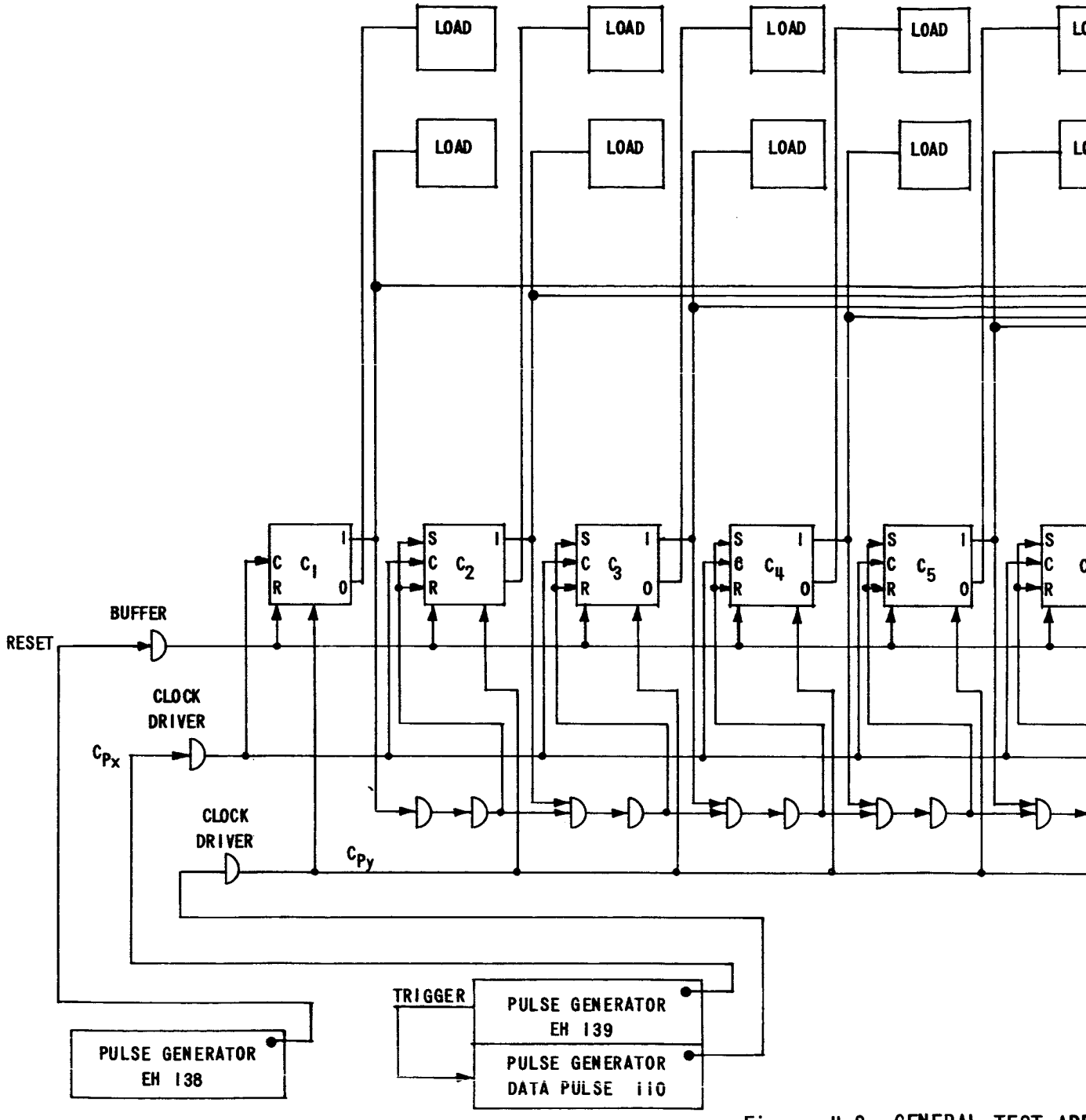
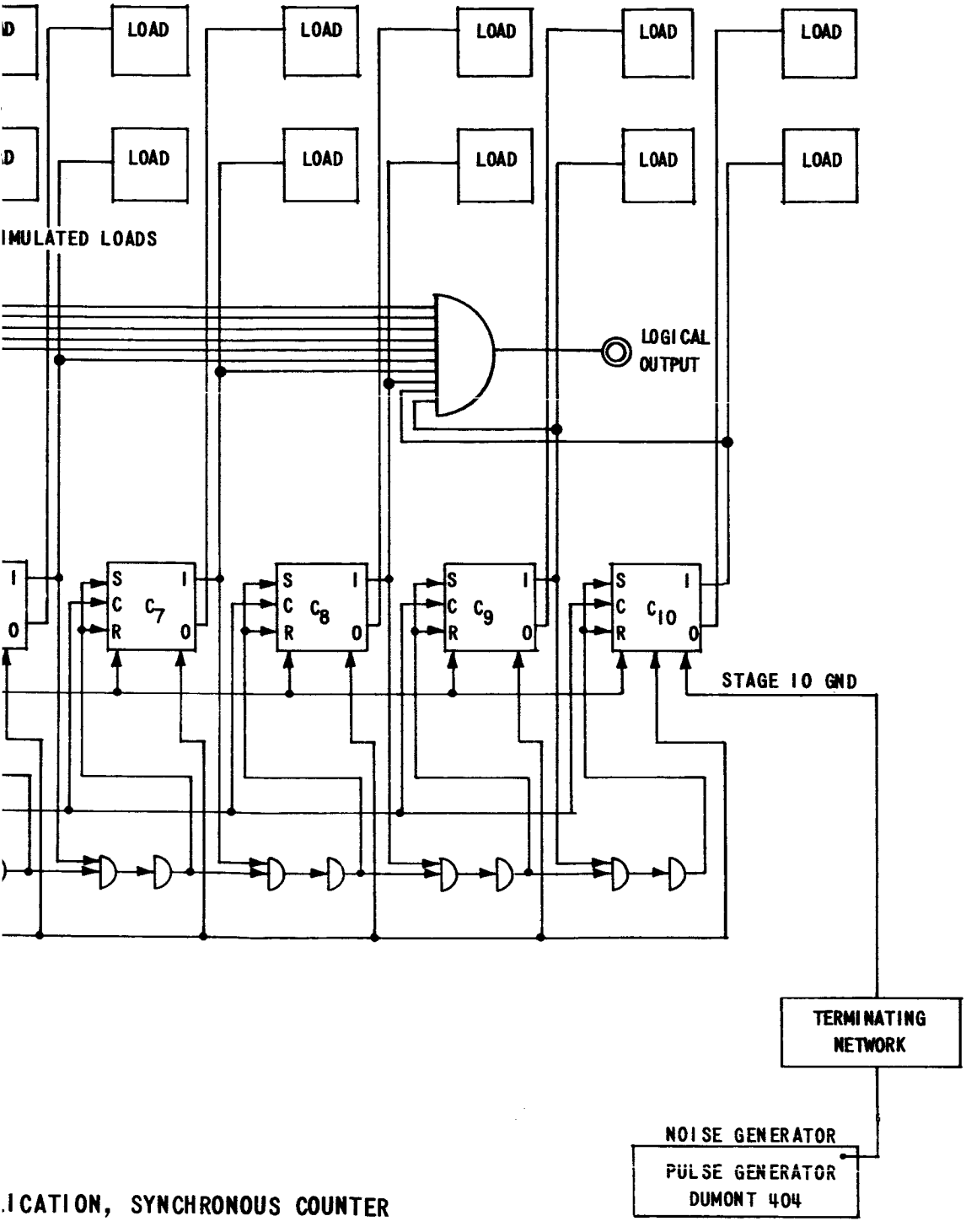


Figure 4.8 GENERAL TEST API



.ICATION, SYNCHRONOUS COUNTER

The tests for the synchronous counters were run at 1 mc, since this was the highest frequency at which the ULD counter would operate. Operation at 1.5 mc was tried at each temperature but could not be accomplished with the ULD counter. Generally, the limit of the upper frequency of operation occurred when the input logic signal to the 10th stage was delayed beyond the end of the clock pulse. The 10th stage would not count when required. Even with proper operation, the logic input to the 10th stage might occur after the start of the clock signal, as shown for the ULD counter in Figure 4.9. In this figure, note the additional 30 ns delay at 90°C of the X9 input to the 10th stage, over that at 0°C.

The curves of maximum counting frequency as a function of temperature for all three logic lines are shown in Figure 4.10. It should be noted, in the case of the Fairchild counter, that 1K pull-up resistors were added to the output of each gate which was an input to a counter stage, considerably increasing the maximum frequency at which the counter would operate. These pull-up resistors provide a current source to charge the wiring capacity at the gate output, thus speeding up the transition from logical ZERO to ONE.

In Figure 4.10 the high temperature value of the Sylvania operating frequency was not measured because of a failure in a clock driver SNG 4B after the units were at 113°C ambient for some time. The probable cause of this failure is discussed in the section on failures.

The curve of power as a function of temperature, Figure 4.11, indicates that the Fairchild and Sylvania units do not differ much in power consumption in this application. It should be remembered that the pull-up resistors add about 225 mw to the power consumption of the Fairchild units. The ULD's consume considerably more power.

The minimum voltage curve, Figure 4.12, is spread out more than in the shift register case. It indicates that the Fairchild and Sylvania units could operate at a voltage of 4 volts, but the ULD units would need 4.5 volts.

During the noise test performed on the synchronous counter, it was noticed with the Sylvania units that several noise figures could be arrived at, depending on what type failure was looked for. Failure of the counter to count

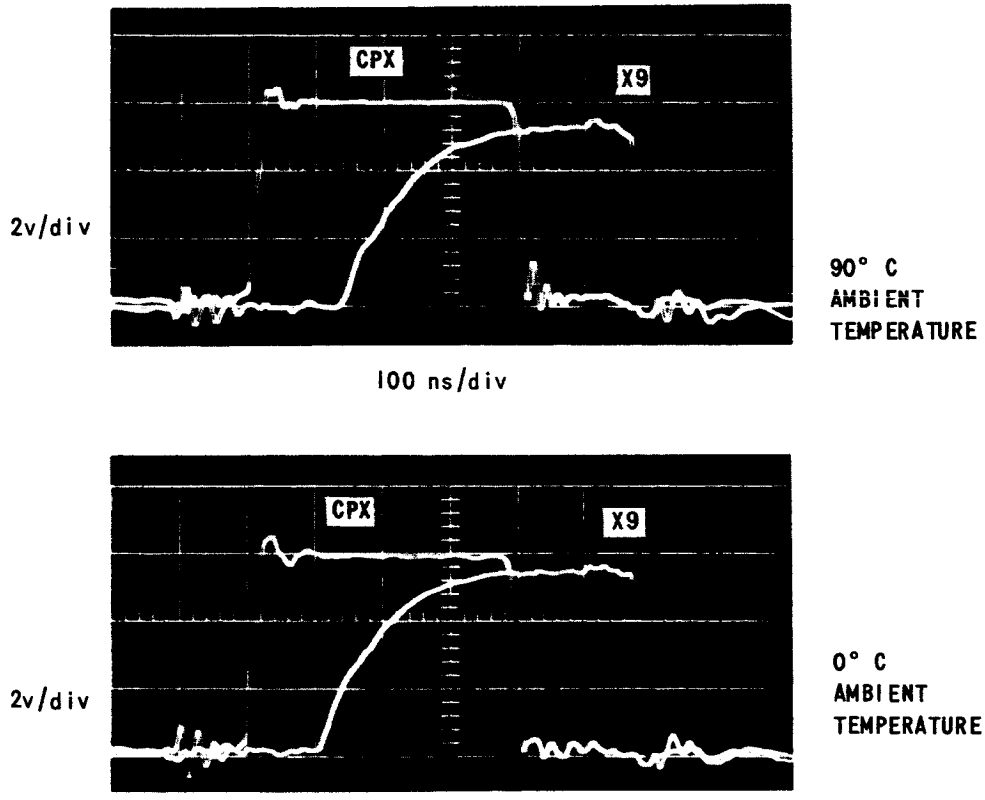


Figure 4.9 INPUT TO 10th STAGE (X9) OF THE ULD SYNCHRONOUS COUNTER AND C_{PX}. C_{PX} OCCURS FIRST. NOTE INCREASED DELAY AT 90° C OVER DELAY AT 0°

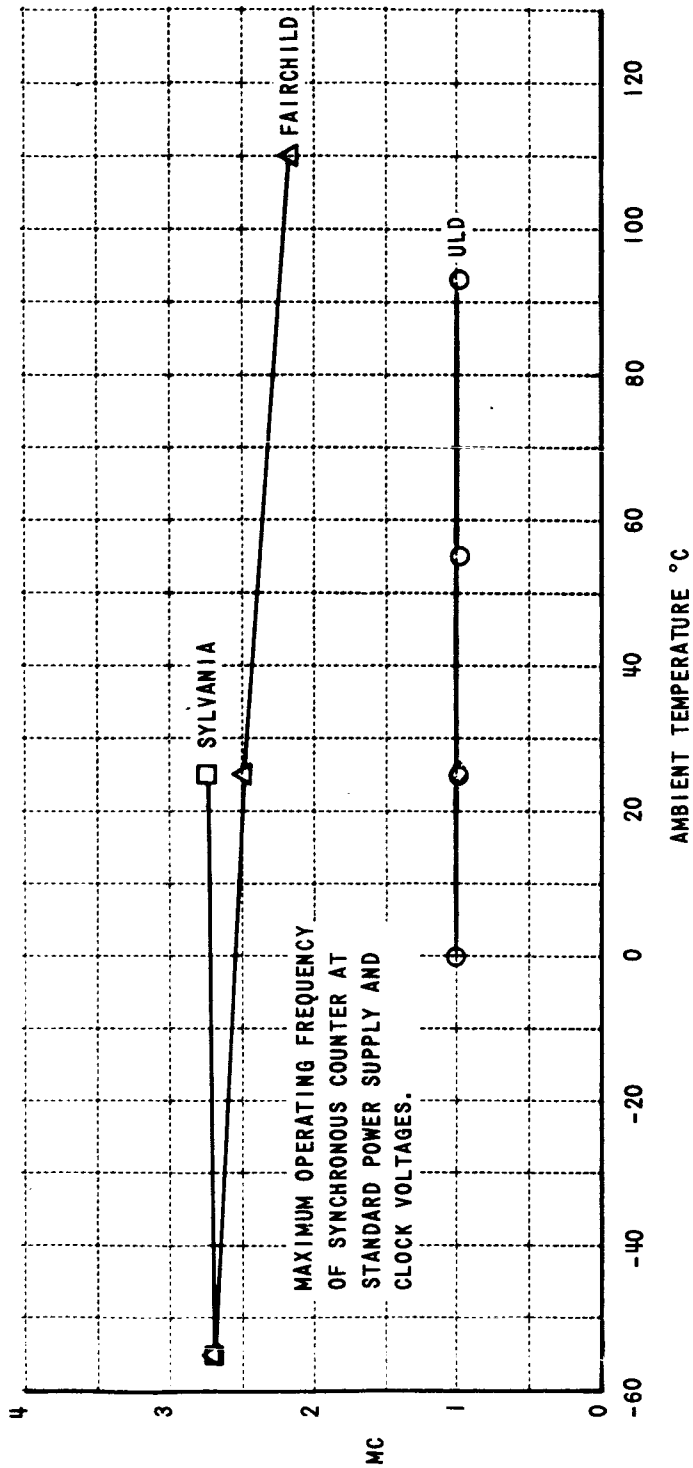

FAIRCHILD
SYLVANIA
ULD
MAXIMUM OPERATING FREQUENCY
OF SYNCHRONOUS COUNTER AT
STANDARD POWER SUPPLY AND
CLOCK VOLTAGES.
MC
4
3
2
1
0
-60
-40
-20
0
20
40
60
80
100
120
AMBIENT TEMPERATURE °C

Figure 4.10

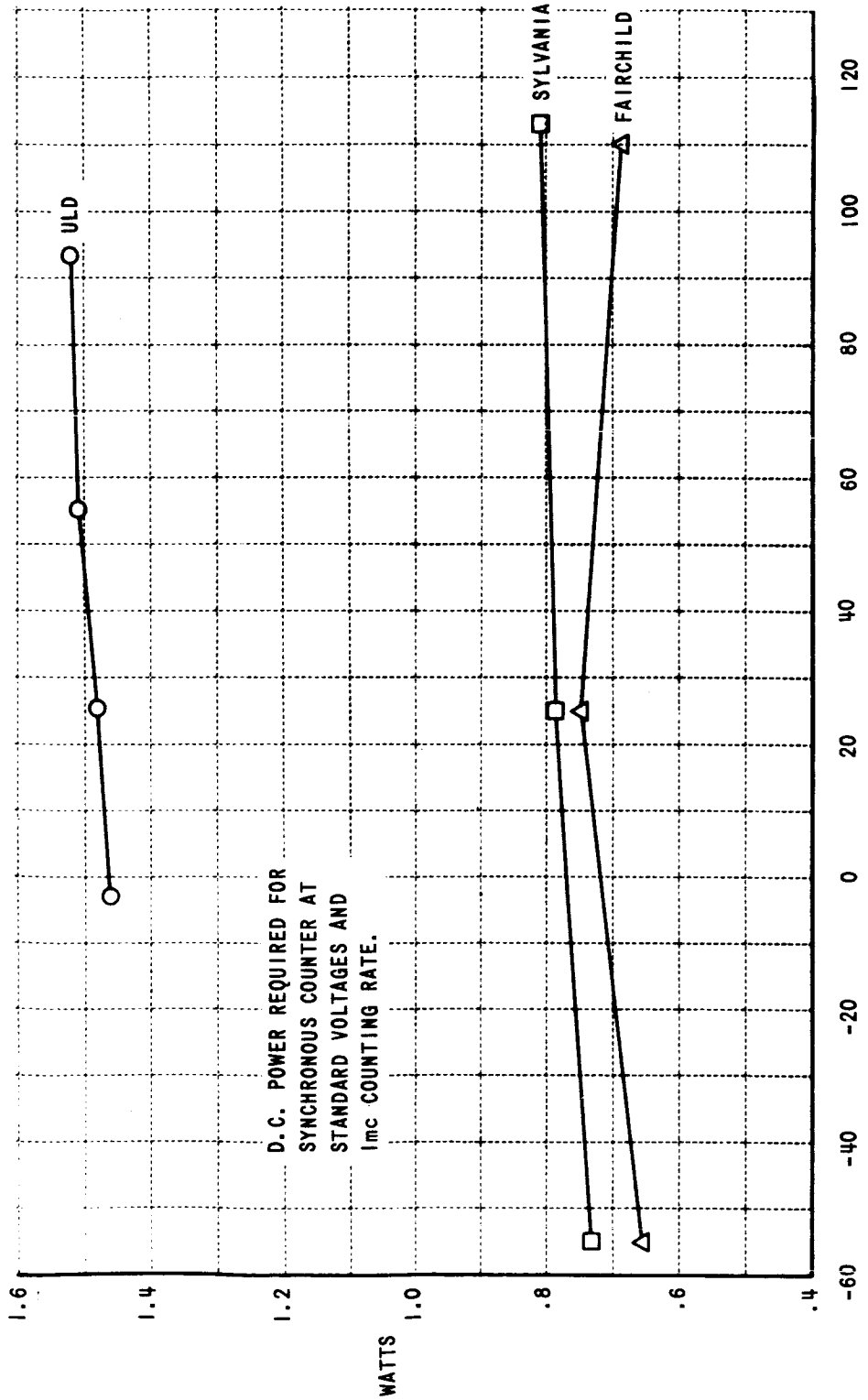

ULD
SYLVANIA
FAIRCHILD
D.C. POWER REQUIRED FOR
SYNCHRONOUS COUNTER AT
STANDARD VOLTAGES AND
Imc COUNTING RATE.
WATTS
1.6
1.4
1.2
1.0
.8
.6
.4
-60
-40
-20
0
20
40
60
80
100
120
AMBIENT TEMPERATURE °C

Figure 4.11

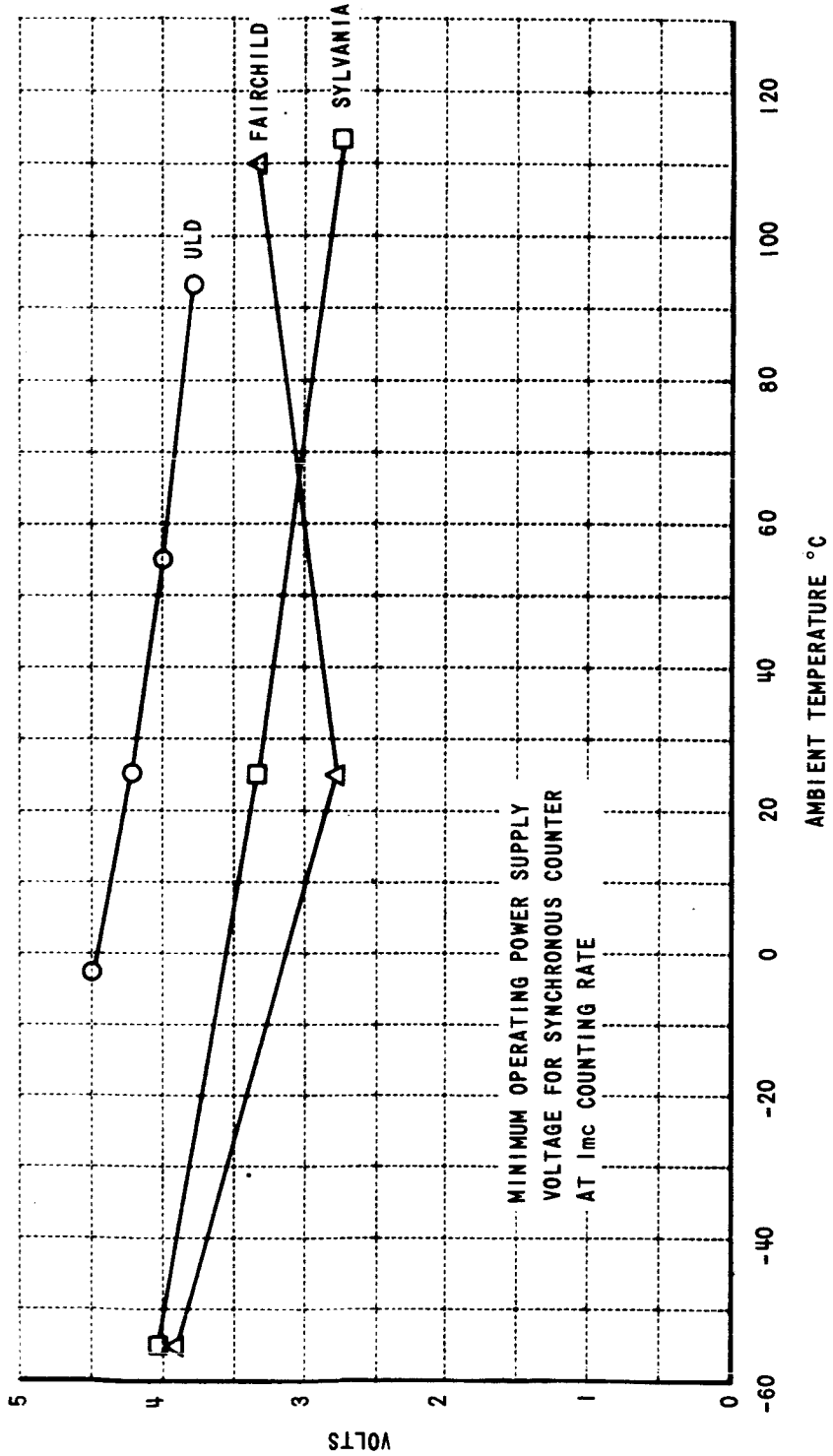

MINIMUM OPERATING POWER SUPPLY
VOLTAGE FOR SYNCHRONOUS COUNTER
AT Imc COUNTING RATE
ULD
FAIRCHILD
SYLVANIA
VOLTS
AMBIENT TEMPERATURE °C
5
4
3
2
1
0
-60
-40
-20
0
20
40
60
80
100
120

Figure 4.12

properly occurred at the noise level plotted in Figure 4.13, but false triggers out of the logic output occurred at a somewhat lower level of noise. At first, it appears that to have a false trigger out of the logic output, stage 10 must be miscounting, but review of the method of applying the noise to stage 10 ground reveals otherwise. The noise pulse raises (or lowers, with negative noise pulses) stage 10 ground above system ground. This will eventually cause the inputs to stage 10 to be interpreted incorrectly and miscounting will occur. However, this same process will cause the output of stage 10 to the logic gate to be interpreted incorrectly and the logic gate will be falsely switched, even though stage 10 has not actually miscounted. In interpreting the noise data, only the noise levels which caused miscounting were used, since this gives consistency with the noise tests for the shift register and ripple counters. Also, it allows measurement of noise at the input to a loaded flip-flop rather than at an unloaded gate, and results in a more meaningful noise figure.

The curves of noise margin shown in Figure 4.13 show that Sylvania circuits can accept the largest noise, 1 volt in the worst case at 113°C ambient. The Sylvania + curve is partly above the scale of the figure. It would generally be expected that noise margins for the tenth stage of this counter would be higher than for the first stage, since the stage is operated at a much lower frequency.

The reason the ULD + curve is so low in value, and in the middle of the - curves, is due to the frequency of operation. The positive noise pulse on the ground of stage 10 is equivalent in polarity to a negative noise pulse on the signal input to stage 10. A negative noise pulse on the output of stage 9 would have to be large to make the 6 volt level of a ONE be interpreted by the 10 stage as a ZERO. The data on Table 3.1 of Section 3.3 indicates a N- noise margin of 4.4 volts for the ULD. However, since the output of Stage 9 rises very slowly to 6 volts, the effective noise margin is much lower than 4.4 volts. If the next clock pulse occurs when the output of Stage 9 has risen to only 3 volts, the actual noise margin will be 3 volts less than predicted in the D.C. case. Since the ULD synchronous counter is operating close to its upper frequency limit when the noise measurements were taken, the noise margin

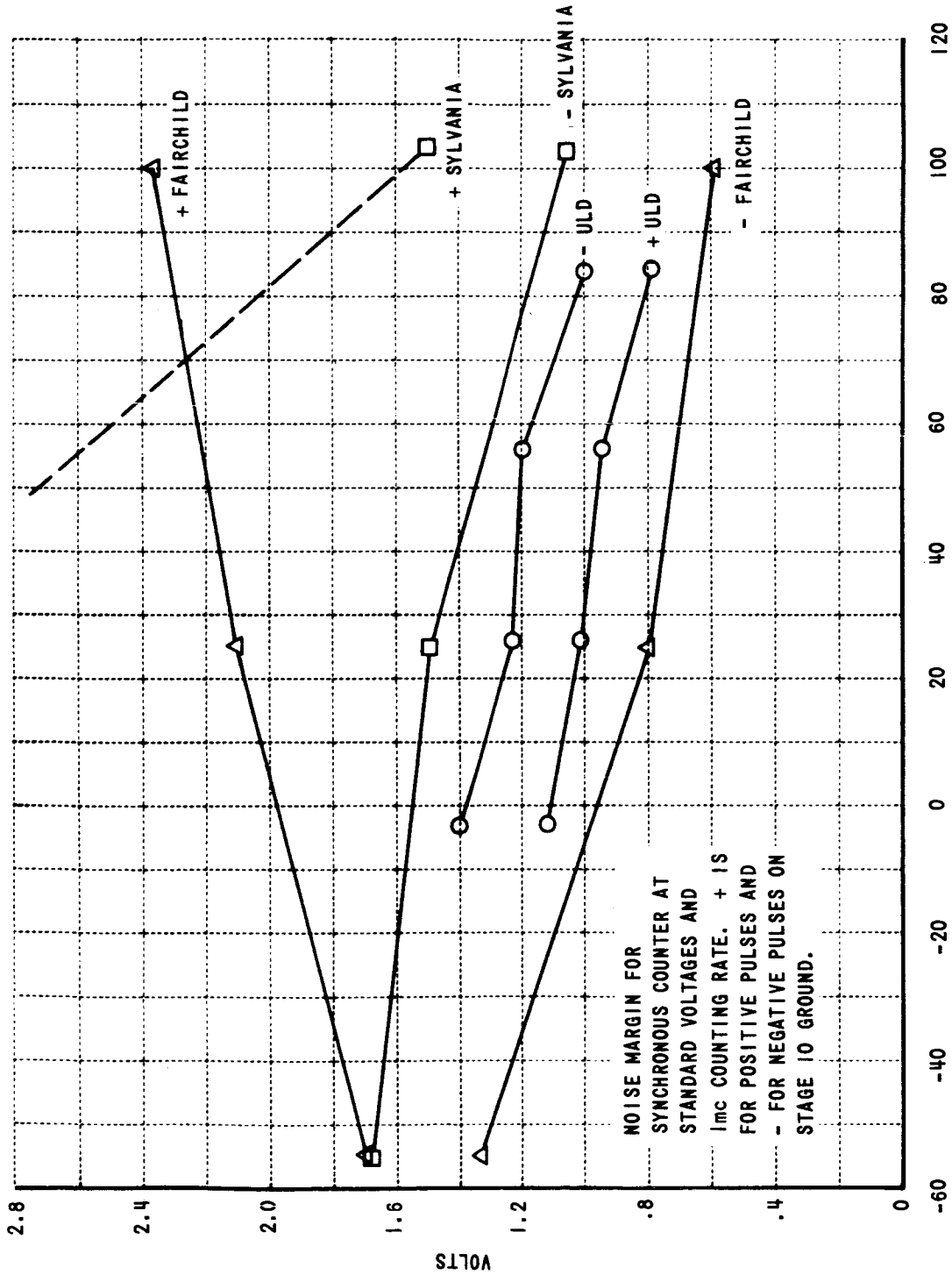

+ FAIRCHILD
+ SYLVANIA
- SYLVANIA
- ULD
+ ULD
- FAIRCHILD
NOISE MARGIN FOR
SYNCHRONOUS COUNTER AT
STANDARD VOLTAGES AND
Imc COUNTING RATE. + IS
FOR POSITIVE PULSES AND
- FOR NEGATIVE PULSES ON
STAGE 10 GROUND.
VOLTS
2.8
2.4
2.0
1.6
1.2
.8
.4
0
-60
-40
-20
0
20
40
60
80
100
120
AMBIENT TEMPERATURE °C

Figure 4.13

for positive pulses is much lower than the Fairchild and Sylvania. This example illustrates how the frequency and loading on a flip flop affects its noise margin.

A plot of delay per gate, Figure 4.14, shows the average delay of one of the gates of the chain. This is computed from the delay of a chain of gates, each loaded with a fan out of only two and a small capacitance load (about 10-15pf). Thus, this is an average delay, positive going delays are larger, negative going delays smaller. If the maximum frequency of the counter is set by the gate delay, as supposed, then the gate delay will be inversely proportional to the maximum counter frequency. Comparison of maximum frequency and gate delay curves verifies this.

Operation of the reset of the ULD was straightforward, and timing of the reset with the clock pulse was not a problem. Reset of the Sylvania counter was not as straightforward. Referring to Figure 2.16, the cross coupling connection between sides of the flip flop is not brought out. The only inputs available for reset are ANDed with the clock. Thus, reset can only be accomplished when the clock is positive. Furthermore, timing of the reset pulse should be so that the pulse rise occurs before the Cpx clock rises. If the clock occurs first, that clock pulse may be counted and reset of counter stages may not occur until the following Cpy clock pulse.

Reset logic of the Fairchild synchronous counter was instrumented but with the knowledge that it should not work. In the test application the reset would force the counter output to ZERO during the reset pulse but when the reset pulse was removed, the output of each counter stage would revert to a ONE if it had been a ONE before the reset occurred. This is the expected operation of the flip flop and points out a logical weakness when used in this type of application. Operation is independent of the sequence of reset and clock pulses. No workable logical arrangement could be arrived at to provide for a synchronous counter with a reset without incurring unreasonable complexity and timing delays.

The logical output of the synchronous counter was a large AND gate which required that all counter stages be at a ONE for an output. This configuration required that a ONE propagate down the carry chain and turn ON the tenth stage accurately, or the logical output would not occur.

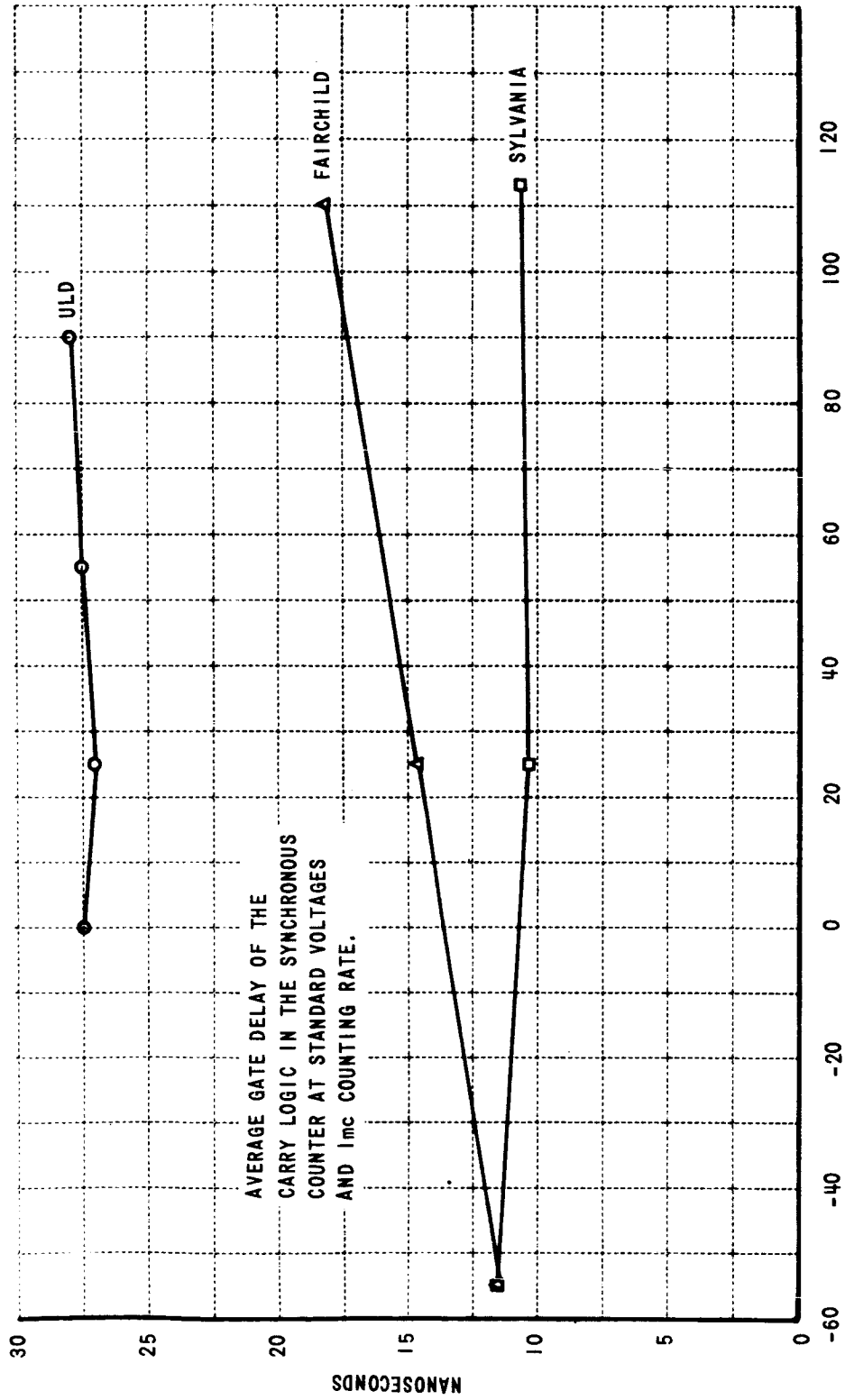

AVERAGE GATE DELAY OF THE
CARRY LOGIC IN THE SYNCHRONOUS
COUNTER AT STANDARD VOLTAGES
AND Imc COUNTING RATE.
ULD
FAIRCHILD
SYLVANIA
NANOSECONDS
30
25
20
15
10
5
0
-60
-40
-20
0
20
40
60
80
100
120
AMBIENT TEMPERATURE °C

Figure 4.14

This logical output occurred accurately in the ULD and Sylvania counter, but there were false spikes on the logical output of the Fairchild counter.

One characteristic of the Fairchild flip flop is that both sides of the flip flop may be ON during the instant of switching states, whereas the ULD and Sylvania flip flops are both OFF during an instant of switching. During the switching transient, the logical AND gate may have all ONES as inputs and momentarily switch, producing a voltage spike at the output when there should be none. These spikes occur at such a time that, with a synchronous or clocked logical output, they would not be readout, but with an asynchronous readout the spikes could cause errors.

Design of the logical output for the synchronous and ripple counters required a ten input AND gate. This was easily connected in the ULD units and, with the aid of a 933 package, there was no problem with the Fairchild units. However, Sylvania units required many more inverters because expansion of the Sylvania inputs is inconvenient. Expansion of the AND input to the Sylvania SNG-14 gate would require that the base and collector connections be brought out, and additional multi-emitter transistors be connected in parallel with the input transistor. Sylvania packages are available to accomplish this task but were not available for evaluation.

4.3 Ripple Counter Evaluation

The ripple counter application tests produced additional information on the capabilities of flip flops to gate other flip flops. The general configuration is shown in Figure 4.15. The standard tests were run at 1 mc to determine delays, power consumption, minimum power supply voltage, and noise margins. Then the counter was operated at its maximum frequency, which was generally determined by the maximum speed the first stage could be driven. The first stage inputs and outputs for maximum frequency operation are shown in Figure 4.16.

A logical output was produced by a ten input AND gate which was ON (zero volts out) when all flip flops were ZERO. Since the case where the counter

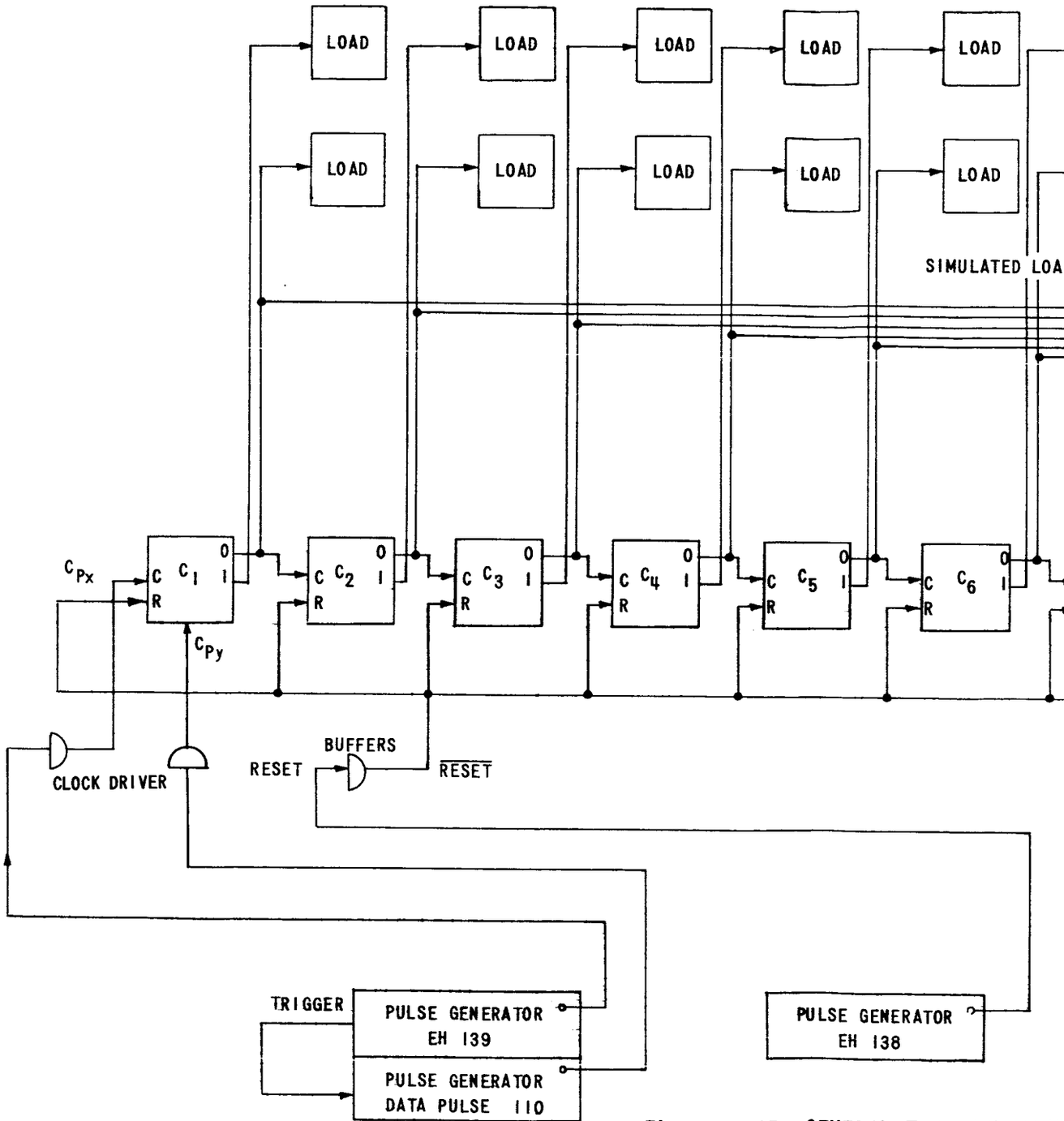
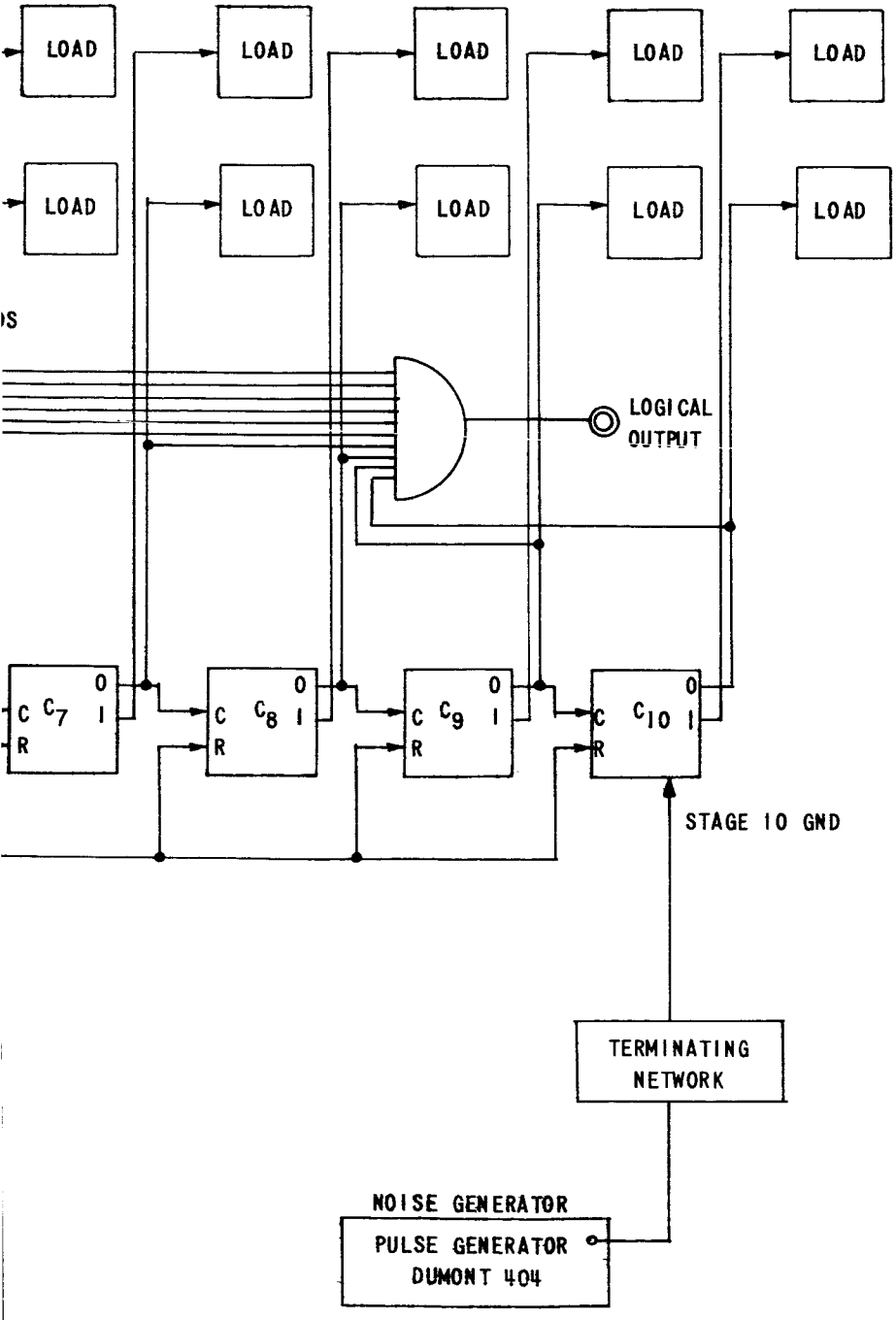


Figure 4.15 GENERAL TEST APPLICAT



ION, RIPPLE COUNTER

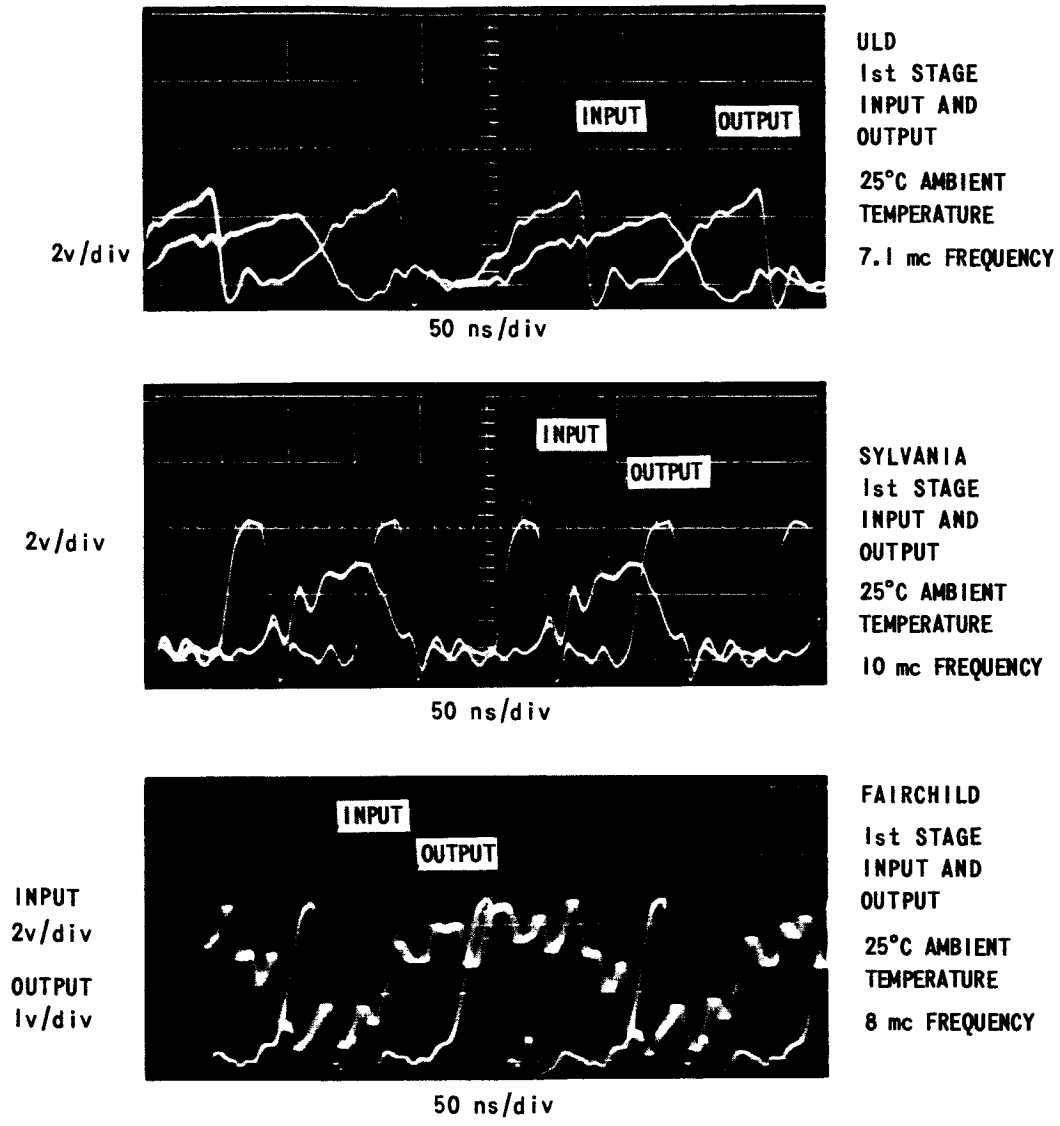


Figure 4.16 INPUT AND OUTPUT WAVEFORMS OF RIPPLE COUNTER FIRST STAGE AT MAXIMUM FREQUENCY WITH STANDARD VOLTAGES

changes from all ONES to all ZEROS produces the most delay in a ripple counter, and the carry must propagate down all ten stages, this is the logical output that is most difficult to obtain.

As might be expected in an asynchronous counter, the logical output gate had noise or false outputs on it following the true output. These are caused when, as a carry propagates down the counter, one stage has flipped to a ZERO before the following stage output becomes a ONE. Figure 4.17 shows the logic output of the three counters, illustrating the true (first) and false outputs. The noise spike length is determined by the delay in one counter stage, and there are nine such false outputs in a ten stage counter. It should be noted that the true logical output in the ULD counter was a spike which did not reach zero volts. For a logical output that was 400 ns wide, the maximum frequency that the ULD counter could be operated was generally around 700 kc.

The reset of the ULD counter worked satisfactorily as expected and produced no critical timing problems. However, the end of the reset pulse should occur between the pulses being counted in order to avoid any doubt that the first pulse will be counted properly.

Curves of minimum operating voltage and power consumed as a function of temperature (Figures 4.18 and 4.19) are in general agreement with previous data. The higher power of the ULD counter is due to the increased number of AND gate resistors to be driven when no clock pulse power is supplied. The curves of maximum operating frequency vs temperature, Figure 4.20, indicates the operating limits of the ripple counters, but generally the logical output was not generated properly below this frequency. The -55° frequency of the Fairchild counter is considerably lower than the 25°C and 110°C frequencies. Failure in this case was due to the second stage's failing to operate rather than the first stage, and indicates that the second stage may have had a low beta (but not below specifications) in one or more of the output transistors.

The noise curves for the ripple counter, Figure 4.21, are spread out even more than the synchronous counter noise curves. Failure due to noise occurred at that voltage which caused the counter to miscount, but logical outputs were generally faulty at lower noise voltages. The curves for negative noise pulses

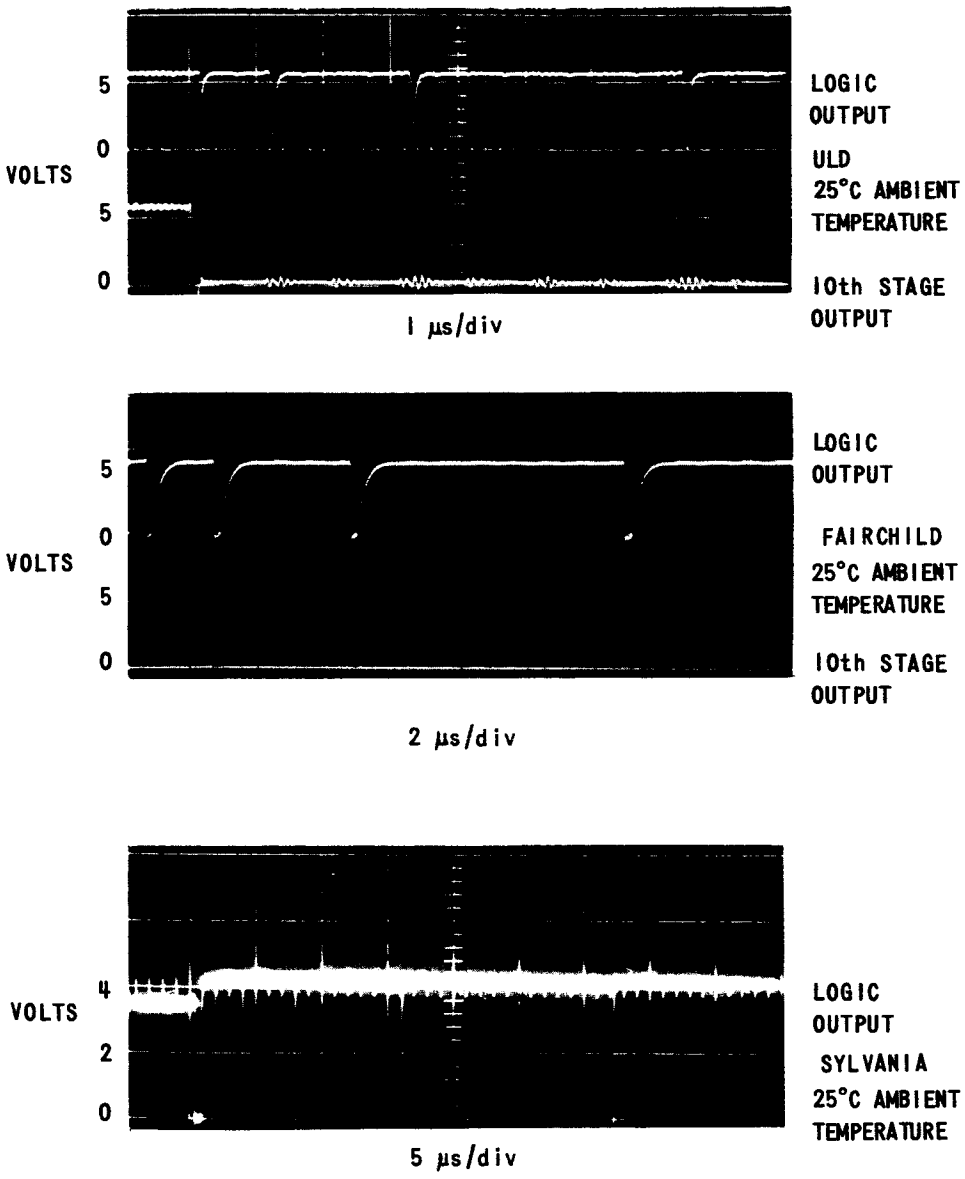


Figure 4.17 LOGIC OUTPUT OF THE RIPPLE COUNTER ILLUSTRATING TRUE (1st) AND FALSE OUTPUTS CAUSED BY RIPPLE DELAY CARRYING TIME. STANDARD VOLTAGE AND 1 mc FREQUENCY

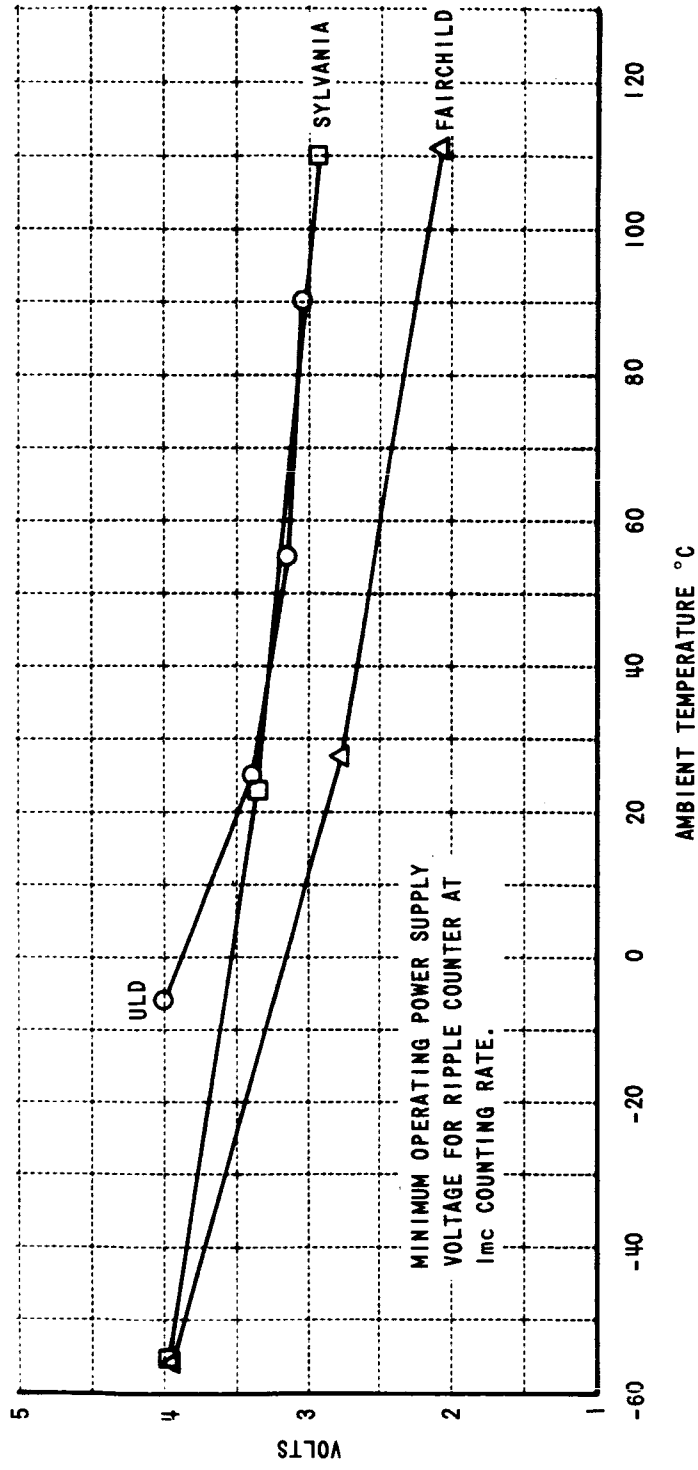

MINIMUM OPERATING POWER SUPPLY
VOLTAGE FOR RIPPLE COUNTER AT
Imc COUNTING RATE.
ULD
SYLVANIA
FAIRCHILD
VOLTS
5
4
3
2
1
-60
-40
-20
0
20
40
60
80
100
120
AMBIENT TEMPERATURE °C

Figure 4.18

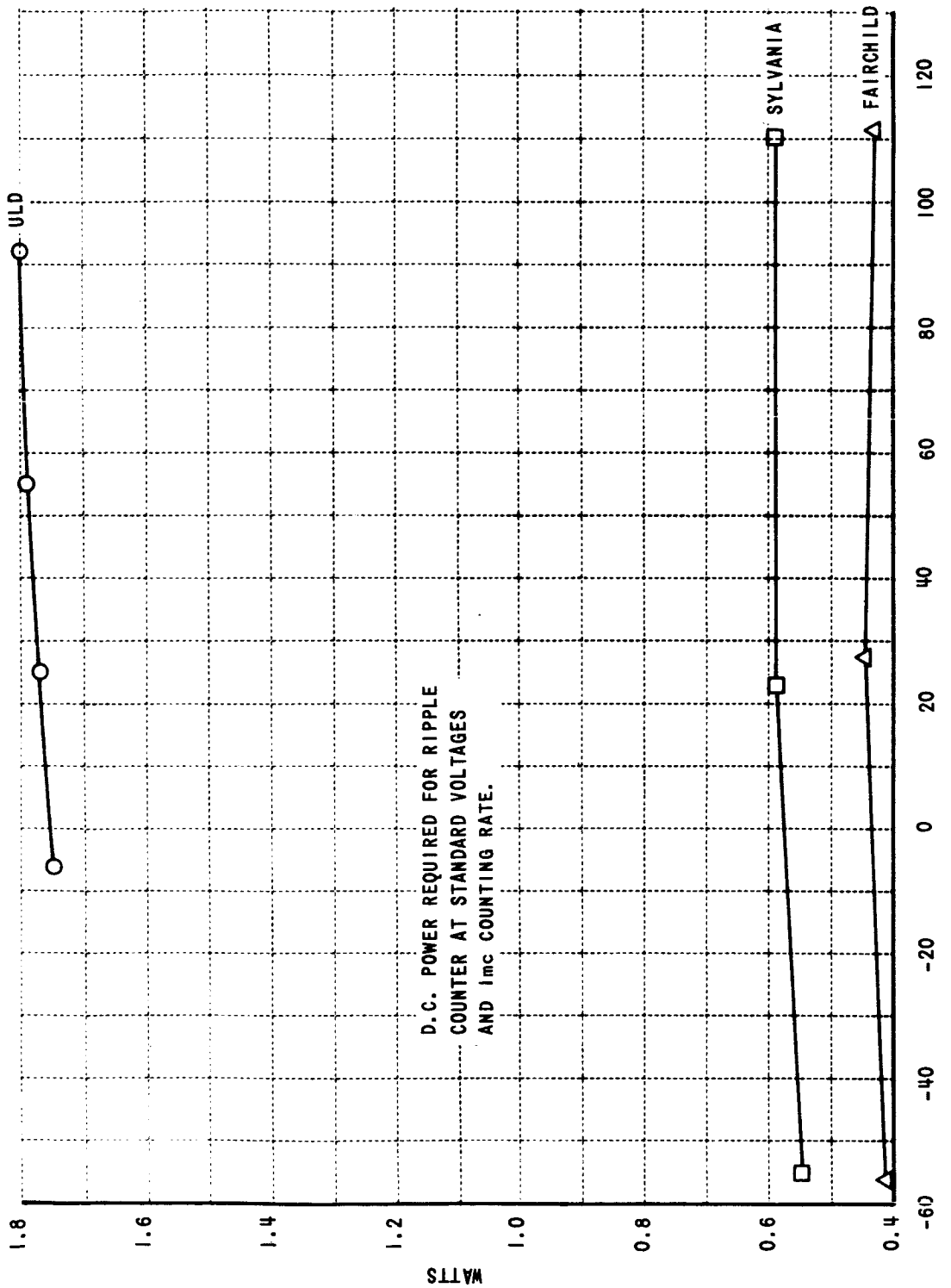

ULD
SYLVANIA
FAIRCHILD
D.C. POWER REQUIRED FOR RIPPLE
COUNTER AT STANDARD VOLTAGES
AND Imc COUNTING RATE.
WATTS
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
-60
-40
-20
0
20
40
60
80
100
120
AMBIENT TEMPERATURE °C

Figure 4.19

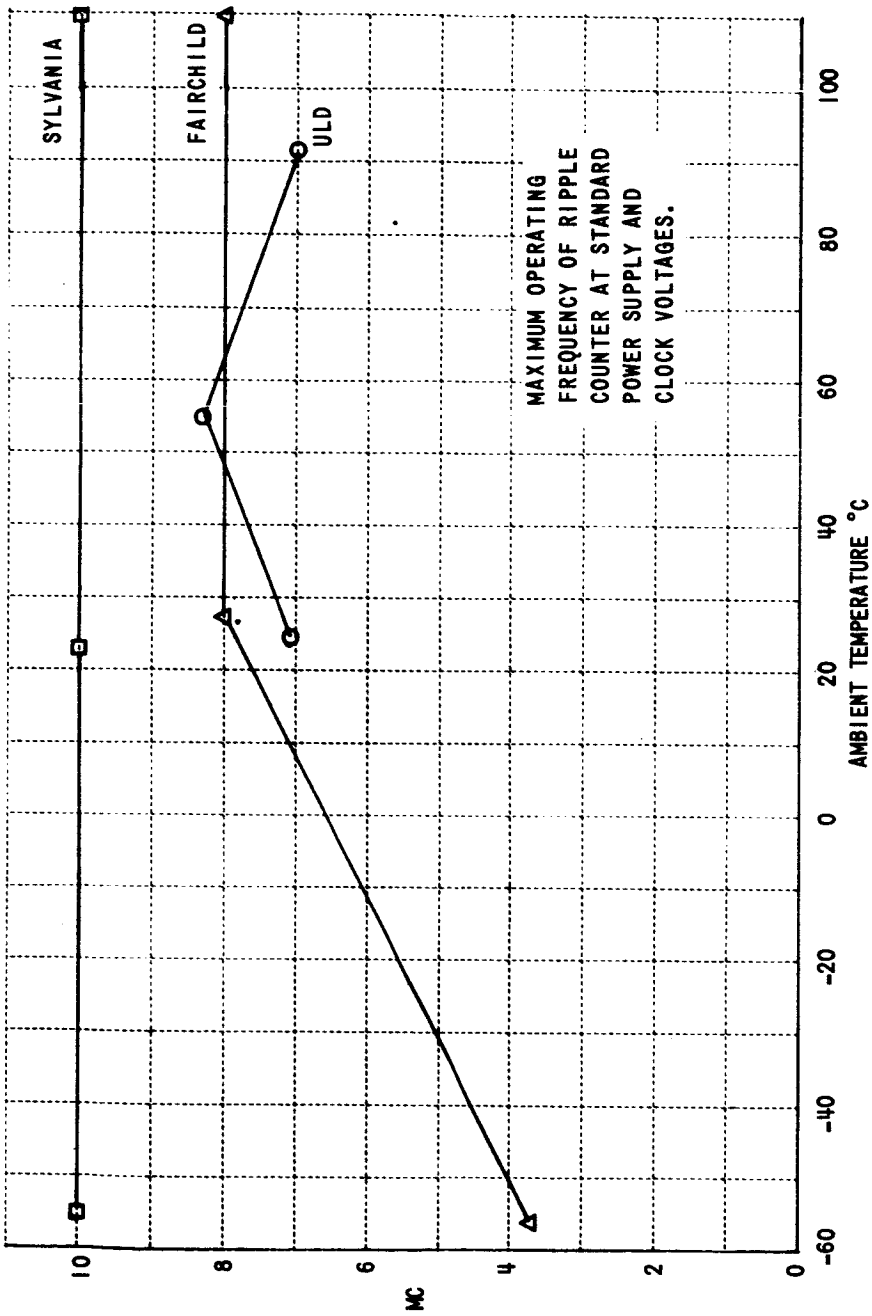

SYLVANIA
FAIRCHILD
ULD
MAXIMUM OPERATING
FREQUENCY OF RIPPLE
COUNTER AT STANDARD
POWER SUPPLY AND
CLOCK VOLTAGES.
MC
10
8
6
4
2
0
-60
-40
-20
0
20
40
60
80
100
AMBIENT TEMPERATURE °C

Figure 4.20

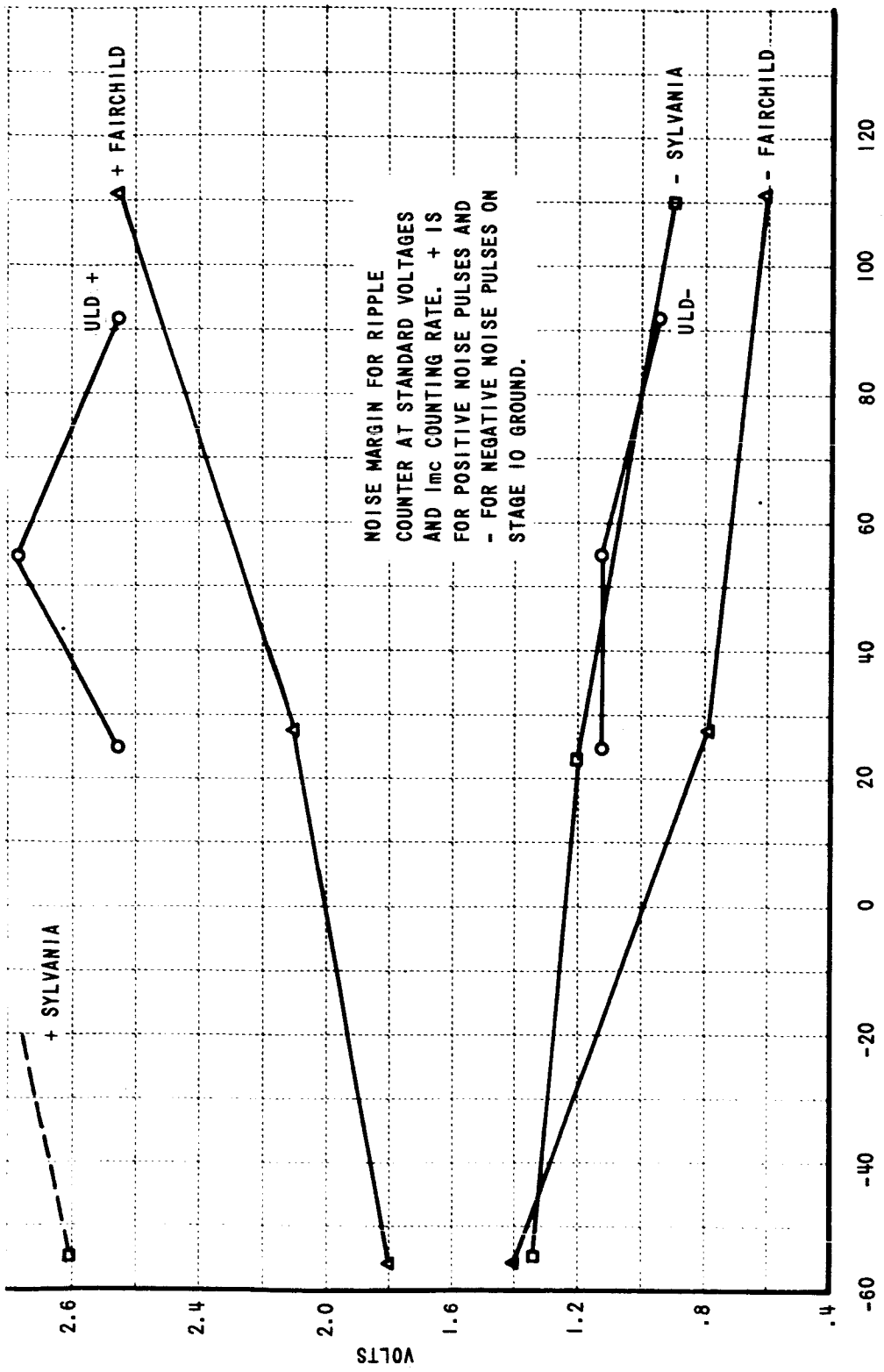

NOISE MARGIN FOR RIPPLE
COUNTER AT STANDARD VOLTAGES
AND Imc COUNTING RATE. + IS
FOR POSITIVE NOISE PULSES AND
- FOR NEGATIVE NOISE PULSES ON
STAGE 10 GROUND.
+ SYLVANIA
+ FAIRCHILD
ULD +
- SYLVANIA
- FAIRCHILD
ULD-
VOLTS
2.6
2.4
2.0
1.6
1.2
.8
.4
-60
-40
-20
0
20
40
60
80
100
120
AMBIENT TEMPERATURE °C

Figure 4.21

generally agree with those in the synchronous counter. On Figure 4.21 the Sylvania and the ULD positive pulse noise curves are partly beyond the limits of the graph.

5.0 THERMAL ANALYSIS

A study was made of the thermal characteristics of the ULD module and the Sylvania and Fairchild flat packs. It was felt that attention to proper cooling paths for the heat generated in the microcircuits would contribute to reliability and proper operation by restricting the temperature rise of the silicon substrate. Since noise margin is generally lowest at high temperature, a lower substrate temperature can increase the system reliability even if failure rates are not significantly decreased.

It was found that very little sound experimental information exists on problems of cooling of integrated circuits. In particular, problems of dynamic heating of the transistors and resistors on the substrate, above that of the d.c. or steady state heating, has had little attention paid to it. Unfortunately, the scope and aim of this program did not allow for the detailed thermal experimental work that is called for in these cases.

5.1 ULD Module

A thermal analysis of the ULD package and its multilayer interconnection board (MIB) was made to determine the effect of the various cooling paths.

The Saturn LVDC page is constructed with two MIB sandwiched around a magnesium-lithium plate, which is clamped to the liquid cooled frame of the computer which acts as a heat sink. Each MIB has 35 ULD modules mounted on it. The chip-to-heat-sink thermal resistance of the page construction is 240°C/watt with free air convection and 290°C/watt with no convection. There is some uncertainty about the thermal resistance of the MIB, since this depends largely on the density of the copper in the board and varies with the circuitry. However, because of the plated-through holes and the conductors plated onto the various layers, the board offers low thermal resistance in both directions and does not greatly affect the total value of thermal resistance.

Mounting and leads are first in importance in providing a good thermal path, convection is second and radiation is almost negligible.

Temperature rises of individual ULD modules on the page will depend on their connection in the circuitry and their resultant power dissipation. For a ULD dissipating 30 mw, the temperature rise for the case with air convection would be about 7°C and without convection it would be about 9°C.

When ULD modules are mounted on a single layer printed circuit board without an adequate metal supporting structure for a heat sink, such as the ULD modules in these tests were, the thermal resistance may be as high as 500 °C watt. This corresponds to a temperature rise of 15°C for a 30 mw dissipation. During test of the shift register and synchronous counter, thermocouples were used to monitor the case and ambient temperatures of the ULD and flat packs. With the ULD's, the case temperature of the inverter modules was usually 1°C, never more than 2°C, above the forced air ambient temperature in the vicinity of the modules.

This indicated that the printed circuit leads on the ULD mounting board were effective in removing heat and the units were derated at 330°C/watt. Since the maximum rated junction temperature of the ULD's was given as 100°C, the units were derated 10°C and the highest temperature tests were run at a forced air ambient of 90°C.

5.2 Flat Pack Module

The thermal circuit of a typical flatpack such as the Sylvania or Fairchild is very similar to that of the ULD, provided a similar MIB and heat sink plate arrangement is used. An estimate of 280°C/watt was derived for a typical 14 lead flatpack. Here again, the conduction through leads and mounting are the most important thermal path. On the printed circuit board upon which the Sylvania or Fairchild circuits were mounted during testing, the flatpacks were thermally bonded to a strip of copper circuit 0.20 inches wide extending the length of the board. Thermal bonding was aided by a film of high conductivity silicone grease between the back of the flatpack and the copper strip. During tests, thermocouples were attached to the flatpack case, the copper strip and in the forced air stream in the immediate vicinity.

The usual temperature differential between flatpack case and copper strip was 1°C and between copper strip and ambient was 1°C. The Sylvania units were derated 13°C and the Fairchild units were derated 15°C because of higher dissipation.

6.0 APPLICATION NOTES

The fact that digital microminiature circuits are very similar to their discrete component predecessors leads system designers to try to use them in much the same way. A straight substitution of microminiature for discrete component circuit often will lead to problems in areas where they are least expected. Some of the information derived in this test and evaluation program is of use in the application of microminiature circuits and is therefore given as a guide to these problem areas.

6.1 Connectors and Connections

As the size of the digital circuit becomes smaller, the size of the whole system also becomes smaller. However, the fraction of the system required for connections certainly increases, and the cost, reliability, size and weight of a system depend more heavily on the connectors in the system. Connectors include (1) the printed circuit boards upon which the microcircuit is mounted, (2) the connector between this board and a mother board, and (3) the wiring harness or ribbon cable tying the system to inputs and outputs. Connectors also include the power distribution system. These connectors become involved as a major cooling path for the heat developed in the circuitry, determine the required noise margin of the circuits and become a major item in determining the reliability of the system. Thus, the connection scheme becomes a part of the circuitry of the digital system, and should not be designed as an afterthought.

New concepts and developments in connections are needed in order that the size, weight and reliability gains made in microminiature circuits are passed on to the system level. However, certain precautions can be taken with the hardware at hand to minimize the connection problem.

An attempt should be made to correlate logical and physical units, so that complete functions can be placed on a single assembly. A counter and its decoding matrix placed on a single assembly would serve to minimize wiring with respect to a design which split these two functions between two assemblies. If splitting is necessary, it may be better, from a total system standpoint, if the counter is split in the middle, each half

with a decoding matrix. The logical designer should become involved in this portion of the layout since he has the knowledge to make these decisions.

Identical signals may be logically generated in several places to minimize transfer of signals between boards. Driver circuits, having high output currents, should be distributed in each assembly and not concentrated at one location. Use of low impedance driver circuits to drive long lines or capacitance circuits is obvious, but use of an input buffer circuit which has very high noise immunity should also be considered. These could be used in cases where signals are transferred between assemblies and, because of signal or ground noise, the signal at the receiving end has a high noise level.

6.2 Multilayer Printed Circuit Boards

Multilayer printed circuit boards are widely used as both mother and microcircuit interconnection boards. One method of construction has signal layers alternating with somewhat solid layers used for ground or power distribution. The idea is that the ground layer will act as a shield between adjacent signal leads, and also tune the signal leads to a characteristic impedance. In actuality the ground planes, carrying high currents with steep wavefronts, generate a high noise level associated with $L \frac{di}{dt}$ and resistance. The signal lead, spaced only .002 to .004 inches away from this ground plane, is capacitively coupled to it and picks up the ground plane noise. Thus the purpose of shielding is defeated and heavy capacity loads are incurred on signal leads. New concepts in the design of multi-layer printed circuit boards are required to circumvent this problem.

6.3 Considerations in Counter Applications

The logical design of the synchronous counter that was evaluated was done with the objective of having a long chain of gates in series, for the carry to propagate so that their delay might be more easily studied. In practice this would limit the speed of operation of the counter and utilize the integrated circuitry poorly. A quick carry scheme where each counter stage is gated with the ANDED ONE side of all the previous counter stages would speed up the carry but would place a large fan-out load on the lower

counter stages. Also, a high fan-in gate would be required for the higher counter stages. A compromise of these two schemes would yield the best balance between delay, fan-out and fan-in factors.

Design of the reset circuitry for the ripple and synchronous counters illustrated the difficulty of using the Sylvania and Fairchild flip flops for these applications. Direct set and reset inputs, free of clock considerations, would have allowed design of a reset logic for the ripple counters and the Fairchild synchronous counter. The logical flexibility of the basic circuit approach used in the ULD modules allowed complete freedom in design of reset logic for both counter applications.

7.0 CONCLUSIONS

A condensation of the parameters of the logic lines tested in the three applications is given in Table 7.1. Values of maximum frequency, noise margin, power supply tolerance and power were taken from the worse case values on their respective curves in the test results. Factors that were very temperature dependent favored the ULD modules because of their more restricted temperature range, so a column rating the temperature range (of the junction) was added to aid in comparison. The value for connections required for each application was the number of leads (pins) required to be connected to operate that application, and with the Sylvania and Fairchild circuits, included back biasing the unused inputs. Also, since the ULD applications did not include a clock driver circuit in the connection or module count, the clock drivers were not counted in the Sylvania and Fairchild applications.

The Sylvania circuits had as high a noise margin as any in all three applications, and had the highest frequency operation, although only slightly higher in the synchronous counter. Fairchild circuits had the lowest power requirements, number of connections and number of modules. The ULD circuits had the highest power requirements, package count and number of connections of all, but had the greatest logical flexibility. From these generalizations and the characteristic curves, relative weights must be put on the various parameters involved and a decision made on the circuits best suited for an application. The relative weights can only be arrived at after a definition is made of the characteristics required of the specific digital system under design.

7.1 Failures:

The ULD, Sylvania and Fairchild circuits were not tested in a standard configuration that would have yielded failure rate data, and the number of circuits involved was so small that confidence limits are very low. Two of the logic lines experienced definite problems in that repeated failures pointed to a weakness in design or manufacture.

TABLE 7.1

Application	Maximun Frequency MC	Noise Margin Volts	Power Supply Tolerance %	Temperature Range °C	Total No. of Connections	Total No. of Modules	Power Required Watts
SHIFT REGISTER							
ULD	4	.27	47	100	412	42	1.4
Fairchild	5.5	.33	25	180	122	11	.44
Sylvania	13	.8	20	155	232	21	.77
SYNCHRONOUS COUNTER							
ULD	1.0	.8	25	100	631	69	1.52
Fairchild	2.2	.6	22	180	237	21	.75
Sylvania	2.7	1.05	20	180	390	34	.81
RIPPLE COUNTER							
ULD	7.0	.9	33	100	592	64	1.8
Fairchild	3.7	.6	20	180	129	12	.45
Sylvania	10	.9	20	180	268	24	.59

ULD

The failure of a high percentage of the ULD inverter circuits that were baked at 150°C points to a connection problem on the ULD substrate between the S clip and the connector pattern on the bottom of the substrate. Failure rate is much higher with connections located near the corners (pins 9 through 14). Examination of a ULD which is soldered to a test board reveals that the S clips are securely fastened to the printed circuit board. If the board bends or vibrates, stresses are set up which may pull S clips away from the substrate. All stresses set up in the board are transmitted to the substrate, which is part of the circuit since the connectors and resistors are bonded to it.

Sylvania

The several Sylvania failures which establish a pattern occurred during the high temperature tests on the shift register and synchronous counter. At about 110°C ambient temperature, three SNG-14 and two SNG-4B units failed while being used as input buffers and being driven by a 5 volt pulse. Two of the units recovered at room temperature, while three did not.

A total of seven Sylvania units were returned to the factory for failure analysis by the manufacturer. Five of these have been analyzed and results forwarded verbally at the time of this report. Two units which had initial faults when received at CAL were reported by the manufacturer to have had open leads due to formation of $AlOH$ on the aluminum conducting layer. This is generally caused by water vapor in the package. For a complete discussion of the cause and its cure, see Reference 9.

The three remaining units were all SNG-14 failures at about 110°C; two of these recovered at room temperature. Of the two which recovered, it was reported by the manufacturer that the fault on one could not be found and the other had an input shorted during analysis before a fault could be found. The report on the third unit was not conclusive in that the fault experienced and trouble reported by the manufacturer did not appear consistent. It was reported that the failure analysis of microcircuits which work at room temperature but not at high temperatures is a very difficult task.

Fairchild

Failures in the Fairchild units did not appear to establish any pattern, other than two units did not operate within specifications.

REFERENCES

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3. Bohn, R., and Seeds, R., "Collector Tap Improves Logic Gating", Electronic Design, pp 50-55, August 3, 1964.

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5. Selikson, B.; and Longo, I.A., "A Study of Purple Plague and its Role in Integrated Circuits", Proc. IEEE, Vol. 52, No. 12, pp 1638-41, December 1964.

6. Luecke, G., "Noise Margins in Digital Integrated Circuits", Proc. IEEE Vol. 52, No. 12, pp 1565-71, December 1964.

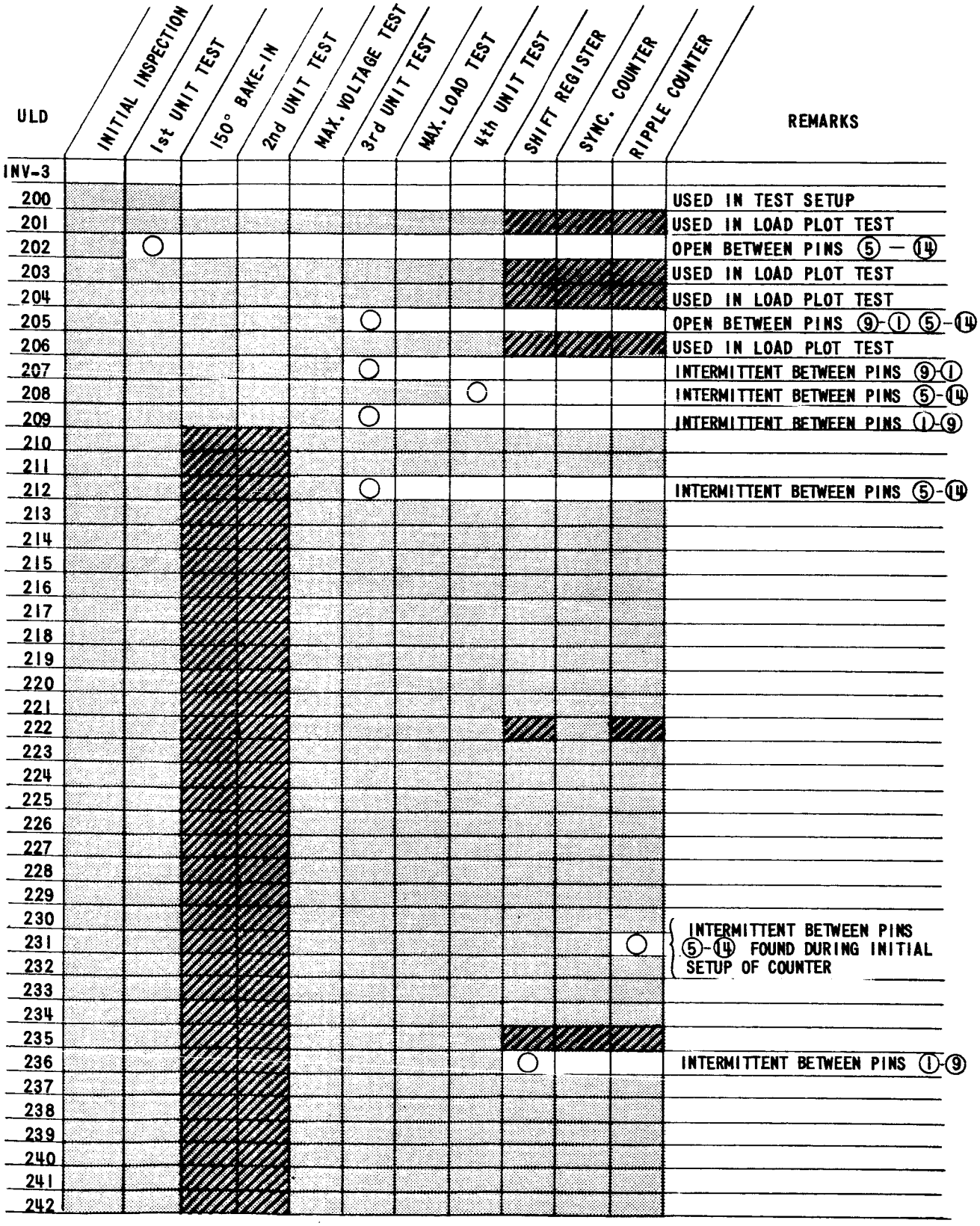
7. Partridge, Jayne; Hanley, L. David; and Hall, Eldon C.; "Progress Report on Attainable Reliability of Integrated Circuits for System Application", Presented at the Symposium on Microelectronics and Large Systems, November 17 and 18, 1964, in Washington, D. C.

8. "Final Report for Integrated Circuit Study", Sperry Rand Corporation, UNIVAC Division, Report PX 3266, August 1963.

9. "Micronotes Number 8", Navy, Bureau of Naval Weapons, pp. 132-50, 1 October 1964.

APPENDIX A

The following Table is a history of each module in this evaluation program, and shows which tests each unit was subjected to. An abbreviated analysis of each failure is given in the remarks column. Units that failed in a stress test may be listed as having failed in that test, if detected, or failed in the following unit test.


ULD
INITIAL INSPECTION
1st UNIT TEST
150° BAKE-IN
2nd UNIT TEST
MAX. VOLTAGE TEST
3rd UNIT TEST
MAX. LOAD TEST
4th UNIT TEST
SHIFT REGISTER
SYNC. COUNTER
RIPPLE COUNTER
REMARKS
INV-3
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
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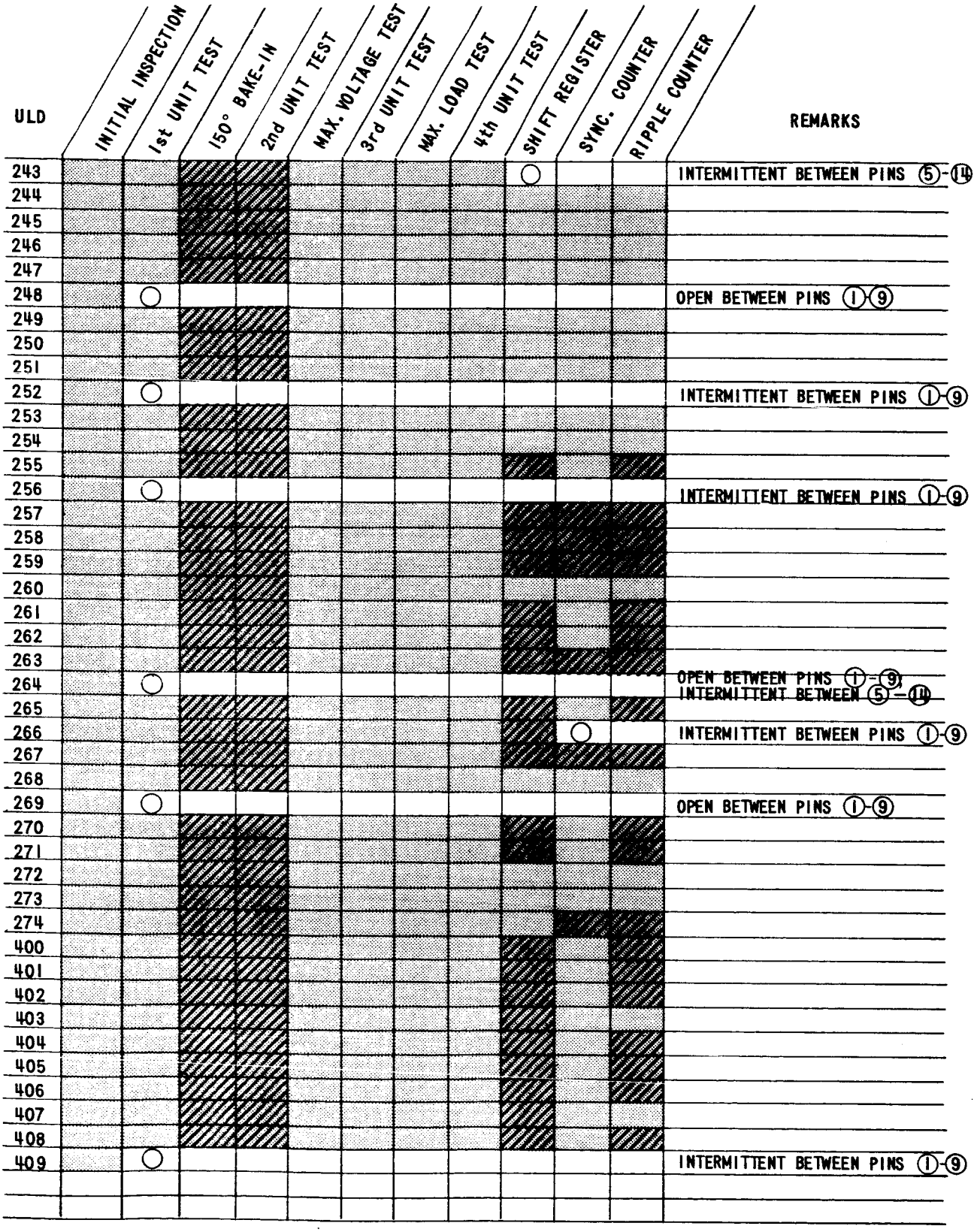
230
231
232
233
234
235
236
237
238
239
240
241
242
USED IN TEST SETUP
USED IN LOAD PLOT TEST
OPEN BETWEEN PINS ⑤ — ⑭
USED IN LOAD PLOT TEST
USED IN LOAD PLOT TEST
OPEN BETWEEN PINS ⑨-①⑤-⑭
USED IN LOAD PLOT TEST
INTERMITTENT BETWEEN PINS ⑨-①
INTERMITTENT BETWEEN PINS ⑤-⑭
INTERMITTENT BETWEEN PINS ①-⑨
INTERMITTENT BETWEEN PINS ⑤-⑭
INTERMITTENT BETWEEN PINS ⑤-⑭ FOUND DURING INITIAL SETUP OF COUNTER
INTERMITTENT BETWEEN PINS ①-⑨


ULD
INITIAL INSPECTION
1st UNIT TEST
150° BAKE-IN
2nd UNIT TEST
MAX. VOLTAGE TEST
3rd UNIT TEST
MAX. LOAD TEST
4th UNIT TEST
SHIFT REGISTER
SYNC. COUNTER
RIPPLE COUNTER
REMARKS
243
244
245
246
247
248
249
250
251
252
253
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255
256
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260
261
262
263
264
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268
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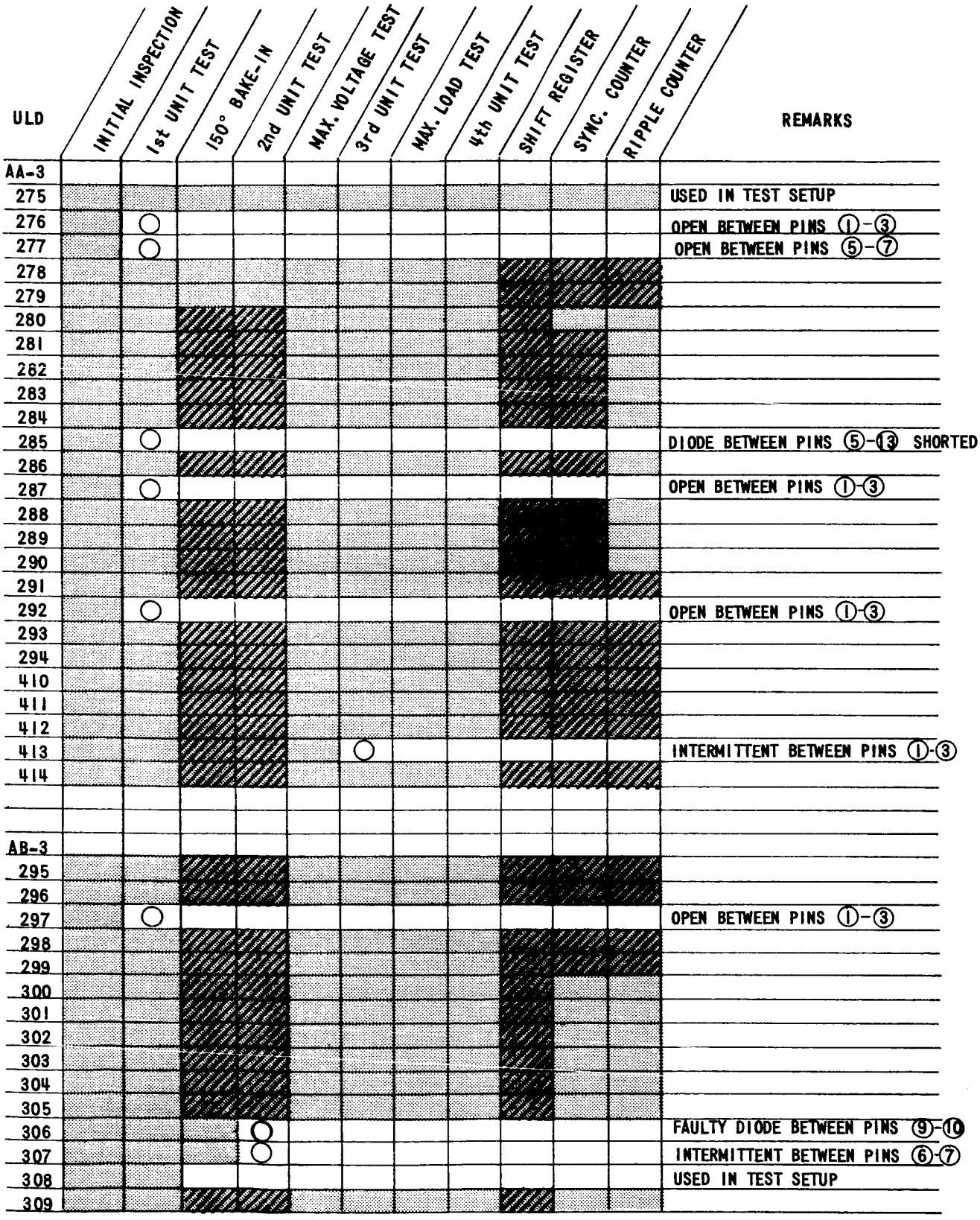
270
271
272
273
274
400
401
402
403
404
405
406
407
408
409
INTERMITTENT BETWEEN PINS ⑤-⑭
OPEN BETWEEN PINS ①-⑨
INTERMITTENT BETWEEN PINS ①-⑨
INTERMITTENT BETWEEN PINS ①-⑨
INTERMITTENT BETWEEN PINS ①-⑨
OPEN BETWEEN PINS ①-⑨
INTERMITTENT BETWEEN ⑤-⑭
INTERMITTENT BETWEEN PINS ①-⑨
OPEN BETWEEN PINS ①-⑨
INTERMITTENT BETWEEN PINS ①-⑨


ULD
INITIAL INSPECTION
1st UNIT TEST
150° BAKE-IN
2nd UNIT TEST
MAX. VOLTAGE TEST
3rd UNIT TEST
MAX. LOAD TEST
4th UNIT TEST
SHIFT REGISTER
SYNC. COUNTER
RIPPLE COUNTER
REMARKS
AA-3
275
276
277
278
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280
281
262
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286
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288
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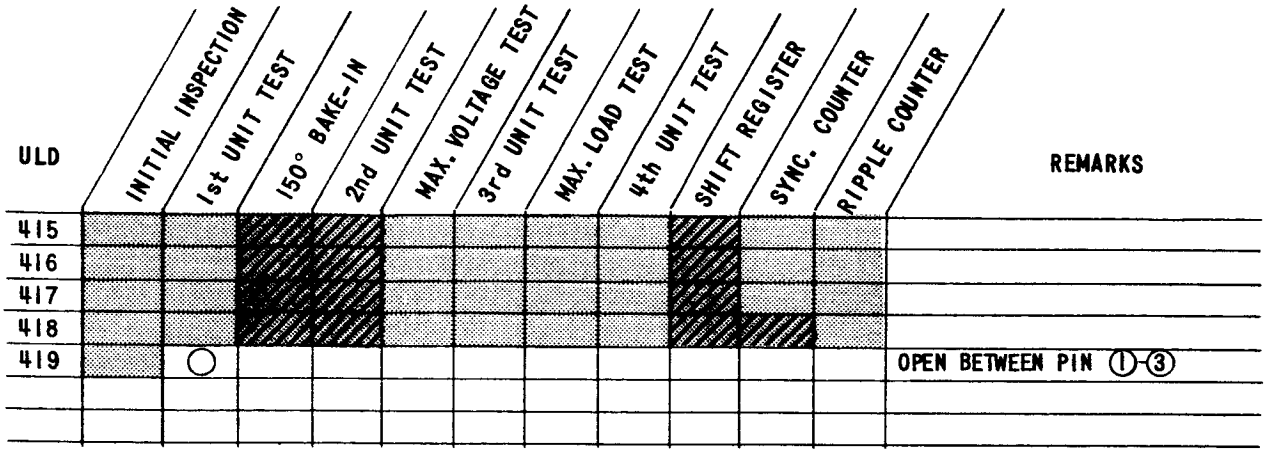
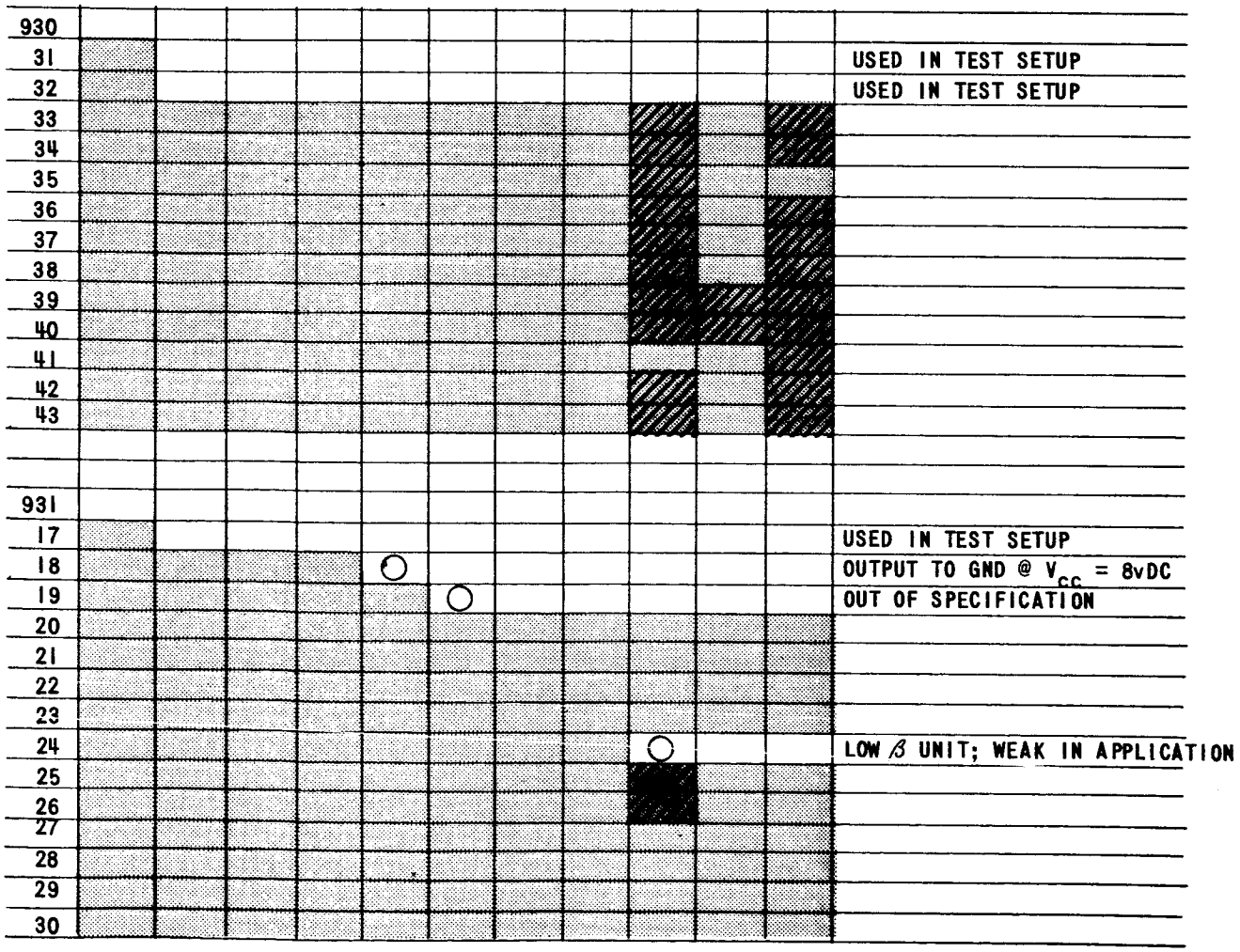
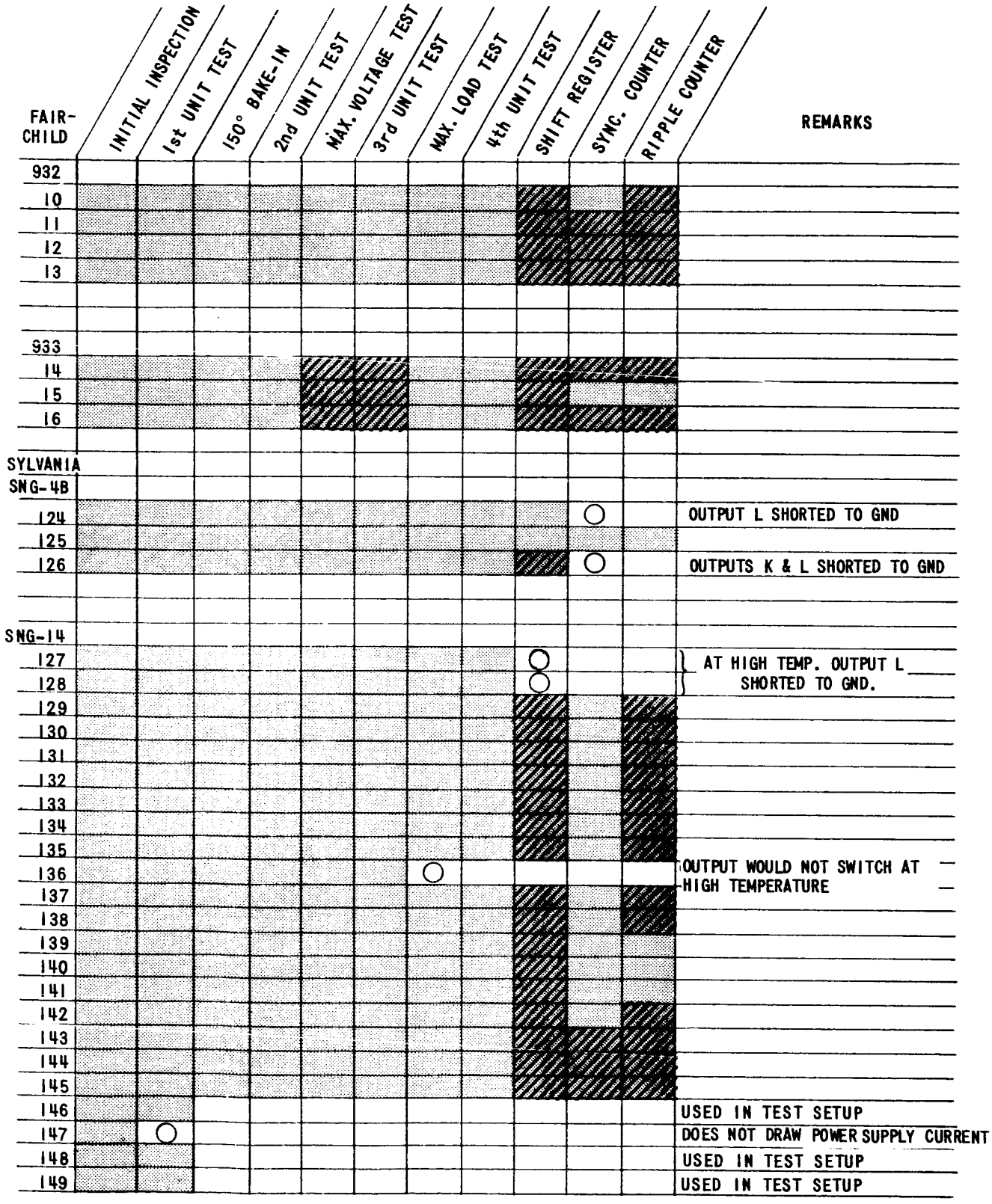
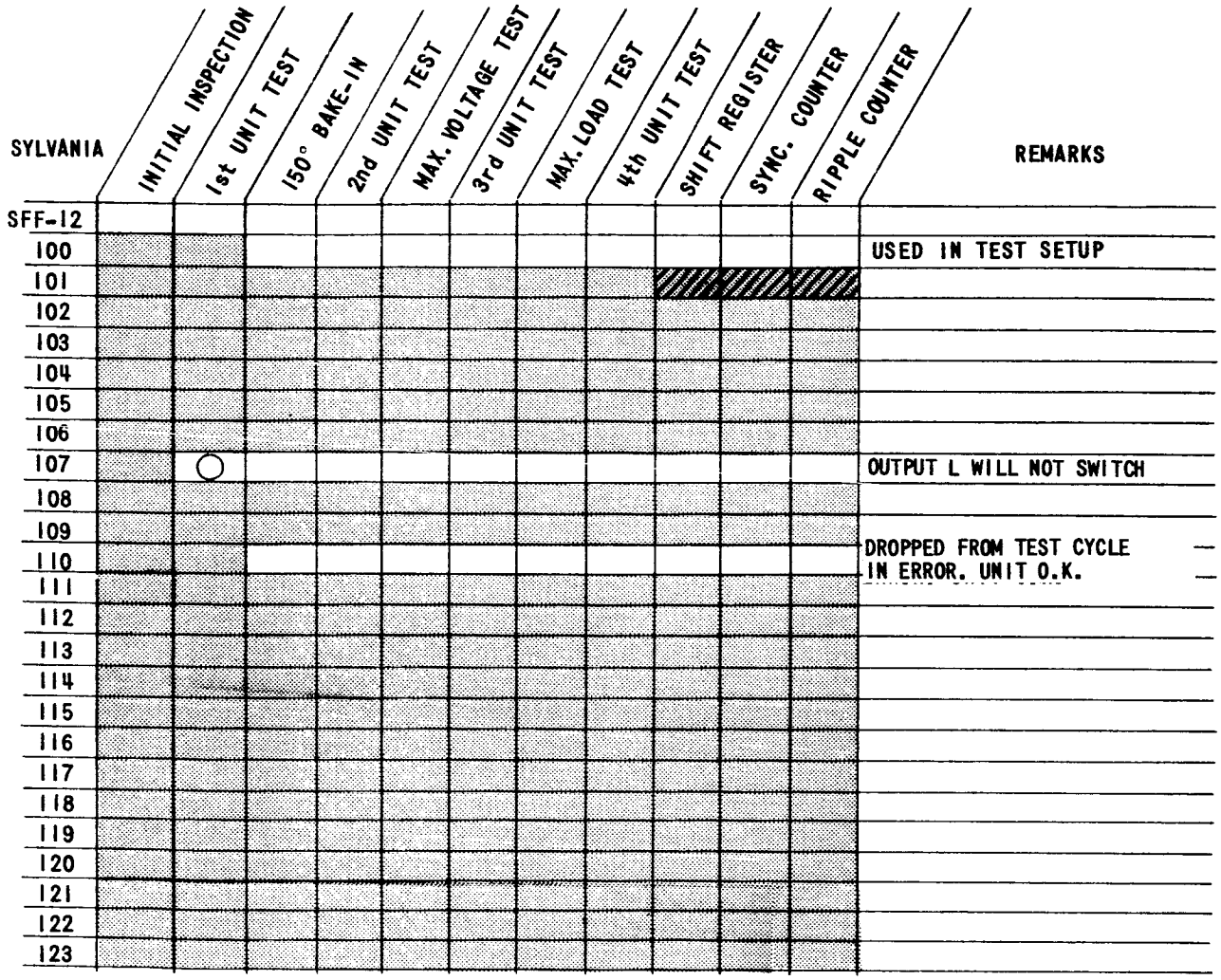
291
292
293
294
410
411
412
413
414
AB-3
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
USED IN TEST SETUP
OPEN BETWEEN PINS ①-③
OPEN BETWEEN PINS ⑤-⑦
DIODE BETWEEN PINS ⑤-⑬ SHORTED
OPEN BETWEEN PINS ①-③
OPEN BETWEEN PINS ①-③
INTERMITTENT BETWEEN PINS ①-③
OPEN BETWEEN PINS ①-③
FAULTY DIODE BETWEEN PINS ⑨-⑩
INTERMITTENT BETWEEN PINS ⑥-⑦
USED IN TEST SETUP


ULD
INITIAL INSPECTION
1st UNIT TEST
150° BAKE-IN
2nd UNIT TEST
MAX. VOLTAGE TEST
3rd UNIT TEST
MAX. LOAD TEST
4th UNIT TEST
SHIFT REGISTER
SYNC. COUNTER
RIPPLE COUNTER
REMARKS
415
416
417
418
419
OPEN BETWEEN PIN ①-③

FAIRCHILD


930
31
32
33
34
35
36
37
38
39
40
41
42
43
931
17
18
19
20
21
22
23
24
25
26
27
28
29
30
USED IN TEST SETUP
USED IN TEST SETUP
USED IN TEST SETUP
OUTPUT TO GND @ V_{CC} = 8vDC
OUT OF SPECIFICATION
LOW β UNIT; WEAK IN APPLICATION


FAIR-CHILD
INITIAL INSPECTION
1st UNIT TEST
150° BAKE-IN
2nd UNIT TEST
MAX. VOLTAGE TEST
3rd UNIT TEST
MAX. LOAD TEST
4th UNIT TEST
SHIFT REGISTER
SYNC. COUNTER
RIPPLE COUNTER
REMARKS
932
10
11
12
13
933
14
15
16
SYLVANIA SNG-4B
124
125
126
SNG-14
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
OUTPUT L SHORTED TO GND
OUTPUTS K & L SHORTED TO GND
AT HIGH TEMP. OUTPUT L SHORTED TO GND.
OUTPUT WOULD NOT SWITCH AT HIGH TEMPERATURE
USED IN TEST SETUP
DOES NOT DRAW POWER SUPPLY CURRENT
USED IN TEST SETUP
USED IN TEST SETUP


SYLVANIA
INITIAL INSPECTION
1st UNIT TEST
150° BAKE-IN
2nd UNIT TEST
MAX. VOLTAGE TEST
3rd UNIT TEST
MAX. LOAD TEST
4th UNIT TEST
SHIFT REGISTER
SYNC. COUNTER
RIPPLE COUNTER
REMARKS
SFF-12
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
USED IN TEST SETUP
OUTPUT L WILL NOT SWITCH
DROPPED FROM TEST CYCLE — IN ERROR. UNIT O.K. —
LEGEND
INCLUDED IN TEST
EXCLUDED FROM TEST
FAILED DURING TEST