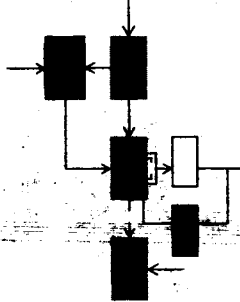


June, 1966

Report **ESL-R-272**
M.I.T. Project DSR 6152
NASA Research Grant NsG-496 (Part)



GPO PRICE \$ _____

CFSTI PRICE(S) \$ _____

Hard copy (HC) 3.00

Microfiche (MF) .75

ff 653 July 65

ELECTRICAL CONDUCTION PROCESSES IN THIN FILMS OF CADMIUM SULFIDE

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N66 37118

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(NASA CR OR TMX OR AD NUMBER)

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Department of Electrical Engineering

ELECTRICAL CONDUCTION PROCESSES IN
THIN FILMS OF CADMIUM SULFIDE

by

James G. Gottling and W. Stewart Nicol

The preparation and publication of this report, including the research on which it is based, was sponsored under a grant to the Electronic Systems Laboratory, Massachusetts Institute of Technology, DSR Project No. 6152. This grant is being administered as part of the National Aeronautics and Space Administration Research Grant No. NsG-496 (Part). This report is published for information purposes only and does not represent recommendations or conclusions of the sponsoring agency. Reproduction in whole or in part is permitted for any purpose of the United States Government.

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ABSTRACT

The electrical conduction properties of vacuum evaporated thin CdS films are studied as a complementary investigation to the fabrication of an active thin film device.

Thermally stimulated emission current measurements indicate that the films have two prominent sets of trapping energy levels, one in the range 0.12 eV to 0.17 eV and the other in the range 0.33 eV to 0.37 eV below the conduction band. Donor levels within 0.004 eV to 0.1 eV below the conduction band are found to have a density of 10^{17} per cm^3 . The effects of post-evaporative treatments of annealing, argon and oxygen ion bombardment, and diffusion of an evaporated sulfur layer, on CdS-metal film barriers are investigated.

The voltage de-excitation of optically modulated conductivity is studied at 77°K and 300°K using voltage pulses of duration between 1 microsecond and 1 second. The change of conductivity, which can be several orders of magnitude depends on pulse duration and is relatively independent of the pulse amplitude.

Current-controlled negative resistance is observed both in the steady-state and at low frequencies for CdS-Au diodes. Evidence of voltage-controlled negative resistance is found for CdS-Ag diodes.

P-type CdS films are formed by controlled amounts of Cu doping and P-N CdS diodes fabricated.

Author

ACKNOWLEDGEMENT

The authors wish to extend grateful appreciation to the Drafting and Publications Staffs of the Electronic Systems Laboratory in the preparation of this document.

Particular acknowledgement is made to Mr. M. Blaho for his valuable contributions to the vacuum evaporation and conductivity measurements of the films.

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CHAPTER I

INTRODUCTION

A. SUMMARY

This report describes an investigation carried out in our laboratory of the conduction-mechanisms occurring in thin films of cadmium-sulfide. The investigation is complementary to the fabrication in the laboratory of an analog thin-film triode, which required that we measure the electrical properties of the cadmium sulfide films and the influence of thin metal film contacts on those properties. Although extensive literature exists^{1*} on single crystal properties of CdS and considerable research has been carried out on the electrical properties of CdS films,^{2,3,4} the variations in those properties are so great that it is necessary to undertake a separate investigation of the conduction behavior for the purpose of device fabrication. Again, the interpretation of the main conduction processes is different for different authors.

The areas which we have investigated experimentally are donor and trapping energy levels, metal-CdS film contacts for various post-evaporation film treatments, the effect of short duration pulsed electric fields on CdS film conductivity, negative resistance phenomena and p-type conduction in CdS films.

Thermally stimulated emission current measurements on our films indicate that they have two prominent sets of energy levels, one in the vicinity of 0.12 eV to 0.17 eV and the other in the vicinity of 0.33 eV to 0.37 eV below the conduction band. Both of these sets of levels are considered to be associated with electron trapping centers. The total energy density of these levels is of the order of 10^{22} per cm^3 , although this anomalously high value should be reduced in proportion to the photoconductive gain. Electron activation energies taken from dark conductivity measurements, have shown additional levels in the 0.004 eV to 0.1 eV region, considered to be

*Superscripts refer to numbered items in the List of References.

associated with donors, and have also shown a remarkably consistent 0.33 eV energy level. A pronounced thermally-stimulated emission current peak at 0.14 eV, which appeared for films that had sulfur diffused into them, agrees with the results of Kulp and Kelly⁵ for interstitial sulfur. For all of our films there was no indication of any pronounced energy level between 0.20 and 0.30 eV, regardless of post-deposition heat treatment at 10^{-5} torr, exposure of the CdS films to argon or oxygen glow discharge, or to diffusion of sulfur into the films. In Chapter II we consider the thermally stimulated emission current measurements in detail.

Barrier measurements on Au-CdS films exhibit Schottky behavior corresponding to an immobile ion density within the CdS films of 10^{17} per cm^3 . This behavior holds for a limited bias voltage range near the zero bias condition. Deviations from the Schottky model outside this range can be explained in terms of higher resistivity or artificial barrier layers within the CdS film adjacent to the blocking electrode. These arise from post-evaporation treatment of the CdS film either before or after evaporation of the blocking electrode. Another possible contributing factor is the importance of the reserve region within the CdS film.

The current-voltage behavior of our Au-CdS-Au films is largely dependent on the Au-CdS barrier at the gold electrode evaporated over the CdS film, rather than on the gold electrode under the film, which is invariably an electrode injecting contact, or on the bulk properties of the CdS film. A V^2 dependence, corresponding to space-charge-limited currents in the presence of shallow trapping levels, has been observed only over limited voltage ranges. This behavior was only found where diffused sulfur or oxygen glow discharge processes were carried out. In general, however, the forward current is according to a higher power of the voltage, or is exponential; the reverse current varies with $V^{1/4}$. The CdS film surface resistivity, measured with electrodes both on the substrate side of the CdS film, is of the order of 10^3 - 10^5 ohm-cm after post-evaporative treatments are made.

A bimodal form of conduction was observed in several films of Au-CdS-Ag diodes which had been annealed in 10^{-5} torr pressure, at 300°C , for approximately six hours before deposition of the silver electrode. This bimodal form was one in which the linear conduction characteristic of the bulk CdS film and the CdS-Ag rectifying characteristic were both displayed on the same trace at 60 c/s. The transition from rectifying to ohmic took place when the reverse breakdown voltage had been reached, and had an accompanying current-controlled negative resistance region; the transition to rectifying occurred at a very low forward voltage and had an accompanying voltage-controlled negative resistance region. So far as is known, this effect had not been observed previously for CdS films. The current-voltage behavior of our films is examined in Chapter IV.

We observed a voltage de-excitation over several orders of magnitude of current at 77°K in CdS films which had been optically excited. Although the effect of electric fields on single crystals is known, no observations have been reported on the effect of variable amplitude and variable duration pulses on polycrystalline films. Our measurements seem to agree with the interpretation given by Kallman and Mark⁶ of an increase in recombination rates. A detailed description of these measurements is given in Chapter V.

We have observed a current-controlled negative resistance that bears a marked resemblance to a similar effect described by Henisch⁷ for point contact rectifiers of Ge, Si, PbSe and PbS. It should be pointed out that negative resistance effects in thin films is by no means a new discovery; it has also been observed by Chopra⁸ and by Beam and Armstrong.⁹ In this report we present two models for the dominant mechanism, of which the model of pair production by avalanche following Schottky emission is the more realistic. Our observations are described in Chapter VI.

P-type CdS films have been formed in our laboratory by W.J. Gajda¹⁰ who determined experimentally that the addition of an amount of copper in the range 1.5-5.0 percent by weight will produce p-type conduction. The Seebeck effect was used as the primary means of verifying that the carriers were holes. P-N CdS diodes were successfully fabricated; their reverse characteristics,

however, proved to be extremely leaky. A discussion of this research on p-type CdS is not included in this report, since it is described in detail in a thesis.¹⁰

B. STRUCTURE OF THE CdS FILMS INVESTIGATED

The electrical properties of thin CdS films, as is well known, are greatly affected both by the film growth and by subsequent post-evaporative treatments. The tendency in the growth of CdS films is to result in a non-stoichiometric film, being deficient in sulfur atoms. These sulfur vacancies have associated donor energy levels, so that film conduction is n-type. Although both source and substrate temperatures are very important in determining the composition of these films, we found that impurities in the CdS evaporant also seem to play an important role in their composition. Although no comprehensive program to study the mechanisms of film growth was undertaken, some qualitative observations were made. Films evaporated from CdS powder which contained approximately 200 ppm impurities (mainly lead), as determined by spectro-chemical analysis, showed only trace amounts, if any, on analysis of the evaporated films; films evaporated from luminescent grade CdS condensed much less readily and with a lower stoichiometric ratio on glass substrates than did the films evaporated from the material containing higher amounts of impurities. We also believe that the rate of evaporation is in some way sensitive to the material of the source. It is, therefore, suggested that a much more detailed study of the role of impurities in the nucleation and growth of CdS films should be made.

On the other hand, several post-evaporative treatments of the films were investigated fairly extensively. Since conduction normal to the plane of the CdS films was examined, usually with a blocking contact at the top surface of the films, it is convenient for the purposes of this report to classify the resulting diode structures as being in one of three categories. We believe that the essential difference between any two categories is in the degree to which the region of the CdS film adjacent to the top surface (remote from the substrate) is affected by the post-evaporative treatment. Briefly:

- | | |
|--------------|--|
| Category I | diodes are annealed following deposition of the blocking electrode |
| Category II | diodes are annealed before deposition of the blocking electrode |
| Category III | diodes have an artificial blocking layer formed either by oxygen glow discharge or by a layer of evaporated and diffused sulfur before deposition of the blocking electrode. |

A more detailed description of the techniques used to form these categories is given in the next section. It is suggested that a separate investigation of the depth of the region which is affected by these treatments could also be made by longitudinal resistivity measurements on both lower and upper surfaces of the films. Most of our investigation was made with conduction normal to the films.

C. EXPERIMENTAL

The thin film evaporations were made in a CEC model LC1-18A vacuum coating unit at a pressure of $1 - 2 \times 10^{-5}$ torr. The unit was equipped with a rotatable source holder, permitting the selection of up to six sources, one at a time. The substrate was mounted 24 cm above the source, with a movable mask holder immediately below the substrate. Both sources and masks could be moved from outside the vacuum system, allowing a sequence of evaporations to be made in one pumpdown. When required, the substrate was heated by a G.E. 250 watt quartz rod heater, placed approximately 3 cm above it. The substrate temperature was measured with an iron-constantan thermocouple placed in contact with the (upper) side of the substrate remote from the source.

Cadmium sulfide, sulfur, gold, silver and indium film evaporations were made from 6 cm x 1 cm molybdenum boats; aluminum was evaporated from 1 cm diam helical tungsten coils. The CdS used was Baker and Adamson Lots K305 and P042, and Sylvania luminescent grade type S-20. Film thickness, in the case of metal films, was obtained from the amount of metal evaporated using the Knudsen source law; in the case of CdS films, film thickness during evaporation was obtained by observation of the color of interference

fringes produced in reflected white light. The CdS film thickness profile at an edge was also obtained following evaporation by an interference method which did not require an overlying contour film.¹¹

The substrates were 75 x 25 mm Fisher microscope glass slides, ultrasonically cleaned in detergent solution, rinsed in distilled water, then in Merck reagent isopropyl alcohol and heat dried in isopropyl vapor.

The electrode configuration for conductivity measurements normal to the CdS film is shown in Fig. 1. Electrode 1, evaporated

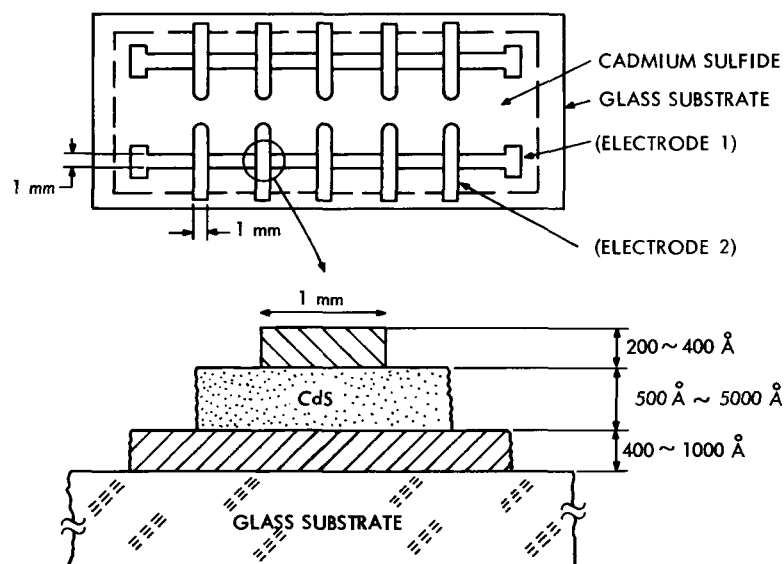


Fig. 1 Arrangement of Diodes on Substrate

directly onto the glass, was invariably an electron injecting contact, even when gold was used for the material. Its thickness was in the range 400~1000 Å. Electrode 2 was of gold for most conductivity measurements, its thickness being limited to the range 200~400 Å so that the underlying CdS film could be optically excited.

The techniques used to form the various categories of diodes were:

Category I: The injecting electrode (≈ 400 to 1000 \AA gold or indium) and the CdS film were evaporated. The CdS surface might then be exposed for two minutes to a glow discharge bombardment

of argon ions at 50 μ Hg pressure and 1500 to 2000 volts, before evaporation of the second electrode. The ion bombardment was carried out with the film at room temperature. Following the evaporation of the second electrode, the complete diode structure was annealed at 300°C for several minutes in air at atmospheric pressure. It was observed that argon ion bombardment, and in a few cases, annealing, was not essential to the formation of this class of diode, but that for most diodes it did enhance the contact formation process.

Category II: The injecting electrode and CdS film were evaporated. Before the evaporation of the second electrode, the film was annealed at 10^{-5} torr pressure. Annealing times and substrate temperatures ranged from 1/2 hour at 360°C to one hour at 320°C. After annealing had been completed, the film was cooled to ambient temperature and the CdS surface might then be exposed for two minutes to a glow discharge bombardment of argon ions at 50 μ Hg pressure and 1500 to 2000 volts. Again, it was verified that argon ion bombardment was not an essential part of the contact formation process, but did enhance it. The second electrode (200 to 400 Å gold) was then evaporated.

Category III: The injecting electrode and CdS film were evaporated and the substrate cooled to ambient temperature. An artificial blocking layer was then formed on the surface of the CdS film before the evaporation of the second electrode. This artificial blocking layer was formed either (a) by exposing the surface to bombardment by oxygen ions at 100 μ Hg pressure and 1000 volts for 30 minutes, or (b) by evaporating a layer of sulfur of less than 100 Å and diffusing it into the cadmium sulfide film by heating the substrate to 90°C for five minutes. In both cases, (a) and (b), the substrate was cooled to ambient temperature before evaporation of the second electrode. Since the cadmium sulfide films exhibit n-type conductivity, in general due to sulfur vacancies, it is very likely that atoms of oxygen or sulfur occupied these vacancies, consequently forming a layer of less n-type cadmium sulfide. In the case of evaporated and diffused sulfur, it is also likely that a thin insulating layer of sulfur was formed.

CHAPTER II

DONOR AND TRAPPING ENERGY LEVEL MEASUREMENTS

A knowledge of the location and energy density of electron energy levels within the forbidden gap in CdS films is relevant to predicting the behavior of these films when used in space-charge-limited current devices. As pointed out by Wright,¹² the presence of high-density, shallow-trapping levels can enhance the gain-bandwidth product of an analog-triode type device; whereas, the presence of high-density, deep-trapping levels will have an adverse effect. High-density, shallow-level traps, in addition to donor states, affect the electronic conduction behavior of the contact region between a thin metal film and the CdS film. Our measurements show that there are two sets of energy levels, one in the vicinity of 0.12 eV to 0.17 eV and the other in the vicinity of 0.33 eV to 0.37 eV below the conduction band, both sets considered to be associated with electron trapping centers. Additional levels in the 0.004 eV to 0.1 eV region are considered to be associated with donor states. Due to the low mobility of holes, only electron trapping has been considered. We have determined the location in energy of levels within the forbidden gap and their energy densities from the measurement of thermally stimulated emission currents. Additional information has been gained by applying a Fermi-level analysis to the measurement of the dark conductivity of the CdS films to obtain electron activation energies.

A. EXPERIMENTAL

The apparatus used for measuring dark and light conductivities and thermally stimulated currents is shown in Fig. 2. The substrate holder consisted of a semi-cylindrical aluminum block in which were embedded three ceramic insulated tungsten heater coils connected in series. The holder was placed in a close-fitting pyrex tube within a liquid nitrogen Dewar. The pyrex tube was connected to a vacuum pump and was surrounded by an opaque foil to permit current measurements to be made in darkness, still allowing circulation of liquid nitrogen around the pyrex tube. A lucite rod, the lower end of which

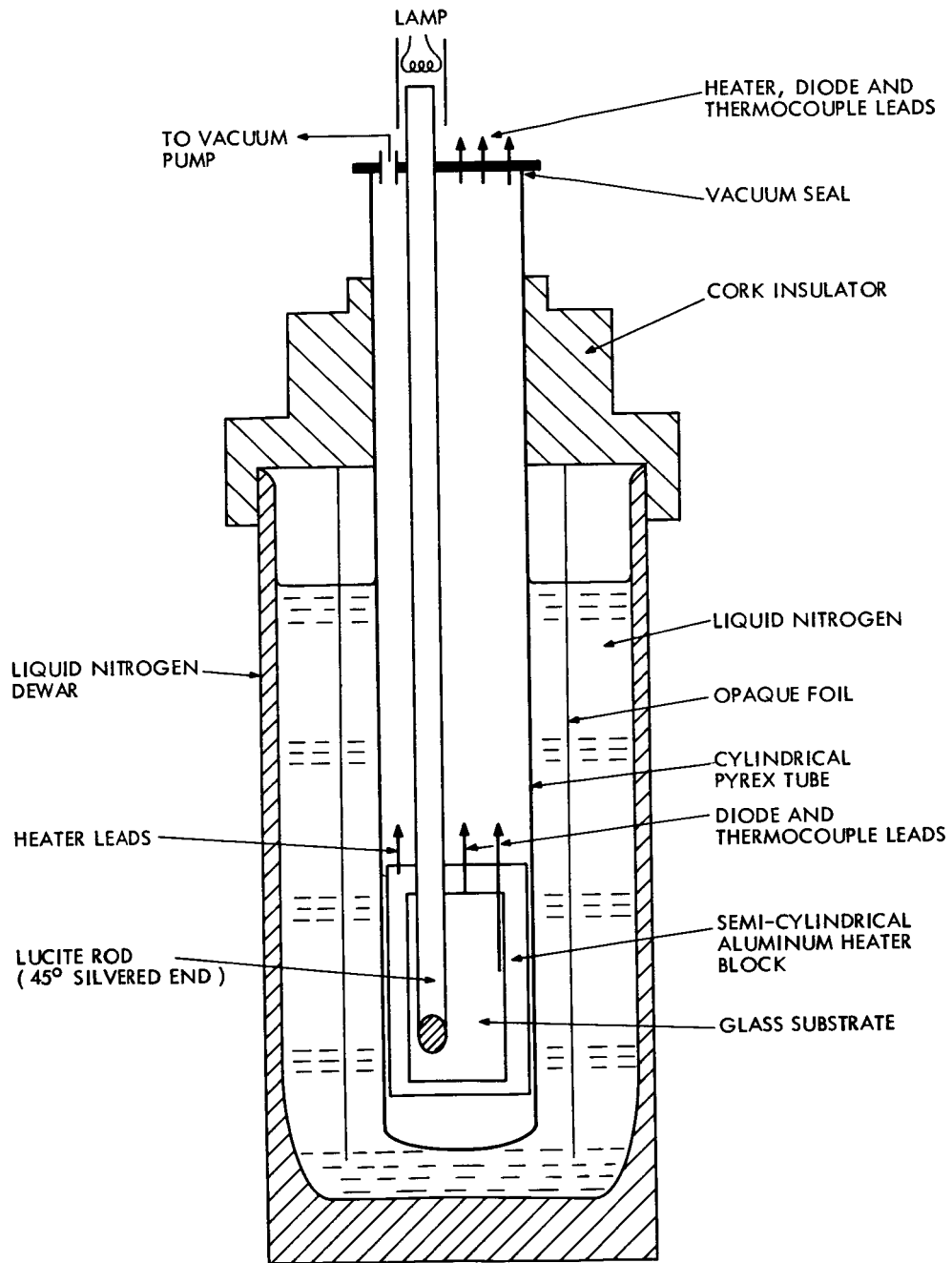


Fig. 2 Apparatus for Measurement of Thermally Stimulated Emission Currents

was cut at 45° and silvered, allowed illumination of any one of the diodes on the substrate without removal of the pyrex tube from the Dewar.

Heating rates of up to $0.2^\circ \text{K}/\text{sec}$ and linear to ± 5 percent within the range 77°K to 400°K were obtained. Electrical contact to each diode electrode was made by beryllium-copper strips which made pressure contact to a silver film painted over each electrode. Four contacts were used for any particular diode measured, two of which were current-supply contacts, the other two were voltage-measuring contacts. Temperature was measured using an iron-constantan thermocouple clamped to the aluminum substrate holder. Current and voltage were both measured by means of Hewlett-Packard Model 412A micro-volt-ammeters.

Before each conductivity vs. temperature measurement, the air pressure in the tube containing the substrate holder was reduced to approximately one micron H_g , with the diode kept in darkness. With the diode leads shorted, the temperature was raised to between 100°C and 140°C before being lowered to 77°K . It was necessary to perform this cycle to obtain the lowest currents at 77°K . Probably this latter process greatly aided the depopulation of the deeper trapping energy levels within the band gap.

B. MEASUREMENTS OF DARK CURRENT VS. TEMPERATURE

The measurements of dark current and thermally stimulated emission current described in this chapter were all taken with electrode 1 biased positively with respect to electrode 2. The voltage applied between the electrodes was 20 mV, that is, in the linear region of the current ~ voltage curve. Where a value for conductivity is stated, this has been calculated assuming that the voltage varies linearly over the total thickness of the film. The error introduced by this assumption into energy level calculations is not too great. Again, the active area of the CdS film is assumed to be 10^{-2}mm^2 , (the electrode overlap area) which may not be correct due to the dominant conduction probably existing along grain boundaries.

Measurements of dark conductivity, σ_D , for most CdS films displayed linear relationships of $\ln \sigma_D$ with inverse temperature. It was observed that for any one film a linear part of the curve holds only for a certain temperature range, but over the whole temperature range between 77°K and 380°K, there were, at most, four linear parts. Assuming that over any particular linear region the dominant conduction mechanism could be attributed to electrons excited from a level of energy E_i , then

$$\begin{aligned}\sigma_D &= n_c q \mu = N_c q \mu \exp [-(E_c - E_i)/kT] \\ &= N_c q \mu \exp [-E_a/kT]\end{aligned}\quad (2.1)$$

assuming non-degenerate statistics to hold, and where

$$E_a = E_c - E_i \quad (2.2)$$

is the electron activation energy. The activation energy for each linear region could, therefore, be obtained from the slope of the $\ln \sigma_D$ vs. $1/T$ curve or from the slope of $\ln i_D$ vs. $1/T$, where i_D is the dark current resulting from the constant applied voltage.

C. VARIATIONS IN THE DARK CONDUCTIVITY OF ANY PARTICULAR CdS FILM

Before measurements of dark current were taken, the film temperature was first raised to 380°K before being lowered to 77°K. It was observed that if this procedure had not been carried out, the conductivity at 77°K would have been several orders of magnitude larger than when this temperature cycling was initiated. However, even after cycling, it was observed that the depopulation of energy levels close to the conduction band had not reached the equilibrium state for 77°K. An example of this is given in Fig. 3 where repeated dark conductivity measurements have been made on a single CdS film. From conductivity decay curves (Chapter V) for temperatures between 77°K and room temperature, it can be shown that negligible error is introduced by decay during the linear temperature rise from 77°K where an equilibrium population of trapping levels has not been reached at the low temperature.

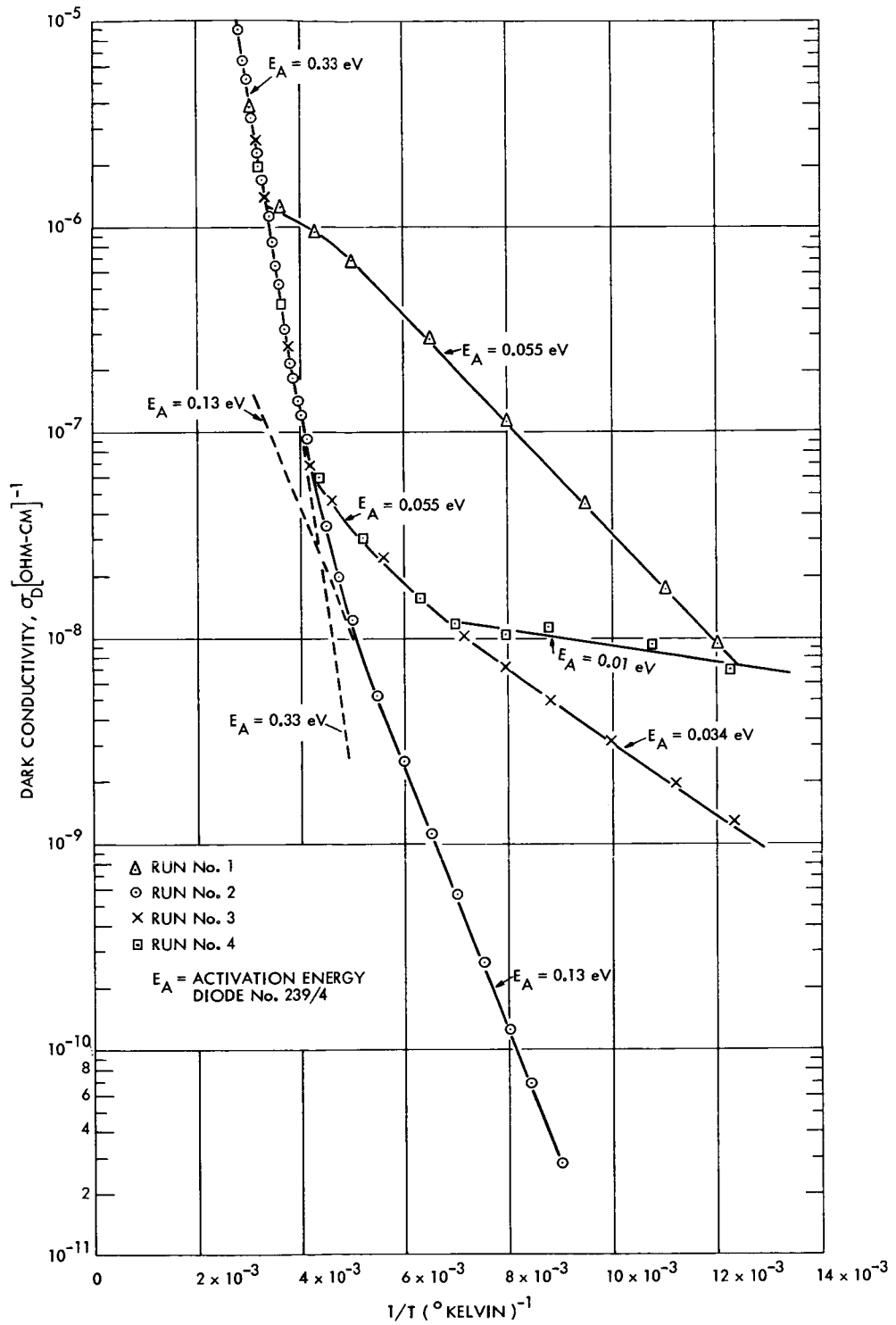


Fig. 3 Variations in Dark Conductivity with Temperature for a Single Film

The activation energies from Eq. 2.1, over various temperature ranges, for a film (No. 239/4) on which a series of conductivity measurements were made are given in Table 1.

Table 1

Activation Energies For One Film

Run	Activation Energy (electron volts) and Temperature Range
1	0.055 eV(80°K~170°K); 0.029 eV(170°K~190°K); 0.33 eV(190°K~350°K)
2	0.13 eV(100°K~230°K); 0.33 eV(230°K~350°K)
3	0.034 eV(80°K~150°K); 0.055 eV(150°K~240°K); 0.33 eV(240°K~350°K)
4	0.01 eV(80°K~150°K); 0.055 eV(150°K~240°K); 0.33 eV(240°K~350°K)

Run No. 1 was made without temperature cycling and shows that a level at 0.055 eV was still largely populated at 80°K. Runs Nos. 2, 3, and 4 were made after temperature cycling and display various degrees of energy level population at the low temperature. A consistency in the 0.33 eV level is found for all runs, which agrees with the predominant energy level in the vicinity of 0.33 eV found by thermally stimulated emission currents.

A Fermi-level analysis can be performed, assuming the applied voltage is distributed uniformly across the width of the film, that the active area is known, and neglecting any temperature variation of mobility or variation of the effective density of states in the conduction band.

$$\frac{i}{A} = \sigma \left(\frac{V}{d} \right) = n_c q \mu \left(\frac{V}{d} \right) = N_c q \mu \left(\frac{V}{d} \right) \exp \left[- (E_c - E_F) / kT \right]$$

or
$$E_F = E_c - kT \ln \frac{N_c q \mu V A}{i d} \quad (2.3)$$

- where
- i = total current, in amps
 - σ = conductivity, in $(\Omega - \text{cm})^{-1}$
 - n_c = free electron density, cm^{-3}
 - μ = electron mobility $\cong 4 \text{ cm}^2/\text{volt-sec}$
 - q = electronic charge
 - N_c = effective density of states at the lower edge of the conduction band, $qN_c = 1.6 \text{ coulombs/cm}^3$
 - A = diode area = 10^{-2} cm^2
 - d = CdS film thickness, cm
 - V = applied voltage
 - E_F = Fermi-level energy, in eV
 - k = Boltzmann constant = $8.62 \times 10^{-5} \text{ eV/}^\circ\text{K}$
 - T = absolute temperature, $^\circ\text{K}$

The Fermi-level variation with temperature for the two lowest conductivity runs, Nos. 2 and 3, is given in Fig. 4. For a temperature

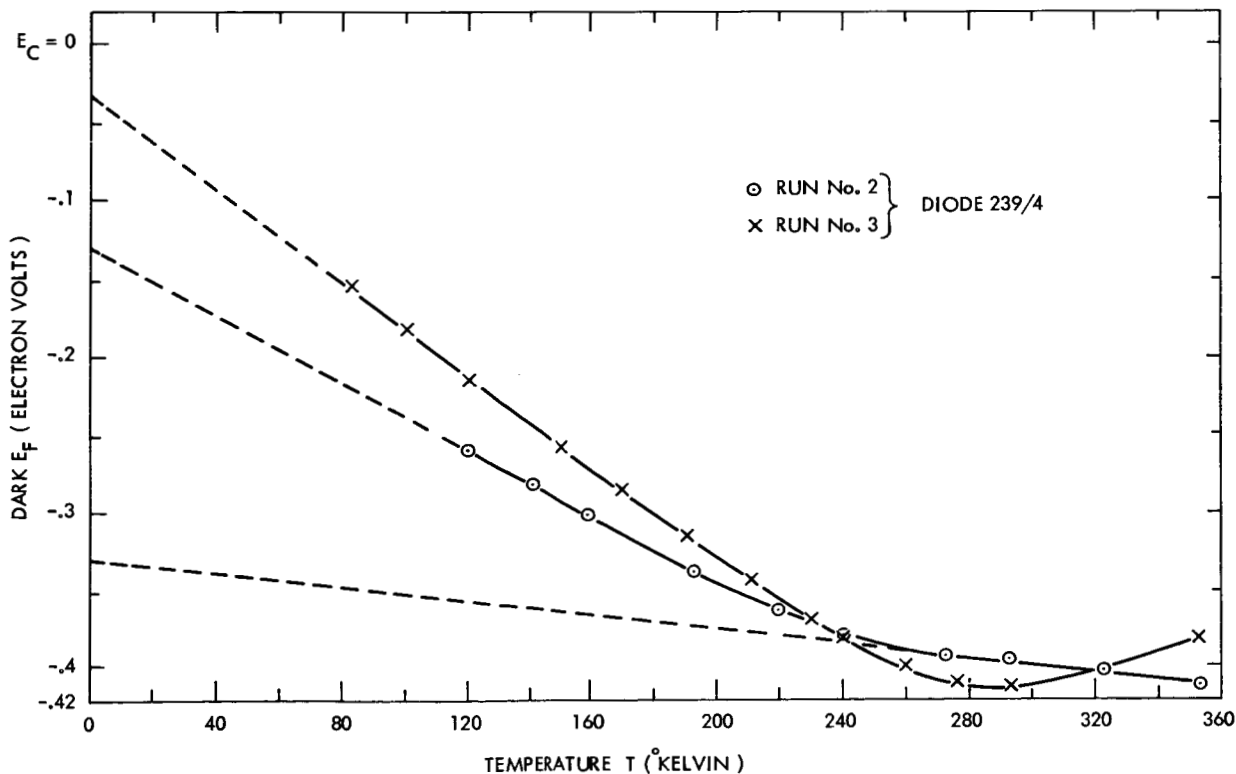


Fig. 4 Variation of Dark Fermi-Level With Temperature

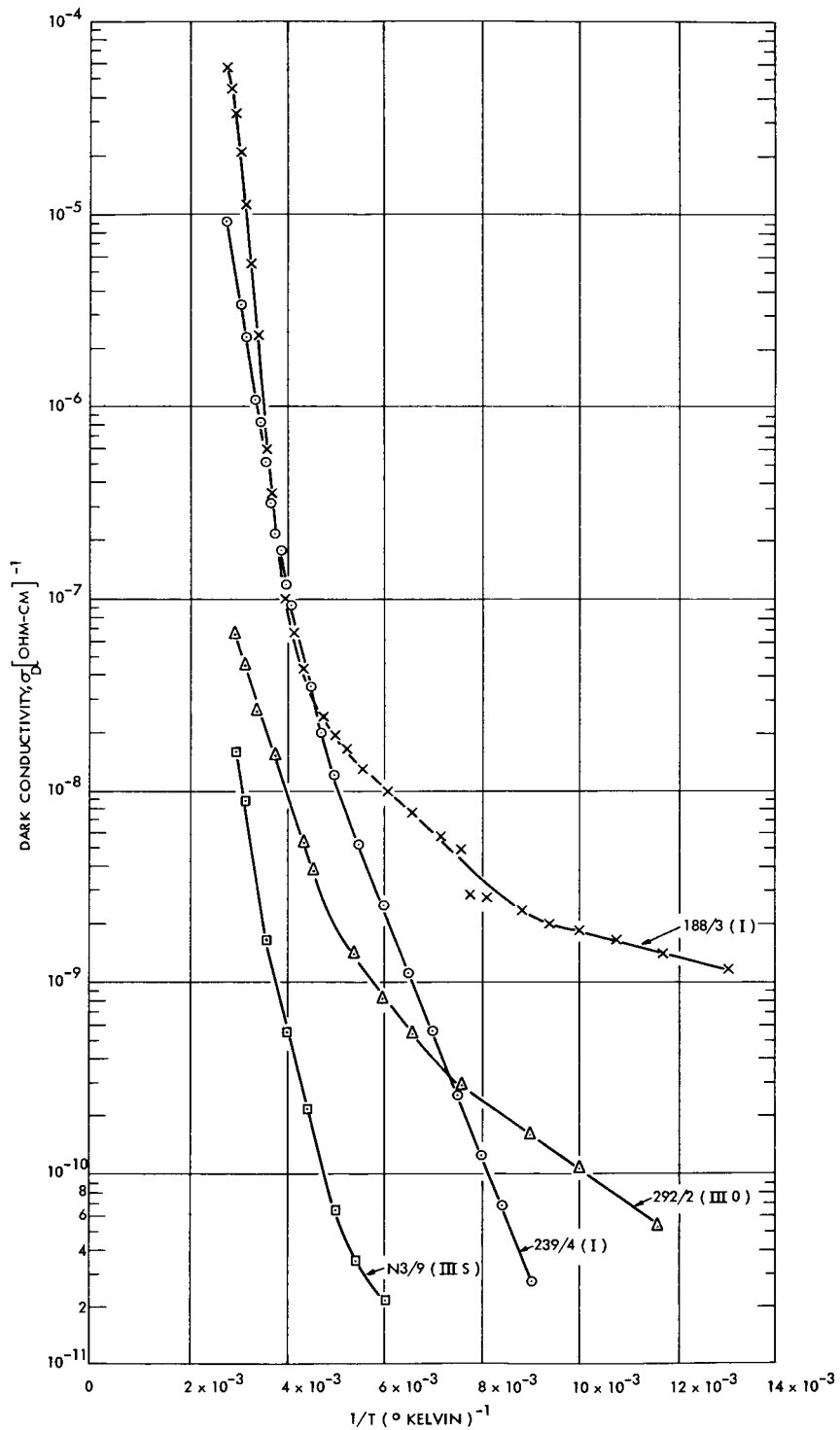


Fig. 5 Variation in Dark Conductivity with Temperature for Several Films

range lower than 200°K in each run the variation is linear:

$$E_F = E_o - AT \tag{2.4}$$

where A is a positive constant. Several models to identify the constants E_o , A, together with a discussion of possible reasons for the activation energies, are contained in Appendix C.

A possible explanation for the predominance of the 0.029 eV level in the mid-range of temperature (170°K to 190°K) in run No. 1, is that it is associated with a center having a fairly large recapture cross-section. In the conditions of run No. 1 it was populated by the large number of carriers excited from the 0.055 eV level over the temperature range 80°K to 170°K, which were then re-excited between 170°K and 190°K.

The variation of Fermi-level with temperature for both dark and light conductivity measurements is shown in Fig. 6.

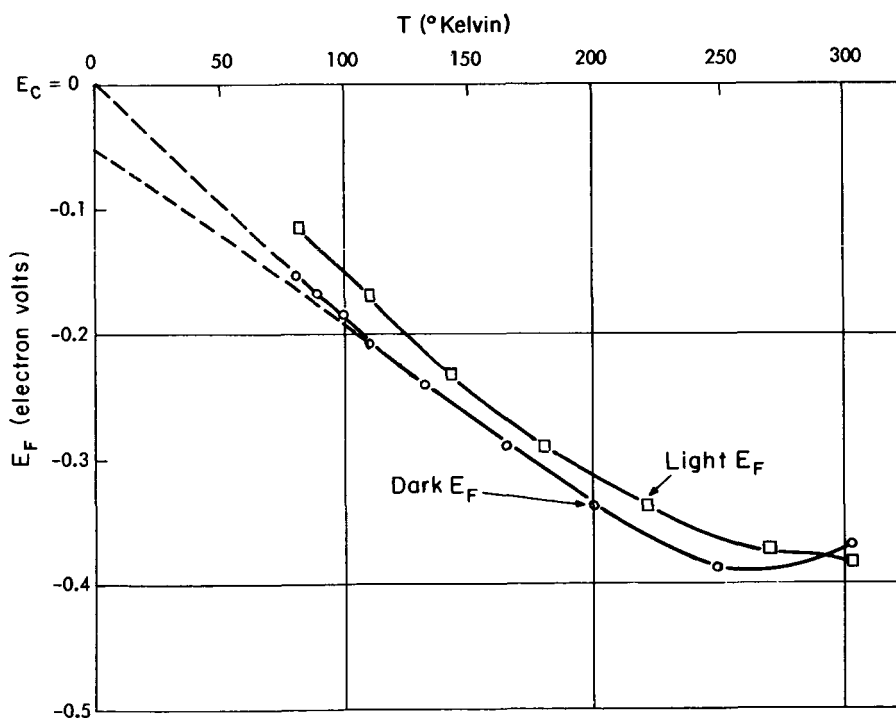


Fig. 6 Variation of Dark and Light Fermi-Levels with Temperature

D. ACTIVATION ENERGIES FOR CdS FILMS FORMED UNDER VARIOUS EVAPORATION CONDITIONS, HAVING DIFFERENT SURFACE TREATMENTS AND OF DIFFERENT THICKNESSES

The variation of dark conductivity with temperature was obtained for several CdS films in Categories I, III (sulfur) and III (oxygen). Dark conductivity measurements were made on a Category II diode at 77°K and at 300°K. Diodes having either an intrinsic or an insulating layer, that is, those in Categories III (oxygen) and III (sulfur) have lower conductivity, which is to be expected, and have very consistent activation energies.

Table 2 lists the activation energies of those diodes, typical examples of whose conductivities are given in Fig. 5. Activation energies obtained during dark conductivity measurements other than those given in Fig. 5 are also included. In the table, the CdS film surface type number refers to that given by A. Aponick.¹³ Although no electron microscope investigation was carried out on these particular films, the evaporation conditions were held as closely as possible to the conditions used by Aponick.

Table 2

Activation Energies for Several Films

Film Number	Diode Category	CdS Film Surface Treatment	CdS Film Surface Type	CdS Film Thickness Å	Activation Energies (eV)
199/1	I	Argon ion bombardment	1	700	0.059, 0.27
200/7	I	Argon ion bombardment	2	2050	0.006, 0.33
184/8	I	none	2	3400	0.178, 0.33 0.43, 0.59
176/8	I	Argon ion bombardment	2	4800	0.041, 0.34
187/3	I	Argon ion bombardment	2	4800	0.053, 0.29
188/3	I	Argon ion bombardment	2	4800	0.008, 0.02 0.043, 0.35 0.59
239/4	I	Argon ion bombardment	2	4800	0.008, 0.034 0.057, 0.33
N3/9	IIIS	Evaporated and diffused sulfur	3	4800	0.004, 0.12 0.27, 0.29
291/2	IIIO	Oxygen ion bombardment	1	4800	0.004, 0.134 0.21
292/2	IIIO	Oxygen ion bombardment	2	4800	0.023, 0.098 0.137, 0.25

E. THERMALLY STIMULATED EMISSION CURRENTS

The energy below the conduction band, E_T , of a defect state (either donor or trapping level) is obtained¹⁴ from the peak temperature, T_m , for which there is a maximum in the difference between the current, i_s , after optical stimulation, and the current, i_D , before optical stimulation, at the temperature, T_m ,

$$E_T = kT_m \ln \left[\frac{qN_c \mu AV}{i_{sm} d} \right] \quad \text{electron volts} \quad (2.5)$$

in which μ = electron mobility in the CdS films
 ≈ 4 cm/volt-sec
 A = diode area = 10^{-2} cm²
 d = CdS film thickness, cm
 V = applied voltage = 20×10^{-3} volts
 i_{sm} = value of light current, i_s , at temperature T_m

Several methods have been given by various authors for calculating defect state energies from either "glow curves" or from thermally stimulated emission currents.¹⁴⁻²² Dittfield and Voigt²³ have compared eleven different methods and have found that Bube's method, used in this report, is superior for heating rates up to $1.5^\circ\text{K}/\text{sec}$. Nicholas and Woods²⁴ have also critically compared several methods.

The energies of defect states using Eq. 2.5 were obtained for CdS films contained in diodes in Categories I, III (sulfur), and III (oxygen). Diodes in these Categories, as well as diodes formed from CdS surface types 2 and 4 were examined. Measurements were also made on CdS film thicknesses ranging from 700 \AA to 5000 \AA .

For most diodes examined there were two thermally stimulated emission current peaks, one in the vicinity of 90°K , and one between 280°K and 340°K . In all cases there is a current minimum at 170°K . The energy levels corresponding to the peaks lie between 0.12 eV and 0.14 eV , and between 0.37 eV and 0.42 eV , respectively. Energy levels having correspondingly smaller thermally stimulated peak currents have been found at 0.31 eV , 0.33 eV , and 0.37 eV .

A list of energies found by this method for typical diodes measured, together with a comparison of their activation energies is given in Table 3.

Table 3

Activation Energies and Thermally Stimulated Emission Current Levels

Diode Number	Activation Energies (electron volts)	Thermally Stimulated Emission Current Levels (electron volts)
199/1	0.059, 0.27	0.31
200/7	0.006, 0.33	0.33, 0.34
184/8	0.178, 0.33, 0.43, 0.59	0.14, 0.42
176/8	0.041, 0.34	0.36
187/3	0.053, 0.29	No distinct level
188/3	0.008, 0.02, 0.043, 0.35, 0.59	0.12, 0.37
239/4	0.008, 0.034, 0.057, 0.33	0.125, 0.37
N3/9	0.004, 0.12, 0.27, 0.29	0.145, 0.15, 0.36, 0.39
291/2	0.004, 0.134, 0.21	0.37
292/2	0.023, 0.098, 0.137, 0.25	0.18, 0.32, 0.51

Typical curves of $(i_s - i_D)$ vs. temperature are shown in Fig. 7 for several films. It is observed that a low temperature peak does not occur in the case of film No. 239/4. This observation was true for many of the films examined, and can be explained by the lack of sufficient optical stimulation of the film to raise the light Fermi-level above the level of the defect state. For example, in Fig. 8, the Fermi-level at a low temperature, T_0 , is raised from the dark value at A to a value at B, above the defect state level, E_T . Provided the initial rapid decay of the Fermi-level at T_0 , to the value at C does not drop below E_T , a thermally stimulated peak current

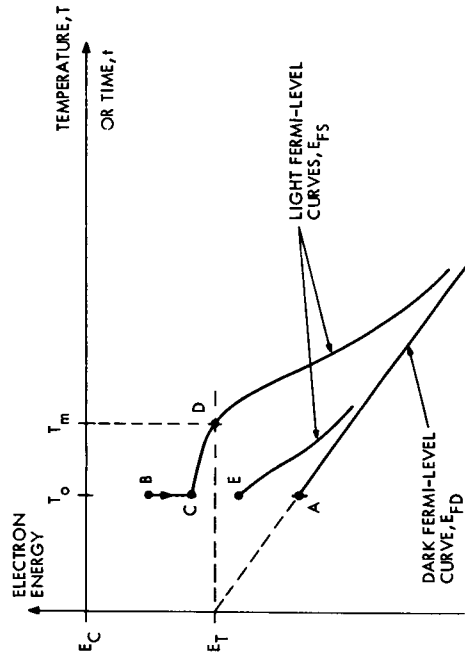


Fig. 8 Variation of Dark and Light Fermi-Levels with Temperature near a Defect Energy Level, E_T

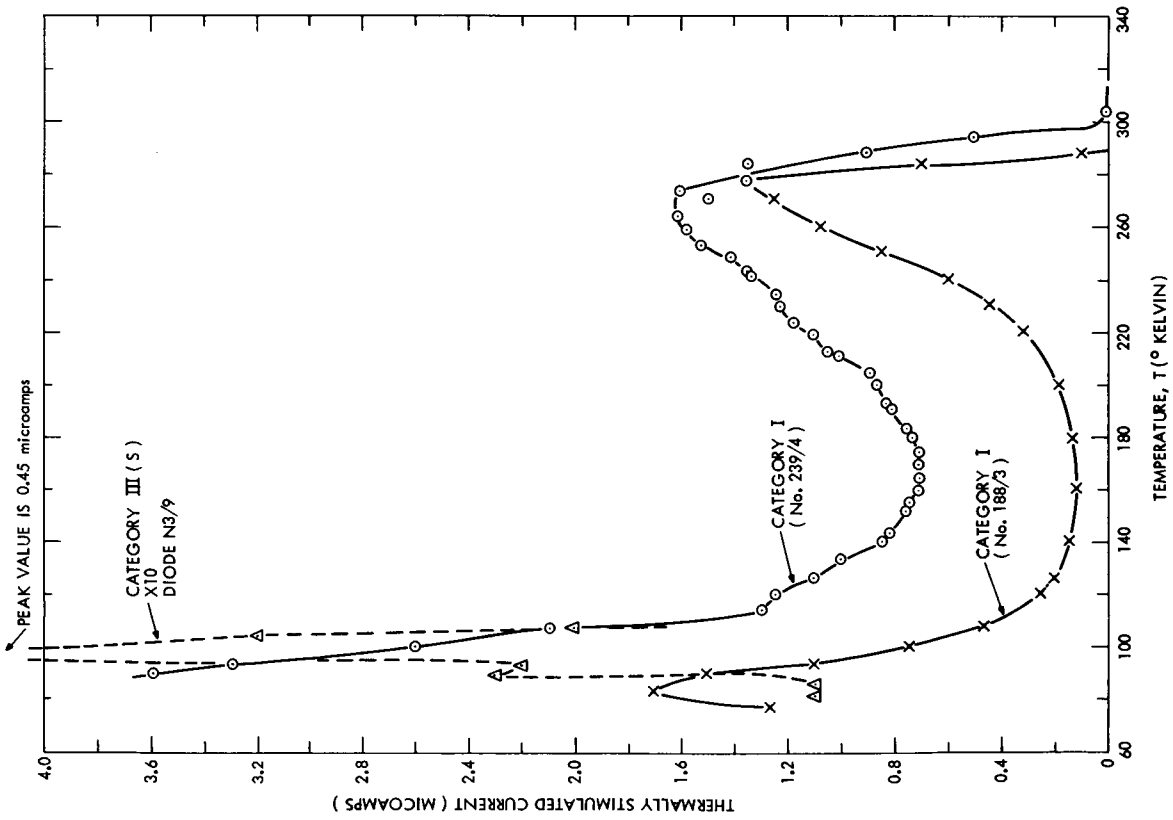


Fig. 7 Temperature Variation of Thermally Stimulated Current ($i_S - i_D$)

will be found at D, corresponding to a temperature T_m . If, however, the optical excitation only shifts the Fermi-level from A to a point E, no peak current is observed at temperature T_m .

In films having diffused sulfur (Category IIIS) there is a pronounced peak at 90°K , corresponding to 0.14 eV below the conduction band. This result is consistent with that of Kulp and Kelley, who find that interstitial sulfur contributes to an edge emission center 0.14 eV below the conduction band. These diodes had very small dark currents, and it was observed that the light current, i_s , increased steeply when approaching the peak value, i_{sm} .

The predominance of the 0.33 eV level is clearly seen in the example given in Figs. 9 and 10.

F. ENERGY DENSITY OF DEFECT STATES

The total energy density of levels within the forbidden band, N_T , per unit volume of the CdS film was obtained from the integral of the thermally stimulated current ($i_s - i_D$) over the measured temperature range. Thus

$$N_T = \int N_T(E) dE = \int \frac{(i_s - i_D)}{q\beta V'} dT \quad (2.6)$$

in which $N_T(E)dE$ = density of levels of energies within (E, E + dE)
 V' = volume of CdS film
 β = constant rate of temperature increase

Measurements of ($i_s - i_D$) as in Figs. 7 or 10 give total energy densities of the order of 10^{22} per cm^3 . From a Fermi-level analysis, it was concluded that only a total energy density, rather than an energy distribution could be meaningfully obtained. The anomalously high value for the energy density should be reduced in proportion to the photoconductive gain, if the large thermally stimulated current is the result of electrons circulating through the film more than once before undergoing recombination. An alternative explanation that removal of holes produces a negative space charge in the vicinity of the blocking contact, thereby effectively reducing the barrier height and increasing the thermally stimulated current, is also possible.

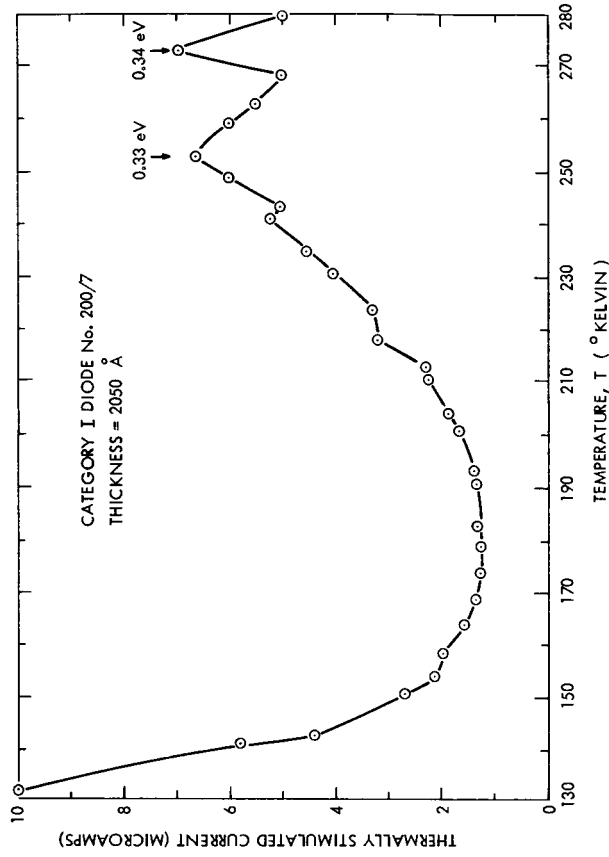


Fig. 9 Dark Current Variation with Temperature for a 2000 Å Au-CdS-Au Diode

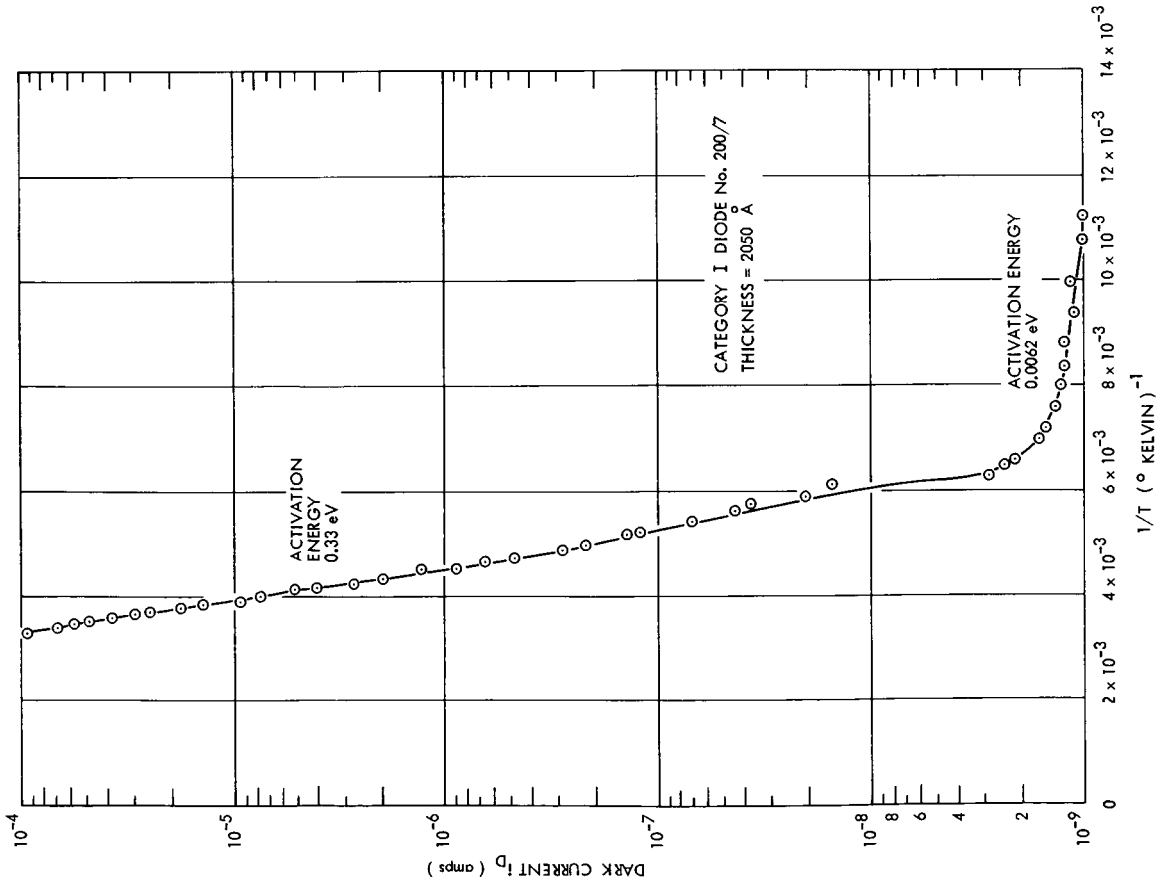


Fig. 10 Temperature Variation of Thermally Stimulated Current ($i_S - i_D$)

CHAPTER III

MEASUREMENTS OF DIFFUSION VOLTAGE, BARRIER WIDTH AND IMMOBILE ION DENSITY

The electronic conduction behavior of evaporated thin CdS films is greatly influenced by the nature of the electrical contacts, which may form ohmic (electron injecting) or blocking junctions to the CdS films. The electron energy profile of the blocking junction between metal and CdS films was determined for our films by measuring the diffusion voltage, ϕ_o , the junction or barrier width, l_o , and the immobile ion density, N_D . These quantities were, in turn, derived from measurements of the variation of the incremental capacitance of the junction with applied bias voltage.²⁵ Measurements of the capacitance~temperature variation were also made for our films. The nature of the contact between evaporated gold films, ranging in thickness from 400 Å to 1000 Å, and evaporated CdS films, ranging from 3400 Å to 5000 Å, was investigated for gold-CdS-gold and indium-CdS-gold diodes. The blocking contact for these diodes was formed, in all cases, in the region of the gold electrode evaporated over the CdS film. The electrode evaporated directly onto the substrate before the CdS evaporation always behaved as an injecting (or much less blocking) electrode. The three categories of diode referred to in the preceding chapters were investigated. As previously explained, the differences between these categories are essentially differences in the post-evaporative treatment of the CdS film either before or after deposition of the second electrode.

A. EXPERIMENTAL

Incremental capacitance measurements were made using a General Radio 1650A impedance bridge, having a signal frequency of 1 kc/s. The maximum signal applied to any diode was limited to 5 mV peak-to-peak, so that negligible error was introduced by the nonlinearity of the current vs. voltage characteristic of the diode. The small signal equivalent circuit was the combination of a variable junction resistance, R_p , in parallel with a variable junction capacitance, C_p , both in series with the bulk CdS film and lead

resistance, R_s . Simultaneous measurements were taken of C'_p and the dissipation factor, D , defined by

$$D = 1/\omega R'_p C'_p \quad (3.1)$$

where R'_p and C'_p are the resistance and capacitance of an equivalent parallel two-element circuit across the bridge measuring terminals. For the diodes investigated, $R'_p = R_p$ and $C'_p = C_p$ with negligible error. Immediately following each measurement of C_p and D_p with an applied bias voltage, corresponding measurements of C_{po} and D_o were made, where C_{po} and D_o are the values of C_p and D with no applied bias voltage. A restriction in the range of bias voltages had to be made so that the dissipation factor D remained under 20; above this value it was found impossible to obtain a unique bridge null. To assist in obtaining an accurate null, the bridge output was displayed on an oscilloscope.

All measurements were taken with the diodes stored in darkness for a sufficiently long time for the values of C_{po} and D_o to reach equilibrium. This time was generally of the order of 15 to 30 minutes at room temperature. At 77°K consistent values were obtained only after several cyclings of the measurement of capacitance vs. applied voltage.

The variation of incremental capacitance with voltage was measured both at room temperature and at liquid nitrogen temperature. The temperature dependence of incremental capacitance was also obtained for a Category IIIS (sulfur diffused) diode. The frequency dependence of capacitance was measured by Ebner²⁶ for diodes evaporated under conditions similar to those of Category I diodes.

B. CAPACITANCE VARIATIONS WITH APPLIED VOLTAGE

The following variations of capacitance with applied voltage were observed for the several categories of diode.

1. Category I Diodes

The variation of $1/C^2$ with applied voltage at 300°K was extremely rapid, and was linear over a very small bias voltage range (50 to 100 mV), as shown in Figs. 11 and 12. For forward bias values, the $1/C^2$ variation tends asymptotically towards a constant value. However, this occurred for forward bias voltages where the dissipation factor was high and only a lower bound on the constant capacitance value could be obtained. In the reverse bias region (electrode 1 positive) at 300°K , there was concavity downward of the $1/C^2$ vs. V curve which resulted either in a constant $1/C^2$ value or even in a turning-over of the curve for reverse bias voltages greater than 120 mV.

At a lower temperature (240°K), the $1/C^2$ vs. V variation shown in Fig. 13, becomes linear over a 300 mV range and the concavity downward now extends into the forward bias region. It is not known whether the asymptotic tendency of the curve for forward bias voltages at 300°K would still be found. At the lower temperature, C_{po} is smaller and the slope $d(1/C^2)/dV$ is less, both of which give a higher forward voltage intercept of the $1/C^2$ curve.

2. Category II Diodes

At room temperature, the $1/C^2$ vs. V curve has a linear relationship up to 0.9 volts reverse bias and to 0.4 volts forward bias (Fig. 13). Near the zero bias point there is, however, a slight tendency to concavity downwards. There is no evidence of any tendency towards a constant $1/C^2$ value with increasing forward bias. At liquid nitrogen temperature (Fig. 14) there is a leveling off at a constant value of $1/C^2$ equal to 9×10^{17} farads⁻². For reverse bias up to 0.9 volts, the curve is quite linear.

Before capacitance readings were taken for the Category II diode, the diode was stored in darkness for several hours. Applying a reverse bias voltage increased the zero-bias capacitance, C_{po} . With repeated excursions of the reverse bias to the maximum used, the value of C_{po} increased with each excursion but by smaller increments, finally reaching a steady value after four excursions. At this stage a repeatable variation of incremental capacitance with both reverse and forward bias could be obtained.

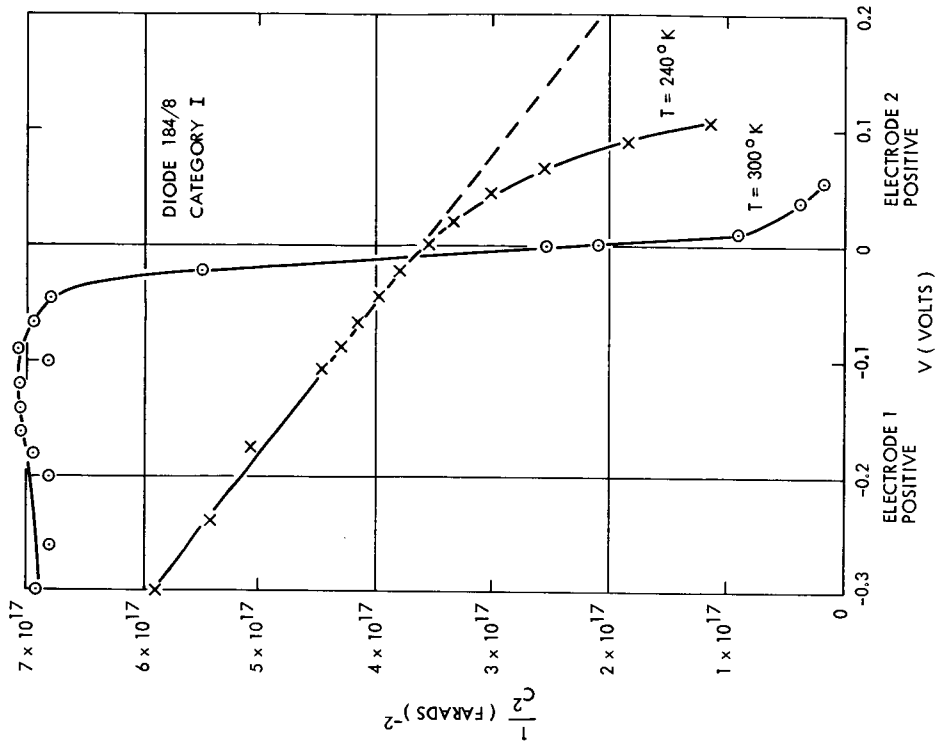


Fig. 12 Variation of $1/C^2$ with Voltage for a Category I Diode at 240°K and at 300°K

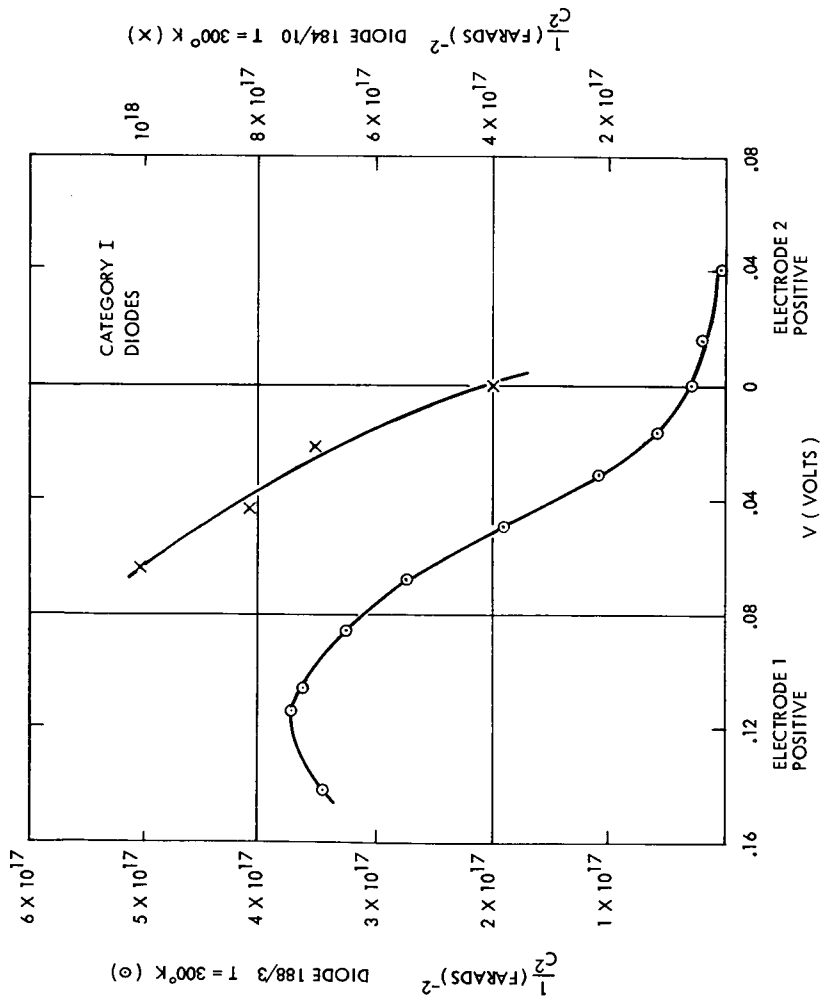


Fig. 11 Variation of $1/C^2$ with Voltage for Category I Diode at 300°K

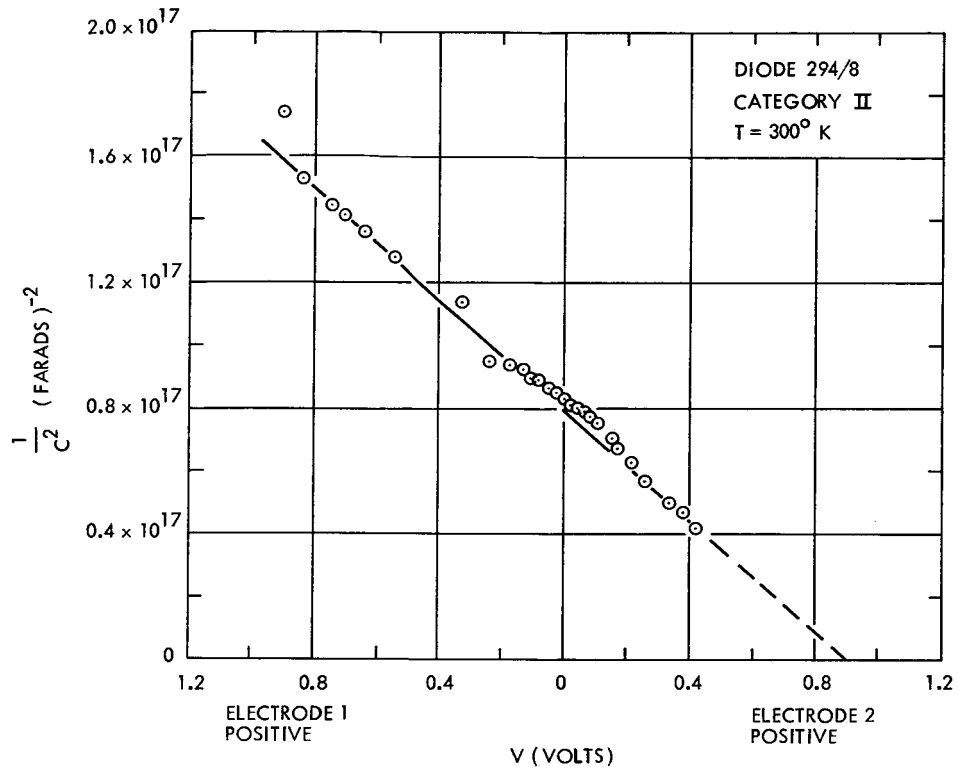


Fig. 13 Variation of $1/C^2$ with Voltage for a Category II Diode at 300°K

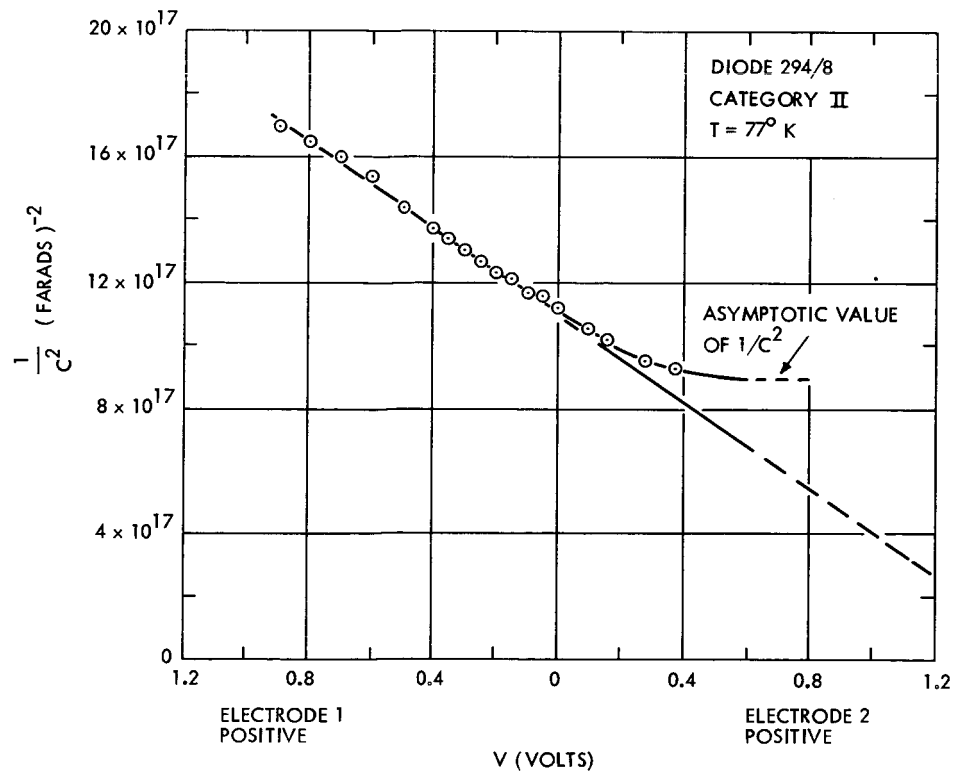


Fig. 14 Variation of $1/C^2$ with Voltage for a Category II Diode at 77°K

3. Category III Diodes

At room temperature, the $1/C^2$ vs. V curve has a linear relationship from zero bias to 0.4 volts reverse bias (Fig. 15). For

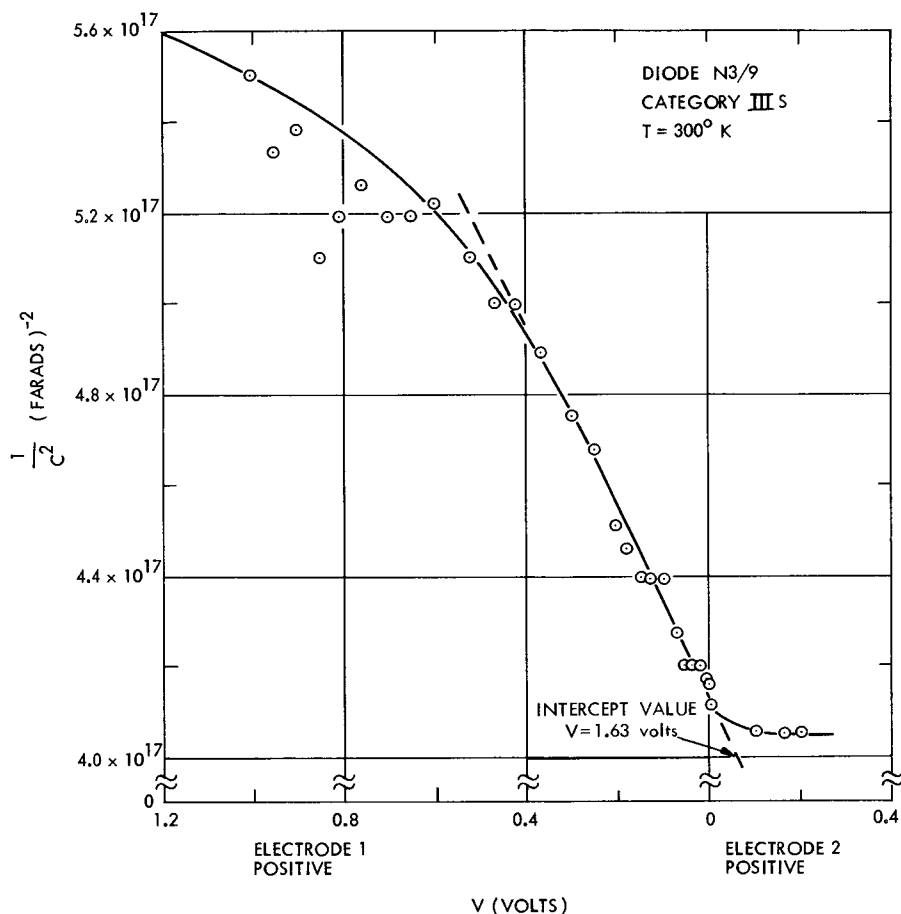


Fig. 15 Variation of $1/C^2$ with Voltage for a Category III Diode at 300°K

reverse bias voltages greater than 0.4 volts, there is concavity downwards. In the forward direction there is a rapid transition to a constant capacitance value. The intercept value of the linear part of the curve with the voltage axis is typically 1.6 volts.

C. CAPACITANCE VARIATION WITH TEMPERATURE

Measurements of capacitance with zero applied bias voltage have shown that capacitance increases with increasing temperature, by approximately a factor of 4 over the range 77°K to 350°K. Measurements have been made by Cooper²⁷ for Category I diodes of the form In - CdS - Au, which have shown a capacitance~temperature variation

of gradually increasing slope, typically capacitance being proportional to $T^{2.5}$.

The variation for a typical Category IIIS diffused sulfur diode showed three linear regions (Fig. 16):

$$\begin{aligned} C &= 0.5 + (2.14 \times 10^{-3})T \text{ nanofarads,} \\ &\text{for } T = 77^\circ\text{K to } 170^\circ\text{K} \\ C &= 0.05 + (4.8 \times 10^{-3})T \text{ nanofarads,} \\ &\text{for } T = 170^\circ\text{K to } 210^\circ\text{K} \\ C &= -1.35 + (1.14 \times 10^{-2})T \text{ nanofarads} \\ &\text{for } T = 210^\circ\text{K to } 360^\circ\text{K} \end{aligned} \tag{3.2}$$

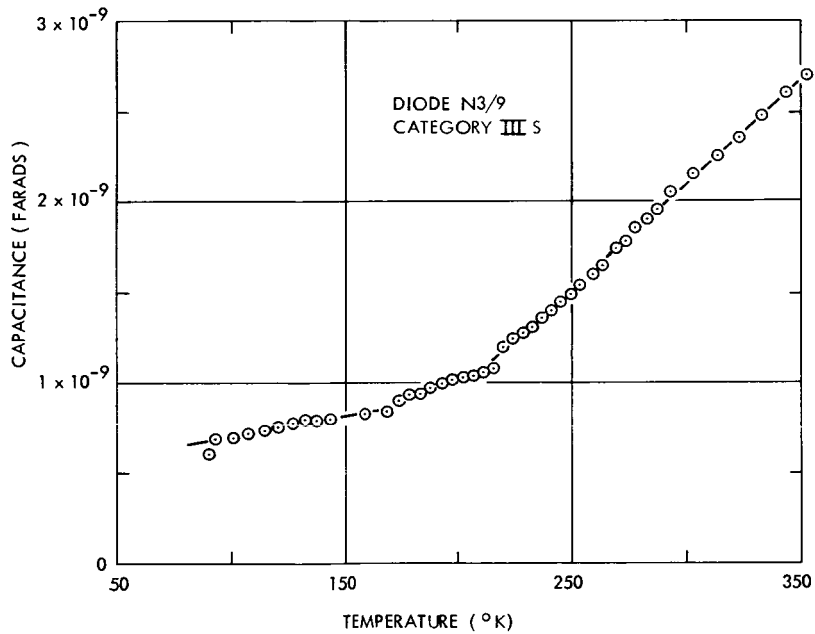
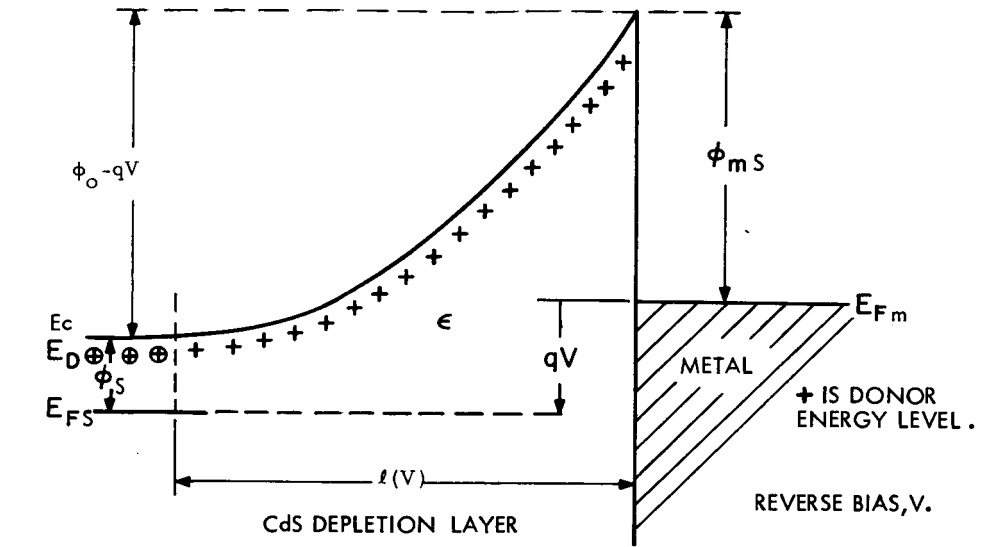


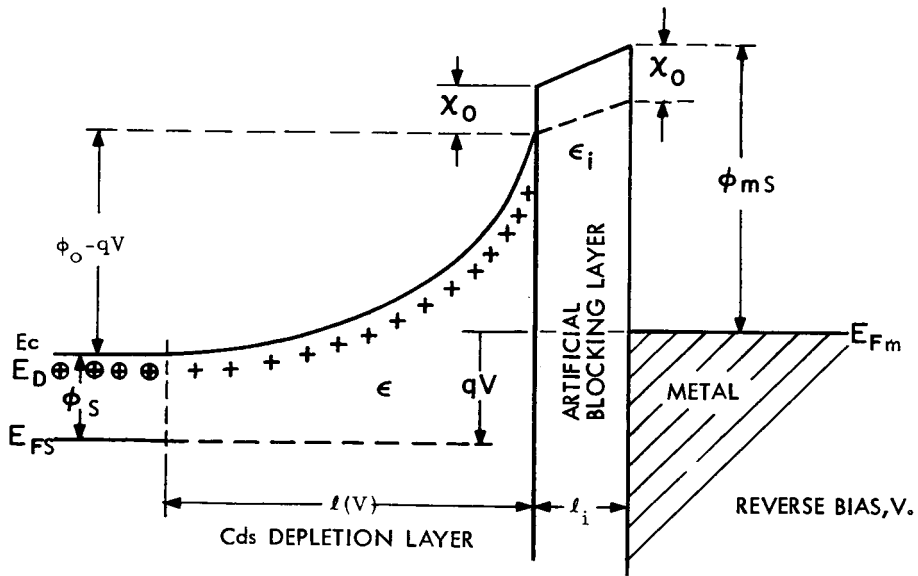
Fig. 16 Variation of Capacitance with Temperature for a Category III Diode

D. DIFFUSION VOLTAGE, BARRIER WIDTH AND IMMOBILE ION DENSITY

From the results it is obvious that the idealized models of either a Schottky barrier or one including an artificial blocking layer can, at most, apply over a very limited range of applied bias near the zero bias condition. To establish the definitions of diffusion voltage, ϕ_0 , barrier width $l(V)$, and donor or immobile ion density, N_D , Figs. 17a



a) Schottky Barrier



b) Including Artificial Blocking Layer

Fig. 17 Electron Energies at Blocking Contact

and 17b show the basic Schottky barrier for both the abrupt metal-CdS film junction and as modified by the presence of an artificial blocking layer. For an abrupt junction in which there is a constant donor density profile within the CdS film, the variation of $1/C^2$ with applied voltage is a straight line intersecting the voltage axis at ϕ_o . The donor or immobile ion density is given by

$$N_D = \frac{-2}{qA^2\epsilon} \left[\frac{d\left(\frac{1}{C^2}\right)}{dV} \right]^{-1} \quad (3.3)$$

in which N_D = donor or immobile ion density, (m^{-3})
 A = diode area = $10^{-6} m^2$
 ϵ = dielectric constant of CdS film = $10^{-10} f/m$
 q = electronic charge = 1.6×10^{-19} coulombs
 V = applied voltage across the barrier, (volts)

The barrier width for no applied bias voltage is given by

$$l_o = \frac{\epsilon A}{C_o} \quad (3.4)$$

in which C_o is the incremental capacitance for no applied bias.

For an artificial barrier layer diode,^{28,29} the barrier width, l_b , measured as $l_b = \epsilon A/C_o$, is given in terms of the CdS depletion layer width, l_o , and the artificial blocking layer width, l_i , as

$$l_b^2 = l_o^2 + l_i^2 \quad (3.5)$$

The intersection of the $1/C^2$ vs. V curve with the voltage axis is then V_o , from which ϕ_o is obtained as

$$\phi_o = V_o - \left(\frac{N_D q \epsilon l_i^2}{2\epsilon_i^2} \right) - \left(\frac{2N_D q \epsilon l_i^2}{\epsilon_i^2} \right)^{1/2} \quad (3.6)$$

where ϵ = dielectric constant of CdS film = $10^{-10} f/m$
 ϵ_i = dielectric constant of artificial blocking layer
 = $4 \times 10^{-10} f/m$, in the case of sulfur
 l_i = width of artificial blocking layer, (m)

Based on Eqs. 3.3 and 3.4, Table 4 gives the values ϕ_o (uncorrected for the presence of an artificial blocking, or insulating, layer*), l_o , and N_D .

Table 4

Barrier Measurements

Diode Number and Category	CdS film Thickness (Angstroms)	Temperature ($^{\circ}$ K)	Diffusion Voltage ϕ_o (eV)	Barrier Width l_o (Angstroms)	Immobile Ion Density N_D (cm^{-3})
184/8, I	3,400	240	0.47	595	2×10^{17}
184/8, I	3,400	300	0.02	430	10^{16}
294/8, II	4,800	77	1.56	1000	2×10^{17}
294/8, II	4,800	300	0.90	290	10^{18}
N3/9, IIS	4,800	77	--	1500	--
N3/9, IIS	4,800	300	1.63	630	5×10^{17}

E. INTERPRETATION OF BARRIER MEASUREMENTS

The first question to arise is whether diffusion or diode theory holds for the gold-CdS junction. Since the mean free path is at least of the order of the barrier thickness obtained from capacitance measurements, diode theory is assumed to hold.²⁸ More exactly, the mean free path is at least of the order of the distance within which the potential near the top of the barrier changes by kT . In fact, from the high values of thermally stimulated emission currents, we have reason to believe that the electrons circulate more than once through the film before recombining. Secondly, the extrinsic Debye length is less than the barrier width:

$$L_D = \left[\frac{\epsilon(kT/q)}{2qN_D} \right]^{1/2} \quad \text{meters} \quad (3.7)$$

* For diodes having an insulating layer, this quantity is V_o .

where L_D = extrinsic Debye length
 ϵ = CdS dielectric constant $\approx 10^{-10}$ farads/meter
 N_D = donor density $\approx 10^{23}$ meters⁻³

It follows that

$$L_D \approx 125 \text{ \AA}$$

The interpretation of capacitance vs. voltage variation in terms of a variable barrier width and uniform donor density is therefore considered meaningful, at least for small applied voltages.

From the value for donor density, N_D , of the order of 10^{17} centers per cm³, it is possible that there are lateral variations of barrier height or "Schottky passes" in the CdS film in the vicinity of the depletion layer. These are the result of a discontinuous space charge, the barrier thickness being only two or three times the average distance between donor centers.

There is considerable evidence that the difference between our various categories of diode is one of degree only. It is suggested that the effect on the CdS film of heat treatment, diffusion of evaporated sulfur, or oxygen ion bombardment is to form, adjacent to the blocking electrode, a diffused layer of lower n-type conductivity than exists in the bulk of the CdS film. It is well known that polycrystalline evaporated films of CdS exhibit n-type extrinsic conduction attributed to sulfur vacancies. For those Category I diodes which were subjected to heat treatment after the deposition of the top electrode (electrode 2), it is likely that diffusion of some of the electrode material into the CdS film occurs. There is also the possibility of the subsequent diffusion of atoms of the residual atmosphere in the vacuum system at 10^{-5} torr which were absorbed in the surface of the CdS film before evaporation of electrode 2. Furthermore, it is possible that a very thin p-type layer will form from acceptors of the electrode 2 material. This could account for the low intercept values for ϕ_0 .

Category II diodes had higher resistivity than those in Category I, because more extensive diffusion of the vacuum-system residual atmosphere had taken place; the surface of the CdS film was exposed to a higher temperature for a longer time. A relatively donor-free region is indicated by the tendency of the $1/C^2$ vs. V curve towards a constant value for forward-bias voltages (Fig. 14). In addition, the apparent high value for ϕ_0 can be attributed to the presence of an artificial blocking layer.

It is significant that the behavior of diodes in Categories II and III is similar, and, in fact, diodes in Category III seem to be identical, regardless of whether an evaporated layer of sulfur or an oxygen glow discharge treatment was used. For IIS diodes, having a diffused layer of evaporated sulfur, there is almost certainly a residual insulating layer of sulfur. If the correction of Eq. 3.6 is applied, it can be shown that a corrected diffusion voltage, ϕ_0 , of 0.59 eV is obtained by assuming the presence of an insulating layer of 35 Å of sulfur. This seems a reasonable thickness since a calculated upper bound on the thickness of the sulfur layers evaporated is 100 Å. In this case the uncorrected diffusion voltage, V_0 , is 1.63 eV and the barrier width, l_0 , is 640 Å.

F. EFFECT OF DEFECT STATES

The voltage dependency of capacitance is considered mainly due to donor levels lying in the vicinity of 0.06 eV below the conduction band in the CdS film. The energy density is of the order of 10^{16} to 10^{18} centers per cm^3 of film.

It is likely that the presence of a high density trapping level region near 0.35 eV below the conduction band is believed responsible for (a) the increase in C_{po} at 77°K, (b) the concavity downwards of most $1/C^2$ vs. voltage curves for reverse voltages, (c) the increase in C_{po} with temperature.

When measurements of capacitance, C_p , were repeated with reverse bias voltage, we found that the zero bias capacitance, C_{po} , increased with each measurement of C_p , eventually reaching a steady value after several excursions to the maximum reverse bias voltage.

This behavior is consistent with the filling-up in the barrier region of trapping levels which are below the Fermi-level throughout most of the CdS film, except very close to the blocking junction. Such levels could be in the vicinity of 0.35 eV, as obtained from conductivity measurements. The filling of these levels with electrons would result in space charge neutralization in the barrier region, implying a decrease in barrier thickness, that is, an increase in C_{po} .

Concavity downwards of the $1/C^2 \sim V$ variation found for most of our diodes can be explained either from trapping level effects as given by Goodman²⁹ or by a linear variation of the ion density which increases with distance from the metal into the barrier region of the CdS film, such as can arise from acceptors diffused into the film.

The capacitance ~ temperature variation has been shown by Cooper²⁷ to agree with a charge density decreasing exponentially with distance from the barrier into the reserve region. This has been explained by considering a Fermi distribution instead of a Boltzmann distribution of trapping levels in the reserve region.

CHAPTER IV

CONDUCTIVITY VARIATION WITH APPLIED VOLTAGE

This chapter is a descriptive account of the current vs. voltage characteristics of gold-CdS-gold and gold-CdS-silver diodes which were fabricated by the methods given in the introductory chapter. The conduction through the CdS film is, therefore, normal to the plane of the film. Current vs. voltage characteristic curves were obtained both for steady values over several orders of magnitude of current, and also at 60 c/s over a single order of magnitude of current. The change in barrier height (or diffusion voltage) with temperature described in Chapter III is related to a corresponding change in the forward conduction region of the characteristic curve.

As a measure of the diode forward conduction properties, we define a forward transition voltage, V_F , as the voltage where there is a transition from linear to nonlinear behavior of the $i \sim V$ characteristic curve.

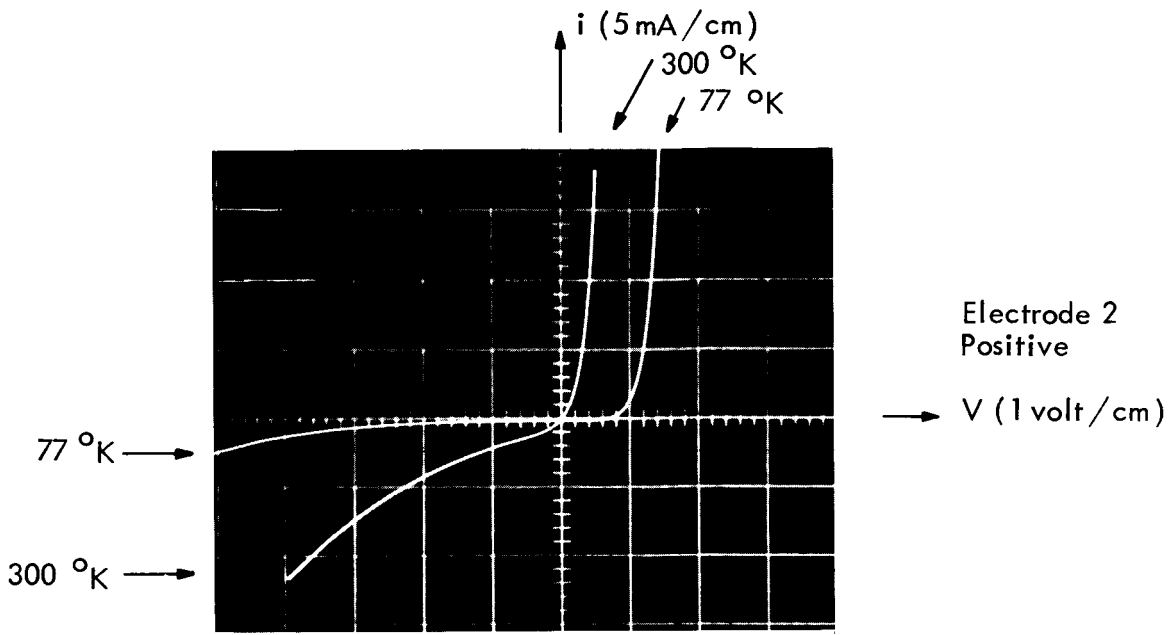
All measurements were made using a four-point probe method in which one end of each of the electrodes 1 and 2 (Fig. 1) was used as a current contact and the opposite end of each was used as a voltage measuring contact. The cross-sectional area of the diodes was 10^{-2} cm^2 .

We also include in this chapter measurements of conduction in the plane of the CdS film which were made between electrodes both on the substrate side of the film.

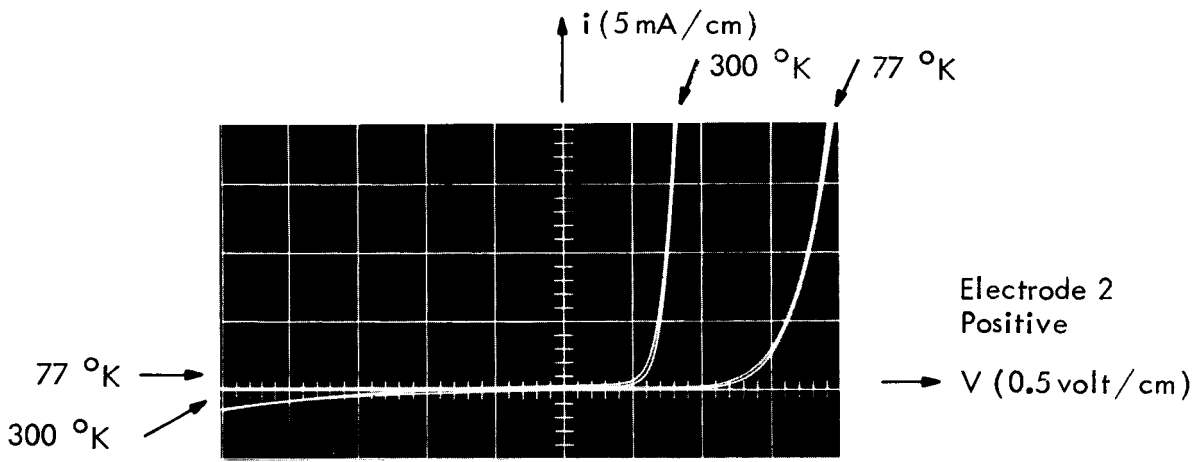
A. CURRENT VS. VOLTAGE CHARACTERISTIC CURVES AT 60 c/s

The basic features of 60 c/s diode characteristics are shown in the oscilloscope traces of Fig. 18.

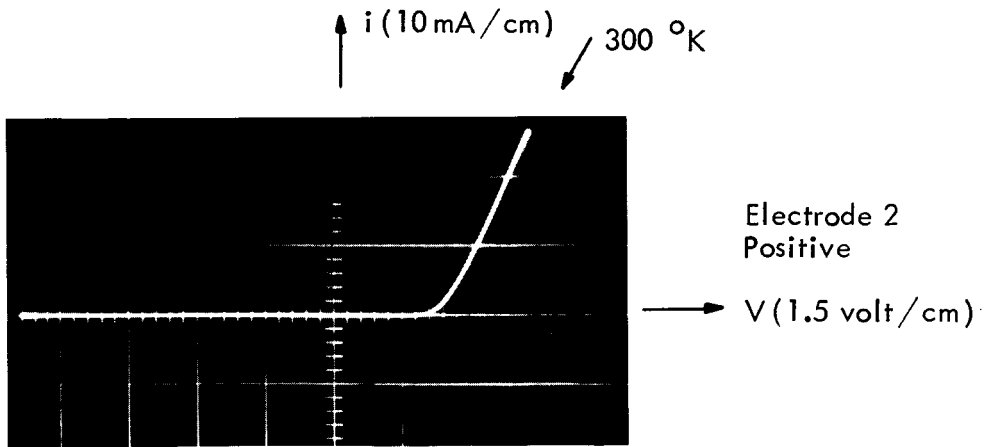
Diodes in Category I have steep forward conduction properties: the current for a forward bias of 0.5 volts is $\approx 50 \text{ ma}$. The transition voltage, V_F , increases from ≤ 0.2 volts at room temperature to 0.7 volts at 77°K . However, for reverse voltages with electrode 2 negative, the characteristic shows considerable leakage currents at room temperature, typically 0.5 ma at 2 volts. The reverse characteristic is markedly light sensitive as well as temperature sensitive.



a) Category I Diode



b) Category II Diode



c) Category III S Diode

Fig. 18 60 c/s Current vs. Voltage Characteristics

Figure 18a shows the 60 c/s characteristics for a typical diode in Category I, both at room temperature and at 77°K.

Diodes in Category II have much smaller reverse leakage currents and exhibit the space-charge-limited characteristic of sliding along the voltage axis in the forward direction as observed by Smith and Rose.³⁰ In addition, V_F is higher, varying between 0.7 volts at room temperature and 2.2 volts at 77°K. The reverse direction is less light and temperature sensitive than for diodes in Category I. Figure 18b shows the 60 c/s characteristics for a typical diode at room temperature and at 77°K.

Category III diodes, both oxygen ion bombarded and sulfur diffused, exhibit high reverse breakdown voltages -- typically 8.5 volts or greater at room temperature -- and are space-charge-limited with a V^2 dependence over a limited part of the forward direction. V_F , the transition voltage from linear to V^2 behavior in these diodes, is typically 1.5 to 2.5 volts. In addition the SCL behavior of the characteristic sliding along the voltage axis with increasing amplitude of the applied 60 c/s voltage is observed. A room temperature characteristic is shown in Fig. 18c.

Figure 19 shows the comparative median characteristics of diodes in the three categories.

The films of Fig. 18 (a, b, c) were taken using the 4-point probe method, one pair of diode electrodes being current supply points, the other pair being voltage measuring points.

B. CURRENT VS. VOLTAGE CHARACTERISTIC CURVES IN THE STEADY STATE

At 77°K, Category I diodes (Fig. 20) display an ohmic variation in the forward direction for voltages less than 250 mV; between 250 mV and 500 mV the behavior is exponential, of the form

$$i = i_o \exp\{qV/akT\} \quad (4.1)$$

in which $a \cong 5$. Above 500 mV the dependence indicates limiting by conduction in the CdS rather than by the barrier. In the reverse direction, the dependence is

$$i \sim (-V)^{1/4} \quad (4.2)$$

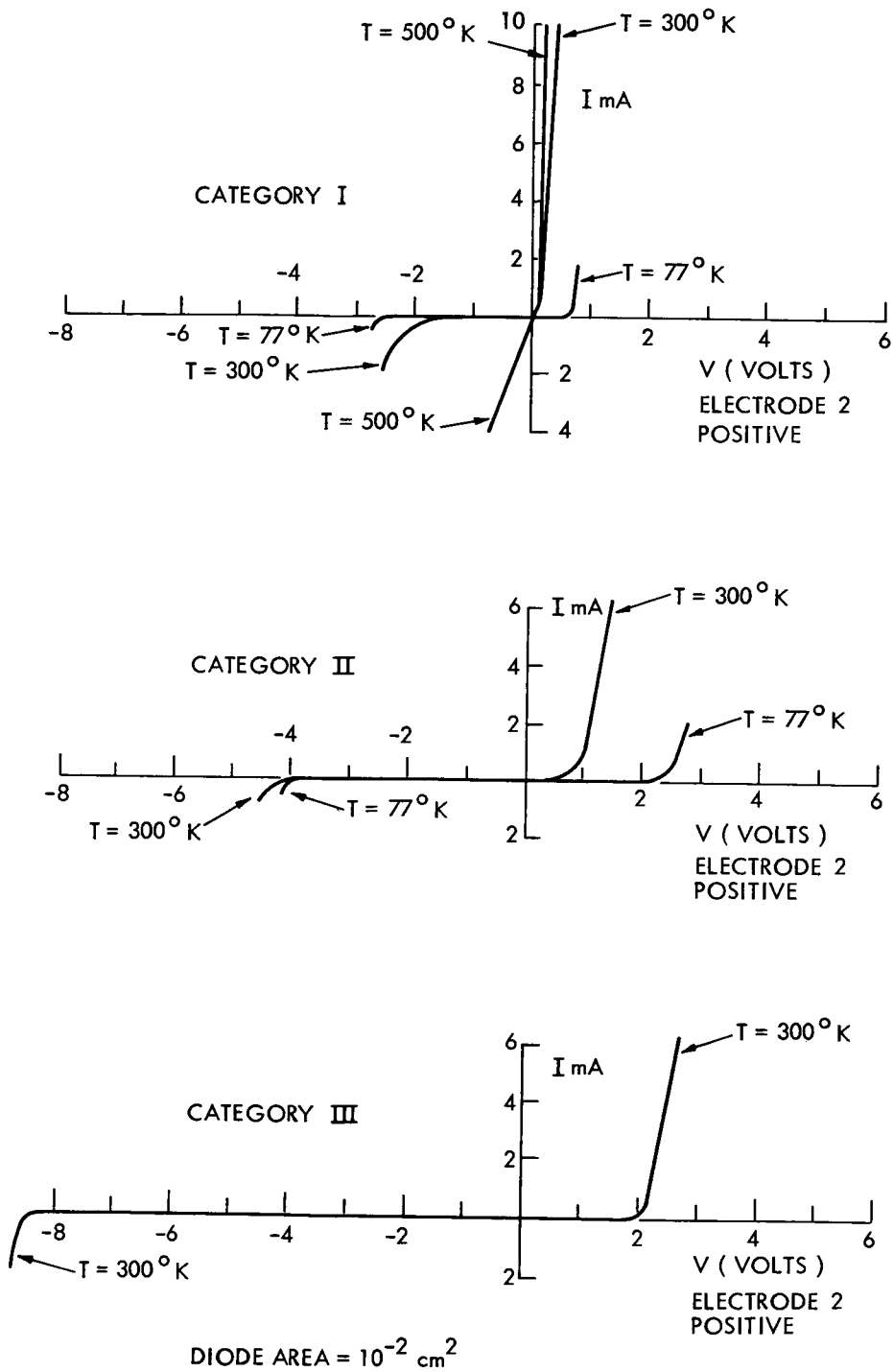


Fig. 19 60 c/s Current vs. Voltage Characteristics

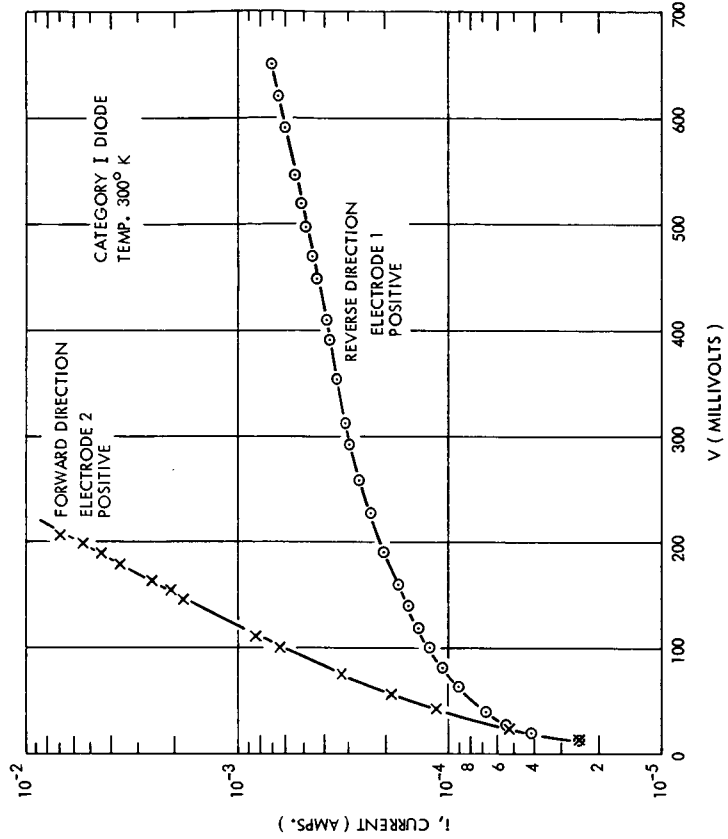


Fig. 21 Current vs. Voltage, Category I Diode, T = 300°K

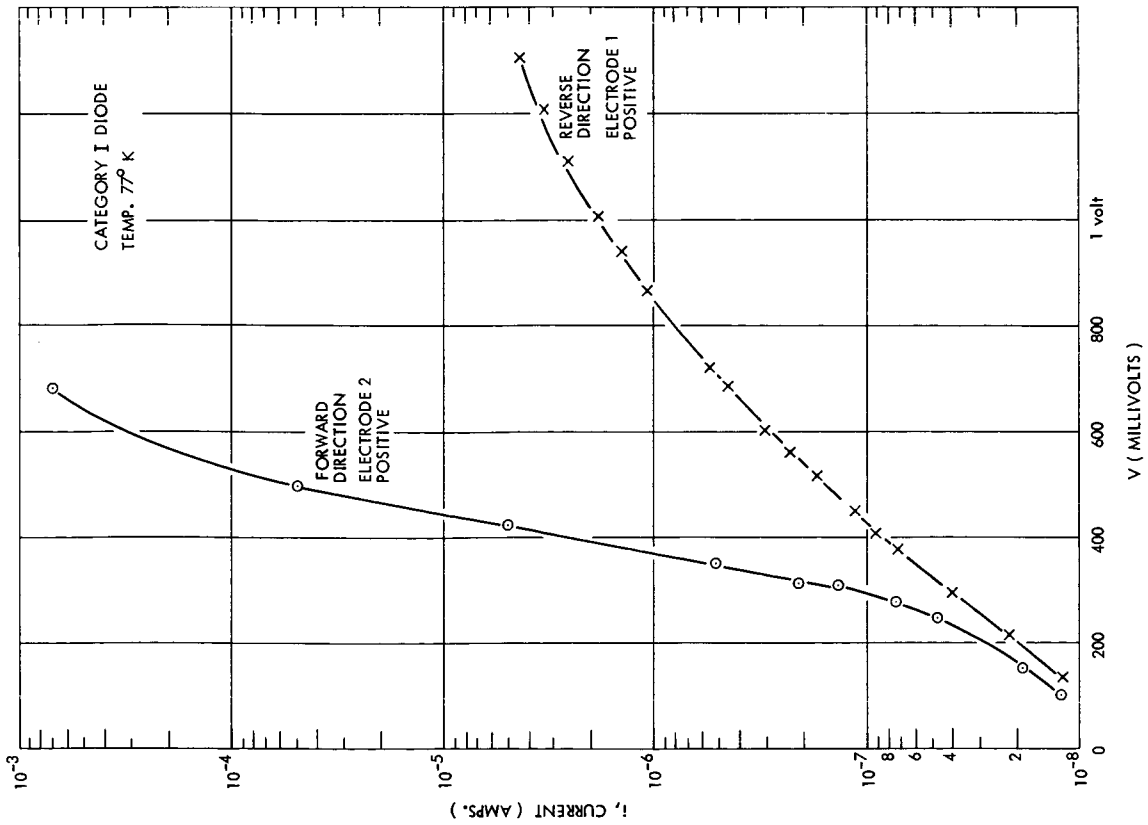


Fig. 20 Current vs. Voltage, Category I Diode, T = 77°K

At 300°K, for Category I diodes (Fig. 21) the transition voltage, V_F , is 100 mV. The current values are two or three orders of magnitude greater than those at 77°K. Above 100 mV in the forward direction, the behavior has been shown to be exponential to at least 300 mV, with an a factor of 2. The reverse direction characteristic shows $(-V)^{1/4}$ dependence for voltages above 700 mV.

No steady state measurements were obtained for a Category II diode.

Figures 22, 23 and 24 show the room temperature characteristics for a Category IIIS (Sulfur diffused) diode. The forward characteristic has a V^2 dependence in the vicinity of 0.5 to 1.0 volt, as in Fig. 25. It becomes purely exponential above 2 volts, again being of the form

$$i = i_0 \exp [qV/akT] \quad (4.3)$$

in which $a = 7.6$. The reverse characteristic of the IIIS diode at 300°K is also exponential between 1 volt and 8 volts, as in Fig. 24.

Figure 26 shows the $(-V)^{1/4}$ behavior found for most diodes in the reverse direction.

C. BEHAVIOR OF DIODES UNDER ILLUMINATION

Under white light illumination, the forward conduction behavior of Category I diodes has been observed to obey the V^3 relationship observed by Muller and Zuleeg.³¹ The voltage range over which this occurs, however, was somewhat limited, between 100 mV and 400 mV. The reverse direction characteristic was markedly light sensitive.

We observed that Category III diodes exhibited a hysteresis effect at 60 c/s over the forward biased region under white light illumination. This may be attributed to an injected space-charge-limited current.

D. CONDUCTION IN THE PLANE OF THE CdS FILM

Although a so-called "bulk resistivity" of CdS films is sometimes derived from the measurement of current and voltage in the low-voltage, linear region of conduction, most of the voltage drop occurs

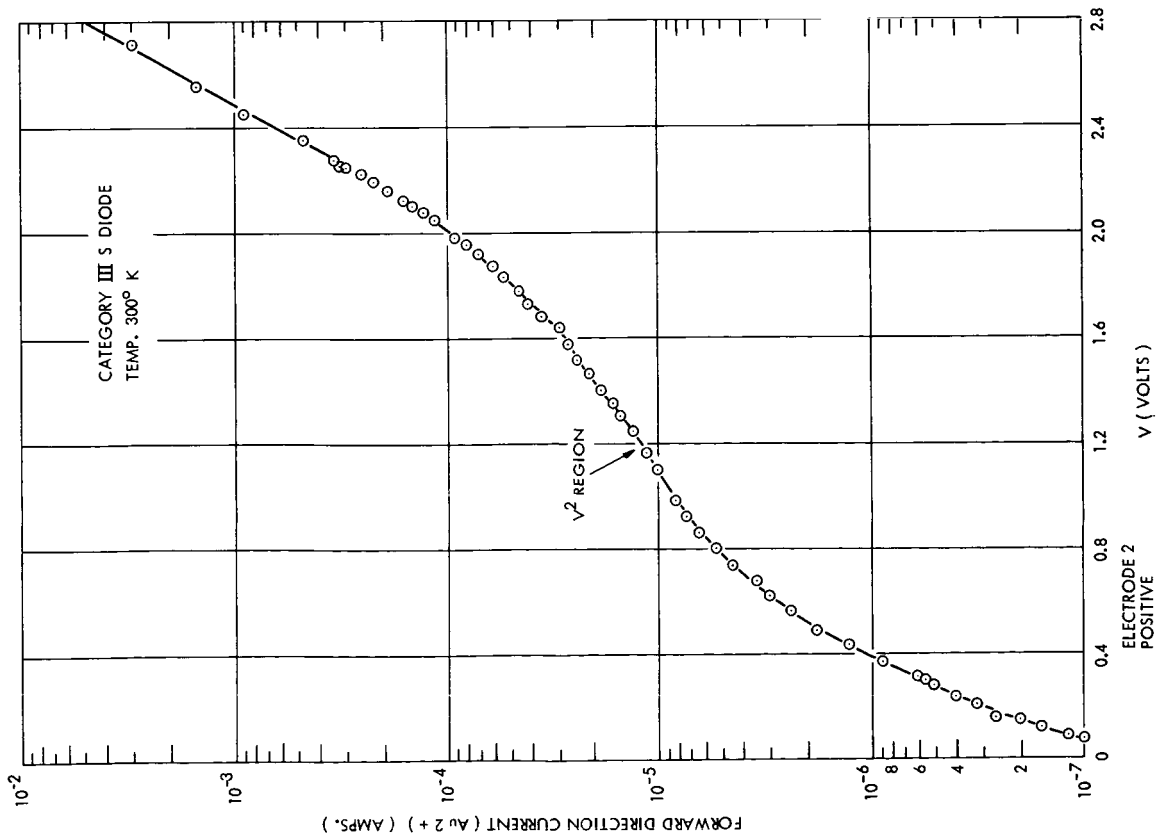


Fig. 22 Current vs. Forward Voltage, Category III(s) Diode, T = 300°K

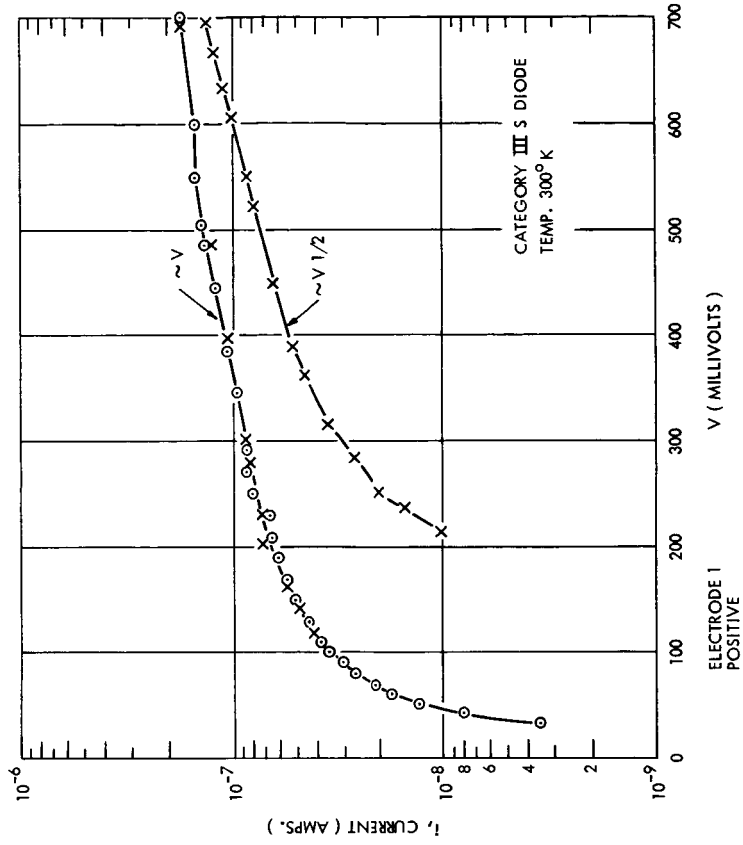


Fig. 23 Current vs. Reverse Voltage, Category III(s) Diode, T = 300°K

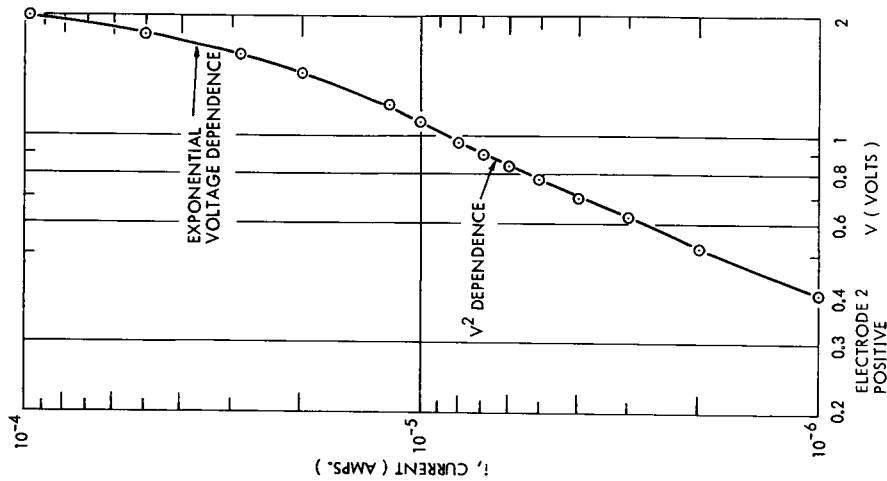


Fig. 25 V^2 Dependence of Forward Current vs. Voltage, Category III(s) Diode, $T = 300^\circ K$

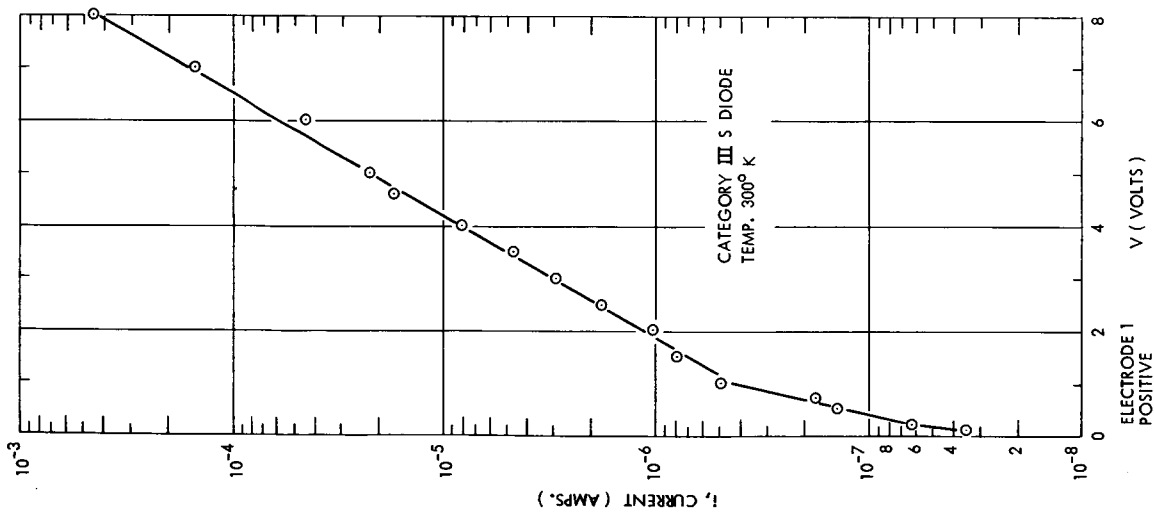


Fig. 24 Current vs. Forward Voltage above 1 Volt, Category III(s) Diode, $T = 300^\circ K$

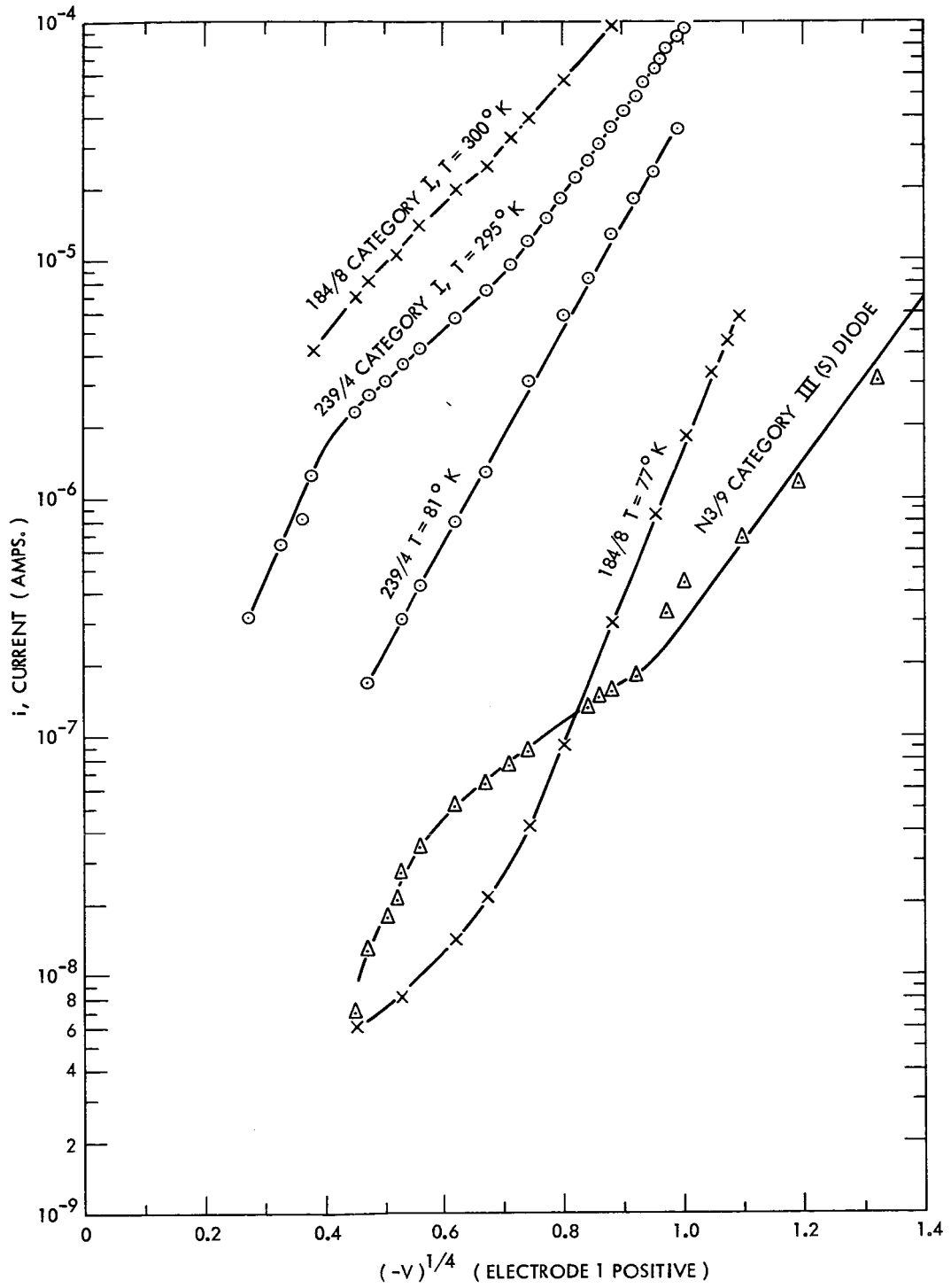


Fig. 26 Fourth Root Variation of Diode Characteristics

across the barrier region (see Appendix A). Even for "surface resistivity" measured with electrodes on the same side of the CdS film, difficulties were encountered where a layer of resistivity, different from the CdS film, formed over the film. This is especially true for diodes in Categories II and III which were subjected to the special surface treatments as defined. For these reasons we derived the resistivity of the CdS film outside the depletion region from injecting electrodes both on the substrate side of the film. The resistivity of the films obtained in this way was of the order of 10^3 to 10^5 cm. This gives a resistance value normal to the film in the range 50Ω to 100Ω , in agreement with the value derived by Ebner²⁶ from impedance measurements at high frequency.

E. OBSERVATIONS OF MORE THAN ONE MODE OF CONDUCTION

The following observations were made on Au-CdS-Au and Au-CdS-Ag diodes under the application of 60 c/s voltages whose peak values were beyond the reverse-breakdown voltages.

- (a) A current-controlled negative resistance was found for many diodes. This is considered in detail in Chapter VI.
- (b) Transition to purely ohmic conduction from a nonlinear characteristic occurred, giving the appearance of a short-circuit between the electrodes. The resistance between the electrodes, however, remained at 40 to 100Ω , consistent with the "bulk" CdS film resistance.
- (c) The nonlinear characteristic could in all cases be regained from the ohmic conduction state in (b), by switching off the 60 c/s signal and then re-applying it with a peak value slightly less than the breakdown value. The presence of a transient signal value greater than the breakdown value on re-applying the signal is highly probable, but whether it was necessary is not known. The nonlinear characteristic which was regained did not in all cases exhibit as large a reverse breakdown voltage value as it had before transition to ohmic behavior.
- (d) A series of Category II diodes, having gold electron injecting contacts (electrode 1) and silver blocking contacts (electrode 2), exhibited both current-controlled negative resistance, (CCNR), in the reverse direction and voltage-controlled negative resistance, (VCNR), in the forward

direction. The 60 c/s characteristic displayed both the ohmic and the nonlinear behavior of a CdS film on a single trace (Fig. 27). CCNR was observed on the reverse voltage

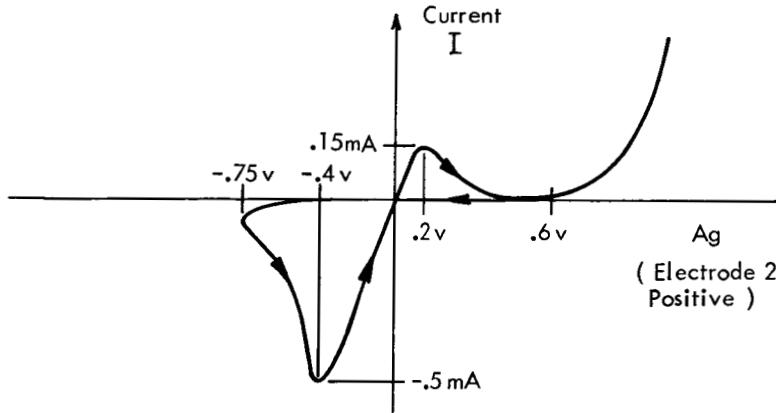


Fig. 27 Bimodal Conduction Characteristic for an Au-CdS-Ag Diode

trace, breaking down to the ohmic curve which was followed until a very low forward bias was reached, at which point VCNR was observed as a very rapid transition to the forward bias part of the nonlinear characteristic. The nonlinear characteristic was then retraced until reverse breakdown again occurred.

F. INTERPRETATION

The current for most diodes examined is Schottky emission limited by a barrier at the top electrode (electrode 2). Electrode 1, over which the CdS film is deposited, acts as a good electron injecting contact. Whether this is due to the higher condensation rate of Cd over the Au film which was generally used as electrode 1, as suggested by Shallcross and Dresner,³² or field emission as reported by Zuleeg³³ or high fields at the intercrystallite boundaries as suggested by Muller³⁴ is not known.

If we take a linear approximation to the barrier as in Fig. 28, then from

$$J = ST^2 [\exp - (\phi_{ms} - \Delta\phi)/kT] [\exp(qV/kT) - 1] \quad (4.4)$$

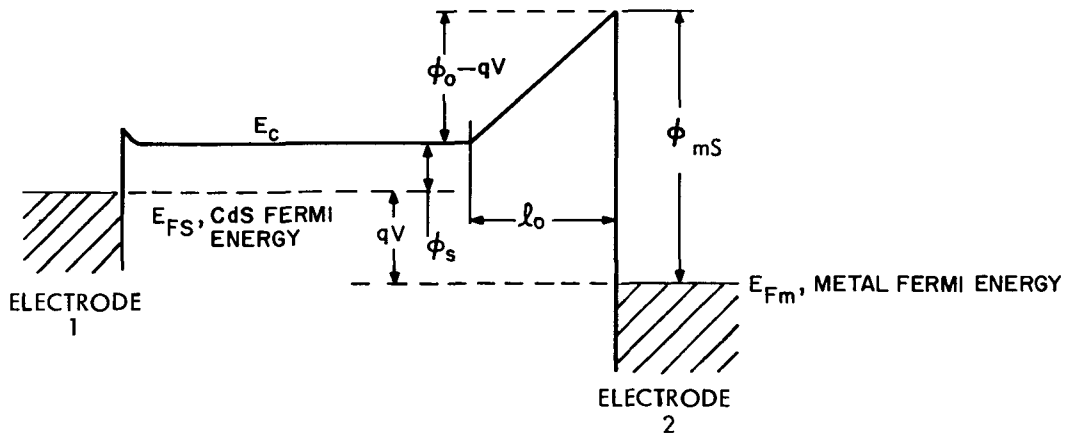


Fig. 28 Electron Energy Diagram for CdS Diode (Linearized Approximation; Drawn for Forward Bias Voltage, V)

where Richardson's constant is

$$S = (1-r) 4\pi q m^* k^2 / h^3 = 120(1-r)m^*/m \text{ amp. cm.}^{-2} \text{ } ^\circ\text{K}^{-2} \quad (4.5)$$

and the Schottky correction term is

$$\Delta\phi = \sqrt{q\overset{\circ}{E}/4\pi\epsilon} = \sqrt{14.3 \overset{\circ}{E}/K} \text{ electron volts} \quad (4.6)$$

$\overset{\circ}{E}$ = electric field in volts / $\overset{\circ}{\text{A}}$

K = relative dielectric constant

≈ 11.3 for CdS

For the linear barrier of Fig. 28

$$\overset{\circ}{E} = \frac{\phi_0/q - V}{l_0} \quad (4.7)$$

From current-temperature measurements, the current variation above 260°K appears not to be described by a Fermi-level analysis. The predominant current variations for Category I diodes (for which we should expect a Schottky barrier rather than an insulating layer) are of the form $\exp(-0.33/kT)$ and $\exp(-0.59/kT)$. It is significant

that for those diodes for which the energy 0.59 eV occurs, the energy 0.33 eV also occurs. For Category I diode 184/8, $\phi_0 = 0.47$ eV and $\lambda_0 = 595 \text{ \AA}$ at 240°K . The Schottky correction is then

$$\Delta\phi = 0.03 \text{ eV} \quad (4.8)$$

Consequently, if we assume $\phi_{ms} - \Delta\phi = 0.59$ eV the height of the barrier between the top gold electrode and the conduction band in the CdS appears to be

$$\phi_{ms} = 0.62 \text{ electron-volts} \quad (4.9)$$

The reverse characteristics have the variation $(-V)^{1/4}$ (Fig. 26 and 34) which is in agreement with the assumption of emission-limited image-force barrier reduction. This is described in Appendix B.

CHAPTER V

OPTICALLY MODULATED CONDUCTIVITY WITH VOLTAGE DE-EXCITATION

A. OBSERVATION

We have shown experimentally that the conductivity of a thin polycrystalline evaporated CdS film can be increased by at least an order of magnitude under optical stimulation by white light. The conductivity can then be restored, or "de-excited", to its original value by the application of a high-pulsed electric field. We have investigated this effect at 77°K and at room temperature. There is a much more pronounced effect at 77°K as the film is optically more sensitive at the lower temperature. The influence on photo-conductivity of high electric fields applied from one to several minutes has been reported by several authors for single crystals of CdS^{35, 36, 37} but as far as we know there are no published results for polycrystalline films. The present observations were made on polycrystalline evaporated CdS films and with fields of duration between 1 microsec and 1 second. Measurements of conductivity change were made: (a) to investigate how large a change in conductivity can be obtained with high field pulses; (b) to obtain a relationship between change in conductivity and the amplitude and duration of a single voltage pulse -- possible storage device applications of the effect requiring that the result of short de-excitation pulses be found; (c) to identify which is the dominant conduction process responsible for voltage de-excitation. A description of this research is contained in a thesis.³⁸

B. EXPERIMENTAL TECHNIQUE AND RESULTS

Measurements on thin CdS films were made using Category I, Au-CdS-Au diodes. Conductivity was measured with the liquid nitrogen cryostat used to observe thermally stimulated emission currents (Fig. 2). The effect of voltage pulses was found using the circuit of Fig. 29, the pulses being obtained from a GR-1217B pulse generator. It was found more convenient to measure the current through the film,

as monitored by the voltage developed across a 500 ohm resistor, rather than the voltage applied across the film. This applied voltage

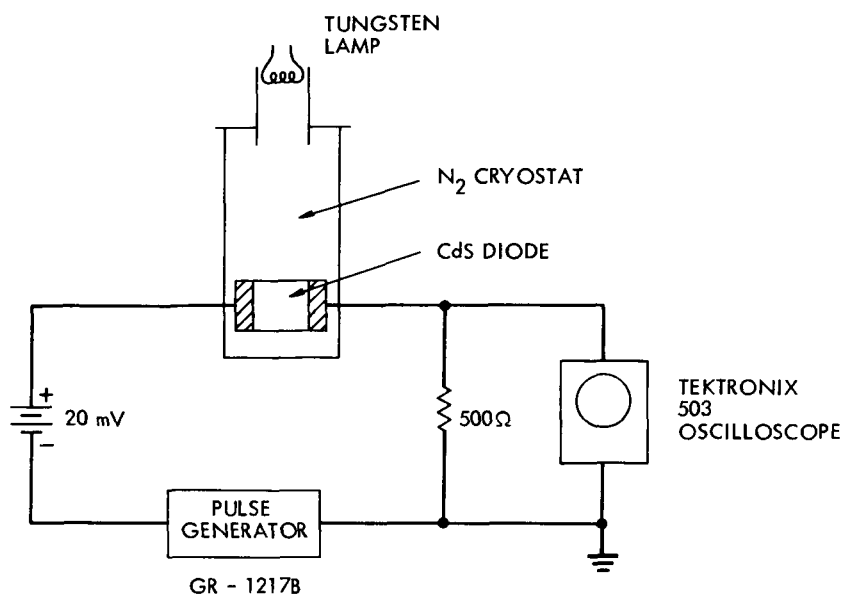


Fig. 29 Circuit for Measuring Effect of a Single Pulse on Conductivity

was obtained from a simultaneous measurement of the pulse generator output voltage. Before all conductivity decay and de-excitation experiments, the conductivity was allowed to reach an equilibrium value under constant illumination by white light, one minute being found sufficiently long for this purpose. The applied voltage for the measurement of photocurrent was 20 mV, which is in the linear current-voltage region of the diodes. Before the effect of field pulses was investigated, the normal conductivity decay was examined, the results of which are summarized as follows:

1. A $t^{-\alpha}$ decay relationship held for times between 10^{-1} and 10^3 minutes, α assuming several values over this time scale.
2. At 77°K, for an illumination which gave a photocurrent of 10^{-7} amps, there was an initial rapid decay in current for less than 1 second, after which α remained constant at 0.15. For a higher illumination, with a photocurrent of 5×10^{-5} amps, α assumed the values 0.73, 0.40 and 0.23 at times typically 1 1/2 minutes, 3 minutes, and 20 minutes, respectively, following the illumination. Once a value in the range 0.15 to 0.25 had been reached, this value remained for several hours.
3. At 300°K, the values for α are somewhat smaller, typically 0.07, and are reached after several seconds.

4. For low levels of illumination, it was occasionally found that the value of α would change to a higher value.
5. The continuous application of the 20 mV voltage gave a higher α value than when applied only sufficiently long for a conductivity measurement to be made.

Typical decay curves at 77°K and at 300°K are shown in Fig. 30.

The change in conductivity resulting from a single applied voltage (or current) pulse was obtained by applying the pulse 30 seconds after the end of illumination. Pulse width, amplitude, and polarity were varied. The change in conductivity, obtained as a percentage of the increase in conductivity above the dark value before illumination, is shown in Fig. 31. Although the curves are for a pulse applied 30 seconds following illumination, it was verified that the shape of the curves does not depend on when the pulse is applied, except possibly during the initial rapid decay. The following summarizes the results:

1. Pulses shorter than 100 microseconds had little effect on the conductivity decay, regardless of pulse amplitude.
2. When the pulse length was increased to 100 microseconds, the change in conductivity reached a "saturation" value; pulses of greater length were no more effective than 100 microsecond pulses.
3. Pulses applied with the blocking contact reverse-biased (Curves 3, 4 in Fig. 31) were more effective than forward biased pulses in changing the conductivity (Curves 1, 2). The voltages across the diode for the reverse-biased pulses were approximately 2 volts; those for forward-biased pulses, 0.5 volts.
4. The effect of field pulses is smaller for films which are less optically sensitive.
5. Following de-excitation there is practically no subsequent decay.
6. When a current pulse was applied to a film which had not been optically excited, no discharge current was observed immediately following the pulse.

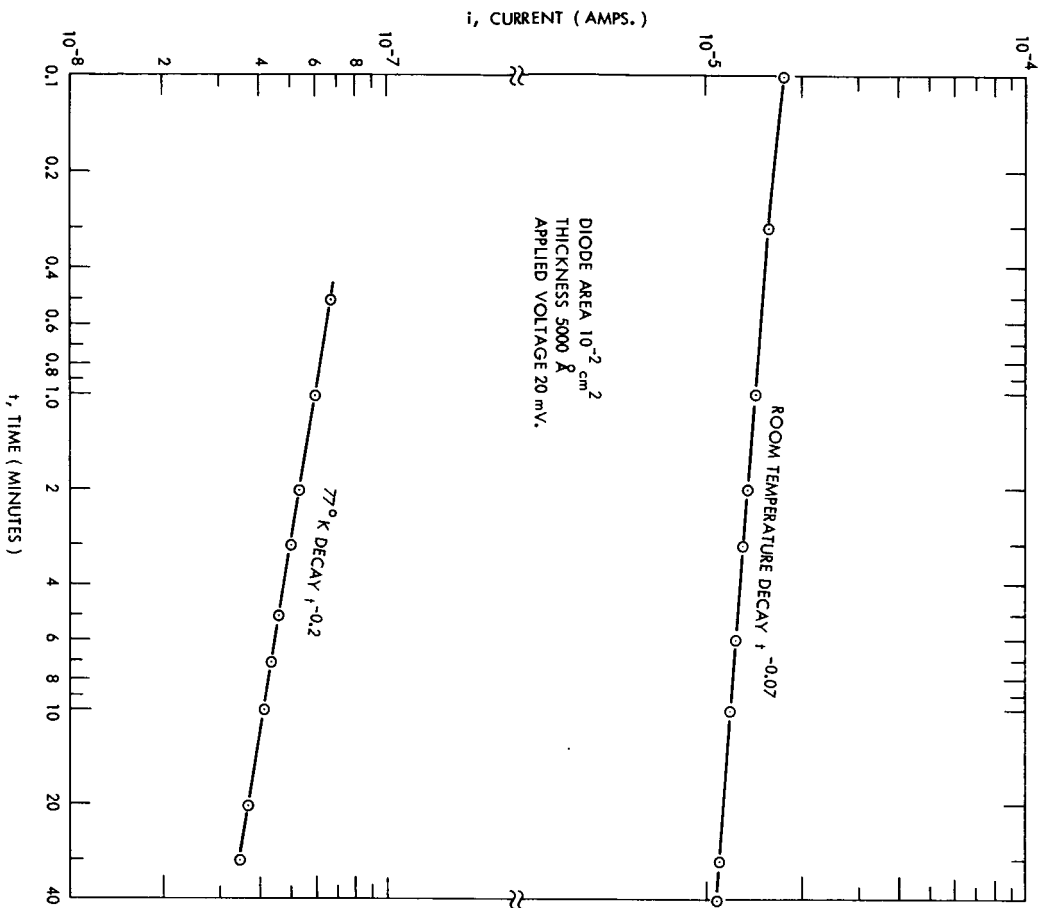


Fig. 30 Conductivity Decay Curves

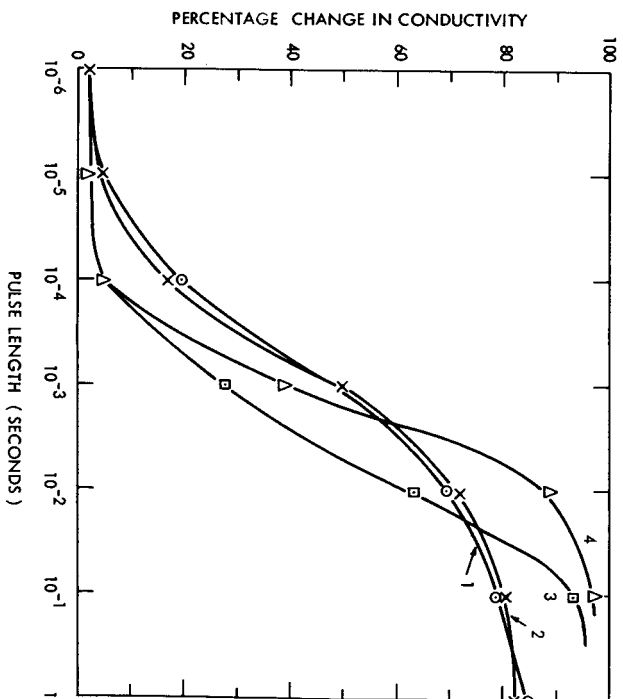


Fig. 31 Percentage Change in Conductivity with Pulse Length

C. INTERPRETATION

The interpretation of the effect of high electric fields on single CdS crystals is different for several authors. Boer and Kummel³⁵ suggest that high electric fields free electrons from traps. Kallmann and Mark³⁶ interpret their data as a decrease in the probability for retrapping. Bube³⁷ indicates that the modulation of conductivity could be the result of space-charge-limited currents injected by high fields.

Our measurements taken of dark conductivity at low temperature, (Chapter II), have indicated that various degrees of population of the donor and/or trapping levels are possible as evidenced by marked differences in conductivity. Since the differences in conductivity at 77°K produced by voltage pulses are similar to those produced during repeated measurements of dark conductivity with temperature, it was at first assumed that field ionization from donor or trapping levels was taking place. However, the probability for tunnel emission from a level 0.1 eV below the conduction band, subject to a field of 10^5 volt cm^{-1} , is very small ($\approx 5 \times 10^{-5}$).³⁹ Even if the voltage were applied across the barrier region alone, it is doubtful if there is field ionization from all but extremely shallow levels, and the predominant levels for our films were >0.1 eV below E_c .

A more likely explanation would be that there is an injected space-charge effect. However, no discharge current was observed immediately following the applied pulse. According to Lindmayer,⁴⁰ an injected charge which becomes trapped during a current pulse will give rise to a discharge current on subsequently shorting the film, unless the zero-field point in the film does not move. This can happen where only a single trapping level is involved. It is possible, however, that either the discharge current time constant is shorter than the R-C time constant of the diode and measuring circuit, or that the discharge current is too small to be detected by the technique used.

Since it was observed that during the application of a pulse both the voltage and current remained constant (after the initial charging time), there cannot only be current from trap emptying since this current would decrease with time. This is in agreement with the

observations of Kirov and Zhelev.⁴¹ The polarity dependence of reverse-bias pulses giving a greater change in conductivity, together with the change being relatively independent of pulse amplitude, could be due to barrier width modulation. Since the field is higher across the barrier region (see Appendix A for integrated resistance of the barrier), the modulation of barrier width would result in a change of the effective volume of film over which the high field is applied. The conductivity change with polarity reversal being much greater than with amplitude change for either polarity, is in agreement with the greater barrier width change on reversal of the polarity.

At 77°K, the density of conduction band electrons before optical excitation, from $\sigma = nq\mu$, is of the order of 10^{10} cm^{-3} . During optical excitation the density of carriers is increased to 10^{13} cm^{-3} , while during the voltage pulse the density is further increased to 10^{15} cm^{-3} . Following the pulse, the density again becomes of the order of 10^{10} cm^{-3} . Since no discharge current corresponding to this large fall in charge density was observed, (subject to the limitations mentioned above of no zero-point movement following the application of a voltage pulse), we consider that the effect of the pulse is to shift electrons within the film to a region of lower re-trapping and higher recombination, as proposed by Kallmann and Mark,³⁶ rather than an injected space-charge effect.

CHAPTER VI

NEGATIVE RESISTANCE IN CdS DIODES

A. OBSERVATION

We observed a current-controlled negative resistance (CCNR) in the conduction of some metal-CdS-metal thin-film diodes. Because the effect depends on the excitation frequency, it is not expected to be useful for high-frequency electronic applications. However, the presence of CCNR at low frequencies can provide insight into the nature of the conductivity mechanism in thin CdS films.

The effect for an Al-CdS-Au diode is shown in Fig. 32 with values

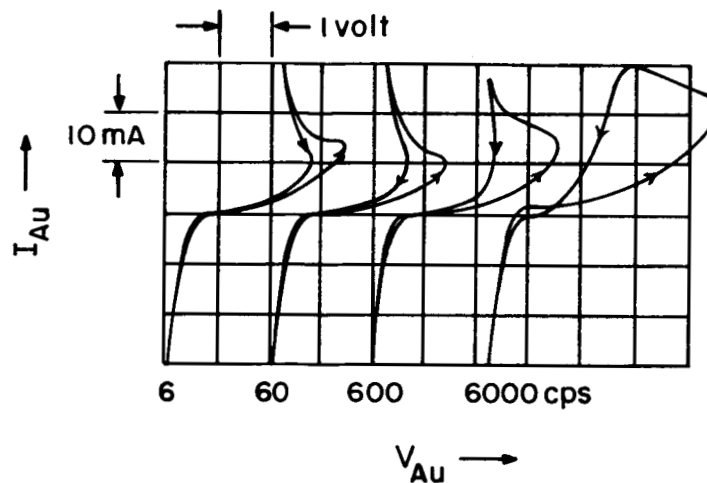


Fig. 32 Negative Resistance of Al-CdS-Au Diode at Various Sweep Frequencies

of excitation frequency ranging from 6 to 6000 c/s. A hysteresis effect is present even at 6 c/s, and it increases with excitation frequency. The negative resistance portion of the current-voltage characteristic occurs with the Au (last deposited or top) electrode positive; however some diodes display a negative resistance for both polarities of the current. At low frequencies the voltage peak for the diode characteristic in Fig. 32 is 2.4 volts and occurs at an average current density of 10 ma per mm². The current increases beyond the negative resistance region with little accompanying voltage change,

and the value of the voltage is then 1.2 volts. Diodes of this type are often observed to undergo a forming process when the current excitation is first applied, and during this period of operation the negative resistance region develops from an initial hysteresis at high voltage with the Au electrode positive.

In contrast to this example of negative resistance, Au-CdS-Au diodes, which invariably form with the top Au electrode as the blocking contact, exhibit a similar CCNR when the bottom Au electrode is positive (reverse bias). The negative resistance characteristic for a diode of this type is shown in Fig. 33. The data was obtained for this curve with d.c. excitation, and a four-terminal measurement technique was used to eliminate any voltage drop caused by series resistance in the leads from contributing to the measured voltage. The average current density at the voltage peak is again 10 ma per mm²; however the voltage at the peak is 1.65 volts. The voltage for current above the negative resistance region is 1.35 volts.

Films, with voltages applied of magnitude in the range of the voltage at the peak, exhibit destructive changes as shown in Figs. 34a and 34b. The film in Fig. 34a was observed visually in the microscope, and a red optical emission was noted. The emission originated from regions where the small dots in Fig. 34a occur. The red emission occurred only when the Au electrode was positive. When the Al electrode was positive, emission occurred also, but this emission was white and did not have the red color. The pattern of destruction in Fig. 34b is typical of Au-CdS-Au diodes, where the damage progresses across the surface of the film in an oscillatory manner.

B. INTERPRETATION

Observation of CCNR in materials such as CdS is by no means a new discovery. Henisch⁴² describes similar effects for point contact rectifiers involving materials such as Ge, Si, PbSe, and PbS. The physical description of this effect in these materials as affected by excitation frequency, temperature, and peak applied voltage bears a marked resemblance to our observation in CdS thin-film diodes. Negative resistance in CdS films has also been observed by Chopra,⁴³

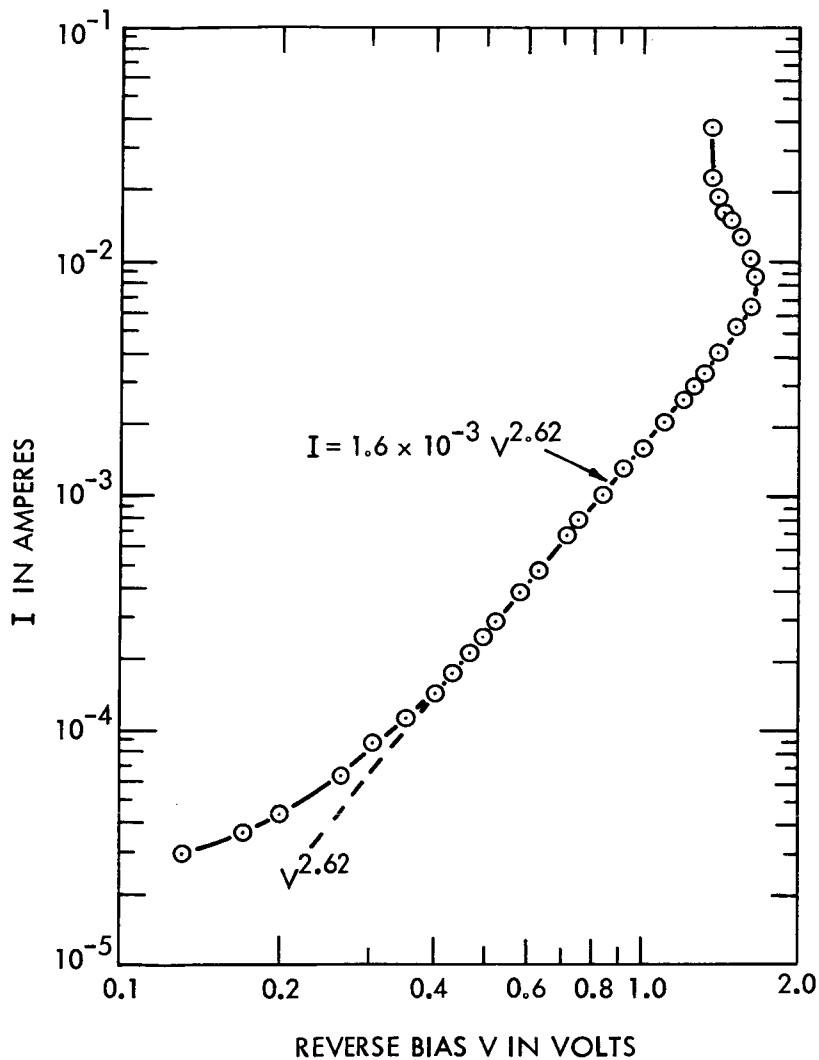
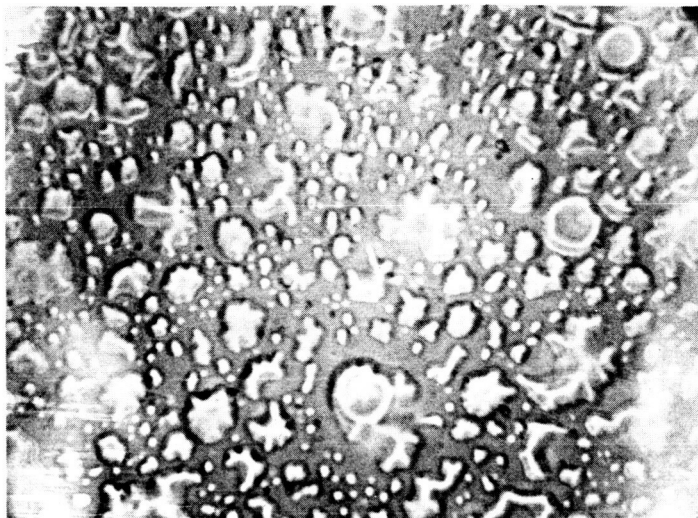
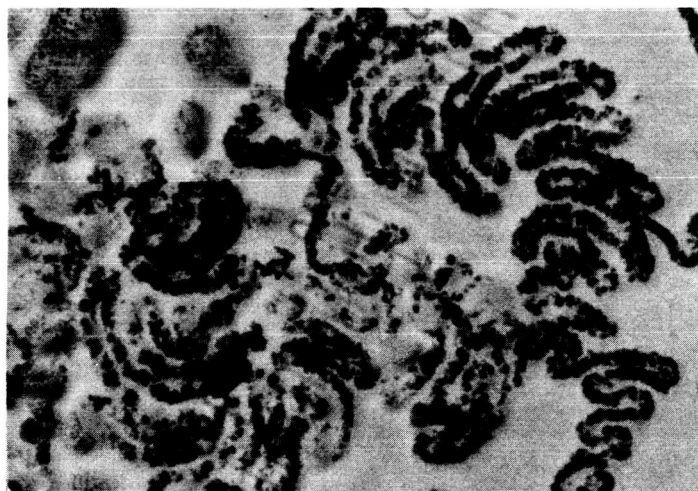


Fig. 33 Au-CdS-Au Diode Negative Resistance
Film No. 188, Diode No. 8. $T = 300^{\circ}\text{K}$



→|.05mm|←

a) Al - CdS - Au



b) Au - CdS - Au

Fig. 34 Destructive Changes to Au Electrode
During Negative Resistance Observation

and similar effects have been observed in thin films of Nb, Ta, and W by Chopra⁴⁴ and by Beam and Armstrong.⁴⁵ The latter observations may be related to the CCNR in the Al-CdS-Au diodes, where an Al_2O_3 film can form at the surface of the Al electrode.⁴⁶

Litton and Reynolds⁴⁷ observed a negative resistance in bulk CdS samples $\cong 1$ cm thick. These observations were performed on special crystals called "tap" crystals which are doped with elements from Column I of the periodic table. "Tap" crystals are remarkable for the photo-emission of green light when tapped or otherwise mechanically disturbed. They also exhibit photo-induced conductivity effects which are similar to those described for CdS thin-film diodes in Chapter II of this report. The CCNR in these crystals can only be observed after they have been optically stimulated by light with photon energies exceeding 1.75 eV. The explanation for CCNR in CdS tap crystals is that injection of holes from a Ag electrode occurs at the voltage peak. The space-charge within the crystal produced by electron injection from an In electrode is thereby suppressed, so that the current increases as the voltage decreases. However, this explanation is not acceptable for the CdS thin-film diodes because the CCNR occurs in this case for the top electrode negative. The top electrode of an Au-CdS-Au diode is invariably more blocking than the bottom electrode; hence it is more likely that hole injection, if it occurs at all, will do so when the top electrode is positive.

Observations of CCNR in Ge samples by Steele, Ando, and Lampert⁴⁸ are explained by the theory of double-injection space-charge-limited current.^{49, 50} Double injection is accomplished by avalanche breakdown, which injects minority carriers generated by the impact ionization process only when the sample is biased in the forward direction. The pre-breakdown characteristic in this theory is ohmic, and the theory does not depend upon space-charge-limited current alone providing the negative resistance. We do not believe this theory applies to CdS thin-film diodes because holes in CdS are not mobile, due to the presence of hole traps. Thus, ionization of electron-hole pairs is not likely to produce much increased conductivity.

A possible explanation for the CCNR in CdS thin-film diodes is suggested by the form of the current voltage characteristic prior to breakdown, as shown in Fig. 33 for diode 188/8. At low voltages the current varies linearly with voltage and the value of the constant of proportionality is consistent with the integrated ohmic resistivity of the depletion layer beneath the top Au electrode (see Appendix A). As the voltage is increased, diode nonlinearity becomes evident. Because the diode is in reverse bias the saturation current increases because of image force lowering of the barrier. However, the CdS thin-film diode is known to have traps due to defect structure, and these reduce the space-charge-current limit below the Schottky emission limit. The straight line portion of the curve in Fig. 33 is typical of space-charge-limited current in the presence of a quasi-continuous exponential distribution of traps. According to the theory of single-carrier space-charge-limited current

$$I \propto V \left(\frac{T_c}{T} + 1 \right) / l^3(V) \quad (6.1)$$

where I is the current, V is the voltage across the low-conductivity layer adjacent to the top Au contact, and T is the absolute temperature. The thickness of the region in which the space-charge-limited current is confined is the depletion layer width, $l(V)$, which is proportional to the square-root of the junction voltage. Therefore, Eq. 6.1 can be rewritten as

$$I \propto V \left(\frac{T_c}{T} - \frac{1}{2} \right) \quad (6.2)$$

In the above expressions the distribution of traps is presumed to be exponential and is described by a characteristic temperature, T_c , through the expression

$$M_t = A \exp[-E/kT_c] \quad (6.3)$$

where E is the depth of a trapping level below the conduction band and k is Boltzmann's constant. According to Eq. 6.2 and the data of Fig. 33 for a Category I diode, the characteristic temperature is 914° , so that the average trap depth is 0.08 eV. When the voltage reaches the peak

value the carriers begin to produce impact ionization of trapped electrons. Consequently, the conductivity returns to the emission-limited value. Although this explanation for the negative resistance is simple and physically plausible, it is not entirely convincing. The trapping energy of 0.08 eV is not unreasonable; however, the assumption of an exponential trapping distribution is not consistent with other measurements of the CdS films. The thermally-stimulated current measurements give trapping levels at 0.12 and 0.37 eV. Although the current peaks spread somewhat, this type of measurement is expected to produce a distributed current response for a discrete trapping level. We have no reason to believe from the thermally-stimulated-current measurements that traps are distributed even quasi-exponentially at a level of 0.08 eV below the conduction band.

A second interpretation of the negative resistance is based upon the plot shown in Fig. 35 where the data for Fig. 33 is replotted with $\log I$ as a function of $(-V)^{1/4}$. The data is seen to fit a straight line over nearly two decades of current variation, in agreement with the assumption of emission-limited image-force barrier reduction as described in Appendix B. From the slope of the straight line we can determine, using Eq. B.11 of Appendix B, that the donor concentration is $7.5 \times 10^{17} \text{ cm}^{-3}$; this value agrees closely with the differential capacitance measurements. Further, from the deviation of the data at low voltages from the straight line, we can estimate that the contact potential is approximately 0.01 volt. The saturation current, I_s , agrees with the theory if ϕ_{ms} is assumed to be $\cong 0.58$ eV which agrees with the temperature dependent activation energy measured for some of the Au-CdS-Au diodes. Because of the excellent agreement of the data with the theoretical reverse-bias emission current and with measured differential capacitance results, it appears likely that this mechanism is responsible for the pre-breakdown current. There cannot be any appreciable space-charge present, so that the CCNR has to be interpreted as avalanche breakdown due to electron-hole pair production in the depletion region. The only flaw in this model is that the contact potential is so low that there is little change from the depletion region to the interior of the CdS diode.

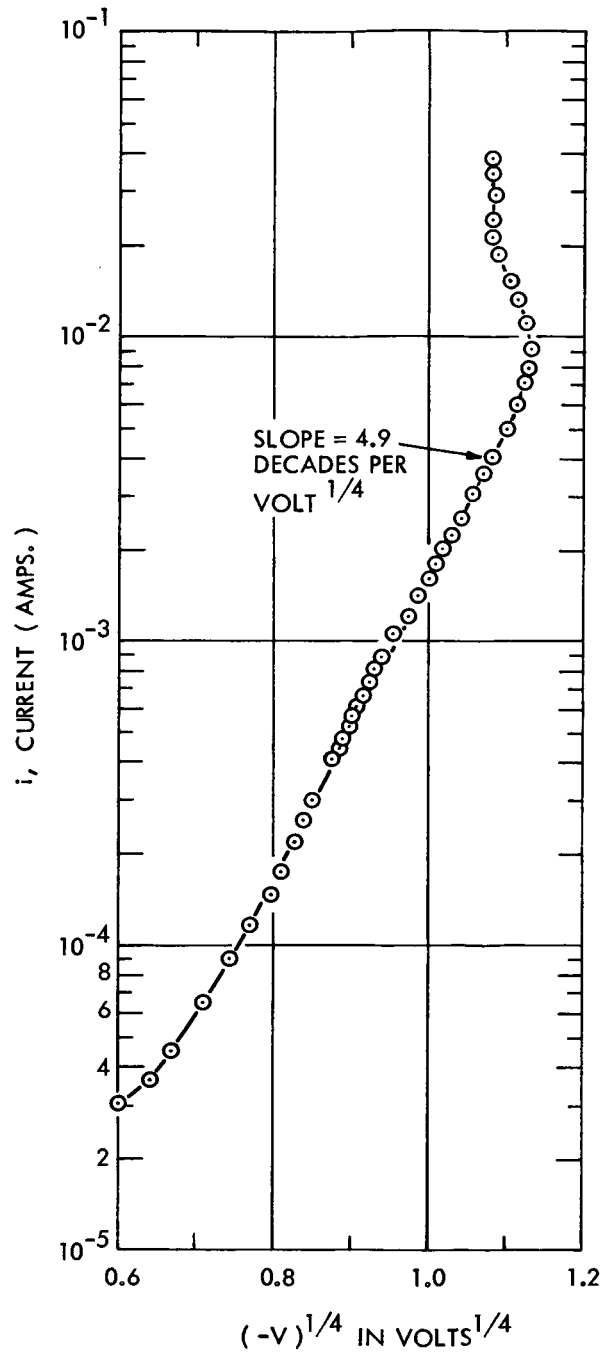


Fig. 35 Au-CdS-Au Diode. Log I vs. $(-V)^{1/4}$
Film No. 188, Diode No. 8. $T = 300^\circ\text{K}$

C. CONCLUSIONS

Although both models proposed to account for CCNR in Au-CdS-Au diodes suffer from major defects, we are more confident that the second-pair production by avalanche, following Schottky emission, is the more realistic of the two. Four impressive points of agreement occur for this model, namely:

- a. straight line plot of $\log I$ vs. $(-V)^{1/4}$,
- b. slope agrees with N_D determined by differential capacitance measurements,
- c. deviation of data from straight line agrees with value of ϕ_0 deduced from differential capacitance measurements,
- d. saturation current provides a measure of ϕ_{ms} which agrees with typical current vs. $1/T$ activation energies.

APPENDIX A

INTEGRATED RESISTIVITY OF DEPLETION LAYER

In the absence of an externally applied voltage the total current density in a depletion layer must be everywhere zero, and can be resolved into the sum of a diffusion component and a drift component

$$J_T = J_{\text{diff}} + J_{\text{drift}} \quad (\text{A.1})$$

Spence⁵¹ has shown that the Fermi-level has the same relationship to the total current as the electrostatic potential has to the drift current or the chemical potential to the diffusion current. Therefore,

$$J_T = \mu n \frac{dE_f}{dx} = 0 \quad (\text{A.2})$$

where μ is the electronic mobility and n is the concentration of conduction electrons. Consequently, when there is no applied voltage, the Fermi-level is constant. When there is an applied voltage, if we assume Eq. A.2 with $J_T \neq 0$ still applies, then

$$\frac{dE_{fn}}{dx} = \frac{I}{\mu A n} \quad (\text{A.3})$$

in which E_{fn} is the nonequilibrium Fermi-level and A is the area of the depletion layer. The concentration of conduction electrons is given by

$$n = N_c \exp \left\{ - \frac{[\phi(x, V) - E_{fn}]}{kT} \right\} \quad (\text{A.4})$$

where N_c is the effective density of states in the conduction band and $\phi(x, V)$ is the energy of the conduction band edge. Substituting Eq. A.4 into Eq. A.3 and rearranging:

$$\exp [E_{fn}/kT] \frac{dE_{fn}}{dx} = \frac{I}{\mu N_c A} \exp [\phi(x, V)/kT] \quad (\text{A.5})$$

Multiplying both sides by dx and integrating from $x = 0$ to $x = l(V)$:

$$\int_0^{qV} \exp [E_{fn}/kT] dE_{fn} = \frac{I}{\mu N_c A} \int_0^{l(V)} \exp [\phi(x, V)/kT] dx \quad (A.6)$$

with $E_{fn}(x = l(V)) = qV$, $E_{fn}(x = 0) = 0$, and $l(V)$ = the width of the depletion layer. Integration yields

$$kT(e^{qV/kT} - 1) = \frac{I}{\mu N_c A} \int_0^{l(V)} \exp [\phi(x, V)/kT] dx \quad (A.7)$$

If $qV \ll kT$, then $l(V) \cong l(0) = l_0$ and $\phi(x, V) \cong \phi(x, 0) = \phi(x)$.

Then for this low-voltage condition,

$$V = \frac{I}{q\mu N_c A} \int_0^{l_0} \exp [\phi(x)/kT] dx \quad (A.8)$$

or $V = RI \quad (A.9)$

where $R = \frac{1}{q\mu N_c A} \int_0^{l_0} \exp [\phi(x)/kT] dx \quad (A.10)$

Now, the function $\phi(x)$ for a constant donor doping has the form (see Fig. 36)

$$\phi(x) = \phi_s + (\phi_0 - qV) \left(\frac{x}{l_0}\right)^2 \quad (A.11)$$

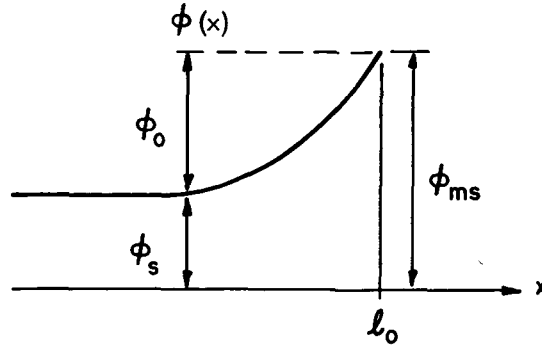


Fig. 36 Conduction Band Edge vs. Distance Across Barrier

Substitution of Eq. A. 11 into Eq. A. 10 yields

$$R = \frac{\exp[\phi_s/kT]}{q\mu N_c A} \int_0^{l_0} \exp[(\phi_0 - qV)(\frac{x}{l_0})^2/kT] dx \quad (A.12)$$

The principal contribution to the integral occurs near $x = l$ where the integrand is large. As a lower bound estimate of the value of the integral, we approximate the quadratic form of $\phi(x)$ with a linear function using the slope at $x = l$. Then

$$\phi(x) \cong \phi_s + \phi_0 - 2\phi_0(l-x)/l \quad (A.13)$$

Using Eq. A. 13 instead of Eq. A. 11, we obtain for the resistance

$$R \approx \frac{kTl_0}{2\phi_0 q\mu AN_c \exp[-\phi_{ms}/kT]} \quad (A.14)$$

where l_0 is the zero-bias depletion layer width and is given by

$$l_0 = \sqrt{\frac{2\epsilon}{q} \phi_0} \quad (A.15)$$

For the diode whose I-V reverse-bias data is shown in Fig. 33,

reasonable values for the constants involved in Eqs. A.14 and A.15 are

$$\begin{aligned}kT/q &= 0.025 \text{ eV} \\ \phi_o/q &= 0.3 \text{ eV} \\ \phi_{ms}/q &= 0.6 \text{ eV} \\ A &= 10^{-6} \text{ m}^2 \\ N_c &= 10^{24} \text{ m}^{-3} \\ \epsilon &= 10^{-10} \text{ f/m} \\ \mu &= .02 \text{ m}^2/\text{V-sec}\end{aligned}$$

With these values, the expected value of resistance at low applied voltages (less than 25 mv) is 7000Ω . The resistance at low voltage for the diode we are considering is about 4000Ω , so that the integrated resistance gives a correct order of magnitude estimate of the diode performance for low voltage.

APPENDIX B

SCHOTTKY EMISSION FOR REVERSE BIASED METAL-SEMICONDUCTOR JUNCTION

The Schottky emission equation for the current passing through a metal-semiconductor barrier rectifier, whose band diagram is as shown in Fig. 37, is

$$I = AST^2 \exp[-\phi_{ms}/kT] \{ \exp[qV/kT] - 1 \} \quad (B.1)$$

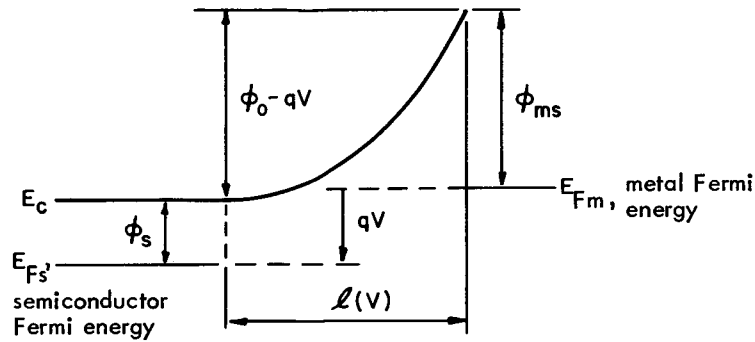


Fig. 37 Electron Energy Diagram for Metal-Semiconductor Contact (Drawn for Reverse Bias)

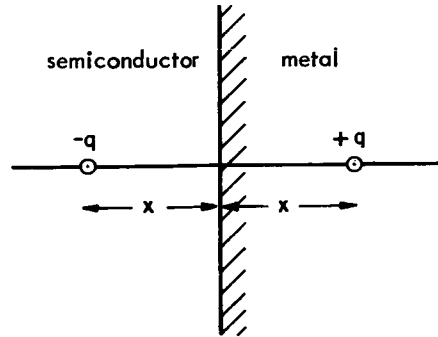


Fig. 38 Charge ($-q$) Within Semiconductor and Its Image ($+q$) in Metal

where

- A = area of the diode
- S = emission constant ($120 \text{ amp-cm}^{-2} \text{ } ^\circ\text{K}^{-2}$)
- T = absolute temperature
- k = Boltzmann's constant
- ϕ_{ms} = metal-semiconductor work function

- q = magnitude of electronic charge
 V = junction voltage appearing across depletion layer
 (positive for forward bias)

When the magnitude of the reverse bias is large compared to kT/q , the emission current reduces to the saturation value

$$I_s = AST^2 \exp[-\phi_{ms}/kT] \quad (B.2)$$

However, saturation does not occur because the effect of an image potential has to be included. The effect of the image potential is to lower the value of ϕ_{ms} by an amount that is dependent on the reverse-bias voltage. A negative charge in transit across the junction is shown in Fig. 38 at a distance x from the metal surface. The potential energy of this electron in the field of its image is

$$\phi_i(x) = \frac{q^2}{16\pi\epsilon_0} \left(\frac{1}{x}\right) \quad (B.3)$$

where ϵ_0 is the free-space dielectric constant. The dielectric constant appropriate to the semiconductor is not used because we assume that the charge crosses the barrier so fast that the semiconductor polarization cannot respond. Using Eq. B.3 as a correction to the potential function, $\phi_d(x)$, of a constant donor density, N_D , depletion layer, we obtain

$$\begin{aligned} \phi(x) &= \phi_d(x) + \phi_i(x) \\ &= \phi_{ms} + [\phi_0 - qV] \left\{ \frac{[x + \ell(V)]^2}{\ell^2(V)} - 1 \right\} + \frac{q^2}{16\pi\epsilon_0} \left(\frac{1}{x}\right) \end{aligned} \quad (B.4)$$

where $\ell(V)$ is the width of the depletion layer. The location of the maximum of $\phi(x)$ occurs near the metal surface and therefore, to simplify the resulting equations, we approximate $\phi_d(x)$ by a linear function of x using the slope of $\phi_d(x)$ at $x = 0$, then

$$\phi(x) = \phi_{ms} + \frac{2(\phi_0 - qV)}{\ell(V)} x + \frac{q^2}{16\pi\epsilon_0} \left(\frac{1}{x}\right) \quad (B.5)$$

The maximum of $\phi(x)$ determined from Eq. B.5 is

$$\phi(x_{\max}) = \phi_{ms} - q \left\{ \frac{\phi_o - qV}{2\pi\epsilon_o \ell(V)} \right\}^{1/2} \quad (\text{B. 6})$$

and occurs at

$$\phi_{\max} = -q \left\{ \frac{\ell(V)}{32\pi\epsilon_o(\phi_o - qV)} \right\}^{1/2} \quad (\text{B. 7})$$

The depletion layer thickness, $\ell(V)$, is related to the junction voltage by the well-known relation

$$\ell(V) = \left\{ \frac{2\kappa\epsilon_o}{q^2 N_D} (\phi_o - qV) \right\}^{1/2} \quad (\text{B. 8})$$

where κ is the dielectric constant of the semiconductor and is used here because the voltage is assumed to change slowly enough for the polarization to respond. Substitution of Eq. B.8 into Eq. B.6 gives

$$\begin{aligned} \phi(x_{\max}) &= \phi_{ms} - \Delta\phi \\ &= \phi_{ms} - q \left\{ \frac{q^2 N_D (\phi_o - qV)}{8\pi^2 \kappa \epsilon_o^3} \right\}^{1/4} \end{aligned} \quad (\text{B. 9})$$

The above expression represents the barrier height and is used in place of ϕ_{ms} in Eq. B.2 to obtain the reverse-bias diode current, I_r .

$$\begin{aligned} I_r &= AST^2 \exp[-\phi_{ms}/kT] \exp[\Delta\phi/kT] \\ &= I_s \exp[\Delta\phi/kT] \end{aligned} \quad (\text{B. 10})$$

Because $\Delta\phi$ is proportional to $(-V)^{1/4}$ for values of $(-V) > \phi_o/q$, a semi-log plot of I vs. $(-V)^{1/4}$ is expected to provide a straight-line fit of the data. The current should be twice the extrapolated

straight-line value when the voltage, $(-V)$, falls to a value that is equal to $15\phi_0$. The slope of the straight line is

$$\frac{\Delta \log I}{\Delta \{(-V)^{1/4}\}} = \frac{q}{2.3 kT} \left\{ \frac{q^3 N_D}{8\pi^2 \kappa \epsilon_0^3} \right\}^{1/4} \quad (\text{B.11})$$

APPENDIX C

DONOR AND TRAPPING LEVEL CONTROL OF CONDUCTIVITY

1. DONOR LEVEL CONTROL OF CONDUCTIVITY

If we assume the presence of both donor and trapping energy levels, uniformly distributed spatially throughout the CdS film, and that there is a much larger rate of carrier exchange between the donor levels and the conduction band, than between the trapping levels and conduction band the following analysis holds.

If there is a narrow band of donor levels of average energy, E_D , having an average density of states, N_D , and, similarly, trapping levels of average energy, E_T , and density, N_T , then if we use the rate equation approach for thermal equilibrium:

Rate of ionization of donors = rate of capture by ionized donors

$$(N_D - N_T - n_c) \nu \exp [-(E_c - E_D)/kT] = \nu s n_D^+ n \quad (C.1)$$

in which

- n_D^+ = number of ionized donors
- ν = "attempt to escape" frequency from donors
= $\nu_s N_c$
- n = number of electrons available for capture by donors
= n_c
- ν = thermal velocity of free electrons
- s = donor ion capture cross-section for electrons

Therefore,

$$(N_D - N_T - n_c) N_c \exp [-(E_c - E_D)/kT] = n_c (n_c + N_T) \quad (C.2)$$

Since $n_c \ll N_T$,

$$(N_D - N_T) \exp [-(E_c - E_D)/kT] = N_T \exp [-(E_c - E_F)/kT] \quad (C.3)$$

then

$$E_F = (E_C - E_D) + kT \ln [N_T / (N_D - N_T)] \quad (C.4)$$

For example, for diode 239/4, the linear variation of $\ln i_D$ with $1/T$ holds for several orders of current magnitude. For this diode

$$E_F = -1.08 \times 10^{-3} T - 0.13 \text{ eV}$$

and

$$N_T / (N_D - N_T) = 3.7 \times 10^{-6}$$

If we assume (from Chapter III) that $N_D = 10^{17}$ per cm^3 , then $N_T \cong 10^{11}$ or 10^{12} per cm^3 , which is low for polycrystalline films.

2. TRAPPING LEVEL CONTROL OF CONDUCTIVITY

Measurement of thermally stimulated emission current densities (Chapter II) and the predominance of 0.13 eV and 0.33 eV activation energies, suggest that there are large densities of traps, $\gg N_D$, at these levels. If we consider equilibrium between the conduction band and the higher of these levels, that is, the 0.13 eV level, and that there is complete donor ionization from levels higher than 0.13 eV, then

Rate of escape from the trapping level, E_T , = rate of trapping by this level

$$n_T \nu \exp [-(E_C - E_T) / kT] = \nu s' (N_T - n_T) n_C \quad (C.5)$$

Since

$$\nu = \nu s' N_C \quad (C.6)$$

where

- ν = attempt to escape frequency of an electron from a trapping level
- ν = thermal velocity of free electrons
- s' = trapping cross-section for electrons
- n_T = number of trapped electrons
- n_C = number of free electrons

For $N_D \ll N_T$, and $n_c \ll N_T$,

$$n_c = \frac{N_D}{N_T} N_c \exp[-(E_c - E_T)/kT] \quad (C.7)$$

Since $n_c = N_c \exp[-(E_c - E_F)/kT]$ (C.8)

$$E_F = kT \ln \left(\frac{N_D}{N_T} \right) + E_T \quad (C.9)$$

For $N_D \cong 10^{17}$ per cm^3 , and $N_T \cong 10^{22}$ per cm^3

$$E_F = -10^{-3}T + E_T \quad (C.10)$$

This agrees with the observed variation of the Fermi-level for temperatures below 240°K . For temperatures above 240°K , the conductivity appears to be controlled by the 0.33 eV level. The variation of E_F with temperature is then much smaller, however, and, for many diodes measured, there is a tendency for the Fermi-level to rise towards the conduction band at temperatures above 290°K . This region appears not to be described by a Fermi-level analysis. The highest activation energy measured for diodes in this region of temperature is 0.59 eV. It is significant that for these diodes the activation energy of 0.33 eV also occurs.

3. IDENTIFICATION OF THE ACTIVATION ENERGY, E_A , WITH DEPTH OF A TRAPPING ENERGY LEVEL, $(E_c - E_T)$.

The activation energy, E_A , can be expressed in terms of σ and σ_∞ , (the "conductivity" when $T \rightarrow \infty$), as

$$E_A = +kT \ln \sigma_\infty / \sigma \quad (C.11)$$

where

$$\sigma = n_c q\mu$$

$$\sigma_\infty = n_{c_\infty} q\mu$$

If we assume trapping level control of the conductivity,

$$n_T N_c \exp [-(E_c - E_T) / kT] = (N_T - n_T) n_c \quad (C.12)$$

$$(E_c - E_T) = kT \ln \left[\frac{n_T N_c}{(N_T - n_T) n_c} \right] \quad (C.13)$$

Identifying E_A and $(E_c - E_T)$, requires that

$$\frac{(N_T - n_T) n_c}{n_T N_c} = \frac{n_c}{n_{c\infty}} \quad (C.14)$$

But $N_D = n_T + n_c$, so we require that

$$\frac{(N_T - N_D + n_c) n_c}{(N_D - n_c) N_c} = \frac{n_c}{n_{c\infty}}$$

or

$$\frac{N_T}{N_D N_c} = \frac{1}{n_{c\infty}}$$

Since $N_T \gg N_D \gg n_c$

we require $n_{c\infty} = \frac{N_D N_c}{N_T}$ or $\sigma_{\infty} = \frac{q \mu N_c N_D}{N_T}$ (C.15)

Typical values for the variation of Fermi-level with temperature below 280°K are

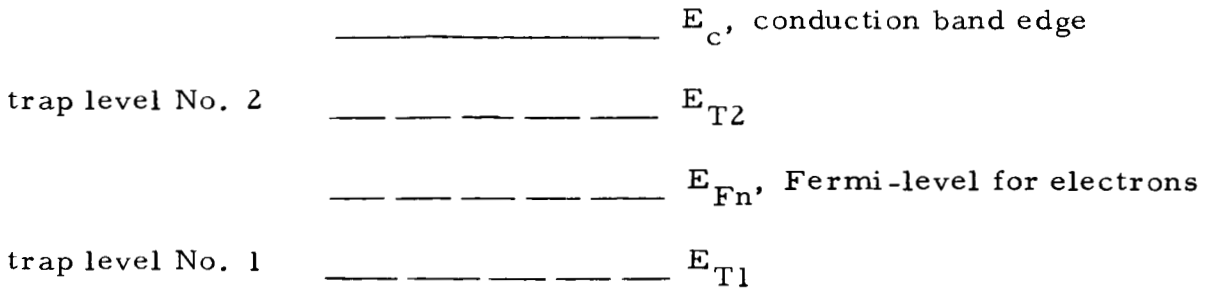
$$E_F \cong -10^{-3} T + E_T$$

and $\sigma_{\infty} = 2 \times 10^{-5} (\text{ohm-cm})^{-1}$

Therefore, we require $N_D / N_T = \frac{\sigma_{\infty}}{q \mu N_c} \cong 10^{-5}$, which is consistent with $N_D = 10^{17}$ per cm^3 and $N_T = 10^{22}$ per cm^3 .

4. IDENTIFICATION OF THE ACTIVATION ENERGY, E_A ,
WITH THE AVERAGE ENERGY OF TWO TRAPPING LEVELS

Consider the Fermi-level located between two trapping levels as shown below.



- Let
- n_{T1} = No. of electrons in level 1, (m^{-3})
 - N_{T1} = Density of states in level 1, (m^{-3})
 - n_{T2} = No. of electrons in level 2, (m^{-3})
 - N_{T2} = Density of states in level 2, (m^{-3})
 - n_c = No. of electrons in conduction band, (m^{-3})

First let us assume that

$N = N_{T1}$ = total number of electrons in system. This is constant providing we can neglect excess of recombination over generation or that photo excitation is not occurring. That is, we assume photo excitation has occurred and is over. Further recombination is for the moment small compared to retrapping into E_{T2} and E_{T1} levels.

We further assume that

$$n_c \ll n_{T2}$$

which holds provided $E_c - E_T$ is not comparable to kT or that N_c is not much larger than N_{T2} . Then, with these assumptions,

$$n_{T2} \cong p_{T1} \cong N_{T1} - n_{T1} \tag{C.16}$$

where p_{T1} is the number of vacant states at level E_{T1} .

Therefore

$$\frac{N_{T2}}{\frac{1}{2} e^{(E_{T2}-E_{Fn})/kT} + 1}} = N_{T1} \frac{N_{T1}}{\frac{1}{2} e^{(E_{T1}-E_{Fn})/kT} + 1}} \quad (C.17)$$

with $E_{T2} - E_{Fn} \gg kT$

$$E_{Fn} - E_{T1} \gg kT$$

Eq. C.17 reduces to

$$2N_{T2} e^{-(E_{T2}-E_{Fn})/kT} = \frac{1}{2} N_{T1} e^{-(E_{Fn}-E_{T1})/kT} \quad (C.18)$$

Solving for the Fermi-level

$$E_{Fn} = \frac{E_{T1} + E_{T2}}{2} + \frac{kT}{2} \ln \frac{N_{T1}}{4N_{T2}} \quad (C.19)$$

The number of electrons in the conduction band is

$$n_c = N_c e^{-(E_c - E_{Fn})/kT}$$

$$n_c = N_c \sqrt{\frac{N_{T1}}{4N_{T2}}} e^{-[E_c - \frac{E_{T1} + E_{T2}}{2}]/kT} \quad (C.20)$$

From Eq. C.20 we note

$$\ln n_c = \ln N_c \sqrt{\frac{N_{T1}}{4N_{T2}}} - \frac{E_A}{kT} \quad (C.21)$$

where E_A is the mean value of E_{T1} and E_{T2} as measured downward from conduction band. Then if $\sigma = nq\mu$ with $\mu \neq \mu(T)$ the plot of $\ln \sigma$ vs. $\frac{1}{T}$ has a slope of $-E_A/k$. From the preceding we see that the slope of the data is not necessarily directly related to the value of a single trapping level, but can depend upon two levels.

Next, let us assume that the total number of electrons in the system, $N < N_{T1}$. Now E_{Fn} will be close to E_{T1} . $E_{Fn} - E_{T1}$ may not be large compared to kT . Also n_{T2} , n_c are both small compared to N , unless the separation between E_{T1} and E_{T2} and the relative magnitudes of N_{T1} , N_{T2} are unfavorable. If the above conditions prevail, then

$$N = \frac{N_{T1}}{\frac{1}{2} e^{(E_{T1} - E_{Fn})/kT} + 1} \quad (C.22)$$

Solving for E_{Fn}

$$E_{Fn} = E_{T1} - kT \ln 2 \left(\frac{N_{T1}}{N} - 1 \right) \quad (C.23)$$

and n_c is

$$n_c = \frac{N N_c}{2(N_{T1} - N)} e^{-(E_c - E_{T1})/kT} \quad (C.24)$$

or

$$\ln N_c = \ln \left\{ \frac{N_c}{2 \left(\frac{N_{T1}}{N} - 1 \right)} \right\} - \frac{E_c - E_{T1}}{kT} \quad (C.25)$$

In this case the slope of $\ln \sigma$ vs. $\frac{1}{T}$ is directly a measure of the depth of the trapping level below the conduction band. We note also that the intercept for $\frac{1}{T} = 0$ is dependent in either case upon the degree of excitation (N).

It is likely that N does not remain constant throughout the time that T is increased, and may change primarily when E_{Fn} is near a trapping level. This would suggest, then, that regions of $\ln \sigma$ vs. $\frac{1}{T}$, showing constant slope, are related to the average of two adjacent trapping levels. Also the breaks between regions of constant slope correspond to E_{Fn} values near the trapping levels, when N is changing. This situation is indicated in Fig. 39.

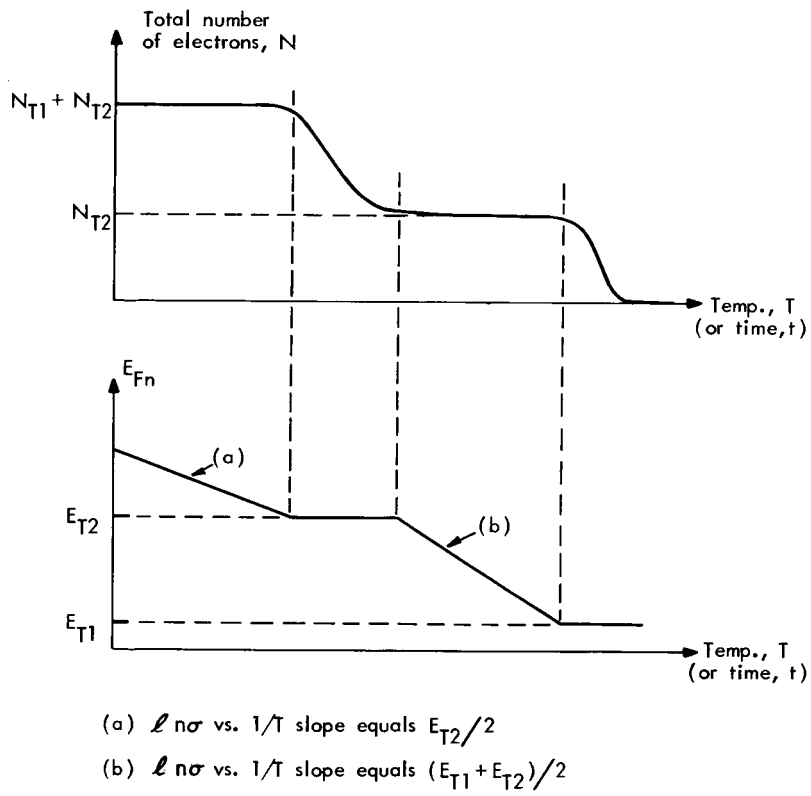


Fig. 39 Hypothetical Variation of Total Electron Density and Fermi-Level With Temperature

REFERENCES

1. Bube, R.H. Photoconductivity of Solids, John Wiley and Sons, 1960.
2. Dresner, J. and Shallcross, F.V., J. Appl. Phys. 34, 2390, (1963).
3. Zuleeg, R., Solid State Electronics 6, 645, (1963).
4. Miksic, M.G., Schlig, E.S., Haering, R.R., Solid State Electronics, 7, 39, (1964).
5. Kulp, B.A., and Kelley, R.H., J. Appl. Phys. 31, 1057, (1960).
6. Kallman, H., and Mark, P., Phys. Rev. 105, 1445, (1956).
7. Henisch, H. K., Rectifying Semi-Conductor Contacts, Chapter V, Oxford University Press, London, (1957).
8. Chopra, K. L., J. Appl. Phys. 36, 184, (1965).
9. Beam, W. R., and Armstrong, A.L., Proc. I.E.E.E., 52, 300, (1964).
10. Gajda, W.J., "Hole Conduction in Thin Films of CdS," SM Thesis, Mass. Inst. Tech., Cambridge, Mass., (June, 1965).
11. Gottling, J.G., and Nicol, W.S., "Double-Layer Interference in Air-CdS Films," to be published in J. Opt. Soc. Am.
12. Wright, G. T., J. Brit. IRE., 20, 337 (1960).
13. Aponick, A. A., Jr., "An Electron Microscopic Investigation of CdS Thin-Film Surfaces," M.I.T. Electronic Systems Laboratory Report ESL-R-229, (March, 1965).
14. Bube, R. H., Photoconductivity of Solids, p. 294, John Wiley and Sons, 1960.
15. Bube, R. H., J. Appl. Phys., 33, 1733 (1962).
16. Bube, R. H., J. Chem. Phys., 23, 18 (1955).
17. Randall, J. T., and Wilkins, M. F. A., Proc. Phys. Soc., A 184, 366, (1945).
18. Garlick, G. F. J., and Gibson, A. F., Proc. Phys. Soc., 60, 574 (1948).
19. Booth, A. H., Canad. J. Chem., 32, 214, (1954).
20. Hoogenstraaten, W., Philips Res. Rep., 13, 515, (1958).
21. Haering, R. R., and Adams, E. N., Phys. Rev., 117, 451, (1960).

REFERENCES (Continued)

22. Franks, J., and Keating, P. N., *J. Phys. Chem. Solids*, 22, 25, (1961).
23. Dittfield, H. J., and Voigt, J., *Phys. Stat. Sol.*, 3, 1941, (1963).
24. Nicholas, K. H., and Woods, J., *Brit. J. Appl. Phys.*, 15, 783, (1964).
25. Hensch, H. K., Rectifying Semiconductor Contacts, Oxford Univ. Press, 1957.
26. Ebner, G., "Capacitance Properties of a Cadmium Sulfide Thin-Film Diode," S.B. Thesis, M.I.T., May, 1964.
27. Cooper, M. S., "Variation of Differential Capacitance of Cadmium Sulfide Thin-Film Diodes," S.M. Thesis, M.I.T., August, 1965.
28. Bethe, H. A., "Theory of the Boundary Layer of Crystal Rectifiers," M.I.T. Rad Lab. Report, 43-12, 1942.
29. Goodman, A. M., *J. Appl. Phys.*, 34, 329, (1963).
30. Smith, R. W., and Rose, A., Phys. Rev., Vol. 97, p. 1531, (1955).
31. Muller, R. S., and Zuleeg, R., J. Appl. Phys., Vol. 35, p. 1550, (1964).
32. Shallcross, F. V., and Dresner, J., Solid State Electronics, Vol. 5, p. 205, (1962).
33. Muller, R. S., J. Appl. Phys., Vol. 34, p. 2401, (1963).
34. Zuleeg, R., Solid State Electronics, Vol. 6, p. 193, (1963).
35. Böer, K. W., and Kummel, U., *Ann. d. Physik*, 6, 303, (1957).
36. Kallmann, H., and Mark, P., *Phys. Rev.*, 105, 1445, (1957).
37. Bube, R. H., Photoconductivity of Solids, p. 292, John Wiley & Sons (1960).
38. Jenssen, H. P., "De-excitation of CdS Films by High Electric Fields," S. B. Thesis, Dept. of Elec. Engineering, M.I.T. (June, 1965).
39. Franz, W., *Ann. d. Physik*, 11, 17, (1952).
40. Lindmayer, J., *J. Appl. Phys.* 36, 196, (1965).
41. Kirov, K., and Zhelev, V., *Phys. Stat. Sol.*, 8, 431, (1965).

REFERENCES (Continued)

42. Henisch, H. K., Rectifying Semi-Conductor Contacts, Chapter V, Oxford University Press, London, (1957).
43. Chopra, K. L., Proc. IEEE, 51, 1242, (1963).
44. Chopra, K. L., J. Appl. Physics, 36, 184, (1965).
45. Beam, W. R., and Armstrong, A. L., Proc. IEEE, 52, 300, (1964).
46. McAfee, R. E., Current Flow in a Thin Film Cadmium Sulfide Diode, S. M. Thesis, M. I. T., (1963).
47. Litton, C. W., Reynolds, D. C., Phys. Rev., 133, A536, (1964).
48. Steele, M. C., Ando, K., and Lampert, M. A., J. Phys. Soc. Japan, 17, 1729, (1962).
49. Lampert, M. A., and Rose, A., Phys. Rev., 121, 26, (1961).
50. Rose, A., Phys. Rev., 97, 1938, (1955).
51. Spenke, E., Electronic Semiconductors, p. 293, McGraw-Hill, (1958).