June, 1966

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PART I
COMPUTER-AIDED ELECTRONIC CIRCUIT DESIGN

PART II
CONDUCTION PROCESSES IN THIN FILMS

Status Report

December 1, 1965 - May 31, 1966

Electronic Systems Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY, CAMBRIDGE, MASSACHUSETTS 02139

Department of Electrical Engineering

(PART I)

COMPUTER-AIDED ELECTRONIC CIRCUIT DESIGN

and

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ABSTRACT

Research in Computer-Aided Design of Electronic Circuits through use of time-shared computers has been pursued along several lines. The CIRCAL-1 circuit analysis computer program has been completed and is providing valuable insights to requirements for the more extensive program CIRCAL-2 which is in the planning stage. Several parts of the CIRCAL-1 program have been written in a way that will make them directly useful as CIRCAL-2 is developed. A low-cost graphical display unit has been devised and tested, and work on a digital-system simulation program has continued. The AEDNET scheme of network simulation is essentially complete and is undergoing evaluation.

Fundamental investigations pertinent to the long-term goal of achieving a thin-film solid-state analog of the vacuum triode have been conducted. Experiments with an aluminum-grid and cadmium-sulfide film combination have been made for the purpose of investigating isolation between structures. Techniques for establishing aluminum-grid formation over CdS film surfaces have also been investigated.

Research in the use of thin magnetic films for a computer memory that operates on the principle of coincident frequency sought to clarify the following matters: techniques for improving nondestructive readout signal-to-noise ratio, problems relating to pulse-writing, ability to obtain coincident frequency write-mode operation at radio frequencies, and performance characteristics of Nickel-Iron films.

J. F. Reintjes
Professor of
Electrical Engineering

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PART I

COMPUTER-AIDED ELECTRONIC-CIRCUIT DESIGN

A. CIRCAL DEVELOPMENTS

Professor M. L. Dertouzos
Mr. Charles W. Therrien,
Research Assistant

Development of the CIRCAL-1 circuit analysis programs has continued.[1] The most significant change has been the provision for current and voltage sources which may depend on a node-pair voltage. These are brought into the network in the same manner as independent sources. The voltage on which the source depends is identified by specifying the appropriate nodes. The library of source functions has been augmented to include, as standard waveforms, impulse functions and exponentials in addition to the step functions and sinusoids previously available. Further, new branch elements have been permanently added to the system. These are the diode, the zener diode, and the tunnel diode. Previously only one of these types could be incorporated into any particular circuit.

Most recent work has been directed toward modification of the CIRCAL-1 programs to make them compatible with peripheral programs developed by other members of the project. In particular, machinery has been set up that allows one to call upon programs which enable the user to describe nonlinear resistors and include them in the circuit being analyzed.

In addition to this work on CIRCAL-1, time was spent on the design of the next generation of circuit analysis programs, CIRCAL-2. Conferences with circuit designers have provided considerable data regarding features that would be desirable for the new system. In the light of these requirements a new method of simulation seems desirable and is being considered.

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[1] See "Computer-Aided Electronic Circuit Design," December 1965, Status Report ESL-SR-256; also, M. L. Dertouzos and C.W. Therrien, "Circal: On-Line Analysis of Electronic Networks," Report ESL-R-248, Electronic Systems Laboratory, Massachusetts Institute of Technology, Cambridge, Massachusetts, October 1965.

B. ON-LINE DESCRIPTION OF NEW ELEMENTS

Professor M. L. Dertouzos
Mr. C. W. Therrien,
Research Assistant

A compiler has been developed to permit expansion of CIRCAL by enabling the inclusion of memoryless nonlinear elements, nonlinear capacitors and inductors, and arbitrary voltage and current excitations.

The technique consists of a method of compiling on-line descriptions of arithmetic expressions that are of the general form $G = f(x, y, z)$, where G is a single-valued function of variables $x, y,$ and z. The maximum number of variables in the expression can be increased from three to any size by a simple extension.

The standard precedence grammar of algebra is employed, thus making a form of bounded context translation possible. In this translation, action to be taken is determined solely by the symbol currently being scanned, and at most three symbols to its left.

The compiler generates its output in the form of two tables. The first contains a set of integers that specifies a sequence of arithmetic operations to be executed. Among these arithmetic operations are addition, subtraction, multiplication, division, exponentiation, and negation. The second table contains the numerical values to be used when the operations are to be performed. Execution is accomplished by successively performing these arithmetic operations until the tables have been exhausted.

An engineer using the CIRCAL programs uses the compiler feature as follows: Suppose a diode is needed which has exponential characteristics between -0.3 volt and +0.5 volt, looks like a current source for voltages less than -0.3 volt, and looks like a linear resistor of 50 ohms for voltages greater than +0.5 volt. The engineer would give the command "Define DIODE" and then type the algebraic expressions and break points defining the diode. The result is a new circuit element called DIODE which could be inserted at will into any circuit that the engineer is simulating.

The compiler programs were written so that they are completely independent of the CIRCAL programs. Hence the compiler which is presently compatible with CIRCAL-1 will also be compatible with CIRCAL-2 no matter how different the new circuit analysis program may be.

C. INPUT-OUTPUT PROGRAM FOR CIRCAL

Professor M. L. Dertouzos
Mr. G. A. Walpert,
Graduate Student

In order for a computer-analysis program to be useful, means must be available to input the relevant data and to output the results. This work allows the user to display the results of on-line circuit analysis through the Project MAC system on a remote teletype, IBM 1050 typewriter, or the ESL display console. A second part of the work enables the user to input a piecewise-linear function of one variable, on-line, through the ESL display console.

Output capabilities allow up to three voltages to be plotted versus time on a single graph or to have one voltage plotted against another with time as the independent parameter. The voltages are single-valued functions of time although the result of plotting two voltages in quadrature may be multivalued. There is no restriction on the magnitude of the voltages except that they must be representable in the computer. For any physical problem this restriction is certainly satisfied.

Although the programs have been designed for use with CIRCAL, they are independent and have also been used in distributed system design. See Section E.

One advantage of these programs, in addition to their ability to plot many curves simultaneously, is the comparatively high speed of the typewriter outputs. The use of the typewriter tabulate command substantially reduces the time required to produce a completed graph. Typical time for a sixty-line plot is three minutes.

Since tabulator stops cannot be programmed, tabs on the IBM 1050 must be manually set fifteen spaces apart to be compatible with the plotting procedures. Tabs on the teletypes are preset by the manufacturer to 15. The first 15 spaces of each line, the space to the first tab, are used for a coordinate if one is printed, and the remaining 65 spaces of the data field are used to plot data points. The graph of one voltage versus another uses a grid sixty divisions square while the graph of voltage versus time uses sixty divisions in the vertical direction and a number of lines equal to the number of time points in the horizontal direction.

To facilitate reading the graph, coordinates of the form of an integer times a power of ten are provided. In addition, if the value zero is in the range of the data plotted on the vertical axis, the vertical scale is shifted until the zero line coincides with one of the vertical coordinates. The graph of one voltage versus another has the parameter (time) indicated in at least ten places. This allows a user to follow a complicated plot and to determine in which direction the curve is going and how rapidly.

The displays on the ESL console provide a fine-grain grid structure and have the data points connected by straight lines to form continuous curves. In the case where more than one curve is displayed or, if one voltage is being plotted against a second, the curves are labeled to indicate the voltage being plotted or the starting point of the trajectory. Some representative plots are shown in Figs. 1 and 2.

The input procedure gives the user great flexibility in describing piecewise linear functions. After choosing the range of values on the horizontal and vertical axes, he uses the light pen to position the tracking cross at the various breakpoints of his curve. In case of error, there are provisions to restart the entire process, to remove the last breakpoint, or to change the location of any breakpoint.

D. ON-LINE GRAPHICAL DISPLAYS

Professor M. L. Dertouzos
Mr. H. L. Graham,
Research Assistant

An experimental prototype of an on-line graphical display system, intended for use at a remote station of a time-shared computer facility, has been designed, constructed, and tested. This system uses

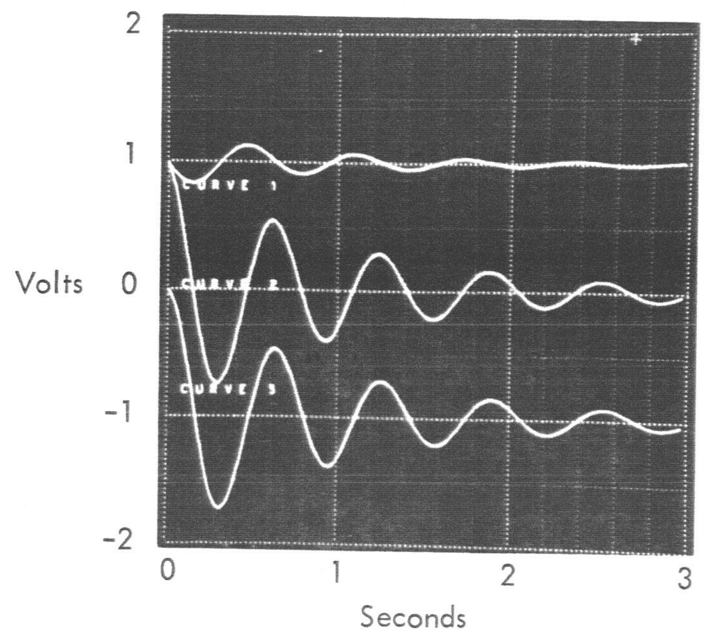


Fig. 1 Simultaneous Display of Three Network Voltages

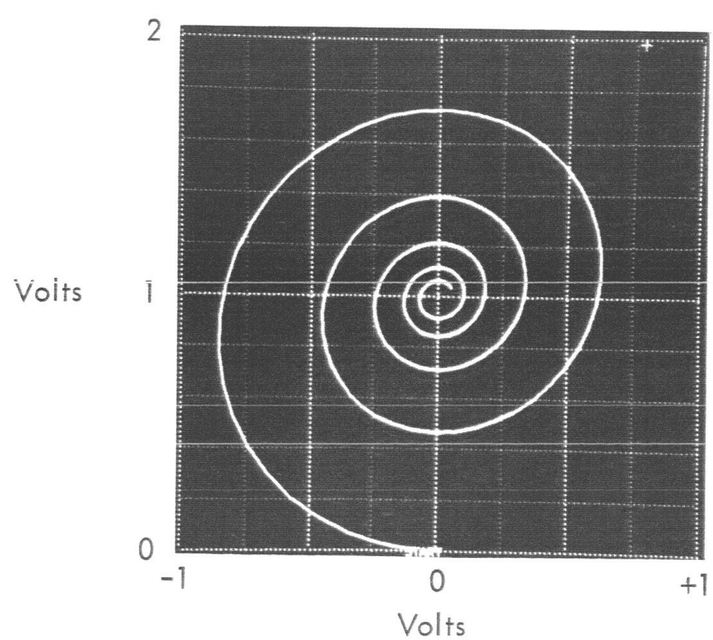


Fig. 2 Plot of One Network Voltage versus Another

a parametric technique based on the control of exponential curve segments. A complex curve is composed of the minimum number of such segments that achieves the prescribed fitting error. Such a technique permits a compact description of graphical data.

The experimental prototype uses a storage-type cathode-ray tube (CRT) for visual display. The CRT is driven by two waveforms, $x(t)$ and $y(t)$, which are the outputs of linear networks T_x and T_y. These networks are characterized by their respective step responses $T_x(t)$, $T_y(t)$, and are constrained to have unity steady-state gain. Each computer command supplies a set of coordinate values which, after being converted to analog signals, are used to drive T_x and T_y. A third portion of each computer-command controls the parameters of T_x and T_y. A curve segment is plotted as follows.

Assume that at some time, t_k, the linear networks have attained steady state, such that $x(t_k) = x_o$ and $y(t_k) = y_o$, and at this time the computer supplies a new set of coordinates $(x_o + \Delta x,\ y_o + \Delta y)$. The signals supplied to the CRT will then be

$$x(t) = x_o + \Delta x T_x(t-t_k)$$

$$y(t) = y_o + \Delta y T_y(t-t_k)$$

resulting in a displayed curve segment starting at point (x_o, y_o) and ending at $(x_o + \Delta x,\ y_o + \Delta y)$. The particular trajectory, $f(x, y) = 0$, between these two points will depend upon the parameters of T_x and T_y. Through proper choice of T_x and T_y, a large class of curve segments can be drawn between any two points on the scope by controlling the parameters of T_x and T_y.

The major criteria used in selecting a realization for T_x and T_y were

1. It should provide a large and varied family of segments,
2. It should have the ability to match slopes of connecting segments,
3. It should have a configuration which can be reliably implemented.

The chosen realization is given by

$$T_x(t) = \{1 - [a_x e^{-\sigma_o t} + (1 - a_x) e^{-\sigma_x t}]\}, \quad t \geq 0$$

$$T_y(t) = \{1 - [a_y e^{-\sigma_o t} + (1 - a_y) e^{-\sigma_y t}]\}, \quad t \geq 0$$

under the constraints

$$\leq \quad 0 \leq a_x \leq 1 \qquad \sigma_x < 1 \rightarrow \sigma_y = 1 \qquad \sigma_x > \sigma_o, \ \sigma_y > \sigma_o$$

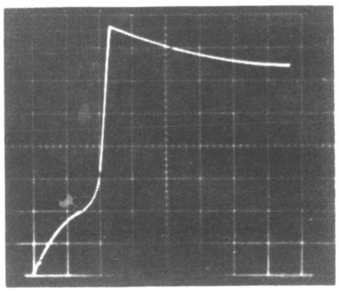
$$0 \leq a_y \leq 1 \qquad \sigma_y < 1 \rightarrow \sigma_x = 1$$

This realization has four degrees of freedom; two degrees for determining steady-state coordinates, one degree to specify final slope, and one degree to yield a family of segments having that slope. The exponential time response results in an economical implementation.

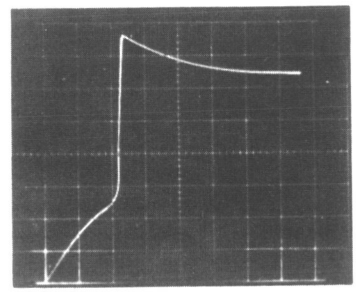
A software translator was written to convert a desired curve from a point-by-point description to a series of curve segments realizable by T_x and T_y. A given curve to be plotted is matched within a given maximum allowable error using the minimum number of segments necessary. Wherever possible, slopes of connecting segments are matched.

For testing purposes the prototype hardware and translator software were used in connection with CIRCAL-1. It was found that the step response of a simple tunnel-diode circuit, computed by CIRCAL at 100 points, can be displayed by means of three to five segments, depending upon the desired fit. The circuit analyzed and the response plotted using first three then four curve segments are shown in Fig. 3.

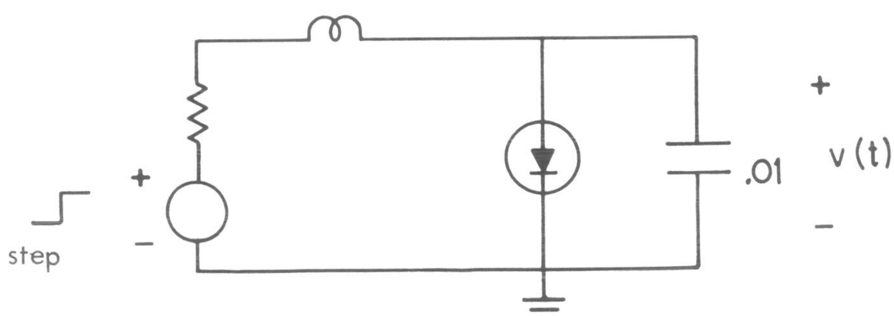
The main feature of this display technique is the utilization of few computer words for the display of a complex curve. Advantages resulting from this feature are small storage requirements for the translated curves and a relatively fast display time. The main penalty is the computational effort necessary for translation of a given curve into appropriate display commands.



a) Response plotted using 3 segments



b) Response plotted using 4 segments



c) Tunnel diode circuit

Fig. 3 Response of Tunnel Diode Network Plotted Using the On-Line Graphical Display

E. COMPUTER-AIDED DISTRIBUTED SYSTEM SIMULATION

Professor M. L. Dertouzos
Professor L. A. Gould
Mr. C. N. Taubman,
Graduate Student

Many engineering systems can be expressed and analyzed in terms of electrical analog-distributed models. The modelling process involves two steps. First the system-defining differential equations are determined, and then an equivalent electrical network characterized by the same equations is generated. Work has focused on linear bilateral flow processes. Typical examples of these are countercurrent heat exchangers and fixed-bed reactors. The objective of this research has been to develop software for the on-line analysis of these network models.

The electrical analog for these systems is a finite cascade of identical, linear RLC cells, connected through isolation amplifiers. The electrical isolation results from neglecting physical diffusion in the model development, but it can be shown that proper selection of the number of cells to some extent compensates for this.

A set of programs has been developed that allows topological description of the electrical model, analyzes the system, and provides output in graphical or tabular form. The solution method takes advantage of the properties of symmetry and isolation present in these models. The analysis of a typical distributed system proceeds as follows. The user, seated at a remote terminal of a time-shared computer, describes to the computer the basic cell configuration, the number of cells in the model, and the external boundary conditions. Computer simulation now commences, with each cell being treated as an independent input-output problem.

The analysis algorithm is intended to imitate the physical process. For each time interval, a spatial distribution of input potentials to each cell is assumed and the corresponding output potentials are computed. The output potentials are taken to be the input potentials to the adjacent cells, and the entire process is repeated in an iterative manner until the magnitude of the differences between adjacent input and output values for all cells is less than a specified small number. It has been proven analytically that this iterative method is convergent for the special cases of two and three cascaded cells.

When convergence is reached, the output potentials are stored in arrays for use by the output programs.

There are four types of output presently available. For any specified time point, the spatial distributions of voltage may be either printed in tabular form or plotted on the typewriter or the display console. In addition, the time response at any electrical node in the model may be printed or plotted.

The programs accept systems consisting of as many as 50 cells, each of which may contain up to 20 linear elements and sources. External sources must be sinusoidal or step-voltage sources. A provision for two internal current sources (at any node) also exists. Analysis for as many as 1000 time points is permissible, although a maximum of 50 points in time (uniformly spaced over the analysis interval) are stored.

The simulation method used here is similar to that of CIRCAL. However, the individual subroutines are specifically designed to utilize in an optimum way the characteristic symmetry and isolation properties of the models being simulated. At present, the severest limitation is the restriction to linear systems. The intention has been to treat bylateral systems, since unilateral systems may be considered to be a special case of the former.

The programs have been used to calculate temperature responses in a counter-current heat exchanger with conducting walls. Transient temperature gradients closely approximate the physical wave-like behavior, and the steady-state time response is within two percent of the exact value, as determined by analytical techniques. Computation time, for a system comprised of 15 cascaded cells with 9 RC elements per cell is less than 25 seconds. As might be expected, time to convergence decreases as a steady-state value of the solution is approached.

F. DIGITAL-SYSTEM SIMULATION

Professor M. L. Dertouzos
Mr. Paul Santos, Jr.,
Research Assistant

Work on the Digital Simulation System is being continued.[2] The core of the simulation routines was completed and tested on a small system. Further work was done in designing the overall system structure, reworking part of the data structure, and documenting the work already done.

The "core" routines are the group that, when given an array of input values, identification of block class, and an array in which to store the results, will iterate the block function through one time cycle at all levels. The new inputs and previous states are used to compute the new states. Any logical errors are reported as they occur. At present these routines are equipped to handle only standard blocks and wrapped-up structures with single-line inputs. (See Section G). However, specific planning has gone into the work so that the addition of the capability to handle user-defined blocks and "bundled" signal lines is straightforward and will require no change in the already existent system.

The sample block diagram used to check out the core routines was a scale-of-three counter using two-level flip-flops, four delays, and seven gates. A dummy main program was written to call on the core routines in the proper repetitive fashion with a square-wave input. When simulated, the counter did not appear to operate correctly, and it was found that a mistake in the logical design of the counter had been made and a fifth delay had to be included in the counter to make it operate as desired. The above experiment, though somewhat crude, provided a startling example of the usefulness of such a simulation.

The overall system is organized into an on-line command-type structure with three main subsystems. These three subsystems deal with the graphical input of block diagrams, the on-line definition of

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[2] See "Computer-Aided Electronic Circuit Design," Status Report ESL-SR-256, December 1965.

special blocks and input signals, and the actual simulation and debugging of the digital system specified by the first two. The portions completed to date are the core routines for the third part and the master program to control the entire process of block definition, block diagram description and wrap-up, and simulation.

The data structure has been modified slightly to better accommodate the "defined" type blocks and "bundled" blocks, while remaining as efficient as possible for standard operation.

An explanation of the purpose and general concepts of the system has been written and is forthcoming.

G. GRAPHICAL INPUT-OUTPUT FOR DIGITAL SYSTEM SIMULATION

Professor M. L. Dertouzos
Mr. J. Gertz,
Graduate Student

A companion part of the preceding task consisted of the design and implementation of a computer program that allows arbitrary digital systems to be described to a computer in a graphical manner.[3] The system is drawn in block-diagram form on the screen of the ESL Display Console through the use of program-controlled interrupt buttons, a light-sensitive pen, and a set of program-controlled passive inputs (shaft encoders, digital switches, and toggle switches). The blocks of the diagram may range in detail from an individual gate to a complete digital subsystem.

Concurrent with the formation of this display, a comprehensive data structure is established within the computer which stores all classification and topological information contained in the display. The structure is built in the form of an interconnected string-pointer list. When this list is completed, the data within it can be used by the accompanying simulation programs (see preceding section) to analyze the overall system behavior.

An attempt has been made to minimize as much as possible the number of un-natural actions the engineer is required to perform when

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[3] See "Computer-Aided Electronic Circuit Design," (Status Report ESL-SR-256) December 1965.

using this program, specifically:

1. No programming ability of any kind is required.

2. No artistic talent is required to draw a neat diagram.

3. The display is in standard block diagram form, so the engineer speaks to the computer in his own graphical language.

The program defines a number of common digital elements to be standard objects. These are the six common logic gates (AND, OR, NOT, NAND, NOR, EXCLUSIVE OR), the various types of flip-flops (complement, set-reset, combination), delays, and lead junction boxes or fanout points. Each of the standard objects is accorded the following special treatment:

1. It has a unique, easy to recognize symbol.

2. It may be oriented in any direction.

3. It has individual buttons assigned to it to minimize the necessary man-machine interaction.

All an operator need do to plot one of these objects is position the tracking cross correctly on the screen and push the appropriate button (or buttons). Any block that the designer wishes to use in his system diagram that is not a standard object must be explicitly defined by him. The program gives him two alternative methods of doing this: Either he can draw a block diagram of the object using standard objects and previously defined non-standard ones, or he can give a suitable input-output description of the block. If the first method is used, the resulting block is denoted as a "wrapped-up" element. The wrap-up feature allows the engineer to test his system in small units and to use nesting of definitions.

Once a new element has been defined, it may be called by name at any future time, since the program "remembers" what has already been defined. Furthermore, the internal structure of a wrapped-up element may be viewed at any time, while the truth table of a defined combinatorial element or the transition table of a defined sequential element can be printed out when requested.

The blocks of the diagram can be interconnected by the operator through use of the light pen. Each lead may have any number of segments, each of which may be placed and oriented as desired. Thus the operator can reproduce his pencil picture exactly on the screen. Perfect pen positioning at the ends of lines is not required, as lines are made to latch automatically to the correct picture parts. Should the designer make an error while building the display, or should he change his mind, he may delete any line or object on the screen, this is done simply by pointing the pen at the incorrect part. Also, if the block-diagram is too large for the screen, the display may be translated out of the visible region, thereby creating more room for drawing. That is, the display acts like a "window" through which a large drawing is viewed.

During the time the engineer is creating the display, inputting instructions are being given to him via the teletypewriter. This action relieves the engineer of the necessity to read an instruction manual while he is using the system, thereby reducing the expected number of errors. When an operator becomes sufficiently familiar with the program, he can reduce the long instructions to short hints by actuating an appropriate push button. In addition, should the operator perform an action which cannot be correct at that time, an error message is printed out which tells him the error he made and how he is to proceed.

Several logic diagrams have been inputted using this program, all successfully. The average amount of computer time required to complete these diagrams is twenty to thirty seconds.

H. THE AEDNET PROGRAM

Dr. J. Katzenelson,
Staff Member
Mr. D.S. Evans,
Research Assistant

AEDNET is a system of digital computer programs for simulation of nonlinear electronic circuits. It takes maximum advantage of the similarities between resistive nonlinear networks (where the pertinent variables are voltage and current), inductive networks (where the pertinent variables are flux linkage and current) and capacitive networks (pertinent variables are charge and voltage) to arrive at an approach to the solution of nonlinear RLC networks. Through use of this approach, devices with a variety of types of nonlinearities can be included in the networks to be analyzed.

The system has two main features: (1) the ability to simulate the behavior of a wide class of nonlinear networks, (2) the on-line use of a digital computer and its oscilloscope display unit for on-line interaction. AEDNET is written in AED-0 language and it operates on the Project MAC Time-Sharing Computer and the Electronic Systems Laboratory display unit.

AEDNET simulates networks whose elements are nonlinear time-varying capacitors, resistors, inductors, and dependent and independent sources. The network is required to satisfy certain topological conditions and the elements' characteristics are required to satisfy suitable Lipschitz conditions. Nonlinear characteristics are represented in the computer either by a table or a subroutine. Elements with non-monotonic characteristics are allowed and elements' characteristics are required to be continuous but not differentiable.

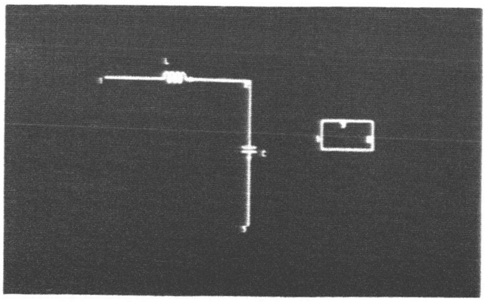
At the time when the last progress report (ESL-SR-256) was written the system existed as two separate parts: the analytic part or the part which calculates the network response, and graphical part. The two parts were connected together and the system was given the name AEDNET. The complete system has been operating for the last five months. The work during this period was characterized by extensive introduction of modification and improvement which were based on experience gained while using the system. The introduction of various improvements demonstrates the advantage of the modular structure of the system discussed in a previous memorandum (ESL-SR-245) — changing a module was a rather straight-forward task and the knowledge of the interface between modules ease the debugging considerably.

Improvements in the analytic part include the storage system, fast multiplication subroutines, and an addition of a variable step integration formula. To the graphical part we added a completely new feature — the device.

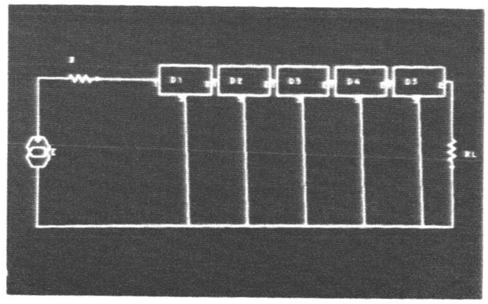
The device is a way of summarizing network information by giving it another name. Thus the device's function in a description of a network is similar to the procedure (subroutine) in writing programs. It also has some special value to AEDNET. The nonlinear capability of the system is achieved by defining some basic generalized elements. This implies that a diode, for example, is considered by the analysis part of the system as a nonlinear resistor. The user however would like to call a diode "a diode" and to address it by a "diode" symbol. This is done by defining a subnetwork with an appropriate resistor, giving it a "diode" symbol, and using the newly-created device as a new element.

To the command system we introduced two major features: complete error checking and the stacking of command. The purpose of the first feature is to insure 'fail safe' in case of human operator errors. The second feature saves computer time by eliminating unnecessary core swaps and thus speeds up the response considerably.

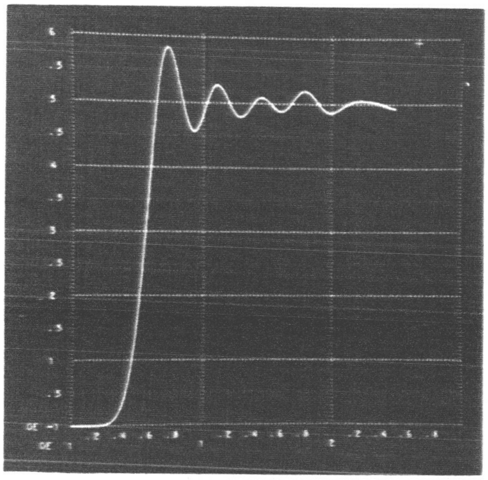
The following is an example of the use of AEDNET. Illustrated in Fig. 4 is a feature recently introduced into the system -- the use of "devices". It includes the ability to define a subnetwork, give it a special symbol, and use the result as a new network element in the construction of larger networks. Figure 4(a) shows a single L-section filter network after it was defined and assigned the three-terminal symbol which is shown to the right of the network. The number indicates the correspondence between the network nodes and the symbol's poles. This filter section is now connected to make the larger filter of Fig. 4(b) which is terminated by appropriate resistors and tested by a step input. A calculation of the response is now requested. The output voltage across R_L is given in Fig. 4(c), the input current in Fig. 4(d), and the 'flower' of Fig. 4(e) is the output voltage as the function of input current.



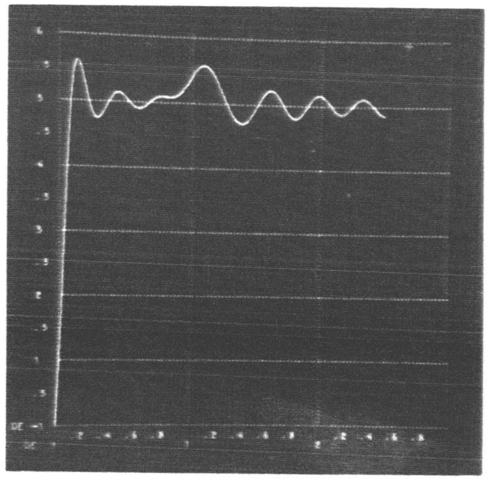
(a) A network and its equivalent "device"



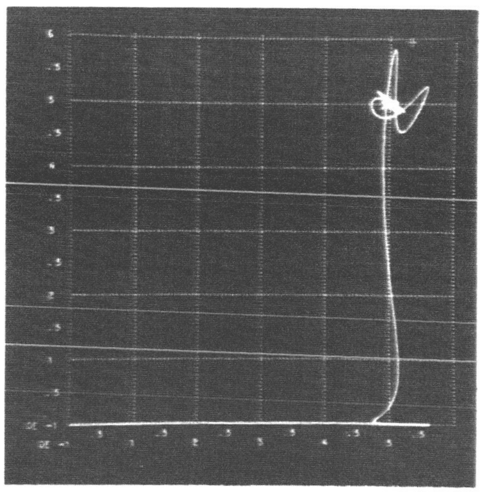
(b) A filter made up of the devices of (a)



(c) Output voltage in response to a step input



(d) Input current



(e) Output voltage as a function of input current

Fig. 4 An Example of the Use of AEDNET

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MOTION PICTURE

CIRCAL: Computer-Aided Electronic Design, January, 1966.

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Computer-Aided Electronic Circuit Design, Status Report ESL-SR-225, December, 1964.

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PART II

CONDUCTION PROCESSES IN THIN FILMS

CONTENTS

A. STUDY OF CdS THIN-FILM VACUUM ANALOG TRIODES

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Research during the previous six-month period had shown that the problem of isolation of the grid structure from the CdS film evaporated over it could be solved through use of an aluminum grid. Gold grids, which had been studied extensively, could be isolated from the underlying CdS film either by subjecting the CdS film surface to an oxygen-glow discharge, or by diffusing an evaporated layer of sulfur into the film. The difficulty with the use of gold as grid material is that it usually forms an electron-injecting contact for a CdS film evaporated over it. An aluminum grid, on the other hand, is readily oxidized to provide insulation from the overlying CdS film. Although an aluminum grid had been formed after evaporation of the aluminum over an untreated CdS film surface, grid formation had still to be verified over treated surfaces.

During the six-month period just ended, a study was made to establish aluminum-grid formation over CdS film surfaces either subjected to an oxygen-ion glow discharge or into which an evaporated layer of sulfur had been diffused. It was found that grid annealing must be commenced as soon as possible after the evaporation of the aluminum film in the case of the CdS film surface exposed to oxygen glow discharge. This, however, is limited by the thermal time lag of the substrate radiation heater. The effect is attributed to the formation of aluminum oxide from absorbed oxygen in the CdS film which then stops the grid formation. It was established that grids can be successfully formed on sulfur-treated surfaces. The detailed structure of these grids was not studied since the examination was limited to the use of a metallograph (Seitz, 2000 x), rather than an electron microscope. Electrical continuity between emitter and collector, still with isolation between emitter and grid or collector and grid, substantiated the optical observations that a grid was formed. Further details of this research are given in the following thesis:

"The Fabrication of Thin-Film Triodes," Stephen N. Teicher, S.B. Thesis, M.I.T., June, 1966.

Although the main purpose of this research was to establish the formation of the isolated aluminum grid, brief studies of the surface resistivity of the CdS films used in the grid investigation and of the role of impurities in the CdS evaporant were also made in the course of the work. The electrical-conduction properties of the evaporated CdS films are described in detail in a forthcoming report.[1]

As a result of this work, it is planned to investigate complete triode structures utilizing aluminum grids. It is also considered that a study of the initial growth of CdS films during evaporation as opposed to post-evaporative treatments of glow-discharge, annealing, sulfur or copper diffusion, and recrystallization, would be worthwhile areas of research.

B. A COINCIDENT-FREQUENCY MEMORY USING THIN MAGNETIC FILMS

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The objective of this research is to demonstrate the application of radio-frequency drive-field techniques to the obtaining of a coincident-frequency, non-destructive readout memory which uses thin magnetic films. The technical background of this work was given in the preceding status report, ESL-SR-256. As described in that report successful nondestructive readout (NDRO) has been obtained. The direction of the magnetization of a film is either the 0° or 180° phase of the sum frequency component (60-Mc/s) resulting from driving the film in a

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[1] Gottling, J.G., Nicol, W.S., "Electrical Conduction Processes in Thin Films of Cadmium Sulfide," Report ESL-R-272, in preparation.

rotational, non-switching mode with coincident 20-Mc/s and 40-Mc/s magnetic fields in the hard-axis direction.

Research in the past six-month period has been conducted on (a) improvements in the nondestructive readout signal-to-noise ratio, (b) pulse write mode experiments, (c) r-f write mode experiments, and (d) magnetic film evaporation.

1. Improvements in the NDRO Mode Signal/Noise Ratio

No experimental difficulties had been found with the nondestructive readout mode in observing the two phases 0° and 180°, of the 60-Mc/s component frequency, associated with the two saturated states of magnetization. It had also been clearly demonstrated that the stored information was not disturbed by the readout technique. There remained an amplitude difference in the two phases, however. This was traced to 20-Mc/s and 40-Mc/s ground-plane currents which were not orthogonal to the sense line, so that their associated magnetic fields had components which linked the sense line. The presence of any slight distortion of the 20-Mc/s or 40-Mc/s drive signals, having a 60-Mc/s component would, therefore, appear as noise in the sense amplifier output. This noise signal was superimposed on the readout signals. The noise signal by itself was easily observed by preventing the film magnetization from rotation by being clamped by a strong d-c field. We have now eliminated this noise by experimenting with several configurations of drive lines and ground planes. These have included the use of double-shielded stripline (two parallel ground planes, one on each side of the stripline), folded stripline (no ground plane used — the current return path being a parallel stripline of the same width as the drive line), and a single-shielded stripline (having a single-ground plane). Lines of 20 mils and 40 mils in width have been tried. The use of a single-shielded stripline 20 mils wide has enabled us to increase the signal/noise ratio to between 40:1 and 60:1. Through elimination of all 60-Mc/s distortion in the 20-Mc/s and 40-Mc/s drive signals, this ratio could be increased further. The improvement has allowed us to observe that:

(a) The 60-Mc/s signal amplitudes are the same for both phases of magnetization saturation, with an exception which is discussed below.

(b) The earth's cancelling field can be removed without disturbing the readout signal.

(c) Readout drive signals at least as low as 30 mA, peak-to-peak amplitude of both 20-Mc/s and 40-Mc/s will give discernible 60-Mc/s output signals of opposite phase. This is shown in the photograph of Fig. 1(a). Figure 1(b) shows a typical sense-amplifier output signal for a 150 mA (peak-to-peak) drive signal.

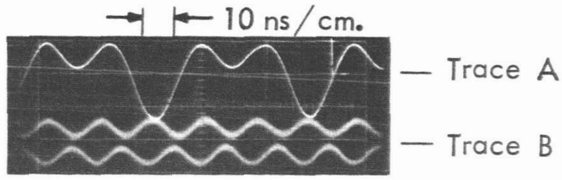
(d) Nondestructive readout can be obtained from films which are in a demagnetized or partially magnetized state, the signal amplitude being a function of the resultant magnetization.

(e) Nondestructive readout can be obtained from films having a large range of values for the angular dispersion of the easy axis. As measured by the Crowther technique, the angle within which 90 percent of the normal distribution of the easy axis lies, α_{90}, varied between 1° and 10°. These films had both square and skewed 1000 c/s hysteresis loops along the easy axis.

For observation (a), the output amplitudes are the same for films which have been demagnetized and then saturated by a field along the easy axis not greater than, by an order of magnitude, the coercive force H_c. However, it has been found possible to induce a difference in amplitude of the two phases by applying a strong magnetic field of approximately 100 oersteds, so that the film assumes slight unidirectional, rather than uniaxial, properties. The mechanism responsible is not yet known.

2. Pulse-Write Experiments

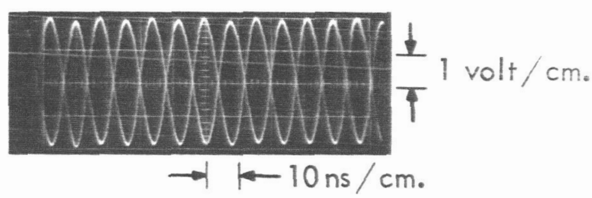
Coincident pulse-write experiments have been made using up to 1.2-amp pulses of width 80 nsec to 1 μsec, in the transverse (hard axis) direction and using longitudinal (easy axis) pulses up to 160-mA amplitude and of width $\geq$ 300 nsec overlapping the transverse pulses. Twenty-mil wide striplines with a single ground plane were used. Measurements were made of the amount of film switched, as given by the readout signal amplitude, both for the coincidence of a single



Trace A: Combined drive signal, 20 mA/cm. Vertical

Trace B: Sense amplifier output for both states of magnetization. 0.1 volts/cm. Vertical

(a) Nondestructive readout from 500-Å film with 30 mA, peak-to-peak, 20-Mc/s and 40-Mc/s readout drive signals.



(b) Sense amplifier output from 1000-Å film with 150 mA, peak-to-peak, 20-Mc/s and 40-Mc/s readout drive signals.

Fig. 1 Nondestructive Readout Signals

pair of pulses and for the concidence of a train of several hundred thousand pulses. The latter gives the inner boundary of the region of creep as described in report ESL-SR-256. Mapping the switching asteroid (critical switching curve) showed:

(a) there is an apparent skew of the hard axis much larger than that measured at 1000 c/s in that a reversal of the transverse-axis current polarity, as well as that of the easy axis-current polarity, is necessary to switch the magnetization from one saturated state to the other.

(b) the large apparent skew results in films switching from a saturated state (induced by a strong applied d-c field) back to the same state, even when the easy-axis steering pulse should theoretically reverse the magnetization.

From the model of a uniformly distributed current in a strip-line, the applied fields should be sufficient to give total magnetization reversal in regions where only slight reversal takes place. This implies that the actual applied fields are much smaller due to eddy currents or to time-dependent effects as considered by Edwards,[2] to demagnetizing effects,[3] or to an incorrect assumption of uniformly distributed currents in the striplines.[4]

(c) thresholding could not be obtained for field pulses. Thresholding is the condition in which a single transverse field pulse H_T in association with a longitudinal (bit or steering) field pulse H_L will produce switching of the magnetization, whereas $H_T/2$ in association with H_L will not disturb the magnetization, even after many pulses. However, a bipolar pulse for H_L (two pulses of opposite polarity applied in succession) at the same time as H_T was not tried, although this method is believed to eliminate, or at least reduce, the effect of creep.

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[2] J. G. Edwards, Proc. Inst. Electrical Engineers (Brit.), Vol. 112, No. 6, (June, 1965).

[3] H. J. Kump, I.B.M. Journal, March 1965, p. 118.

[4] H. J. Gray, IEEE Trans. EC-13, 576 (1964).

3. R-F Write Experiments

We have obtained coincident frequency r-f write-mode operation for several continuous sheet 500 A films, provided a simultaneous small d-c bias field (0.35 œ) is applied in the longitudinal (easy) axis direction in which the magnetization is switched. These films have typical coercive force values:

$$H_c = 2.1 \text{ œ}$$

$$H_k = 2.8 \text{ œ}$$

Values for the angular dispersion of the easy axis range from $\alpha_{90} = 1^\circ$ to $\alpha_{90} = 5^\circ$.

Coincident writing occurred under the following conditions:

(a) signals of 200 mA, peak-to-peak, and of frequency of 20-Mc/s and 40-Mc/s applied, in phase, to two separate transverse (hard axis or word) drive lines,

(b) at least 400 mA, peak-to-peak, 20-Mc/s signal applied to the longitudinal (easy axis, or sense/bit) line, 90° or 270° out of phase from the transverse 20-Mc/s current.

(c) a 0.35 œ d-c bias field applied from external Helmholtz coils along the easy-axis direction.

Under (a), (b), and (c), full switching of the magnetization was found. If only one signal in (a) together with both (b) and (c) was applied, no switching took place. If the phase was not within $\pm 20^\circ$ of the 90° phase condition, again no switching occurred. From the simple theoretical model, this phase condition for coincident switching should be 0° or 180°.

Figure 2 shows the theoretical applied magnetic-field pattern traced during the write mode. It has also been found that transverse 20-Mc/s and 40-Mc/s drive signals, 100 mA, peak-to-peak, can be used for both readout and coincident r-f writing. The easy-axis 20-Mc/s current has then to be increased to 800 mA. The d-c bias field must, however, be applied in all cases of r-f write we have tried thus far. The reason for this is as yet unknown.

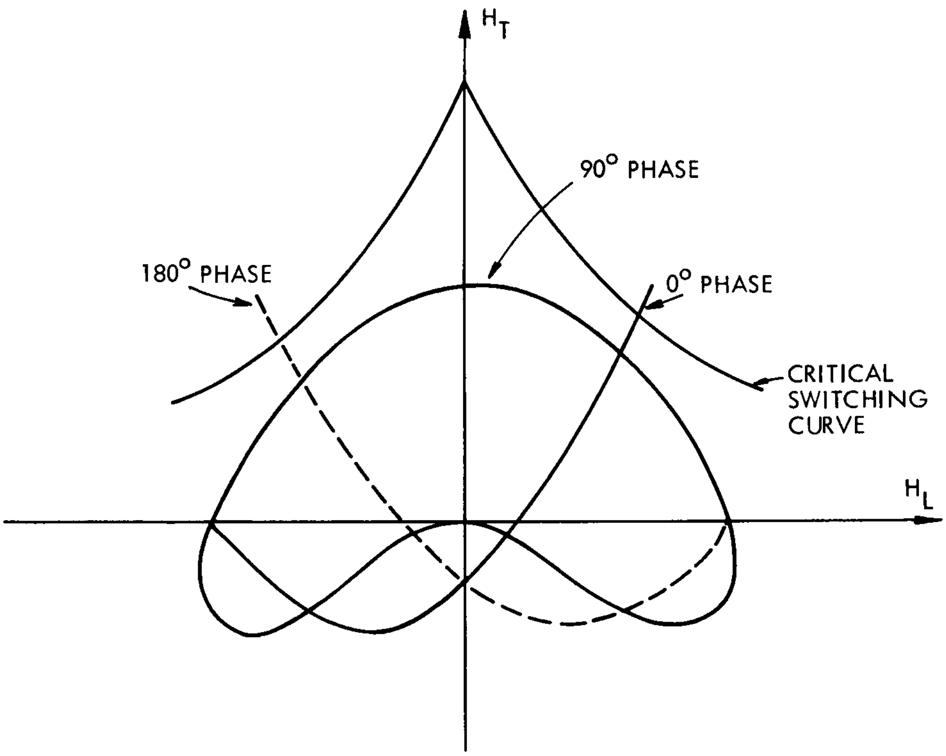

Fig. 2 Locus of Resultant Applied Field for R-F Write

4. Ni-Fe Film Evaporations

We have continued to make experimental evaporations of 81:19 Ni-Fe films in the thickness range 200 Å to 1000 Å. The substrate temperature is maintained at 350°C during evaporation, which has resulted in films of lower H_k than previously. Masked evaporation of 10-mil, 20-mil, 40-mil wide strip films have also been carried out, but a comparison of their memory properties has not been completed. Dispersion values as low as $\alpha_q = 0.4°$, and $\alpha_{90} = 1°$ have been obtained, although values of $\alpha_q = 2°$ and $\alpha_{90} = 4.5°$ are typical.

We have evaporated multilayer films consisting of 250 Å Ni-Fe at 200°C substrate temperature, 50 Å Cu or Al, at room temperature, and 250 Å Ni-Fe, at 200°C substrate temperature. These did not have the expected improved creep properties, however.

5. Future Investigations

That coincident r-f writing is possible for a few films, and that nondestructive readout has been obtained for many films of varied properties (low and high dispersion, square and skewed 1000 c/s hysteresis loops along the easy-axis) are encouraging. However, the following areas require a much fuller investigation:

(a) the reasons for the existence of an induced unidirectional anisotropy by means of a strong d-c field,

(b) the reasons for the apparently large skew effect under coincident pulse writing,

(c) the requirement for a small d-c bias field for r-f writing,

(d) for reasonable power dissipation in a memory, the r-f write fields must be reduced from the values of 200 mA for the transverse fields and greater than 400 mA peak-to-peak, for the easy-axis field.

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