NASA CONTRACTOR REPORT

NASA CR-642

DEVELOPMENT OF A THERMIONIC DIODE CONTROLLED POWER SYSTEM

by H. Dean Venable

Prepared by
FAIRCHILD HILLER CORPORATION
Rockville, Md.
for Goddard Space Flight Center

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FOREWORD

This document describes work performed on Goddard Space Flight Center Contract NAS 5-5890, by Fairchild Hiller Corporation. Mr. Robert L. Weitzel, of the Spacecraft Projects Directorate provided guidance and monitored the program for Goddard.

1.0 INTRODUCTION

Future space systems will require more electrical power. For reasons which are discussed at length in the literature, solar cells are not well suited to high power levels except in earth orbits and in the vicinity of the near planets.

The Thermionic Diode is a thermal-to-electrical energy converter. It is compact, efficient, and adaptable for use with radioisotope fuels, solar energy collectors, or nuclear reactors. As a potentially vital source of space power, much experience is needed in operating spacecraft systems from thermionic diode power sources.

A limiting factor in gaining such experience is the current lack of availability of high power thermionic converters. As an economical means of solving the problem of diode availability, and in response to a request for proposal by NASA/GSFC, Fairchild Hiller Corporation proposed to design, develop, and fabricate a dual channel analog system employing two power chains. One power chain is driven by thermionic diodes and delivers 35 watts to a dummy load. The second power chain is driven by conventional laboratory type dc power supplies but slaved to the thermionic diode chain so that the diode current-voltage characteristics can be reproduced at a one kilowatt power level.

This report details the successful design and development of such a system under GSFC Contract NAS 5-5890. The system, as shown in Figure 1, is housed in two relay racks. The low power chain is powered by four 12.5 watt thermionic diodes (not shown) delivering a total of 50 watts at 2 volts. The high power chain operates from a 5-volt source and delivers 1000 watts at 56 volts. Conditioner efficiencies exceed the specification requirements by a considerable margin.

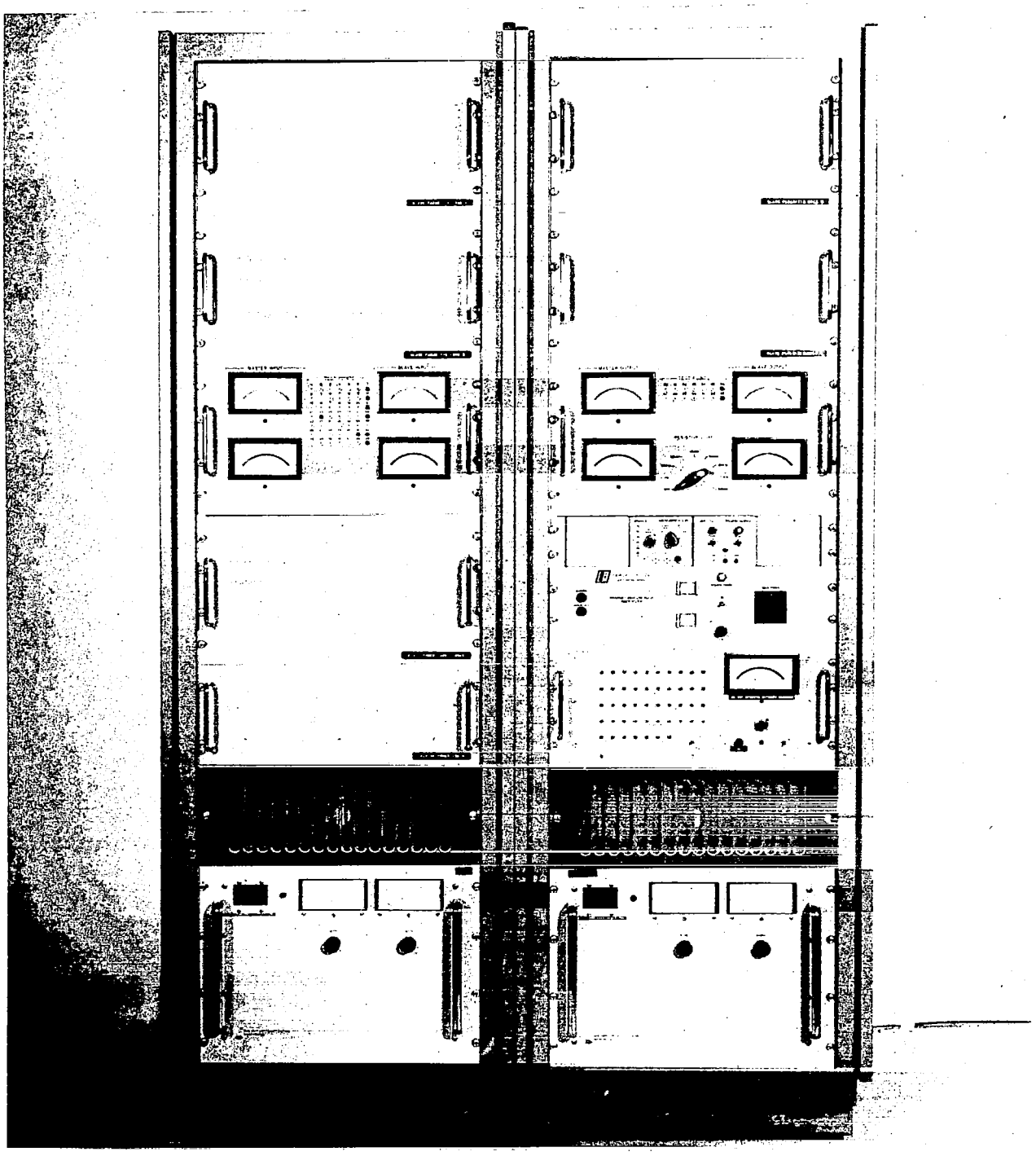


Figure 1 Thermionic Diode Controlled Power System

The system described herein was developed primarily as a means of obtaining integrated system performance of high power ion thrust systems using thermionic diodes as energy converters. The techniques developed on this program are directly applicable to many other types of power simulation equipment. For example, only slight design modification would be required in order to fabricate a power system employing solar cells as the source of prime power.

2.0 SYSTEM DESCRIPTION AND ANALYSIS

2.1 ORIGINAL SYSTEM CONCEPT

The original system as proposed visualized the thermionic diode as a current source. Using this as a starting point, a two-loop feedback system was devised to reflect the load onto the diode and the diode characteristic onto the load. The conceptual system took the configuration shown in Figure 2.

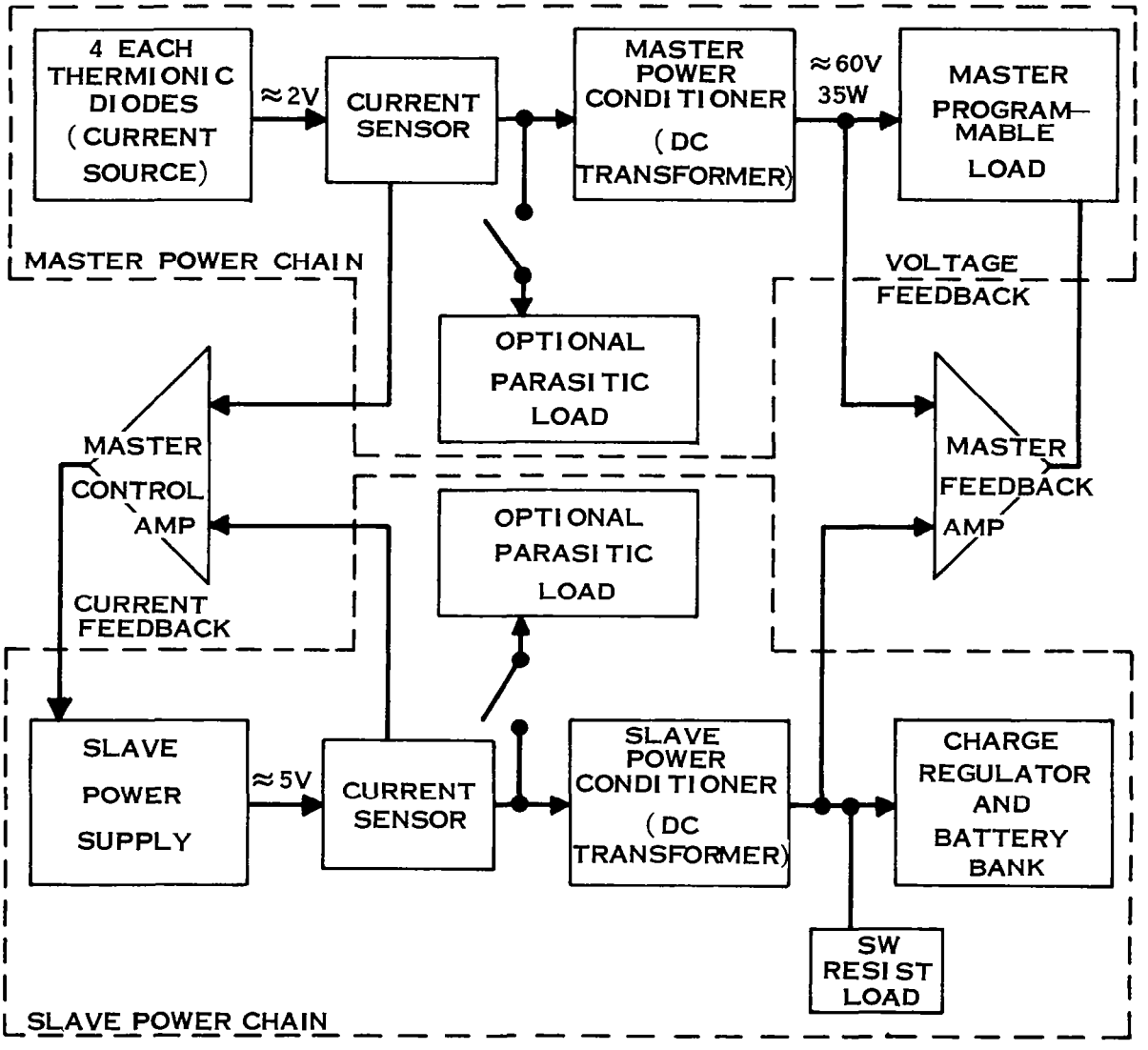


Figure 2 Block Diagram, Original System Concept

The Master Power Conditioner was a dc transformer with a step-up turns ratio a_m, of 30. The Slave Power Conditioner was similar, but with a turns ratio a_s, of 12. Figure 3 shows the various relationships. Subscripts m and s refer to master and slave. Subscripts 1 and 2 refer to primary and secondary of the power conditioners.

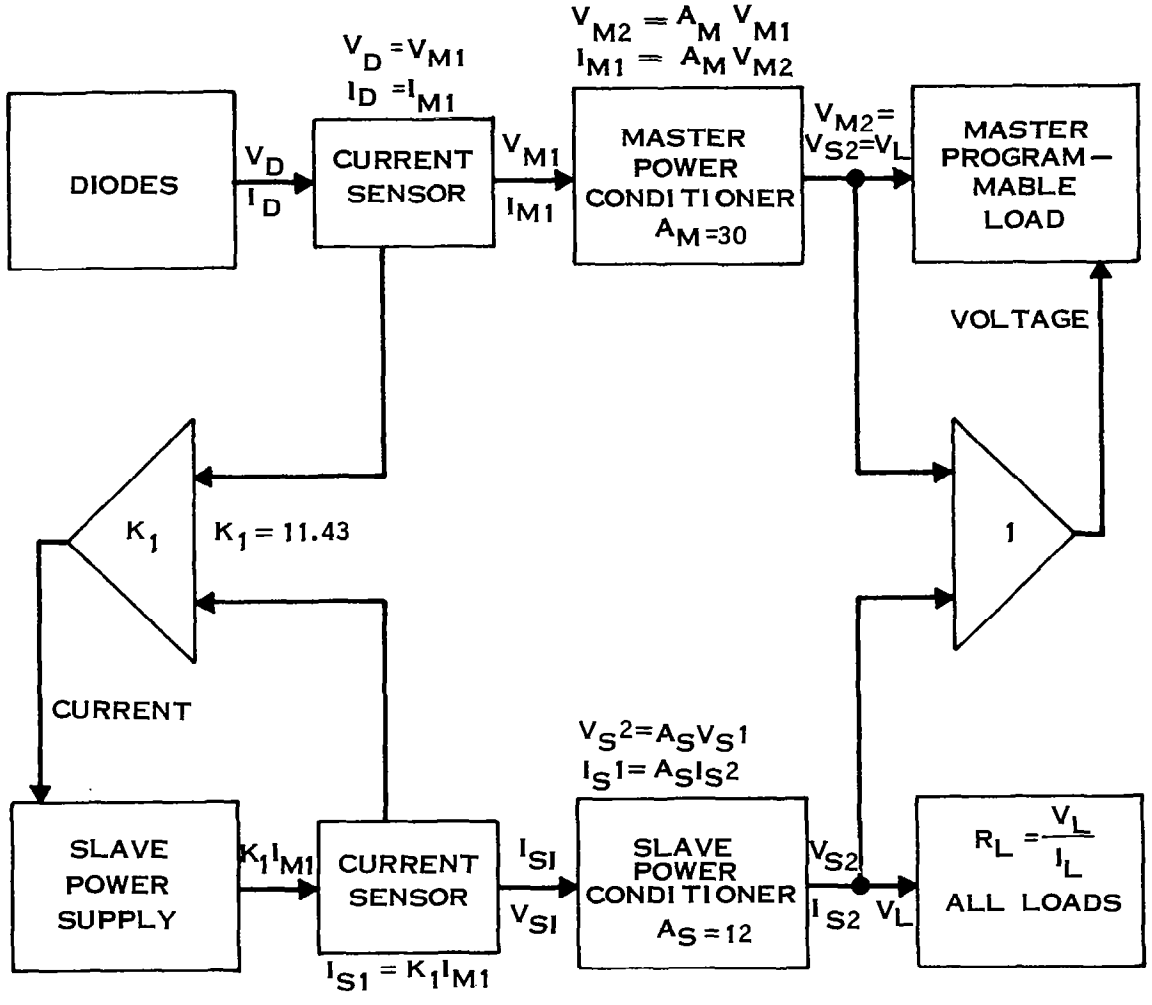


Figure 3 System Relationships

Using the relationship shown in Figure 3, it is noted that

$$V_D = \frac{V_{m2}}{a_m} = \frac{V_L}{a_m} \tag{1}$$

and

$$I_D = \frac{I_{s1}}{K_1} = \frac{a_s I_{s2}}{K_1} = \frac{a_s I_L}{K_1} \tag{2}$$

The current feedback loop constant, K_1, is a function of the power and transformation ratios. Specifically, since $a_s = 12$, $P_s = 1000$, $a_m = 30$, and $P_m = 35$,

$$K_1 = \frac{K_1}{a_m P_m} \approx 11.43 \tag{3}$$

from the above equation

$$\frac{V_D}{I_D} = \frac{K_1}{a_m a_s} \quad \frac{V_L}{I_L} = \frac{K_1 R_L}{a_m a_s} \approx 0.0317 R_L \tag{4}$$

The above analysis ignores the presence of the Master and Slave Parasitic Loads. When the parasitic loads are disconnected, a resistance of approximately 0.0317 R_L is placed across the diode terminals.

When the parasitic loads are considered, the picture changes. The parasitic loads are, in reality, shunt voltage regulators. When used in conjunction with the diode or slave power supply they make the supplies appear as voltage sources.

The slave power supply in conjunction with the slave parasitic load appears as a five volt supply with an internal resistance of 0.00015 ohms, as determined by test. The relationships of Figure 3 must be modified as shown in Figure 4.

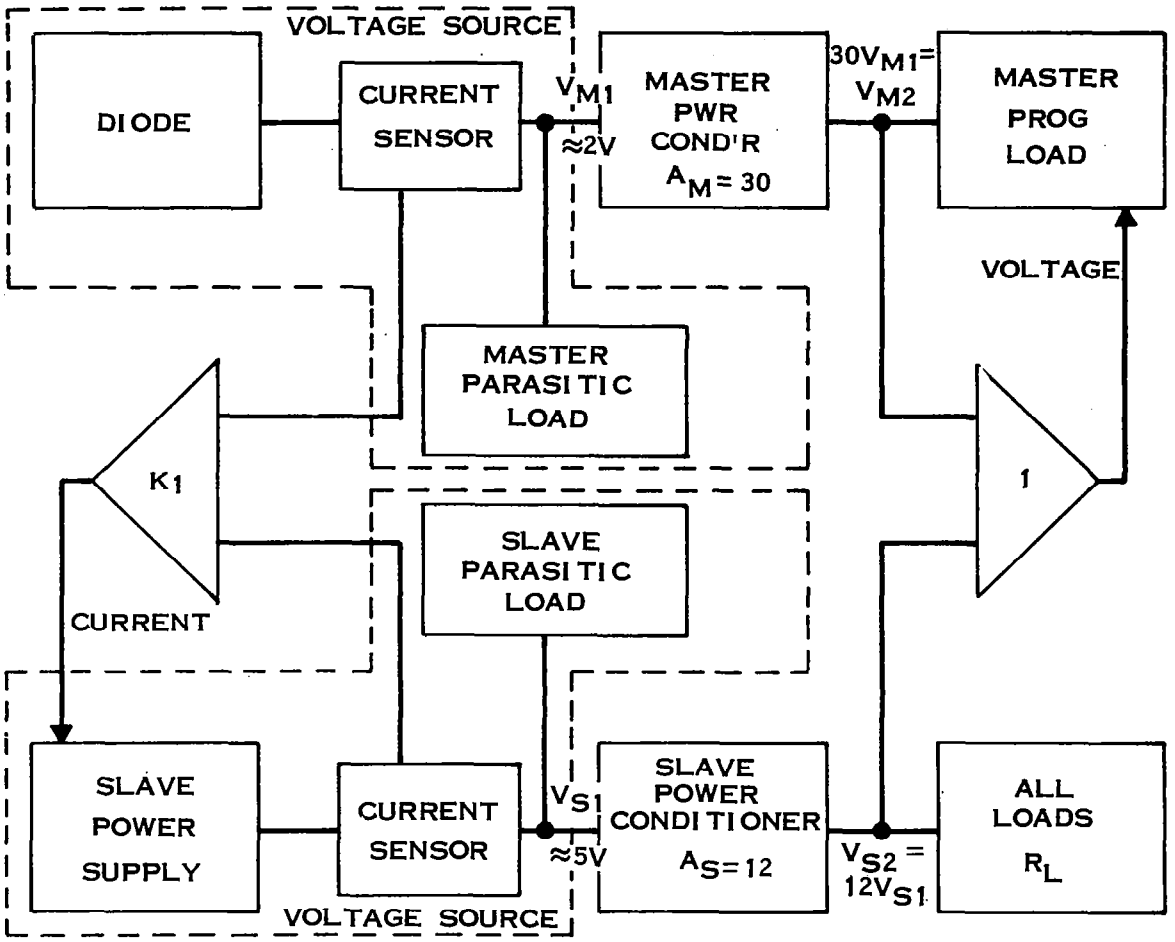


Figure 4 System Relationships with Parasitic Loads

In conjunction with the master parasitic load, the diode appears as a 2-volt source, with an internal resistance of 0.0004 ohms also determined by test. The system equivalent circuit is shown in Figure 5.

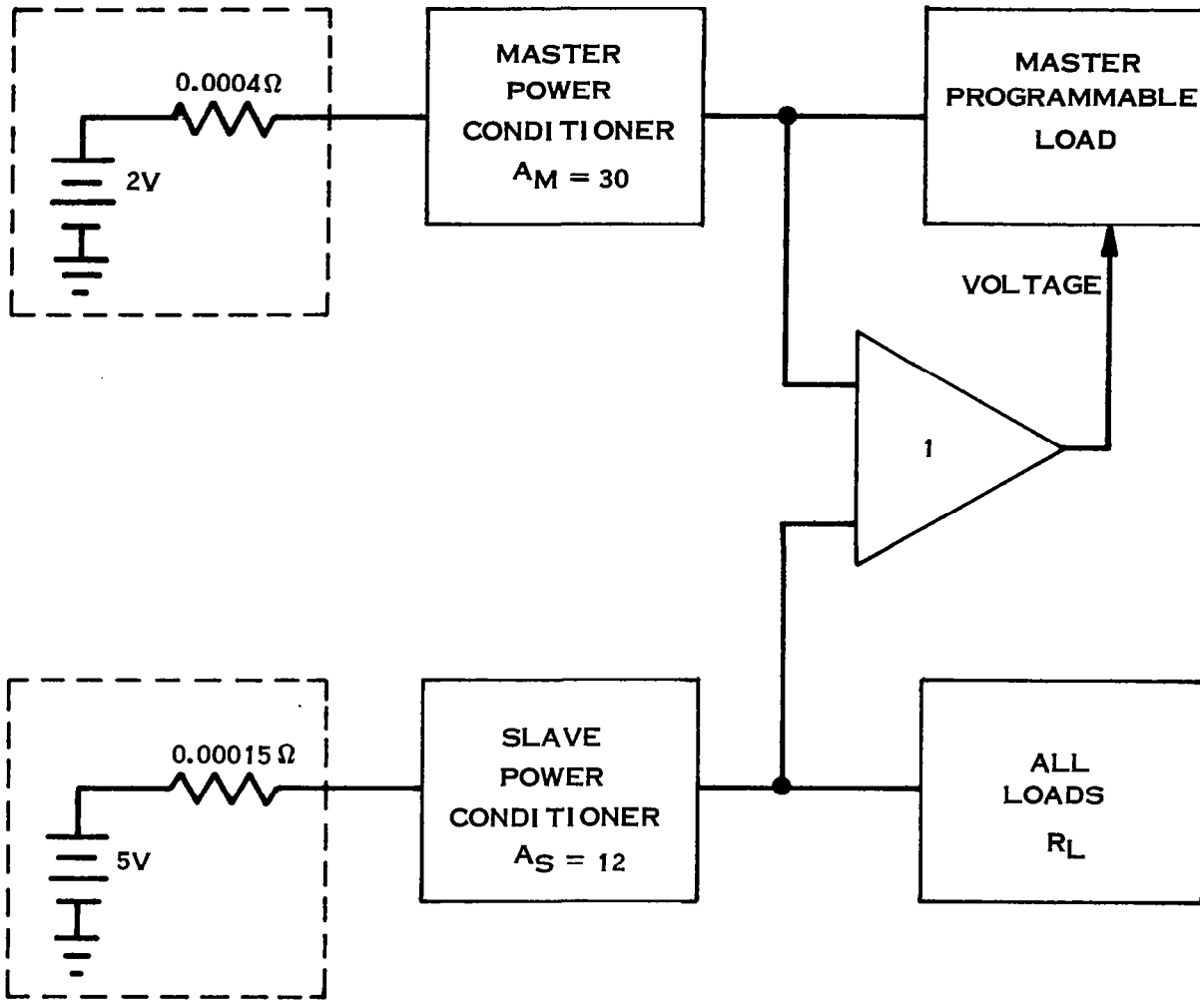


Figure 5 Equivalent System

From Figure 5, it can be seen that the action of the slave parasitic load has reduced the effect of the current feedback loop.

A second simplification in the pictorial representation of the system may be made by utilizing the transformer equations, $V_2 = aV_1$ and $Z_2 = a^2 Z_1$. Transforming the input sources, and adding resistance terms corresponding to the master and slave power conditioner series losses, a simpler equivalent

circuit is derived as shown in Figure 6.

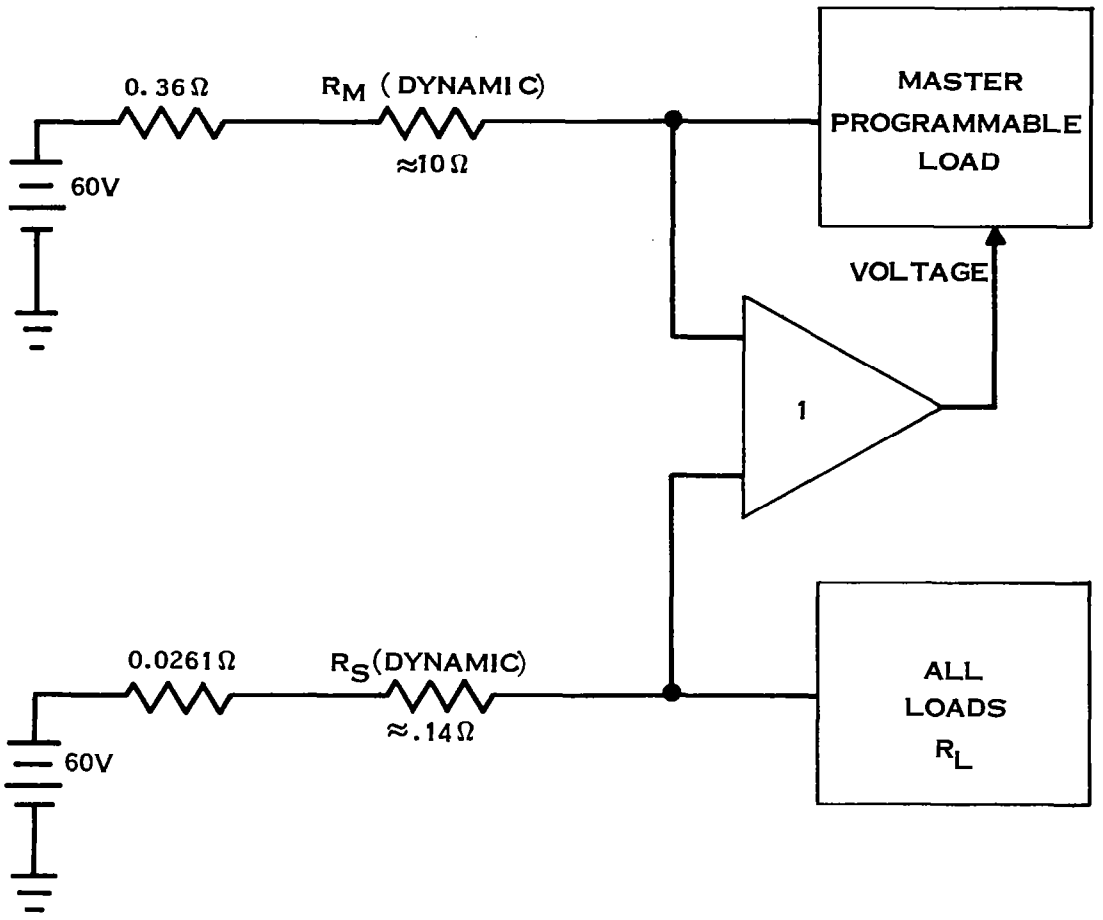


Figure 6 Simplified Equivalent System

From the simplified equivalent system, possible problems become obvious. First of all, the two 60-volt sources are unrelated, and probably will not track with temperature. Second, the conditioner dynamic impedances R_m and R_s must have a precise relationship and must track over the current and temperature range. The currents which flow from each system are determined by the differential between the source and load voltage and the Power Conditioner resistance. While the system could be made to work, it would be almost

entirely dependent on the parameters of the power conditioners and parasitic loads. The characteristics of the diodes and actual loads would have negligible effect on the system performance. This effect is caused by the addition of the parasitic loads, and the system needs modification to accommodate the effect.

2.2 ALTERNATE APPROACH

In order to make a workable system, an approach was conceived which considers the thermionic diode as a voltage source. Using this as a starting point, a configuration was derived which is the analog of the original system. As shown in Figure 7, the configuration uses voltage feedback in the primary and current feedback in the secondary.

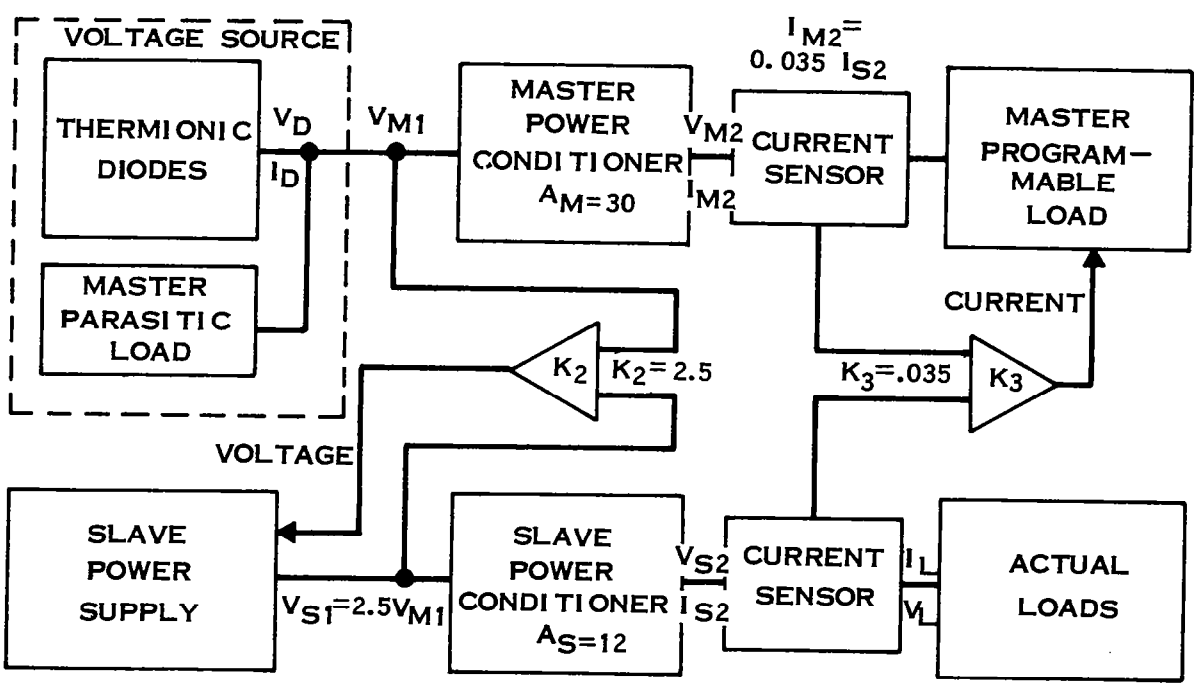


Figure 7 Analog of Original System

The system shown in Figure 7 can accurately reflect the actual load characteristics onto the diode source. If the master parasitic load is disconnected, the dynamic response of the system can be tested. The relationships are now

$$V_D = \frac{V_L}{K_2 a_s} \tag{5}$$

$$I_D = K_3 a_m I_L \tag{6}$$

from (5) and (6)

$$\frac{V_D}{I_D} = \frac{1}{K_2 K_3 a_m a_s} \quad \frac{V_L}{I_L} = \frac{R_L}{K_2 K_3 a_m a_s} \tag{7}$$

Comparison of Equations (4) and (7) indicates that K_1 should equal $\frac{1}{K_2 K_3}$. Numerical substitution proves that this is true. The system now has the same response the original system had before addition of the parasitic loads, that is,

$$\frac{V_D}{I_D} \approx 0.0317\ R_L \tag{8}$$

Although the system of Figure 7 will solve the load reflection problem, it creates a new problem in that the heat balance is destroyed. The slave parasitic load is not needed and, in fact, cannot be safely connected if it has the form of a self-contained 5-volt regulator. Although the above system is more efficient in certain instances, the desired operating mode is to have the input power constant. This can be accomplished by using the slave parasitic load to accomplish the voltage feedback, as shown in Figure 8.

The combination of the Slave Power supply and resistor R_o approximates the diode characteristic. It is not necessary that the combination closely approximates the diode, but this is easily accomplished. The reason dynamic tracking is not necessary is that the action of the master parasitic load

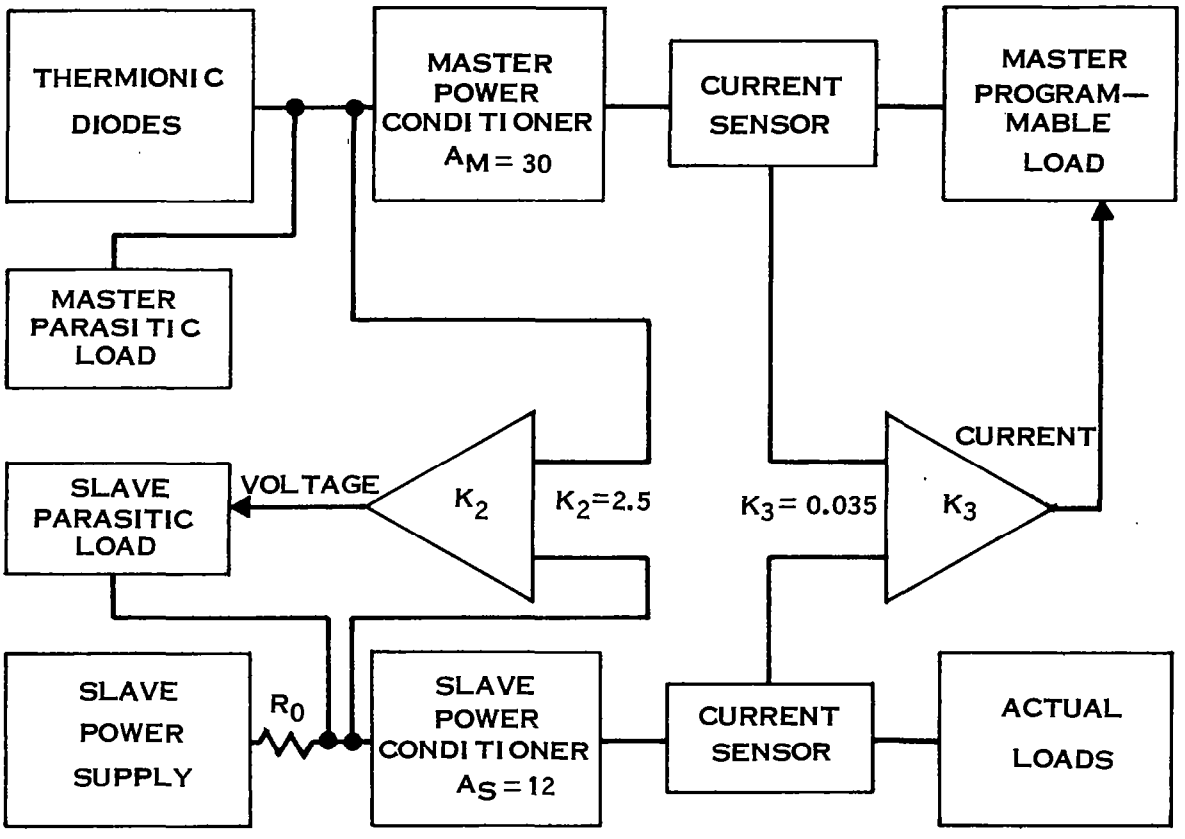


Figure 8 Alternate System with Proper Heat Balance

restricts the diode to one operating point. The slave power supply can then be adjusted manually to the equivalent operating point. For a dynamic test, the slave power supply can be manually adjusted for the period of the test. Even these extremes are unnecessary however, because only the heat balance is affected and the effect is minor. Figure 9 shows a typical approximation curve and a typical diode curve.

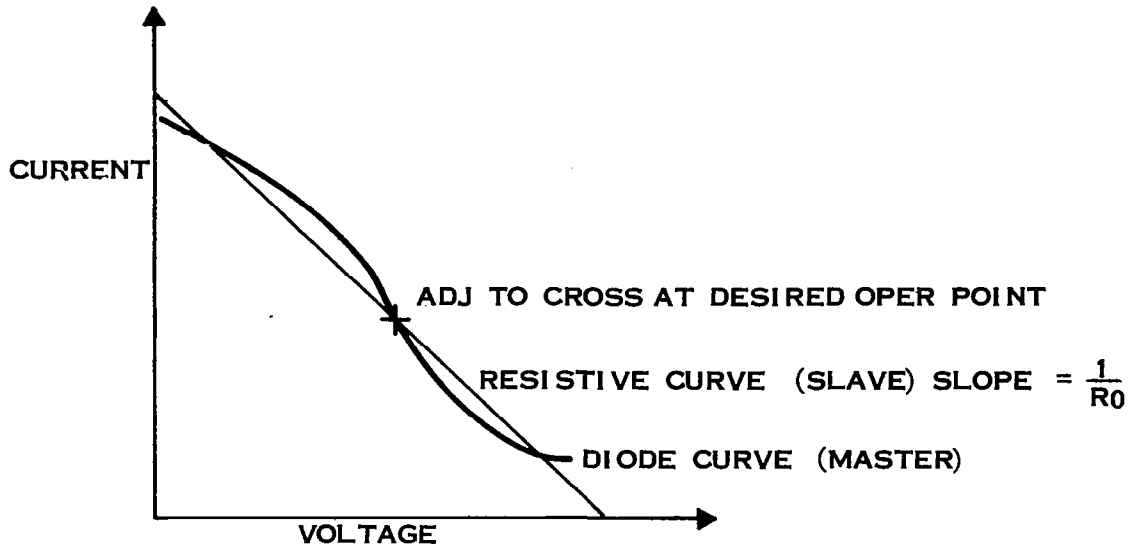


Figure 9 Resistive Approximation of Diode Characteristic

The slave power supply voltage is adjusted so that the approximation crosses the actual curve at the desired operating point. R_o is chosen to approximate the scaled diode characteristic. The reflection of the actual load onto the diodes is dependent on the absolute characteristics of the system components rather than the differential between system characteristics. This is desirable from an engineering standpoint.

2.3 IMPLEMENTATION OF THE ALTERNATE SYSTEM

In addition to being more accurate than the original concept, the alternate system is easier to implement. The high-current sensors are eliminated. Proportional voltage control can be accomplished in the slave parasitic load as shown in Figure 10.

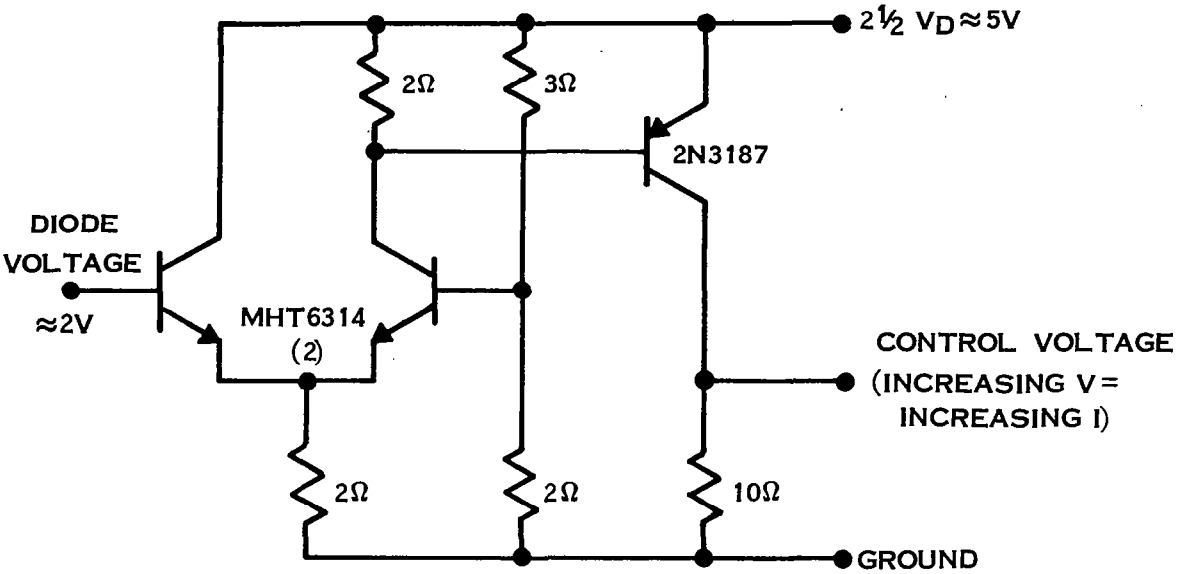


Figure 10 Slave Parasitic Load Controller

Proportional current control on the outputs of the system is slightly more difficult to accomplish than proportional voltage control on the inputs. The most difficult part is sensing the slave system output current (I_L). A method using a shunt is shown in Figure 11.

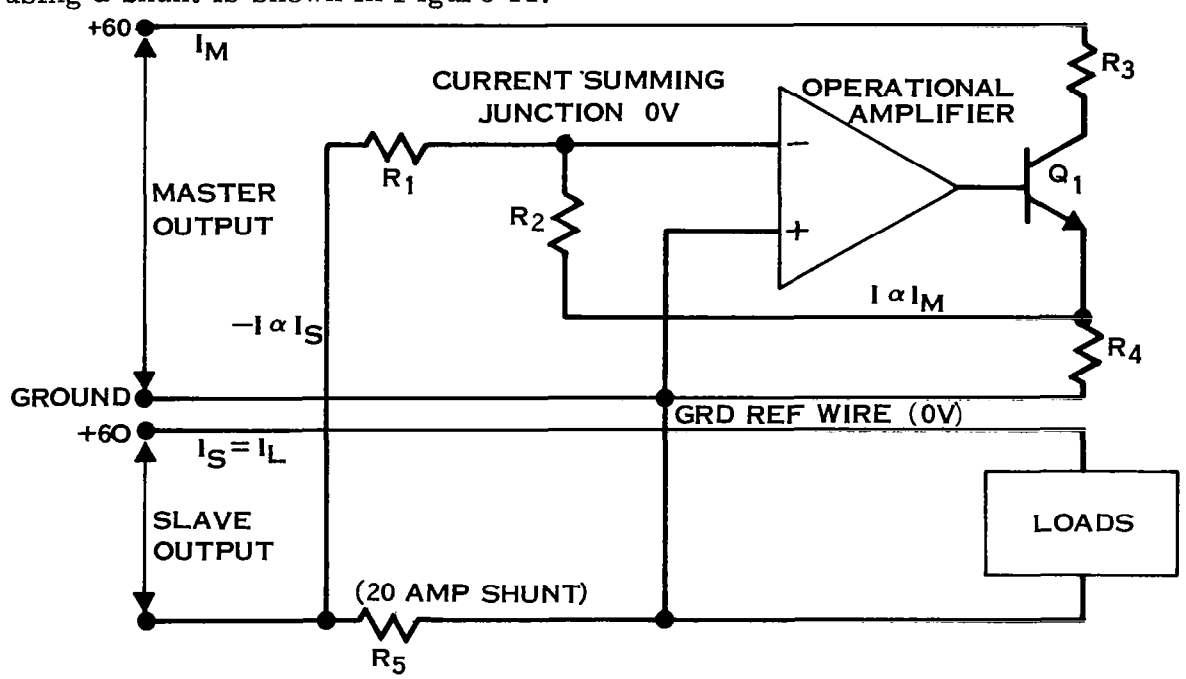


Figure 11 Proportional Current Control

Necessary conditions are that $R_2 \gg R_4$ and $R_1 \gg R_5$. If these conditions are satisfied, the differential operational amplifier will control the system such that

$$\frac{I_m R_4}{R_2} = \frac{I_s R_5}{R_1} \tag{9}$$

Equation (9) is the equation that satisfies the current summing junction conditions ($V_{csj} = 0$).

$$\frac{I_m}{I_s} = \frac{R_2 R_5}{R_1 R_4} = K_3 = 0.035 \tag{10}$$

As an efficiency consideration, the voltage drop across R_5 should be low. If this condition exists, the differential amplifier drift must be two orders of magnitude lower to assure accurate tracking. If a standard 50 millivolt 20 amp shunt is used for R_5, the input voltage drift of the differential amplifier should be less than 0.5 millivolt. This may be difficult to obtain without re-adjustment for long periods of time or wide temperature excursions. A larger value of shunt resistance would ease the requirements of the differential amplifier. (A 20 amp shunt has a value of 0.0025 ohm.)

Another solution is possible which solves the drive problem and at the same time allows the negative output terminals of the Master and Slave chains to be connected directly together.

Figure 12 shows an improved current feedback system. By connecting an inverting, chopper-stabilized amplifier to the slave current sensor, the negative terminals of both power systems can be made common. The low drift of a chopper-stabilized amplifier assures adequate performance for extended periods and over wide temperature extremes. Operation is similar to the circuit of Figure 11. A voltage drop across R_s is amplified and inverted and presented to R_4 as a large negative voltage. The A_2-A_3 combination is

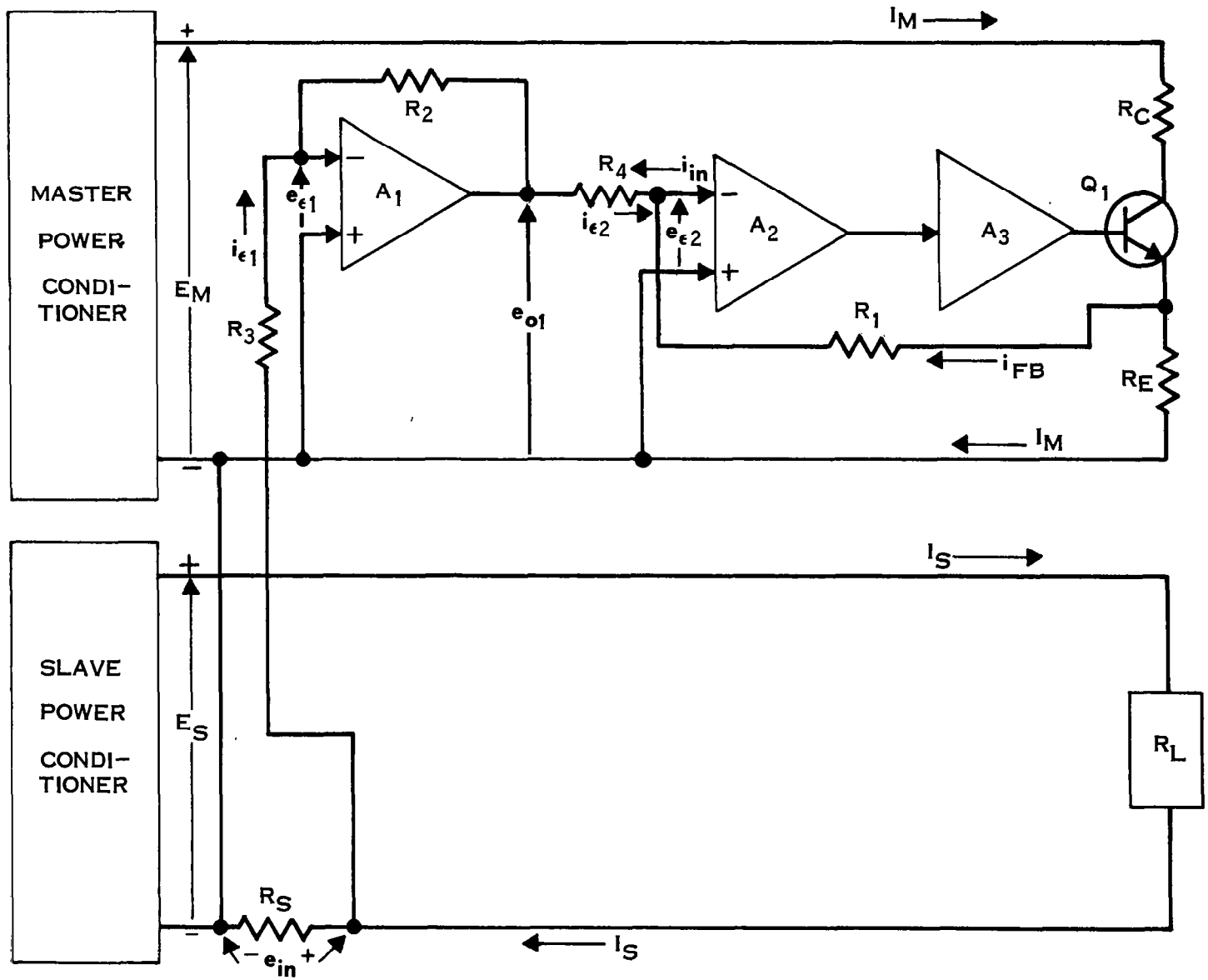


Figure 12 Block Diagram - Current Feedback System

representative of the actual circuit, which requires a booster amplifier (A_3) to adequately drive Q_1. A current flows out of the current summing junction through R_4 proportional to the slave output current. This causes operational amplifier A_2 to drive Q_1 harder until enough voltage is dropped across R_E to force a current through R_1 equal to the current in R_4. There can be no net current at the negative input of A_2.

Figure 13 shows how the current feedback system is implemented in practice. In order to justify the assumption that a chopper-stabilized amplifier is adequate for the application, the following analysis was performed.

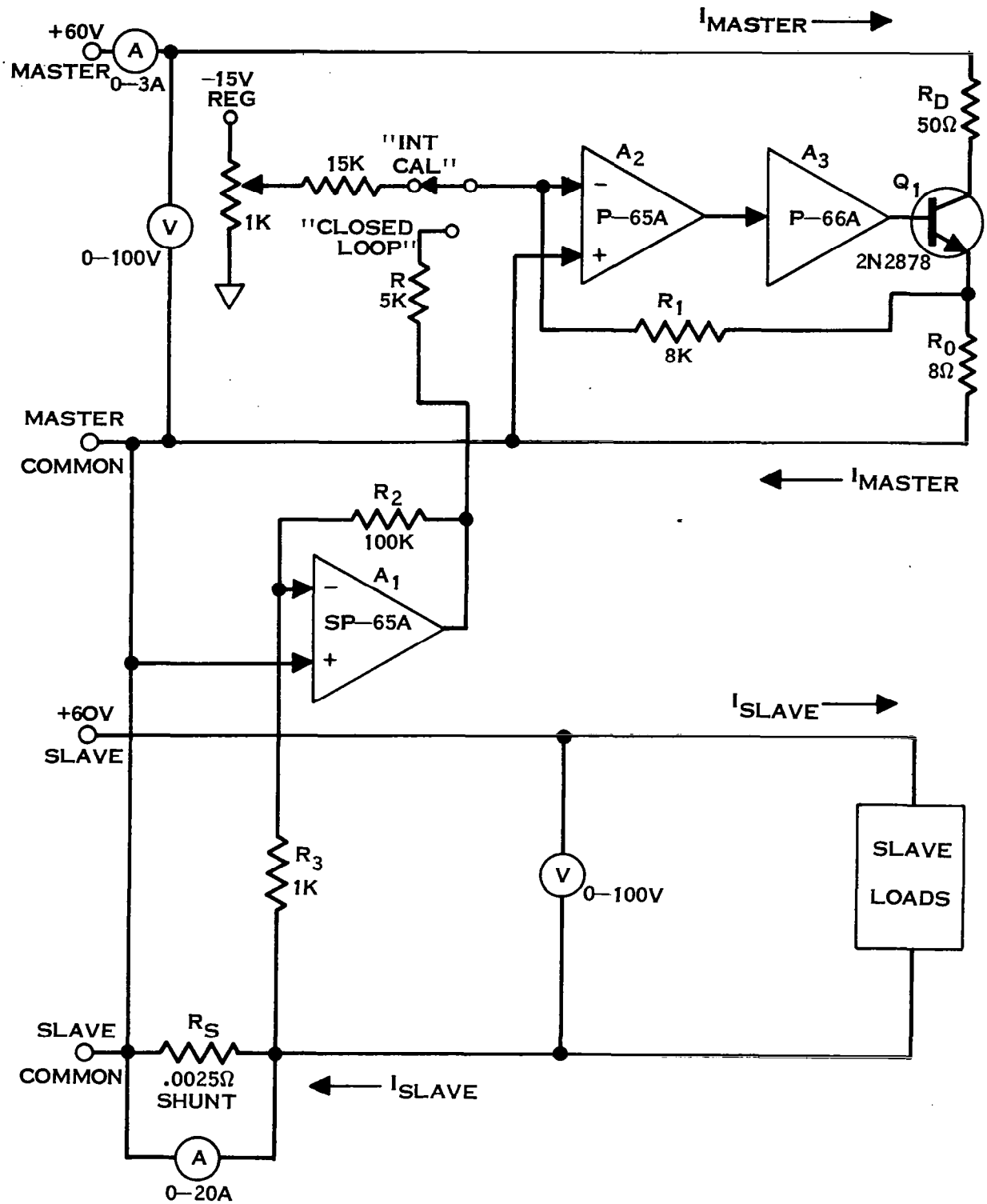


Figure 13 Actual Circuit for Proportional Current Control

2.4 ERROR ANALYSIS

Consider the diagram of Figure 12 which depicts a closed loop control system of the type used in the Thermionic Diode Power Supply simulation system. The purpose of this system is to accurately control the current flow in the upper loop (I_m) in such a fashion that it is at all times proportional to the current flow in the lower loop (I_s). In addition, it is required to maintain this proportionality accurate to ±1% or less in the face of temperature and long term induced error signals. This analysis indicates the quantity of I_m which may be expected to flow as a result of the combined affects of these error signals. The diagram (Figure 12) indicates the most important error voltages and currents present in a system of this type. The e_ϵ terms are those attributed to voltage offsets caused by temperature variations and long term drifts. In a similar fashion, the i_ϵ terms indicate those unbalanced offset currents which flow <u>into</u> the terminals of the amplifiers (as a result of temperature variations or long term drift) chosen in this application (G. A. Philbrick Research types). Taking into consideration the input stage only (A_1 and its associated components), the following equations referring to Figure 14 are presented. (GAPR Data Sheet on PP-65A).

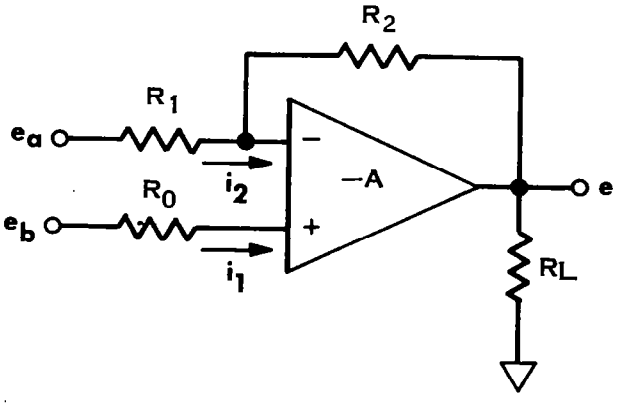


Figure 14 Operational Amplifier Configuration with Error Currents

$$e = (e_b - e_a - i_1 R_o)\left(1 + \frac{R_2}{R_1}\right) + i_2 R_2 \qquad (11)$$

In this equation, $e_b - e_a$ may be regarded as the error offset voltage (e_ϵ), which is essentially multiplied by the operational or closed-loop gain of the configuration. Referring again to Figure 12, it is seen that for our case, $R_o = 0$ which forces $i_1 R_o$ to zero. Therefore, this equation becomes

$$e = (e_b - e_a)\left(1 + \frac{R_2}{R_1}\right) + i_2 R_2 \qquad (12)$$

or in the case of Figure 12

$$e_{o1} = (e_{\epsilon 1})\left(1 + \frac{R_2}{R_3}\right) + i_{\epsilon 1} R_2 \qquad (13)$$

Now this voltage error equation is applicable to both the first and second stage, however, as in any cascade control amplifier chain, the error in the first or input stage predominates in the end output variable. By analyzing the last stages as an entity, (ie, A_2, A_3, Q_1 and their associated components), the following equation is stated with respect to Figure 15. (GAPR Application Brief No. D8, 8/15/63).

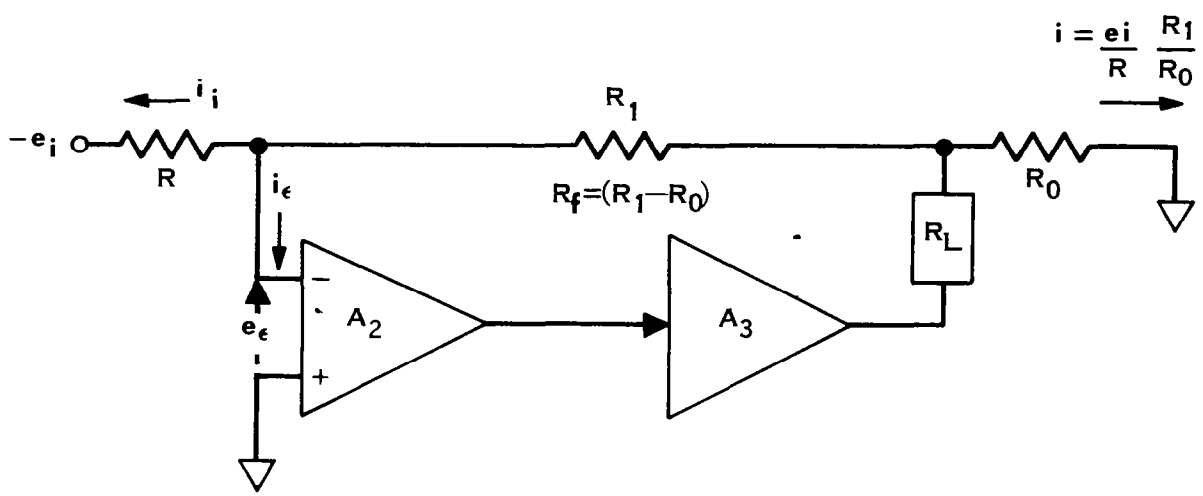


Figure 15 Constant Current Amplifier Configuration

$$I_{(\epsilon)} = i + \left|\frac{e_\epsilon}{R_o}\right| (1 + \frac{R_1}{R}) + \left|i_\epsilon\right| \frac{R_1}{R_o} \quad (14)$$

which for our case reduces to:

$$I_{m(\epsilon)} = I_m + \left|\frac{e_{\epsilon 2}}{R_o}\right| (1 + \frac{R_1}{R}) + \left|i_{\epsilon 2}\right| \frac{R_1}{R_o} \quad (15)$$

Notice that i_{ϵ_2} should be the difference in error current between the i_{in} generated by e_{ϵ_1} offset error, and the inherent error current of A_2 (A_3 is a booster amplifier whose error is assimilated by including it <u>within</u> the closed loop). The reason this point is valid, is that only those i_{in} currents which are flowing <u>away</u> from the summing point node will induce I_m errors at zero input signal. Any i_{in} currents flowing into the node will tend to "cut off" transistor Q_1 by virtue of the inversion performed by A_2. However, it must be realized that when the system is at some steady-state value <u>above</u> zero I_m, this "positive" i_{in} current <u>will</u> be additive. It will be shown further in the analysis that the difference and sum of these currents is quite close to each other, (ie, the difference or sum of two numbers, one of which is larger than the other by an order of magnitude). So that we may now say that:

$$i_{\epsilon_2}' = i_{in} - i_{\epsilon_2} \text{ (a new value for } i_{\epsilon_2} \text{ in Equation (15)} \quad (16)$$

Referring again to Figure 11:

$$i_{in} = \frac{e_{o1} - e_{\epsilon 2}}{R} \quad (17)$$

and substituting (13) into (17) and reducing, results in:

$$i_{in} = \frac{e_{\epsilon 1}}{R} - e_{\epsilon 1} \frac{R_2}{R_3 R} + i_{\epsilon 1} \frac{R_2}{R} - \frac{e_{\epsilon 2}}{R} \quad (18)$$

Now, substituting (18) into (15) (with i_{ϵ_2} replaced by i_{ϵ_2}' of Equation (16),

$$I_{m(\epsilon)} = I_m + \left|\frac{e_{\epsilon 2}}{R_o}\right| (1 + \frac{R_1}{R}) + \left|i_{in} - i_{\epsilon 2}'\right| \frac{R_1}{R_o} \qquad (19)$$

which reduces to

$$I_{m(\epsilon)} = I_m + \left|\frac{e_{\epsilon 2}}{R_o}\right| (1 + \frac{R_1}{R}) + \left|\frac{e_{\epsilon 1}}{R} - \frac{e_{\epsilon 1} R_2}{R_3 R} + i_{\epsilon 1}\frac{R_2}{R} - \frac{e_{\epsilon 2}}{R} - i_{\epsilon 2}\right| \frac{R_1}{R_o} \qquad (20)$$

which, when disregarding the first term, represents the total system error to be expected. It must be noted that the e_ϵ and i_ϵ terms to be considered will be of three different types; (1) static, (2) temperature drift, and (3) long term drift. Reference to manufacturer's data indicates that the static and temperature terms are by far the most influencial, however, both these and long term errors will be calculated.

Case I - A_1 = P-65A, A_2 = P-65A, A_3 = P-66A

Static Worst Case for $+10^{o}C$ to $+60^{o}C$

$e_{\epsilon 1} = 1.5 \times 10^{-3} V$ $\qquad$ $e_{\epsilon 2} = 1.5 \times 10^{-3} V$

$i_{\epsilon 1} = .4 \times 10^{-6} A$ $\qquad$ $i_{\epsilon 2} = .4 \times 10^{-6} A$

Substituting the above values into Equation (20) and using the resistance values shown in Figure 13 results in the following error current,

$$I_{m(\epsilon)\ \text{static temperature}} = 28.98 \text{ ma}$$

which represents a percentage error of approximately 4.8% of $I_{m(FL)}$ (ie, $I_{m(FL)} = \frac{35W}{60V} = 583$ ma). It may be seen that this is an unacceptable solution without proceeding to long term drift errors. An amplifier with lower offset errors is required.

Case II A_1 = SP-65A, A_2 = P-65A, A_3 = P-66A

Static Worst-Case for +10°C to +60°C

$e_{\epsilon 1} = 20 \times 10^{-6}$V $\qquad e_{\epsilon 2} = 1.5 \times 10^{-3}$V

$i_{\epsilon 1} = 30 \times 10^{-12}$A $\qquad i_{\epsilon 2} = .4 \times 10^{-6}$A

Substituting the above values into Equation (20) and using the resistance values shown in Figure 13 results in the following error current:

$$I_{m(\epsilon)\ \text{static temperature}} = 1.68\ \text{ma}$$

This represents a 0.288% error of $I_{m(FL)}$

to continue: Per Day Worst-Case Drift (any temperature)

$e_{\epsilon 1} = 10^{-6}$V $\qquad e_{\epsilon 2} = 50 \times 10^{-6}$V

$i_{\epsilon 1} = 10 \times 10^{-2}$A $\qquad i_{\epsilon 2} = 10 \times 10^{-12}$A

and substitution in Equation (20) as before reveals the following error current:

$$I_{m(\epsilon)\ \text{per day}} = 0.045\ \text{ma}$$

which is approximately 0.0076% error. Thus, the worst-case error combination, results in an anticipated total system error over a temperature range of +10°C to +60°C in a day's operation of:

$$I_{m(\epsilon)\ \text{total}} = \pm 0.2956\%$$

which exceeds the requirements originally set forth.

3.0 ELECTRICAL DESIGN AND DESCRIPTION OF OPERATION

3.1 MASTER POWER CHAIN

The Master Parasitic Load, Master Power Conditioner, and Master Programmable Load form the Master Power Chain, as shown in Figure 16.

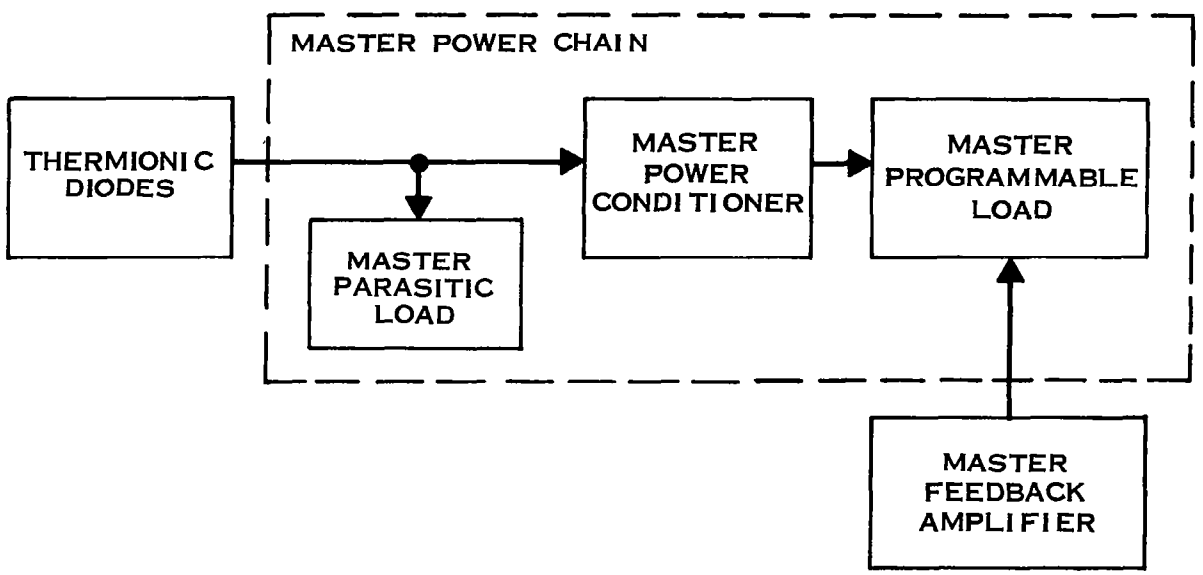


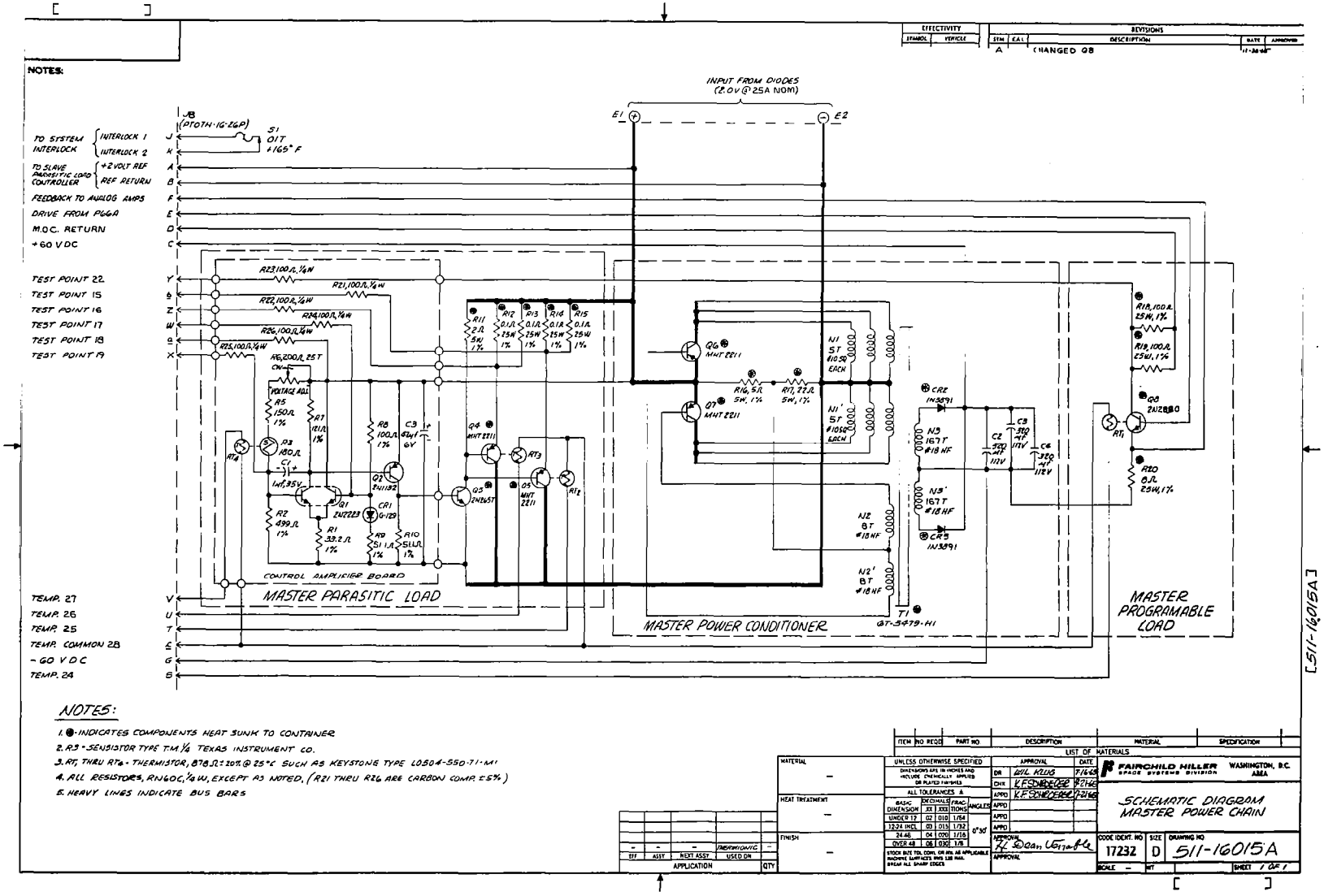
Figure 16 Master Power Chain

Figure 17 is the electrical schematic of the Master Power Chain.

The Master Parasitic Load is a shunt voltage regulator, internally adjusted for 2.00 volts, and capable of accepting up to 50 amps of input current. It acts much like a temperature compensated, 2 volt, 100 watt zener diode.

The Master Power Conditioner is a dc to dc converter with a transformation ratio of 30 to 1. It is nominally rated at 35 watts output power, but a 100% safety margin allows it to deliver 70 watts if required.

The Master Programmable Load is designed to work with the Master Power Conditioner. Maximum power dissipation of about 60 watts occurs when Q8 (see Figure 17) is saturated.



NOTES:

1. ● INDICATES COMPONENTS HEAT SUNK TO CONTAINER
2. R3 = SENSISTOR TYPE T.M ¼ TEXAS INSTRUMENT CO.
3. RT1 THRU RT4 = THERMISTOR, 878Ω ± 20% @ 25°C SUCH AS KEYSTONE TYPE L0504-550-71-M1
4. ALL RESISTORS, RN60C, ¼ W, EXCEPT AS NOTED. (R21 THRU R26 ARE CARBON COMP. ±5%)
5. HEAVY LINES INDICATE BUS BARS

ITEM	NO REQD	PART NO	DESCRIPTION	MATERIAL	SPECIFICATION

LIST OF MATERIALS

EFFECTIVITY: SYMBOL | VEHICLE

REVISIONS: SYM | E.A.L. | DESCRIPTION | DATE | APPROVED
A — CHANGED Q8

MATERIAL: —
HEAT TREATMENT: —
FINISH: —

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND TOLERANCE EXCEPT AS SPECIFIED OR PLATED (or BOLD)
ALL TOLERANCES ±

BASIC DIMENSION	DECIMALS XX	DECIMALS XXX	FRACTIONS	ANGLES
UNDER 12	02	010	1/64	0°30'
12 TO 24 INCL	03	015	1/32	
24 TO 48	04	020	1/16	
OVER 48	06	030	1/8	

STOCK SIZE TOL CONTROL OR MFG AS APPLICABLE
MACHINE SURFACES MAKE 125 MAX.
BREAK ALL SHARP EDGES

APPROVAL		
DR	WILL KLUG	7/66
CHK	V. SCHNEIDER	7/66
APPD	K.F. SCHNEIDER	7/66
APPD		
APPD		
APPD		
APPROVAL	H. Dan Ufferfle	
APPROVAL		

FAIRCHILD HILLER SPACE SYSTEMS DIVISION — WASHINGTON, D.C. AREA

SCHEMATIC DIAGRAM MASTER POWER CHAIN

CODE IDENT. NO	SIZE	DRAWING NO
17232	D	511-16015A

SCALE — | WT | SHEET 1 OF 1

APPLICATION: THERMIONIC | USED ON | NEXT ASSY | ASSY | EFF | QTY

Figure 17

Referring again to Figure 17, input power is applied to terminals E1 and E2. Heavy lines indicate high current bus bars within the Master Power Chain package. The Master Parasitic Load sensing circuit is connected directly across the high current bus. Dual transistor Q1 serves as a differential amplifier to sense the bus voltage and control the high current transistors. The CR1/R9 combination presents a lower dynamic resistance than static resistance. Static and dynamic resistances of complementary resistor R2 are equal. For this reason, an increased bus voltage (increased current through R2 and CR1/R9) causes less voltage change across the CR1/R9 combination, simultaneously causing increased conductance in the left side of Q1.

Transistors Q2, Q3, Q4, and Q5 follow suit increasing their conductance to hold the bus voltage change to a minimum. R6 sets the voltage to a nominal 2 volts. The amplifier and temperature compensation sensistor R3 hold the voltage change with temperature and current to ±1% respectively.

Transistors Q4 and Q5 are germanium, but operation in the common collector configuration assures stability and freedom from thermal runaway. Capacitor C1 provides a. c. stabilization.

Various test points are brought out to front panel jacks to facilitate trouble shooting in the event of a malfunction. Test points 21 and 23 are the Master Power Chain input and output grounds, respectively. Adjustment of R6 is preset. R6 is sealed in the Master Power Chain container and cannot be readjusted. Testing of the Master Chain at input voltages other than 2 volts can be accomplished by shorting test point 19 to test point 21. This reduces the effective resistance of R2 to 83 ohms and prevents conduction of the Parasitic Load. There is no lower limit on the input voltage. Caution should be used when exceeding 2 volts because of the 80 volt breakdown rating of Q8. Collector voltage of Q8 appears on test point 22 referenced to test point 23.

The Master Power Conditioner is designed to be simple, reliable, and efficient. Minneapolis-Honeywell MHT 2211 transistors are used as Q6 and Q7 in the switching stage. These transistors are specially designed for this low-voltage high-current application. Their specifications appear as Appendix I to this report.

The primary windings of T1, N1, and N1 , consist of three parallel five-turn windings using number 10 AWG square cross-section copper wire. Square wire is used because it offers the best space factor for the wound core. Number 10 is the largest practical wire which can be wound on a core. Three windings in parallel reduce the winding resistance losses.

N2 and N2' are feedback windings. They provide base drive for switching transistors Q6 and Q7. R16 limits the base drive current. R17 provides current for starting.

Diodes CR2 and CR3 rectify the square wave voltage on output windings N3 and N3' . The diodes are type 1N3891, chosen for their high conductance and low recovery time. Capacitors C2, C3, and C4 are hermetically sealed tantalum electrolytics, used to smooth the output voltage.

The rectified output voltage leaves the package on connector J8 pin C, passes through ammeter M5, and returns on J8 pin D, to the Master Programmable Load. Q8 is the programmable load transistor, rated at 80 volts and 5 amps, but not simultaneously. R18, R19, and Q8 dissipate most of the Master Chain output power. R20 is primarily a current sensing resistor, providing a current feedback signal to the analog instrumentation on J8 pin F.

Thermistors are provided at strategic locations inside the package to monitor critical temperatures and to allow evaluation of the thermal control system. S1 is a thermal interlock to protect the system in the event of overheating.

3.2 MASTER CONTROL AMPLIFIER AND SLAVE PARASITIC LOAD

The Master Control Amplifier is located inside the Slave Power Conditioner container so that it can sense the bus voltage directly. It appears on the Slave Power Conditioner schematic diagram (Figure 20) labeled "Slave Parasitic Load Comparator and Driver" and is reproduced below as Figure 18.

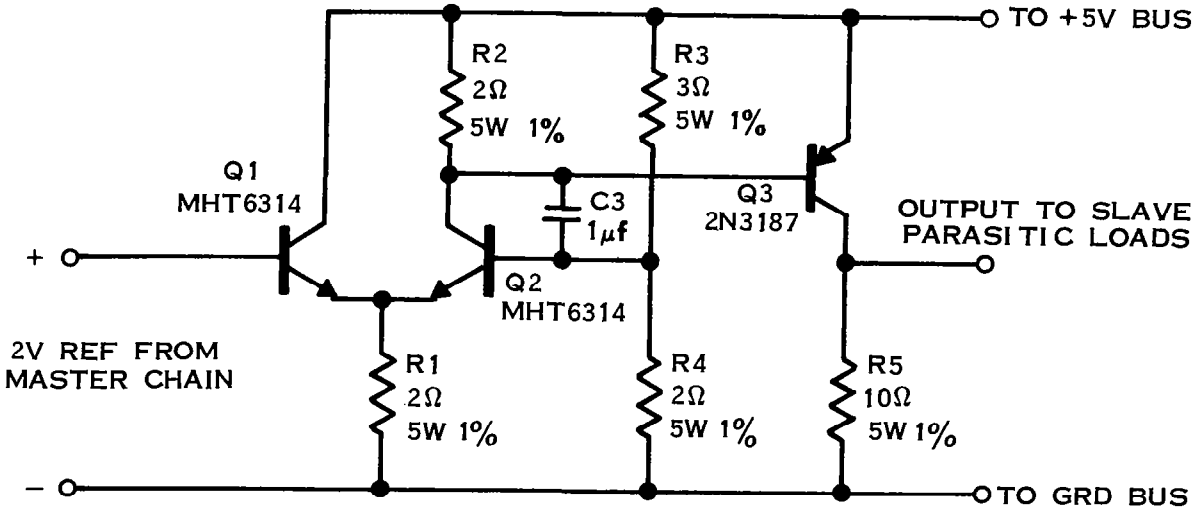


Figure 18 Master Control Amplifier

A typical Slave Parasitic Load unit is shown schematically in Figure 19. There are four identical Slave Parasitic Load boxes. Splitting of the Slave Parasitic Load unit into four boxes was dictated by thermal considerations. In a flight-type space application the design would be modified to greatly improve the radiating surface-to-volume ratio.

As is the case in the Master Power Chain, the voltage sensing amplifier is tied directly across the high current bus. The reference voltage for the Master Control Amplifier comes from the Master Power Chain. This

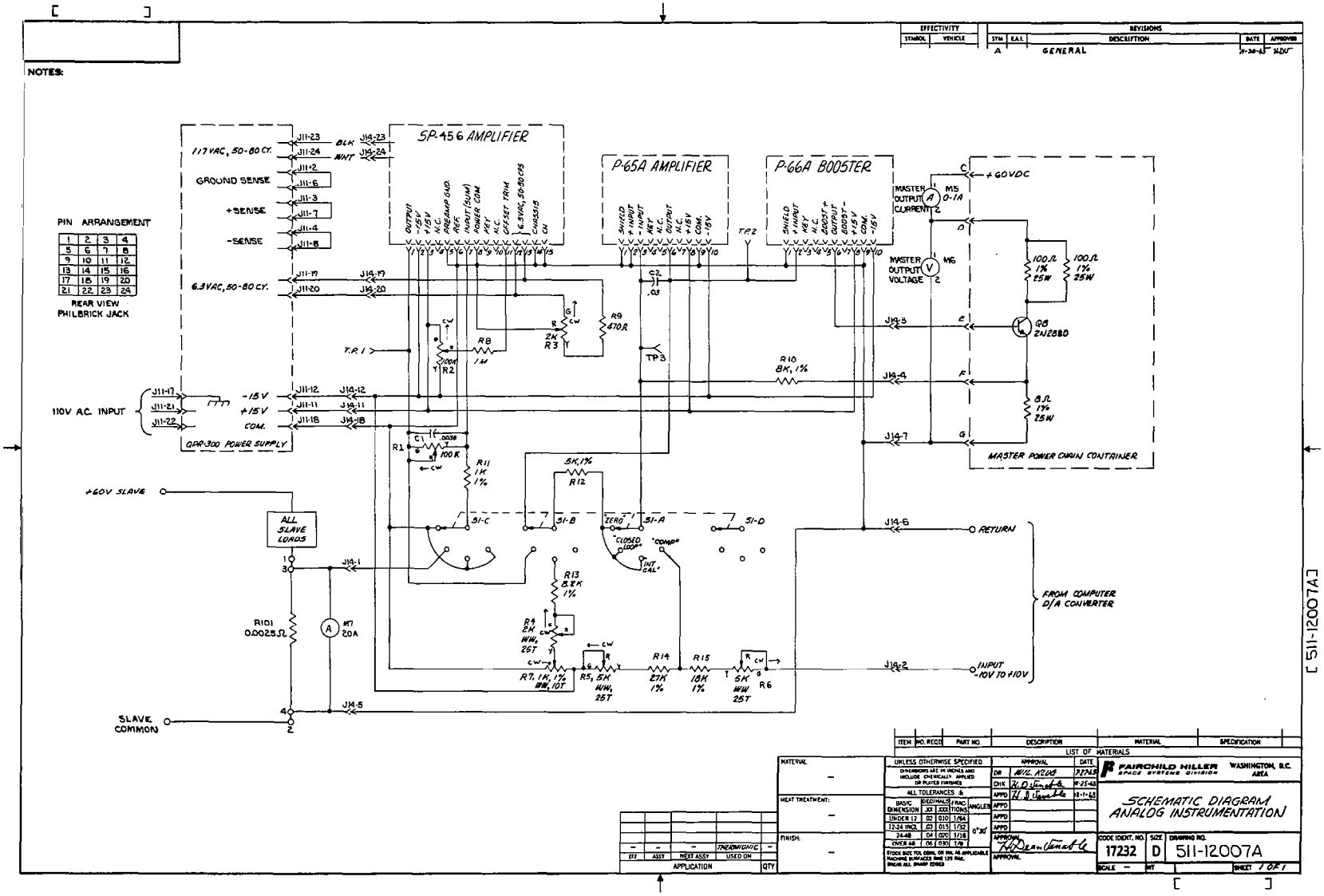

NOTES:
SP-456 AMPLIFIER
P-65A AMPLIFIER
P-66A BOOSTER
117 VAC, 50-80 CY.
GROUND SENSE
+SENSE
-SENSE
6.3 VAC, 50-80 CY.
PIN ARRANGEMENT
REAR VIEW
PHILBRICK JACK
110V A.C. INPUT
QPR-300 POWER SUPPLY
+60V SLAVE
ALL SLAVE LOADS
SLAVE COMMON
MASTER OUTPUT CURRENT
MASTER OUTPUT VOLTAGE
+60VDC
MASTER POWER CHAIN CONTAINER
RETURN
FROM COMPUTER D/A CONVERTER
INPUT -10V TO +10V
R1 100K
R2 100K
R3 2K
R4 2K WW, 25T
R5, 5K WW, 25T
R6 5K WW 25T
R7, 1K, 1% WW, 10T
R8 1M
R9 470Ω
R10 8K, 1%
R11 1M 1%
R12 5K, 1%
R13 8.2K 1%
R14 27K 1%
R15 18K 1%
R101 0.0025Ω
Q8 2N2880
ZERO
CLOSED LOOP
COMP
INT CAL
EFFECTIVITY
REVISIONS
GENERAL
FAIRCHILD HILLER
SPACE SYSTEMS DIVISION
WASHINGTON, D.C. AREA
SCHEMATIC DIAGRAM
ANALOG INSTRUMENTATION
CODE IDENT. NO. 17232
SIZE D
DRAWING NO. 511-12007A
SHEET 1 OF 1
511-12007A

Figure 19

voltage is 2 volts under normal conditions or is set by the operator in the event he has chosen to short test point 19 to test point 21. Resistors R3 and R4 divide the bus voltage so that 2/5 of it is applied to the base of Q2. Feedback action will then maintain the bus voltage at 2.5 times the reference voltage. If the bus voltage increases, Q2 conducts more. This, in turn, increases the current through Q3, providing more drive for the Slave Parasitic Load units. Connector J7, pins C, D, E, and F, tie to pin A on J5A, J5B, J5C, and J5D, respectively.

The high-current bus bars labeled E1 and E2 in the Slave Power Conditioner unit are common to the high current bus bars labeled E1 and E2 in the Slave Parasitic Load unit. When the conduction through Q3 is increased, Q1 in each of the Slave Parasitic Load units is turned on harder, providing more base drive for transistors Q2 through Q7.

Q2 through Q7 are high power 30 amp transistors. They are supplied in sets of six, and are matched for transconductance. The resistor/transistor combinations such as R4/Q2 are designed so that the power ratings of the six transistors Q2 through Q7 are not exceeded. Current through each of these high power transistors is limited to about 20 amps. Each Slave Parasitic Load unit is therefore limited to 120 amps. Total capacity of the four units is 600 amps. This matches the output capabilities of the Slave Power supplies.

Correlation between the Slave Parasitic Load unit test points and the respective front panel test jacks are given in the table at the top of Figure 19.

One-quarter of the Switched Resistive Load is located within each Slave Parasitic Load unit box. This is to preserve a proper heat balance. When the Slave Power Conditioner is lightly loaded, most of the input power is dissipated in the Slave Parasitic Load. As the switched resistive load power is increased, a correspondingly smaller amount is dissipated in the Slave

Parasitic Load. By placing the resistive load elements in the parasitic load box, approximately the same amount of power is dissipated regardless of load setting. As in the Master Power Chain, thermistors are located at strategic points within the box to monitor critical temperatures. The fail-safe thermal circuit breaker, S1, is set for a higher temperature in the Slave Parasitic Load boxes than in the Master Power Chain. These boxes are designed to work at a higher temperature to dissipate the larger amount of power. Maximum power dissipation of any individual box is approximately 600 watts.

3.3 SLAVE POWER CONDITIONER AND CHARGE CURRENT REGULATOR

Figure 20 is the schematic diagram of the Slave Power Conditioner unit. The charge current regulator and its associated supplies are housed within the Slave Power Conditioner box, as is the Slave Parasitic Load comparator and driver, formally called the Master Control Amplifier.

The original system concept provided for the Slave Power Chain to be a scaled-up version of the Master Power Chain. This dictated the basic design of the Slave Power Conditioner. The only difference between the Slave Power Conditioner and the Master Power Conditioner is in the interconnection of the base drive limiting and starting resistors. The Master unit has the base drive and starting resistors in a biasing arrangement to allow them to do double duty. This configuration is not practical in the slave unit due to the large number of parallel transistors. Separate base drive limiting resistors are provided to assure that each transistor will carry its fair share of the load.

Switching transistors Q4 through Q8 conduct simultaneously. Transistor bank Q9 through Q13 conducts alternately with transistor bank Q4 through Q8. Typically, for Q4, R6 is the starting resistor and R7 is the base drive limiting resistor. The feedback winding provides 2 volts of base drive. R7 limits the

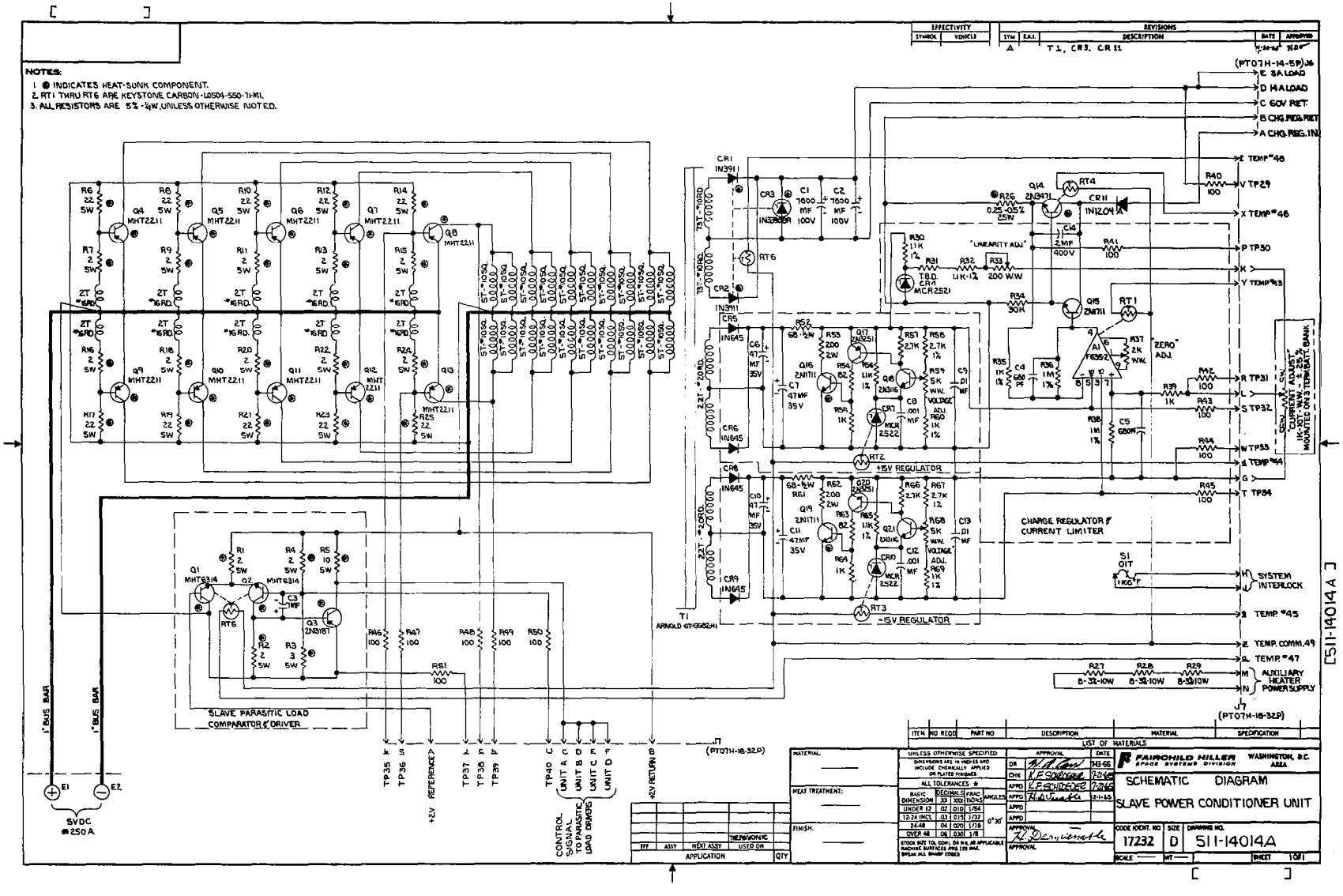

NOTES:
1. ● INDICATES HEAT-SINK COMPONENT.
2. RT1 THRU RT6 ARE KEYSTONE CARBON-L0504-550-1-M1.
3. ALL RESISTORS ARE 5% -½W, UNLESS OTHERWISE NOTED.
EFFECTIVITY
SYMBOL VEHICLE
REVISIONS
SYM E.A.I. DESCRIPTION DATE APPROVED
A T1, CR3, CR11
(PT07H-14-59)J6
E SA LOAD
D MA LOAD
C GOV RET.
B CHG REG & RET
A CHG REG. IN
CHARGE REGULATOR & CURRENT LIMITER
+15V REGULATOR
-15V REGULATOR
SLAVE PARASITIC LOAD COMPARATOR & DRIVER
SYSTEM INTERLOCK
AUXILIARY HEATER POWER SUPPLY
J7 (PT07H-18-32P)
LIST OF MATERIALS
ITEM NO REQD PART NO DESCRIPTION MATERIAL SPECIFICATION
FAIRCHILD HILLER SPACE SYSTEMS DIVISION WASHINGTON, D.C. AREA
SCHEMATIC DIAGRAM
SLAVE POWER CONDITIONER UNIT
CODE IDENT. NO 17232
SIZE D
DRAWING NO. 511-14014A
SCALE
WT
SHEET 1 OF 1
511-14014 A

Figure 20

base current to 1 amp. As in the Master Power Conditioner, number 10 AWG square cross-section copper wire was used because it has the best space factor and is the largest practical wire than can be wound on the core. Each transistor uses two parallel windings. Three would be preferable, but are impractical because of space limitation of the core window. There is a reasonably good balance between copper loss, transistor saturation drop and switching loss, indicating a near optimum choice of switching frequency.

The 73 turns of number 10 AWG round copper wire in the secondary was chosen to give the supply its output capacity of 60 volts nominal at 17 amps. The actual output voltage is somewhat higher, dictated by the high peak voltage necessary to charge the battery bank. Diodes CR1 and CR2, types 1N3911, were chosen for their high conductance and low recovery time. Zener diode CR3 provides over-voltage protection for C1 and C2 when the secondary is not loaded.

The battery charge regulator, located within the Slave Power Conditioner unit, has little direct effect on the operation of the Slave Power Conditioner. The +15 volt regulator and -15 volt regulator are mounted on printed circuit boards attached to the sides of the Slave Power Conditioner container. The two 20-volt, 20-turn windings are shunt regulated to provide regulated ±15 volts to the operational amplifier A1, a Fairchild modular operational amplifier, type F635-2. It is used to sense the battery charge current and compare it to the setting of the current-adjust potentiometer located on the front panel of the battery bank. Resistor R26 is the current sensing element and its voltage drop is applied directly to the inverting input of the operational amplifier. The wiper of the current-adjust potentiometer provides a reference voltage for the non-inverting input of the operational amplifier. If the current should increase above the set value, an increased voltage drop across R26 would drive the output of the amplifier (pin 4) negative. This would turn off Q15, in turn decreasing the conductance of Q14. CR11 prevents the battery from discharging through the switched resistive load and through the charge regulator in the reverse direction.

As was done in other boxes, thermistors are provided to monitor critical temperatures. In the Slave Power Conditioner unit, three resistors, R27, R28, and R29 are provided as an auxiliary heat source to prevent overcooling in a cold thermal vacuum test at light load. When operating in this condition, 28 volts dc should be applied to the series string.

3.4 ANALOG INSTRUMENTATION

The analog instrumentation controls the current in the Master Programmable Load. It is shown on the block diagram as the Master Feedback Amplifier, and is shown schematically in Figure 21. The electronic circuitry consists of commercial operational amplifiers and their associated feedback and scaling resistors. The amplifiers are housed in plug-in modules for easy accessibility and maintenance. Space is provided for four plug-in modules. Only two are presently used allowing space for future extension of system capability. The G. A. Philbrick Research QPR-300 power supply occupies one module. The analog instrumentation is housed within the other module.

Operation of the analog instrumentation in the closed-loop mode is shown in Figure 22.

The G. A. Philbrick Research SP-65A is a chopper-stabilized dc amplifier which senses the Slave output current. It amplifies and inverts the voltage drop across R101. Voltage gain is adjustable from 0 to 100 with potentiometer R1. This adjustment is used to set the scaling factor between the Master and Slave output currents. Nominally, the scale factor is 0.035, which requires an amplifier gain of 70.

As an example, consider a Slave output current of 10 amps and the nominal scaling factor of 0.035 or 350 milliamps of Master output current. Referring to Figure 22, the 10 amps of Slave output current would produce a voltage drop of +25 millivolts across R101. A voltage gain the the SP-65A of -70

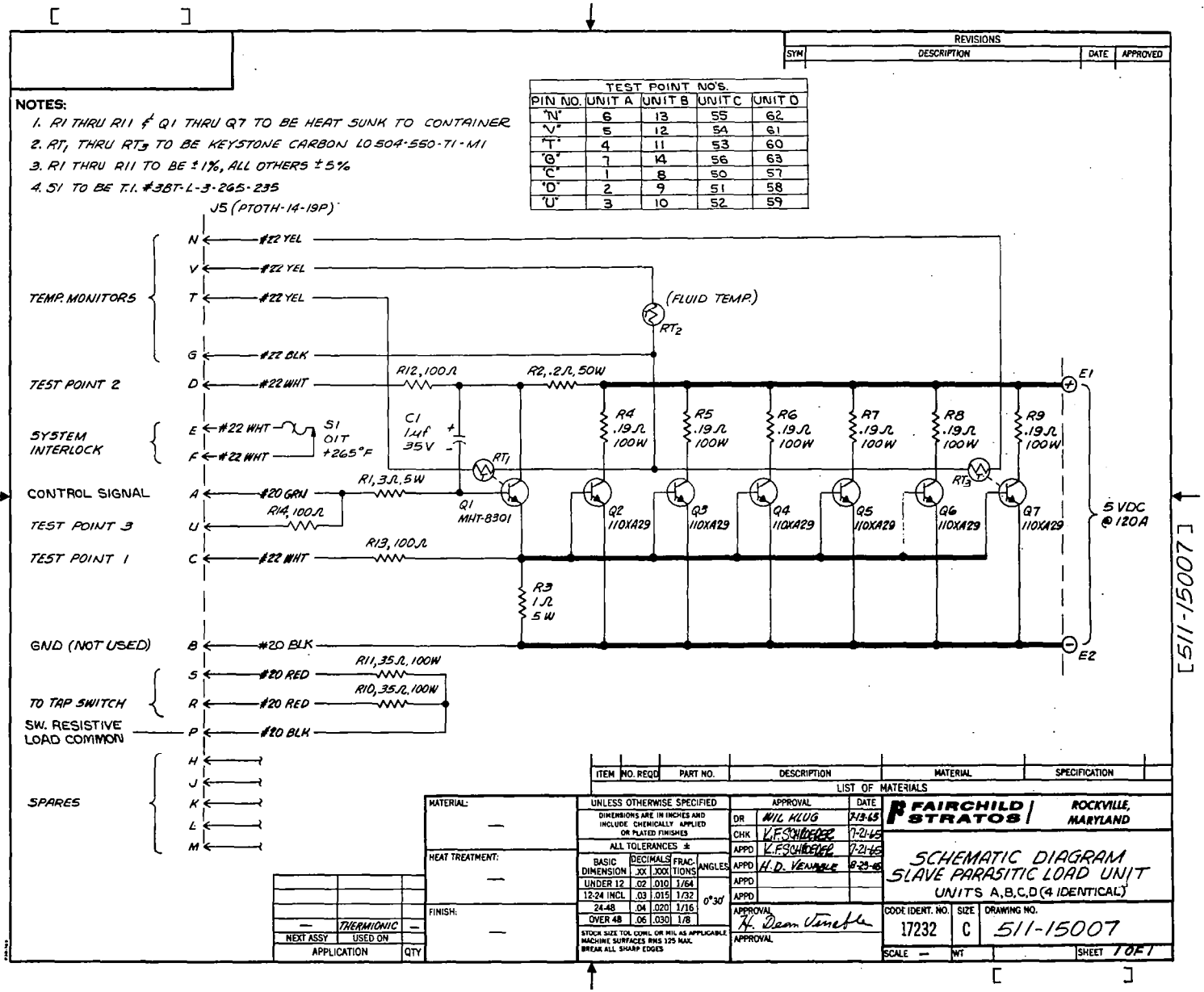

REVISIONS
SYM | DESCRIPTION | DATE | APPROVED
NOTES:
1. R1 THRU R11 & Q1 THRU Q7 TO BE HEAT SUNK TO CONTAINER
2. RT1 THRU RT3 TO BE KEYSTONE CARBON LO504-560-71-M1
3. R1 THRU R11 TO BE ±1%, ALL OTHERS ±5%
4. S1 TO BE T.I. #3BT-L-3-265-235
TEST POINT NO'S.
PIN NO. | UNIT A | UNIT B | UNIT C | UNIT D
"N" 6 13 55 62
"V" 5 12 54 61
"T" 4 11 53 60
"G" 7 14 56 63
"C" 1 8 50 57
"D" 2 9 51 58
"U" 3 10 52 59
J5 (PTOTH-14-19P)
TEMP. MONITORS
TEST POINT 2
SYSTEM INTERLOCK
CONTROL SIGNAL
TEST POINT 3
TEST POINT 1
GND (NOT USED)
TO TAP SWITCH
SW. RESISTIVE LOAD COMMON
SPARES
#22 YEL
#22 BLK
#22 WHT
#20 GRN
#20 RED
#20 BLK
(FLUID TEMP.)
RT2
RT1
RT3
S1 OIT +265°F
C1 1μf 35V
R12, 100Ω
R2, .2Ω, 50W
R1, 3Ω, 5W
R14, 100Ω
R13, 100Ω
R3 1Ω 5W
R11, 35Ω, 100W
R10, 35Ω, 100W
R4 .19Ω 100W
R5 .19Ω 100W
R6 .19Ω 100W
R7 .19Ω 100W
R8 .19Ω 100W
R9 .19Ω 100W
Q1 MHT-8301
Q2 110XA29
Q3 110XA29
Q4 110XA29
Q5 110XA29
Q6 110XA29
Q7 110XA29
E1
E2
5 VDC @ 120A
511-15007-151
ITEM | NO. REQD | PART NO. | DESCRIPTION | MATERIAL | SPECIFICATION
LIST OF MATERIALS
MATERIAL: —
HEAT TREATMENT: —
FINISH: —
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
ALL TOLERANCES ±
BASIC DIMENSION | DECIMALS .XX .XXX | FRACTIONS | ANGLES
UNDER 12 .02 .010 1/64
12-24 INCL .03 .015 1/32 0°30'
24-48 .04 .020 1/16
OVER 48 .06 .030 1/8
STOCK SIZE TOL COMM. OR MIL AS APPLICABLE
MACHINE SURFACES RMS 125 MAX.
BREAK ALL SHARP EDGES
APPROVAL | DATE
DR NIL KLUG 7-13-65
CHK V.F. SCHNEIDER 7-21-65
APPD V.F. SCHNEIDER 7-21-65
APPD H.D. VENABLE 8-25-65
APPD
APPD
APPROVAL H. Dean Venable
APPROVAL
— THERMIONIC —
NEXT ASSY | USED ON
APPLICATION | QTY
FAIRCHILD STRATOS | ROCKVILLE, MARYLAND
SCHEMATIC DIAGRAM
SLAVE PARASITIC LOAD UNIT
UNITS A,B,C,D (4 IDENTICAL)
CODE IDENT. NO. 17232 | SIZE C | DRAWING NO. 511-15007
SCALE — | WT | SHEET 1 OF 1

Figure 21

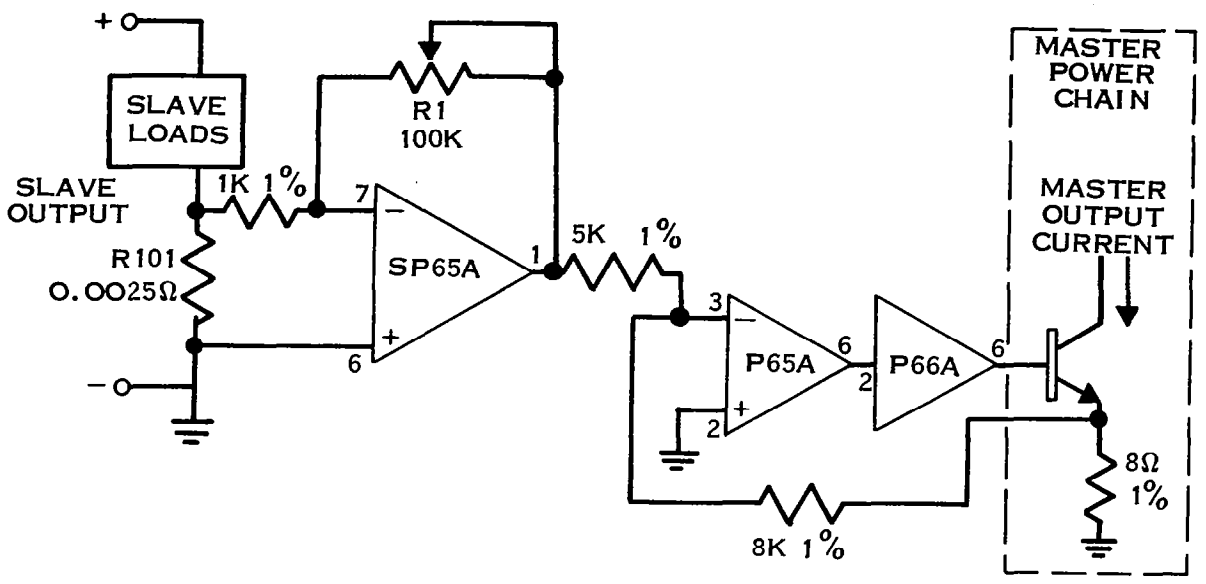


Figure 22 Analog Instrumentation Closed-Loop Mode

produces an output voltage of -1.75 volts. Pin 3 of the P65A is virtual ground, so a current of -1.75/5000 or -0.35 milliamps will flow through the 5K resistor. The same current must flow through the 8K resistor to satisfy Kirchoff's Current Law. Voltage drops across the 8K and 8 ohm resistors are equal, therefore a current of 0.35 milliamps in the 8K resistor is equivalent to 350 milliamps of Master output current and the scale relationship is satisfied.

Operation in the "Internal Calibrate" mode is shown in Figure 23. Variation in the "CURRENT ADJUST" potentiometer between its two extremes produces a current from zero to one milliamp through the 15,000 ohm resistor. As in closed loop operation, this current is scaled up by a factor of 1000 to become zero to one amp of Master output current.

In the computer programmed mode, shown in Figure 24, a bias current of 0.5 milliamps is applied to the P65A input causing a no-input or standby Master output current of 0.5 amps. Computer output voltage swing from +10 volts to -10 volts varies the Master output current from zero to one amp respectively. These values represent the nominal output of a Scientific Data Systems digital to analog converter. Modification to work with other computers

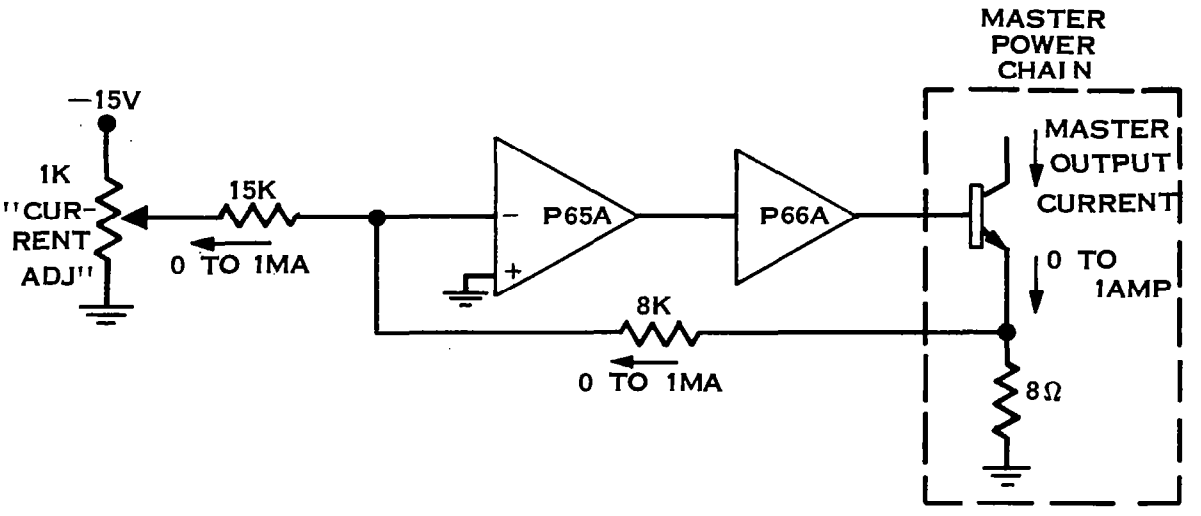


Figure 23 Analog Instrumentation - Internal Calibrate Mode

can easily be accomplished, since the analog instrumentation is in plug-in modular form and is readily accessible.

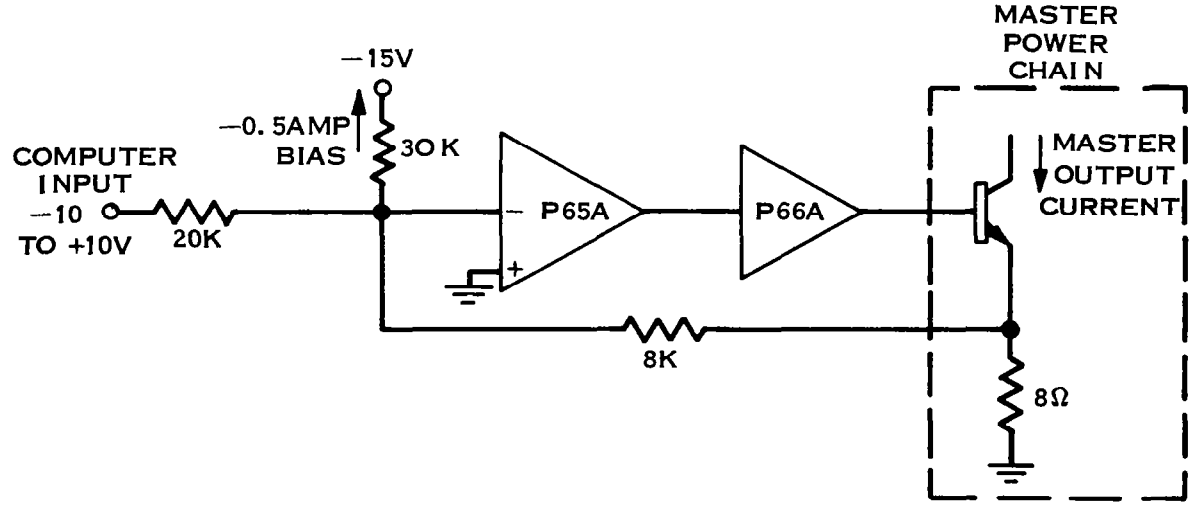


Figure 24 Analog Instrumentation - Computer Programmed Mode

3.5 SWITCHED RESISTIVE LOAD AND BATTERY BANK

The battery bank is designed to draw 3 amps or about 200 watts from the Slave Power Conditioner. Since the Slave system is capable of delivering up to 1000 watts, a switched resistive load representing system growth potential, and capable of dissipating an additional 800 watts, is incorporated. The Switched Resistive Load consists of eight 35-ohm, 100-watt resistors and a power tap switch and is shown schematically in Figure 25. The power tap switch is wired to place the 35 ohm resistors sequentially in parallel across the Slave output terminals. A 35 ohm resistor with the rated output voltage of 60 volts applied will dissipate 103 watts. Two of the Switched Resistive Load resistors are located within each Slave Parasitic Load unit. This was done to provide heat balance in each parasitic load box. The power tap switch is a four-deck switch wired to produce minimum transients during switching. Make-before-break contacts prevent arcing and assure long life.

The battery bank consists of forty-seven 12 amp-hour rechargeable nickel cadmium cells, charge-control modules for each cell and an indicator light system to visually indicate when a cell is fully charged. A Fairchild Hiller Model 6401-6A Constant Current Cell Charger is included with the battery bank but is not normally used. The system normally depends on a similar constant current charger located with the Slave Power Conditioner container. The Model 6401-6A Constant-Current Charger can be used in situations where it is desirable to use the battery bank as an entity. Specifications of the 6401-6A are included as Appendix II of this report.

The schematic diagram of the Three-Terminal Battery Bank is shown in Figure 26. The current-bypass control modules are shown schematically in Figure 27. Referring to the battery bank schematic, the charging current comes in through terminal board TB1 and the 3 amp circuit breaker to the 5 amp shunt, RS1. The charging current then passes through each of the cells

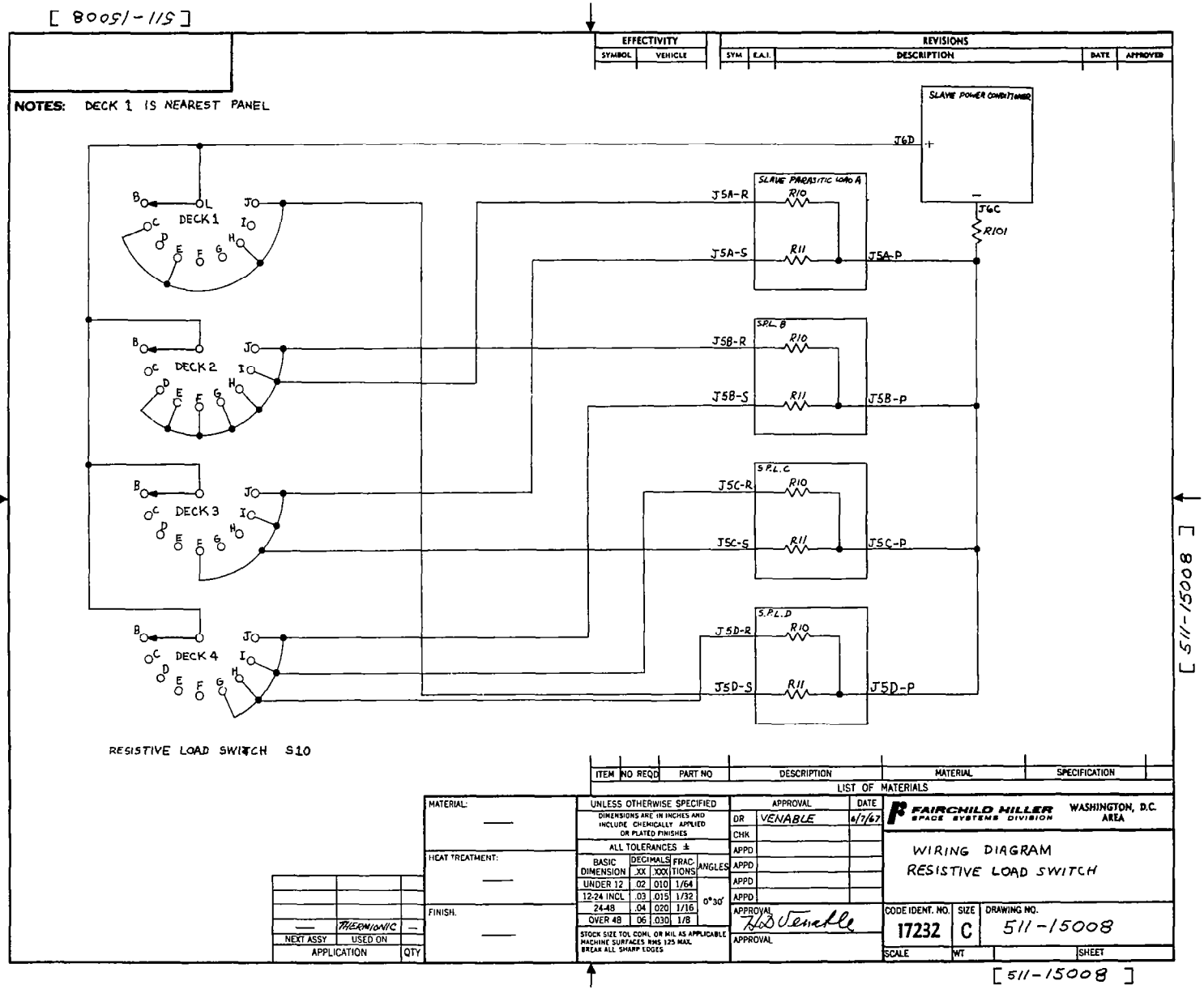

[8005/-115]
EFFECTIVITY
SYMBOL
VEHICLE
REVISIONS
SYM
E.A.I.
DESCRIPTION
DATE
APPROVED
NOTES: DECK 1 IS NEAREST PANEL
SLAVE POWER CONDITIONER
J6D
J6C
R101
SLAVE PARASITIC LOAD A
J5A-R
J5A-S
J5A-P
R10
R11
DECK 1
S.P.L. B
J5B-R
J5B-S
J5B-P
DECK 2
S.P.L.C
J5C-R
J5C-S
J5C-P
DECK 3
S.P.L.D
J5D-R
J5D-S
J5D-P
DECK 4
RESISTIVE LOAD SWITCH S10
[511-15008]
ITEM
NO REQD
PART NO
DESCRIPTION
MATERIAL
SPECIFICATION
LIST OF MATERIALS
MATERIAL:
HEAT TREATMENT:
FINISH:
THERMIONIC
NEXT ASSY
USED ON
APPLICATION
QTY
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
ALL TOLERANCES ±
BASIC DIMENSION
DECIMALS XX XXX
FRAC. TIONS
ANGLES
UNDER 12 .02 .010 1/64
12-24 INCL .03 .015 1/32
24-48 .04 .020 1/16
OVER 48 .06 .030 1/8
0°30'
STOCK SIZE TOL COML OR MIL AS APPLICABLE
MACHINE SURFACES RMS 125 MAX.
BREAK ALL SHARP EDGES
APPROVAL
DATE
DR VENABLE 6/7/67
CHK
APPD
APPD
APPD
APPD
APPROVAL H.D. Venable
APPROVAL
FAIRCHILD HILLER SPACE SYSTEMS DIVISION
WASHINGTON, D.C. AREA
WIRING DIAGRAM
RESISTIVE LOAD SWITCH
CODE IDENT. NO. 17232
SIZE C
DRAWING NO. 511-15008
SCALE
WT
SHEET
[511-15008]

Figure 25

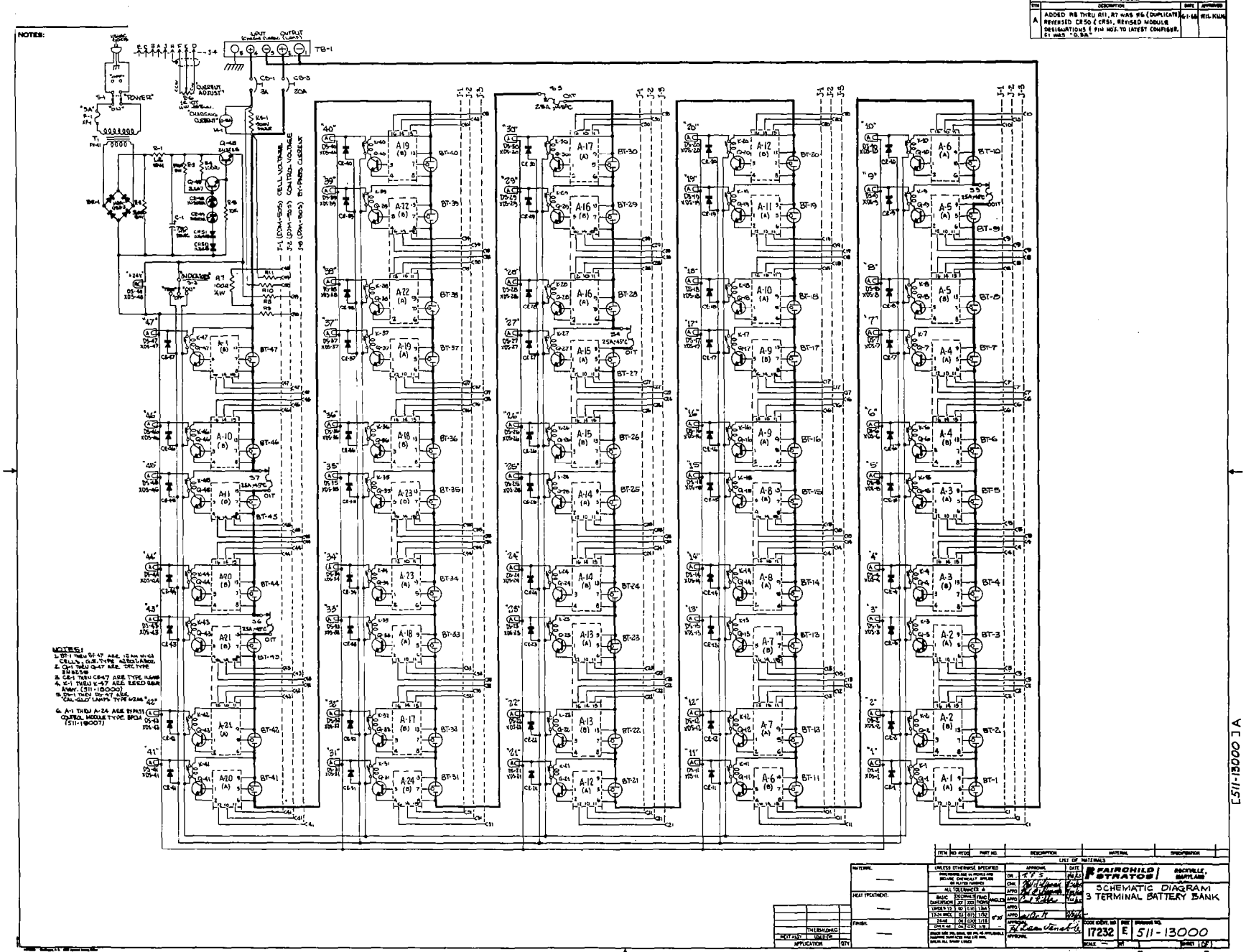

NOTES:
SCHEMATIC DIAGRAM
3 TERMINAL BATTERY BANK
FAIRCHILD STRATOS
17232
511-13000
E

Figure 26

NOTES:

1. THE FOLLOWING DESIGNATIONS ARE NOT USED:
   A. RESISTORS - R10
   B. TRANSISTORS - Q3 THRU Q10
   C. DIODES - CR3 THRU CR10
2. DOTTED LINE CIRCUITRY IS NOT INCLUDED IN MODULE.

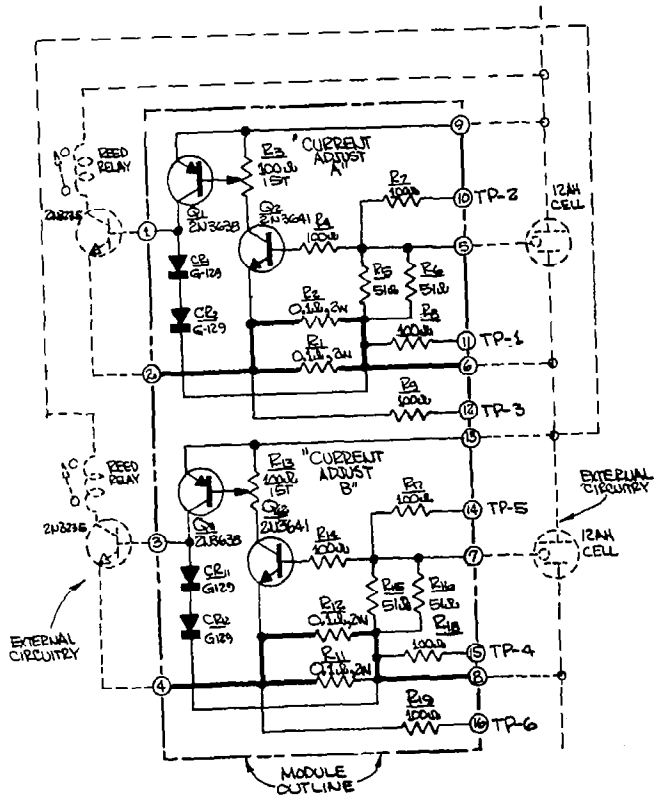


Figure 27

and returns on the negative terminal of TB1. Five thermal circuit breakers labeled S3 through S7 are connected in series with the battery to prevent damage in the event of overheating. The thermal circuit breakers are set to open at 45°C.

A typical cell/control module combination is cell BT47 and control module A24B. Operation can be seen more clearly by referring to the schematic diagram of the Current Bypass Control Module, Figure 27. The 3 amp charge current passes down through the cells until they become fully charged and oxygen begins to evolve. The presence of oxygen causes a voltage proportional to oxygen pressure to appear on the control electrode of the cell. The control electrode is connected to the cell case. It is tied to pin 5 of the "A" section of a control module or pin 7 of the "B" section of a control module.

Operation of the "A" section of a module is as follows: When the control voltage reaches the set point, usually about 850 mv, the voltage is sufficient to cause Q2 to conduct. Conduction of Q2 provides base drive for Q1, causing it to conduct. Gain of the circuit is determined by the setting of a potentiometer R3. Gain is increased by moving the wiper toward the collector of Q2, which is counterclockwise rotation of the adjustment screw. Full counterclockwise rotation of R3 provides maximum sensitivity of the module to control voltage.

The collector current of Q1 provides base drive for the bypass transistor 2N3235. A reed relay in series with the bypass transistor is set to close at 2.7 amps of bypass current. The closing of the reed relay lights the appropriate indicator lamp. Setting of the reed relay to come on at 2.7 amps of bypass current assumes that 300 milliamps of charge current is sufficient to keep a cell fully charged. The charge current can be measured by observing the voltage between Test Point 1, pin 11 and Test Point 3, pin 12. The bypass current flows through the parallel combination of R1 and R2.

The parallel resistance is 0.05 ohms, so the correspondence between voltage and bypass current is 50 millivolts per amp.

Automatic testing equipment has been designed to sequentially scan 156 data points within the battery bank. The 156 point scanner is divided into three scans of 52 data points each. The first scan measures the terminal voltage of each cell. The second scan measures the control voltage of each cell. The third scan measures the voltage drop across the parallel combination of R1 and R2 which yields bypass current of each cell in the ratio of 50 millivolts per amp previously mentioned.

The indicator lights are powered by a separate regulated power supply which operates from the 115 volt 60 Hz line. A press-to-test switch assures the operator that all indicator lamps are functioning. Battery discharge current passes through the 20 amp circuit breaker into the positive load terminal on TB1. This bypasses the charging current ammeter shunt. Battery current is the difference between charge current and load current. The 10-turn current-adjust potentiometer is used to adjust the current regulator in the constant current cell charger located within the Slave Power Conditioner box.

3.6 CONTROL AND FAIL-SAFE CIRCUITS

The control and fail-safe circuits are shown schematically in Figure 28. The system power is 208 volt, 3 phase, 30 amp, 60 Hz. Power input connection to the system is made by P19, a four prong 30 amp Hubbel connector located on the top of rack number 2. No power is applied until the rack power circuit breaker CB1 is closed. Closing CB1 energizes the power strip in the back of rack number 2. The analog instrumentation and the battery bank indicator lights are powered from this strip. This allows the analog instrumentation to be powered continuously to avoid warmup drifts.

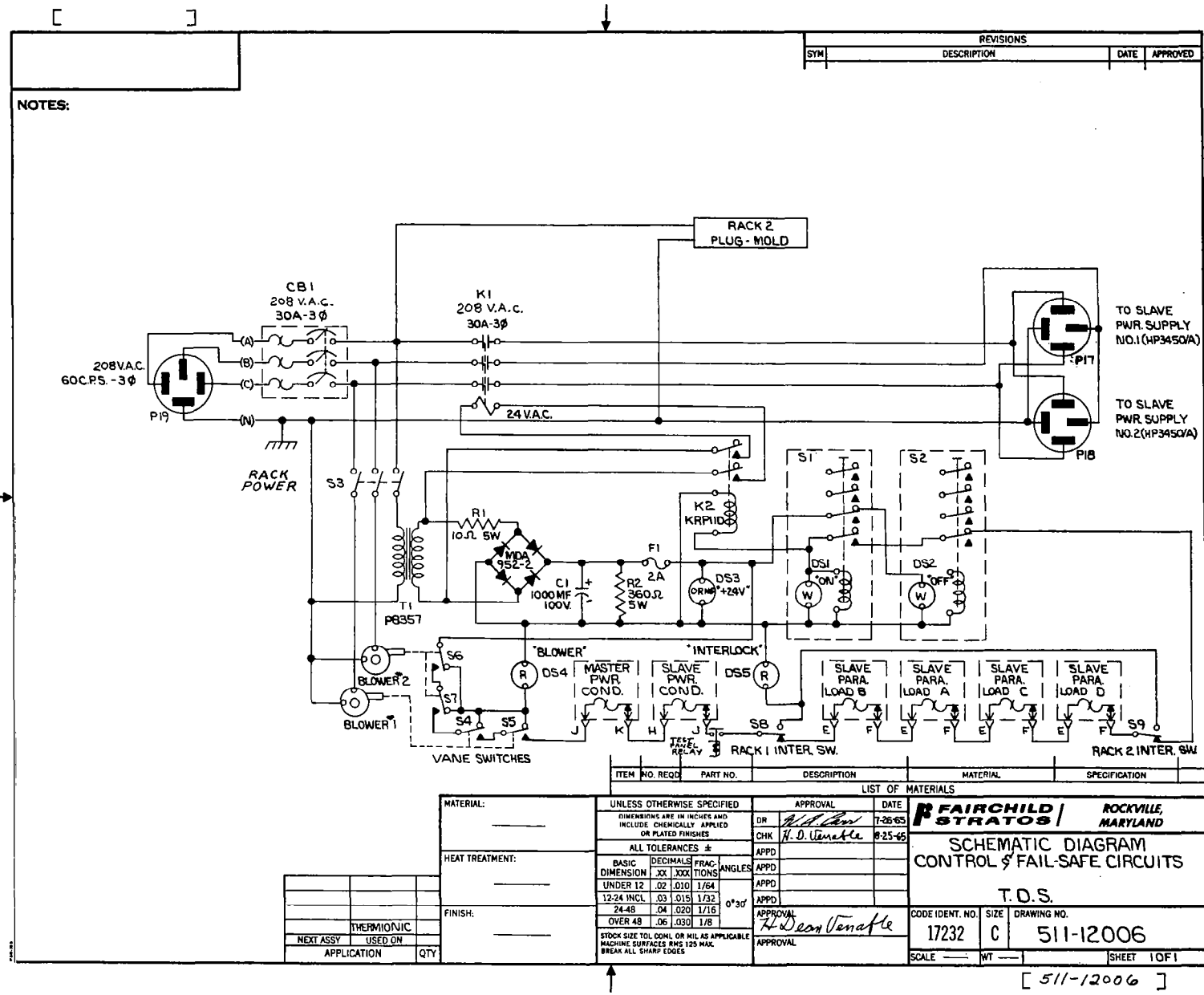

NOTES:
REVISIONS
SYM
DESCRIPTION
DATE
APPROVED
RACK 2 PLUG-MOLD
CB1
208 V.A.C.
30A-3Ø
K1
208 V.A.C.
30A-3Ø
208V.A.C.
60C.P.S.-3Ø
P19
(A)
(B)
(C)
(N)
24 V.A.C.
TO SLAVE PWR. SUPPLY NO.1 (HP3450/A)
TO SLAVE PWR. SUPPLY NO.2 (HP3450/A)
P17
P18
RACK POWER
S3
R1
10Ω 5W
MDA 952-2
C1
1000 MF 100V.
R2
360Ω 5W
F1
2A
K2
KRP11D
DS3
+24V
S1
S2
DS1
"ON"
DS2
"OFF"
T1
P8357
BLOWER 2
BLOWER 1
S6
S7
S4
S5
VANE SWITCHES
"BLOWER"
"INTERLOCK"
DS4
DS5
MASTER PWR. COND.
SLAVE PWR. COND.
SLAVE PARA. LOAD B
SLAVE PARA. LOAD A
SLAVE PARA. LOAD C
SLAVE PARA. LOAD D
TEST PANEL RELAY
S8
RACK 1 INTER. SW.
S9
RACK 2 INTER. SW.
ITEM
NO. REQD
PART NO.
DESCRIPTION
MATERIAL
SPECIFICATION
LIST OF MATERIALS
MATERIAL:
HEAT TREATMENT:
FINISH:
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
ALL TOLERANCES ±
BASIC DIMENSION
DECIMALS .XX .XXX
FRACTIONS
ANGLES
UNDER 12 .02 .010 1/64
12-24 INCL .03 .015 1/32
24-48 .04 .020 1/16
OVER 48 .06 .030 1/8
0°30'
STOCK SIZE TOL COMM. OR MIL AS APPLICABLE
MACHINE SURFACES RMS 125 MAX.
BREAK ALL SHARP EDGES
APPROVAL
DATE
DR
T-26-65
CHK
H. D. Venable
8-25-65
APPD
APPROVAL
H. Dean Venable
APPROVAL
THERMIONIC
NEXT ASSY
USED ON
APPLICATION
QTY
FAIRCHILD STRATOS
ROCKVILLE, MARYLAND
SCHEMATIC DIAGRAM
CONTROL & FAIL-SAFE CIRCUITS
T.D.S.
CODE IDENT. NO.
17232
SIZE
C
DRAWING NO.
511-12006
SCALE
WT
SHEET 1 OF 1
[511-12006]
[511-12006]

Figure 28

Closing switch S3 energizes the two rack blowers and the fail-safe and control circuitry. When S3 is closed the red blower light will come on momentarily until the blowers reach their operating speed. The red "OFF" push button will also light. In normal operation the green "ON" push button will light and latch in when depressed. The three phase relay, K1, will be automatically energized, applying power to the two Slave Power Supplies.

The system can be turned on only when the series fail-safe circuit is complete. Failure of the system to turn on can be the result of discontinuities in the fail-safe circuit caused by any one of the following:

- blowers not up to speed
- dirty air filters
- improper or lack of mating of system plugs
- open rack doors
- absence of Thermionic Diode or equivalent power input

The entire system can be made fail-safe by adjusting the upper and lower set points of the meter relay limit switch on the Thermionic Diode test panel near the desired operating point. Any significant change will then disconnect both Thermionic Diode racks from the ac line, simultaneously opening a relay in the fail-safe line and turning off the Slave Power Supplies.

3.7 TEST POINTS

There are 63 system test points. They are located on a 7 x 7 matrix on the input meter panel and a 2 x 7 matrix on the output meter panel. The test points are logically grouped and color coded.

Test points 1 through 7 are for Slave Parasitic Load A. White test points are electrical test points within the box and are referenced to the Slave input ground, test point 41. The three yellow test points, 4, 5, and 6 are temperature monitoring test points and are resistances measured with respect to

temperature common, test point 7. The resistance between test point 4 and test point 7 is thermistor 1. The resistance between test point 5 and test point 7 is thermistor 2 and the resistance between test point 6 and test point 7 is thermistor 3. Test points 8 through 14 are arranged in a similar manner and are associated with Slave Parasitic Load B. The white test points 8 through 10 are again referenced to input ground, test point 41. Test point 14 is the common for the three yellow temperature test points. The same system is repeated on the output meter panel for test points 50 through 63. Test point 56 is the temperature common for temperature test points 53, 54, and 55 and test point 63 is the common for temperature test points 60, 61 and 62. The ground reference for white internal test points 50 through 52 and 57 through 59 is again TP41.

Test points 15 through 28 are for the Master Power Chain. Test points 15 through 20 are input test points and are referenced to TP21. Test point 22 is an output test point and is referenced to TP23. TP24 through 27 are for thermistors 1 through 4 respectively and are referenced to thermistor common TP28.

Test points 29 through 49 are for the Slave Power Conditioner. Test points 29 through 34 are output test points and are referenced to TP42. Test points 35 through 40 are input test points and are referenced to TP41. Test points 43 through 48 are thermistors 1 through 6 respectively and TP49 is thermistor common.

3.8 THERMIONIC DIODE INTERFACE

The only connections necessary between the two Thermionic Diode racks and the two Thermionic Diode Controlled Power System racks are the diode power output and the fail-safe. The fail-safe requires two connections to the terminal block on the right rear corner of the Thermionic Diode test chassis.

4.0 MECHANICAL DESIGN AND PACKAGING

4.1 OVERALL SYSTEM

Mechanical design and packaging tasks were mainly concerned with the following items:

- design of sealed containers to package the electronics which must operate in a vacuum chamber
- design of conductors and connections capable of high current distribution with low loss
- layout and packaging of relay racks and peripheral equipment which need not operate in a vacuum chamber

The "vacuum chamber" electronics is subdivided into separate black boxes in order to maintain good thermal equilibrium in both vacuum and room environment and to provide ease of handling. Figure 29 is representative of this subdivision.

Thermal equilibrium is achieved within each box by immersing all components in an ebullient coolant. Effective and predictable use of ebullient coolants requires that only coolant liquid and vapor be present. The fluid selected, Minnesota Mining and Manufacturing Company FC–75, has a vapor pressure on the order of 30 mm Hg at 25°C. A sealed box containing only FC-75 at 25°C will show a vacuum. When the box is dissipating heat, however, its internal pressure will rise. In the case of the Slave Parasitic Load it will rise to 760 mm Hg absolute. Pressure differentials while the box is in a vacuum environment are as high as 760 mm Hg. Operation, both in the laboratory and in the vacuum chamber, requires reliable long term positive seals against a plus or minus one atmosphere pressure differential.

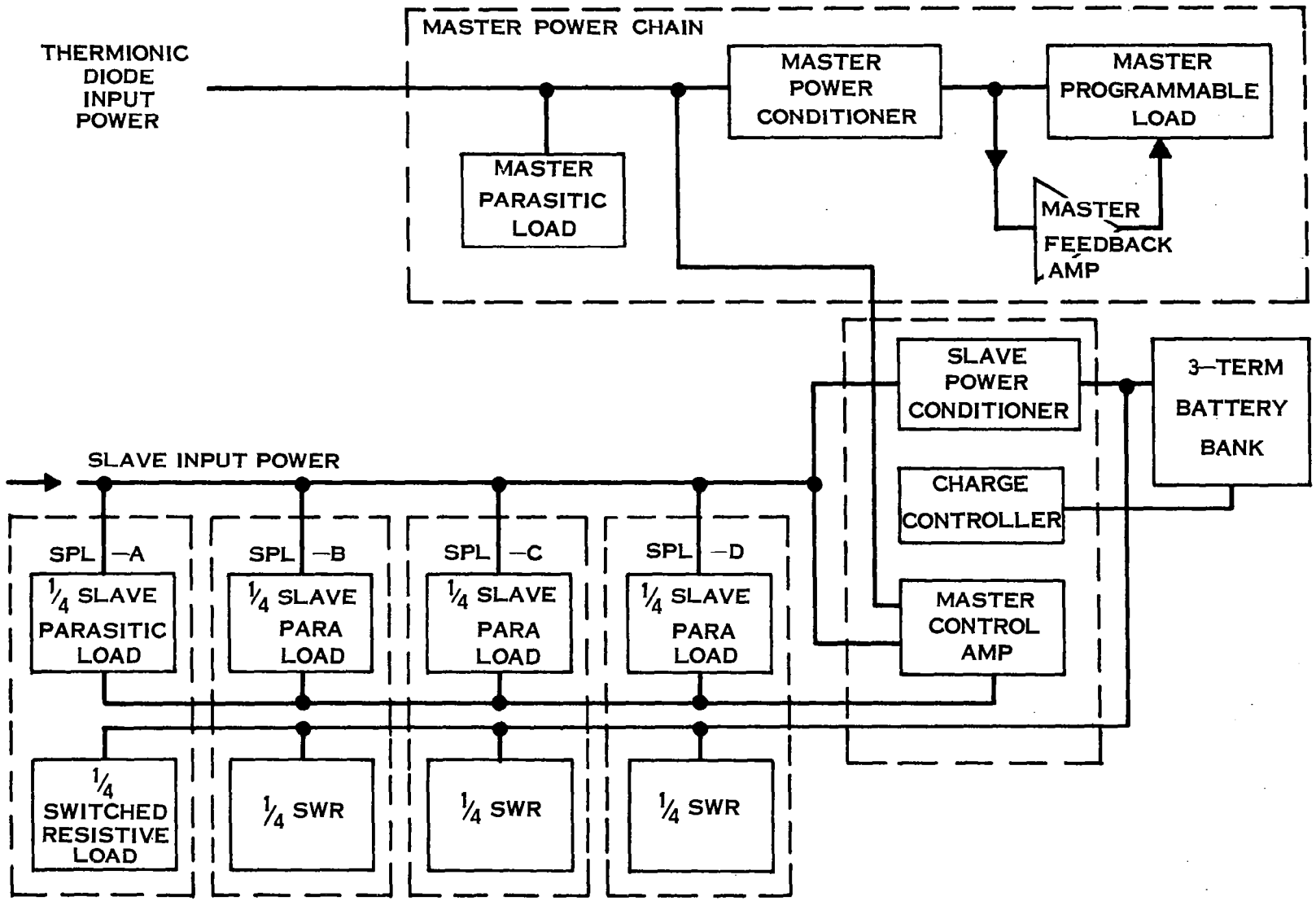


Figure 29 Component Location in Boxes

The six "vacuum" boxes share the same basic design. The top and bottom halves of the boxes are similar, each being machined from a solid block of aluminum with the mating surface flat to ±.0005 inches. Hermetic sealing between mating halves is achieved through the application of grade AV red loctite on the mating surface immediately prior to assembly. When cured, the loctite gasket will not be affected by the temperature extremes or the cyclic positive-negative pressure profile which the system must withstand.

Low-current lead penetrations are made through hermetically sealed glass-to-metal connectors. High-current lead penetrations require Fairchild Hiller designed bus bar feed-throughs.

Figure 30 is a pictorial representation of bus bar feed-through fabrication. Advantages of this feed-through technique include mechanical strength, the lack of a discontinuity in the current path, and relative ease of disassembly.

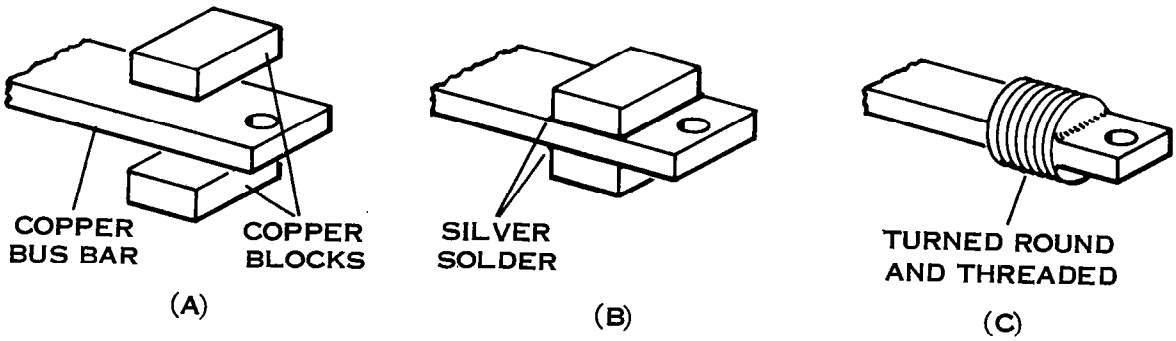


Figure 30 Bus Bar Modification

The Martin hard coat is the electrical insulation used between bus bar and case. Triple redundancy is provided by the threaded aluminum bushing also protected by Martin hard coat (see Figure 31). Hermetic sealing of the bus bar penetrations is achieved through application of grade HV brown loctite on all mating threads.

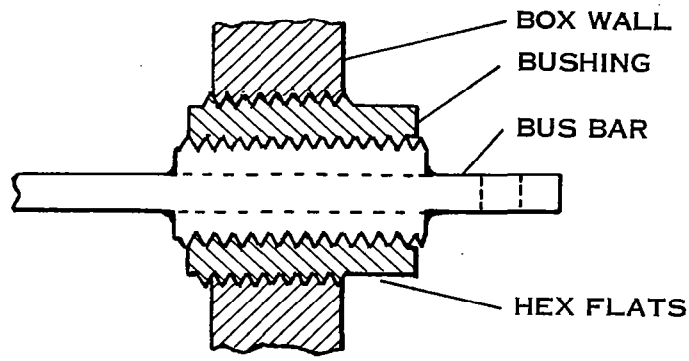


Figure 31 Bus Bar/Bushing Assembly

Figure 32 is a view of a typical hermetically sealed box. Exterior walls of the box are thick enough to provide for tapped mounting holes and structural rigidity adequate to support heavy components, and to withstand high internal and external pressure.

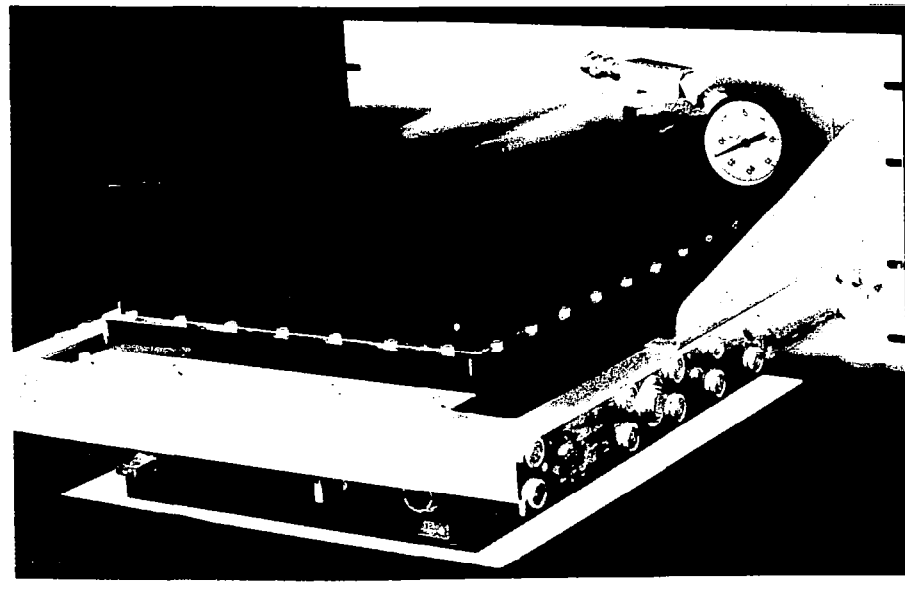


Figure 32 Typical Hermetically Sealed Box

To make good electrical contact to the power transistors and also to carry heat away, a thermal clamp was devised. The clamp was made to fit the case of MHT 2211 transistors, which are the type used for switching in both power conditioners. The clamp is shown in Figure 33.

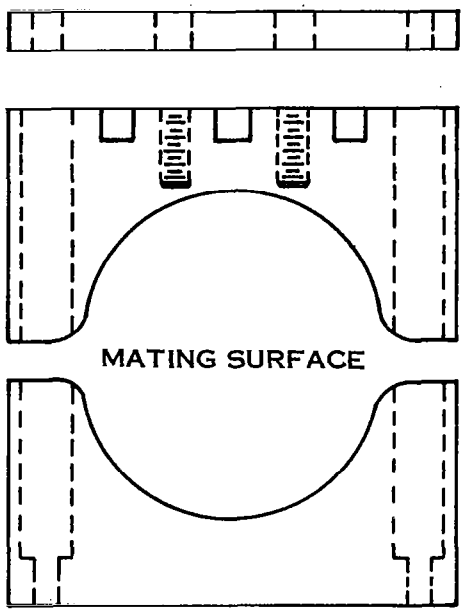


Figure 33 Thermal Mounting Clamp for MHT 2211

A MHT 2211 was squeezed between the two main halves of the clamp. Since the collector was common to the case, the clamp was used to make electrical contact to the collector. In the case of the switching transistors, the transformer windings needed to be connected to the case. This was done by cutting wedge-shaped slots in the top of the clamp block. The square wires from the transformer were then pressed down into the slots and held in place by the top bar. The two mounting studs and additional screws were used to hold the bar in place.

The high surface contact area made the joint extremely low in electrical resistance. When the collector was to be connected to a bus bar, as in the Master Parasitic Load, the thermal clamp was bolted directly to the bus bar. In other cases, an insulator was used under the clamp.

4.2 RACK LAYOUT

Figure 34 shows the positions of the system components in the racks.

The Slave Parasitic Load is equally distributed among four boxes to limit the power dissipation of each box to 600 watts. This was necessary in order to radiate the thermal energy without excessive temperature.

The input meter panel contains the master and slave input voltage and current meters and test points 1 through 49. The test points are for troubleshooting the various boxes mounted in rack 1. The test points on the output meter panel are for boxes in rack 2.

The Slave Power Conditioner is in a separate box. Also contained in the Slave Power Conditioner box is the Master Control Amplifier and the battery charge-current regulator.

The master power chain is contained in one box. This includes the Master Parasitic Load, the Master Power Conditioner, and the Master Programmable Load.

Blowers are mounted in each rack above the slave power supplies. They are of the dual centrifugal fan type, and are conservatively rated for long life.

The slave power supplies are rated at 300 amperes at 8 volts, and are connected in parallel. Their output current passes through a grid-type resistor located in the top of each rack. This resistor dissipates about 1000 watts in normal operation and is cooled by the rack airflow.

The output meter panel contains the master and slave output current and voltage meters, test points 50 through 63, and the switched resistive load control. The test points are for slave parasitic loads C and D and are color coded as explained in Section 3.7.

The high-current slave input interconnection is made with 1-1/4 inch by 1/4 inch silver-plated copper bus bars. All other connections and test points are through glass to metal hermetically sealed connectors.

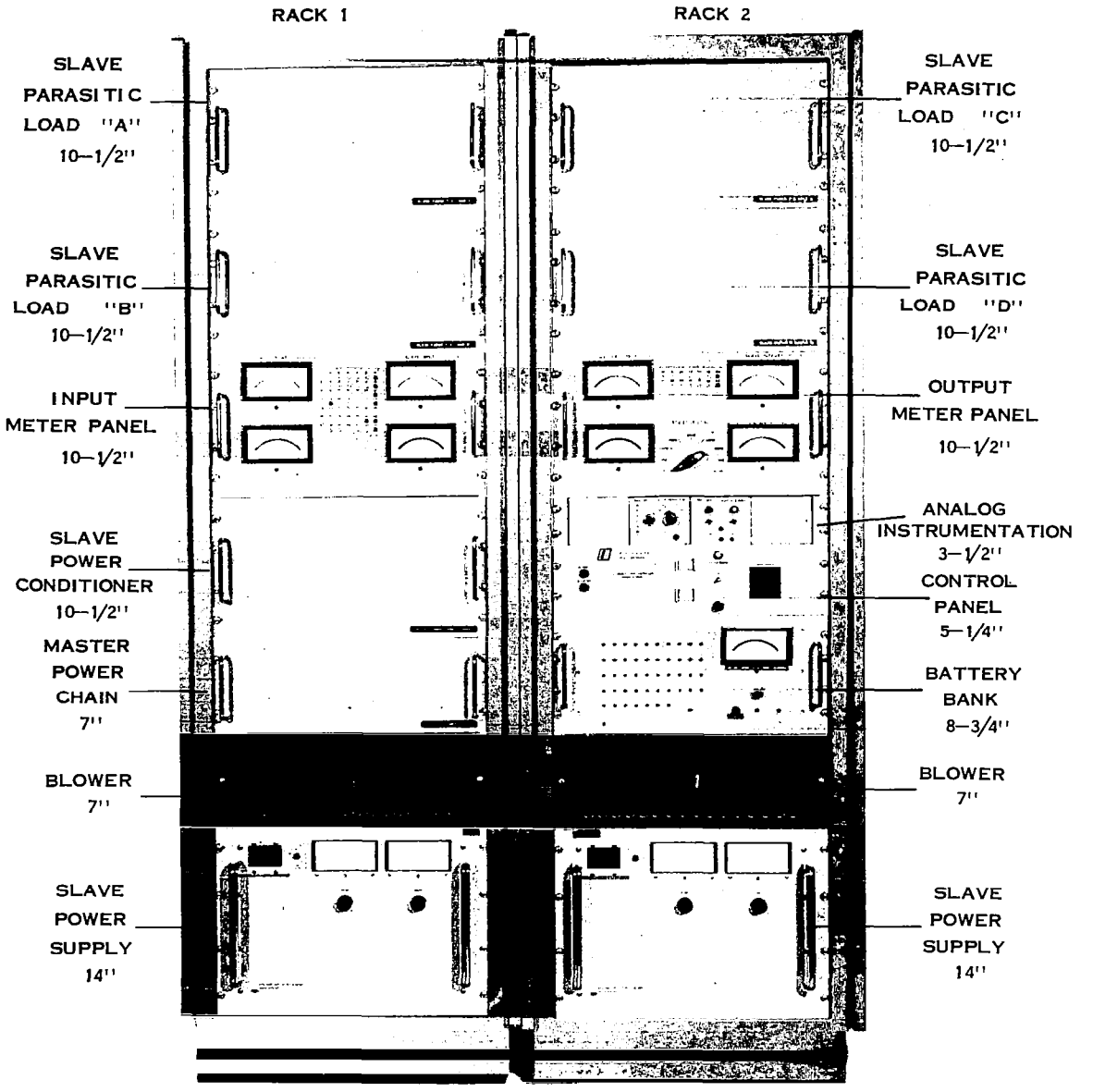


Figure 34 Rack Layout

4.3 MASTER POWER CHAIN

The entire Master Power Chain is housed in one hermetically sealed unit.

The transformer was potted with Emerson and Cummins Stycast 1090. The purpose of the potting material was to provide mechanical support for the windings during vibration, and to ease the problem of securing the core. The cylindrical potted core was fitted into a circular recess milled in the bottom of the Master Chain container. The core was then secured by a cover plate and redundantly secured by a protrusion from the Master Power Chain cover. Stycast 1090, a filled epoxy resin, was chosen for its light weight.

Two switching transistors and two parasitic load power transistors were mounted in thermal clamps on opposite sides of the core. The remaining sides of the case were provided with shelves to support the power resistors and programmable load power transistor. A printed circuit board containing the parasitic load sensor and regulator circuitry was mounted over one of these shelves.

4.4 SLAVE POWER CONDITIONER

Figure 35 shows the Slave Power Conditioner breadboard. Figure 36 shows the final configuration. The two are very similar, due to the physical constraints imposed and the successful performance of the breadboard model. The core was wound in ten 36^{o} segments. The ten switching transistors were spaced around the core to keep lead length short. Two circular copper bus bars were placed near the core for the same reason. The upper bus bar is the ground terminal. The lower bus bar is the positive five volt connection.

At one point, the finish of one winding and the start of the next are connected to transistors. On the opposite side of the core, both the start and finish are grounded. This was accomplished physically by crowding two transistors into one 36^{o} segment at one point. This left a gap on the opposite side of the core. This space was used for a diode heat sink for the output rectifier diodes.

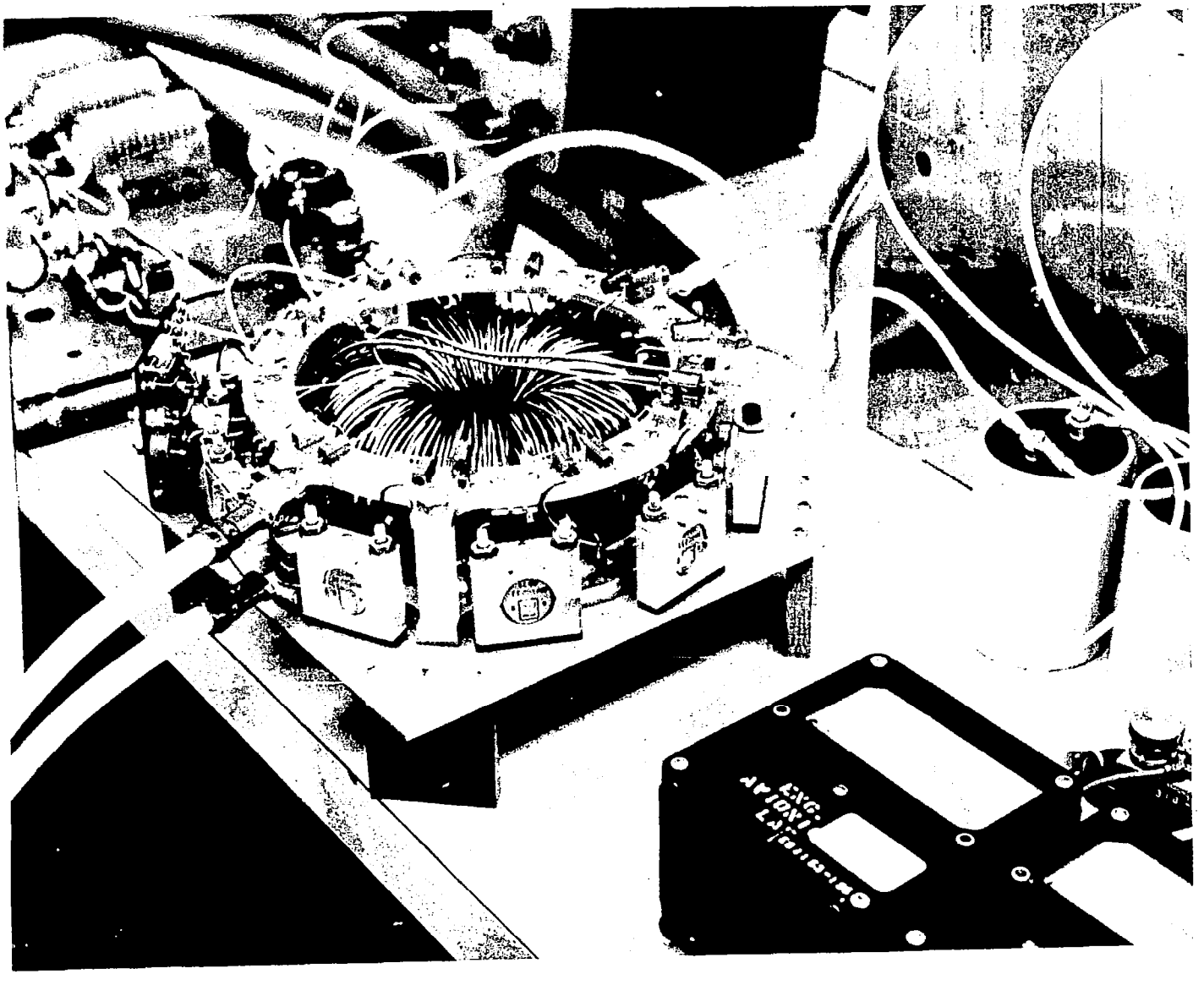


Figure 35 Slave Power Conditioner Breadboard

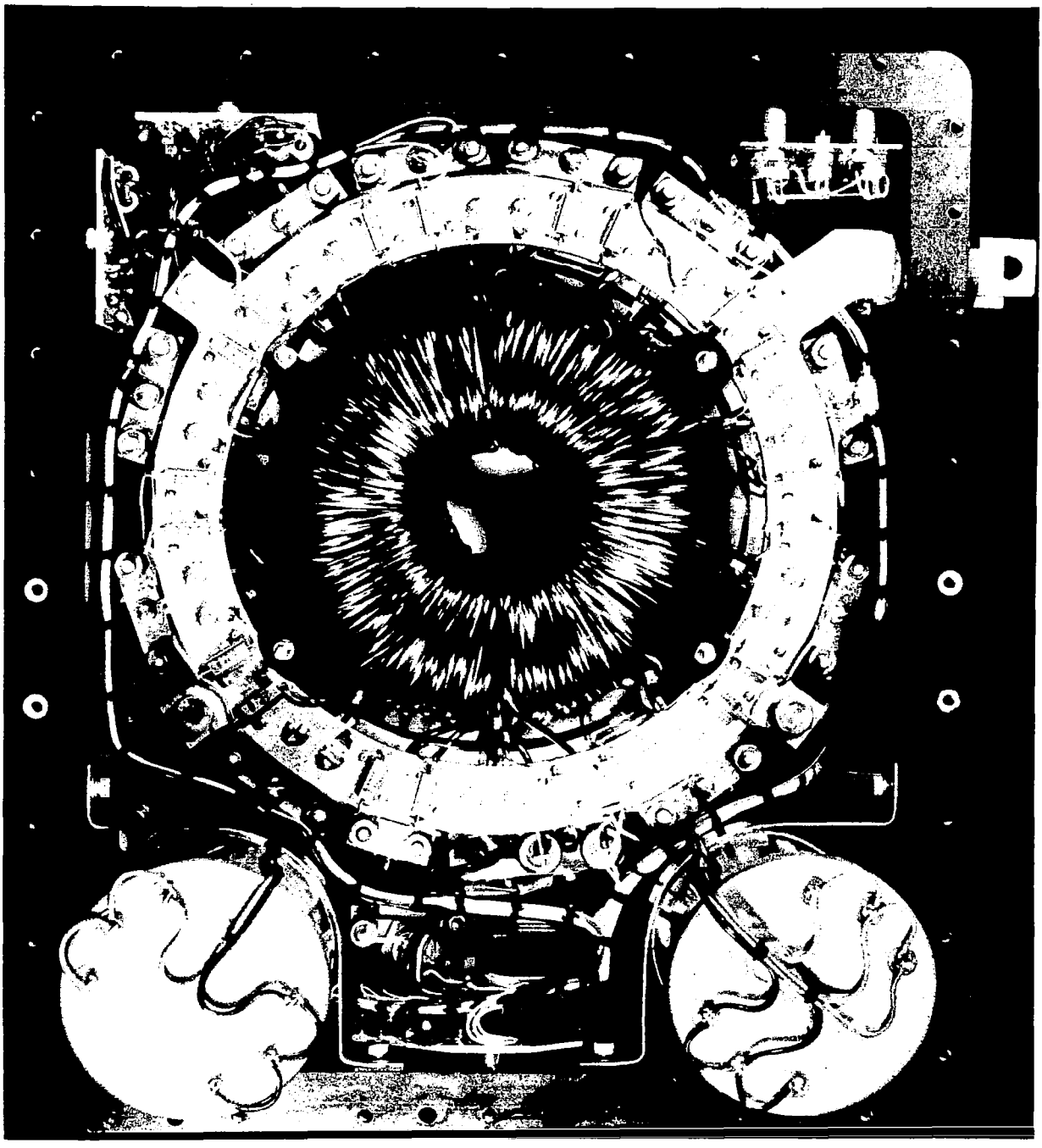


Figure 36 Final Slave Power Conditioner Configuration

Electrical contact to the number 10 AWG square wire on the transformer primary was made to the transistors as described in Section 4. 3. The grounded wires were clamped to the underside of the top bus bar with stainless steel bars. The size of the clamp bar provided contact area seven times greater than the cross-section of the wire.

Starting and drive-limiting resistors are mounted on the top bus bar for accessibility and convenience.

When viewing the finished Slave Power Conditioner box from the connector side, the two filter capacitors are located in hermetically-sealed cans on the near and far left corners. Between them is a printed circuit board containing most of the circuitry for the battery charge regulator. The ±15 volt regulator printed circuit cards are mounted in the far right corner. In the near right corner is the Master Control Amplifier, which supplies drive for the Slave Parasitic Load.

Hermetic sealing of the bus bar entrances is accomplished as described in Section 4. 3. Two hermetically-sealed connectors are used on the Slave Power Conditioner box. The small connector at the upper right carries the output current of the power conditioner. The large connector carries test points and control signals.

4. 5 SLAVE PARASITIC LOAD AND SWITCHED RESISTIVE LOAD

Thermal considerations dictate that the Slave Parasitic Load be equally divided among four hermetically-sealed boxes. The Slave Parasitic Load must dissipate about 2400 watts total in the worst case. Dividing the system into four 600 watt boxes eases the problem in the vacuum chamber, where all power dissipated must be radiated. The size, and consequent weight, of the parasitic load could be drastically reduced in a flight version by adding radiator extensions to a smaller box or boxes.

The internal arrangement of the Slave Parasitic Load box is shown in Figure 37.

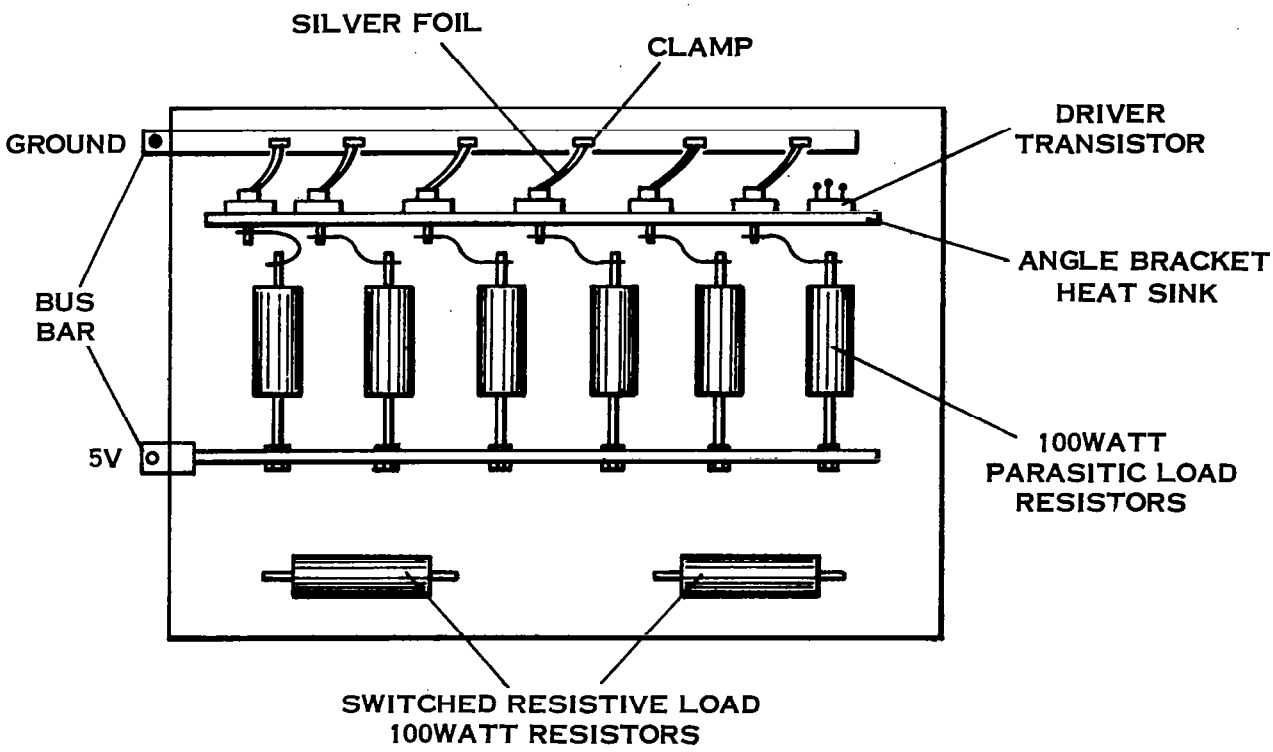


Figure 37 Internal Arrangement of Slave Parasitic Load Box

4.6 BATTERY BANK

Figure 38 shows the Battery Bank. It is designed to mount in a 19-inch relay rack and requires 8-3/4 inches of panel space. Forty-seven three-terminal nickel cadmium cells occupy the lower portion of the chassis. They are arranged in four rows of ten and one row of seven. The cells are compressed "sandwich style" to prevent bulging of the cases from the inherent internal pressure buildup.

Each cell has automatic charge control. This is accomplished by means of an electronic welded module to sense charge state and a power transistor to bypass the charging current. Two charge state sensors are located in each welded module. The modules, clearly visible in Figure 38, are mounted on printed circuit boards. An aluminum angle bracket attached to the printed circuit board functions as a mount and heat sink for the power transistors which bypass the cell charging current. Reed relays, mounted on the printed circuit board near each power transistor, are sensitive to the current flowing through the bypass transistor and are used to energize the state-of-charge indicator lamps on the front panel.

The entire module-transistor-reed relay assembly is rigid and hinged on each end. It is secured by two 1/4 turn fasteners and can be lifted after undoing the two fasteners. Figure 39 shows an assembly lifted. The tops of ten cells are clearly visible. Adjustment screws on each charge control module set the level at which charge current is bypassed.

The empty space in the rear of the battery bank (visible in Figure 38) accepts a Fairchild Hiller Corporation Model 6401-6A Charge Current Regulator. Addition of this item allows the battery bank to function independent of the rest of the system.

4.7 ANALOG INSTRUMENTATION

A Philbrick Research modular enclosure houses the analog instrumentation.

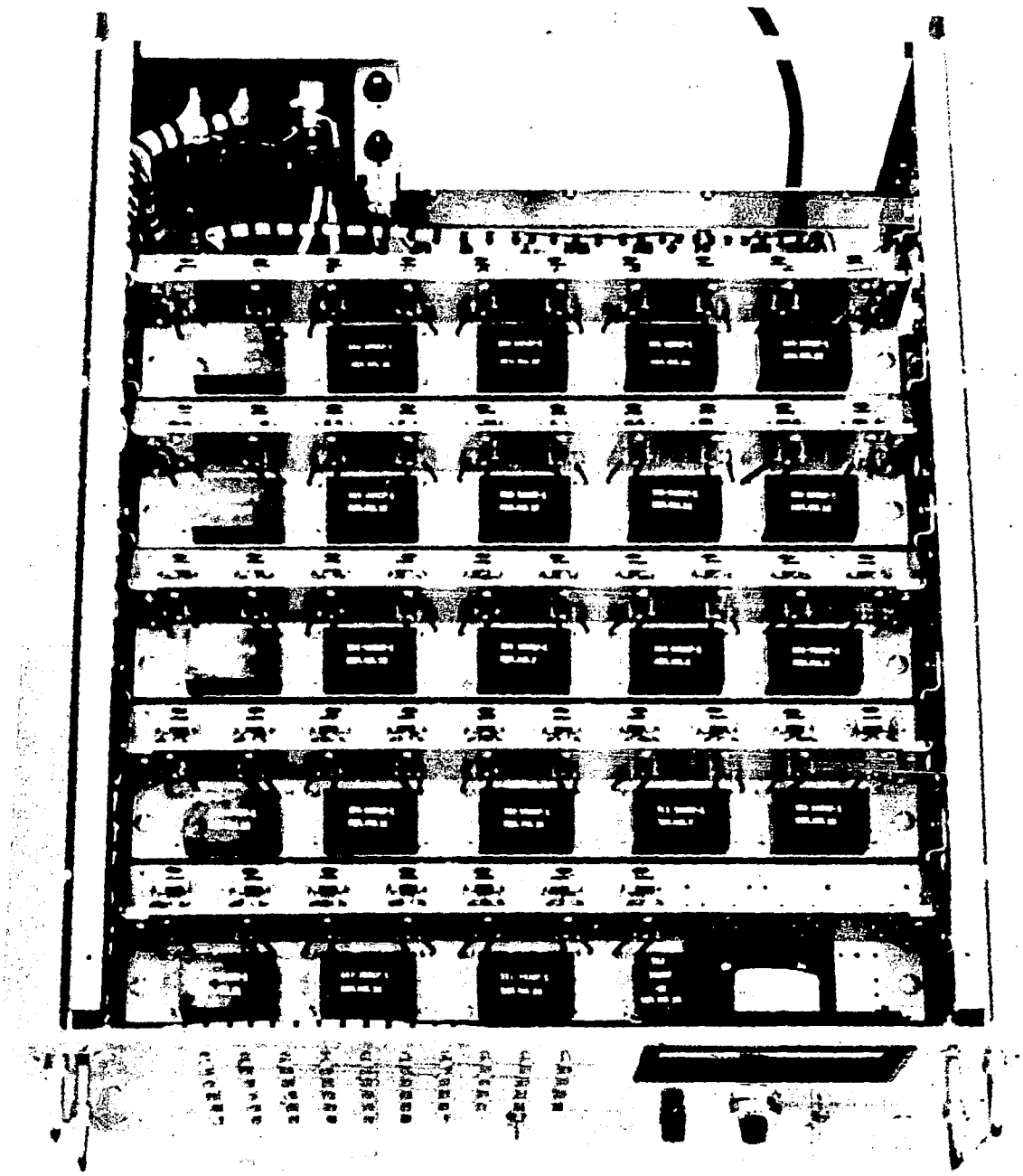


Figure 38 Three-Terminal Battery Bank

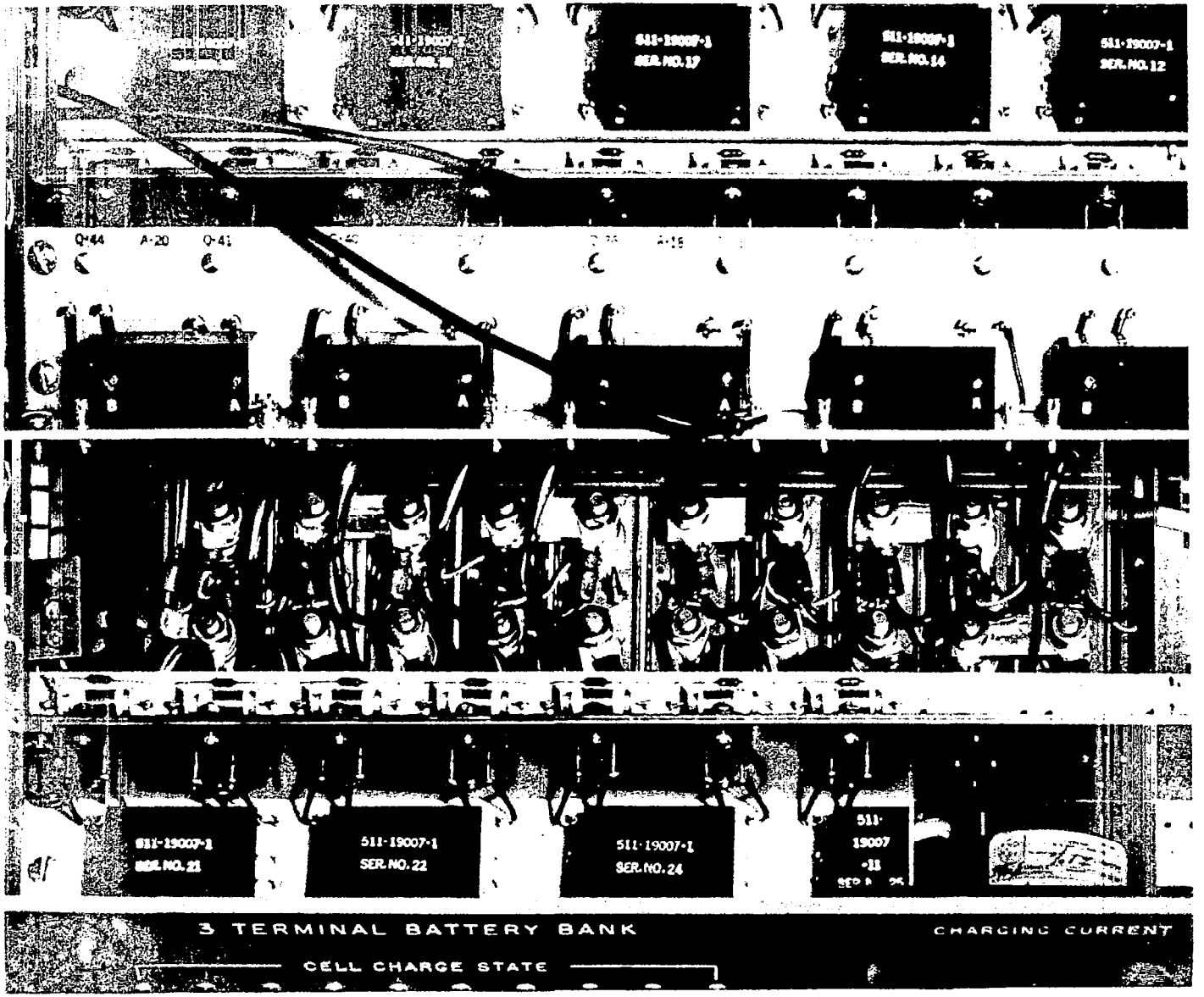


Figure 39 Battery Bank with Control Assembly Lifted to Show Individual Cells

There are four modules in the enclosure. Only two modules are presently used. One is a standard power supply, Model QPR-300. The other is the analog instrumentation circuitry. Figure 40 shows a plan view of the analog instrumentation module.

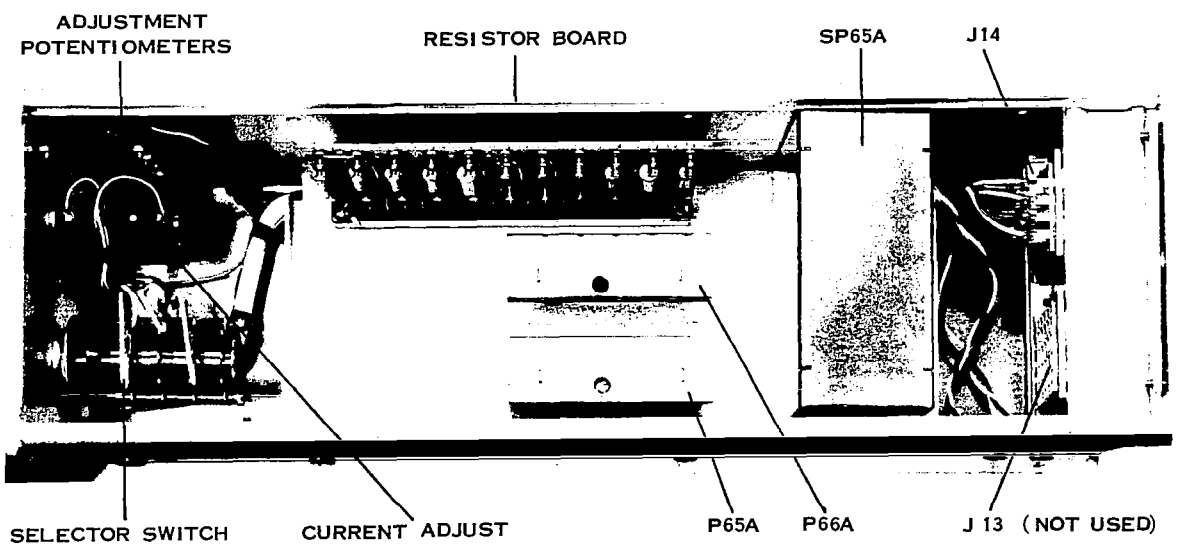


Figure 40 Analog Instrumentation Module (Top View)

The calibration adjust potentiometers are stacked along the left side of the module. They are accessible through the front panel. The current-adjust potentiometer and function selector switch are mounted on the front panel.

Fixed resistors used for scaling factors, etc, are mounted on a plug-in section of vector board. There is space for three additional resistors. Three electronic plug-in modules are also contained in the module. Power, input, and output signals all use connector J14 on the rear of the module.

5.0 THERMAL CONTROL

The thermal design for the Thermionic Diode Power Supply System required that the following tasks be accomplished:

- Selection of an ebullient coolant based on proven reliability, cost, and an experimental determination of heat transfer characteristics, chemical inertness, and electrical compatibility
- Design of sealed containers to package the electronics which are submerged in the coolant. The configuration and size of the container is such that it allows sufficient condensing area (and radiating area in the case of vacuum chamber operation) to maintain reasonable temperatures of the components for all operating conditions
- An evaluation of the effects of the components radiation interchange and the variation of temperature along the mounting plate

5.1 COOLANT SELECTION AND TESTING

5.1.1 Coolant Selection - The design of the system required tight packaging of the electronic equipment and high heat dissipation per unit volume. Chemically inert fluids possessing good electrical properties have proven to be excellent dielectric coolants in similar situations. Experience and an extensive literature survey have shown that utilization of their high heat transfer capabilities results in low component operating temperatures and reduction in system size and weight.

A program was initiated to obtain and test a number of commercially available coolants. These materials are manufactured by several chemical companies

among which are Minnesota Mining and DuPont. The fluids are referred to as "inert fluorochemical liquids" and they included:

a)	3M FC 43	Normal boiling point	337°F
b)	3M FC-75	" " "	210°F
c)	3M FC-77	" " "	194°F
d)	3M FC-78	" " "	112°F
e)	DuPont Freon E-3	" " "	306°F
f)	DuPont Fluoro-compound II	" " "	214°F
g)	DuPont Fluoro-compound IV	" " "	400°F

5.1.2 Description of Boiling Heat Transfer Experiment - The purpose of the tests was to obtain the burnout heat flux and critical temperature difference of the inert fluids, and to examine the effects of the coolant on the submerged electronics. The burnout test apparatus consisted of a kettle containing an immersed tungsten wire and the fluid which was tested at its normal boiling point. The voltage across the wire was measured at the junctions it made with copper bus bars. The resistance of the wire, obtained from voltage and current measurements, indicated the wire temperature up to 3700°K. By increasing the power in steps, a curve of heat flux versus the temperature difference between the wire and the fluid was obtained. The curves were of the Nukiyama type which is typically represented by Figure 41. As the flux in the wire approached the burnout value, the character of the boiling changed from nucleate to film and a very large, rapid temperature excursion occurred in the wire. The value of the burnout flux and the corresponding ΔT were measured by riding the hysteresis loop in the opposite direction.

The effect of the coolant on the characteristics of the electronics was studied mostly by observation. The inert ebullient coolant was introduced into an open tank in which a set of the components was mounted on a breadboard.

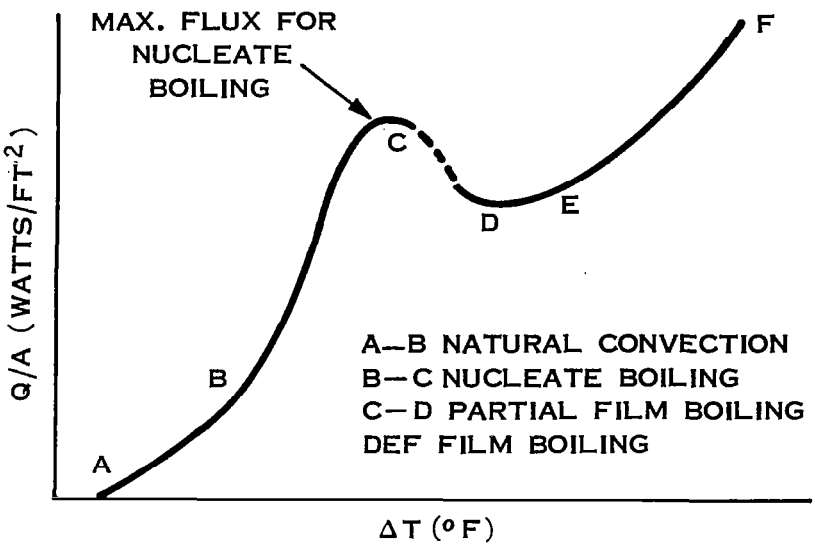


Figure 41 Boiling on an Electrically Heated Wire

Thermocouples, placed on selected components and key areas, provided data on the temperature and temperature gradients during various modes of operation. No component was allowed to reach a dangerous temperature.

Two conclusions were obtained from these tests:

1. Unless the fluid is boiling, the heat transfer is poor.
2. Three types of failures of Dale power resistors were observed for certain coolants. These were resistance element failure, failure of adhesive between resistance element and case, and case failure.

5.1.3 FC-75 Fluorochemical Coolant - Of the coolants tested only FC-43 and FC-75 met all the requirements desired for a good thermal design. Cost considerations, with no loss in quality, made it necessary to choose FC-75 as the coolant to be employed in the final design. The properties of FC-75

include thermal stability, inertness to physical and chemical change, low surface tension, and low freezing point. Another advantage is that the specific heat of its vapor state is approximately the same value as that of its liquid state.

5.2 THERMAL DESIGN OF PACKAGING PRESSURE VESSELS

5.2.1 Introduction - An analysis was performed to determine the dimensions of the pressure vessels needed to package the Thermionic Diode Power System. The containers are partially filled with FC-75 in which the power dissipating units are submerged. The space above the liquid is intended to allow for expansion and condensation. The design is such that the system will operate under reasonable temperatures and pressures both outside a vacuum chamber (with forced convection supplied by a fan) and inside a vacuum chamber with liquid nitrogen coolant circulated within the walls. No inert gas is employed, and the restrictions imposed on the operating pressure and temperature are those of boiling conditions since experiments showed that the heat transfer is best when these conditions are attained. Requirements for an acceptable design include easy handling of the system and provisions for a possible $-20^{\circ}C$ cooling of the liquid.

5.2.2 Handling of the System - The system must be at a safe temperature when taken in or out of the vacuum chamber so that no special handling techniques become necessary. This can be achieved by pouring the coolant into the pressure vessel at room temperature and pressure (no boiling) and heating it at one atmosphere (pressure vessel open) until boiling is reached. The container is then sealed and the liquid allowed to cool to room temperature. With good sealing, the resultant pressure and temperature will always result in a boiling coolant.

5.2.3 Amount of Coolant - The components are completely covered by the coolant at all conditions in order to insure maximum boiling heat transfer. The lowest level of the liquid will be reached when the temperature is lowest

and the contraction is greatest, or at some operating temperature when, in spite of the expansion of the liquid, the mass of the vapor may be a large fraction of the original liquid mass. The quantity of coolant that must be poured at room temperature can be calculated based on the minimum temperature condition provided that a constraint be imposed to assure that the liquid level does not go below the components level during the operation. The amount of coolant that should be poured into the vessel at $20^{\circ}C$ is:

$$W = (A_b L - f A_b L_c)\, \rho_{20^{\circ}C} \tag{21}$$

where W = the coolant weight, (pounds)

A_b = the base area of the vessel (ft^2)

L = level of the liquid when poured at $20^{\circ}C$

L_c = height of the component above the inner bottom of the vessel (ft.)

f = fraction of base area occupied by the component

$\rho_{20^{\circ}C}$ = density of the liquid at $20^{\circ}C$ (lb/ft^3)

L can be calculated from the relation:

$$L = L_c \left[(1.0833 - f)\, 40\bar{\gamma} + 1.0833\right] \tag{22}$$

where $\bar{\gamma}$ is the average volumetric coefficient of expansion of the coolant between $-20^{\circ}C$ and $+20^{\circ}C$, per $^{\circ}C$. The number 0.0833 is introduced as a conservative factor based on a minimum level of the coolant being 0.25 inch above a 3.0 inch high component. If the temperature of the liquid or vapor is above $20^{\circ}C$, the requirement that the liquid level not fall below the component level during operation can be satisfied by the inequality:

$$\frac{P_v V_v}{R T_v} < \rho_v\, V_o\, \bar{\gamma}\, (t_v + 20) \tag{23}$$

where P_v, V_v, T_v, and ρ_v are respectively the pressure (lb/ft^2), volume (cu.ft), temperature ($^{\circ}R$) and density (lbs/cu. ft) of the vapor, t_v is the vapor temperature in $^{\circ}C$, R is the gas constant ($ft/^{\circ}R$), and V_o is the minimum allowable

volume of the liquid at -20°C. V_o is calculated from the equation:

$$V_o = (1.0833 - f) A_b L_c$$

For values of V_o which are in the range expected in the design, Equation (23) is always satisfied.

5.2.4 Design of Pressure Vessels - The solution of the problem of heat rejection from the condensing inert gas is a compromise between the operations inside and outside the vacuum chamber. When the system is operated outside the vacuum chamber, heat is transferred by convection to the surrounding air. Measurements showed that the condensation of FC-75 on an aluminum plate exposed to still air (free convection) is achieved by a convective heat transfer coefficient between 0.05 and 0.10 watts/in^2/°C. Forced convection improves this coefficient to about 0.50 watts/in^2/°C. A fan of moderate capacity is used when the system is operated in air. The size of the containers which house the components must be such that the heat dissipated by the components at the boiling temperature is equal to the heat convected on the surface of the vessel. The model used in the analysis is shown in Figure 42.

In steady state operation, the rate of heat flow from the component surface (Q_d) which is equal to the heat convected on the container surface (Q_a) can be shown to be:

$$Q_d = Q_a = U_{cond} A_{cond} (T_v - T_a) \text{ watts} \quad (24)$$

where $$U_{cond} = \frac{1}{1/h_m + \delta/k + 1/h_a} \quad (25)$$

is the overall heat transfer coefficient, and

A_{cond} = area normal to heat flow (ft^2)

T_v = vapor temperature (°C)

T_a = air temperature (°C)

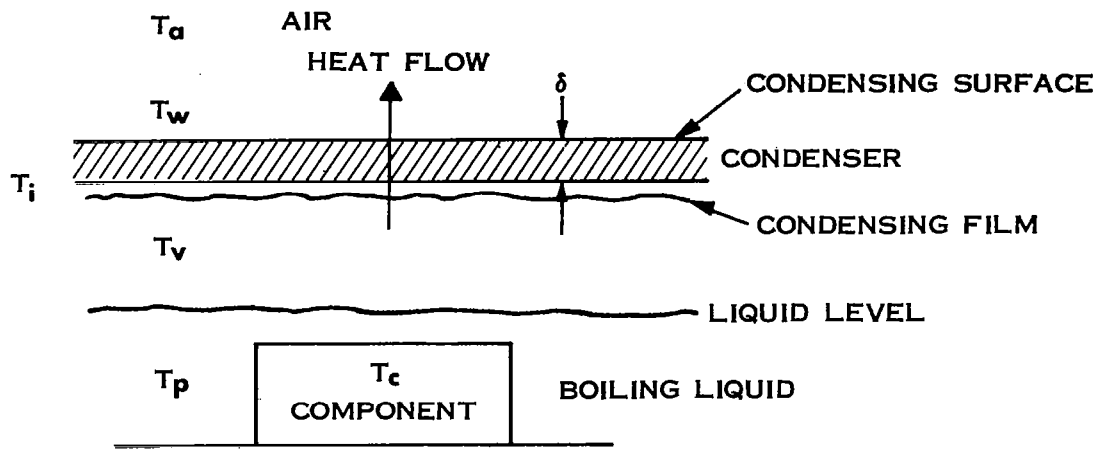


Figure 42 Convective Heat Rejection at Condensing Surface

h_m = film coefficient of heat transfer (watts/ft^2/^{o}C)

h_a = air coefficient of heat transfer (watts/ft^2/^{o}C)

δ = condenser thickness (ft)

k = condenser thermal conductivity (watts/ft^2 ^{o}C/ft)

The value of $Q_d = Q_a$ in Equation (24) is specified by the dissipation of the component at some $T_c \approx T_v$. The air temperature, T_a, is specified by the ambient conditions. The product

$$K = U_{cond} A_{cond} \tag{26}$$

may be changed at will by varying A_{cond} or δ/k or both. The choice of the factor K in Equation (26) must conform with the working conditions in the vacuum chamber.

For steady state operation in the vacuum chamber two conditions must be satisfied:

1. The heat dissipated by the electronics, Q_d, must be radiated by the walls of the container at the same rate (conservation of energy).

2. The rate of liquid evaporation, W_v must equal the rate of condensation (conservation of mass).

The general configuration of the units comprising the Thermionic Diode Controlled Power System is shown in Figure 43. The steady state rate of heat radiated by the walls is:

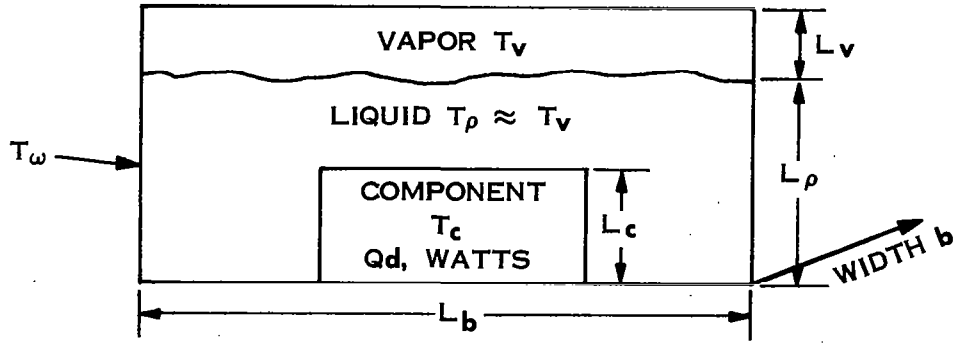


Figure 43 Steady State Operation in Vacuum Chamber

$$Q_r = Q_d = \sigma\epsilon\left[2b\,(L_b + L_l + L_v) + 2L_b\,(L_l + L_v)\right] T_\omega^4 \qquad (27)$$

where Q_r = heat radiated by the walls of the container (watts)

b = width of the container (ft)

L_b = length of the container (ft)

L_l = height of the liquid level above the inner bottom (ft)

L_v = height of the vapor space above the liquid level (ft)

T_ω = wall temperature (^oR)

σ = Stefan-Boltzman constant (0.05×10^{-8} watts/ft^2 $^oR^4$)

ϵ = emissivity of the outer surface of the container

Equation (27) assumes that the wall temperature is uniform around the casing and that it is much higher than the sink temperature (vacuum chamber walls). ϵ was taken as 0.95 which is the emissivity of Parson's Black Thermal coating.

The evaporation rate W_ν, which occurs in the vapor space, must compensate for the heat radiated by the vapor walls, and this is found to be

$$W_\nu = \frac{Q_d}{\lambda}\left[\frac{b(L_b + 2L_\nu) + 2L_b L_\nu}{2b(L_b + L_1 + L_\nu) + 2L_b(L_1 + L_\nu)}\right] \tag{28}$$

where W_ν is the condensation rate, in pounds per hour, and λ is the latent heat of evaporation of the liquid at the vapor pressure and temperature (watt-hour/lb).

In order to insure the equality of the evaporation rate and condensation rate, Equation (27) and Equation (28) are connected by the heat transfer equation across the film of condensate on the vapor walls. For each wall in the vapor region the heat flux q is given by

$$q = h_m \Delta T \tag{29}$$

h_m is the condensing film coefficient, and ΔT is essentially $T_\nu - T_\omega$. h_m is given in the literature (Reference 1) for vertical walls as:

$$h_m = 0.943\left(\frac{k_\nu^3 \rho_\nu^3 g\lambda}{L_\nu \mu_\nu \Delta T}\right)^{0.25} \tag{30}$$

where k_ν, ρ_ν and μ_ν are the thermal conductivity, density, and viscosity respectively evaluated at T_ν. g is the acceleration due to gravity. Since T_ω was assumed constant throughout the whole surface, h_m as given in Equation (30) was assumed to hold also for the horizontal top. The final equation

which relates the required dimensions to the heat dissipation and the operating temperature is found to be:

$$T_v = \left[\frac{Q_d}{\sigma\epsilon\left[2b\,(L_b + L_1 + L_v) + 2L_b\,(L_1 + L_v)\right]}\right]^{1/4} \tag{31}$$

$$= \left(\frac{\mu_v\, Q_d^{\,4}}{(0.943)^4\, K_v^{\,3}\, \rho_v^{\,2}\, g\lambda}\right)^{1/3} \left[\frac{L_v^{1/4}\left\{b(L_b+2L_v) + 2L_b L_v\right\}}{\left\{2b(L_b+L_1+L_v) + 2L_b(L_1+L_v)\right\}\left\{2b(L_v+\frac{L_b}{2})+2L_b L_v\right\}}\right]^{4/3}$$

Q_d and the maximum boiling temperature are specified for all units. The fluid properties are evaluated at T_v. L_b and b are controlled by the size of the electronics and may be chosen for all units, and L_1 can be found in terms of the thermodynamic properties and L_v from the equation:

$$L_1 = (L - fL_c)\,\frac{\rho 20^{\circ}C}{\rho_v} + fL_c - \frac{P_v}{\rho_v RT}\,L_v \tag{32}$$

where f is the fraction of base area occupied by the component, and L is the liquid level at $20^{\circ}C$ as given in Equation (22).

Equation (31) was solved numerically for the vapor space L_v necessary to maintain a temperature T_v at a component dissipation Q_d. The solution is in accordance with the conditions imposed by Equations (24) and (26). The results of the analysis are included in Table I.

5.3 RADIATION AND CONDUCTION INTERCHANGE BETWEEN UNITS

An evaluation was made to determine the effects of interradiation between the units and the temperature gradients along the mounting plate. Various modes of operation which cover the range of possible performances were considered. The analysis was based on a method introduced by Newhouse (Reference 2). The calculations showed that in a mode of maximum dissipation, radiation interchange and temperature gradient along the mounting plate cause a rise of $5.0^{\circ}C$ in the Master Power Conditioner and the Slave Power Conditioner units.

The Slave Parasitic Load temperature drops by about 3.0°C. The maximum temperature gradient on the mounting plate in this case occurs in the vicinity of the slave power conditioner and is of the order of 2.0°C. The situation during minimum dissipation similarly shows small variations in the temperatures with ±5.0°C as maximum changes.

It was found that the cold operation predicts a temperature lower than the minimum allowable for the slave power conditioner. In order to maintain a temperature slightly higher than -20°C, an external power input of 33 watts, in addition to the unit's dissipation of 77.8 watts, is required. This may be achieved in a vacuum chamber by active thermal control such as external heat inputs, or by passive control as in the use of superinsulators for reducing the heat transmitted by radiation.

The overall system with the units arranged in one plane is shown in Figure 44.

References

1. McAdams, W. H., "Heat Transmission", McGraw-Hill Book Company, 1954, pp 325 - 409.

2. Newhouse, K. N., "Radiation from a Plate with Nonuniform Heat Input". ASME paper, 64-HT-21, May 15, 1964.

TABLE I - ANALYSIS RESULTS

		Master Power Conditioner	Slave Power Conditioner	Slave Parasitic Load (one unit)
Dissipation, watts	Hot Operation	100	286	597
	Cold Operation	50	77.8	200
Outer Dimensions, in. x in. x in.		8.5 x 8.5 x 5.27	11.0 x 11.0 x 10.75	16.75 x 11.25 x 8.5
Highest Component, in.		3	5	3.5
Component Volume Percentage		50%	36%	22%
Liquid level at 20°C, in.		3.334	6.419	3.938
Liquid weight at 20°C, lbs.		6.2	28.0	29.0
Operating temperature °C	Hot Operation	30.0	50.0	100.0
	Cold Operation	-18.0	-40.0	10.0
Wall Temperature, °C	Hot Operation	29.78	49.70	99.3
	Cold Operation	-18.8	-40.10	9.94
ΔT across the wall, °C	Hot Operation	0.22	0.30	0.70
	Cold Operation	0.80	0.10	0.06
Operating Pressure, mmHg	Hot Operation	36	100	760
	Cold Operation	3	1	- -
Cold Operation additional heat input, watts		- -	33	- -

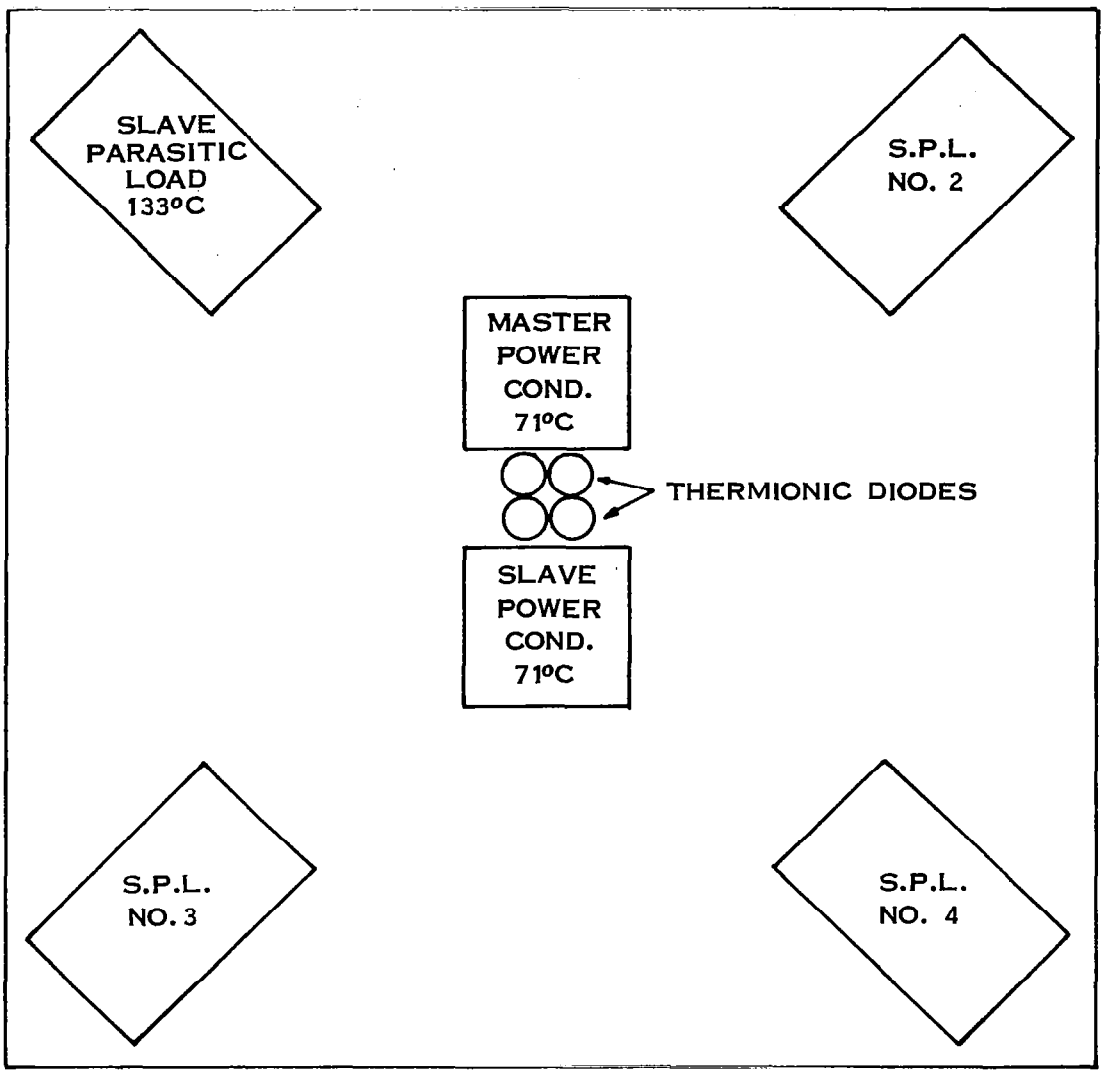


Figure 44 Vacuum Chamber Mounting Plate

6.0 TEST RESULTS

Figures 45 through 49 show the salient operating characteristics of the Thermionic Diode Controlled Power System.

6.1 MASTER PARASITIC LOAD

Figure 45 shows performance of the Master Parasitic Load with temperature and current variations. Total variation over the -20°C to +85°C temperature range is less than ±1%. Regulation from 2 to 50 amperes of pass current is also better than ±1%.

6.2 SLAVE PARASITIC LOAD

Figure 46 shows performance of the Slave Parasitic Load with current and temperature. The reference voltage in this test is 2.000 volts. Self-compensating properties of the sensing and control differential amplifier are adequate and no additional temperature compensation is employed. Regulation over the -20°C to +85°C range is better than ±1%. Current variations from 40 to 400 amperes produce voltage variations less than ±0.2%.

6.3 MASTER POWER CONDITIONER

Efficiency and regulation characteristics of the Master Power Conditioner are shown in Figure 47. Maximum efficiency is almost 84%, considerably exceeding the design goal of 70%. Voltage regulation over a 0.1 to 0.6 ampere output current range is ±2.8%.

6.4 SLAVE POWER CONDITIONER

Efficiency and regulation characteristics of the Slave Power Conditioner are shown in Figure 48. The maximum efficiency of almost 79% again exceeding the design goal of 70%. Voltage regulation of ±6.5% over a 2 to 16 ampere output current range does not compare to the Master Power Conditioner.

This is primarily because the Master operates with over 100% safety margin, compared to 20% in the Slave.

6.5 SYSTEM PERFORMANCE

Linearity of the dual-feedback system is shown in Figure 49. Data points are for various settings of the switched resistive load from 100 to 800 watts. The high Slave output voltage needed to charge the battery bank raises the power of each switched resistive load step to a level considerably beyond that originally planned. For this reason, the switched resistive load can be used to test the system over its entire design range (1000 watts) since the 800 watt setting is in reality 1064 watts.

Figure 49 shows 32 watts of Master output power for 1000 watts of Slave output power. The scaling factor is adjustable by means of R1 on the analog instrumentation module. The nominal relationship is 35 watts of Master output power for 1000 watts of Slave output power. Linearity is unaffected by changes in scaling factor adjustment.

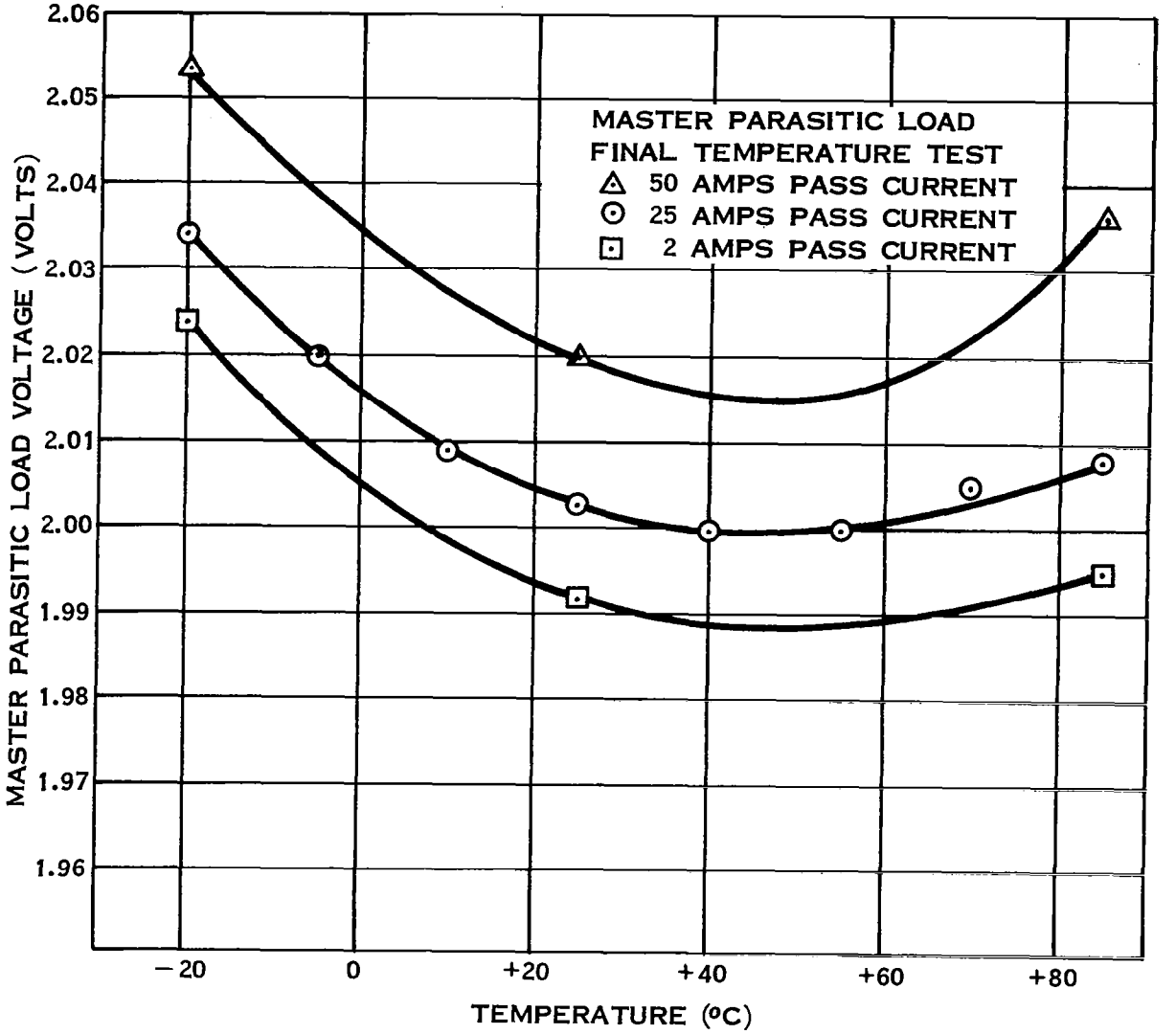

MASTER PARASITIC LOAD
FINAL TEMPERATURE TEST
50 AMPS PASS CURRENT
25 AMPS PASS CURRENT
2 AMPS PASS CURRENT
MASTER PARASITIC LOAD VOLTAGE (VOLTS)
2.06
2.05
2.04
2.03
2.02
2.01
2.00
1.99
1.98
1.97
1.96
−20
0
+20
+40
+60
+80
TEMPERATURE (°C)

Figure 45

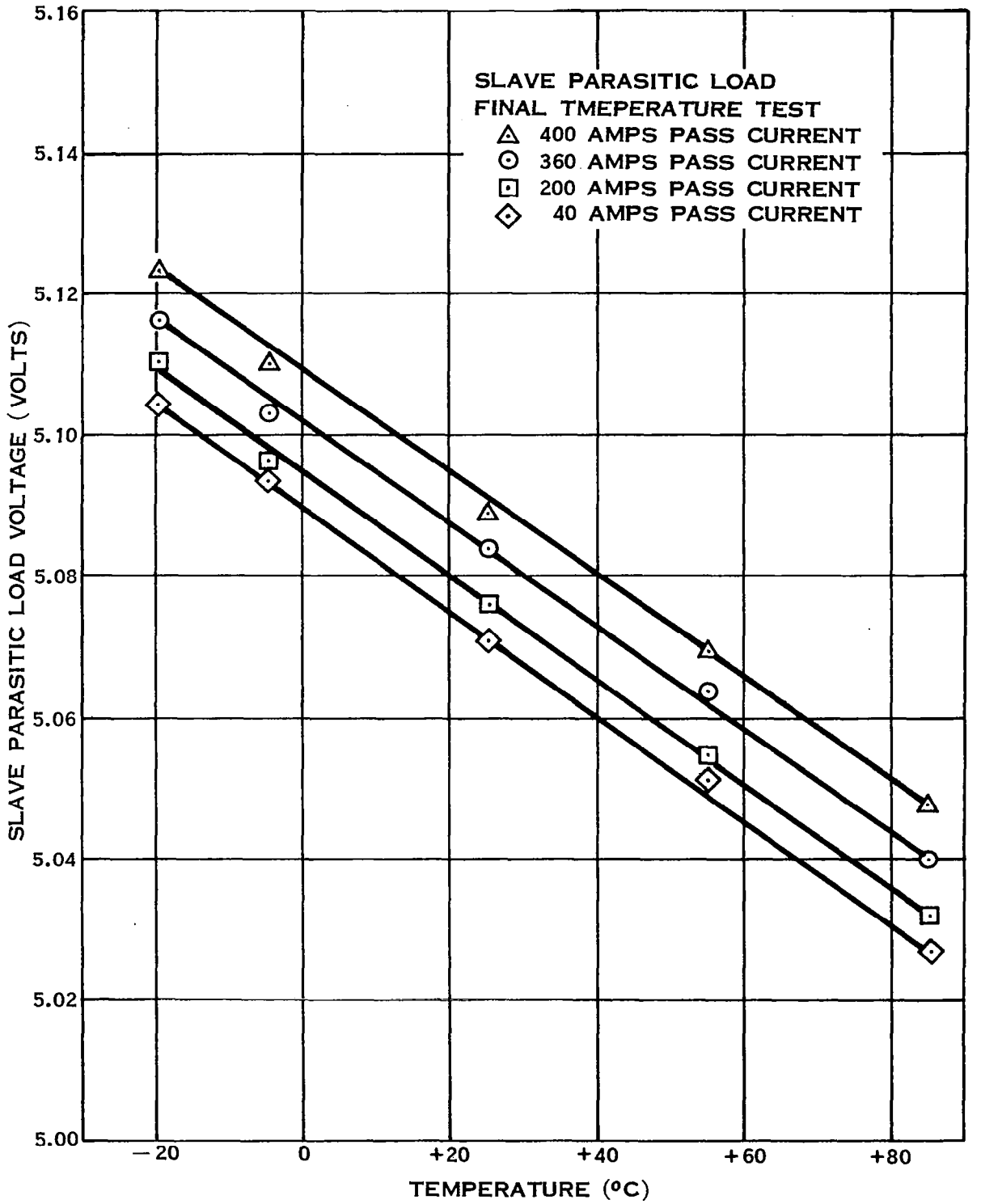

SLAVE PARASITIC LOAD
FINAL TMEPERATURE TEST
400 AMPS PASS CURRENT
360 AMPS PASS CURRENT
200 AMPS PASS CURRENT
40 AMPS PASS CURRENT
SLAVE PARASITIC LOAD VOLTAGE (VOLTS)
5.16
5.14
5.12
5.10
5.08
5.06
5.04
5.02
5.00
−20
0
+20
+40
+60
+80
TEMPERATURE (°C)

Figure 46

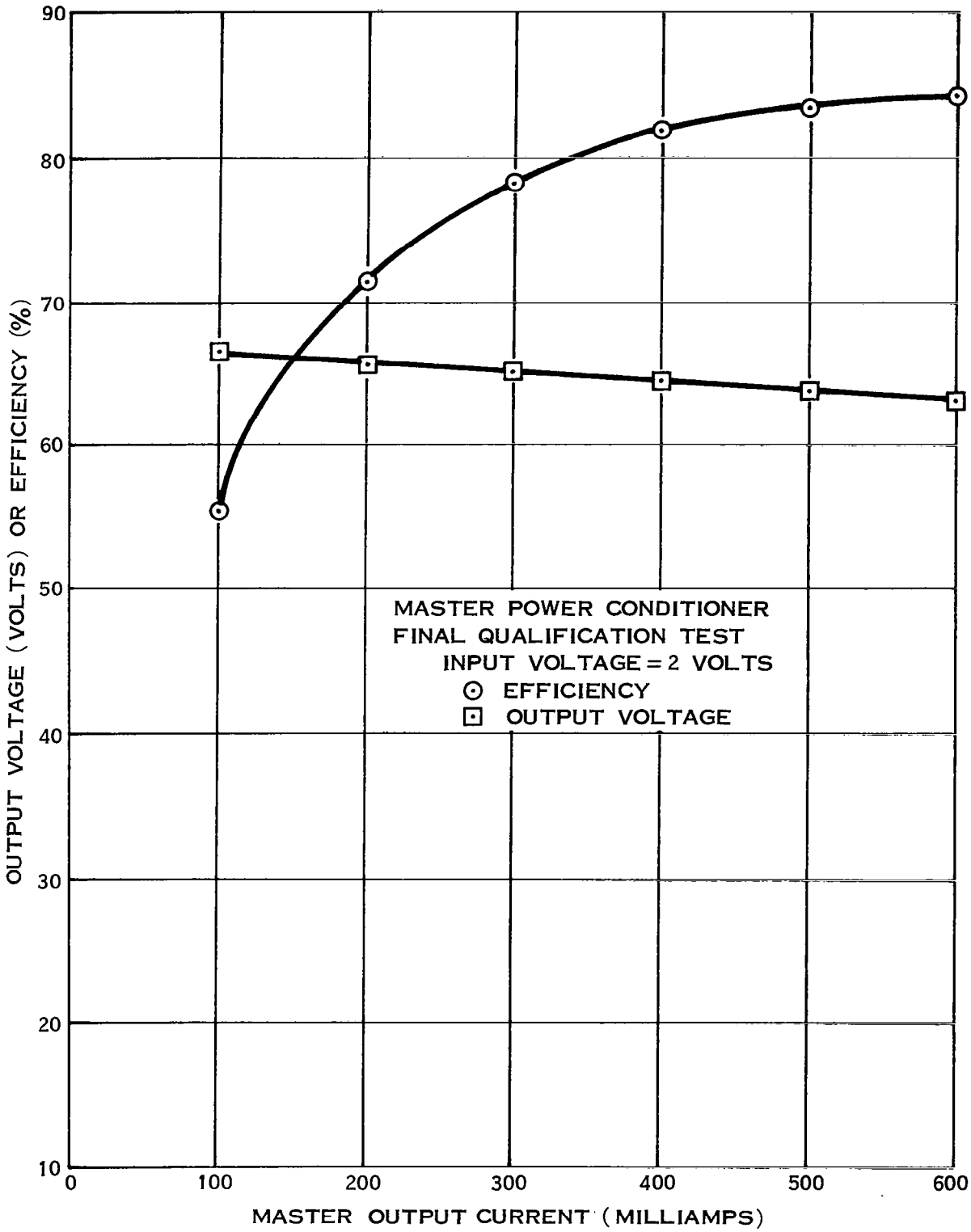

90
80
70
60
50
40
30
20
10
0
100
200
300
400
500
600
OUTPUT VOLTAGE (VOLTS) OR EFFICIENCY (%)
MASTER OUTPUT CURRENT (MILLIAMPS)
MASTER POWER CONDITIONER
FINAL QUALIFICATION TEST
INPUT VOLTAGE = 2 VOLTS
⊙ EFFICIENCY
⊡ OUTPUT VOLTAGE

Figure 47

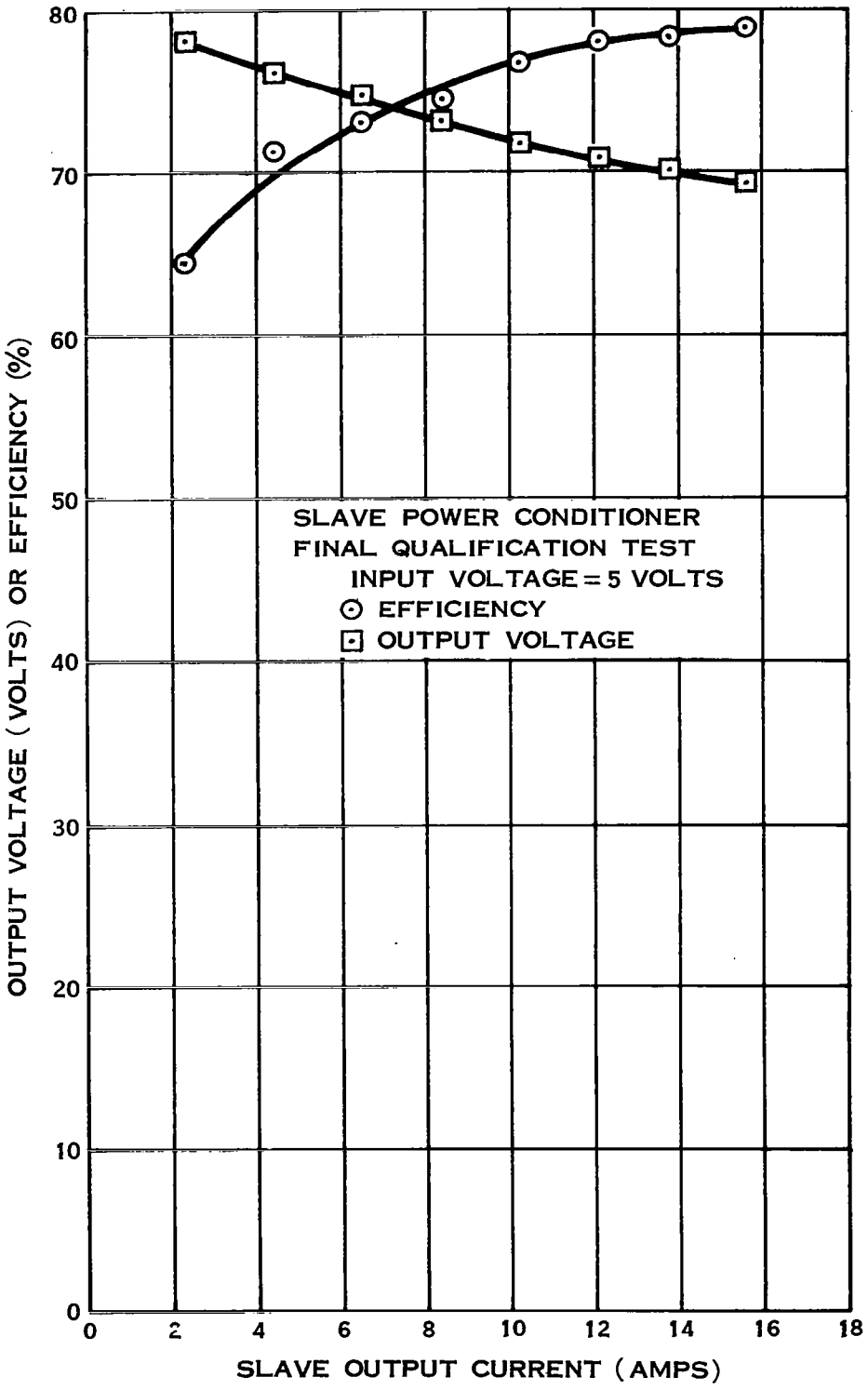

SLAVE POWER CONDITIONER
FINAL QUALIFICATION TEST
INPUT VOLTAGE = 5 VOLTS
⊙ EFFICIENCY
⊡ OUTPUT VOLTAGE
OUTPUT VOLTAGE (VOLTS) OR EFFICIENCY (%)
SLAVE OUTPUT CURRENT (AMPS)
0
10
20
30
40
50
60
70
80
0
2
4
6
8
10
12
14
16
18

Figure 48

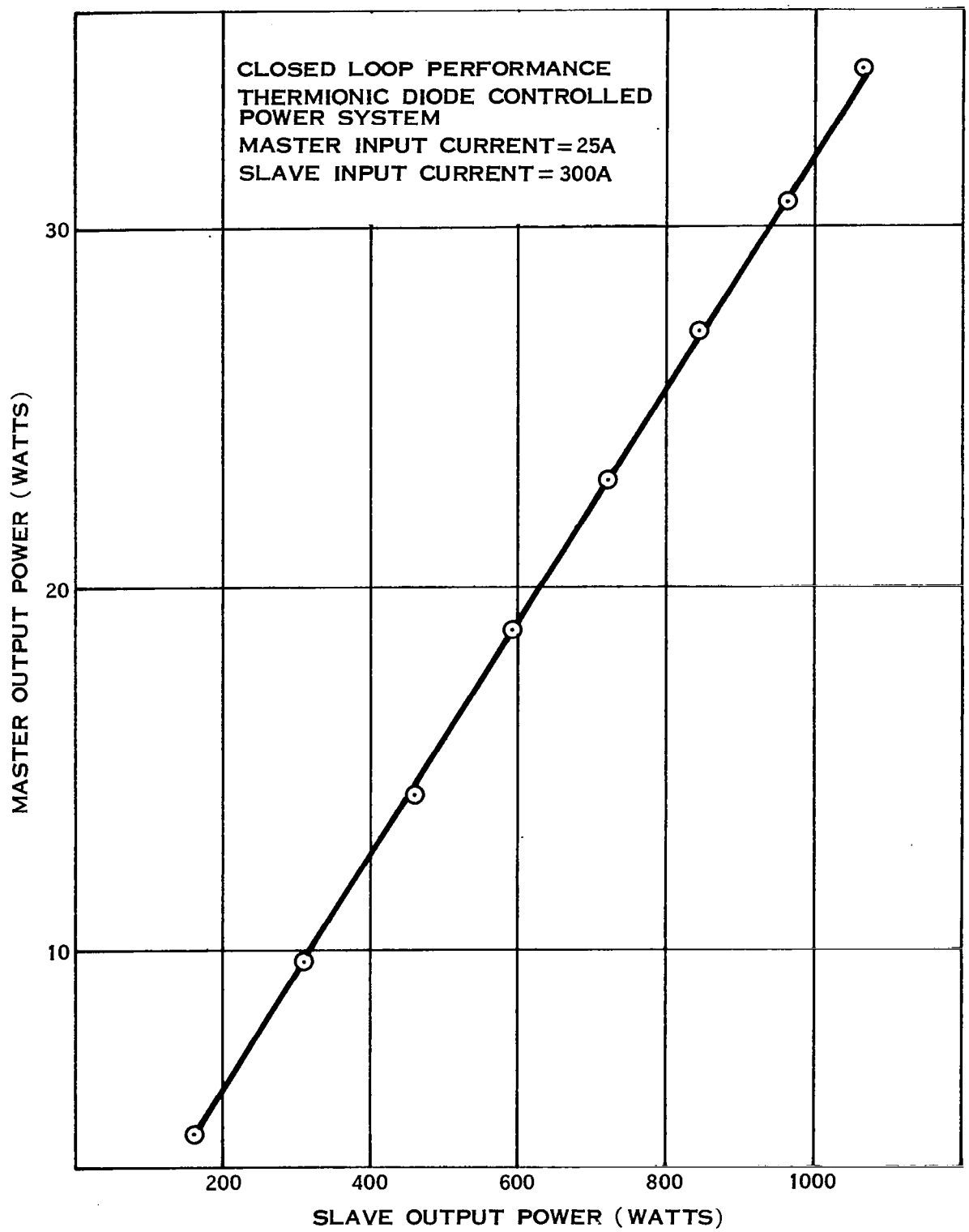

CLOSED LOOP PERFORMANCE
THERMIONIC DIODE CONTROLLED POWER SYSTEM
MASTER INPUT CURRENT = 25A
SLAVE INPUT CURRENT = 300A
MASTER OUTPUT POWER (WATTS)
30
20
10
200
400
600
800
1000
SLAVE OUTPUT POWER (WATTS)

Figure 49

7.0 CONCLUSIONS AND RECOMMENDATIONS

Development of the Thermionic Diode Controlled Power System is an unqualified success. Feasibility of high power, high efficiency, high reliability, and low input voltage power conditioning has been proven. No problems or failures of the power conditioners, parasitic loads, or feedback loops which link the system have been observed in hundreds of hours of testing. The system is intended to be a research tool for electric thrustor application studies. It should serve well in this capacity. Most of the system will operate in a vacuum, over a $-20^{\circ}C$ to $+85^{\circ}C$ temperature range, for extended mission studies.

Output voltage of the system was chosen to be 56 volts because of the power levels. During the course of development NASA policy seemed to standardize on 28 volts for all space missions, regardless of power level. It is recommended that the power conditioning, loads, and battery bank be modified for 28 volt operation to conform with NASA policy.

The system could also be modified to work with other power sources such as solar cells, fuel cells, thermoelectric generators, etc. to economically amplify their output power levels while maintaining their electrical characteristics.

Using the technology gained to produce a flight qualified system is the next logical step in the development. Higher power capability is also a worthwhile pursuit.

APPENDIX A

TRANSISTOR

SPECIFICATIONS MHT-2211

Specification No. TDS-SC-001

FAIRCHILD HILLER CORPORATION
SPACE SYSTEMS DIVISION

October 12, 1964

Written by: Karl F. Schwaderer, Proj. Engr

Approved by: C. A. Duffy, Product Assurance

TRANSISTOR SPECIFICATIONS - MHT-2211

1.0 SCOPE

The purpose of this specification is to delineate the electrical and physical characteristics of MHT-2211 transistors to be selected and matched in sets of five (5) by the manufacturer. These sets of transistors will be chosen (according to this specification) from the standard line of commercially available transistors manufactured by Minneapolis Honeywell Regulator Company, Semiconductor Division, denoted MHT-2205 and MHT-2305. It is anticipated that no other manufacturer other than M. H. T. will be solicited, therefore, this is to be considered as a sole source procurement specification.

2.0 ELECTRICAL SPECIFICATIONS

With the exception of certain parameters, the electrical specifications of this transistor (MHT-2211) are identical to those of the MHT-2205 or MHT-2305 and are listed below.

2.1 Design Limits (Single Transistors)

Junction Temperature T_j	-	$110^{\circ}C$ maximum
† Collector-to-base voltage V_{CB}	-	-15 VDC maximum
† Collector-to-emitter voltage V_{CE}		
Active Region (emitter forward biased)	-	5.0 VDC maximum
Cut-off Region (emitter reverse biased)	-	15 VDC maximum
Emitter-to-base voltage V_{EB}	-	5 VDC maximum
Collector current I_c	-	50 amp D. C. maximum
Base Current I_B	-	10 amp D. C. maximum

† Indicates Changed Rating.

2.2 Performance Specifications (Single Transistors)

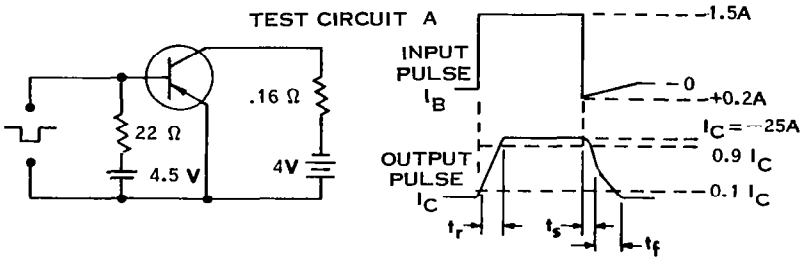
Performance Specifications T_{MB} = 25°C (unless otherwise specified)

Static Characteristics	Conditions	Symbol	Min.	Typ.	Max.	Unit
Current Gain, Common Emitter	I_c=-25A, V_{CE}=-IV*	h_{FE}	30	180	-	-
	I_c=-50A, V_{CE}=-IV*		40	120	-	-
Collector-to-Emitter Saturation Voltage	I_c=-25A, I_B=-1.5A	$V_{CE(sat}$		-0.04	-0.075	V
	I_c=-50A, I_B=-3A			-0.06	-0.1	V
Base-to-Emitter Saturation Voltage	I_c=-25A, I_B=-1.5A*	$V_{BE(sat)}$		-0.45	-0.6	V
	Ic=-50A, I_B=-3A*			-0.50	-0.7	V
† Collector-to-Emitter Current, Reverse Bias	V_{CE}=-15V, V_{BE}=+1.0V T_{MB}=+70°C	I_{CEX}		-1.0	-10.0	Ma
Collector-to-Emitter Voltage	I_c=-1A, IB=0*	V_{CEO}	-5			V
† Collector Junction Leakage Current	V_{CB}=-15V, I_E=0	I_{CBO}		-0.6	5.0	Ma
Emitter Floating Potential	V_{CB}=-15V, R_{EB}=10K	V_{EBF}		-0.12	-0.5	V
Emitter Junction Leakage Current	V_{EB}=-5V, I_c=0	I_{EBO}		-1.0	-5.0	Ma

* To limit collector dissipation use sweep or pulse measurement technique.

Dynamic Characteristics	Conditions	Symbol	Min.	Typ.	Max.	Unit
Pulse Rise Time	I_c=-25A, I_B=-1.5A	t_r		11		μs
Pulse Storage Time	V_{BE}=+4.5V, R_{BE}=22Ω	t_s		30		μs
Pulse Fall Time	Test Circuit A	t_f		17		μs
High Frequency Small Signal Forward Current Transfer Ratio	V_{CE}=-2V, I_c=-5.0A f = 100 kc	h_{fe}	2.0	4.5		
Thermal Characteristics						
Thermal Resistance **		Θ_{J-MB}			0.7	°c/w

** Includes dry interface between transistor and dissipation.



2.3 Performance Specifications (Matched Sets)

Each set of five matched transistors will, in addition to falling within the individual specification outlined in 2.2 above, meet the following requirements.

2.3.1 $\Delta V_{BE(sat)}$: For I_c=-50A, I_B=-3.0A, any unit in a group of five units shall not vary by more than 0.020V from any other unit in this group.

2.3.2 $\Delta V_{CE(sat)}$: For I_c =-50A, I_B=-3.0A, any unit in a group of five units shall not vary by more than 0.030V from any other unit in this group.

2.4 Pre-Shipment Aging

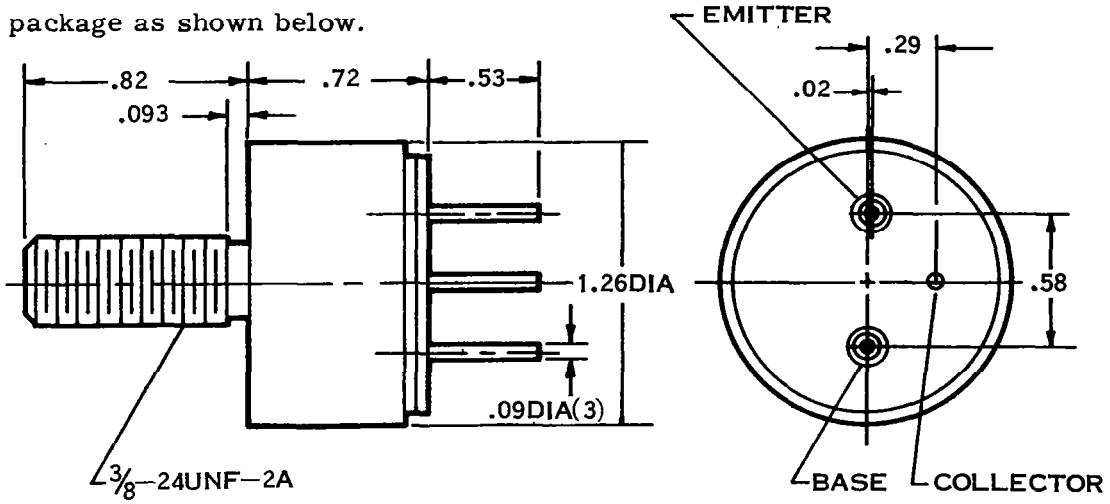
All transistors selected to meet the specifications outlined in this document shall be stored prior to selection for 100 hours at $T_{j\,(max)}$ to eliminate infant mortality failure.

3.0 MECHANICAL SPECIFICATIONS

The transistors comprising a matched set of five will be housed in the same case configurations as presently available for MHT-2205 series. In addition, "stripped down" version consisting of the cold-welded can which is inserted in a heat-sink package may prove desirable. The sets shall be marked in a fashion to allow easy correlation with test data.

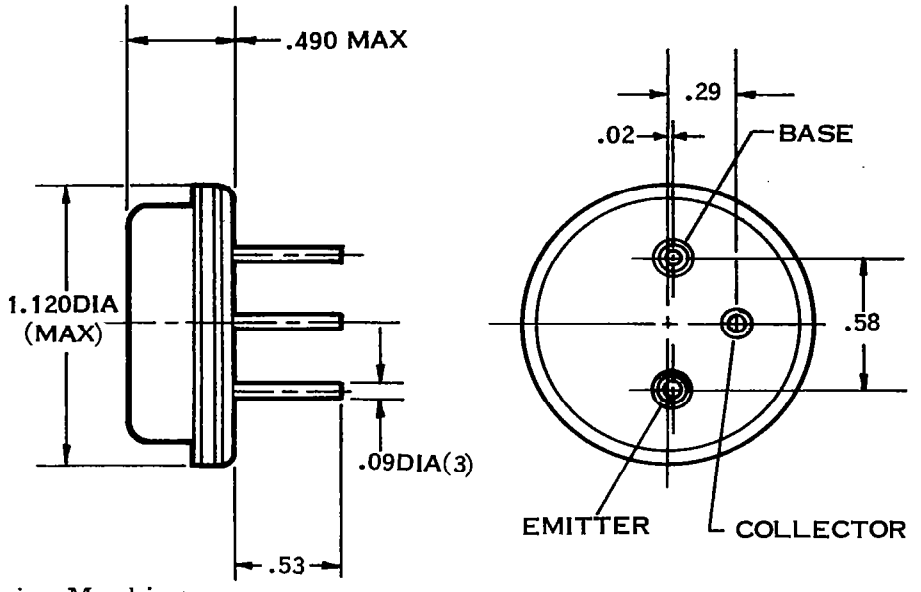
3.1 Configuration I (Double-ended Package)

The above specified transistors shall be housed within the confines of a package as shown below.



3.2 Configuration II (Cold-weld Can Package)

In addition, the above specified transistors shall be made available within the confines of a package as shown below.



3.3 Device Marking

Each transistor delivered will be marked with a unique serial number, which shall be traceable to test data accrued during its manufacture. In addition, each transistor delivered shall be marked in a fashion that will allow ready establishment of the set from which it came.

(Example: Serial No. 5-23 corresponds to Set No. 5, Transistor No. 23)

Marking shall be accomplished with standard imprinting methods employed in the semi-conductor industry.

4.0 QUALITY CONTROL REQUIREMENTS

The vendor shall supply certified acceptance test reports in triplicate which shall list, by transistor serial number, the variable readings obtained for characteristics listed under Section 2.0 of this specification. Also all applicable drawings and Control Specifications shall be furnished by vendor with the initial shipment and incorporation of any revisions.

Receiving Inspection shall check vendor test reports for completeness, compliance to limits of Section 2.0 of this specification, and correlation with serial numbers of items received. A visual inspection shall be performed to assure freedom from handling and shipping damage, legibility and completeness of marking to paragraph 3.3 of this specification, pin integrity and proper packaging per paragraph 3.0 of this specification. Dimensions shall be checked to paragraph 3.1 or 3.2 of this specification as applicable.

Acceptable units shall be marked with a small white dot approximately 1/16" in diameter, shall be re-packaged and forwarded to stores with Receiving Report showing inspection acceptance. No incoming functional test or burn-in is required.

APPENDIX B

6401-6A CONSTANT CURRENT CELL CHARGER SPECIFICATIONS

SPECIFICATIONS:

I. Electrical

Charging Current	- 0 to 6 amperes (adjustable to ± 5ma)
Charging Voltage	- any voltage up to +5.0 volts above the sum of uncharged cell voltages (see Note 1 below)
Set-Point Accuracy	- Linear within ±1% of dial reading
Accuracy	- ± 1% of full load output (±60 ma) over temperature range.
Input Voltage	- 115 VAC ± 10%, 60 cps, 30 ma

II. Temperature

Operating Range	- 0°C. to $+55^{\circ}$C.

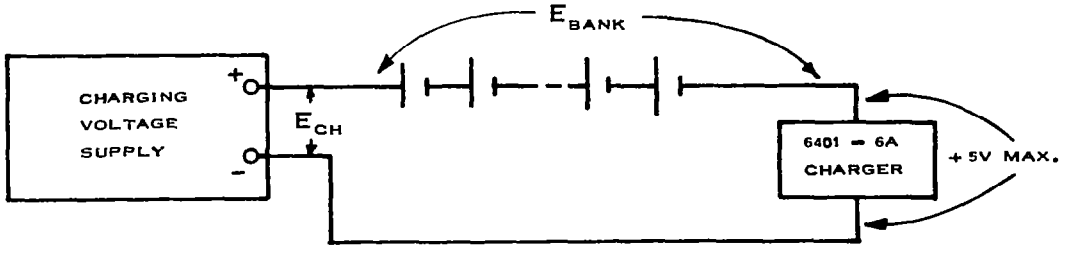
III. Mechanical

Size	- 10" x 6-3/4" x 3" max.
Weight	- approximately 10 lbs.
Mounting	- Flange mount to panel with eight #6 screws (see outline below)
Connectors	-
One	- MS-3102 A-10SL-3P (3 pin) for connection to external charging voltage and cells. (Mating side supplied)
One	- #126-220 (Amphenol) (9 pin) for connection of remote set-point potentiometer. (Mating side supplied)

IV. Price

$873.00 F.O.B., Rockville, Maryland.

Note 1: This unit may be used to charge any number of series cells which are connected to an external charging voltage source provided the difference between the sum of the cell voltages in the discharged state and the charging voltage does not exceed +5.0. (See Figure 1 below).



$E_{CH} \leq E_{BANK} + 5V$

FIGURE 1

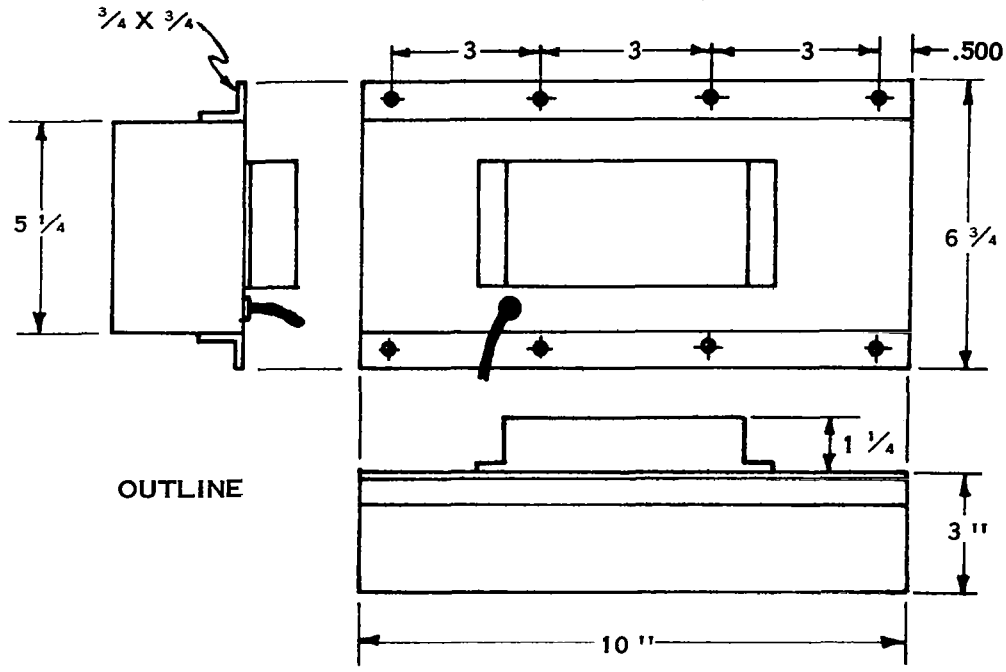


FIGURE 2

V. Description

Model 6401-6A Constant Current Cell Charger is designed to provide very accurate and stable charging current for use in replenishing the charge in high efficiency Nickel-Cadium and Silver-Zinc cells. It features simple adjustment of current level with a direct reading dial, precision 10-turn potentiometer which is provided with six (6) feet of shielded cable for remote control. Once the level of charging current is set and locked, it remains stable within ± 1% over load and temperature variations. The unit has a self-contained precision regulated power supply which provides all control circuitry voltages when connected to ordinary AC line voltage. Provision is made for connection to the load and remote potentiometer by inclusion of two (2) connectors on the rear surface. This surface is hinged for easy maintenance of the circuitry within the unit, upon removal of four (4) screws. Design of the unit was such that it may be mounted onto the back of existing chassis' where rack clearance permits. Operation of this unit is intended for commercial-industrial environments, typically room temperature ambients. Special designs for aerospace use are available by consulting the home plant.

VI. Theory of Operation (Refer to Block Diagram, Figure 3 below)

Charging current through the series pass element (a high power transistor) is controlled by the comparator and control amplifier in such a fashion that the voltage dropped across R sample is equal to E ref. The "Set-Point" control is calibrated to provide a voltage proportional to its rotation which is a direct display of the magnitude of charge current desired. Because the comparator is of the differential type utilizing high loop gains, the accuracy with which the charging current may be controlled depends only on the accuracy of R sample, the stability of the reference, and the equivalent input off-set of the comparator. Similarly, temperature variations are dependent only on the change in resistance of R sample, the temperature coefficient of the reference and the equivalent input drift of the comparator. Appropriate selection of components has been made to minimize these errors. It is of interest to note that variations in gain in the series element either with temperature or age are automatically compensated for in this technique. Also, changes in charging voltage or cell voltage leave no effect on the value of charging current. It is to be noted that this unit does not provide any method of safety preventing overcharging of cells. Additional control circuitry is required for this mode of operation.

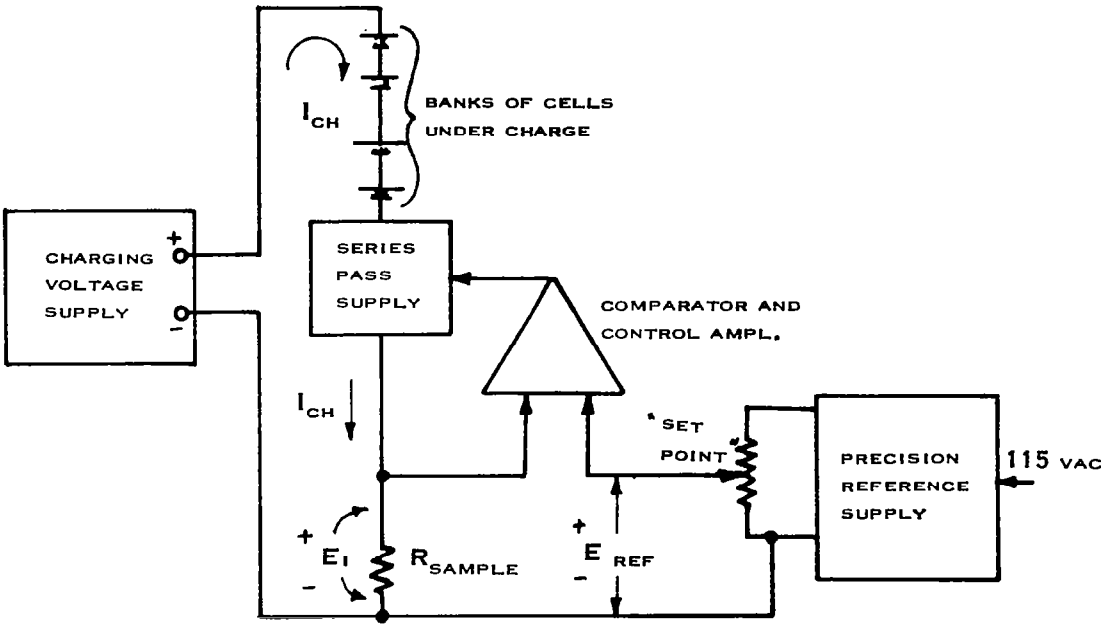


FIGURE 3

VII. Warranty

(a) Fairchild Hiller Corporation warrants that the 6401-6A Constant Current Cell Charger furnished hereunder shall be free from defects in workmanship and material; and shall survive any delivery to or inspection and acceptance or payment by the Purchaser for a period of ninety (90) days from the day of delivery.

(b) If the article specified under (a) above does not meet the warranties as specified above the Purchaser may, at its election (1) require Fairchild Hiller Corporation to correct at no cost the Purchaser, any defect in material or workmanship; or, (2) return such defective article to Fairchild Hiller Corporation and recover from Fairchild Hiller an equitable adjustment in price of the article; however, such price shall not exceed the control price for the Constant Current Cell Charger furnished to the Purchaser under contract.

APPENDIX C

The following pages describe the interconnecting wiring of the Thermionic Diode Controlled Power System. Jacks J1, J2 and J3 are battery bank test points and are described in report FHC/SSD-66-58. Jacks J11 and J14 are the only ones used on the Philbrick analog instrumentation chassis.

Wire size, color, and function are indicated where applicable. Destinations in parentheses indicate continuation of a series connected circuit.

J-4 9-Pin Amphenol on Battery Bank

Pin		Description	Destination
A		N. C.	
B		N. C.	
C		N. C.	
D	#22, Red	CW end Pot R6	J7K
E		N. C.	
F	#22, Black	CCW end Pot R6	J7G
H	#22	Shield	
J		N. C.	
K	#22, Green	Wiper (Shielded Cable)	J7L

J5A (PTO7H-14-19P) Slave Parasitic Load A

Pin		Description	Destination
A	#20, Green	Control Signal	J7C
B		Ground (not used in system)	
C	#22, White	T.P.	T.P. 1
D	#22, White	T.P.	T.P. 2
E	#22, White	System Interlock	J5B-F
F	#22, White	System Interlock	J5C-E
G	#22, Black	Temperature common	T.P. 7
H		N. C.	
J		N. C.	
L		N. C.	
M		N. C.	
N	#22, Yellow	Temperature Mon. 3A	T.P. 6
P	#20, Black	Switched resistive load common	R101-1
R	#20, Red	R10A	S10 Deck 2
S	#20, Red	R11A	S10 Deck 3
T	#22, Yellow	Temperature Mon. 1A	T. P. 4
U	#22, White	T.P.	T. P. 3
V	#22, Yellow	Temperature Mon. 2A	T. P. 5

J5B (PTO7H-14-19P) SLAVE PARASITIC LOAD "B"

Pin		Description	Destination
A	#20, Green	Control Signal	J7D
B		Ground, not used	
C	#22, White	T. P.	T. P. 8
D	#22, White	T. P.	T. P. 9
E	#22, White	System Interlock	S8-N.O.
F	#22, White	System Interlock	J5A-E
G	#22, Black	Temp. Common	T. P. 14
H		N. C.	
J		N. C.	
K		N. C.	
L		N. C.	
M		N. C.	
N	#22, Yellow	Temp. Mon. 3B	T. P. 13
P	#20, Black	Switched Resistive Load Common	R101-1
R	#20, Red	R10B	S10, Deck 2
S	#20, Red	R11B	S10, Deck 4
T	#22, Red	Temp. Mon. 1B	T. P. 11
U	#22, White	T. P.	T. P. 10
V	#22, Yellow	Temp. Mon. 2B	T. P. 12

J5C (PTO7H-14-19P) SLAVE PARASITIC LOAD "C"

Pin		Description	Destination
A	#20 Green	Control Signal	J7-E
B	#20 Black	Ground, not used	
C	#22 White	T.P.	T.P. 50
D	#22 White	T.P.	T.P. 51
E	#22 White	System Interlock	J5A-F
F	#22 White	System Interlock	J5D-E
G	#22 Black	Temp. Common	T.P. 56
H		N. C.	
J		N. C.	
K		N. C.	
L		N. C.	
M		N. C.	
N	#22 Yellow	Temp. Mon. 3C	T.P. 55
P	#20 Black	Switched Resistive Load Common	R101-1
R	#20 Red	R10C	S10, Deck 4
S	#20 Red	R11C	S10, Deck 3
T	#22 Yellow	Temp. Mon. 1C	T.P. 53
U	#22 White	T.P.	T.P. 52
V	#22 Yellow	Temp. Mon 2C	T.P. 54

J5D (PTO7H-14-19P) SLAVE PARASITIC LOAD "D"

Pin		Description	Destination
A	#20, Green	Control Signal	J7F
B	#20, Black	Ground, not used	
C	#22, White	T.P.	T.P. 57
D	#22, White	T.P.	T.P. 58
E	#22, White	System Interlock	J5C-F
F	#22, White	System Interlock	S9-Com.
G	#22, Black	Temp. Common	T.P. 63
H		N.C.	
J		N.C.	
K		N.C.	
L		N.C.	
M		N.C.	
N	#22, Yellow	Temp. Mon.	T.P. 62
P	#20, Black	Switched Resistive Load Common	R101-1
R	#20, Red	R10D	S10, Deck 4
S	#20, Red	R11D	S10, Deck 1
T	#22, Yellow	Temp. Mon. 1D	T.P. 60
U	#22, White	T.P.	T.P. 59
V	#22, Yellow	Temp. Mon. 2D	T.P. 61

J6 (PTO7H-14-5P) SLAVE POWER CONDITIONER

Pin		Description	Destination
A	#18, Black	Charge Regulator Input (battery bank return)	TB1-3
B	#18, Black	+Current return	R101-1
C	#16, Black	60v return	R101-2
D	#14, Black	14A Load	S10-L all decks
E	#18, Red	3A Load	TB1-4

J7 (PTO7H-18-32P) SLAVE POWER CONDITIONER

Pin		Description	Destination
A	#20 Red	+2V reference	M2-1
B	#20 Black	+2V reference return	M2-2
C	#20 Green	Control Signal to S. P. L. A	J5A-A
D	#20 Green	Control Signal to S. P. L. B	J5B-A
E	#20 Green	Control Signal to S. P. L. C	J5D-A
F	#20 Green	Control Signal to S. P. L. D	J5D-A
G	#22 Black	CCW end "Current Adj. Pot"	J4-F
H	#22 White	System Interlock	J8-K
J	#22 White	System Interlock	S8-Common
K	#22 Red	CW end "Current Adj. Pot"	J4-D
L	#22 Green	"Current Adj. Pot" Wiper	J4-K
M		+28 from Aux. heater power supply	used only in cold vacuum chamber
N		+28 return, Aux. heater power supply	used only in cold vacuum chamber
P	#22 White	T. P.	T. P. 30
R	#22 White	T. P.	T. P. 31
S	#22 White	T. P.	T. P. 32
T	#22 White	T. P.	T. P. 34
U	#22 White	T. P.	T. P. 40
V	#22 White	T. P.	T. P. 29 (M8-1)
W	#22 White	T. P.	T. P. 33
X	#22 Yellow	T. P.	T. P. 46
Y	#22 Yellow	Temp. Mon.	T. P. 43
Z	#22 Black	Temp. Common	T. P. 49
a	#22 Yellow	Temp. Mon. 5	T. P. 47
b	#22 White	T. P.	T. P. 35
c	#22 White	T. P.	T. P. 38
d	#22 Yellow	Temp. Mon 2	T. P. 44
e	#22 Yellow	T. P.	T. P. 36
f	#22 Yellow	Temp. Mon. 6	T. P. 48
g	#22 Yellow	Temp. Mon. 3	T. P. 45
h	#22 White	T. P.	T. P. 39
j	#22 Red	T. P.	(T. P. 37) M4-1

J8 (PTO7H-16-26P) MASTER POWER CHAIN

Pin		Description	Destination
A	#20 Red	+2 volt reference	M2-1
B	#20 Black	+2 volt reference return	M2-2
C	#20 Red	+60 VDC	M5-1
D	#20 Red	MOC Return	M5-2
E	#22 Green	Drive from P66A	J14-3
F	#22 Green	Feedback to Analog Amps	J14-4
G	#20 Black	-60V D. C.	M6-2 (J14-7)(T. P. 2)
H		N. C.	
J	#22 White	System Interlock	S5-N. O.
K	#22 White	System Interlock	J7-H
L		N. C.	
M		N. C.	
N		N. C.	
P		N. C.	
R		N. C.	
S	#22 Yellow	Temp. Mon. 1	T. P-24
T	#22 Yellow	Temp. Mon. 2	T. P-25
U	#22 Yellow	Temp. Mon. 3	T. P-26
V	#22 Yellow	Temp. Mon. 4	T. P-27
W	#22 White	T. P.	T. P-17
X	#22 White	T. P.	T. P-18
Y	#22 White	T. P.	T. P-22
Z	#22 White	T. P.	T. P-16
a	#22 White	T. P.	T. P-18
b	#22 White	T. P.	T. P-15
c	#22 Black	Temp. Common	T. P-28

J-11 Amphenol 24 Pin Hermaphroditic - Philbrick Chassis

Pin		Description	Destination
1		N. C.	
2		Jumper (ground sense)	J11-6
3		Jumper (+ sense)	J11-7
4		Jumper (- sense)	J11-8
5		N. C.	
6		Jumper (ground sense)	J11-2
7		Jumper (+ sense)	J11-3
8		Jumper (-sense)	J11-4
9		N. C.	
10		N. C.	
11	#22, Red	+15 output	J14-11
12	#22, Green	-15 output	J14-12
13		N. C.	
14		N. C.	
15		N. C.	
16		N. C.	
17	Green	Chassis Ground	Power Ground (plug mold)
18	#22, Black	Power Ground	J14-18
19	#22, Blue	6.3 v AC	J14-19
20	#22, Blue	6.3 v AC	J14-20
21	Black	110 AC input	Plug Mold
22	White	110 AC input	Plug Mold
23		117 AC } photochopper	J14-23
24		117 AC } photochopper	J14-24

J-14 Amphenol 24 Pin Hermaphroditic - Philbrick Chassis

Pin		Description	Destination
1	#20, Black	Slave Current	M8-2 (M7-1) (R101-3)
2	(not used)	Comp. input	
3	#22, Green	Booster output	J8-E
4	#22, Green	Master Feedback	J8-F
5	#20, Black	Slave Common	M7-2 (R101-4) (T. P. 42)
6	(not used)	Comp. common	
7		Master Common	M6-2 (J8-G) (T. P. 23)
8		N. C.	
9		N. C.	
10		N. C.	
11	#22, Red	+15 output	J11-11
12	#22, Green	-15 output	J11-12
13		N. C.	
14		N. C.	
15		N. C.	
16		N. C.	
17		N. C.	
18		Power Ground	J11-18
19	#22, Blue	6.3 v AC	J11-19
20	#22, Blue	6.3 v AC	J11-20
21		N. C.	
22		N. C.	
23		117 AC } photochopper	J11-23
24		117 AC } photochopper	J11-24