CALIFORNIA INSTITUTE OF TECHNOLOGY
JET PROPULSION LABORATORY
Pasadena, California

HIGH POWER SWITCHING TRANSISTOR

Contract Number 951156
(Subcontract under NASA Contract NA 57-100)

Final Report - Phase I
May 1966

Prepared by
Richard Finch and Jacques Beaudouin

Submitted by
International Telephone and Telegraph Corporation
ITT Semiconductors Product Laboratory
Palo Alto, California

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, pursuant to a subcontract issued under Prime Contract NAS 7-100 between the California Institute of Technology and the United States of America represented by the National Aeronautics and Space Administration.

ABSTRACT

The design theory and fabrication procedure is presented for an npn 100 ampere silicon switching transistor. This transistor has a saturation voltage less than 200 millivolts at 75 amperes. This device has several unique features. The base is produced by a "planarized" epitaxial layer. This makes it possible to have a highly doped collector and therefore a relatively high inverse alpha. The metal contacts incorporate a 10 micron electroplated silver layer which allows long narrow emitter fingers. A system of multiple chips in parallel was found to be satisfactory and was used instead of one large chip. This improved the effective yield of the transistor.

Table of Contents

List of Figures

1. THEORY AND DESIGN

1.1 Intrinsic Saturation Voltage

Consider first an ideal transistor structure free of ohmic resistances. The effect of these resistances will be considered later. Figure 1 shows current and voltage reference polarities appropriate to an npn transistor; by reversing these, the results of course apply to pnp devices.

For the polarities shown in Fig. 1 the emitter and collector currents, for forward bias on both junctions producing currents much larger than reverse saturation currents, can be written in terms of the junction voltage by the well-known equations:*

$$\begin{aligned} I_E &= a_{11} \exp (V_{eb}/V_\theta) - a_{12} \exp (V_{cb}/V_\theta) \\ I_C &= a_{21} \exp (V_{eb}/V_\theta) - a_{22} \exp (V_{cb}/V_\theta) \end{aligned} \tag{1}$$

where V_θ is the thermal voltage $kT/q \simeq 26$ mV. It can be shown under very general conditions, including the structures considered here, that $a_{12} = a_{21}$. The normal and inverse alphas are $\alpha_N = a_{21}/a_{11}$ and $\alpha_I = a_{12}/a_{22}$ respectively.

From Eq. (1) and the preceding relations, the collector-emitter voltage V_{ce} in terms of I_C and $I_B = I_E - I_C$ is found to be:

$$\begin{aligned} V_{ce}/V_\theta &= \ln [1 + (1 - \alpha_I) I_C/I_B] \\ &\quad - \ln [1 - I_C/\beta_N I_B] - \ln \alpha_I \end{aligned} \tag{2}$$

---

* A useful reference for the theory relevant to this proposal is J. J. Ebers and J. L. Moll, "Large-Signal Behavior of Junction Transistors", Proc. IRE 42, 1761 (1954).

where β_N is the normal common-emitter current gain. Since the arguments of the last two terms are less than one ($\alpha_I < 1$ and $I_C/I_B < \beta_N$ in saturation), these terms contribute positive values to V_{ce}.

Consider two cases. In both we shall assume the minimum specified $\beta_N = 20$ and the specified $I_C/I_B = 15$. The first case corresponds to double-diffused high frequency type transistors which have a very low inverse alpha, typically less than 0.1. This is because the collector region is much higher resistivity than the base, leading to poor injection efficiency at the collector base junction. Taking $\alpha_I = 0.05$ gives

$$V_{ce}/V_\theta = 2.72 + 1.39 + 2.99 = 6.36$$

$$V_{ce} = 0.185 \text{ volts.} \tag{3}$$

This is far from the design goal of 0.1 volts, and allows insufficient margin for resistive voltage drops to meet the required minimum of 0.2 volts.

In the second case, we consider a structure with a much higher α_I. This can be achieved by using a highly doped collector which injects efficiently into the base, and maximizing the ratio of emitter area to collector area. A value of $\alpha_I = 0.5$ is readily obtained. In this event

$$V_{ce}/V_\theta = 2.14 + 1.39 + 0.69 = 4.22$$

$$V_{ce} = 0.11 \text{ volts.}$$

This shows the importance of a reverse current gain as close to unity as possible. Figure 2 shows a sketch of V_{ce} vs α_I for the parameters assumed in the paragraph preceding Eq. (3). It can be seen that $\alpha_I > 0.6$ is necessary for $V_{ce} < 0.1$ volts.

1.2. Effect of Bulk Resistances

The saturation voltage of a real transistor includes components produced by bulk resistances in the structure, principally those of the collector region and base layer. Figure 3A shows how these resistances arise in a typical planar structure, and Fig. 3B shows an approximate equivalent circuit. The diode D represents that portion of the collector-base junction immediately under the base contact. It can be shown that the total saturation voltage is the larger of the following two voltages:

$$V_{SAT} = V_{ce} + I_B R_B \frac{1 + I_C/I_B}{1 + \beta_N} \approx V_{ce} + I_B R_B \tag{5}$$

or $$V_{SAT} \simeq V_{ce} + I_C R_C (1 + I_B/I_C) \tag{6}$$

where V_{ce} is the intrinsic saturation voltage of Eq. (2). As discussed in part 2.1.1 above, a very low collector resistivity will be chosen in order to obtain an α_I near unity. Fortunately, this also minimizes the $I_C R_C$ drop, so that the base resistance drop $I_B R_B$ dominates and Eq. (5) applies. At a base current of 5 amperes and allowing $I_B R_B < 0.05$ volts for a total V_{SAT} of the order of 0.15 volts, requires

$$R_B < 0.01 \text{ ohms} \tag{7}$$

With this low a base resistance, the V_{BE} voltage in saturation will be well below the specified maximum of 1.4 volts.

1.3 Emitter, Base and Collector Region Design

Figure 4 summarizes the cross-sectional structure of the proposed device. A heavily doped N^+ substrate doped with antimony to minimize diffusion during subsequent operations forms the collector region. On this

is grown epitaxially a p type base region, produced in two steps. The first portion, about 5 μ thick, has a resistivity of 1 ohm-cm. The collector space-charge layer spreads into this portion, providing a collector-base breakdown of 40 volts which is estimated to be necessary for a collector-emitter breakdown of 20 volts.

If the base layer were 1 ohm-cm throughout, its sheet resistance would be undesirably high. A design value of 20 ohms per square will be chosen, based on current-crowding considerations and on achieving the very low overall base resistance demanded by Eq. (7). A second portion of the base region, heavily doped (0.01 ohm-cm) and about 5 μ thick, provide low sheet resistance. A planar diffused emitter in an interdigitated pattern is produced by standard oxide masking techniques.

1.4 Device Geometry

1.4.1 Proposed Geometry

The size and configuration of the device is determined from considerations of thermal resistance, maximum current density and current crowding. The maximum current density depends upon conductivity modulation effects in the 1 ohm-cm portion of the base, and is estimated to be about 500 amps/cm^2. Thus the emitter area must be $A_e = 75/500 = 0.15$ cm^2. With this current density and a base sheet resistance of 20 ohms per square, calculations and previous experience show that emitter fingers wider than 150 μ (6 mils) will not emit uniformly because of the transverse biasing effect in the base. Thus the total length of emitter fingers has to be $0.15/0.015 = 10$ cm. It is reasonable to allow a spacing of 75 μ (3 mils) between emitter fingers for the base contacts (see Fig. 4). An approximately square array then consists of 25 emitter stripes, each 0.4 cm long (see Fig. 5). This leads to a collector base junction of about 0.4×0.56 cm^2 $\simeq 0.22$ cm^2 $= A_c$.

1.4.2 Final Geometry

For the first evaluation of the structure a mask set with a smaller area device was made. Because of the better yield of the smaller area unit, the device could be more quickly evaluated. When the small units were complete we placed several units in parallel configuration and found that they performed quite well. With these results it was decided to use parallel chips in the final device, rather than one large chip.

Since there can be problems associated with mesa type functions, we evaluated a planarizing technique (see Fig. 6). This method proved to be successful and was used for all samples produced. With planarized base-collector junctions we were not able to have the low resistivity portion of the epitaxial base since this would lower the voltage of the base collector junction. To replace this heavily doped portion of the epitaxial layer a p^+ diffusion will be made under the base contacts. This p^+ region can also be modified to serve as a channel stopper. See Figs. 7 and 8 for the geometry and cross section of the two designs used.

1.5 Thermal Resistance

We now estimate the thermal resistance of a chip of the above size. The specific thermal resistance of silicon is about 1 cm - °C/watt. If the heat is generated over the emitter area of $A_e = 0.15\ cm^2$ and has to penetrate through the equivalent of 500 μ of silicon (this allows for a molybdenum mounting plate), the thermal resistance is:

$$R_T = 1 \times \frac{500 \times 10^{-4}}{0.15} = 0.33\,°C/watt \qquad (8)$$

Since the total can be 0.5°C/watt, this allows for 0.17°C/watt thermal resistance in the copper mounting base itself.

1.6 Contacts

To distribute current uniformly over the proposed relatively large area device, the metal contacts must be thick enough that the maximum voltage drop occurring over the device is less than 26 millivolts. Single sided comb contacts are proposed, as in Fig. 5. Consider a single emitter finger which must carry 3 amperes. The metal is 100 μ wide and 0.4 cm long, so there are 40 squares in series along the finger. The resistance from end to end is thus $40\ R_m$, where R_m is the sheet resistance of the metal. The voltage drop along the finger for uniform current is $80\ R_m < 26$ mV, or

$$R_m < 3 \times 10^{-4} \text{ ohms per square} \qquad (9)$$

This low resistance calls for a contact thickness of about 40 μ (1.5 mils) if silver is used. Similar considerations show that the bonding region connecting the fingers of the comb, if of the same thickness, should be about 800 μ (32 mils) wide. As shown in Fig. 4, this bonding area lies over the collector region on top of a thick oxide layer.

For the small chips used in the final geometry a silver layer only 10 μ thick is needed. This is based on the same voltage drop considerations as mentioned previously. With the thinner silver we are able to place the base contact closer to the emitter. Because of lateral plating if the proposed thickness of 40 μ were used the base contact would have had to be 80 to 90 μ away from the emitter edge. This would have added to the base resistance.

1.7 Switching Times

Consider first the switching times neglecting collector capacitance. These may be estimated by standard formulas given in the reference quoted in subsection 2.1.1 above. For a 10μ base width, the forward cutoff frequency ω_N is $2D/w^2 \simeq 10^8$ rad/sec. Because of the impurity distribution in the base much more carrier storage will occur in the reverse direction so the inverse cutoff frequency ω_I may only be 10^6 rad/sec. Using these quantities, and $\alpha_N \simeq 0.95$, $\alpha_I = 0.5$ results in the following estimates:

$$\begin{aligned} t_{rise} &\sim 0.2\ \mu\text{sec} \\ t_{storage} &\sim 0.3\ \mu\text{sec} \\ t_{fall} &\sim 0.1\ \mu\text{sec} \end{aligned} \tag{10}$$

These estimates assume a collector current of 75 amperes, a turn-on base current of 5 amperes, and a turn-off base current of 5 amperes. Since turn-off is specified from a reverse voltage source, the storage and fall times may be shorter than estimated above.

Consider now the influence of collector capacitance. An estimate of an upper limit on rise time due to capacitance alone is made as follows. The collector capacity C_c is calculated to be 2500 pF. A base current of no more than 3.75 amperes is required to produce 75 amperes in the collector. The remaining current of about 1.3 amperes of the total 5 amperes drive is available to charge the collector capacity. It can thus be charged at a rate of $I/C_c = 520$ volts per microsecond. To change the collector voltage by 20 volts requires $20/520 \simeq 0.04\ \mu$sec. This is only one-fifth of the rise time given in Eq. (10) so it is concluded the capacitance will not significantly affect the total rise time. The times of Eq. (10) are much

less than the specified maximum values (15 μsec total, including delay time; delay time is harder to estimate, but based on typical emitter capacities of 10^5 pF/cm^2 it should be well under 0.1 μsec starting from V_{be} = -1.5 volts).

2. FABRICATION

2.1 Introduction

The switching transistor developed as a result of this contract is an npn structure. The emitter is divided into many narrow fingers in order to give maximum emitter base periphery per unit of silicon area. To have a high inverse alpha a heavily doped (9×10^{18} impurities/cm^3) collector is used and a lowly doped (4×10^{15}) base layer. The specifications which are the goal of this prototype device are shown in Table I.

The base layer is formed by growing a 7.0 - 8.0 μ, 2.5 Ω-cm boron doped epitaxial layer. This layer is grown on an antimony doped substrate 0.008 Ω-cm and 200 μ thick.

For the diffusions two (2) different sets of masks were tried. Both sets produced a device about 3 mm × 3 mm. Mask set 180 has ten (10) emitter fingers 150 μ by 1900 μ (see Fig. 7). Each emitter finger has its own separate base collector junction. This was done so that the yield of usable fingers would be higher. The yield of good fingers for this mask set, 180, varies from 60 to 80%. The other mask set, 194, has 24 emitter fingers 75 μ by 1700 μ (see Fig. 8). These fingers share a common base collector junction. With mask set 194, the yield of good chips varies from 10 to 50%. The 24 finger devices are not able to operate at as high a current density per unit length of emitter base periphery as the 10 finger mask and still meet the saturation voltage specification. The limiting factor may be the spreading

Table I

ENGINEERING NOTE No. 342-51

HIGH POWER, LOW SATURATION VOLTAGE SILICON SWITCHING TRANSISTOR

Absolute Maximum Ratings:

Collector to Emitter Voltage (BV_{CEO})	20 V/min
Emitter to Base Voltage (BV_{EBO})	4 V/min
Collector Current (I_C)	100 A/min
Base Current (I_B)	15 A/min
Collector Dissipation, T_C = 100° C(P_C)	150 W/min
Thermal Resistance, Junction to Case (θ_{JC})	0.5 °C/W
Junction Temperature Range (T_J)	-65 to +175° C

Electrical Characteristics: (100° C Case Temperature)

Characteristics	Test Conditions	Min.	Max	Units
Breakdown Voltage (BV_{CEO})	I_C = *	20		V
Breakdown Voltage (BV_{EBO})	I_{EB} = *	4		V
Collector Cutoff Current (I_{CEX})	V_{CE} = 10V V_{BE} = *		*	mA
Emitter Cutoff Current (I_{EBO})	V_{EB} = 4V		*	mA
DC Current Gain (h_{FE})	I_C = 75A V_{CE} = 1V	20		
Saturation Voltage ($V_{CE(sat)}$)	I_C = 75A I_B = 5A		0.2 (see Note 1)	V
Saturation Voltage ($V_{BE(sat)}$)	I_C = 75A I_B = 5A		1.4	V
Total Switching Time ($t_d + t_r + t_s + f_f$)	I_C = 75A I_B = 5A V_{BE} = 1.5V on turn off		15	μsec

* Manufacturer's standard specifying procedure acceptable.

Notes: 1. A saturation voltage of 0.1 V under the above conditions shall be a design goal.

2. Device is to be used in DC to DC converter of parallel configuration. Duty cycle is 50% and operating frequency may be up to approximately 5 KC. Operating conditions are either fully saturated or cutoff.

resistance in the collector which limits the current density of the chip.

The base collector junction is planarized and reduced to the active device size by an n type diffusion made with the device area covered with silicon dioxide. The emitters are made by standard diffusion techniques.

Due to the long narrow emitter fingers a contact was needed with a very low voltage drop along the length of the emitter finger. To achieve this a completely new contacting method was developed. This method gives metal contacts 10 μ thick as compared to about 1 μ for the standard aluminum techniques and also has the low ohmic contact to the silicon of the aluminum method. The important aspects of this procedure are listed below (see Fig. 9).

1. Evaporation and alloy of aluminum onto only the contact areas, base and emitter.
2. Evaporation of chromium and silver layers over the entire surface of the slice.
3. Plating of silver in selected areas for the thick contacts over the base and emitter fingers and the bonding pads. KTFR is used to restrict the plating to the desired area.
4. Removal of the photo resist, thin chromium and thin silver layers between the thick plated contacts.

This contact has proved to be satisfactory and has been repeated many times. It does not lift or peel and thermo-compression gold bonds can easily be made to it. Also the chromium-silver-silicon dioxide-silicon system appears to be thermally and chemically stable.

We have shown experimentally that a system of chips mounted in parallel will satisfactorily meet the device specifications. We selected this method rather than one large chip because of yield considerations.

Because of the complexity of the device it took some time to obtain the yield of diffused devices quoted previously. However, once this yield was achieved, it was found to be reproducible (see Section 3).

The package requirements for this device are unique and no standard type package has been designed that we could use. We need a package with a very low voltage drop in the emitter lead and a large area for mounting the chips. As far as possible we have tried to use techniques in the mounting with which we have some experience. To facilitate the handling and mounting of the parallel chips, a subassembly was designed. Using this subassembly the chips could be mounted, bonded and tested in a convenient manner. When a subassembly is completed it is soldered to a 1-1/4 inch stud type header.

A detailed description of this process and entire procedure is given in the next section.

2.2 Specifications for Substrate and Epitaxial Base Layer

2,2,1 Substrate

Antimony doped .005 to .008 Ω-cm.
1-2° off, 111 orientation, 7 mil and 1/2 mil thick.
1-1/4 inch diameter.
Mechanically polished surface.
Back surface either lapped or sawed finish.

2.2.2 Epitaxial Base Layer

- 2 - 4 μ of silicon are etched from the surface in the reactor with HCl.

- Silicon is grown at the rate of about 1 μ/min to a thickness of 7.2 - 7.8 μ and a resistivity of 2.0 to 3.0 Ω- cm.

2.3 Diffusion Procedure

The basic processing steps for producing the transistor die are presented in this section. The outline of the schedule is not meant to be so complete as to allow someone without any semiconductor processing to perform the operations; but is written so that someone familiar with the techniques will know what is done.

(1) To clean slice, boil in $H_2SO_4 : HNO_3$ (8 : 1) and water; blow dry with nitrogen.

(2) First oxidation:

As soon as slice is cleaned, place in oxidation furnace at 1200° C for 1-1/2 hours. Ambient, oxygen 300 cc/min bubbled through 95° C water.

(3) Isolation mask:

- Common base design, 194:
  Apiezon wax W is sprayed through a metal mask to the pattern of the base area. Wax is annealed at 166° C.
- Separate base for each emitter finger design, 184.
  Kodak photo resist is applied, exposed and developed so that the hardened photo resist film is left over the areas which will be the bases for each emitter.

(The processing of each design is the same from this point on.)

(4) Oxide etch: oxide is removed from the unprotected areas with dilute solution of hydroflouric acid.

(5) Removal of resist material:

- Apiezon wax W is removed with trichloroethylene.
- Photo resist is removed with a hot solution of $H_2SO_4 : HNO_3$ (8 : 1).

(6) Isolation predeposit: phosphorus source material deposited at 950° C for 1 hour. (P_3N_5 and $POCl_3$ have both been used.)

(7) Post-predeposit etch: the phosphorus glass is removed from the top of the masking oxide by a 4 minute etch in the dilute hydrofluoric acid solution.

(8) Isolation diffusion: furnace temperature 1200°C for 1-1/2 hour. Oxygen 300 cc/min bubbled through 95°C water.

(9) Photo resist for p^+ regions: Kodak photo resist is applied, exposed and developed so that the area under the base contact and a line completely surrounding each emitter can be etched free of oxide.

(10) A boron predeposit is made in these areas. The purpose of this predeposit is to lower the contact resistance under the base contact and to help stop channels formed on the surface of the p base region. B_2H_6 at 1050°C for 15 minutes.

(11) Diffusion of p^+ layer and oxidation of surface: 1200°C for 30 minutes; 300 cc/min of oxygen bubbled through 95°C water.

(12) Emitter photo resist.

(13) Emitter predeposit. The depth of the emitter is varied to allow for variation in epitaxial layer thickness. Normally the emitter predeposit is varied from 20 to 60 minutes at 1050°C using $POCl_3$ as a source.

(14) Post emitter oxidation: 1000°C for 15 minutes; steam ambient.

(15) Kodak photo resist is used to remove the oxide from the base and emitter contact areas.

(16) Probe test of units to determine yield. DC measurements of junction quality are made.

2.4 Metal Contacting Procedure

The contacts for this device needed to be different from those normally used for transistors. The contact needed to have a low ohmic contact resistance to the silicon and a low sheet resistance so that long narrow

emitter fingers could be used. The contacts were so designed that there is only 30 mV drop or less down the length of the emitter finger at the operating current. This is achieved by making an electroplated silver contact 10 μ thick. The following schedule gives the detailed steps for making this contact. (See Fig. 9).

(1) Start with slice directly after base and emitter contacts have been opened.

(2) Clean in solvents and dry.

(3) Dip slice in dilute HF for 10 seconds and quench in DI water.

(4) Rinse in running DI water for 10 minutes.

(5) Blow dry with nitrogen.

(6) Evaporate 1000 Å of Al.

(7) Immediately apply KPR.

(8) Air dry 15 minutes.

(9) Dry 3 minutes on 94° C hot plate.

(10) Register, expose and develop photo resist so that it is polymerized on areas above contact areas.

(11) Etch off excess aluminum in phosphoric acid etching solution (100 ml acetic acid, 100 ml nitric acid, 200 ml water, 1600 ml H_3PO_4). Etch 30 seconds after aluminum has disappeared from unwanted areas.

(12) Rinse in DI water.

(13) Rinse in methanol.

(14) Store in TCE until ready for alloy.

(15) Alloy, heat to 600° C in vacuum and hold for 2 minutes.

(16) Let cool to 100° C or less and remove from vacuum.

(17) Slice may be stored at this point while waiting further processing.

(18) Etch in hot chromic acid until excess Al is removed.

(19) Pour off chromic acid.

(20) Rinse in DI water.

(21) Blow dry with nitrogen.

(22) Dip in dilute HF for 10 seconds.

(23) Quench in DI water.

(24) Rinse in DI water for 10 minutes.

(25) Place in evaporator on special evaporation jig (one slice at a time).

(26) Evacuate.

(27) Melt Ag.

(28) Evaporate 1000 to 2000 Å of chromium.

(29) Start Ag evaporation before Cr is turned off.

(30) When Ag has started to evaporate turn off Cr.

(31) Evaporate all Ag.

(32) Let cool to 100°C or less and remove.

(33) Immediately apply KTFR, dry, expose, develop and bake so that the KTFR is removed from those areas where the thick contacts are wanted.

(34) Apply liquid black wax to back side.

(35) Let dry.

(36) Clip on cathode connection.

(37) Dip in plating solution.

(38) Adjust voltage to 0.2 V, current will be about 30 mA depending on slice size.

(39) Plate for 20-25 minutes; silver will be 8-10 μ thick.

(40) Turn off, remove from bath.

(41) Rinse in DI water.

(42) Rinse in methanol.

(43) Remove black wax with trichloroethylene.

(44) Remove KTFR in hot J100 10 minutes.

(45) Pour off J100 and rinse in MeOH.

(46) Rinse in DI water.

(47) Make slice anode and etch in 1N KCN solution.

(48) Adjust voltage to 1.2 - 1.4 volts.

(49) As silver is removed, the area between fingers gets darker. Continue for 1 minute after all in-between areas are dark. This means that all evaporated silver is removed and chromium is left.

(50) Remove from bath.

(51) Rinse in DI water. Do not expose to air.

(52) Dip in concentrated HCl at room temperature, leave until no more bubbles.

(53) Rinse well.

(54) Invert slice and dip in HCl again.

(55) Rinse well in DI water.

(56) Dip briefly in dilute HNO_3 1 : 1.

(57) Rinse in DI water.

(58) Slice is now finished and ready for testing.

(59) Store in nitrogen box to avoid tarnish.

2.5 Mounting and Packaging

2.5.1 Testing of Unmounted Devices

It is preferable to test all the devices on a slice and mark them so as to recognize the desirable chips. Any convenient probe set up with probes for the base and emitter contacts is satisfactory.

At this time only the DC electrical parameters of the junctions are recorded. A conventional 60 cycles curve tracer (see schematic in Fig. 10) in conjunction with an x-y oscilloscope (HP Model 130 A or B, Tektronix 503 or equivalent) are used.

2.5.2 Scribing

A silicon dice scriber is used. The slice is carefully placed and secured on the vacuum chuck of the scriber. It is then scribed between rows of devices in the x and y directions. The vacuum is released and the slice is mounted upside down with black wax on a quartz slide.

2.5.3 Etching

The back side, or substrate side of the slice is etched in order to reduce the saturation voltage by reducing the thickness of the collector region and prepare the surface for a good alloy contact. The minimum slice thickness should be 125 μ.

The etching solution used is referred to as I_2 etch. This etch is made in the following proportions: acetic acid, 125 ml; nitric acid, 100 ml; and hydrofluoric acid, 25 ml. Before the acids are mixed the acetic acid is saturated with resublimed iodine crystals. It was found that the type of etch used could affect the saturation voltage. This etch gave the best results of those tried. Water is used to quench the solution and prevent oxidation of the freshly etched surface and the slice is then thoroughly rinse with DI water and then methanol.

The quartz slide is then placed in a small beaker of trichloroethylene (TCE), standing up, until the slice is freed. The slice is rinsed with TCE until clear and then three more times followed by a methanol rinse. The slice is sandwiched between two pieces of filter paper which have been dipped in methanol and by just running the filter papers over a sharp edge (the edge of a stainless steel block is satisfactory for this purpose) in both directions the slice will break along the scribed lines.

The individual transistors are rinsed again with methanol, dried over a hot plate or in an oven at 100 to 150°C maximum and stored in a nitrogen dry box.

2.5.4 Alloying of the Device to Molybdenum Substrate

The molybdenum pieces used are the same shape and size as the silicon chips. They are gold clad on both top and bottom. The gold thickness is 50 μ; the molybdenum itself is 500 μ thick. A gold solder preform is used with 0.5% antimony.

The alloying of the device is done as follows:

(1) The molybdenum rectangles are degreased by boiling in TCE for 5 minutes followed by successive rinses in methanol and acetone.
(2) The KS 601 waferbonder is set at 520°C and flushed with forming gas at a rate of 300 liters per hour.
(3) The molybdenum piece with a gold antimony solder preform is set on the heat column. A transistor dice is set on top of the molybdenum with the pick up tool vibrated for about 10 seconds with the sonic vibrator built in the machine.

Each mounted unit is then stored in a nitrogen flushed dry box.

2.5.5 Saturation Voltage Test

Each alloyed unit is tested at this time. The marked fingers of each unit are checked once more and the saturation voltage of each good finger of every device is measured. Probe contacts to the base and emitter are used.

The V_{sat} target specification is 200 mV or less. The circuit used is illustrated in Fig. 11. Units which show a saturation voltage above the average for the run can be re-alloyed. Re-alloying has shown to decrease the saturation voltage of previously high units to a minimum value which is representative of that particular run.

2.5.6 Constructing the Subassembly

The subassembly is constructed as follows: Copper parts A and B are made following the drawings on Figs. 12 and 13. It is essential to assure that all burrs have been removed from the machined copper parts. They are then thoroughly cleaned. Ceramic spacers metallized on both sides and gold plated are also cleaned.

Cusil solder preforms (1.5 mm x 1.5 mm x 100 μ) are cleaned in the same manner and stored in a nitrogen flushed dry box until used. Part "B" is placed on top of the carbon centering jig (see Fig. 14). The Cusil solder preforms are carefully placed on both grooves of part "B" with the spacers immediately on top and another solder preform on top of each ceramic spacer. As illustrated in Fig. 14, part "A" of the subassembly is set on top of part "B". The two locating pins of the centering jig assure the correct positioning of the two parts. There should not be any ceramic spacers directly under the section of part "A" which is to be cut away later (see Fig. 12). A stainless steel weight, about 50 to 60 grams is set op top of the whole assembly and put through a belt type furnace at 830° C. The hot zone is about 25 cm and the speed of the belt is approximately 3 cm/minute.

2.5.7 Plating of the Subassembly

Immediately after brazing, the subassembly is stored in MeOH. An electroless plating solution is prepared as follows:

30 g $NiCl_2 \cdot 6H_2O$ (Nickel Chloride)
65 g Ammonium nitrate
50 g NH_4Cl Ammonium Chloride
Add water to make 1 liter of solution.

One gram of sodium hypophosphite per 100 ml of solution is added to the solution before use and NH_4OH (Ammonium Hydroxide) is added to adjust the pH to about 9 or 10. The subassembly is submerged in the boiling solution for 30 to 45 seconds, then rinsed in water several times and kept in a beaker of water.

The subassembly is next gold plated with a commercial electroless solution, Atomex. The solution is mixed as directed. The assembly is submerged after the solution comes to a boil. After 6 minutes it is taken out and rinsed thoroughly with DI water and kept in water until the next step. The subassembly is next electrolytically gold plated for 60 minutes at 2 V and 20 mA. Gold plating solution used is as follows:

Potassium gold cyanide (67.5%)	2.75 g/liter
Potassium cyanide	15.0 g/liter
Anode	Stainless steel
Current density	27 mA/cm^2
Agitation	Magnetic stirring

The subassembly is removed from the solution, rinsed and dried.

At this time the subassembly should be tested for possible electrical short circuits between the three isolated parts (collector, base, and emitter.

2.5.8 Gold Bonding

Each good emitter pad is thermo compression gold bonded using four mil gold wire. The base pad is also bonded. The gold wires are automatically cut off and left standing. K &S model 402 nail head bonder is used.

2.5.9 Protective Coating Application

A silicon rubber compound, Bayer SV-1, diluted with cyclohexane is used to cover the bonded chips. It protects them from splashing solder and other unwanted foreign matter which may cause shorting during the soldering operation described in the following paragraph.

2.5.10 Soldering the Alloyed Chip on the Subassembly

To facilitate soldering, the selected alloyed chips are pre-coated with gold germanium solder on the bottom side of the molybdenum piece. Soldering is done in a tabletop furnace at 470° C (see Fig. 15).

A TO-3 transistor base is inserted into the hot zone and coated with gold germanium. The molybdenum substrate of the alloyed chips are coated with solder by rubbing it on the solder coated TO-3 base. After seven selected alloyed chips are presoldered the TO-3 base is removed from the furnace and a special TO-3 base described below is inserted into the hot zone of the furnace.

The special TO-3 base has a hole drilled in the center. A pin fits into that hole centering the subassembly and permitting it to rotate. A thin disc of carbon is placed between the subassembly and the TO-3 carrier to prevent solder from flowing onto the TO-3 base. The subassembly is inserted into the furnace on top of the carbon disc and TO-3 carrying jig.

Using a gold germanium solder stick, the exposed surface of part "B" is wetted. The seven presoldered alloyed chips are then set down and arranged as shown in Fig. 16 with the emitter pads towards the center. The subassembly is pushed into the cold zone of the furnace and allowed to cool and then taken out.

2.5.11 Gold Leads Attached to Subassembly

Using the K & S gold bonder, the 4mil gold leads are thermocompression bonded to the subassembly. The emitter leads to the center circle, and the base lead to the outer ring.

2.5.12 Soldering Subassembly on Stud Header

Soldering is done in an atmosphere of forming gas, 95% N_2 and 5% H_2. The large stud package has been gold plated. A small flat copper plate, approximately 4 cm x 4 cm is set on top of the heat block (see Fig. 17) and wetted with solder. The subassembly is rubbed carefully on top of the plate in order to presolder the bottom surface of part "B" and facilitate soldering on the large package. The stud is inserted in the fixture (Fig. 17); the top surface of the package is tinned with solder and the subassembly is set down on top of the package flush against its surface. The pins are also soldered to the subassembly.

The package is finally removed and allowed to cool. All of the electrical parameters of the device described in the next section can now be tested. If a device fails at this point the subassembly can be removed and the stud reused.

2.5.13 Final Seal

The tested device is capped and sealed in a controlled atmosphere of forming gas using the same heating clock as described in Fig. 17. The

device is set once again into the hole of the heating block and the cap is set on top of it. When both parts are at temperature, a commercial non-corrosive flux solder is used to solder the cap to the large study simply by running the solder stick along the point of contact of the cap and stud.

The base and emitter pins are allowed to protrude through the cap by an insulated tube. The base and emitter pins are soldered to these tubes to complete the seal. The transistor is removed from the heating block and allowed to cool.

3. YIELDS

Due to the large area of the base collector junction, over 6 mm^2, it has been difficult to obtain a sufficiently high yield of devices. After refining and developing our processing procedures, we were able to achieve a satisfactory yield. For the last 34 slices processed, we obtained an average yield of devices with good junctions of 30%. This was as measured after diffusion. Some devices were lost during the metallizing process. This loss was usually due to faulty metallizing such as a metal "bridge" between the base and emitter contact, and not a failure of the junctions. At least 75% of all good devices should survive the metallizing giving an average yield after contact of about 21%.

There has been another yield problem which has resulted in a significant loss of devices during the mounting process. Since the base layer is a high resistivity p type layer, it is susceptible to inversion layers. Inversion layers on the p base layer of an npn transistor are very serious. Because of this we added a p^+ diffused region in the base area surface separating the emitter and the collector. However, for base layer resistivities of above 2.5 Ω-cm, inversion layers were introduced between the base and the collector. This caused very high leakage currents and the devices were discarded. However, they still

operated as a transistor and the saturation voltage seemed unchanged. Because of this upper restriction on resistivity the $V_{EOC(sus)}$ is limited to a maximum of about 18 volts. The yield of devices through mounting has been at least 75% when the p^- resistivity is kept to reasonable limits. We should be able to get an average yield of mounted chips of 16%. It should be pointed out these are only average values and semiconductor yields usually run in streaks. Many times results can be very bad for a long period until the trouble is found.

It is estimated that the yield of good epitaxial substrates from started runs will be in the neighborhood of 70%.

4. ELECTRICAL RESULTS

The most important parameter of the device is the saturation voltage. A typical curve of V_{CE} vs I_C is shown in Fig. 18a. It can be seen that at 75 amps collector current and 5 amps base current the saturation voltage is about 130 mV. These measurements were taken with the circuit shown in Fig. 19. Switching time measurements indicated that total switching time is about 8 μ sec; t_{on} = 0.2 μsec; $t_{storage}$ = 5 μ; t_{off} = 2.5 μsec. These measurements were made with V_{BE} = 0. If V_{BE} were -1.5 V as the conditions allow the total switching time would be lower. Measurements of the saturation voltage in a 75° C oven showed an increase of about 9%. Table II gives the characteristics at room temperature of the devices delivered for Phase I of this contract.

5. COMMENTS FOR PHASE II

Phase II of this contract involves producing 100 transistors of the type developed. The following suggestions are given in order to facilitate this part of the project.

Table II

Results of Prototype Devices

Device No.	BV_{EOC}	BV_{EBO}	$V_{CE(sat)}$ I_c = 75 amp I_B = 5 amp	h_{FE} I_c = 75 amp
II	22V	7V	185 mV	110
III	24V	7V	150 mV	80
V	16V	5.5V	120 mV	100
VIII	19V	4V	120 mV	75
IX	15V	6.5V	150 mV	150

Improvements can be made in the existing device in three major areas: (1) package design; (2) optimize (lower) $V_{CE(sat)}$; (3) raise BV_{CEO} by controlling inversion problems. Of these the last is the most important for the second phase. It is felt that the inversion layer leakage currents can be controlled by a redesign of p^+ channel stopper diffusion. Specifically it will be made wider than the base metal contact.

If the above modification does not completely remove the instability problem a more extensive mask redesign is proposed. It is suggested that the mask be redesigned so that the base metal contact be extended so that it covers the entire base-collector junction. Since the base has a negative charge in relation to the collector it would serve to counteract an inversion layer caused by positive charge on the oxide. Also this layer will prevent ion migration on the surface of the oxide. This suggested redesign could be accomplished without any change in the process. A new set of masks is all that is needed.

Another point of difficulty for Phase II will be the initial delivery of materials, particularly silicon substrate slices and the 1-1/4 inch stud packages. Also some time will be needed to have the newly designed masks completed.

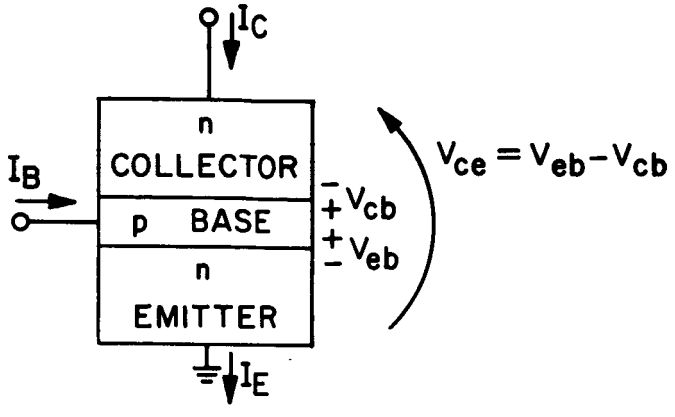


Fig. 1. Reference polarities

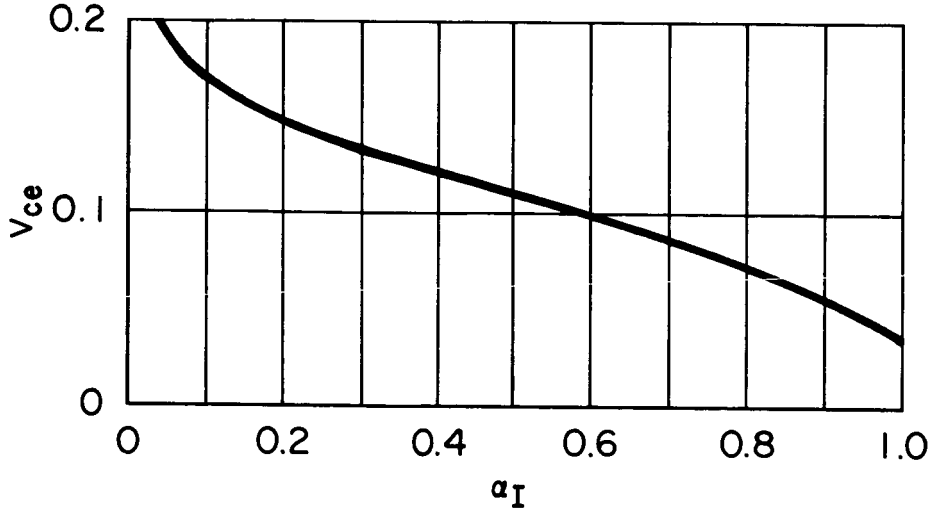


Fig. 2. V_{ce} vs α_I for $\beta_N = 2$
$I_C/I_B = 15$
$kT/q = 26$ mV

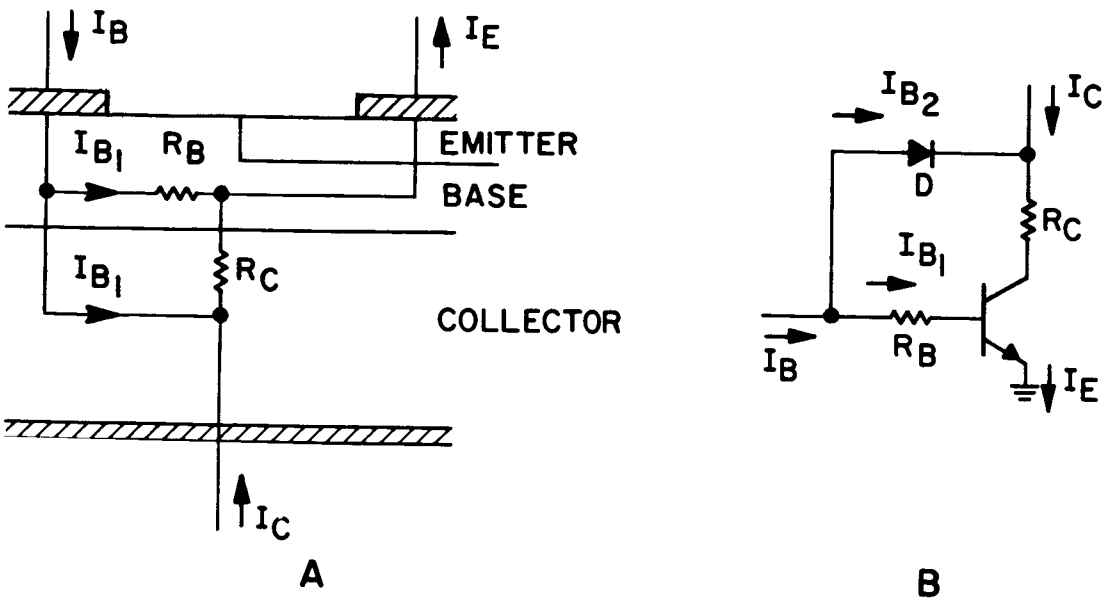


Fig. 3. Internal resistances

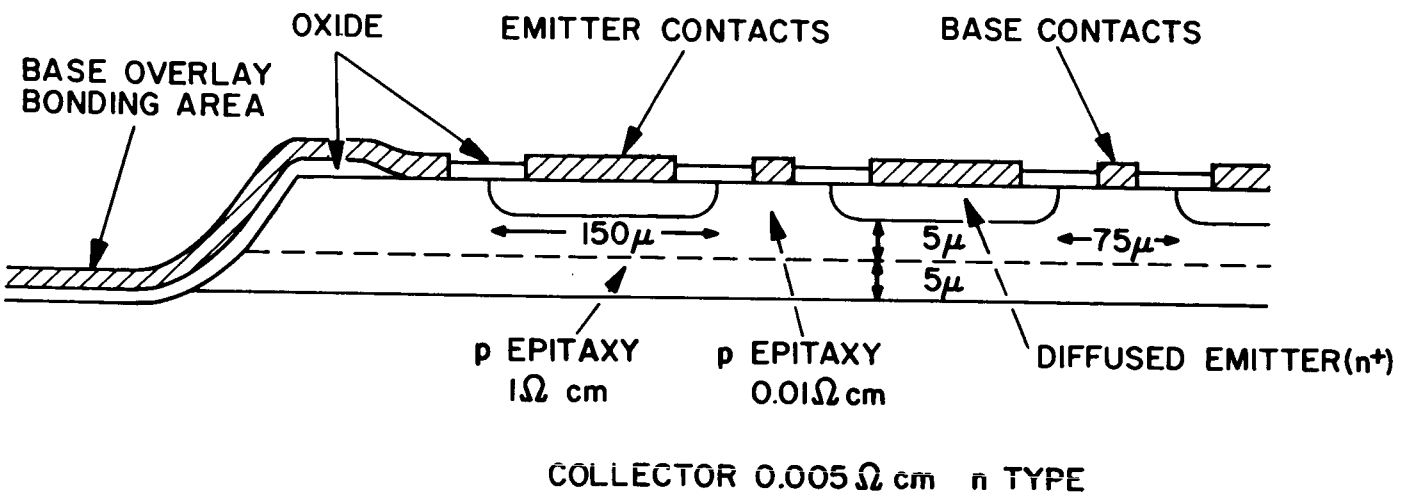


Fig. 4. Cross section perpendicular to emitter fingers (vertical scale exaggerated)

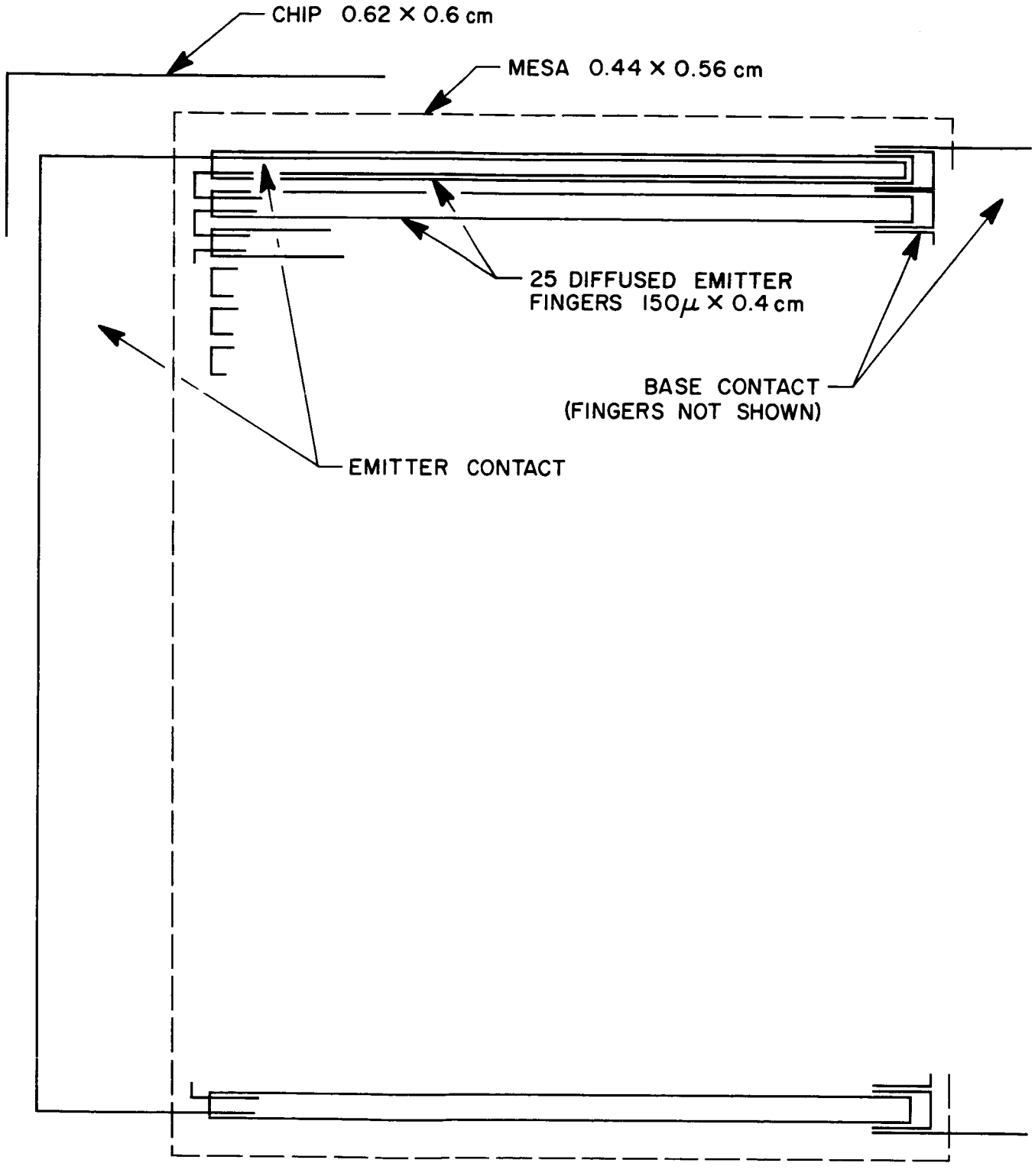
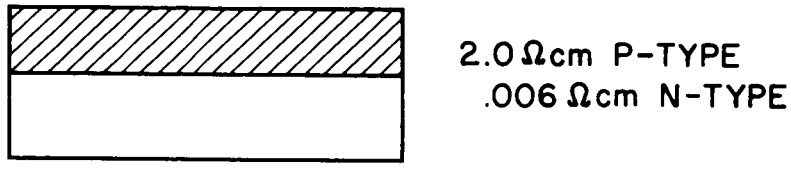
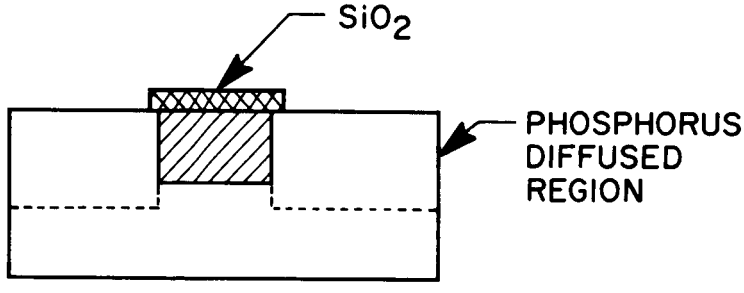


Fig. 5. Geometry of proposed transistor (single-chip design)

7-26-66
51568



EPITAXIAL LAYER WITH EXPOSED JUNCTION



EPITAXIAL JUNCTION "PLANARIZED"
BY A PHOSPHOROUS DIFFUSION

Fig. 6. "Planarizing" epitaxial base layer

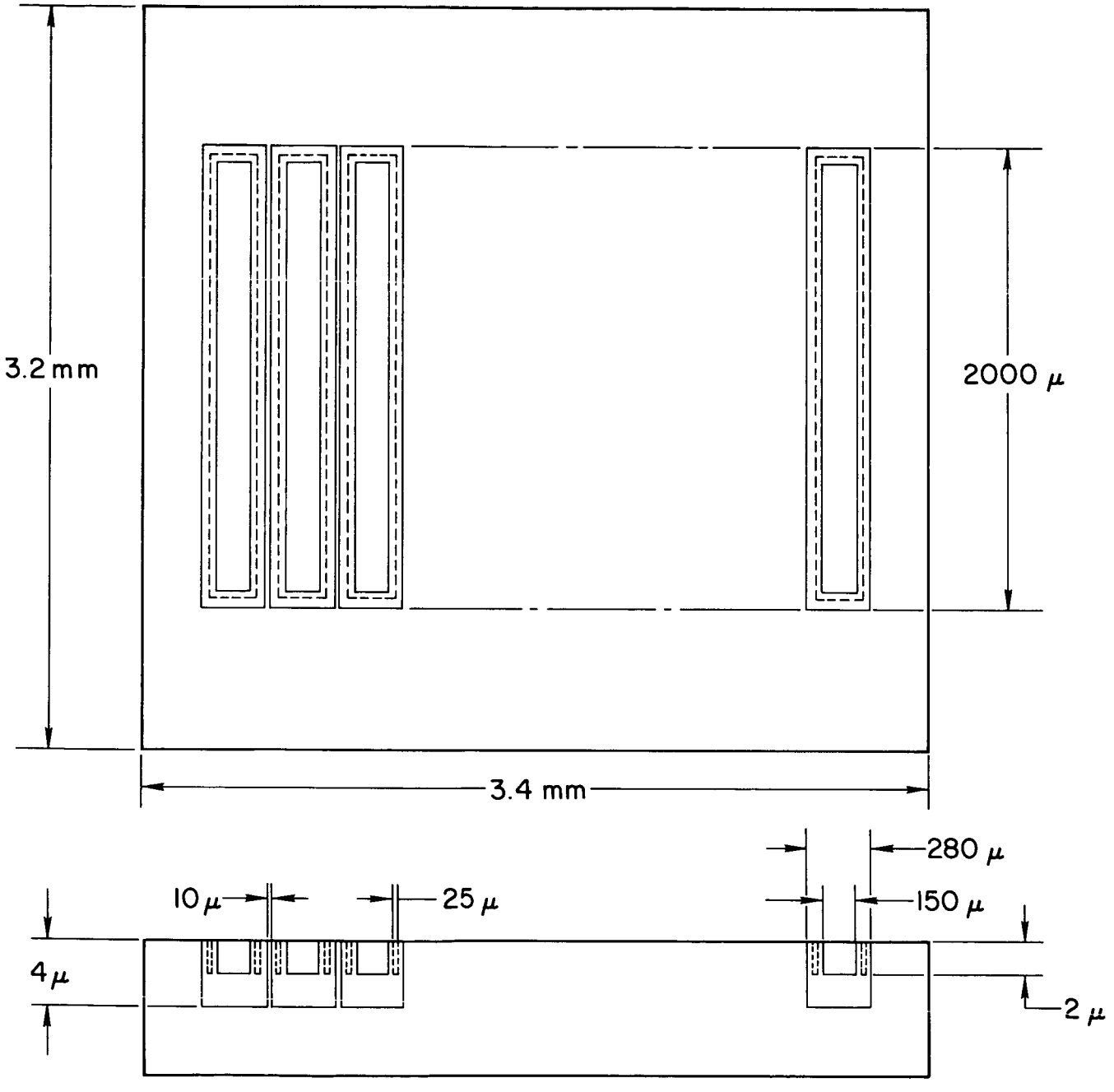


Fig. 7. Geometry and cross section of 10 isolated finger device.

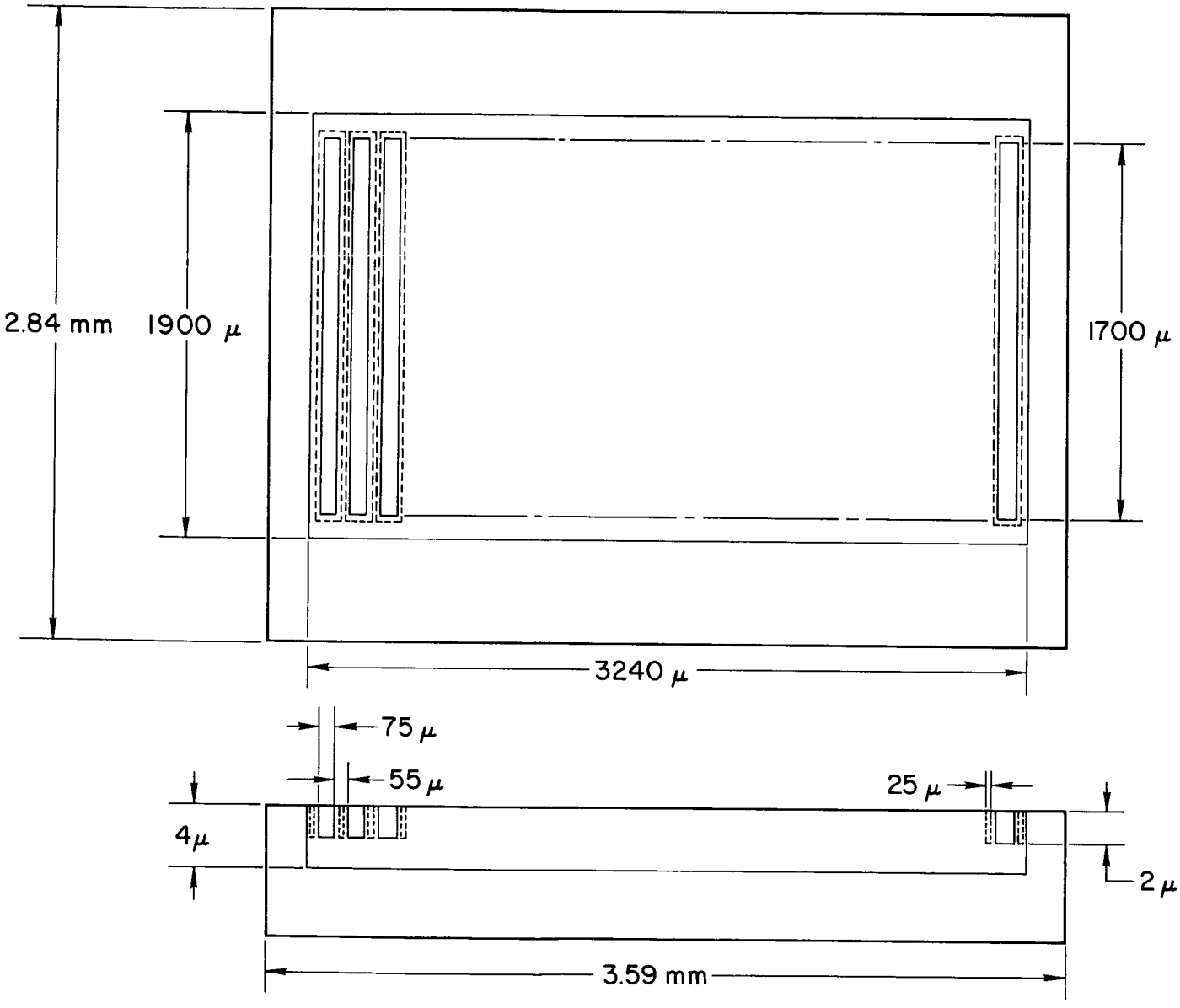


Fig. 8. Geometry and cross section of 24-finger device.

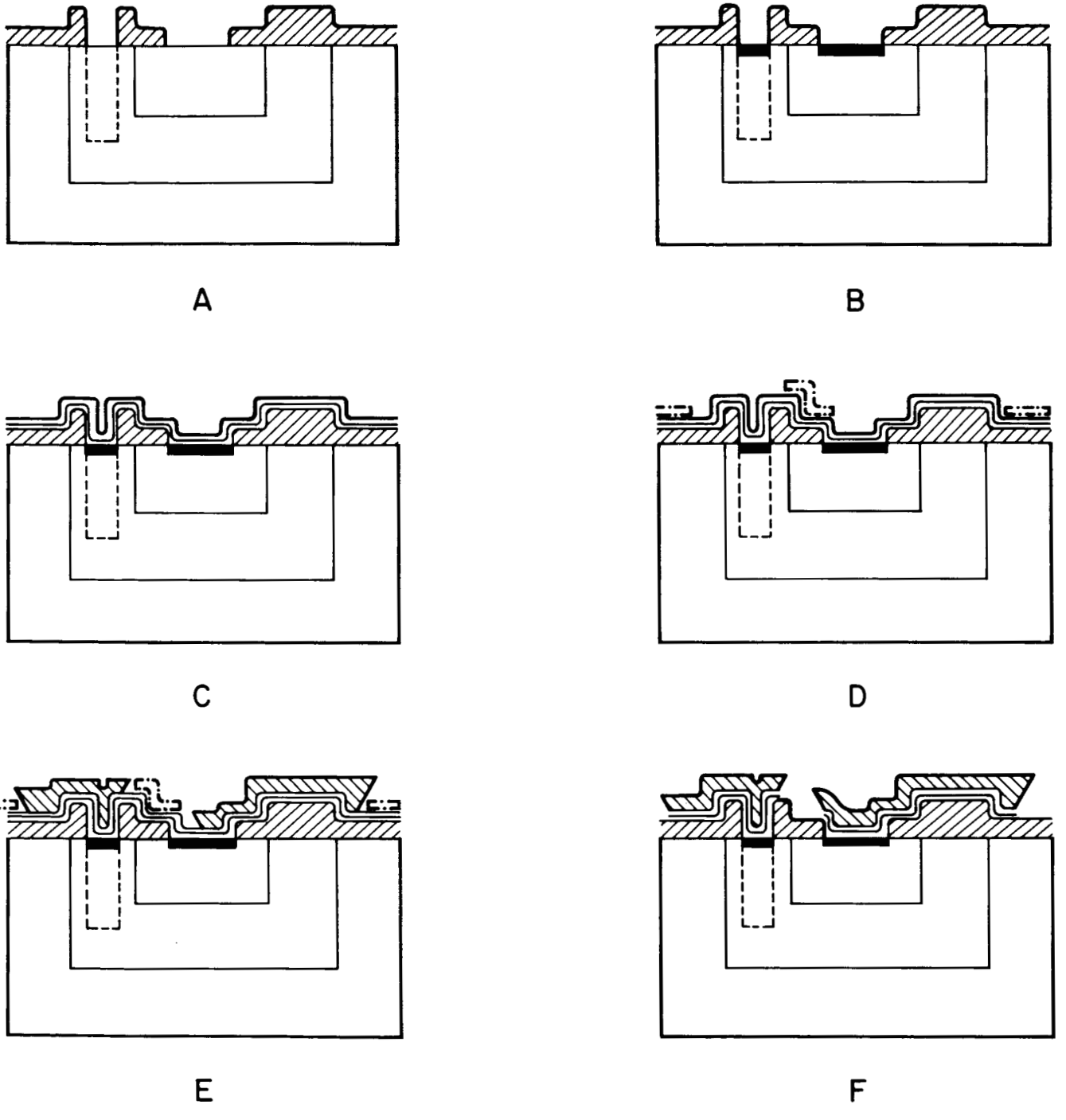


Fig. 9. Schematic representation of contacting procedure.

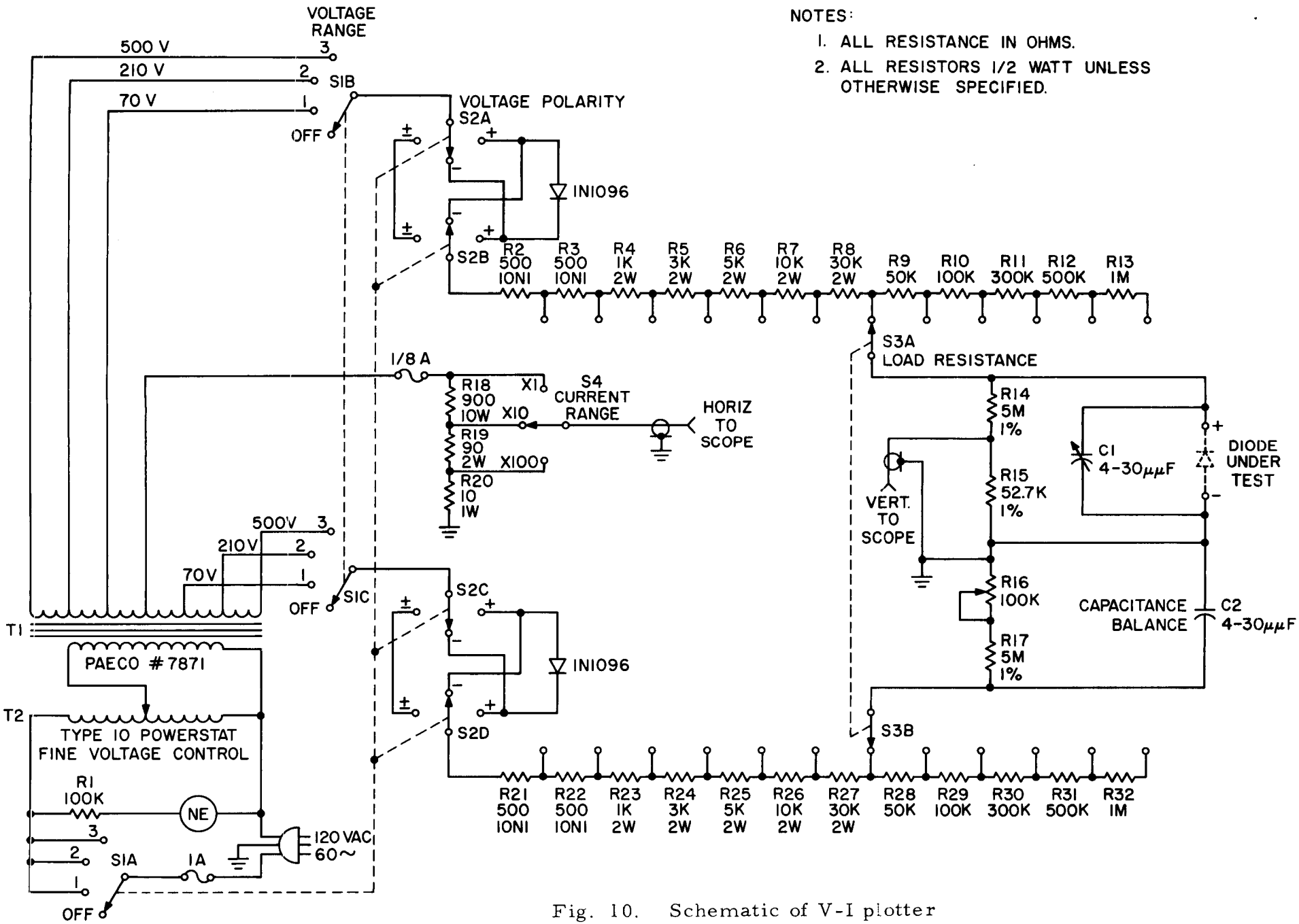


Fig. 10. Schematic of V-I plotter

50296 7-25-62

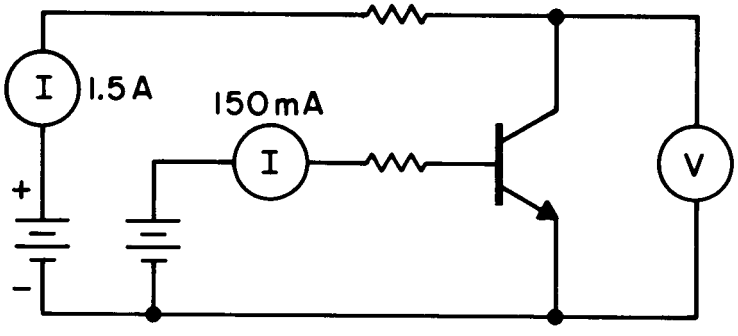


Fig. 11. Circuit for saturation voltage test

PART A

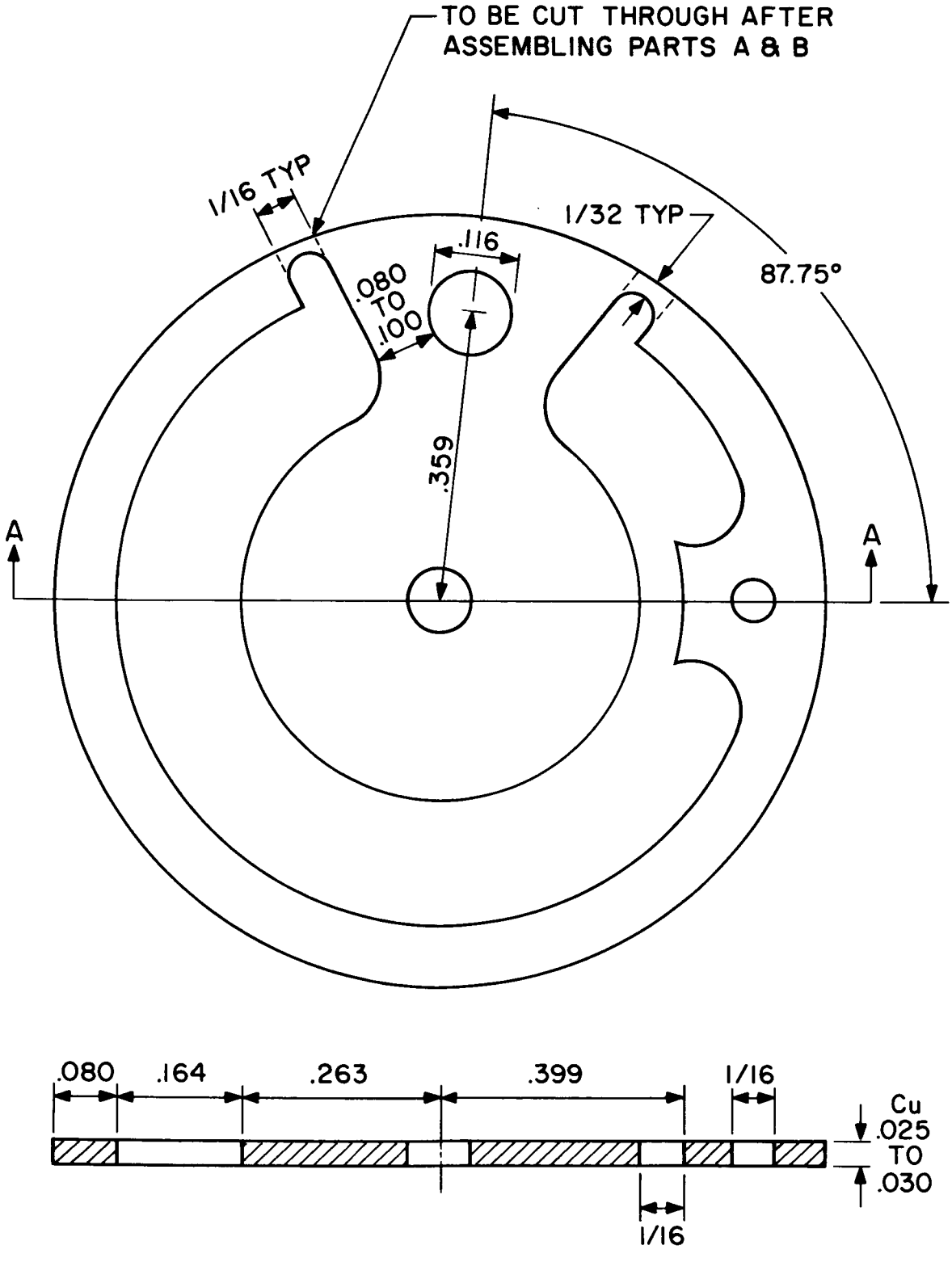


Fig. 12. Part A of subassembly

5-19-66
51536

PART B

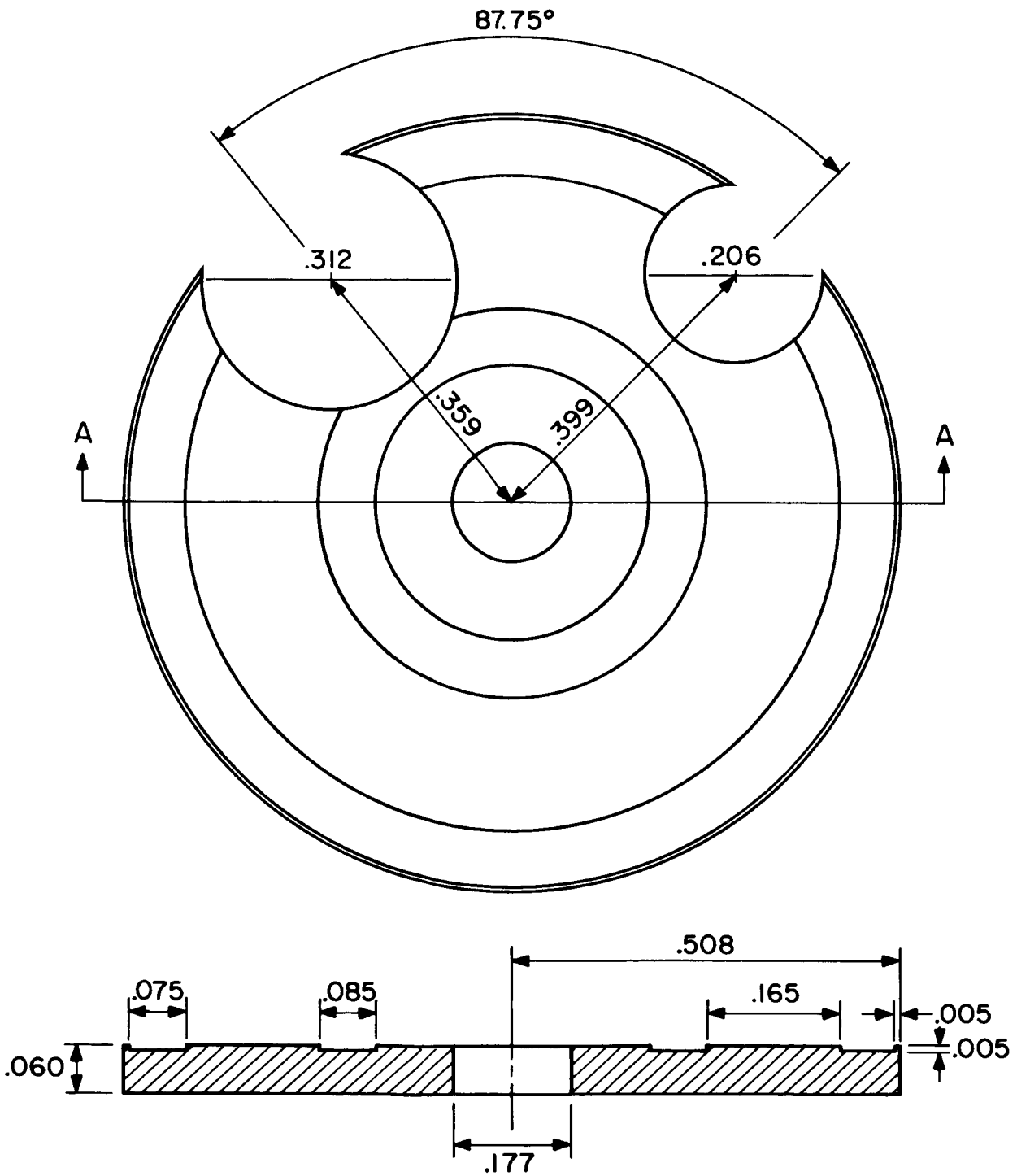


Fig. 13. Part B of subassembly

5-19-66
51535

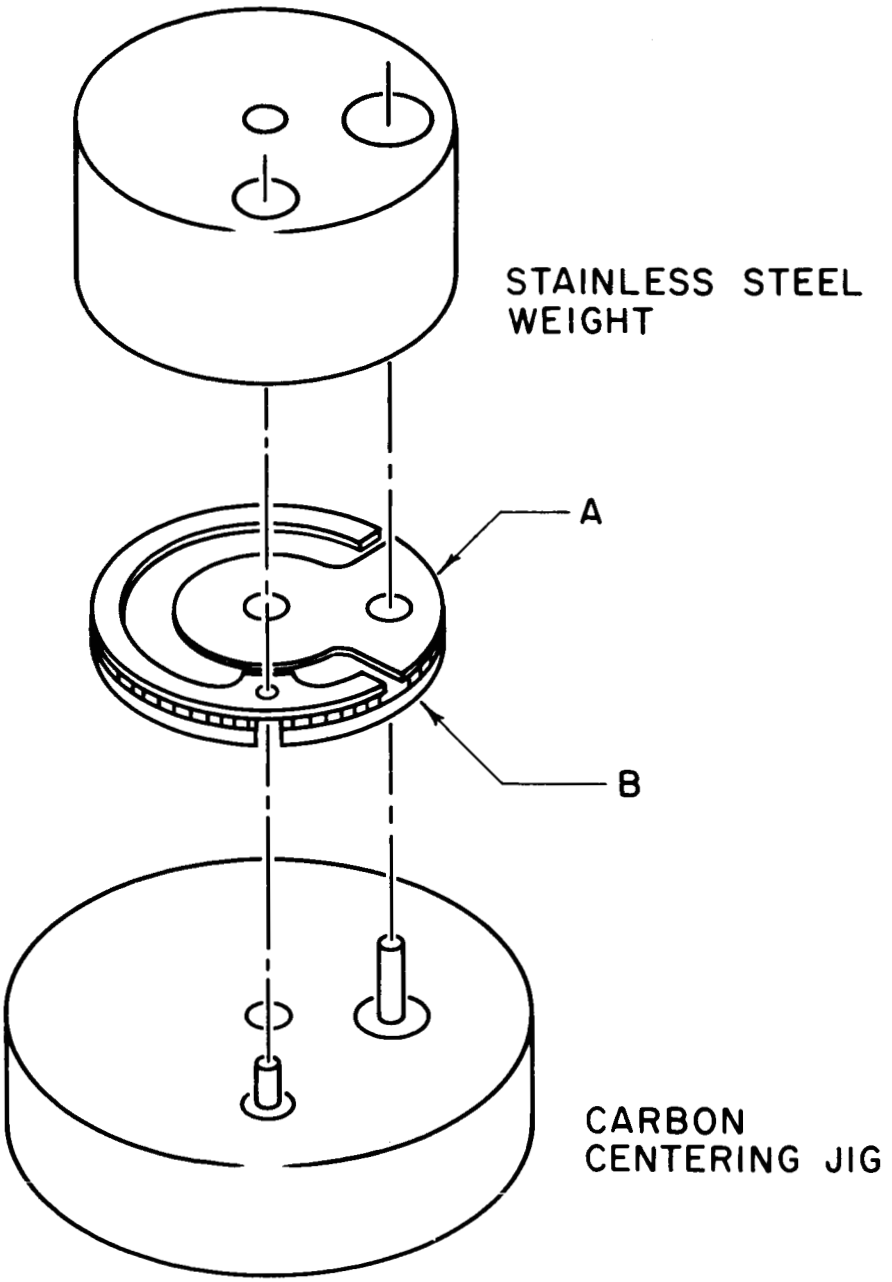


Fig. 14. Construction of subassembly.

5-19-66
51538

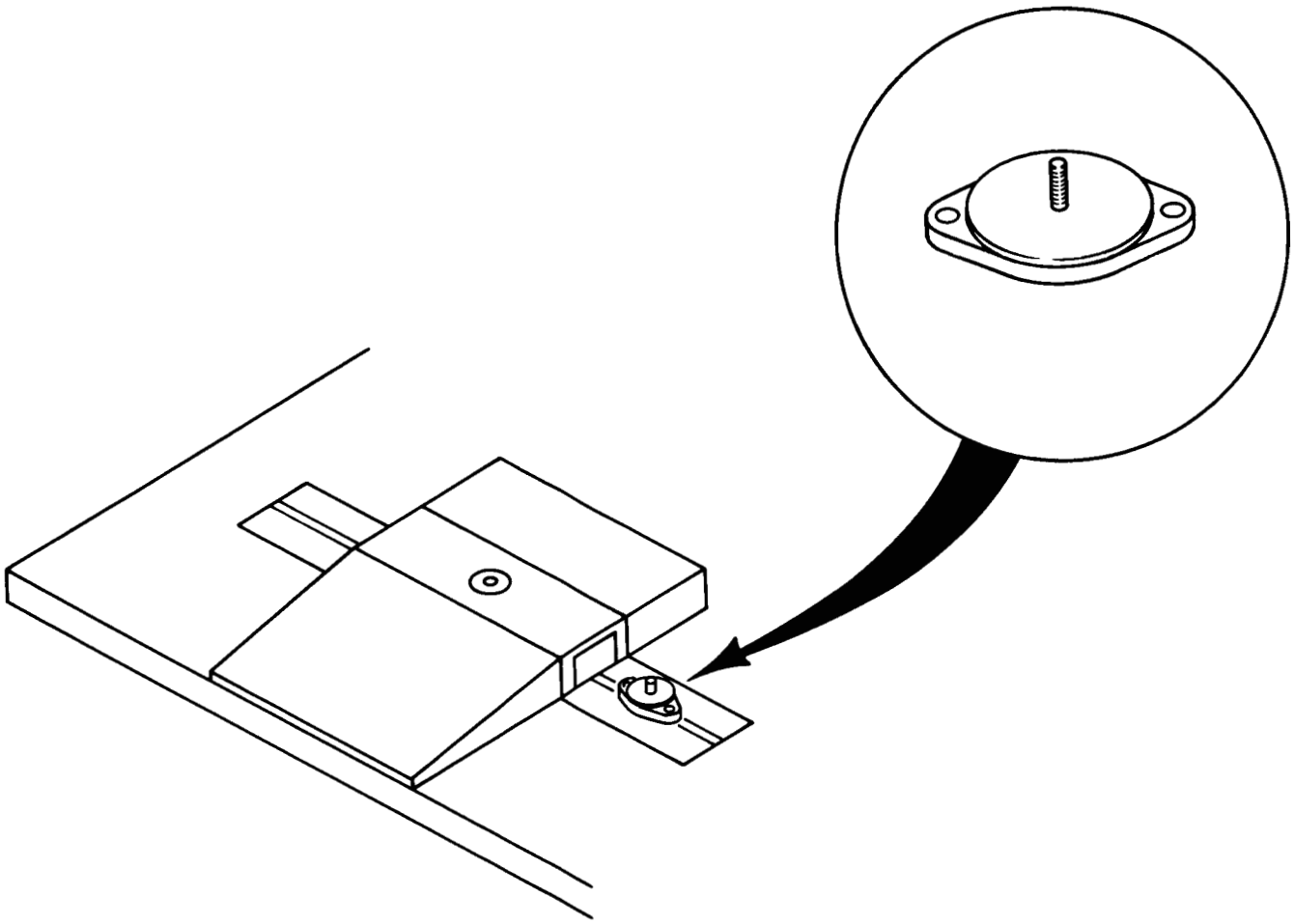


Fig. 15. Fixture for soldering chips on subassembly

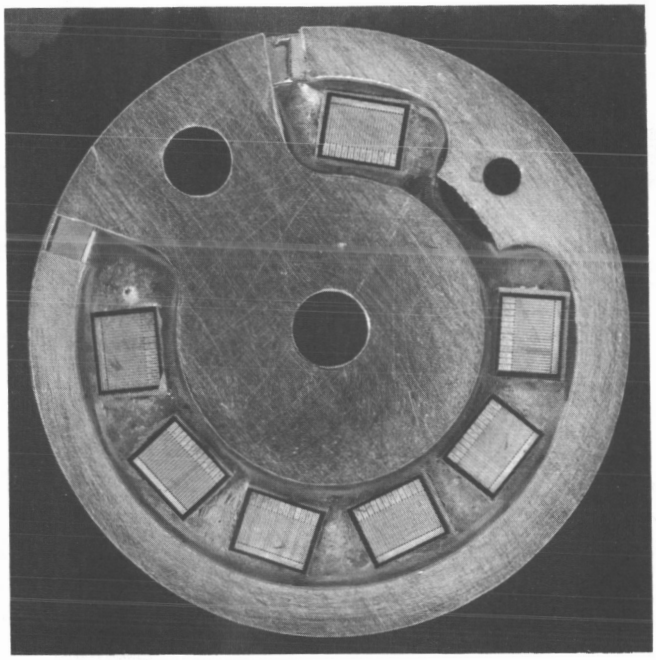


Fig. 16. Chips mounted on subassembly

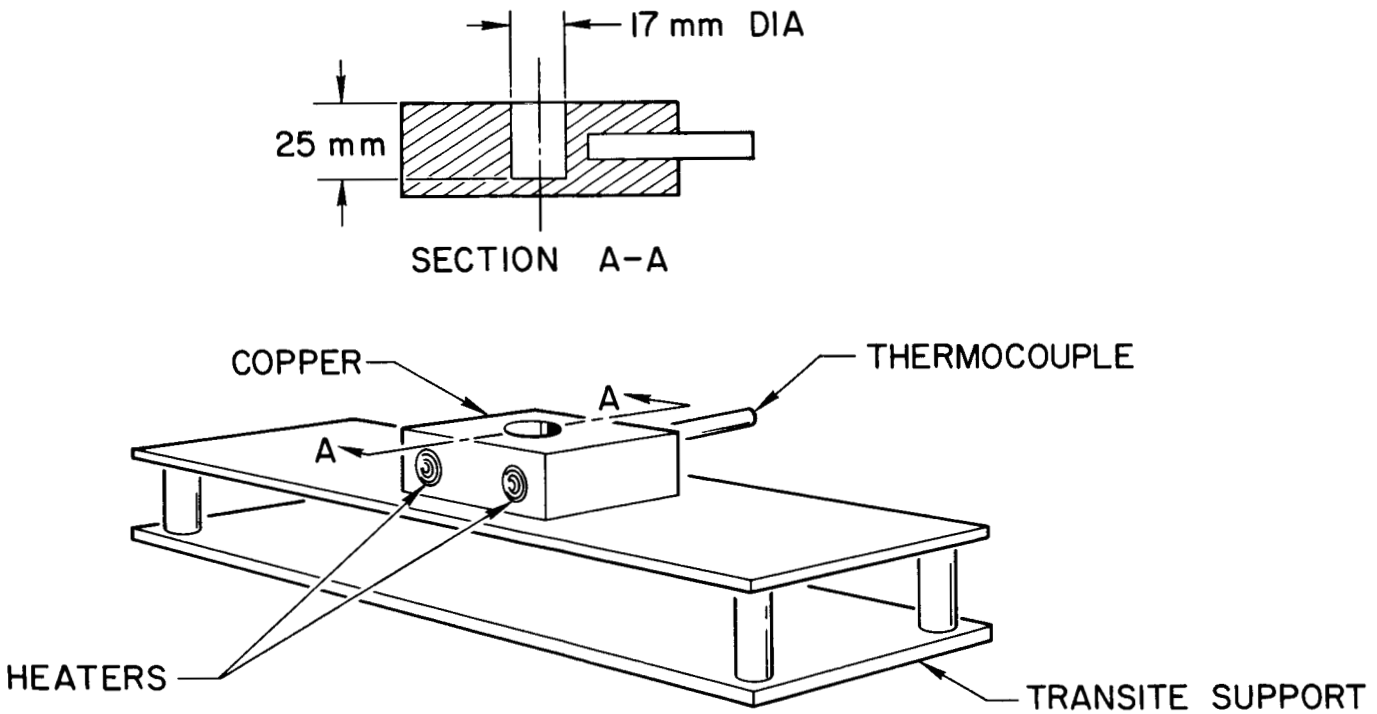
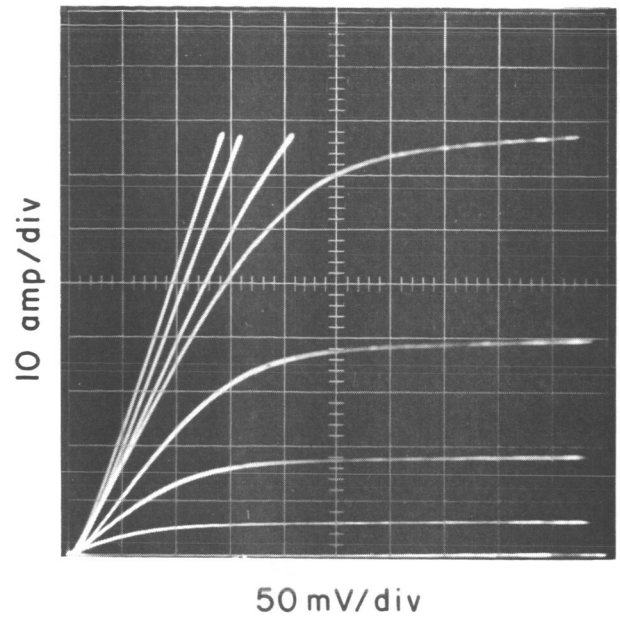


Fig. 17. Fixture for soldering 1-1/4 inch stud package



I_B = 5.0 ampere
3.0
1.5
1.0
0.5
0.25
0.1
0

Fig. 18a. I_C vs V_{CE} for a typical transistor

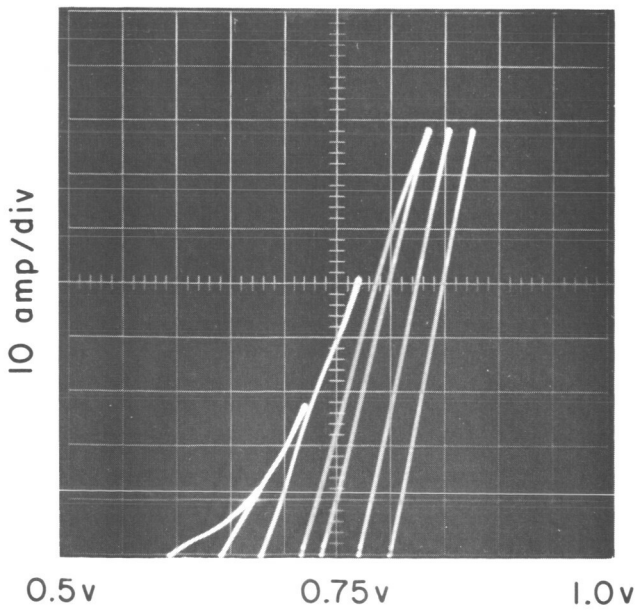


Fig. 18b. I_C vs V_{EB} for a typical transistor

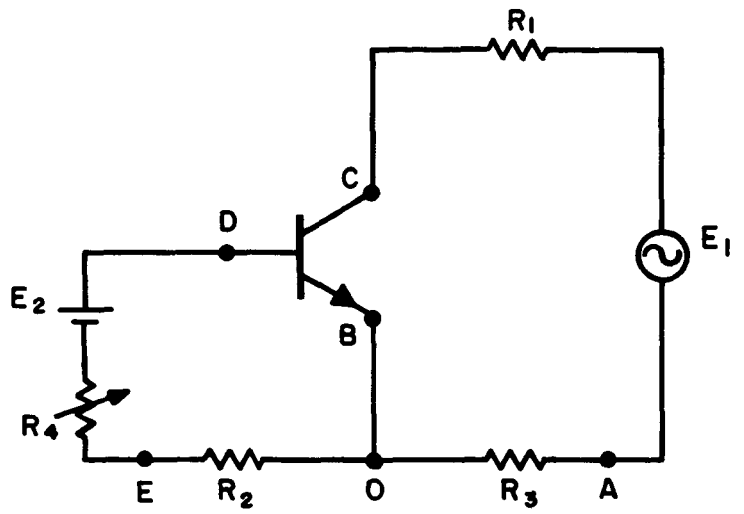


Fig. 19. Circuit used for measuring V_{EC} and V_{EB} vs I_C

E_1 Bridge Rectified Power Supply, 100 amp, 20 volt - ITT

E_2 Power Supply, 5 amp, 20 volt - Power Designs, Model 2050

R_1 0.3 ohm Resistor (5 x 1.5 ohm, 250 watts)

R_L 1.0 ohm Resistor - Base Current Sensor (15 x 15 ohms, 15 watt (Lectrohm)

R_3 0.001 ohm Resistor - Collector Current Sensor (50 amp Meter Shunt)

R_4 0.5 ohm Variable Resistor - Base Current Fine Control (Ohmite Vitreous Rheostat 150 watt-Model Series A)

O Common Terminal

A To Vertical Amplifier of Oscilloscope

B To Horizontal Differential Amplifier of Oscilloscope

C To Horizontal Differential Amplifier of Oscilloscope (1)

D To Horizontal Differential Amplifier of Oscilloscope (2)

E To Base Current Monitoring Meter

Oscilloscope - Tektronix Type 536 with Plug-in Units, Type 53/54D on Vertical, Type W on Horizontal.

Meter - Triplett VOM 630-A.

Oven - Delta Design, Inc. Model 6545W: with A.P.I. Thermocouple Control