DIGITAL SYSTEMS LABORATORY

ENGINEERING DIVISION CASE INSTITUTE OF TECHNOLOGY

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THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

THEORY AND DESIGN TECHNIQUES FOR MAGNETIC-CORE MEMORIES

Vol. I of II

Report No. 1-66-38

by

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1966

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ERRATA

P 4 — Lines 9 and 10
should read.. The core is either set or reset, and the presence or absence of an output is observed....

P 49 — Line 13
should read.. voltage occurs only then indicating that the function is true....

P 153 — Line 14
should read.. in an ℓxm bit plane...

Line 20
should read.. cores in an ℓxm bit plane...

Line 15
should read.. and the result is dependent upon whether ℓ and m are ....

P 166 — Fig 5-7 — The upper equation should be

$$I_d / I_{sm} = K = 1/2 \left(\frac{1 + \Delta}{1 - \Delta}\right) (1 + \Delta)$$

and the lower equation should be

$$I_d / I_{sm} = K = 1/2 \, (1 + \Delta) \, / \, (1 - \Delta)$$

P 181 — Fig 5-12 — The equation should be

$$\Delta_I = \frac{(2I_d / I_{sm} - 1) - \Delta_w}{1 + (2I_d / I_{sm} + 1) \, \Delta_w}$$

P 319 — Fig 9-2 — All resistors should be 6.8K and not 608K

ABSTRACT

A tutorial discussion of magnetic-core memories is presented with emphasis placed on memories that would be suitable for use in special purpose digital computers or control systems.

The material is developed in a manner that allows the two usual forms of core memories to be logically synthesized following a review of relevant concepts from magnetic-circuit theory. A discussion of practical problems of memory cores then leads to the development of design considerations for core memory systems. Many examples are used to illustrate the problem of selecting a core for use in a memory and the design of the electronic circuitry necessary to operate a core memory.

The work is concluded with a procedure for the design of a core memory and an example to illustrate its use.

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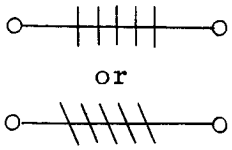
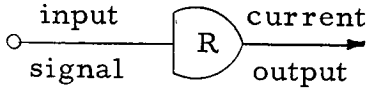
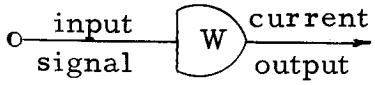


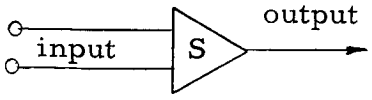
Line of Memory Cores



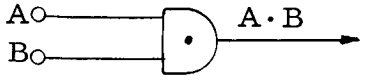
Read Current Driver



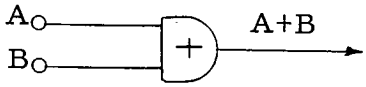
Write Current Driver



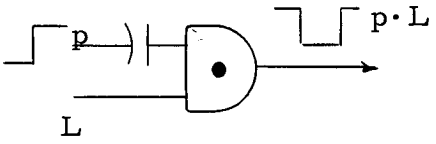
Sense Amplifier (may sometimes have only one input shown)



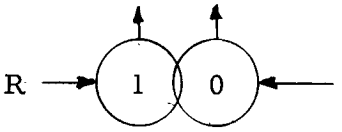
AND Gate (functional)



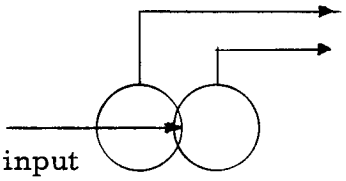
OR Gate (functional)



Gated Pulse Generator



RS flip flop (Bistable Multivibrator)



Monostable Multivibrator

CHAPTER 1

INTRODUCTION

1.1 Introductory Comments

Any digital control system or computer is characterized by its possession of a memory sub-system where instructions and/or data are stored.[1*] In all but the simplest of digital systems, the memory sub-system is clearly defined and would be given a separate block in the system block diagram. Oftentimes the design specifications will demand or perhaps suggest that a random-access memory - that is, a memory in which each word of stored data is just as readily accessible at a given time as is any other word - be used, and "transistor driven core memories ... have become the classic form of random access memories."[2]

The first core memories were constructed in the early 1950's. Because they were intended for use with general purpose computers, they were relatively large, providing storage for several thousand words of data. The cycle time - the time required to read and write information at any given memory address - of these early memories was on the order of 10 to 15

*Superscripts in each chapter refer to the references listed in the last section of each chapter.

microseconds. These systems were quite large in physical size since they were operated by and in conjunction with vacuum-tube equipment. As the technology improved and with the advent of the transistor, the physical size decreased, and operating speeds increased. In the early 1960's cycle times on the order of two microseconds were realizable.[2, 3]

In 1965 and in early 1966 cycle times on the order of one microsecond were commercially available, and also the first core memories utilizing integrated circuits for their control appeared on the market. Physical size had been reduced to the point where a fairly large capacity memory could be contained in a package six to eight inches high.

In December of 1965 it was announced that the International Business Machines Corporation had developed an 8192 word core memory with a cycle time of 375 nanoseconds utilizing extremely small cores with an outside diameter of 12 mils (over 17,000 of these cores will fit inside the hole of a Life Saver). At the same time it was announced that Control Data Corporation was developing a core memory with a cycle time of 250 nsec., and that I.B.M. was endeavoring to achieve a cycle time of 110 nsec.[4]

These trends of increased speed and decreased physical size have been coupled with a trend for increased storage capacity. To illustrate, the first core memories of 1953 provided in the neighborhood of 15, 000 bits of storage; core memories with capacities of two to three million bits were in use around 1960.[3] In the spring of 1965 a core memory "capable of capacities up to 20 million bits" was demonstrated by Fabri-Tek, Incorporated.[5]

These historical trends reflect the continued development of more compact, faster, and physically smaller general purpose computers. However, in small, special-purpose computers and digital control systems, the storage requirements may be considerably less than those of a general purpose computer (a few hundred words or less in comparison to several thousand words or more), and the necessary operating speed may be considerably slower (cycle times on the order of milliseconds in some instances). Although the requirements are quite different from those of a general purpose computer, a core memory may still provide the most attractive solution in the design of these special purpose systems.[3]

1.2 Logical Properties and Types of Square-Loop Magnetic Cores

The square-loop magnetic core has two stable states in its

magnetic hysteresis loop and is therefore commonly used to store a single binary digit (a 1 or a 0). The core may be set (told to store a 1) or reset (told to store a 0) but not triggered (told to compliment its present state). It therefore falls into the general classification of RS memory elements. In addition, the square-loop core as typically used has the following two important properties:

1. Read-out is destructive because the core only gives an output during the transition between states. In order to determine its present contents, the core is set or reset and observing whether or not there is an output. For example, if the core is presently storing a 1 and is reset, it makes a 1 to 0 transition and there is an output; but if it is presently storing a 0 and is reset, it does not change states and there is no output.

2. The core may be used to perform logical gating in that it is a current operated device which is capable of summing independently generated and simultaneous currents, together with sign, and interpreting the sum to be a set command, a reset command, or no command.

Square-loop cores are generally either "tape-wound" cores or ferrite. Tape-wound cores are made by winding ultra-thin metallic tape on a bobbin, while ferrite cores are molded of iron oxide and other metallic oxides. Virtually all magnetic-core memories use the ferrite cores as storage elements because they are much less expensive to manufacture than the tape-wound cores. In addition, the ferrite cores may be made much smaller than the tape-wound cores (20 to 80 mills in outside diameter as compared with 0.20 in. and up) which gives decreased physical size to the memory and higher speeds of operation.[3, 5] Indeed, although the idea of the random-access core memory was proposed before the advent of the ferrite core, the first practical core memories were constructed with ferrites.[3]

The small ferrite cores which are manufactured primarily for use in memories are termed ferrite memory cores or simply memory cores. Larger ferrite cores (with outside diameters greater than 0.10 in.) and the tape wound cores are best suited for other purposes and are termed switch cores.

The trend today is towards the use of smaller and smaller cores. The advantages of smaller cores are:

1. They allow memories that are smaller in physical size.

2. They allow increased operating speeds.

3. Less energy is required to store and retrieve a bit of data.

The first is self explanatory, the second is demonstrated in Chapter 4, and the third is demonstrated in Chapter 2.

In addition to toroidal cores, there are what are called multi-aperture cores available. These are small ferrite devices capable or storing a single bit of information and available in various shapes having two or more holes through which wires may be passed. Their chief use is in random access memories requiring non-destructive read-out as well as ease in altering stored data.[7]

1.3 The Basic Design Problem

A magnetic-core memory consists of many magnetic cores, each core storing one bit of data. Typically the cores are strung on wires in a two or three dimensional array. The wires not only provide support for the cores, but carry the input and output signals as well.

Because the core acts as a gate as well as a memory element, magnetic-core memories are inherently simple in nature.

However, the inputs required and the outputs produced by the cores are not directly compatable with conventional transistor logic, and consequently an interface must be provided between the transistor logic system and the memory system.

The capacity of the memory is generally specified by system requirements; therefore, the number of cores and their cost may be considered relatively fixed. The biggest variable in the cost of the memory system is in the interface which consists primarily of current generators and sensing amplifiers.

The final form, and hence the cost, of the interface will depend partially upon:

1. The geometry of the core array.
2. The electrical characteristics of the core chosen for use.
3. The required speed of operation.
4. The electrical properties of the associated logic system.

1.4 Purpose of this work

In order to allow the digital systems designer to best utilize core memories, it is the purpose of this work to enlighten

him as to the properties and operation of conventional magnetic-core memories in general and as to design methods and criteria for small (on the order of a few hundred words or less) magnetic-core memories in particular.

Particular emphasis is placed on the design of small memories for several reasons. First of all, large memories with storage capacities ranging from 256 to 8192 words are commercially available from several manufacturers. Secondly, the general design techniques for the smaller memories are not so specialized that they cannot be applied to larger memories. And finally, the literature is virtually void of mention of the savings that can be achieved in small memories, particularly when high speed is not involved.

Furthermore, discussion will be limited to the use of conventional ferrite memory cores as they are typically used. Discussions of switch cores and design details of their applications are to be found in References 3, 6, 7, and 8 of Chapter 7 . The electronic circuitry necessary to operate memories utilizing multi-aperture devices does not differ too much from that required to operate conventional core memories, and it is felt that the reader who wishes to employ these devices will still find this work a good

reference. Also other storage devices sometimes used in random access memories such as the twister and thin films are excluded from the discussion as are several novel but not too successful ideas involving core memories that have appeared in the literature over the years.

1.5 References for Chapter 1

1. Ledly, R.S., Digital Computer and Control Engineering, New York: McGraw Hill Book Co., 1960, pp 26-29.

2. Rajchman, J.A., "Computer Memories: A Survey of the State-of-the-Art", Proceedings of the IRE, Vol. 49, Jan., 1961.

3. Quartly, C.J., Square-Loop Ferrite Circuitry: Storage and Logic Techniques, London: ILIFF Books Ltd. (Englewood Cliffs, New Jersey: Prentice Hall, Inc. 1962, pp.3-8.

4. "The Speed Limit", Electronics, Vol. 38, No. 26, Dec. 27, 1965, p. 36.

5. "M.I.T. Buys Mass Memory", Fabri-Tek Inquirer (Available from Fabri-Tek Inc., Minneapolis 2, Minn.), Vol. 2, Issue 5, p 1.

6. Meyerhoff, A. J., et al., Digital Applications of Magnetic Devices, New York: John Wiley and Sons, Inc., 1960, pp. 30-31.

7. Quartly, pp. 58-62.

CHAPTER 2

QUALITATIVE DESCRIPTION OF SQUARE-LOOP CORES IN TERMS OF MAGNETIC CIRCUITS

It is the purpose of this chapter to review some results from magnetic circuit theory that are essential to a thorough understanding of square-loop cores. This information is necessary background for Chapter 3, where the logical structure of core memories is developed. Discussion of practical details of ferrite memory cores is postponed until Chapter 4 for two reasons:

1. An understanding of the logical structure and the basic operation of a core memory is needed to appreciate the practical problems of memory cores.

2. The fundamental concepts involved in core memories are independent of these practical details, and the development in Chapter 3 is neater without becoming involved in the practical details.

2.1 Digital Operation of the Square-Loop Core

The general form of a hysteresis loop for a magnetic material is shown in Fig. 2-1, and an ideally square hysteresis loop is shown in Fig. 2-2. The independent variable H is the vector quantity magnetic field intensity, has the units amperes per meter in the rationalized MKS system, and is a measure of the magnetic excitation applied to the material by a current. The dependent variable B is the vector quantity magnetic flux density, has rationalized MKS units of webers per square meter, and is a measure of the total magnetic field inside the material due to the application of a given H.[1]

It is seen that when there is no excitation B has two possible values, $+B_R$ and $-B_R$, and B will stay at either of these two values until an excitation is applied. The hysteresis loop, therefore, has two stable states, and it is possible to store one bit of binary data in the sign of B. For example, the state at $+B_R$ could be defined to store a one, and the state at $-B_R$ defined to store a zero.

Suppose that a core is made of a material having the hysteresis loop of Fig. 2-2 and is at the point $B = -B_R$, $H = 0$. If a positive H is applied whose magnitude is less than H_0, the value of

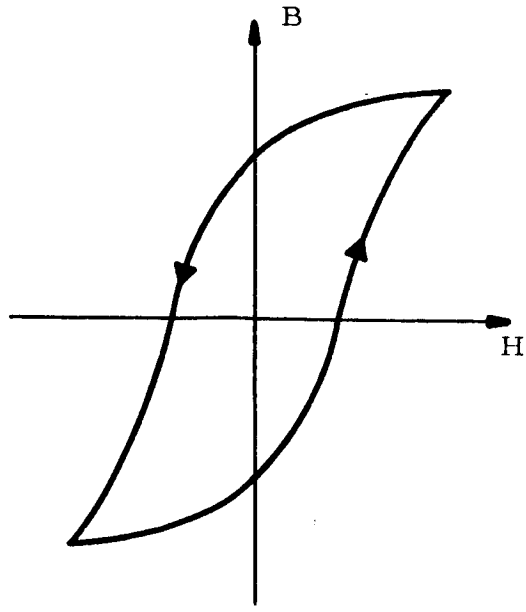


Fig. 2-1: A Hysteresis Loop

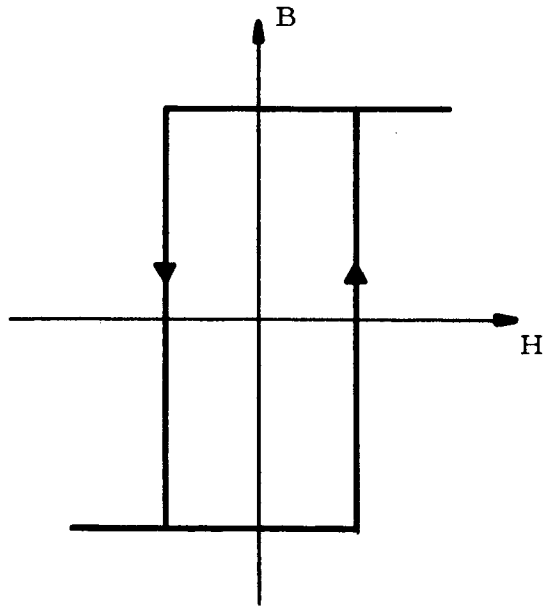
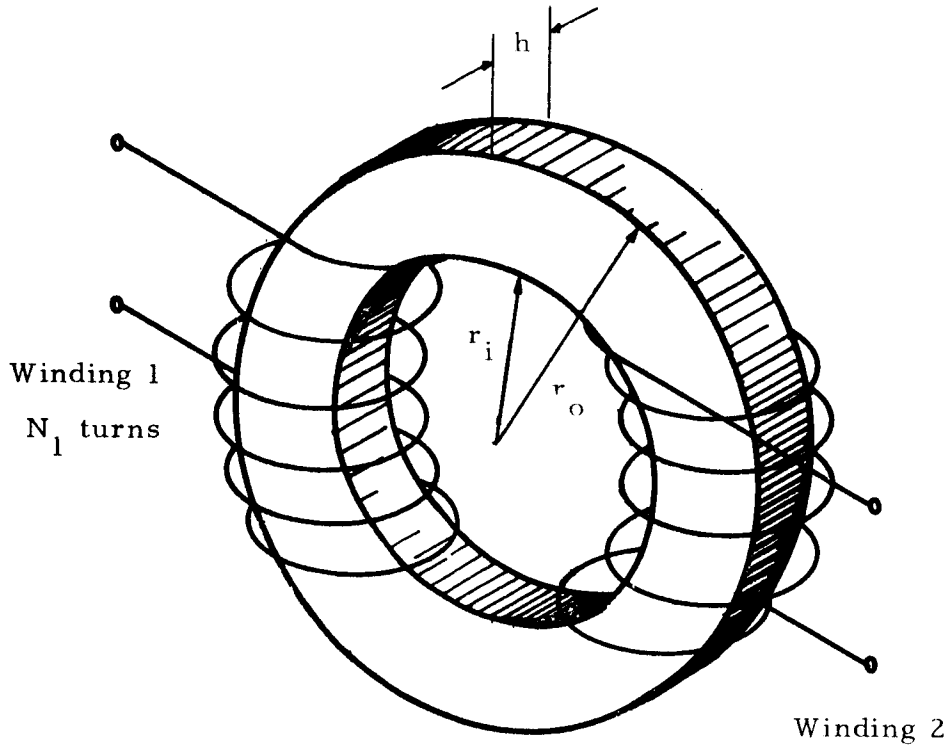


Fig. 2-2: An Ideally Square Hysteresis Loop

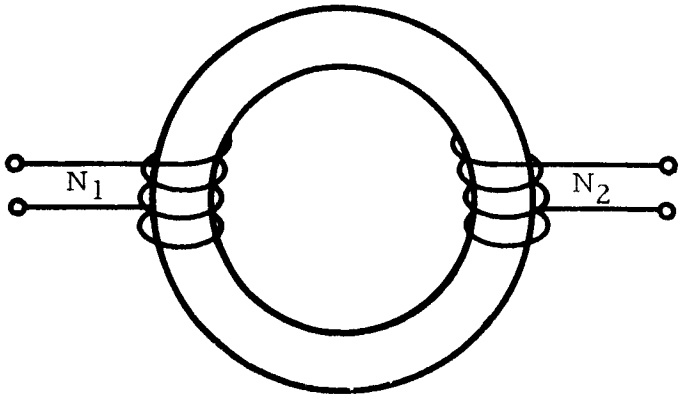
B does not change; and upon removal of the excitation, the material will return to the state that it was initially in. However, application of a positive H greater than H_0 causes a large change in B of $2B_R$, and upon removal of H the state at $+B_R$ is reached. Clearly, application of the proper negative H will cause the return to $-B_R$. Also when the device is at $+B_R$ and any positive H is applied (or when at $-B_R$ and any negative H is applied) and then removed, there is no change in B during the excitation period, and the original state is returned to.[2, 5]

Thus, a magnetic core of square-loop material has as inputs bipolar excitations of H and behaves in a similar manner to an RS memory element. Furthermore, because the excitation must exceed the threshold H_0, logical functions may be implemented by summing the outputs of two or more independent sources of H.

Fig. 2-3 shows pictorially and schematically a toroidal core with two windings on it, and it will be temporarily assumed that the toroid is made of a material having the hysteresis loop of Fig. 2-2. A current flowing in either winding produces a magnetic excitation, H; and a change in B produces a voltage across both windings. As an example of how this core may be used to store information, assume that winding 1 is to be used for providing excitation, and



(a) Pictorial



(b) Schematic Representation

Fig. 2-3: Torroidal Core of Magnetic Material with Windings

winding 2 is to be used for outputting information. Define the stable state at $+B_R$ to be the logical "one" state and the state at $-B_R$ to be the "zero" state. To set the core, a current is provided in winding 1 such that an H is produced of proper sign and of sufficient magnitude to drive the core to the $+B_R$ or "one" state. To reset the core, a current (in the opposite direction) is provided to drive the core to $-B_R$ or the "zero" state.

To read or retrieve, at time n, the binary digit stored in the core, the core may be reset at that time. If the core is already in the zero state then there is no significant change in B and no voltage appears at the terminals of winding 2. But, if the core was in the one state a large change in B occurs at time n, producing a voltage at the output. Thus, the presence or absence of a voltage at time n indicates whether the core stored a one or a zero at time n-1.[2, 5] Clearly, information could also be retrieved just as readily by setting the core at time n.

The output is normally used in one of two ways: it may be used to provide current excitation for other cores, or it may be sensed by an electronic amplifier and shaped to operate other forms of digital circuitry.[6] In the first case the output is heavily loaded, and the core acts as a current transformer.

In the second case the output sees essentially an open circuit. The cores of a memory are normally operated under open-circuit conditions, and with the exceptions of Sect. 2.2.6 and Sect. 7.3, the remainder of this work will be concerned with the operation of memory cores under these conditions.

2.2 Review of Magnetic Circuit Fundamentals

In order to arrive at a more detailed understanding of the operation of square-loop cores, it is first necessary to briefly review some of the fundamentals of electromagnetic theory which pertain to magnetic circuits. Recall that a magnetic circuit is characterized by well defined, closed paths in which a magnetic flux density may exist and that a negligible flux density exists outside the paths.[1] A square-loop core is a closed path with this property and, therefore, is a simple form of a magnetic circuit. Most of the material in this section is covered in such sources as References 1, 2, 3, and 6.

2.2.1 Magnetic Field Intensity and Magnetomotive Force

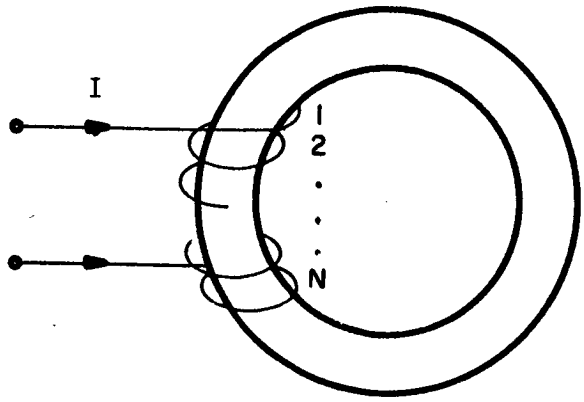
The magnetic fields of interest here are produced by electrically charged particles in motion, i.e., a current. An important relationship between current flow and an $\vec{H}$ field in the region of the current is Ampere's circuital law which states that

the line integral of $\vec{H}$ around a closed path, ℓ, is exactly equal to the net amount of current enclosed by the path (or equivalently, the net amount of current which pierces the surface bounded by the path). Expressed in vector notation[7]

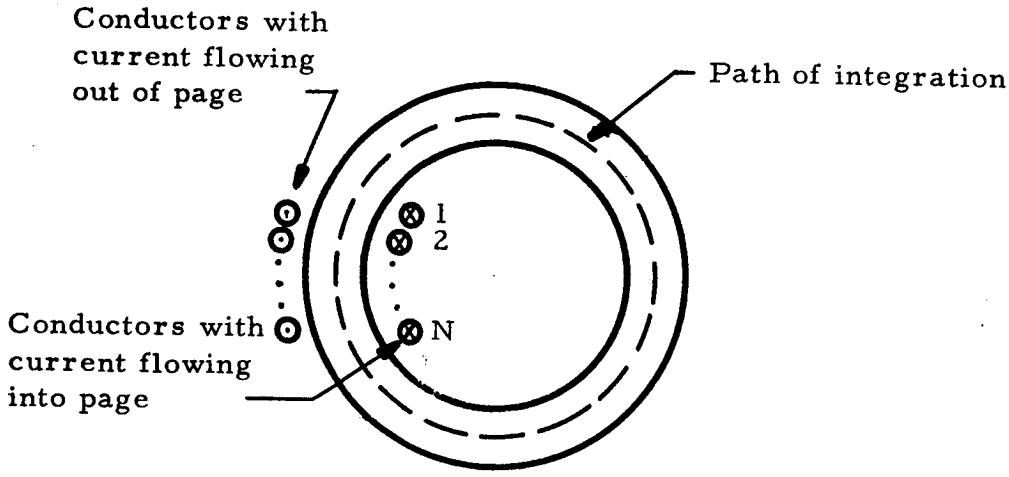
$$\oint \vec{H} \cdot d\vec{\ell} = I_e \qquad (2.2.1)$$

where I_e is the net enclosed current, and $d\vec{\ell}$ is an incremental length of the path.

Application of Ampere's law will now be made to the toroid of Fig. 2-4a which has one winding of N turns with a current I flowing into the upper terminal. A cross sectional view is shown in Fig. 2-4b; a circular path ℓ inside the toroid and centered at the axis of the toroid has been chosen as the closed path of integration. If the number of turns is defined to be equal to the number of times the conductor passes through the core, the current enclosed by the path is NI as indicated by the figure; and Ampere's law states that the value of the integral in (2.2.1) around the path is exactly NI. This may be interpreted to say that there is a net $\vec{H}$ field in a direction that is tangential to the path. If the length of the path is L then the average magnitude, H_{ave}, of the components of the field



(a) Schematic



(b) Cross Section

Fig. 2-4:

Core with one winding of N-turns carrying a current of I amps

tangential to the path is

$$H_{ave} = \frac{NI}{L} \qquad (2.2.2)$$

The direction of the tangential field (clockwise or counter-clockwise) is determined by the right-hand rule which states that if the thumb of the right hand is pointed in the direction of net current flow, then the fingers of the right hand curl in the direction of the field. In Fig. 2-4b the net tangential H field is in the clockwise direction.

Now as the radius of the path is varied, it is seen from equation (2.2.2) that along the inside circumference H_{ave} is greater than at the outside circumference which has a longer path length. A mean value of H_{ave} occurs on the mean circumference of the core, and it is this value of H that is generally given as the independent variable on the B-H characteristic for a material. However, in taking data for the characteristic, steps are generally taken to insure that H is nearly uniform along the mean path.[8]

In most memory applications a core is typically threaded on one or more conductors (the conductors actually provide the means of support for the core). Fig. 2-5a shows a core threaded by two

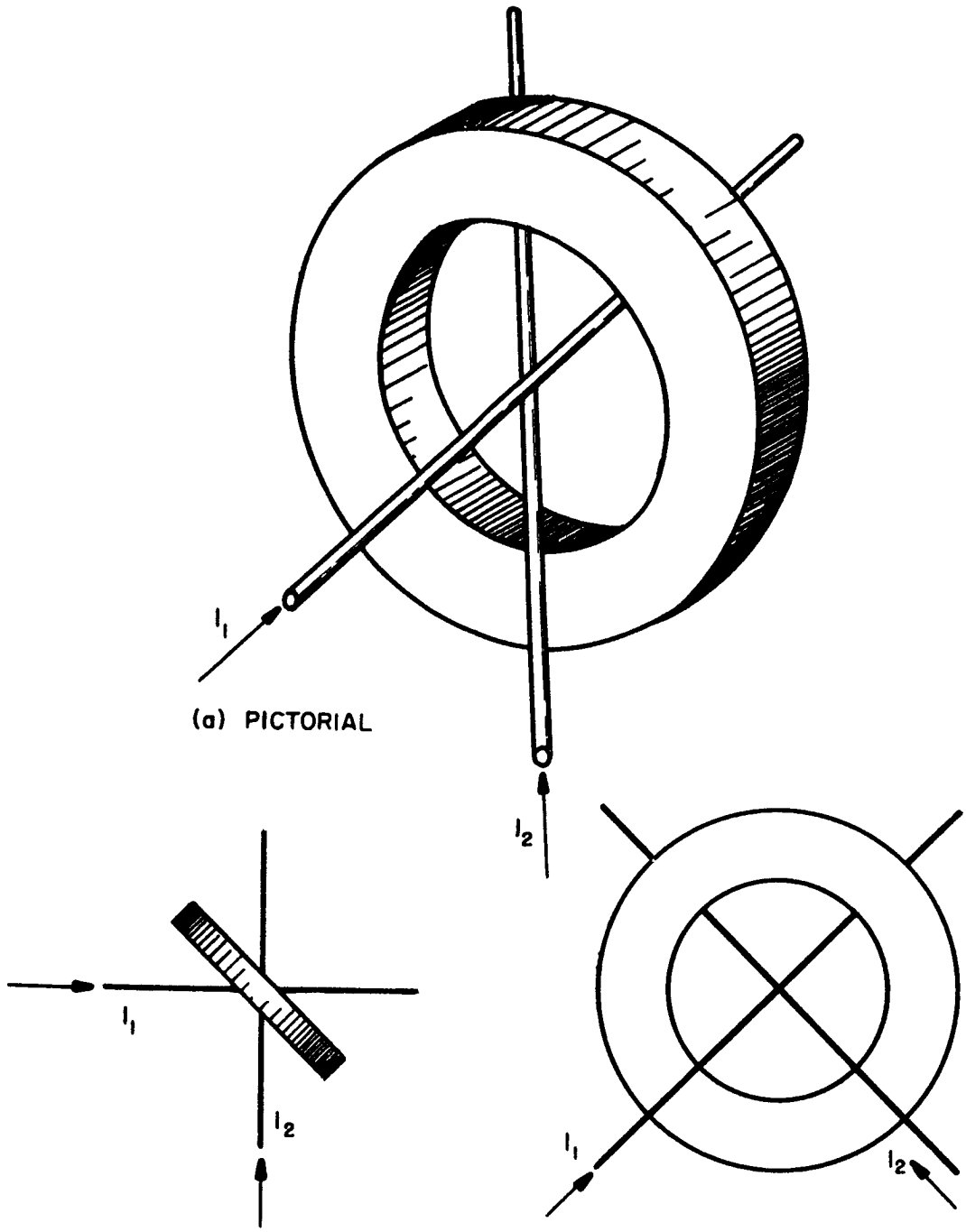


Fig. 2-5: Core Threaded on Two Conductors

conductors carrying I_1 and I_2 amperes respectively in the directions shown. Fig. 2-5b shows two common schematic representations of the configuration. Ampere's law (2.2.1) is independent of how the enclosed current crosses the surface formed by the closed path of integration. Thus, if a path is chosen around the core as in the preceding example, the current enclosed is $I_1 + I_2$; and the average value and direction of H around a given closed path in the core is the same as if the core had an N turn winding carrying a current of $(I_1 + I_2)/N$ amp., even though the actual H field is not exactly the same for both cases. Thus, each wire acts as a separate winding of one turn.

The numeric value of the integral in Ampere's law is called the magnetomotive force around the path $\mathscr{l}$ (abbreviated mmf and symbolized F). That is,

$$F = \oint \vec{H} \cdot d\vec{\mathscr{l}} = I_e \qquad (2.2.3)$$

Because an mmf is usually (or may be considered as being) generated by an N-turn coil carrying I amps, mmf is usually stated in the units "ampere-turns". It should be emphasized that mmf (like electromotive force) is a scaler quantity and not a true vector force.

For a given closed path, the mmf is exactly equal to the enclosed current, and H_{ave} on the path is directly proportional to the mmf. Thus, for a particular core (or any given magnetic circuit in general) F may be used as the independent variable on the magnetic characteristic rather than H; and it is frequently convenient to do so since F is merely the current times an integral number of turns and, therefore, easier to handle.

2.2.2 Total Field Inside a Magnetic Material

The motion of sub-atomic, charged particles inside a material constitute tiny current loops, and a tiny magnetic field is associated with each. In general, the sub-atomic current loops are randomly aligned and their associated fields cancel one another producing zero net field. However, when an external magnetic field is applied, they tend to become aligned with it and either aid or oppose it depending on the material.

The net field in the material produced by the sub-atomic currents alone is called the intrinsic field, and it may be represented by the vector $\vec{M}$ which has the same dimensions as $\vec{H}$ and is termed the magnetic polarization vector. The total magnetic field intensity inside the material, $\vec{H}_T$, is the vector summation of the applied field $\vec{H}$ and the magnetic polarization vector.

$$\vec{H}_T = \vec{H} + \vec{M} \qquad (2.2.4)$$

In nonmagnetic materials $\vec{M}$ is very small in comparison to and directly proportional to the applied $\vec{H}$; the total field is then essentially $\vec{H}$. But in ferromagnetic and ferrimagnetic materials, $\vec{M}$ is much greater than $\vec{H}$; and once a particular $\vec{M}$ is established, it tends to remain established with the removal of $\vec{H}$ giving rise to hysteresis. In the magnetic materials the relationship between $\vec{M}$ and $\vec{H}$ is nonlinear and highly dependent on the present value of $\vec{M}$. Stated another way, the present value of $\vec{M}$ is a function of the present value of $\vec{H}$ and the entire past history of the speciman of the material.

It is clear that for a given material $\vec{M}$ must have a maximum value which occurs when all sub-atomic currents that are available for alignment are aligned so that their magnetic fields all aid one another. When this occurs the material is said to be saturated.

2.2.3 Magnetic Flux Density

A magnetic field may be represented by lines of magnetic flux that are everywhere in the same direction as $\vec{H}_T$. The number of lines of flux, ϕ, in a particular region is proportional to the

magnitude of $\vec{H}_T$ in that region. The amount of flux crossing a given surface S may be found by the surface integral

$$\phi = \int_s \mu_0 \vec{H}_T \cdot d\vec{s} \qquad (2.2.5)$$

where the proportionality constant μ_0 is the permeability of free space, and $d\underline{s}$ is an increment of surface area.

The magnetic flux density vector $\bar{B}$ may be defined as

$$\vec{B} = \mu_0 \vec{H}_T = \mu_0(\vec{H} + \vec{M}) \text{ webers/meter}^2 \qquad (2.2.6)$$

and equation (2.2.5) is usually written as

$$\phi = \int_s \vec{B} \cdot d\vec{s} \text{ webers} \qquad (2.2.7)$$

Because there is no source or sink of magnetic flux (and hence every flux line must close on itself) and because the intrinsic field of the core tends to align itself with the applied field, the B field is either in a clockwise or counter-clockwise direction around the core. That is, the magnetic core forms a path for magnetic flux.

In dealing with magnetic cores it is usually assumed that $\vec{B}$ is uniform throughout the core and that any $\vec{B}$ field outside the core is neglegible in comparison to that inside the core. Under these assumptions the flux is entirely contained in the core, and its direction is either clockwise or counter-clockwise. If the cross sectional area of the core is A, the total flux in the core is given by

$$\begin{aligned} \Phi &= |\vec{B}| \cdot A \\ &= |\vec{B}| \cdot (r_0 - r_I) \cdot h \end{aligned} \qquad (2.2.8)$$

since $\vec{B}$ is assumed uniform, and r_0, r_I, and h are the dimensions shown in Fig. 2-3.

For a given core, then, ϕ may be used instead of B as the dependent variable on the magnetic characteristic.

2.2.4 Hysteresis Loops

Because the present value of magnetic-flux density inside a magnetic core is a function of the entire past magnetic history of the core as well as the presently applied excitation, it is apparent that B may take on other values than those indicated by a hysteresis loop. For example, it is possible for a magnetic material to have zero magnetic flux when there is zero excitation. This corresponds

to the point $B = H = 0$ (or $\phi = F = 0$) on a magnetization characteristic; and when a material is at this point, it is said to be completely demagnetized.

Assume now that the core of Fig. 2-4 is in such a condition of demagnetization, and that a gradually increasing current is caused to flow in the winding to apply a slowly increasing mmf (or H) to the core. As the mmf increases, the flux in the core also increases in a fashion depicted by curve OAC in Fig. 2-6. When point C is reached, $\vec{M}$ has virtually reached its maximum value, and any further increase in applied field results only in a very small increase in total flux as indicated by the extension of the curve to point C'. When point C has been reached, the core is said to be saturated; and the curve OACC' followed from total demagnetization into saturation is called the magnetization curve.

If after point C (or C') has been attained, the applied field is gradually removed, $\vec{M}$ tends to remain constant and the path C'CD is followed leaving a net magnetic flux density B_R in the core with zero applied field.

Now a negatively increasing mmf is applied, and the path DEGJ is followed. At point J the core is once again saturated, but the flux is in the opposite direction to what it was at point C. It

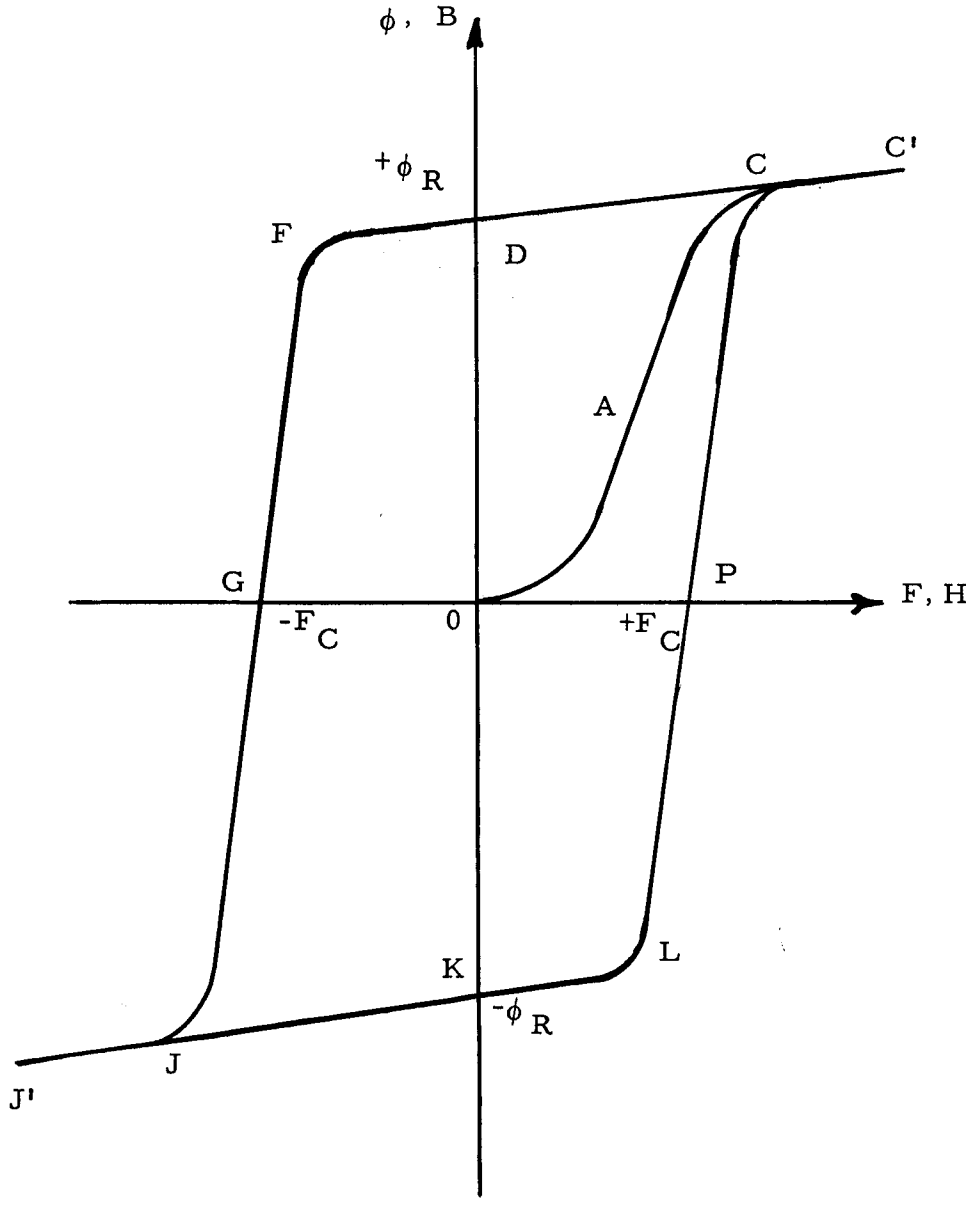


Fig. 2-6

Magnetization Curve and Major Hysteresis Loop

will be observed that the flux remains in the positive direction until point G is reached. The values of H and F corresponding to point G are called the coercive force and the coercive mmf respectively. Removal of the mmf after the core has been driven into negative saturation at point J', causes the path J'JK to be followed, and a residual flux density $-B_R$ remains.

In a similar fashion, path KLPCC'CD is followed with the application and removal of a slowly changing positive mmf which reaches an amplitude sufficient to drive the core into positive saturation.

The total path DFGJKLPCD is termed the major hysteresis loop or saturation loop of the core (or material), and it is clear that no flux densities may be produced in the core that do not lie inside the loop, on the loop, or on the extensions of the loop into hard saturation (curves CC' and JJ').

Referring to Fig. 2-7 it is again assumed that the core is demagnetized and a slowly changing mmf is applied which alternates in polarity in a cyclic fashion and reaches a maximum value F_M in both directions which is not great enough to drive the core into saturation. The core will follow the magnetization curve on the first quarter cycle to point A which corresponds to F_M and from that point on follows the hysteresis loop A $A_1A_2A_3A_4A_5$ which lies well

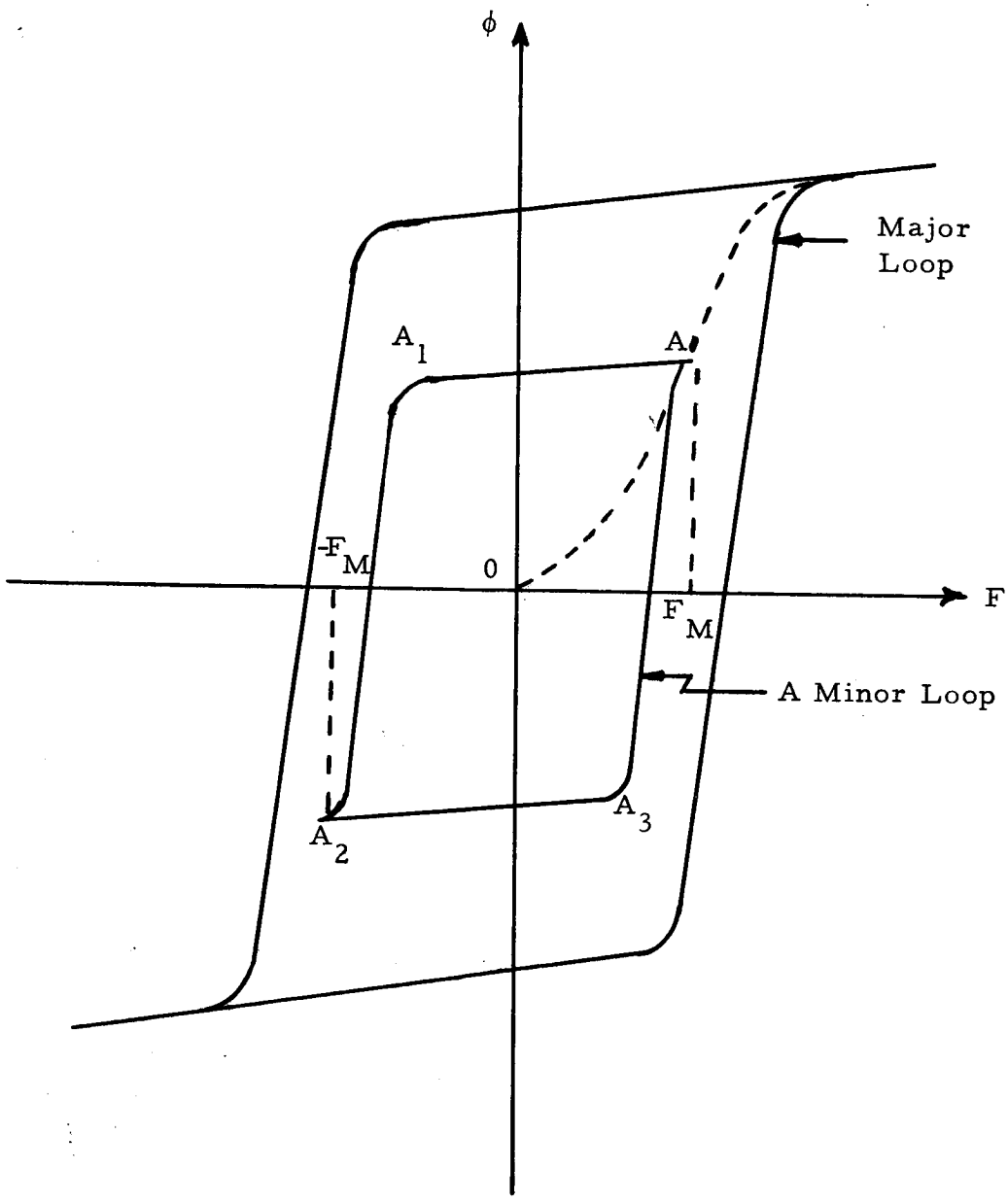


Fig. 2-7

Major and Minor Hysteresis Loops

inside the major hysteresis loop. Such a hysteresis loop is known as a minor hysteresis loop ; and for a given core, there is an infinite number of minor hysteresis loops, each corresponding to one of the infinite number of choices of F_M between zero and a value which first drives the core into saturation.

The hysteresis loops shown in Figs. 2-6 and 2-7 are reasonably square and may be used in certain digital applications. A similar hysteresis loop is shown in Fig. 2-8 with the following defining parameters shown: H_C, H_M, H_D, B_M, and B_R. H_C is the coercive force and it is the required value of H_{ave} to produce zero flux density on the loop. H_M is the maximum value of H_{ave} applied to the core to produce the hysteresis loop. B_M is the flux density when H_M occurs, and B_R is the remanent flux density when H is zero. H_D is termed the dc threshold magnetizing force and marks the first corner of the loop encountered as the core changes from one state to the other. Excitations of polarity that tend to cause the direction of flux to change and of magnitude less than H_D will cause only a very small and essentially reversible flux change; when these excitations are removed, the core returns very nearly to its previous state of remanance. Excitations greater than H_D will cause a large flux change that is not reversible when the applied field is

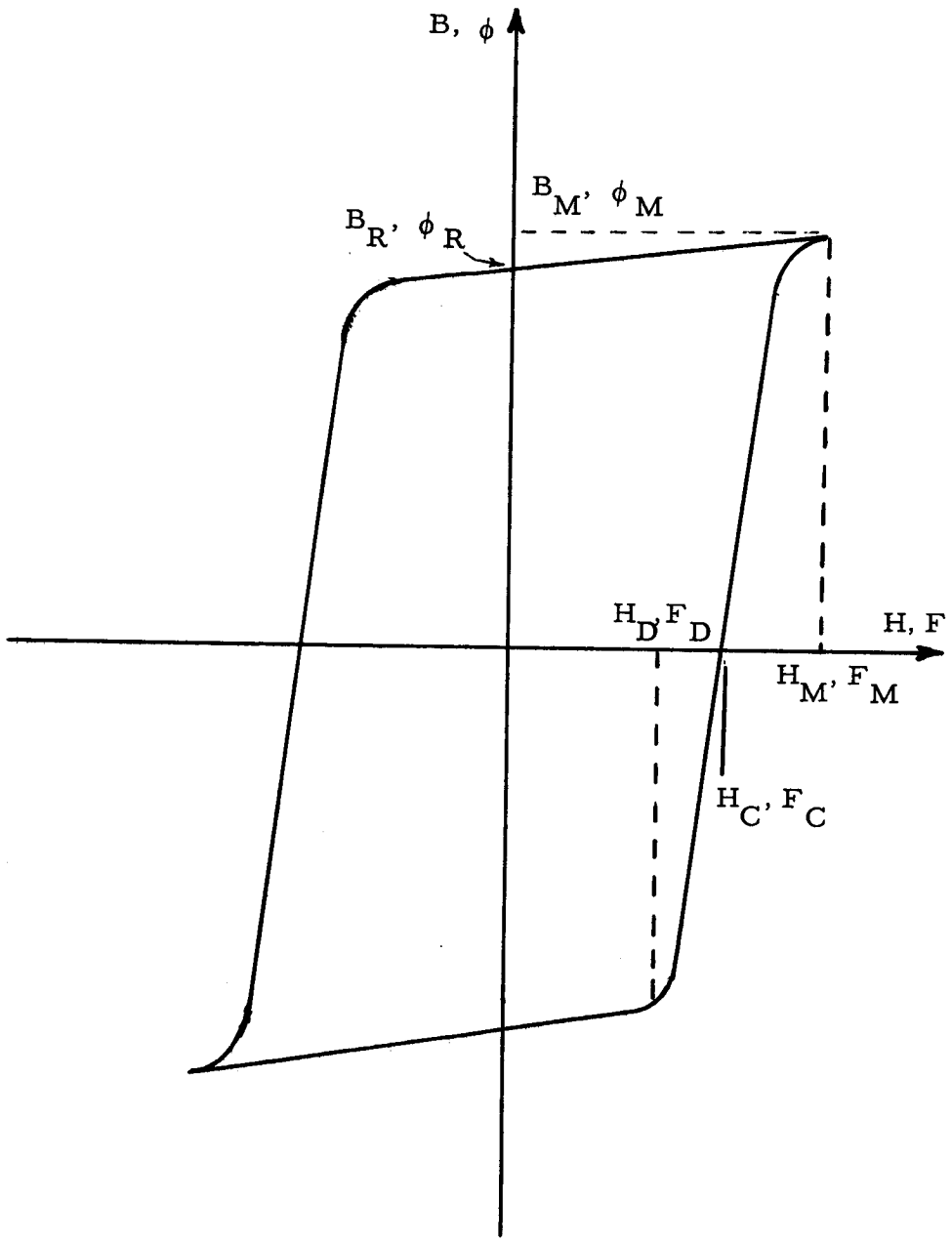


Fig. 2-8

Defining Parameters of a Nearly Square Hysteresis Loop

removed.

The above parameters may also be expressed in terms of F or I and ϕ if the hysteresis loop is for a particular core. Thus, F_C, the coercive mmf, is the value of mmf required to cause ϕ to change sign. F_M is the maximum mmf applied, and ϕ_M is the flux corresponding to F_M. ϕ_R is the remanent flux when F is zero. And F_D is the dc threshold mmf.

The degree of squareness of a hysteresis loop is commonly given by the squareness ratio S, the ratio of B_R to B_M, or equivalently ϕ_R to ϕ_M.

$$S = B_R/B_M = \phi_R/\phi_M \qquad (2.2.9)$$

S is a measure of the slope of the top and bottom of the hysteresis loop but not of the sides. The slope of the sides is partially a function of the material and partially a function of the geometrical configuration of the material. It is necessary that the cores used in a magnetic-core memory possess a high degree of squareness in their hysteresis loops. It has been found that a minor hysteresis loop is generally squarer than a major hysteresis loop, and early magnetic-core memories were designed to operate on a minor loop. Today, with improved manufacturing techniques, memory cores

possess sufficient squareness in their major hysteresis loops to allow operation on that loop or at least on a minor loop very near to the major loop.[9]

The discussion to this point has stressed slowly changing excitations, and a hysteresis loop found from a slowly changing mmf is called a static or a dc hysteresis loop. The flux in the core will follow the excitation along the dc loop so long as the excitation changes slowly. However, in the digital mode, excitations which approximate step changes in mmf are generally used. It has been found that if the excitation causes a core to change state, then a definite length of time is required for the large irreversible flux change to occur. Thus, the flux change occurs after the step change in mmf, and it is necessary to maintain the excitation at its new level long enough for the change to occur. The static loop may be referred to so long as this point is kept in mind.

A further point that the discussion has so far ignored is the temperature dependence of the characteristics of magnetic materials. With increasing temperature the remanent flux density and the coercive force of the hysteresis loop decrease. That is, the hysteresis loop shrinks with increasing temperature. When the temperature reaches what is known as the Curie temperature the

material loses all of its magnetic properties. At temperatures much lower than the Curie temperature the variation in characteristics with temperature is slight and essentially linear. The Curie temperature is a function of the material and manufacturing processes, and at the present it is possible to purchase ferrite memory cores (such as the Indiana General MC-183) which can be operated over wide-temperature extremes (50°C or more) without temperature compensating external circuitry.[10]

2.2.5 Induced Voltages - Faraday's and Lenz's Laws

In general a time varying magnetic field produces an electric field, and the two are related by Faraday's law. For the special case of a winding on a magnetic core in which the flux is changing with time at a rate $d\phi / dt$, Faraday's law states that a potential difference v is induced across the terminals whose amplitude is

$$|v| = N\left|\frac{d\phi}{dt}\right| \qquad (2.2.10)$$

where N is the number of times which the conductor of the winding passes through the core.

Lenz's law states that the polarity of v is such that it opposes the change in flux. That is, if v produces a current i, i is in a direction such that the magnetic field produced by it opposes

the changing field. This law is extended to develop the dot convention in the following section.

Thus, a change in ϕ (or B) in a magnetic core may be used to produce a voltage whose magnitude is proportional to the rate of change, and whose polarity is dependent on the direction of the change.

2.2.6 The Dot Convention

In all electrical engineering work the problem of relative polarities of voltages in mutually coupled coils is handled by the "dot convention" which is simply derived from Lenz's law. Because the present state of a square-loop core is generally detected by attempting to drive it to a specified state and observing whether or not the proper voltage is induced in a sense winding, the dot convention is an important tool in the design of magnetic-core memory.

Consider the core of Fig. 2-9 with two windings on it as shown. Winding 1 is driven by a source and winding 2 is connected to a passive load in series with a switch S. Dots have been placed by one of the two leads of each coil, and their interpretation is as follows. If a positively increasing current is caused to flow into the dotted terminal of winding 1, the voltage observed at either

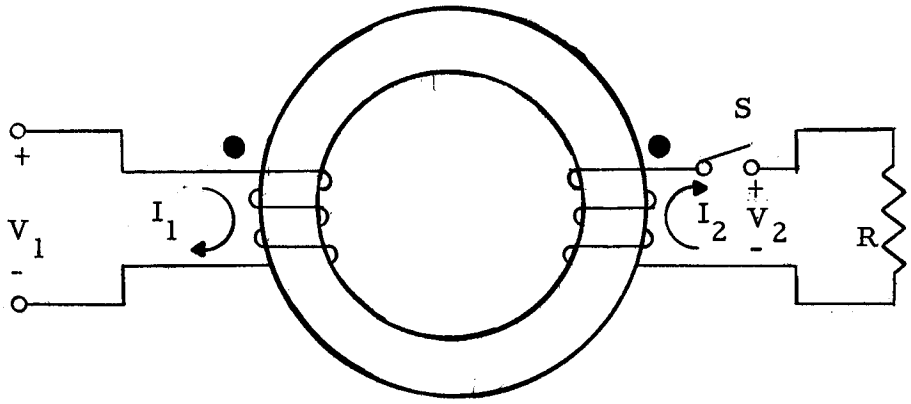


Fig. 2-9

Illustrating the Dot Convention

of the two winding will be positive at the dotted terminal with respect to the other terminal.

A procedure for locating the dots is now outlined.

1. Arbitrarily assume that a positively increasing current I_1 flows in winding 1; place a dot by the terminal in which this current enters, since the voltage must be such that it will tend to drive current in the opposite direction.

2. Assume that S is closed. The current in winding 1 produces a changing flux which induces the voltage in winding 2 so that current I_2 may flow in the passive load. The load current must oppose the changing flux, and therefore it must pass through the core in a direction opposite to that of I_1. Since winding 2 acts as a source to the load, place a dot by the terminal of winding 2 through which current exits.

2.2.7 mmf and Energy Relationships for a Square Loop Core with Several Windings

Assume that the core of Fig. 2-9 has an ideally square hysteresis loop, such as in Fig. 2-2, and is to be operated only on that hysteresis loop. With S closed, observe that the current i_2 in winding 2 will flow if and only if the core changes states, and that the direction of i_2 through the core is opposite to the direction of i_1

which causes the switching. Therefore, during switching the magnitude of the net current enclosed by the core is $N_1 i_1 - N_2 i_2$, and this must exceed F_O, the value of mmf corresponding to H_0 in Fig. 2-2.

Before writing this in equation form it will be convenient to define $F_0(\phi)_n$ as the required mmf to switch the core at time n. The absolute value of $F_0(\phi)_n$ is clearly F_0, and the sign is opposite to that of $(\phi_R)_{n-1}$, (the value of remanent flux at time n-1, just prior to switching). Thus, an expression for $F_0(\phi)_n$ is

$$F_0(\phi)_n = - \frac{(\phi_R)_{n-1}}{|(\phi_R)_{n-1}|} F_0 \qquad (2.2.11)$$

Defining the direction of positive i_1 and i_2 to be those shown in Fig. 2-8, and positive flux to be in the clockwise direction, the following relationship must be satisfied to switch the core

$$N_1 i_1 - N_2 i_2 \geq F_0(\phi)_n \qquad (2.2.12)$$

In general, a core will have several windings; some are driven by currents, and the rest are connected to loads. The driven windings are termed input windings, and those driving loads are called output windings.

In order to generalize (2.2.12) for a core with many windings, assume that the core has r input windings with turns N_1, N_2, . . . N_r, and S output windings, N_{r+1}, N_{r+2}, . . . , N_{r+s}. The current in each winding is i_1, . . . , i_r, i_{r+1}, . . . , i_{r+s} respectively. The positive direction of each input current (i_j, $j \leq r$) is such that it tends to drive the core to $+\phi_R$, and the positive direction of each output current (i_{r+j}, $j \leq s$) tends to drive the core to $-\phi_R$.

Properly summing the currents, as in the previous example, reveals that the condition

$$\sum_{j=1}^{r} N_j i_j - \sum_{j=1}^{s} N_{r+j} i_{r+j} \geq F_0(\phi)_n \qquad (2.2.13)$$

must be satisfied in order to switch the core. This is interpreted to say that in order to switch the core it is necessary to apply an mmf that will overcome the switching mmf of the core plus a back mmf that results from the core driving a load while switching. It is apparent that not all of the energy applied to the inputs is delivered to the outputs. In general energy is always required to produce a change in a magnetic field[1], and that this is true in this case is shown below.

First equation (2.2.13) is multiplied by $d\phi / dt$, and it is recognized that $N_k(d\phi / dt)$ is the voltage, v_k, induced across the kth winding. By Lenz's law each v_k will be of the same sign as the corresponding i_k. Thus,

$$\sum_{j=1}^{r} v_j i_j - \sum_{j=1}^{s} v_{r+j}\, i_{r+j} = F_0(\phi)_n \frac{d\phi}{dt} \qquad (2.2.14)$$

which is an instantaneous volt-ampere relationship, and the equal sign must be taken. Multiplying through by dt, integrating, and rearranging gives the energy relationship

$$\int_0^{T_S} \left(\sum_{j=1}^{r} v_j i_j \right) dt = \int_0^{T_S} \left(\sum_{j=1}^{r} v_{r+j} i_{r+j} \right) dt + \int_{(\phi_R)_{n-1}}^{(\phi_R)_{n+1}} F_0(\phi)_n \, d\phi \qquad (2.2.15)$$

where T_S is the time required for all of the flux to change, and $(\phi_R)_{n+1}$ is the new remanence flux at time n+1 just after switching. The integral on the left-hand side is the energy supplied to the input windings, and it is positive since v_j and i_j are of the same sign. The first integral on the right is the energy delivered to the loads on the output windings, and it too is positive. The last integral is the energy supplied to the core to produce the flux change. Since $F_0(\phi)_n$ is assumed to be constant and is of the same sign as

$(\phi_R)_{n+1} - (\phi_R)_{n-1}$, the last integral is also positive, and it is easily evaluated for the case at hand as $2\phi_R F_0$ which is one-half the area of the hysteresis loop. Notice that when the input currents are removed there is no more change in flux, and as a result all of the energy supplied to switch the core is lost in the form of heat.

The total area enclosed by the hysteresis loop represents the energy lost in every complete traversal of the loop. On ϕ-F coordinates the dimensions of the area are Webers-ampere turns which is the same as volt sec. ampere turn or the energy loss for a given core. But on B-H coordinates the area is (Webers/meter^2)· (ampere/meter) or energy per unit volume of the material. This lost energy tends to raise the temperature of the core; and therefore, change its magnetic characteristics. However, the effects of self heating in ferrite cores are normally minimal as is evidenced by the total lack of mention of the situation in such references as 2, 3, and 11 and in manufacturers' specifications for memory cores.

This analysis also shows that if the physical size of a core made of a given material is reduced, less energy is required for a complete traversal of the hysteresis loop. This implies that less energy would be required to store and retrieve a bit of data from

the smaller core.

It was mentioned in Section 2.1 that square-loop cores are normally operated under unloaded conditions or under heavily loaded conditions. The difference between the two situations is now elaborated upon in light of the results of this section. Consider a core with one input winding and one output winding with turns and currents as in Fig. 2-9. If the output is open circuited, S open, then i_2 is always zero, and all of the applied mmf provides the necessary energy to switch the core. The core will switch very rapidly and in a manner dictated by the applied current and the physics of the internal flux reversal mechanism. Now if a load is connected to the output with an impedance that is high enough so that the output mmf, $N_2 i_2$, is very small in comparison to $N_1 i_1$, virtually all of the input provides energy to switch the core; and the output voltage is the same as if it were open circuited. The output windings of memory cores are normally connected to a voltage sensing device which has a high enough input impedance so that the cores operate as if they were unloaded.

In the situation where the core is heavily loaded, the loud impedance is very small so that $N_2 i_2$ may be of the same order of magnitude as $N_1 i_1$, and F_0. Observe that if i_1 is a constant, if

$N_1 i_1$ is greater than F_0, and if the input is maintained long enough the core will switch. The output current depends upon both the rate-of-change of flux and the load impedance, which may be partly or entirely reactive, and the net mmf applied to the core depends in turn upon the difference between $N_1 i_1$ and $N_2 i_2$. The manner in which the flux change takes place is therefore highly dependent upon the load. For example, assume that the load is a resistance of a low value, and that a constant $N_1 i_1$ is applied. The net mmf applied to the core as it switches must be a constant, and the core must switch at a constant rate. To show this observe that if the rate of flux change increases, the output voltage increases, $N_2 i_2$ increases, the net mmf applied to the core decreases, energy is then applied to the core at a slower rate, and the rate of flux change must decrease. It can also be argued that if the output voltage starts to decrease, energy will be applied at a faster rate, and the core will start to switch faster. When the switching has been completed, the output goes to zero. The shape of the current output will be a pulse with constant amplitude. With a non-ideally square hysteresis characteristic the output would depart somewhat from this shape.

2.3 References for Chapter 2

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CHAPTER 3

MEMORY CORE LOGIC

AND THE LOGICAL STRUCTURE OF CORE MEMORIES

3.1 Performing Logical Functions with Square Loop Cores

This section will illustrate how logical connectives may be implemented using square loop cores by describing possible implementations of the functions AND, OR, and EXCLUSIVE OR for two variables using a single core with an ideally square hysteresis loop. Also, implementation of the function OR using one core per variable is described.

The single core for the first three cases is shown in Fig. 3-1; and it has one winding of one turn for each variable, labeled A and B and having currents I_A and I_B respectively for the Boolean variables A and B. Also it has one output winding which will be assumed to operate a voltage sensing device that has a high input impedance and draws negligible current. Finally it has a reset winding. The logical functions are performed by defining two input current pulse shapes (one to represent truth and the other falsity) for each of the functions A and B. The currents will be combined to switch the core in a specified manner when the function is true. Although the operations may be synchronized with a clock,

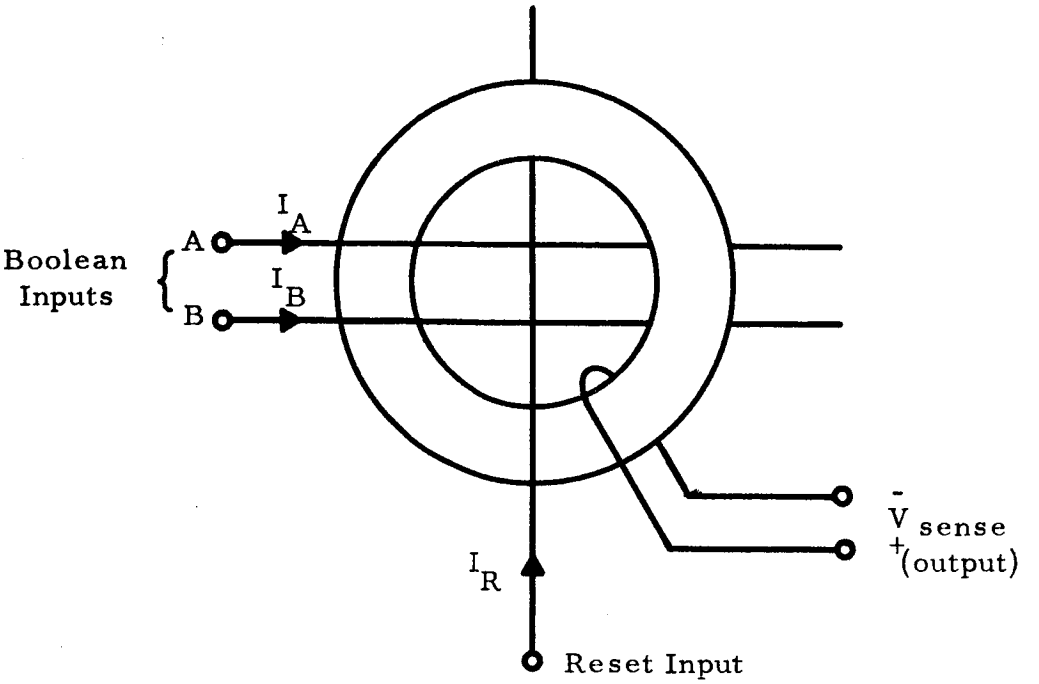


Fig. 3-1

Circuit For Demonstrating That
A Square Loop Core Can Perform Logical Functions

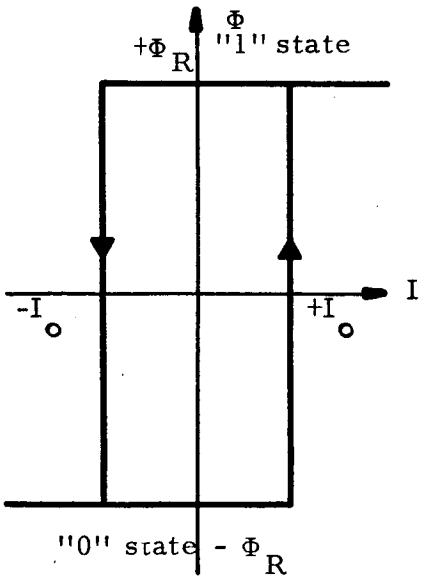


Fig. 3-2 Hysteresis Loop Assumed for the Core of Fig. 9

a continuous mode of operation is not available as it is with the transistorized forms of combinational logic elements. The reset winding is used to insure that the core will be in a specified state before each operation begins. Sections 3.1.1 through 3.1.3 describe the single core logic circuits.

The multiple core OR circuit, described in Section 3.1.4, is shown in Fig. 3-7, and the cores used are assumed to be of the same type as those used in the single core circuits.

Fig. 3-2 shows the hysteresis loop assumed for the cores on I-ϕ coordinates; and it is assumed that $+\phi_R$ will correspond to the "one" state.

To best illustrate the implementations, timing diagrams, showing all possible combinations of inputs with the resultant current through the core, I_E, are given in Figs. 3-3, 3-4, 3-5, 3-6, and 3-8.

3.1.1 Implementation of A and B

Recall that the logical function A and B (A B) is true only when both of the Boolean variables A and B are true. If the core is initially in the zero state, the logical input current pulses may be defined so that the core will be set at time n only when both inputs

are true at that time. This will be done in two ways, each of which is often used in practical memory systems.

Method 1: By Augmenting Currents

Both input currents I_A and I_B are defined in the same fashion; namely, if at time n

(1) the variable is false, then there is no current pulse.

(2) the variable is true then a pulse of amplitude $+(1/2)I_0$ occurs.

At time n+1 a pulse of amplitude $-I_0$ appears on the reset line which resets the core and readies it for the next input.

The core is set at time n only when both variables are true as shown in the timing diagram (Fig. 3-3) and a positive output voltage occurs only then indication the function to be true.

Method 2: By Inhibiting Currents

The logical input currents are not defined in the same manner. The input for the variable A at time n is

(1) no current pulse if A is false

(2) a pulse of $+I_0$ if A is true

And for the variable B

(1) a pulse of $-(1/2)I_0$ if B is false

(2) no pulse if B is true

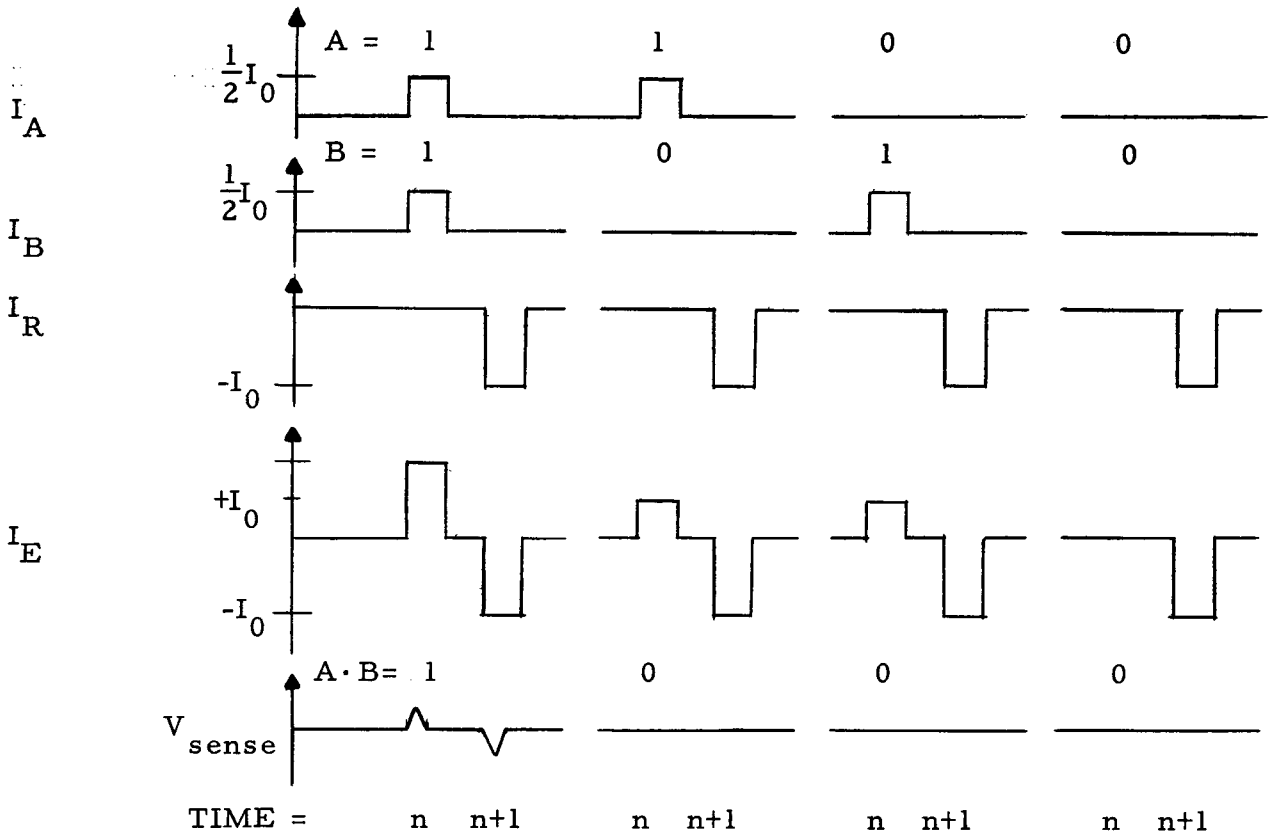


Fig. 3-3: Timing for Implementation of A·B by Augmenting Currents

The timing diagram of Fig. 3-4 shows that the core is set only at time n when both variables are true. Again a reset signal is always applied at time n+1 to ensure readiness for the next input.

3.1.2 Implementation of A or B

The function A or B (A + B) is true when either or both A and B are true. Logical input currents at time n are easily defined so that truth of either variable will set the core. In particular for either variable at time n

(1) there is no current if the variable is false.

(2) there is a current of $+I_0$ if the variable is true.

The timing is shown in Fig. 3-5.

3.1.3 A EXCLUSIVE OR B

The function A EXCLUSIVE OR B ($A \oplus B$) is true when A or B is true, and it is false when both A and B are true. That is, $A \oplus B$ is true only when A is not equal to B.

The implementation requires three steps at three discrete times, n, n+1, and n+2. At time n the operation A + B is performed as in Sect. 3.1.2 to set the core if either or both variables are true. At time n+1, $A \cdot B$ is performed in a manner similar to Method 1 of Sect. 3.1.1, which resets the core if both variables

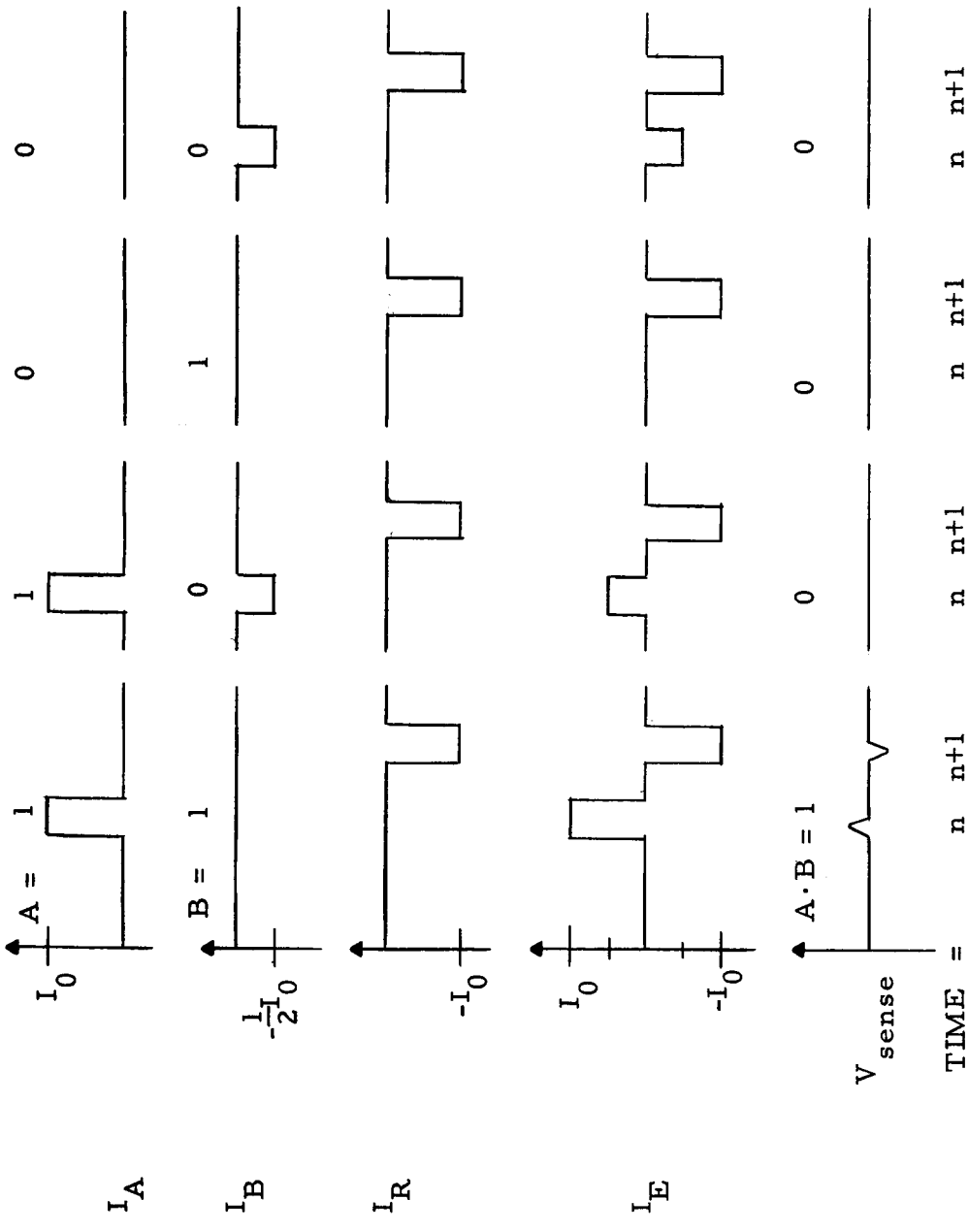


Fig. 3-4: Timing for Implementation of A·B by Inhibiting Currents

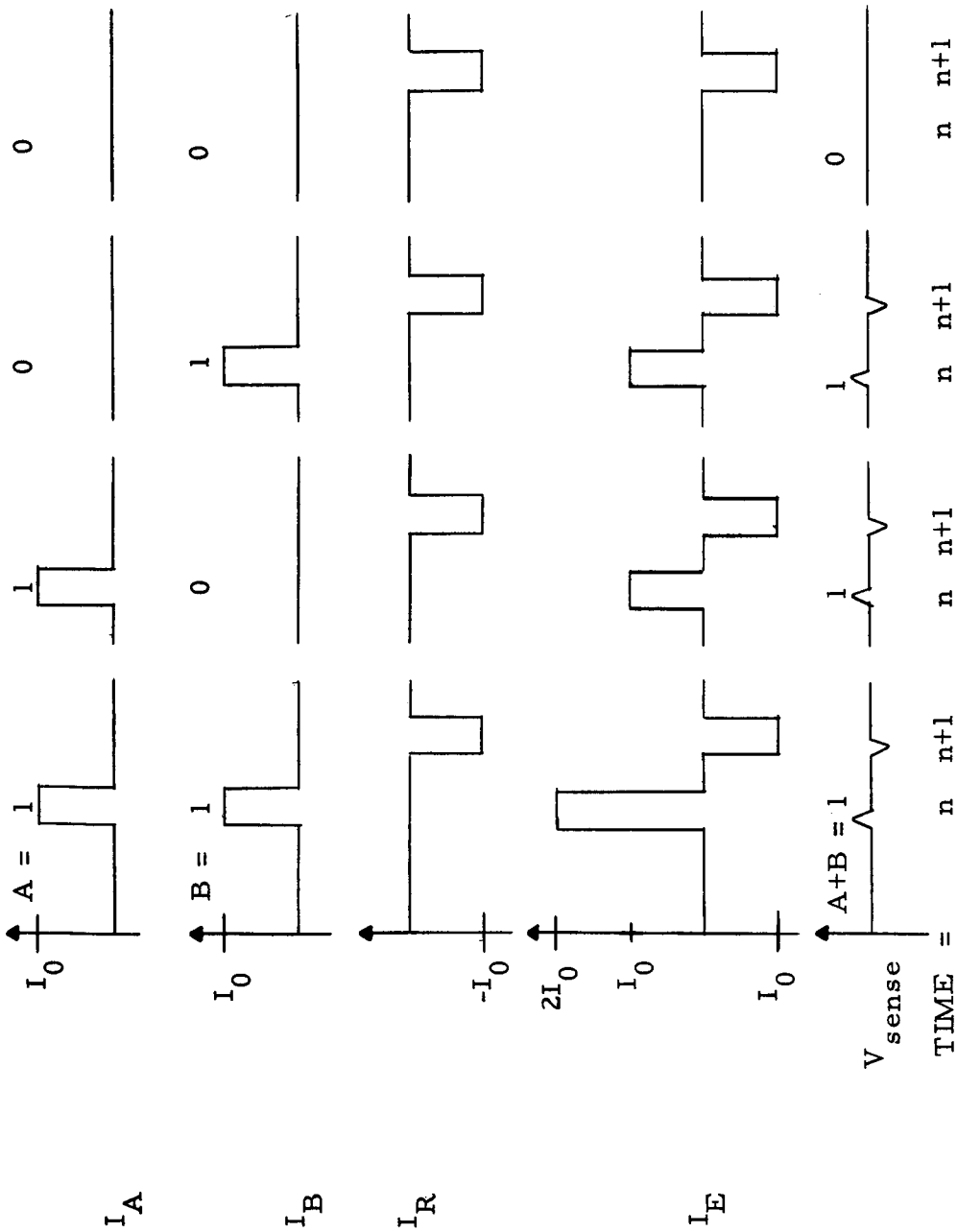


Fig. 3-5: Timing for A + B Implementation Using Circuit of Fig. 3-1

are true. Thus, at time n+2 the core will contain a one only if $A \oplus B$ is true, and accordingly at this time the core is reset giving an output voltage only if it contained a one.

Truth of a variable is therefore represented by a bipolar current pulse which has an amplitude of $+I_0$ at time n, and $-1/2\ I_0$ at time n+1. The absence of a pulse at times n and n+1 indicates that the variable is false. The reset pulse occurs at time n+2 and has an amplitude of $-I_0$.

This implementation requires that the voltage sensing device be strobed at the proper time, since reset outputs may occur at time n+1 or at time n+2. However, the previous circuits required that the output sensers be capable of sensing polarity only.

Because the functions A+B and $A \cdot B$ were formed while forming $A \oplus B$, all three outputs are available. In particular, as is shown in the timing diagram of Fig. 3-6, a positive voltage at time n shows that A+B is true, a negative voltage at time n+1 shows that $A \cdot B$ is true, and a negative voltage at time n+2 shows truth of $A \oplus B$.

3.1.4 Multiple Core OR Implementation

Fig. 3-7 is a method of ORing m Boolean variables,

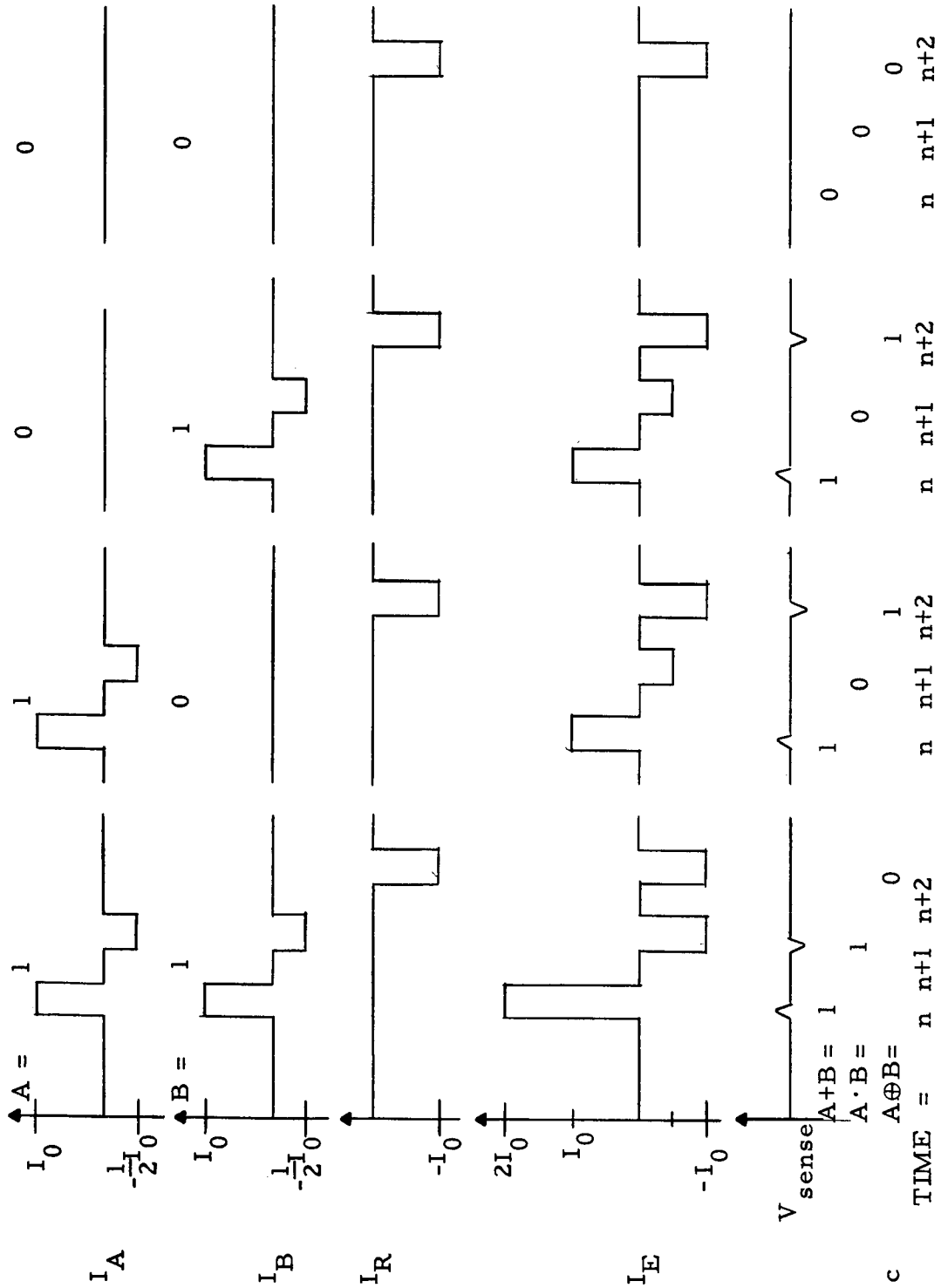


Fig. 3-6: Timing for A ⊕ B Realization

$X_1 + X_2 + X_3 + \ldots + X_m$, using m cores. Each variable is associated with one wire which threads one core. Threading all cores is a reset wire to initialize the system and a sense wire to detect outputs. Initially all of the cores are in the zero state, and at time n when the function is to be performed the currents on the m input wires are:

$$I_j = I_0 \text{ if } X_j \text{ is true.}$$

and $$I_j = 0 \text{ if } X_j \text{ is false.}$$

Thus, if any one or more of the inputs are true one or more of the cores will be set giving a positive output voltage. If all of the inputs are false, there will be no output signal.

At n+1 the reset current $I_R = -I_0$ is applied. A negative output voltage occurs if any of the cores were in the one state indicating that the function at time n was true. No output voltage occurs if the function was false. The peak value of the output voltage at time n or n+1 will be proportional to the number of cores switched, since it is the sum of all of the voltages produced by all of the cores.

A timing diagram for m = 2 inputs is shown in Fig. 3-8.

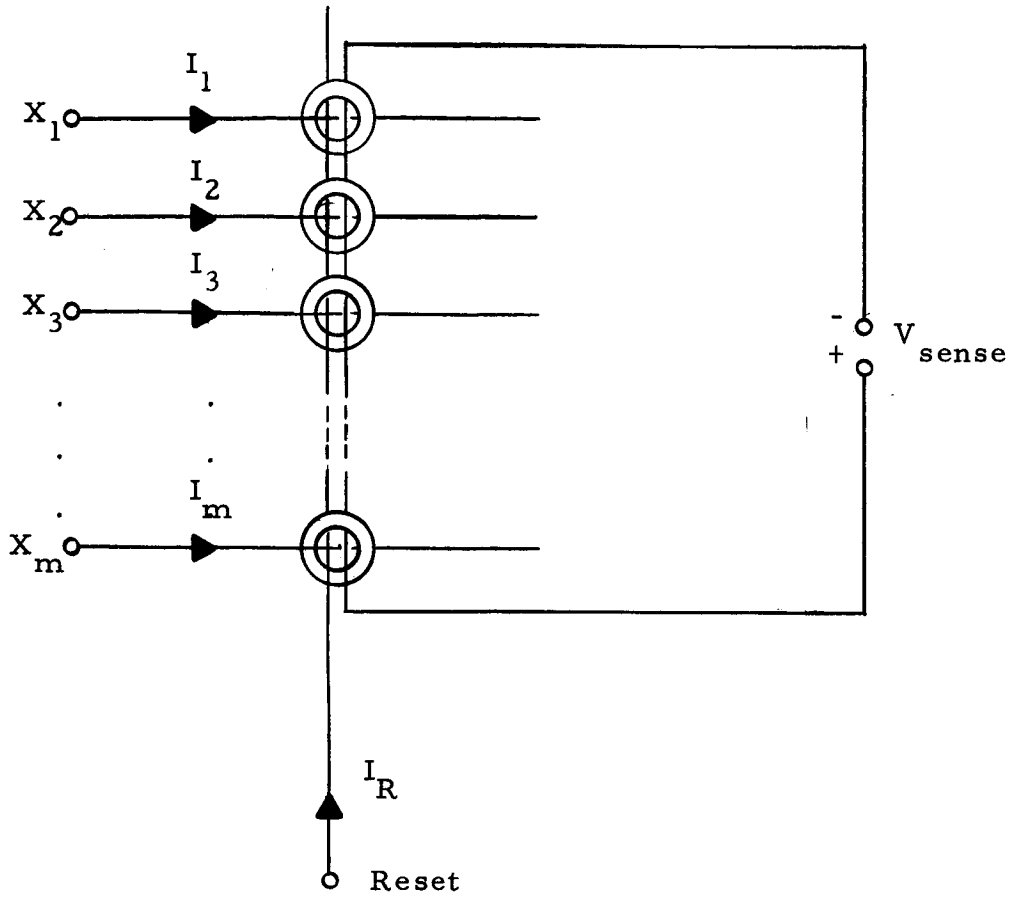


Fig. 3-7: Multiple-Core OR Implementation

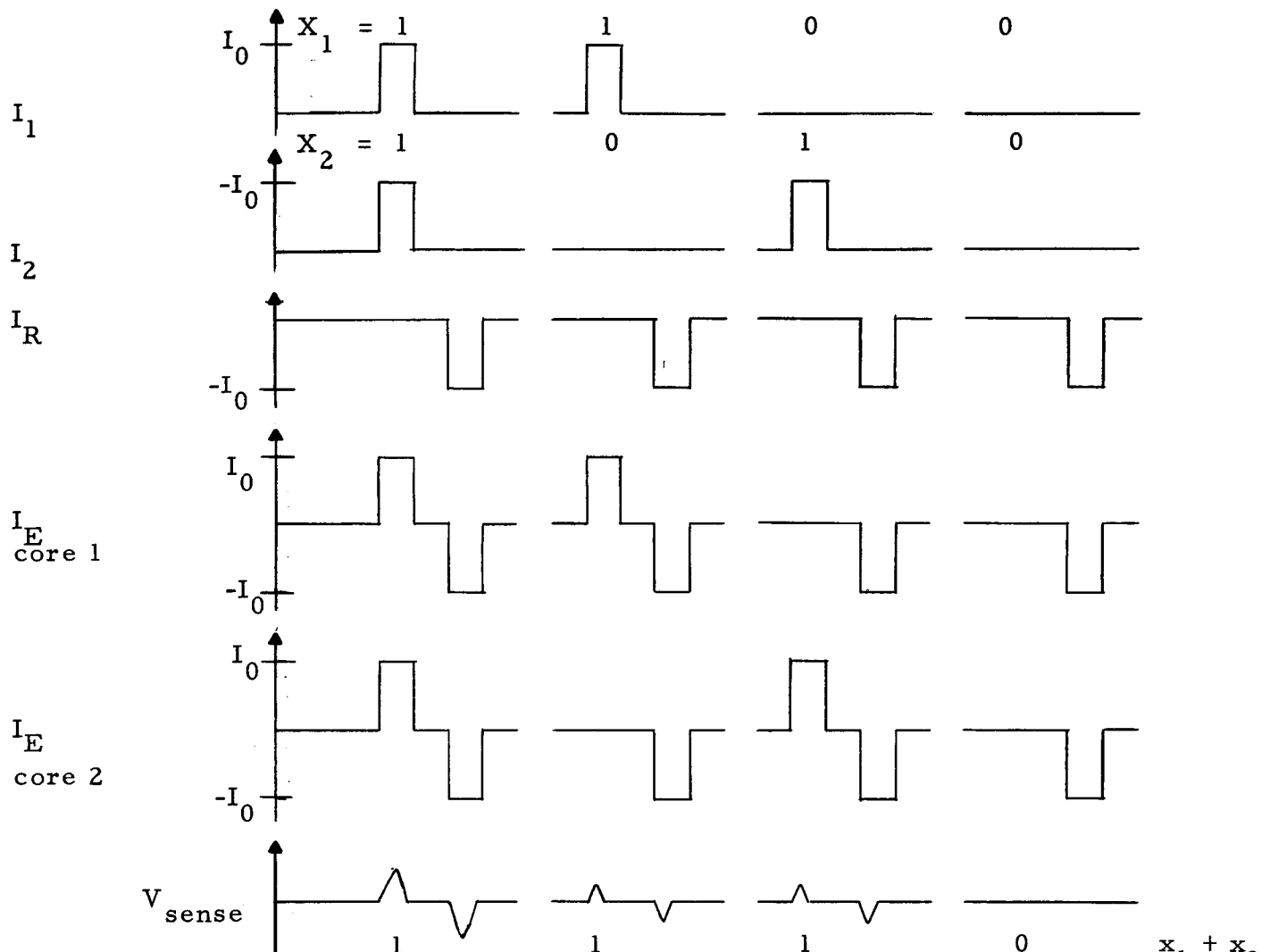


Fig. 3-8 Timing for 2-input, 2-core OR Circuit

3.2 Symbols and Notation for Schematically Showing Memory Arrays

As stated previously, a magnetic-core memory consists of many cores strung on wires in an orderly fashion. In general, a single wire will thread several cores and they will carry currents that perform the same functions for each core. The usual method of diagrammatically showing a two-dimensional memory array is to present a two-dimensional view of it with each core in its actual physical location and orientation by either of the schematic representations of Fig. 2-5 and with all wires shown as they actually thread each core. Three-dimensional arrays are usually made up of several identical two-dimensional arrays and may therefore be conveniently represented by two-dimensional drawings.

To show the function of each wire and thus indicate the operation of the memory, each wire may be labeled as to its function and/or arrows placed on it (if it is an input) to show positive direction of current flow. Each arrow may be identified to indicate the magnitude of the current it represents and the function it performs.

In the remainder of this work, all cores will normally be shown by either of the two schematic representations of Fig. 2-5.

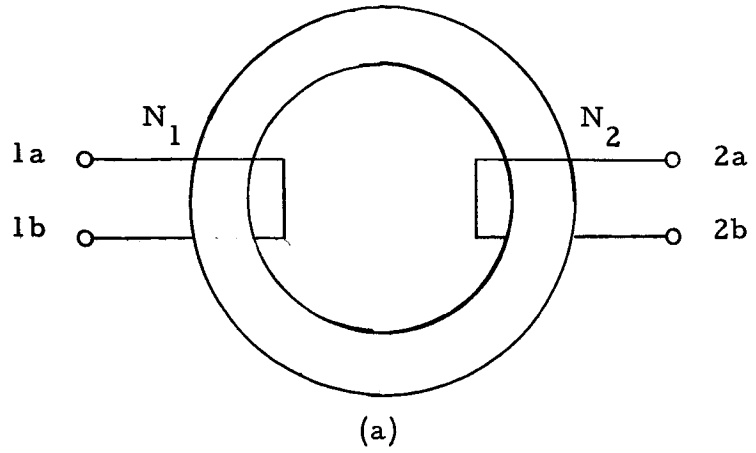
If the core is to have windings of more than one turn, they will be indicated by a single wire passing through the core in the direction of the first turn, and an integer will be placed next to the wire, near the place on the core where the turns are to be made, giving the number of turns. Absence of the integer will indicate that the wire passes through the core only once. Thus, the configuration of Fig. 2-3a might be shown schematically as in either Fig. 3-9a or Fig. 3-9b.

Furthermore, arrows may be placed on each input line to show the direction of current flow and each arrow will be identified by a symbol which will indicate the magnitude of the current as well as the function it performs. Fig. 3-10 shows the schematics for the examples of the preceding section. It is seen that each current arrow is identified by a symbol of the form

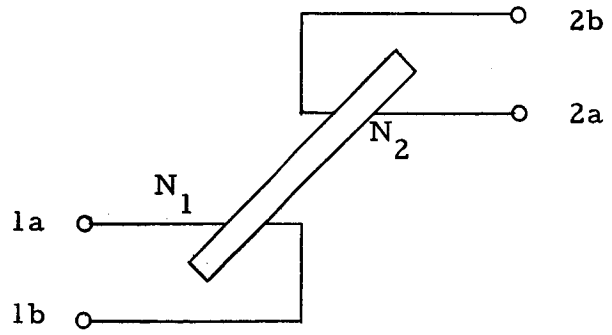
$$K\gamma_j^{\rho}$$

where: γ is either R or S; R if the current is in a direction which tends to reset the core, and S if the current tends to set the core.

K is the ratio of the amplitude of the current in the wire to the amplitude of the current required in that wire to just switch the core; that is, it is the threshold current (I_0 in Fig. 3-2) divided



(a)



(b)

Fig. 3-9: Schematics for Core of Fig. 2-3a.

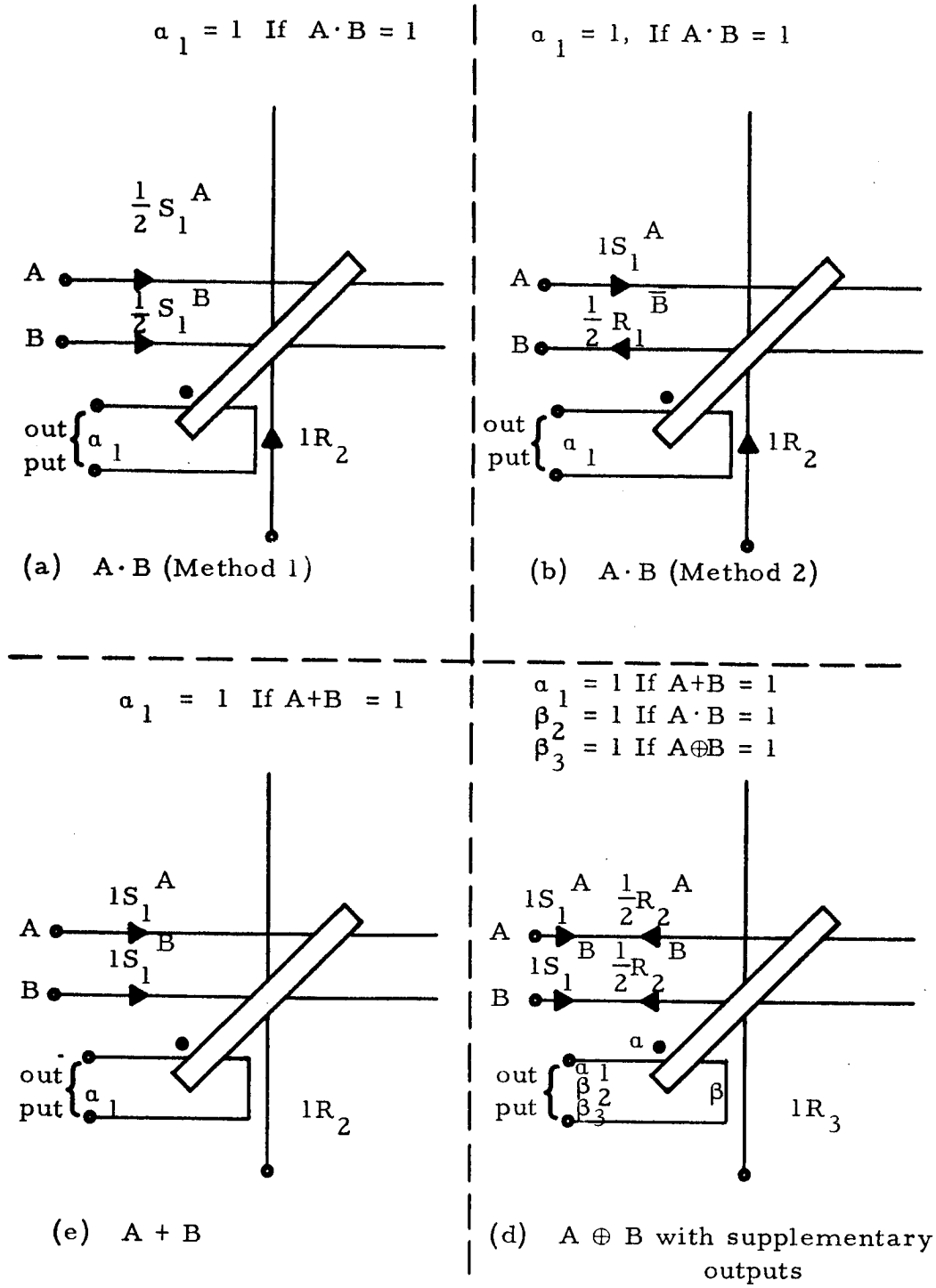


Fig. 3-10 Logic Diagrams for Examples in Section 3.1

by the number of turns N.

j is an integer giving the relative time at which the current pulse occurs.

ρ is used only when the current represents truth of a Boolean variable, in which case ρ is replaced by the asserted state of the variable, and the current is produced only when that state is true.

From the exclusive-or example of the preceding section (Fig.3-10 d) it will be noted that a given wire may carry different currents at different times. This situation is readily handled by placing an arrow on the wire for each current and properly identifying it.

If a wire is to be used for output purposes, it is labeled "sense". If a zero-to-one transition at time j is to be the output, it is labeled α_j; but if a one-to-zero output at time j is to be sensed, it is labeled β_j. The polarity of the output is determined by following the dot convention and indicated on the diagram by placing a dot next to the wire near the core and on that side of the core where the induced voltage is positive for the desired output. The dot will be on the same side of the core for all like transitions but on opposite sides for different transitions. If both α's and β's

are to be sensed, an α is placed where the dot would be for an α transition and a β on the other side.

Algebraically summing the K's together of all currents present at a given time gives the net current applied normalized with respect to I_0. All set currents may be taken as positive and all reset currents negative. If the summation, denoted by ΣK, is positive, the net current is in the set direction. In Fig. 3-8b, for example, ΣK is +1 if both A and B are true at time 1, -1/2 if both A and B are false, +1/2 if A is true and B is false, and 0 if A is false and B is true. At time 2, ΣK is always -1 in this case.

Another system of notation, the mirror notation[1], has been developed, and it is sometimes of advantage in magnetic-core logic circuitry where there are few cores with many windings of several turns on each. The advantage of the system just described is in situations where there are many cores with windings common to all. It not only allows one to show exactly how the cores are strung, but it indicates the function of each wire, the logic performed by the cores, and the timing of events.

In the remainder of this work, this system will be used to describe various memory configurations. Parts of the system which add nothing to the discussion at hand will be dropped.

3.3 Organization of Magnetic-Core Memories [2, 3]

3.3.1 General Form of a Magnetic-Core Memory

The function of a magnetic-core memory is to store j words of digital data, each word consisting of k bits. As a result, core memories generally consist of jk cores, each core storing one bit, arranged to form j storage registers of k cores each. Each such register has an address, and the address of the storage register to be written into or read out of at a given time is contained in an address register. Any particular storage register may be addressed at any given time, and the sequence in which several storage registers may be addressed can be completely random, dictated only by the logic system with which the memory operates. As a result magnetic-core memories fall into the category of random access memories.

Fig. 3-11 is a general block diagram of a random access magnetic-core memory. The address register must have j stable states, each corresponding to one of the j addresses. Decoding logic which has as its input the contents of the addressing register, selects the storage register corresponding to the present address. Its function is to provide logical addressing current pulses to all of the cores of the addressed storage register. The actual current

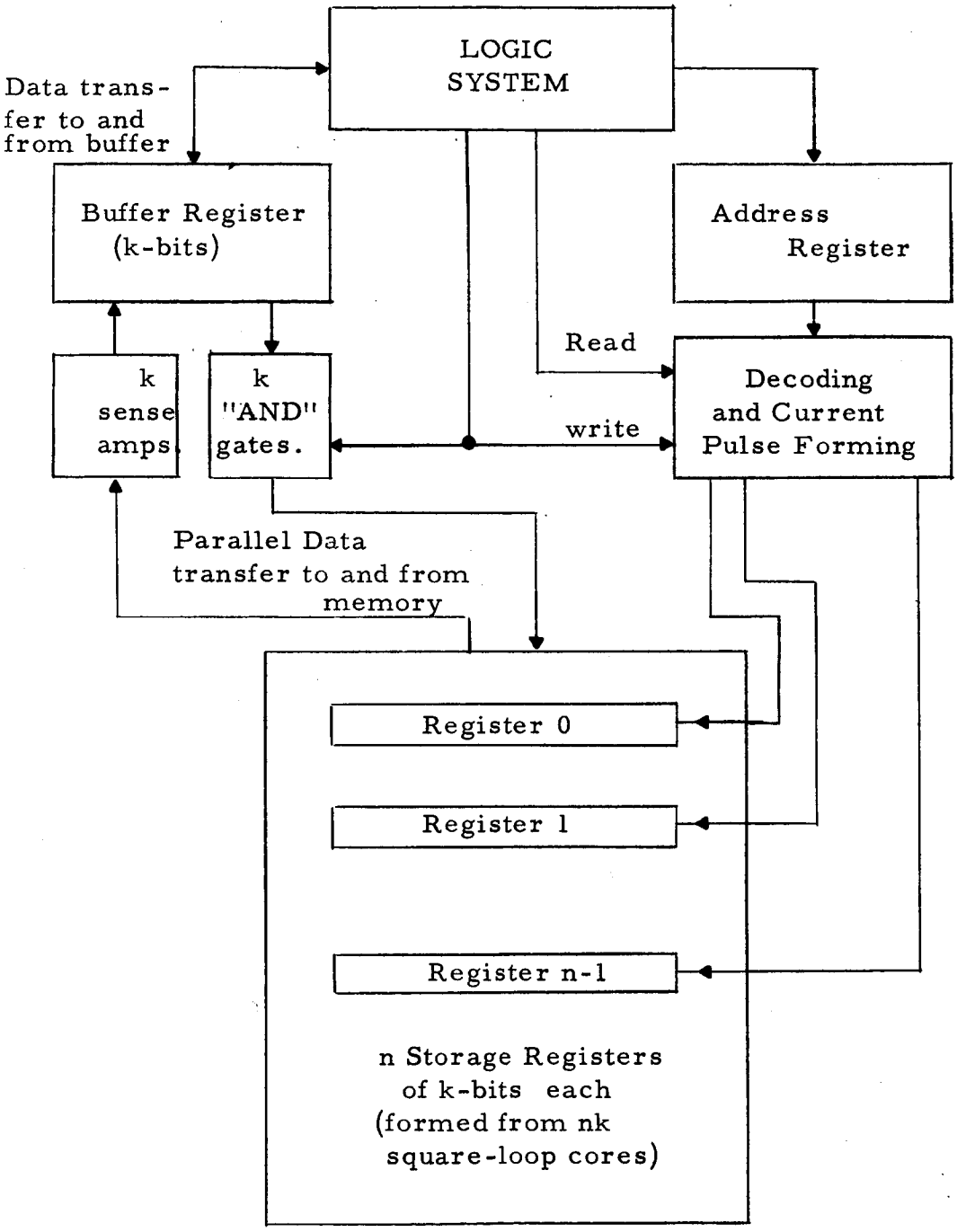


Fig. 3-11 General Block Diagram of Random Access Memory

pulses are formed somewhere in the decoding logic or external to it. For convenience the outputs of the decoding logic will be represented by the Boolean variables $A_0, A_1, \ldots, A_{r_1}, \ldots, A_{j-1}$ where A_r is true when the rth storage register is to be operated on. No two words may be operated on simultaneously so the logical requirement

$$A_r \cdot A_s \neq 1, \quad r \neq s \qquad (3.3.1)$$

is imposed. Each A_r is then considered to be ANDed in some fashion with a command to produce the proper current at the right place.

Data words are transferred between the logic system and the core memory in a parallel mode, one word at a time. That is, information transfer is serial by word and parallel by bit.

The word stored at a particular address is usually read from the memory into a buffer register, which is part of the external logic system and consists of k flip-flops, by means of the addressing currents which simultaneously reset each core of the addressed storage register. The buffer is initially cleared before each read operation, and each core of the storage register is coupled to its corresponding flip-flop in the buffer by a sense

winding which is the input to an amplifier. The amplifier determines whether a one-to-zero transition was made by the core by the presence or absence of the proper signal on the sense winding; and if such a transition was made, the amplifier produces an output which sets the flip-flop to the one state. Because only one word may be read at a time the outputs of all cores of the same bit position may be ORed together. Therefore, the sense winding may link all corresponding bits of the j storage registers, and therefore only k amplifiers are required.

In order to write a word at a given address, the word to be written is inserted into the buffer register, and each core at the selected address is either set or reset according to the state of the corresponding buffer flip-flop. Each bit of the word is brought into the memory array in the form of a current which is applied to every core in the array corresponding to that bit. This current must be of insufficient magnitude to switch a core, and it either augments or inhibits the switching of the addressed core. The wire on which it is carried is termed the information winding. If writing a word is to always follow reading a word at the same address, then all of the cores at the address are in the zero state prior to writing; and it is only necessary to set those cores where the corresponding flip-flop of the buffer contains a one. Because

the read process is destructive, it is frequently necessary to rewrite a word at the same address immediately after it has been read. For these reasons, a read operation always precedes a write operation in most core memories, and the combined operation is known as the read-write cycle. The time required to complete a read-write cycle at an address and to go on to the next address is known as the cycle time of the memory. Cycle times for present-day magnetic-core memories may be as short as 1 microsecond or less in length. The access time of the memory is the time from the initiation of the read-write cycle to the time when the stored information is present in the buffer register.

3.3.2 Logical Equations of a Core Memory

If the following definitions and assumptions are made, logical equations for a core memory may be written.

(1) The read operation at an address will occur at time n, and the write operation at the same address occurs at time n+1.

(2) There are two input commands

a. Rd = 1 when an addressed storage register is to be read.

b. W = 1 when a word is to be written at an address.

(3) The buffer contains

a. all zeros at time n

b. the word to be written at time n+1

(4) The states and names of the buffer flip-flops are B(1), B(2), . . . B(s) . . . B(k) respectively and B(s)=1 when flip-flop B(s) is in the one state.

(5) The names of the memory cores are

C(0, 1), C(0, 2) ... C(0, s) ... C(0, k)

C(1, 1), C(1, 2) ... C(1, s) ... C(1, k)

. . . .

. . . .

. . . .

C(r, 1), C(r, 2) ... C(r, s) ... C(r, k)

. . . .

. . . .

. . . .

C(j-1, 1), C(j-1, 2) ... C(j-1, s) ... C(j-1, k)

(6) The flip-flop B(s) corresponds to the core C(r:s) at the rth address.

(7) The symbols R_γ and S_γ represent the logical inputs reset and set respectively to any storage element γ.

(8) The symbols $\alpha(\gamma)$ and $\beta(\gamma)$ are the outputs of any storage element γ when it makes a zero-to-one transition or a one-to-zero transition respectively.

When the rth storage register is to be read, A_r is true; and all the cores in the register C(r:1) through C(r:k) must be reset. Each core that makes a one-to-zero transition must cause the corresponding buffer flip-flop to be set. Hence the following equations describe the read operation at time n

$$R_{C(r:1)} = R_{C(r:2)} = \cdots = R_{C(r:S)} = \cdots = R_{C(r:R)} = R_d \cdot A_r \qquad (3.3.2)$$

$$\begin{aligned} S_{B(1)} &= \beta_{C(0:1)} + \beta_{C(1:1)} + \beta_{C(2:1)} + \cdots + \beta_{C(j-1:1)} \\ &\vdots \\ S_{B(S)} &= \beta_{C(0:S)} + \beta_{C(1:S)} + \cdots + \beta_{C(j-1:S)} \\ &\vdots \\ S_{B(k)} &= \beta_{C(0:K)} + \beta_{C(1:k)} + \cdots + \beta_{C(j-1:k)} \end{aligned} \qquad (3.3.3)$$

And for writing at time n+1 at the rth address it is recalled that each core of the storage register is set if the corresponding buffer stage contains a one. Hence

$$\begin{aligned} S_{C(r:1)} &= W \cdot A_r \cdot B(1) \\ &\vdots \\ S_{C(r:S)} &= W \cdot A_r \cdot B(S) \\ &\vdots \\ S_{C(r:k)} &= W \cdot A_r \cdot B(k) \end{aligned} \qquad (3.3.4)$$

3.3.3 The Linear Selection Memory (LSM)

A conceptually simple implementation of the equations for a core-memory is shown in Fig. 3-12. The cores are arranged in a rectangular j by k array. The cores in each of the j rows constitute a storage register, and the cores in each column are corresponding bit positions of each word. The parenthesized integers in the name of each core locate its position in the array by the conventional notation that locates the elements in any matrix. Thus, C(r:s) is in the rth row and the sth column. Inputs to the cores are carried on j+k wires, one wire threading the cores of one row or one column. Outputs are produced on k wires, each threading one column.

Equation (3.3.2) is implemented by providing an input to each row such that when a given row is to be read it will reset all of the cores in the row. Equation (3.3.3) is simply handled by amplifying the voltage on each output wires, and determining whether a β_C is present. If a β_C is present, the amplifier produces an output pulse which will set the corresponding buffer flip-flop.

Equation (3.3.4) is implemented breaking it up as follows:

$$S_{C(r:s)} = [\ W \cdot A_r\ ] \cdot [\ W \cdot B(s)] \qquad (3.3.5)$$

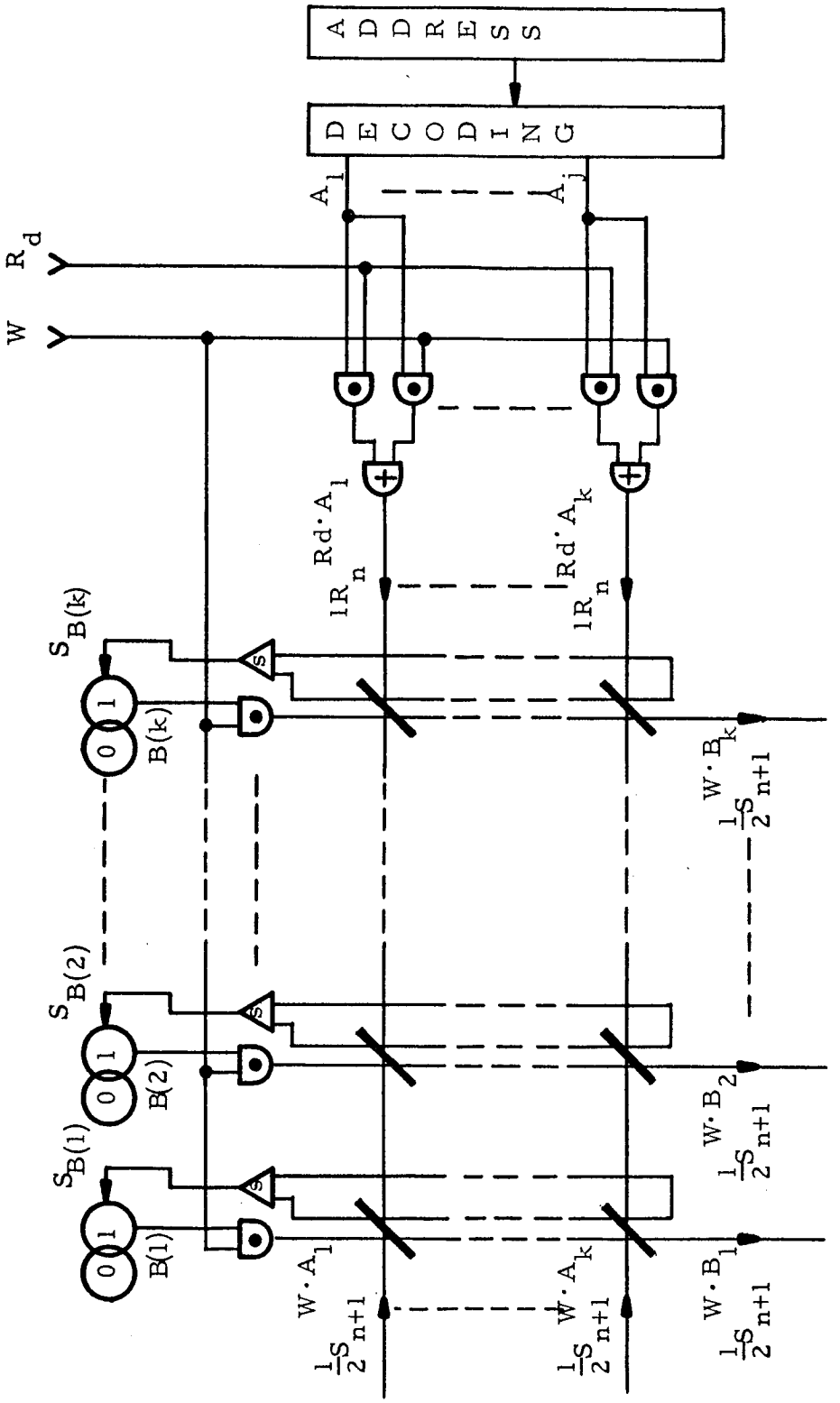


Fig. 3-12 A Linear Select Memory of j Words containing k bits each.

The bracketed quantities are formed external to the core array, but each core ANDs the two together to determine whether or not it has a set input. Either of the two methods of Section 3.1.1 might be used. Arbitrarily the first method is chosen, and currents of half the necessary amount required for setting a core are produced on each information wire (the column input wire) where $W \cdot B(s)$ is true and on the one row input wire where $W \cdot A_r$ is true.

Thus, there are two opposing current arrows on each horizontal wire designated by $1\ R_n^{A_r \cdot R_d}$ and $1/2\ S_{n+1}^{A_r \cdot W}$; and there is one arrow on each vertical input wire designated by $1/2\ S_{n+1}^{W \cdot B(s)}$.

The gates shown are to indicate logical structure only, and they must not be interpreted to be the usual diode gates. The AND gates produce the proper current pulse when the input conditions are met, and the OR gates shown allow undistorted passage of current pulses from either or both inputs, and serve to isolate their inputs from each other. In many applications, the OR gates do not exist at all or are simple solder junctions.

It has been implied and it is now pointed out that after time n new information may be placed into the buffer to be written into the memory at time n+1. Whether the old information is to be

rewritten or new information is to be written is determined by control logic external to the memory and is not of interest here.

The memory just described is characterized by the fact that all of the decoding is done external to the memory array. Memories possessing this characteristic are known as linear-selection , word organized, or word access memories. In future chapters memories of this form will be referred to as linear-selection memories and abbreviated as LSM's. The following section describes the historically older coincident-current memory in which the memory cores participate in the decoding and thereby reduce the decoding logic required.

3.3.4 The Coincident-Current Memory

In a coincident current memory (abbreviated CCM), the memory cores are allowed to participate in the implementation of Equations (3.3.2) and (3.3.4). The ideas involved are best illustrated by considering the simple example of a 16 word memory. Assume that each of the 16 words is k bits long and that the addresses are coded in the natural binary numbers 0000 through 1111. The address register then consists of four flip-flops, Q_1, Q_2, Q_3, and Q_4. Table 3-1 shows the 16 possible states of the address register and the corresponding output of the decoding

Table 3-1: Decoding Logic Output As a Function of Address Register Contents

State of Address Register Flip Flops				True Output Of Decoding Logic
Q_1	Q_2	Q_3	Q_4	
0	0	0	0	A_0
0	0	0	1	A_1
0	0	1	0	A_2
0	0	1	1	A_3
0	1	0	0	A_4
0	1	0	1	A_5
0	1	1	0	A_6
0	1	1	1	A_7
1	0	0	0	A_8
1	0	0	1	A_9
1	0	1	0	A_{10}
1	0	1	1	A_{11}
1	1	0	0	A_{12}
1	1	0	1	A_{13}
1	1	1	0	A_{14}
1	1	1	1	A_{15}

logic. It is seen that the general term A_r is the rth minterm (minterms are discussed in detail in References 4 and 5) of the four input variables (the states of Q_1 through Q_4) contained in the address register.

To perform all of the gating external to the memory array requires 16 AND gates with each having four inputs. This amount of gating may be substantially reduced if each memory core at an address is allowed to AND two functions. In particular the eight functions

$$\begin{aligned} X_0 &= \bar{Q}_1 \cdot \bar{Q}_2 \\ X_1 &= \bar{Q}_1 \cdot Q_2 \\ X_2 &= Q_1 \cdot \bar{Q}_2 \\ X_3 &= Q_1 \cdot Q_2 \\ \\ Y_0 &= \bar{Q}_3 \cdot \bar{Q}_4 \\ Y_1 &= \bar{Q}_3 \cdot Q_4 \\ Y_2 &= Q_3 \cdot \bar{Q}_4 \\ Y_3 &= Q_3 \cdot Q_4 \end{aligned} \qquad (3.3.6)$$

are formed external to the core array, requiring only eight AND gates with two inputs each. Each A_r is a product of a unique pair of these variables. The particular pair is readily found by writing r as a number to the base four.

$$r = a_1 \times 4 + a_0 \qquad (3.3.7)$$

where a_1 and a_0 take on integer values from zero to three. Then it follows that

$$A_r = Y_{a_1} \cdot X_{a_0} \tag{3.3.8}$$

Substituting into Equations (3.3.2) and (3.3.4) results in

$$R_{C(r:1)} = \cdots = R_{C(r:s)} = \cdots R_{C(r:k)} = R_d \cdot Y_{a_1} \cdot X_{a_0} \tag{3.3.9}$$

and

$$\begin{aligned} S_{C(r:1)} &= W \cdot Y_{a_1} \cdot X_{a_0} \cdot B(1) \\ &\vdots \\ S_{C(r:s)} &= W \cdot Y_{a_1} \cdot X_{a_0} \cdot B(S) \\ &\vdots \\ S_{C(r:k)} &= W \cdot Y_{a_1} \cdot X_{a_0} \cdot B(k) \end{aligned} \tag{3.3.10}$$

In implementing these equations, the cores are so wired that each core will perform the function $Y_{a_1} \cdot X_{a_0}$. This is done by arranging the cores in a 4 x 4 x k, three-dimensional array; that is, the cores are arranged to form a 4 x 4 array of k-bit storage registers as shown in the three-dimensional block diagram of Fig. 3-13 where each small cube represents the location of a core.

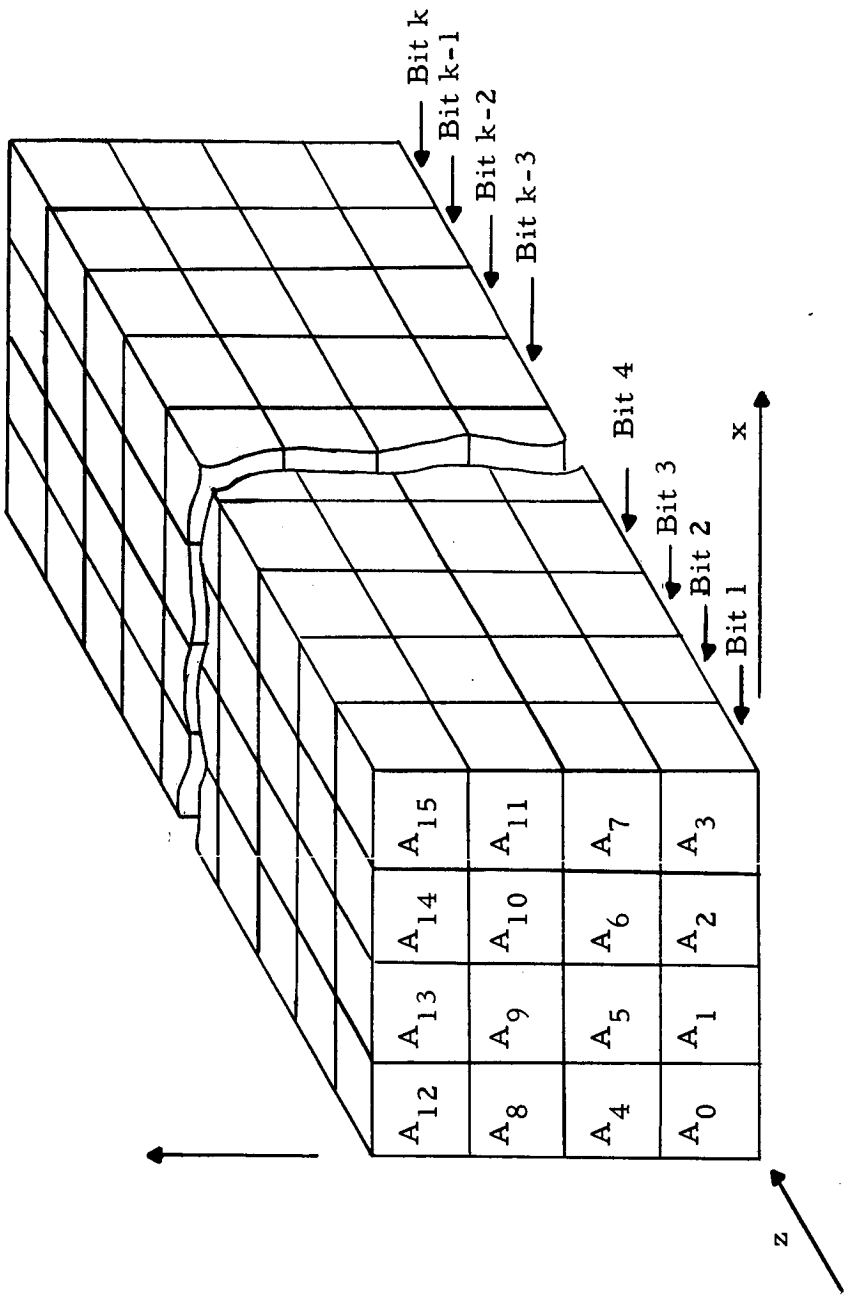


Fig. 3-13 Data Storage in Three Dimensions

The k planes parallel to the xy plane contain the 16 cores of the 16 words having the same bit position, and all k cores having the same xy coordinates constitute one storage register. The address of each register is then expressible in terms of its coordinates, and the addresses may be arranged and/or defined so that if r is expressed as in (3.3.7) a_1 will give the y coordinate and a_0 the x coordinate. Selecting a particular register is then accomplished by applying Y_{a_1} to each register where $y = a_1$ and X_{a_0} to each where $x = a_0$. Only the register at (a_0, a_1) will receive Y_{a_1} and X_{a_0}.

In each bit plane four wires in the y direction thread the cores at each x coordinate, and four wires in the x direction thread the cores at each y coordinate. The eight wires are continued so that they thread the cores of all bit planes at the same respective coordinate in each bit plane as shown in Fig. 3-14. These wires will carry currents such that the cores perform $R_d \cdot Y_{a_1} \cdot X_{a_0}$ (by augmenting currents) when register $Ya_1 + a_0$ is to be read, and $W \cdot Y_{a_1} \cdot X_{a_0}$ when the same register is to be written into. Thus at time n the wires in the x direction have the current $1/2\ R_n^{Y_{a_1} \cdot R_d}$, and those in the y direction have $1/2\ R_n^{X_{a_0} \cdot R_d}$. Only those cores in the addressed register receive the coincidence of the two currents and become reset. Equation (3.3.9) has now been implemented.

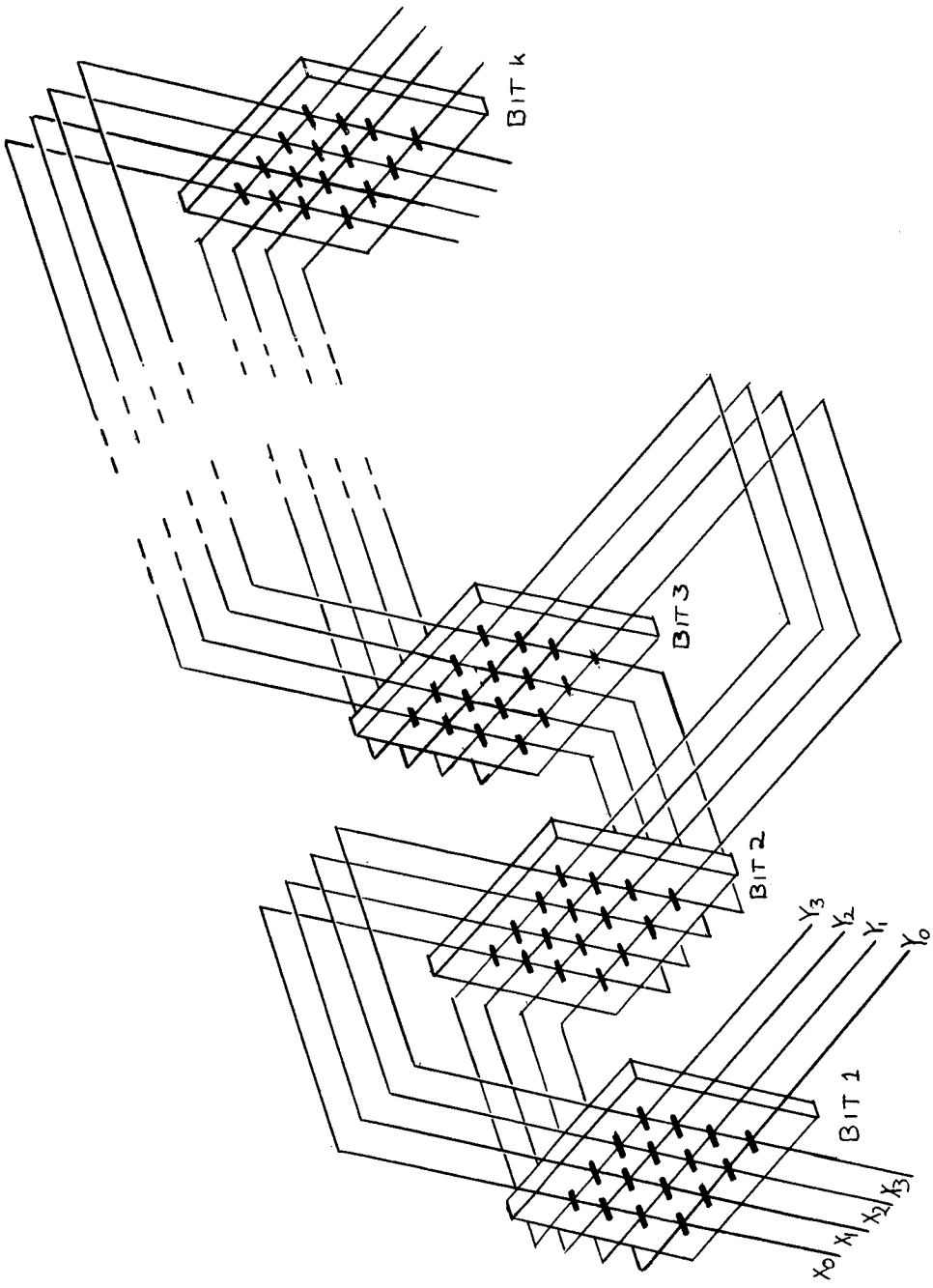


Fig. 3-14 Method of Interconnecting Bit Planes

To implement Equation (3.3.10) the inputs on the wires in the x direction is $1/2\ S_{n+1}^{Y_{a_1} \cdot W}$, and on those in the y direction the current is $1/2\ S_{n+1}^{X_{a_0} \cdot W}$. This takes care of the factor $Y_{a_1} \cdot X_{a_0} \cdot W$ in (3.3.10), but it must be ANDed with $B(s) \cdot W$. This is done in a manner similar to that of the second method described in Section 3.3.1. An information winding, commonly called the inhibit winding, is passed through every core in the sth bit plane in the same relative direction. If a zero is to be written, the wire carries a current which opposes the addressing currents and prevents the addressed core from being set. If a one is to be written, no current is applied to the inhibit winding, and the addressed core is therefore set. The amplitude of the inhibit current must be such that it effects only the addressed core, and it therefore must be $1/2\ S_{n+1}^{\overline{B(s)} \cdot W}$.

Finally, to satisfy Equation (3.3.3), a sense winding is placed in each bit plane, linking all the cores, and coupled to a sense amplifier whose output sets the corresponding buffer flip-flop whenever a $\beta_{C(r:s)}$ is detected. Fig. 3-15 shows schematically the sth bit plane complete with sense and inhibit windings, and a block diagram of the entire memory is shown in Figure 3-16.

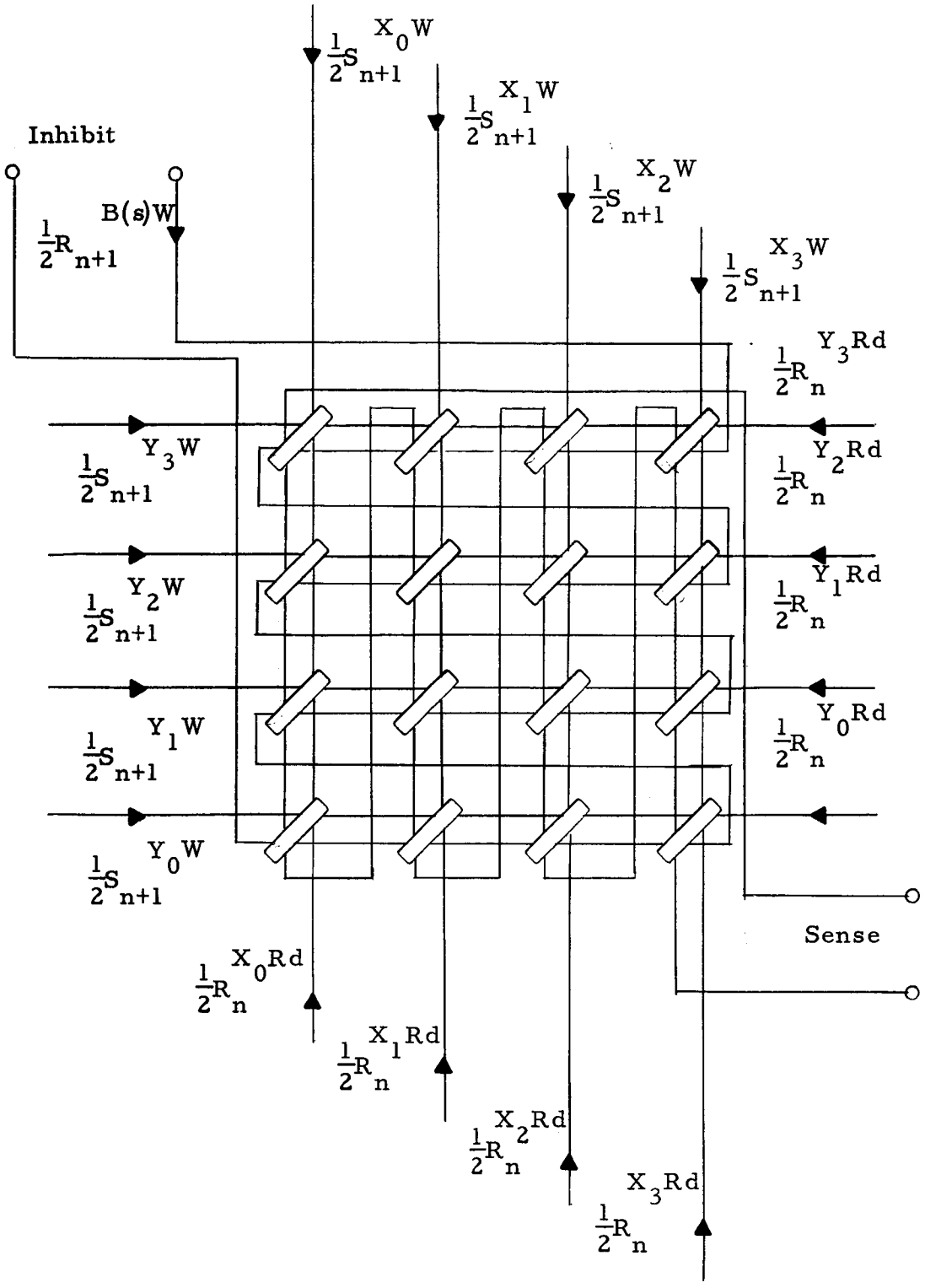


Fig. 3-15 Logical Representation of sth Bit Plane.

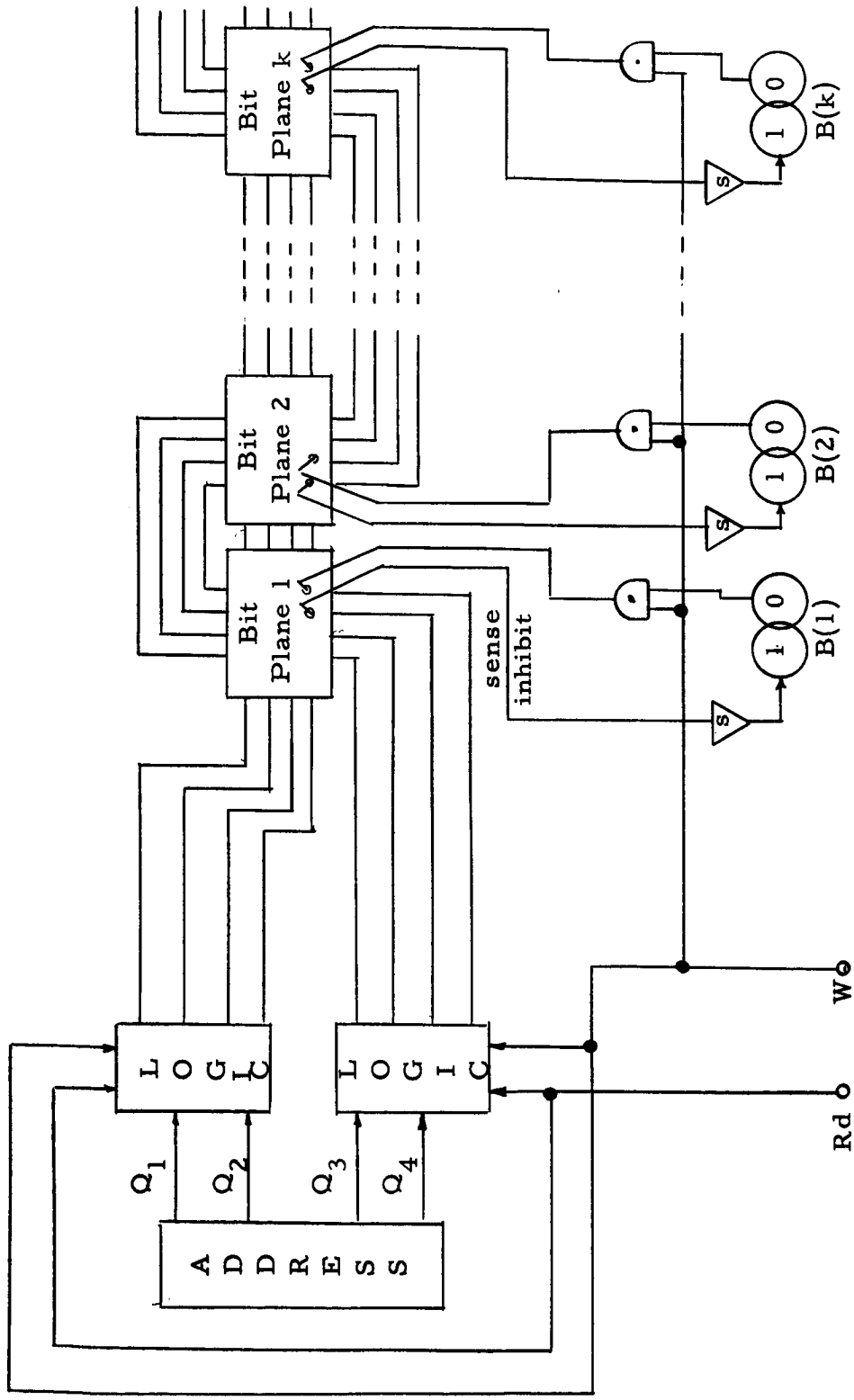


Fig. 3-16 Block Diagram of the 16 word Coincident-Current Memory

In general the CCM is characterized by storage in three dimensions and the use of coincident current pulses in addressing. A CCM for storing n words of k bits each has k bit planes of dimensions ℓ by m cores, where $\ell \cdot m = n$, wired together in a manner similar to that of Fig. 3-14. Each bit plane has sense and inhibit windings similar in function to Fig. 3-15, but, as discussed in Chapter 5, the actual wiring of bit planes is somewhat different from that shown. The addressing logic is designed to produce outputs which are combined in pairs inside the memory array to form each A_r in a unique fashion; this requires two distinct blocks of combinational logic, one having ℓ outputs to select the coordinate in one dimension and the other block having m outputs to select the other coordinate. The LSM, on the other hand, has one block of decoding logic with n outputs.

Although it appears possible to simplify the decoding logic still more by providing addressing currents in three or more dimensions, no practical memories have been built in which this has been done. The accepted form of the CCM is logically the same as that described here.

3.4 References for Chapter 3

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CHAPTER 4

PRACTICAL MEMORY CORES

4.1 Effects of Non-ideally Square Hysteresis Loops

The discussion of Chapter 3 concerning the core as a logic and memory element assumed that the cores in question possessed perfectly square hysteresis loops. In practical applications such a characteristic is not obtainable, although it is possible to purchase cores with a high degree of squareness in their major hysteresis loops. There are essentially three adverse effects that result from not having perfect squareness for operation in the digital mode.

1. The threshold for switching becomes a region of excitation rather than a single value of excitation.
2. Stored data tends to be destroyed when the core is excited by mmf's of magnitudes less than or equal to the d.c. threshold mmf, F_D.
3. The core will produce a small output voltage when it is excited but not switched. This voltage contributes significantly to system noise.

4.1.1 The Threshold Region

It is observed in Fig. 4-1 that the sides of the hysteresis loop are nearly vertical, but they do have a finite slope (which is due in part to the finite thickness of the core wall[1]). The corners of the loop are at $\pm F_D$ and $\pm F_M$. Excitations with a polarity that will tend to switch the core and with an amplitude F that is in the region $|F_D| < |F| < |F_M|$ will produce relatively large, irreversible flux changes, and the remanent flux after the removal of F will be well inside the loop. For example, if a core is at $-\phi_R$ in Fig. 4-1 and a positive F approximately equal to $+F_C$ is applied and removed, the remanent flux would be close to zero as indicated in the figure by path ABCD.

For reliable memory operation, it is necessary to use a core which has a hysteresis loop on which an applied F_M will definitely switch the core, but an excitation of $1/2\ F_M$ must be less than or equal to F_D. Specifications for memory cores normally include the ratio I_D/I_M for a given value of I_M (I_M and I_D are the same as F_M and F_D respectively for single turn windings). A typical value of this ratio is 0.6 which is interpreted to mean that a current of I_M (of the proper polarity) will cause the core to definitely change states, a current in the range $0 < I < 0.6\ I_M$ will not cause switching, and a current in the range $0.6 I_M < I < I_M$

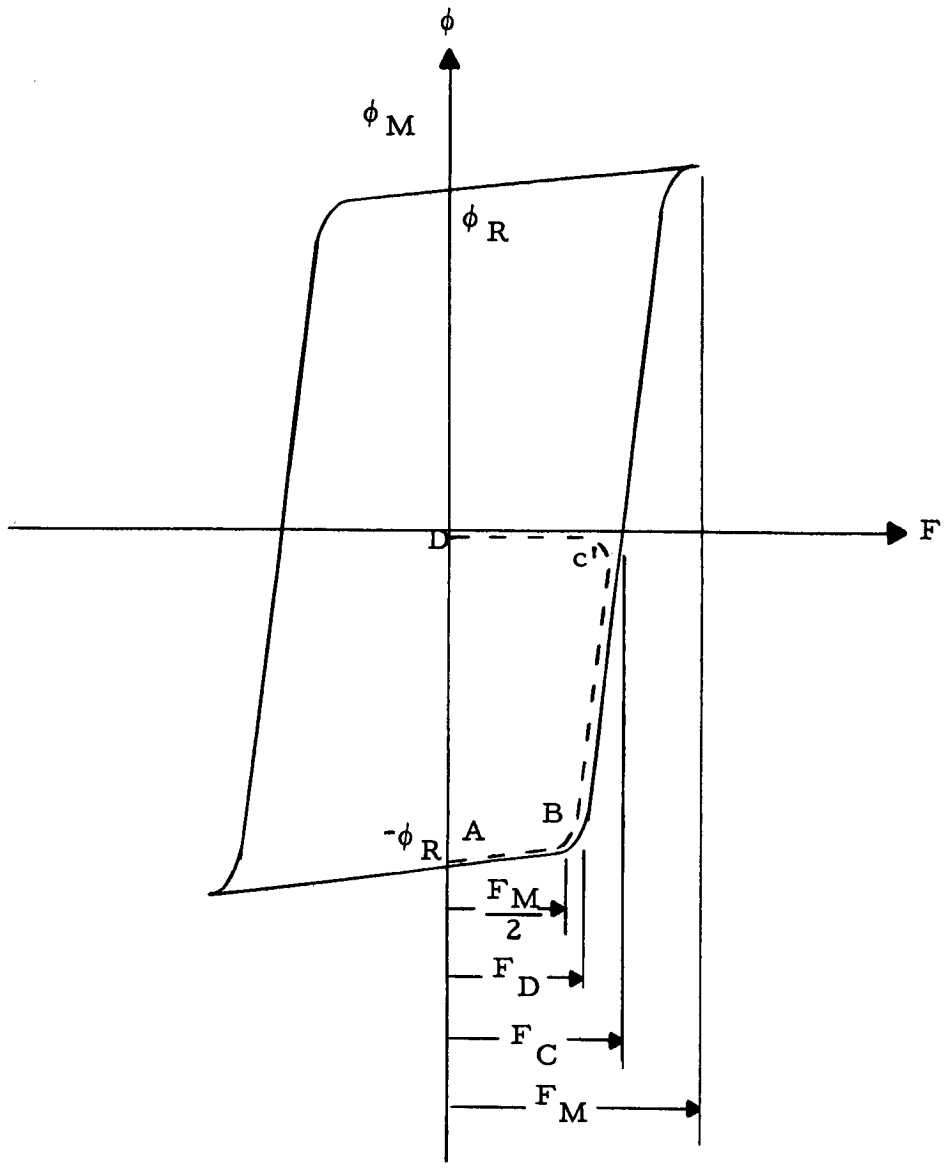


Fig. 4-1 Threshold Region of Non-ideally Square Hysteresis Loop.

will cause ambiguous and irreversible flux changes. More will be said of this parameter in later sections; it is sufficient to observe at the moment that the criteria mentioned above is easily met.

Care must be taken in the use of the current arrow symbol of Section 3.2 to account for this threshold region. In particular, K must be redefined as the ratio of the drive current in the wire in question to F_M / n, where n is the number of turns the current makes through the core. The sum of all currents through a core at a given time should not fall into the threshold region. Thus, when the sign of ΣK is such that the net excitation will tend to switch the core, the magnitude of ΣK must be either less than I_D / I_M or greater than one.

4.1.2 Destruction of Stored Data

Fig. 4-2 shows the same hysteresis loop as Fig. 4-1, and it is assumed that a core possessing this characteristic is to be used in a coincident-current memory. In the operation of the memory the core is considered to have strictly single turn windings and from Section 3.3.4 it can be seen that the only net excitations it can receive are:

(1) 1/2 R from either being partially selected by an addressing current during the read operation, or

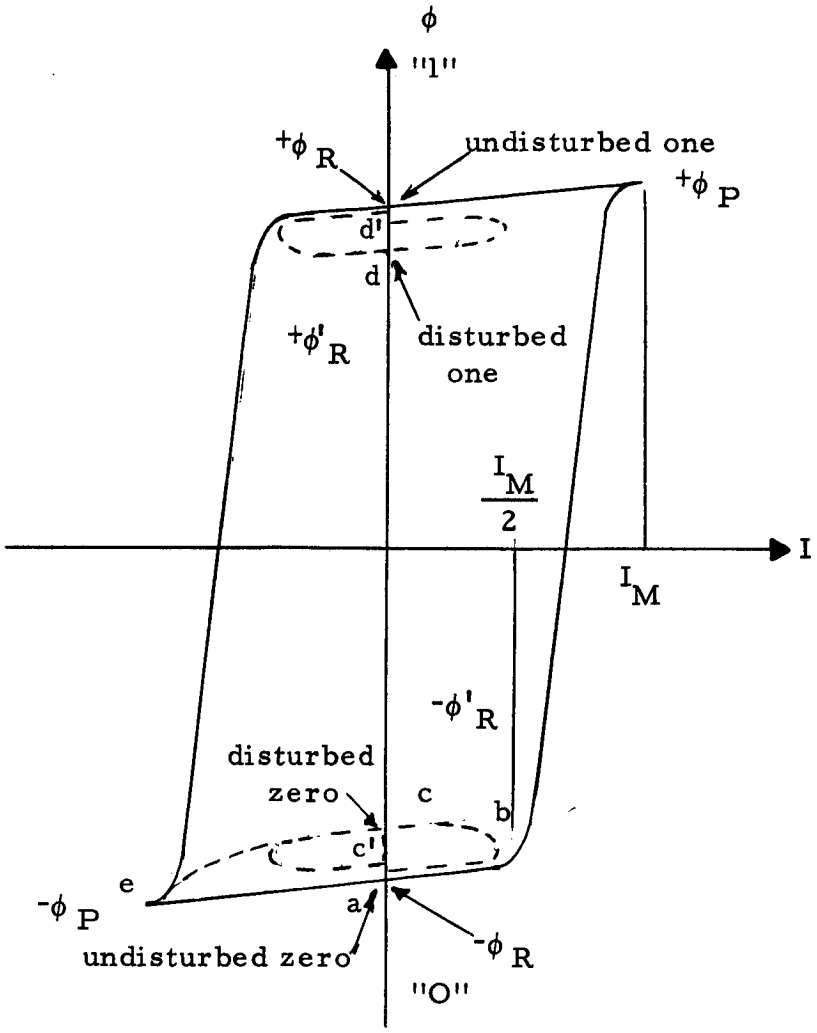


Fig. 4-2 Disturbance of Stored Data

from the inhibit current when a zero is being written into another core that is not in the same row or column of the same bit plane. This will be termed a "half-read" current.

(2) 1/2 R + 1/2 R when the contents of the core is read. The net current is $-I_M$ and termed a "full-read" current.

(3) 1/2 S when a zero is written into the core; or when a one is written into another core in the same row or column of the same bit plane. This is called a "half-write" current.

(4) 1/2 S + 1/2 S when a one is written into the core. The net current is I_M and called a "full-write" current.

(5) Zero in all other situations.

The full read and write currents are commonly called full select currents, and the half read and write currents all are called partial select currents. This terminology will be used where

appropriate.

In Fig. 4-2 it is assumed that a zero is stored at $-\phi_R$ and a one at $+\phi_R$.

Suppose that the core has just received a full-read current and consequently is at point "a" on the loop with remanent flux $-\phi_R$; the core is now said to contain an undisturbed zero. If a zero is now to be written into the core, it receives a half-write current, and a path such as abc is followed resulting in a small irreversible flux change. The remanent flux at c, $-\phi_R'$, is not the same as $-\phi_R$. Further applications of half-write currents tend to drive the core towards a remanent flux closer to the origin; that is they tend to demagnetize the core. However, each successive half-write current produces a smaller change in remanent flux than the preceding one, and a point of convergence is reached, near point c, such that application of further half-write currents produce no more changes in residual flux. It is necessary that such a point be reached for the reliable operation of a magnetic core memory. Even the cores used in early memories were sufficiently square to assure that such a point of convergence was reached, and this has never been a serious problem [2]. When the core is at this point it is said to contain a disturbed zero. Observe that when a disturbed zero is read there will be a greater flux change than

when an undisturbed zero is read.

In a similar fashion, if the core is driven to $+\phi_R$ by a full-write current, it contains an undisturbed one. Application of successive half-read currents drive the core to point "d" where it is said to contain a disturbed one.

Now if the core contains a disturbed zero, a half-read current will tend to drive the core back to point a to a flux at point a' between points a and c. Similarly, a disturbed one will go to point "d'" upon application of a half-write current. Successive application of $\pm 1/2\ I_M$ at either state of the core causes the remanent flux to change in value between those of the fully disturbed and undisturbed states. Application of a full-write or a full-read current will, however, always cause the core to return to an undisturbed state.

It is apparent from Fig. 4-2 that for a given value of disturbing current the difference in flux between corresponding disturbed and undisturbed will increase if the slope at the top and bottom of the hysteresis loop is to increase (i.e., if the squareness ratio decreases). Also for a given squareness ratio the difference between disturbed and undisturbed states will increase with increasing values of disturbing currents. Thus, the degree to which

data tends to be destroyed is a function of both the disturbing current and the squareness ratio. Normally the ratio I_D/I_M is defined so that successive applications of a current I_D will not cause the stored data to be lost.

4.1.3 Noise

From the preceding section it is seen that a changing flux results for each and every input current applied to a core. As a result, voltages are induced in the drive and sense windings. In a memory array, every voltage induced in the sense winding that is not a result of the selected core on the winding changing states when its contents are read constitutes noise.

Clearly noise is produced during the read operation by every core that receives a half-read current and by the addressed core if it is already in the zero state. Although the contributions of each noise producing core is usually small, the total noise produced in a coincident-current memory may be greater than the signal produced by the selected core changing states. Similarly, noise is produced by all fully and partially selected cores during the write operation, but this noise may be easily handled by logically ignoring all outputs from the memory while writing. But noise produced while reading is a more difficult problem, and

usually necessitates in a CCM using a different method of wiring the sense winding than that indicated in Section 3.3.4 as well as other measures. Solutions to the problem are discussed in Chapter 5.

4.2 Memory Cores and Their Describing Parameters

Of chief concern to the core memory designer is information regarding the currents that he must provide to operate the cores and the voltages that will result from these currents. Therefore, memory cores are usually specified in terms of currents and voltages rather than in terms of the hysteresis loop.

The current required to switch a core is typically on the order of several hundred milliamperes, and the usual shape of the current pulse used (Fig. 4-3.a) is trapazoidal with amplitude I_p. The following definitions are made to further describe the pulse:

(1) T_0 is the time at which the current reaches 10% of I_p during the initial rise.

(2) T_R is the rise time measured from T_0 until the time the current reaches 90% of I_p.

(3) T_D is the time duration measured between the two points at which the current is at 90% of I_p.

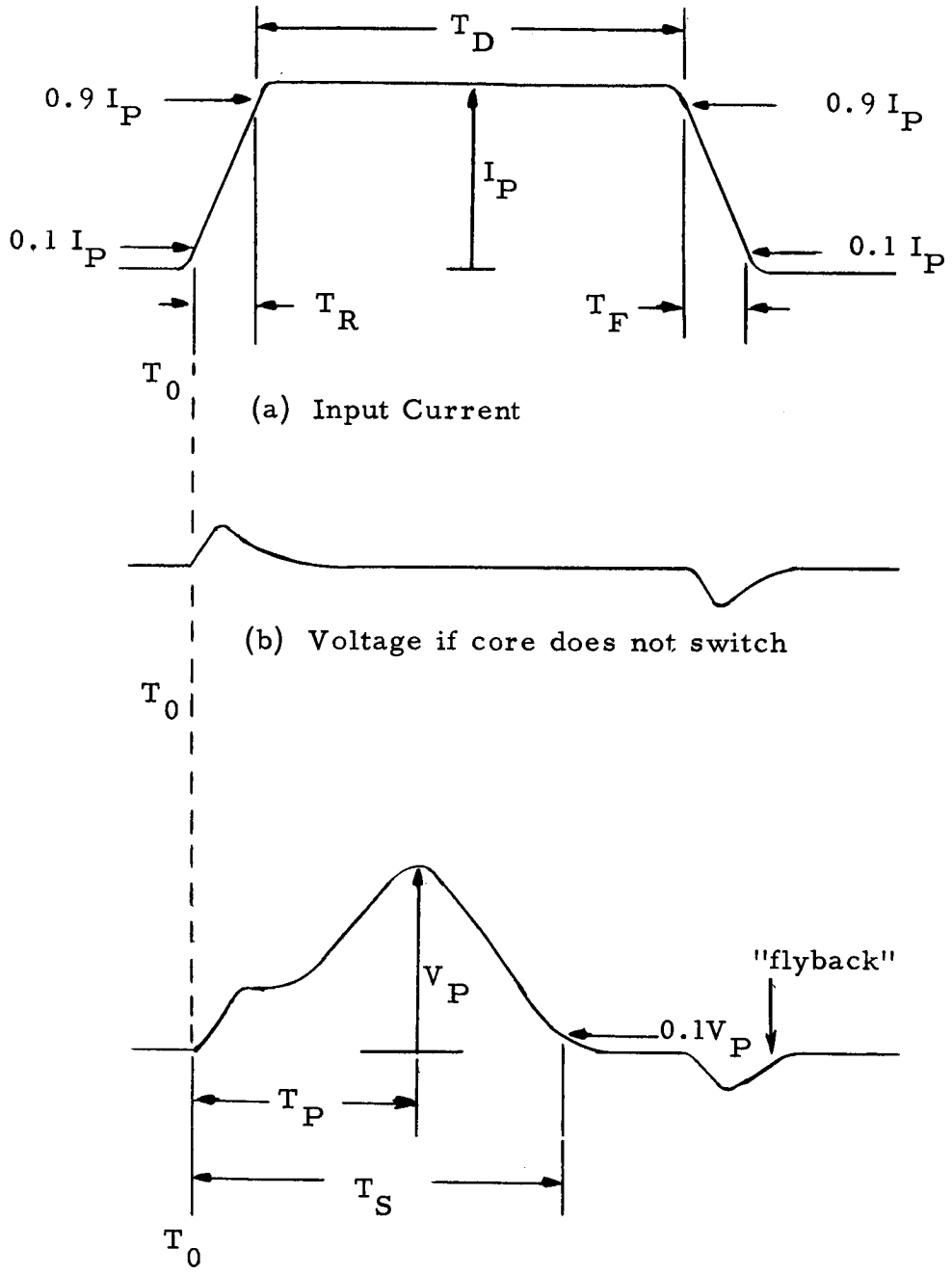


Fig. 4-3 Input Current and Output Voltages of Ferrite Memory Core under Unloaded Conditions.

(4) T_F is the fall time measured from the time at which the current has fallen from 90% of I_p until the time it reaches 10% of I_p.

The waveform of Fig. 4-3b is typical of the response of a core when the trapazoidal drive current does not cause the core to change states. Such a response would occur when a zero is read or when the core receives only a partial select current. The peak value of such a voltage is usually on the order of several millivolts.

The small flux changes which cause this type of response may occur quite rapidly, and they tend to follow the rise and fall of the current along the top or bottom of the hysteresis loop. The voltage, therefore, reaches a peak during the rise of the current, and the height of the peak will depend upon the amount of flux changed (which is in turn related to the squareness ratio) and the current rise time. Because in some cases part of the flux change is irreversible and cannot follow the current rise, a non-zero voltage may be present after the current has reached its peak[3]. The voltage is zero during most of T_D, and it has a negative peak due to the fall of the current which allows the flux to return to a new remanence value.

The voltage that is observed as a result of the core changing states is indicated by Fig. 4-3c. In Sect. 2.2.4 it was pointed out that the large irreversible flux changes will follow the current along the hysteresis loop only if T_R is very long. If T_R is zero, the core will switch much more rapidly and therefore produce a higher rate of change of flux and peak voltage. However, the core cannot switch in zero time because energy is required to produce a flux change. In practice T_R is usually considerably shorter than the time required for the flux change to occur , and Fig. 4-3c is a typical response for this situation.

During the initial part of the current rise, the flux tends to follow the horizontal part of the loop near the initial remanent flux. As the current approaches and exceeds the d-c threshold large changes of flux are called for, and the voltage does not reach its peak value, V_{pk}, until sometime after the current has reached I_p. The initial portion of the voltage pulse is dependent on the rise of the current, and under some circumstances the voltage will reach an initial peak and decay before going to the final peak, V_{pk}. After the flux has arrived at ϕ_p corresponding to I_p on the hysteresis loop, the current is allowed to go to zero, and a small voltage - termed the flyback voltage - results from the flux going from ϕ_p to the new remanent state. It is emphasized that this is the waveform

that occurs when the core is not loaded. Recall that when a core is loaded, the output pulse, or equivalently the manner in which the flux changes occur, depends largely upon the nature of the load. As was stated before, memory cores are normally operated under open-circuited conditions, and switching as a function of a load is not discussed here.

The parameters used to specify the voltage output as a result of an unloaded core changing states and typical values for them are:

(1) V_{pk}, the peak value of the voltage (from 25 to over 100 mv)

(2) T_S, the switching time, usually defined as the time from T_0 until the voltage decays to 10% of V_{pk}. (from a few tenths of a microsecond to five or six microseconds) This quantity may also be defined in terms of the time required for the flux to switch.

(3) T_P, the length of time measured from T_0 until the voltage reaches V_{pk} (slightly less than one-half T_S).

It is clear that in order to insure complete switching T_D must be made longer than T_S, and manufacturers normally suggest

that it be made at least 1.5 times greater than T_S. Also manufacturers normally specify or suggest a T_R to be used that is somewhat less than 25% of T_S.

In comparing Figs. 4-3b and 4-3c it is seen that the output of the core reaches its peak value later when it is switched than when it is not switched, and that the magnitude of the voltage from switching is greater than that of the other. The fact that the core changed states may then be determined by a time discrimination, by an amplitude discrimination, or by a combination of the two. In cases where there is noise produced by many cores, it is usually necessary to use a time descrimination since all of the noise occurs before V_{pk}; this may be accomplished by "strobing" the sense amplifier at T_p, i.e., by allowing the amplifier to operate only in response to the input voltage at time T_p [2].

Four output voltages that may occur in single-turn sense windings when the core is read are of prime interest. The following notation is frequently used:

(1) UV_1 for the voltage produced by reading an undisturbed one.

(2) DV_1 for the voltage produced by reading a disturbed one.

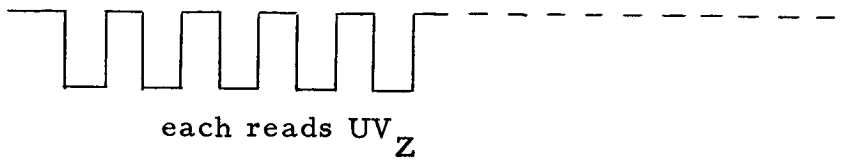
(3) UV_Z for the voltage produced by reading an undisturbed zero.

(4) DV_Z for the voltage produced by reading a disturbed zero.

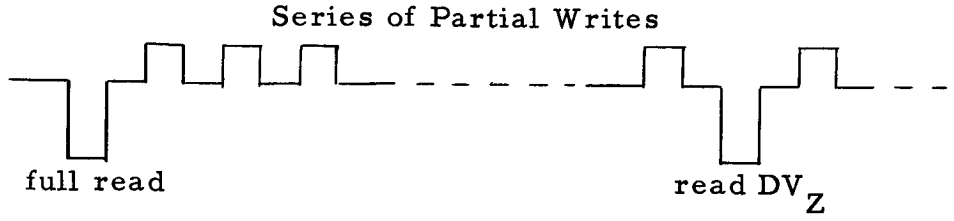
These may refer to either the particular voltage pulse or to its peak value; context normally makes clear which of the two is being referred to. The core response for a given full read current is specified by giving data for T_S, T_P, and the peak value of UV_1 and DV_Z.

These outputs may be observed experimentally by applying programmed sequences of appropriate current pulses to the core. For example, UV_1 may be observed by alternately applying full read and write currents; the voltage induced across a single turn winding when the read current is applied is UV_1. Fig. 4-4 shows four sequences; each sequence will allow one of the four voltages in question to be observed.

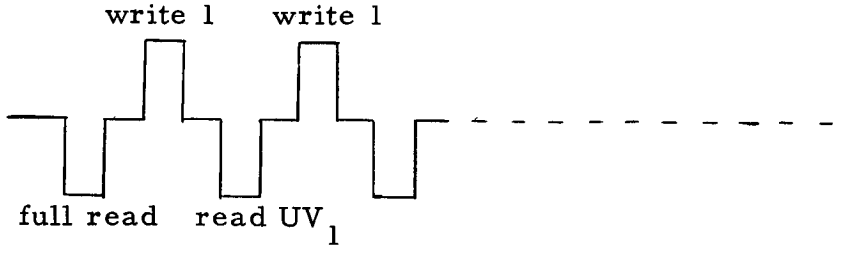
Four current pulse generators were designed and constructed in the laboratory in order to produce sequences such as these. Two have negative output currents, and the other two have positive outputs. The design (discussed in Chapter 5) allows the rise time, width, and amplitude of each generator's output to be



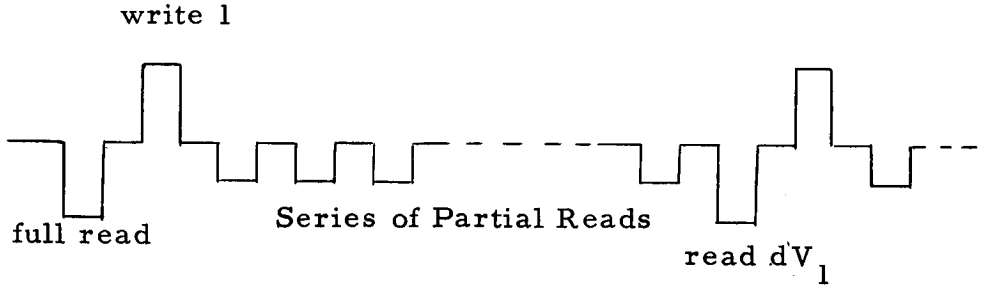
(a) for UV_Z



(b) for DV_Z

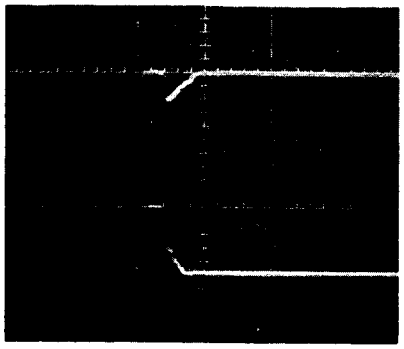


(c) for UV_1

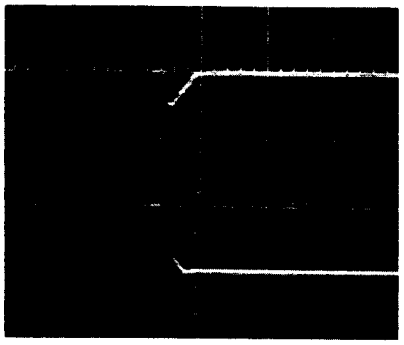


(d) for dV_1

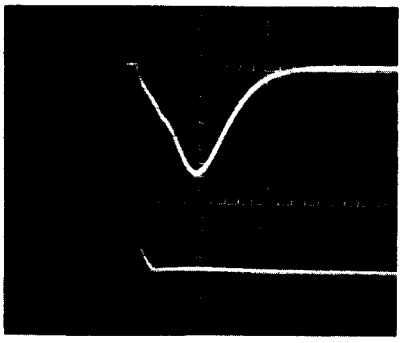
Fig. 4-4 Current Pulse Sequences Applied to a Core to Determine its Voltage Responses



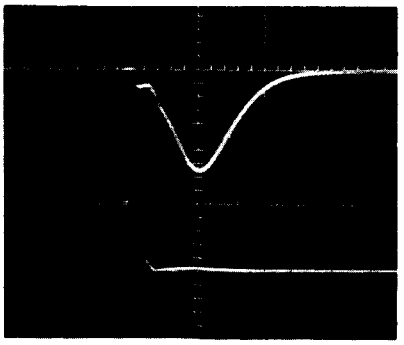
Upper Trace: UV_Z (50mv/cm)
Lower Trace: Read Current (600 ma/cm)
Time Base: 0.5μ sec/cm



Upper Trace: DV_Z (50mv/cm)
Lower Trace: Read Current (600ma/cm)
Time Base: 0.5 μ sec/cm



Upper Trace: UV_1 (100mv/cm)
Lower Trace: Read Current (600ma/cm)
Time Base: 0.5 μ sec/cm



Upper Trace: DV_1 (100mu/cm)
Lower Trace: Read Current (600ma/cm)
Time Base: 0.5 μ sec/cm

FIGURE 4-5 Voltage Responses of a Typical Memory Core

independently adjusted; and each generator produces a single pulse upon receipt of a standard logic signal from the Digital Systems Synthesizer described by P. M. Vargo[4] or from the outputs of the Wang Laboratories, Inc., Programmed Pulse Generator, Model 612AT. These features allow one to produce many different sequences of excitations.

The oscillograms of Fig. 4-5 show the four output voltages of a Lockheed 80-07 memory core. Pulse sequences such as those in Fig. 4-4 were used to generate the outputs; and in all cases the full read and write currents were 600 ma, and the half select currents were 300 ma.

As can be seen from Fig. 4-2, in reading a zero more flux is changed in approximately the same length of time when a disturbed zero is read than when an undisturbed zero is read. Consequently DV_Z is greater than UV_Z as is verified by Figs. 4-5a and 4-5b. Also notice that the slight irreversible flux change associated with DV_Z causes the response to be non-zero for a short time after the current has reached its peak. DV_Z is the worst case zero output from the core; and because a zero is usually written by the application of a half-write current (for addressing purposes), it is a frequently occuring case. Thus, DV_Z is the usual zero output that is specified.

The amount of flux switched when reading a disturbed one is slightly less than when an undisturbed one is read. Consequently DV_1 is slightly less in peak value than UV_1[3,5] as indicated by Figs. 4-5 c and 4-5 d. The percentage difference between the two is small and considerably less than that between UV_Z and DV_Z, and in selecting a core in the initial design of a memory the difference between UV_1 and DV_1 may be ignored. In some memories, such as the LSM described in Section 3.3.2, no half-read excitations exist; and UV_1 is the only situation in reading a one.

The previously mentioned I_D/I_M ratio (or sometimes simply I_D) is normally specified for a given value of full select current I_M, and it is measured in terms of DV_Z[6]. Recall that as the half-write current increases, the flux change that occurs in reading a DV_Z will increase also for a fixed value of full read current. Since the increase in this flux change will be primarily due to irreversible changes, the DV_Z response will lengthen in time as well as increase in peak value[3]. Because descrimination between a UV_1 (or DV_1) and DV_Z is the ultimate goal, a useful value for I_D is determined by observing the DV_Z output and adjusting the half-write current until DV_Z becomes intolerably large. The usual criteria is that I_D is the maximum half-write current which

may be repeatedly applied for which DV_Z is zero volts at time T_p in the UV_1 response for the given full select current I_M[6]. This usually insures that the peak of DV_Z is less than one-third the peak of UV_1. It is clear that the value measured in this manner will be dependent upon T_p.

4.3 Memory Core Response as a Function of Input Current, Size, and Temperature

It is the purpose of this section to discuss how a memory core's response varies with input and temperature, and how changing the size of a memory core will effect its characteristics.

4.3.1 Response as a Function of Input Current

The current pulse sequence of Fig. 4-6 allows one to simultaneously observe UV_Z, DV_Z, and UV_1 by triggering the oscilloscope on the full read pulse. The oscillograms of Figs. 4-7 and 4-8 were made to indicate the effects of varying the rise time and amplitude of the full read current. The core tested was a Lockheed 80-07, and in all tests the full-write and half-write currents were maintained at 600 and 300 ma respectively. The oscillograms of Fig. 4-7 show the effect of keeping the rise time constant and varying the read current from 600 ma to 1080 ma. In Fig. 4-8 the read current was maintained at a constant 600 ma

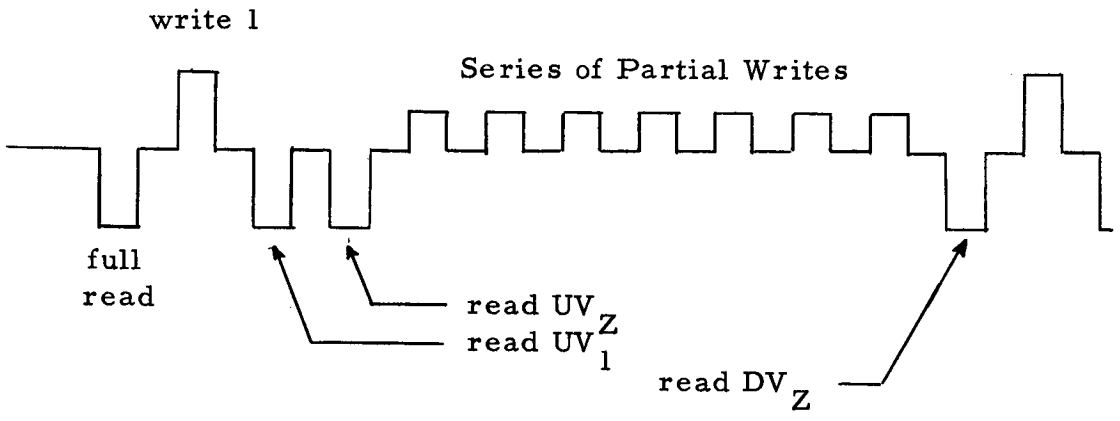
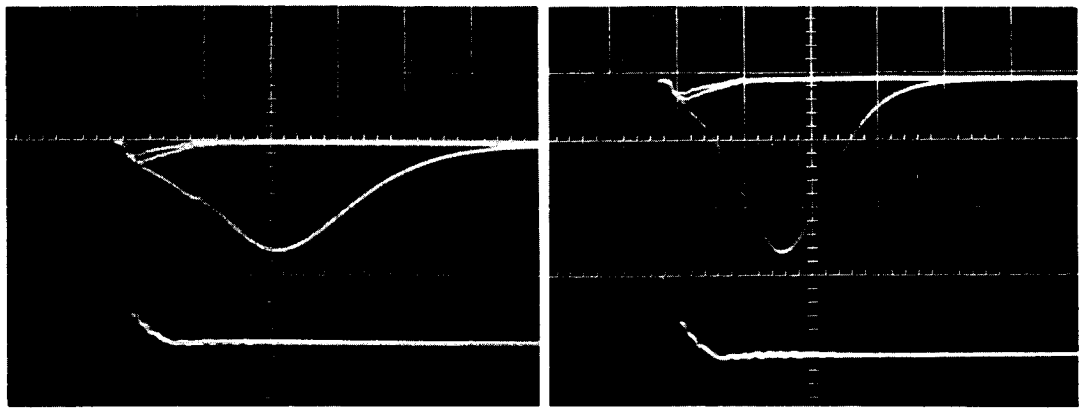
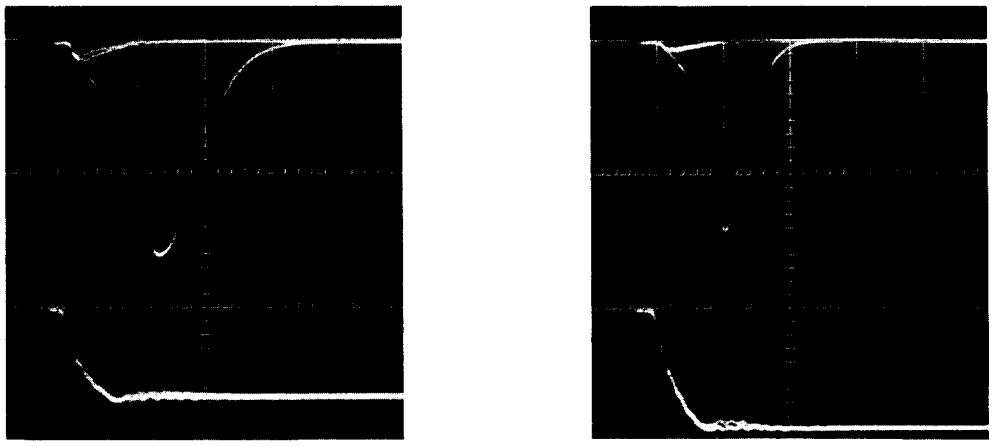


Fig. 4-6: Current Pulse Sequence for Simultaneously Observing UV_1, UV_Z, and DV_Z



(a)
Upper Trace 100 mv/ cm

(b)
Upper Trace 100 mv/ cm



(c)
Upper Trace 100 mv/ cm

(d)
Upper Trace 200 mv/ cm

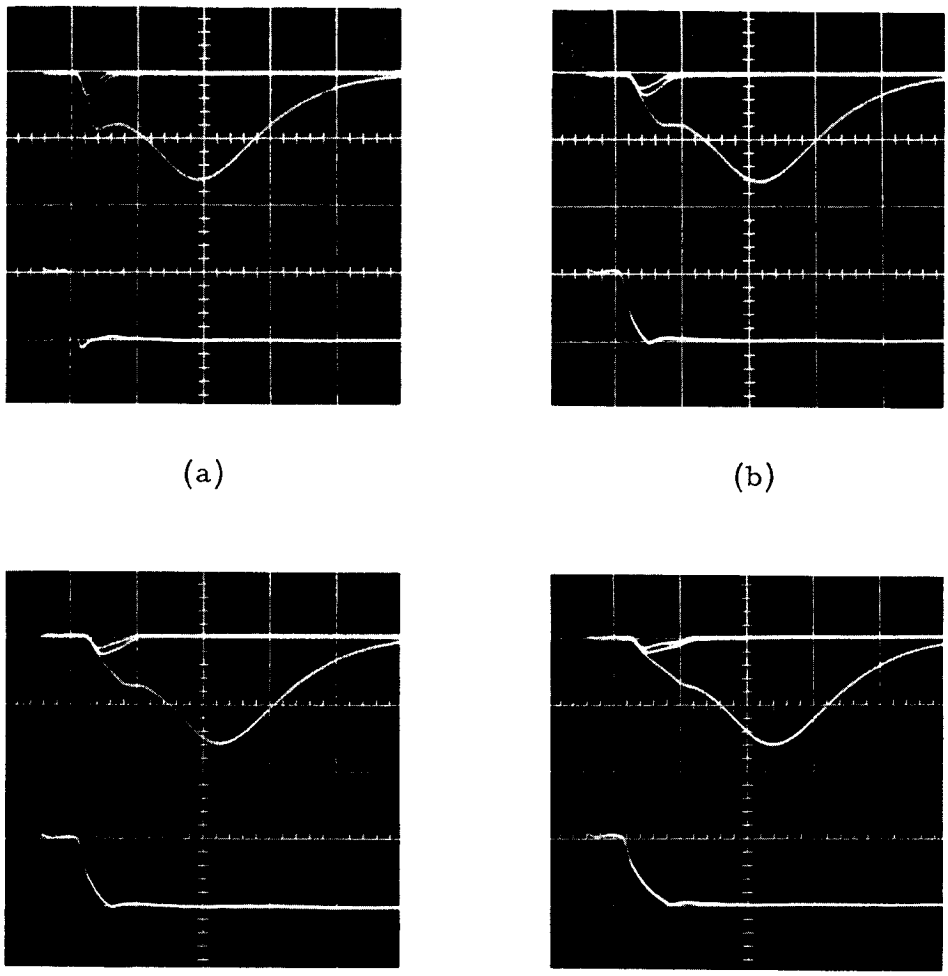
All Upper Traces are - from smallest to largest -

UV_Z, DV_Z, UV_1

All Lower Traces are Read Current at 600 ma/ cm

Time Base in all Cases is 0.2 μ sec/ cm

FIGURE 4-7: Memory Core Response as a Function of Current Amplitude



(a) (b)

(c) (d)

All upper traces are - from smallest to largest -

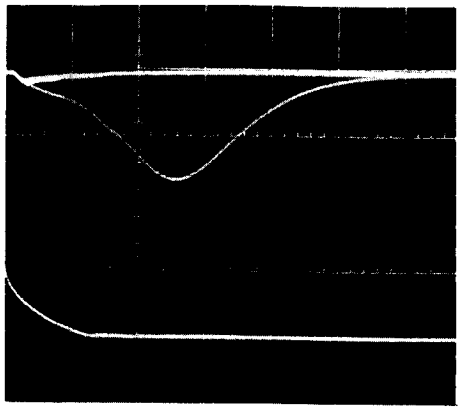
UV_Z, DV_Z, UV_1 at 100 mv/cm

All lower traces are Read Current at 600 ma/cm

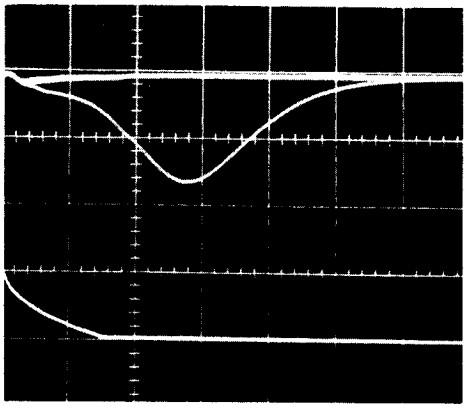
Time Base in All Cases is 0.2 μ sec/cm

- Figure continued on next page -

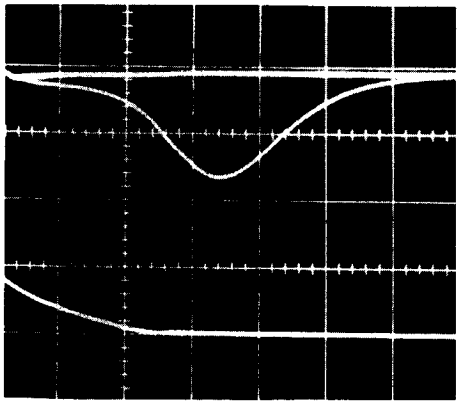
FIGURE 4-8: Memory Core Response as a Function of Rise Time



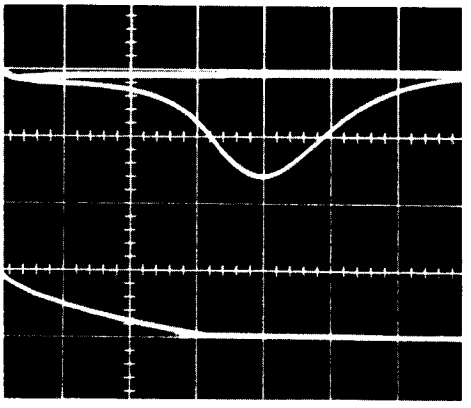
(e)



(f)



(g)



(h)

All upper traces are - from smallest to largest -

UV_Z, DV_Z, UV_1 at 100 mv/cm

All lower traces are read current at 600 ma/cm

Time base in all cases is 0.2μ sec/cm

FIGURE 4-8 (cont.) Memory Core Response as a Function of Rise Time.

while the rise time was varied from less than 0.03 μ sec. to almost 0.60 μ sec. All of the oscillograms were made at room temperature.

In Fig. 4-7 it is observed that as the read current is increased UV_1 increases also, and T_S and T_P decrease. However, UV_Z and DV_Z remain essentially constant in size and shape.

But in Fig. 4-8, as T_R increases the peaks of the zero voltages decrease, and their lengths increase. The peak of UV_1, in Fig. 4-8, stays at approximately 160 mv when T_R is short and decreases slightly after T_R exceeds 0.20 μ sec. When T_R is approximately 0.60 μ sec., UV_1 is about 140mv. T_S and T_P increase with T_R; when T_R exceeds 0.20 μ sec., the increase with T_R is most noticeable, that is T_S and T_P increase at an increasing rate with T_R.

There are three fundamental concepts which aid in the understanding of this phenomenon. The first is that if T_R is considerably less than T_S, then T_S is inversely related to the magnitude of the applied field when operating on the major loop, and any output windings on the core are open circuited.

$$T_S = S_w/(H - H_0) \qquad (4.3.1)$$

where S_w is a constant termed the switching constant, H is the step of applied field, and H_0 is a value of excitation below which the core will not switch. For ferrite memory cores H_0 is approximately equal to the coercive force, H_c [2, 5]. Relating this to a full read current of amplitude I gives

$$T_S = \frac{S_w L}{(I - I_0)} \qquad (4.3.2)$$

where L is the mean path length of the core, and I_0 is the current corresponding to H_0. This relationship has been found to hold reasonably well over a range of drive currents somewhat greater than I_0 [6, 7] and up to two to five times I_0 [5].

The second relationship is derived from Faraday's law. The drive current will cause the flux in the core to go from some remanent flux ϕ_1 to some ϕ_2 (removal of the current causes the flux to go to a new value of remanence). If Faraday's law is integrated over the time, T, in which the flux change occurs then it is seen that the area under the volt-time curve (the area enclosed by the voltage pulse) is exactly equal to the flux change times the number of turns, N, of the winding where the voltage is observed

$$\int_0^T v\,dt = N \int_{\phi_1}^{\phi_2} d\phi = N(\phi_2 - \phi_1) \qquad (4.3.3)$$

The third concept noted in Section 4.2 is that the flux tends to follow the rise of the current along the top and bottom of the hysteresis loop.

To explain the nature of DV_Z, assume that the flux change that occurs in reading a disturbed zero is essentially constant and independent of the amplitude of the read current. This will be approximately true when the squareness ratio is high and most of the flux change is due to the fact that the core had previously received a half-write current. Because most or all of the flux change occurs during the current rise, DV_Z will be independent of the read current amplitude. For the same reason, the time in which the flux change takes place increases with T_R. Thus, the length of DV_Z increases with T_R; and because the area under DV_Z must stay constant, the amplitude decreases with T_R. Stated in a slightly different manner, as the time for the flux change to occur increases, $d\phi / dt$ decreases.

I_D for the core tested is approximately 335 ma. If the half-write current were made greater so that it approaches I_D, then more flux would be switched when reading a disturbed zero. The area under DV_Z would therefore increase, and the amplitude and length of the signal would also increase with a smaller

percentage of the flux change occurring during T_R.

In a similar fashion the initial part of UV_1 is due to traversal along the top of the hysteresis loop (if $+\phi_R$ is defined as the one state), and the maximum value of UV_1 during the initial rise of the current depends upon the rise time as indicated by Fig. 4-8. When operating on the major hysteresis loop, the amount of flux switched when a one is read is approximately $2\phi_R$ if the loop has a high squareness ratio. Hence, the area under UV_1 is reasonably constant. But from (4.3.2) it is noted that as the drive current increases T_S must decrease (as evidenced by Fig. 4-7), and as a result, the final peak of UV_1 must increase. In Fig. 4-8 it will be observed that the trailing edges of all the UV_1's are nearly identical. The differences in T_P and T_S among them is due to the initial maximum voltage which increases with decreasing T_R; T_S must then increase with T_R to keep the area constant. The fact that the peak of UV_1 is essentially constant in all cases in Fig. 4-8 indicates that the maximum rate of change of flux is independent of the rise time over the range shown. But if T_R were to be increased more, it would be found that the peak would begin to decrease rapidly because the flux change would tend to follow the hysteresis loop whose slope would determine $d\phi / dt$.

To summarize the voltage responses, the amplitude of DV_Z increases with decreasing T_R with a constant half-write current; and the amplitude of UV_1, T_S, and T_P are primarily dependent on the amplitude of the read current for sufficiently short current rise times.

For operation on the major loop, I_D is constant, and I_D/I_M is inversely proportional to I_M. As I_M is decreased so that operation goes from the major loop to a minor loop, I_D will decrease also, and a simple relationship is no longer available. Also as T_R is decreased, the length of DV_Z will tend to decrease which implies that I_D can be made slightly larger before the DV_Z response is non-zero at time T_P. But because T_P tends to decrease somewhat with T_R, I_D/I_M will be relatively independent of T_R.

4.3.2 Effect of Core Size

In equation (4.3.1) S_w and H_0 are constants for the particular ferrite material from which the core is made, and they are independent of the size of the memory core. It is therefore apparent that two cores of different sizes but made of the same material will exhibit the same switching time if both are excited by the same value of H. But since $H = I/L$, the smaller of the

two cores will require less drive current to produce the same T_S as the larger core. This reflects the fact that less energy is required to switch the smaller core.

To increase the speed of a memory, it is clear that T_S must be decreased. This may be accomplished by either decreasing S_w or increasing the term $H-H_0$. By varying the composition of the ingredients of the ferrite material and the heat treatment used in molding the core, it is possible to vary the magnetic properties of the material[2]. S_w may be varied over a rather limited range of something less than 55 to approximately 65 μ sec-amp-turn/meter , and it is apparent that a significant change in T_S will not occur by attempts to vary this parameter. However, H_0 may be varied over a wide range from approximately 48 to 240 amp-turns/meter[5], and it is this parameter which will cause the most significant changes in T_S[2].

Decreasing T_S during read in an LSM may be readily accomplished by increasing the read current, but in a CCM the full select excitation is the sum of the two partial select excitations. Because H_c will always be greater than H_0, the total excitation applied in a CCM will be on the order of 1.3 to 1.6 times H_c[2, 5]; and therefore the switching time will be in the

neighborhood of $S_w / 0.5\ H_c$. Thus to increase the speed of a CCM a core with a high coercive force is used, and the same principle may also be applied to increase the writing speed in an LSM. This implies, however, that greater drive currents must be used to give an increase in speed if the core size is to stay constant; but by using smaller core with a greater H_c it is possible to increase the speed of a memory without causing a significant increase in drive currents.

To digress, equation (4.3.1) also holds for the large tape-wound cores. S_w for the tape wound cores is on the order of about one-half that of ferrites, but H_c is at least a factor of ten lower than for ferrites[5]. Thus, the tape wound cores have switching times that are greater than five times the switching speeds of the ferrites. Because the circumferences of the tape wound cores is an order of magnitude greater than those obtainable with ferrites, currents on the same order of magnitude are required to operate both. These facts coupled with price differential between the two types of cores show the desirability of ferrite cores over tape wound cores particularly for memories where cycle times less than 20 μ sec. are desired.

The voltage response as a function of core size is now examined. A relationship which describes the manner in which the flux changes in response to a step of excitation is [7]

$$\frac{dB}{dt} = S'(H - H_0) \qquad (4.3.4)$$

where H is again the applied field and S is a constant which is dependent upon the material. If H is applied at t = 0, this equation may be integrated to yield

$$T_S = \frac{2\,B_R}{S'(H - H_0)} \qquad (4.3.5)$$

where B_R is the remanence flux density of the material (It is assumed that the material has a high squareness ratio). In comparison with equation (4.3.1) it is seen that

$$S_w = \frac{2B_R}{S'} \qquad (4.3.6)$$

Substituting Equation (2.2.8) into (4.3.4) gives

$$\frac{d\phi}{dt} = S'\,A(H - H_0) \qquad (4.3.7)$$

where A is the cross sectional area of the core. From this equation it is seen that as the core size is decreased in a manner such that A is decreased, $d\phi / dt$ will decrease with A for a constant excitation H. Inspection of various manufacturers' data sheets reveals that the ratio of outside diameter to inside diameter for cores of various sizes is normally the same and approximately equal to 1.6. Therefore, as core size decreases, A decreases also. Furthermore, the smaller cores usually have a smaller width (h in Fig. 2.3) so that A decreases at a faster rate than does the diameter.

Thus, two cores of the same material but of different sizes, with cross sectional areas A_1 and A_2 respectively, will exhibit the same T_S for the same excitationH; and the peak values of their UV_1 responses will be in the ratio A_1/A_2 (assuming that both produce similar wave forms).

If the same read current rise time is used for both cores, the DV_Z response will be proportionately less in the smaller core since a proportionately smaller amount of flux will be switched in the same length of time.

In regards to the peak values of the response voltages, inspection of manufacturers' data shows that the faster switching

cores which require higher drive currents produce voltages of greater peak values than do slower cores of the same size.

Memory cores are currently available in four sizes; 20, 40, 50, and 80 mils in outside diameter, and the ratio of outside diameter to inside diameter is usually less than 1.6. Although there is a considerable overlap in characteristics between sizes, two rules of thumb, which are supported by manufacturers' data, are evident from the results of this section for comparing cores.

(1) Cores of the smaller sizes generally have shorter switching times, have smaller output voltages, and often times require somewhat lower drive currents than do the cores of the larger sizes.

(2) Those cores of a given size which require relatively high drive currents will have relatively short switching times and large output voltages.

The range of characteristics available in the 50 mil size, which is probably the most popular size, is the widest and greatly overlaps both the 30 and 80 mil sizes.

4.3.3 Temperature Effects

From Sect. 2.2.4 recall that the major hysteresis loop shrinks with increasing temperature; and over a range of temperatures far removed from the Curie Point, the shrinkage is linear. Therefore, I_D decreases with increasing temperature; and for a given I_M, I_D/I_M varies inversely with temperature. ϕ_R and I_D also decrease with increasing temperature, and therefore T_S and T_P will decrease as can be seen from Equations (4.3.2) and (4.3.5).

The above may be verified by inspecting manufacturers' memory core data which gives temperature information. Further inspection of these data reveals that UV_1 increases with increasing temperature (which implies that because the material contains more energy in the form of heat, the large irreversible flux changes may occur at a faster rate) and that DV_Z is essentially constant with temperature until the temperature has increased enough so that the half-write current exceeds I_D.

The relationships between UV_1, T_S, and I_D/I_M have been found to be reasonably linear with temperature and with drive current amplitude. The following equations have been emperically found, and they hold to within five per cent over a reasonable range of temperature and drive current[6].

$$UV_1 = a I_M + b\,\theta + c$$

$$1/T_S = a' I_M\,\theta + b' I_M + c'\,\theta + d'$$

$$\frac{1}{I_D / I_M} = a'' I_M\,\theta + b'' I_M + c''\,\theta + d''$$

where θ is the temperature in ^{o}C, I_M is the full read current, and the constants a, b, c, a'', etc., may be found experimentally for a given core.

It has been found that most memory cores can be reliably operated over a temperature range of at least $20^{o}C$, and there are cores available that may be operated over a range of $100^{o}C$ without special temperature compensating equipment[8]. These wide temperature range cores are relatively new, and it is expected that a greater variety of them will appear on the market.

4.4 Typical Manufacturers' Specifications

A crucial step in the design of a core memory is the selection of the particular core to be used from the many that are available on the market. By a proper interpretation of manufacturers' data, the designer will probably be able to select a core that meets such system specifications as cycle time and operating temperature range and whose inputs and outputs may be readily

coupled to the logic system. The purpose of this section is to review some of the common ways in which core specifications are presented, and their interpretation in the selection of a core is presented in Sect. 4.5.

Previous sections of this chapter have drawn on data presented by manufacturers; and it is assumed at this point that the reader has acquired a rough idea of what is available in memory cores.

Normally the manufacturer tests the electrical properties of every core produced using a current pulse sequence similar to that of Fig. 4-6. The full read pulse is usually equal to the full write pulse, but the partial select pulses are oftentimes of a magnitude close or equal to I_D and greater than one-half the full select currents. The current rise times are maintained at a value which will provide a minimal switching time yet a small zero output voltage, and it is usually in the neighborhood of 20 per cent of T_S. The output of the core must meet certain standards: DV_Z must be less than a certain value, UV_1 greater than a given value, T_S less than a given value, and T_P equal to a standard value plus or minus a few percent.

The simplest form of a manufacturer's data is a single summary sheet which lists a number of cores and tabulates for each core pertinent specifications from the testing. An example of this is the Lockheed Electronics Company's Ferrite Core Quick Reference Catalog (Bulletin 1001) which lists 30 memory cores and tabulates for each in addition to physical size the current pulse test program, the temperature at which the core is tested, the magnitudes of the currents used, T_R, T_D, the minimum UV_1, the maximum DV_Z, T_s and T_p. The tabulation for the Lockheed 80-07 core whose response is shown in Figs. 4-7 and 4-8 is as follows:

(1) Full read current = 560 ma

(2) Partial select current = 335 ma

(3) T_R = 0.2 μ sec

(4) T_D = 4.0 μ sec

(5) min UV_1 = 100 mv

(6) max DV_Z = 30 mv

(7) T_p = 0.6 $\pm$ 0.05 μ sec (for the full read current above)

(8) T_s = 1.25 μ sec

(9) Temperature = 25°C

(10) The current program was similar to that shown in Fig. 4-6.

Information such as this will eliminate many cores from consideration and may in some instances be sufficient to make the final selection.

Many manufacturers (e.g., Indiana General) provide a specification of one or more pages for each core giving more detailed information. In general size and mechanical standards are given in addition to the specifications for the electrical test outlined above. Also included will be a typical operating point for the core in use in a memory; this will normally state the full read and write currents, the partial select currents, T_R, and T_D as well as the voltage response parameters, UV_1, DV_Z, T_P and T_S. The most important part of the specification is a plot of UV_1, DV_Z, I_D/I_M, T_P, and T_S for a typical core as a function of full drive current. The plot may be for a single temperature, or it may be a family of curves for each variable with each curve in a family corresponding to a given temperature. An example of such a plot for a fictitious core is shown in Fig. 4-9.

Oftentimes a statement of the core's switching speed is mentioned; eg, "This is a one microsecond switching time core." This is interpreted as a round number indication the switching times to be expected in a CCM where the full read current is

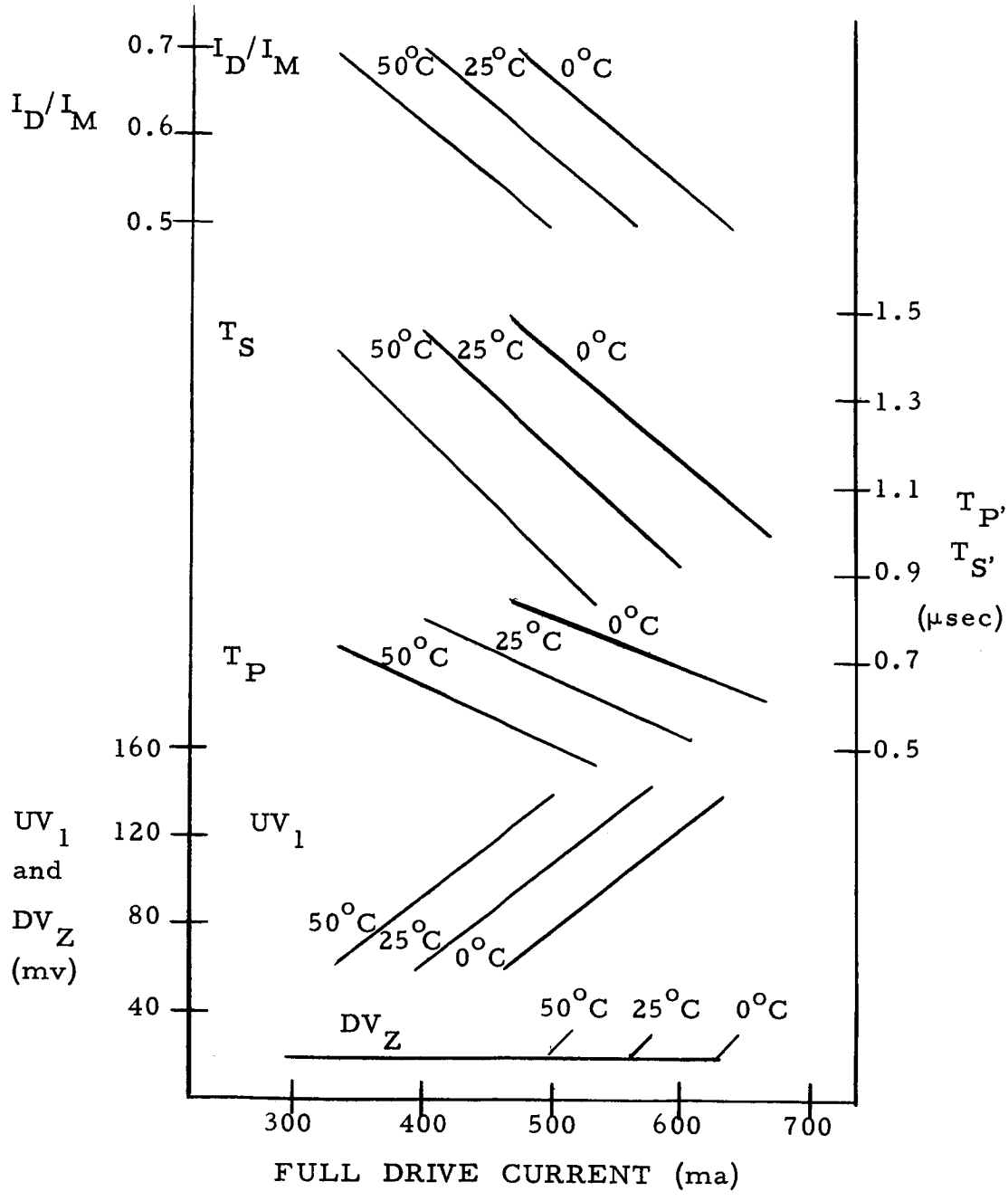


Fig. 4-9 Typical Characteristics of a Ficticious Memory Core

limited to being the sum of two half-read currents. In the LSM the read current is unbounded and much faster switching speeds may be attained during reading by using a higher current.

4.5 Core Selection

All of the core parameters discussed will probably be taken into consideration in the process of selecting a core to be used in a memory. Because there are several variables to be considered, an orderly procedure to follow in the selection process is called for. The procedure described here is essentially that expounded by M. Eisenberg in Reference 6 (which also included nomograms representing the characteristics of seven Indiana General memory cores.)

There are two major duties the core must perform:

1. It must reliably receive and retain one bit of binary data.
2. Upon command it must produce a voltage pulse from which it can be reliably determined what data was stored.

In general, both must be done within the speed

requirements of the memory and under conditions of varying drive currents and temperature.

It is therefore first necessary to define the memory configuration mode of operation, speed requirements, and operating temperature range. Several current drivers will be required to operate the memory, and each will be designed to produce a current of nominal amplitude I with a tolerance Δ so that the output may be written as $I(1 \pm \Delta)$. This gives rise to the condition of variable current, and some statement as to what tolerances are available or desirable should be made. Tolerances in the neighborhood of one to ten per cent are typical depending of course on the memory form.

Following this statement many cores can probably be eliminated from consideration.

The temperature range should first be considered. If the memory is to be operated at room temperature plus or minus $10^{\circ}C$ (about $72^{\circ} \pm 18^{\circ}F$), then most memory cores tested at $25^{\circ}C$ will be suitable.[8] If, on the other hand, the memory is to experience a wide range of temperatures, then many cores will immediately be unsuitable and may be eliminated; the search will be

limited to a few cores whose specifications indicate they are suitable for the temperature range to be encountered.

The speed requirements will eliminate cores whose switching times (or range of switching times available) are longer or close to the time available for writing or reading may be eliminated. (Recall that the drive pulses must be longer than the switching time) Where high speeds are required (cycle times less than 2 μ sec.) it may not be necessary to even look at the characteristics of the larger cores. Where high speed is not a requirement, the smaller and/or fast switching cores might be eliminated since they will require a shorter rise time, which implies more expensive current drivers for good output signals. Rise times on the order of 0.2 to 0.5 μ sec can be readily achieved as indicated in Chapter 6.

The remaining cores are then examined as to the currents that will be required to operate them reliably and their voltage responses. As a starting point, the typical or recommended operating conditions, if given in the specification, are looked at, and cores with drive currents and outputs that are not in a convenient range may be rejected.

Worst case input current equations may be written for any memory configuration in terms of nominal values of drive currents, their associated tolerances, the threshold current I_D, and a current, I_{sm}, which is just sufficient to switch a core in a satisfactory manner. The procedure--illustrated by several examples in Sections 5.2.4 and 5.3.3--in doing so is to sum the worst case currents applied to the addressed cores for the operations of reading, writing ones, and writing zeros. Each sum is made greater than I_{sm} or less than I_D as the situation demands. Relations are also written for the currents that are applied to non-addressed cores; the net current applied to these cores must always be less than or equal to I_D. From these relationships, a new relationship between the tolerances and the ratio I_D/I_{sm} is found. This ratio is the I_D/I_M at the minimum full switching current, and the relationship found will demand that it be greater than or equal to some numerical value that can be computed from the desired tolerances. Because I_D/I_M decreases with increasing current and temperature, the minimum value of I_D/I_{sm} will determine the upper limit of I_{sm} for a given core.

Now I_{sm} and I_D for a given core are determined from the specification sheet or equivalent data. To satisfy the above

relationship, I_{sm} is located from the I_D/I_M characteristic at the upper temperature limit of the specified temperature range for the memory, and its maximum value is the full drive current for which I_D/I_M just satisfies the relationship. In cases where data is given at only one temperature and the expected temperature range will not vary too much from that temperature, say less than 10^{o} or $15^{o}C$, I_{sm} is chosen less than the value of current for which I_D/I_M satisfies the tolerance relationship on the one curve given. From inspection of data for various cores, a reduction of 10 to 15 per cent appears reasonably conservative. In any event I_{sm} should be chosen at least slightly less than the maximum value indicated to allow for small core-to-core variations in threshold. Also it is clear that if at the low temperature this value of I_{sm} fails to switch the core then a higher value of I_{sm} is required. This means that tolerances must be tightened, the temperature range reduced, or discarding the core from consideration.

With I_{sm} and I_D known, the worst case current equations are returned to, and the nominal values of the drive currents are found. The voltage response of the core is found from the core characteristics at the limits of temperature and full select current to determine the variations. The maximum T_S and

T_p and the minimum UV_1 will occur at the minimum current and the minimum temperature; whereas the minimum T_S and T_P and the maximum UV_1 occur at the maximum current and temperature.

This information allows one to compare how several different cores will perform in the memory; and, together with information about the zero output, the final selection can be made. The criteria used in the final selection will depend partly upon the memory configuration. For example, in a CCM the discrimination between a one output and a zero output is often made on a time basis, and uniformity in the output over the extremes of temperature and full read current would then be highly important. In a small LSM, on the other hand, the descrimination will probably be made strictly upon an amplitude basis, and a large difference between peak values of DV_Z and UV_1 are called for.

It should be noted that the core response will usually be taken from data for a typical core. The maximum core-to-core variation in the voltage response from the typical is dependent upon the degree of uniformity to which the manufacturer can produce cores of a given type as well as how faithfully he represents the performance of a typical core. About the only indication that one can get as to the variation is to compare the worst values of the

parameters to which the core is tested to the typical values given at the same drive current. For example, if the minimum UV_1 for the test is 90 mv at 550 ma and the typical UV_1 at the same current is 100 mv, then the typical UV_1 characteristic could be accepted to plus or minus ten per cent. In the final decision, this variation should be considered.

The final steps of this selection procedure were based upon the assumption that current driver tolerances were specified. This is not an unlikely situation since the cost of a current driver will increase as the necessary tolerances are made tighter. However, some other criteria may be used as a starting point, and the procedure will have to be changed to accommodate it. For example, a particular sense amplifier as well as an upper limit on drive currents might be specified. In this case, the search is narrowed to cores which meet speed and temperature requirements and also have the capability to operate within the current range. The sense amplifier characteristics will determine the ranges over which the voltage response parameters can vary. Then for each core the limits on the drive currents may be found and the tolerances determined. The final selection will probably be the core that allows the loosest tolerances.

In situations where a core cannot be found to meet the design requirements, it will be necessary to change or modify some of the requirements, such as tightening current tolerances.

The following example serves to illustrate some of the points of this section. The core whose characteristics are shown in Figure 4-9 is to be investigated for possible use in a CCM operating in a temperature range from 25°C to 50°C. The cycle time is to be 15 μ sec. divided equally between reading and writing. All current driver tolerances are to be plus or minus five per cent or looser where possible. The temperatures and switching times indicated in Figure 4-9 indicate that this core meet the temperature and timing requirements.

The following two relationships have been found in Section 5.2.4

$$\frac{I_D}{I_{sm}} \geq \frac{1}{2}\left(\frac{1+\Delta_R}{1-\Delta_R}\right) = 0.55 \qquad (5.2.5)$$

$$\frac{I_D}{I_{sm}} \geq \frac{1}{2}(1+\Delta_I)\left(\frac{1+\Delta_W}{1-\Delta_W}\right) = 0.58 \qquad (5.2.18)$$

The first is for reading and Δ_R is the tolerance (expressed as a decimal) of the half-read currents. The second

is for writing; Δ_I is the inhibit current tolerance, and Δ_W is the half-write current tolerance. For each tolerance 0.05 has been substituted, and the calculation made. I_D/I_{sm} is greater for writing, and we will let this determine I_{sm} for both cases. This will allow greater freedom in the half-read current. From the I_D/I_M curve for 50°C, I_{sm} is chosen as 420 ma corresponding to $I_D/I_M = 0.59$ which makes I_{sm} slightly less than the maximum value. This gives $I_D = 248$ ma.

Also from Section 5.2.4 the nominal half-write current, $I_{\frac{1}{2}W}$, and the inhibit current, I_I, may be calculated for a given tolerance as follows:

$$I_{\frac{1}{2}W} = \frac{I_{sm}}{2(1-\Delta W)} = \frac{420}{2 \cdot 0.95} = 221 \text{ ma.}$$

$$I_I = \frac{I_D}{(1+\Delta W)} = \frac{248}{1.05} = 236 \text{ ma.}$$

Advantage of the extra freedom in the read currents will be taken to give looser tolerances. Using $I_D/I_{sm} = 0.58$ in (5.2.5) and solving for Δ_R gives $\Delta_R \leq 0.074$. The nominal half-read current, $I_{\frac{1}{2}R}$, must satisfy

$$I_{\frac{1}{2}R} \geq \frac{I_{sm}}{2(1-\Delta_R)}$$

and

$$I_{\frac{1}{2}R} \leq \frac{I_D}{(1+\Delta_R)}$$

using $\Delta_R = 0.074$ allows $I_{\frac{1}{2}R} = 228$ ma $\pm$ 7.4%. The limits on the full-read current are then 420 and 490 ma. The typical core output will vary from

(a) at 420 ma and 25°C

$UV_1 = 65$ mv

$T_P = 0.78$ μ sec

$T_S = 1.45$ μ sec

(b) at 490 ma and 50°C

$UV_1 = 135$ mv

$T_P = 0.52$ μ sec

$T_S = 0.96$ μ sec

DV_Z in all cases is under 15 mv.

Notice that the wide variation in UV_1 and T_P might

make a time discrimination rather difficult, and a better core might be sought or the read current tolerances perhaps tightened.

4.6 References for Chapter 4

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