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Technical Memorandum

GEOS A OPTICAL MEMORY AND CONTROL UNIT

by R. S. COOPERMAN

supported by NASA

THE JOHNS HOPKINS UNIVERSITY ▪ APPLIED PHYSICS LABORATORY

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by R. S. COOPERMAN

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8621 Georgia Avenue, Silver Spring, Maryland 20910

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The Johns Hopkins University
APPLIED PHYSICS LABORATORY
Silver Spring, Maryland

ABSTRACT

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The GEOS Optical Memory and Control Unit is a digital delayed command system with a high accuracy real time clock designed to control the operation of the optical beacon. The memory can store up to 59 light flash sequence requests and operates in a 68 hour cycle. The memory is synchronously loaded from the ground without disturbing timing. The one minute scan period of the memory may be set in coincidence with Universal Time (UT2) by resetting the clock on ground command. A means of digital time normalization of variations in the satellite clock is also provided.

Author

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I. INTRODUCTION

Functionally the GEOS Optical Memory and Control Unit (Figure 1) is a serial operation fixed program special purpose digital machine. The unit controls the operation of four high intensity light flash tubes and has the capability of initiating up to 59 individual light flash sequences over an interval of up to 68 hours. Provision is made for tailoring the intensity and duration of each sequence to the needs of the experimenter. Light flash sequences are programmable to commence at any UT2 minute, with the first flash occurring coincident with the UT2 minute marker and subsequent flashes occurring at intervals of four seconds. Flash sequences may be individually set to any one of four intensity levels and for either five or seven flashes. The total actual number of flashes is accumulated and stored for later readout.

Time markers are generated in the form of a burst of square-wave phase modulation on the doppler and TM transmitters. The time markers are held in close coincidence with the UT mark by a time normalized digital divider operating from a high stability crystal oscillator. Provision is made for stopping the clock in order to resynchronize the satellite time markers with UT2.

The memory is normally synchronously loaded with processed flash request data in the form of initiate time, intensity and duration for each of up to 59 flash sequences. The entire memory contents is then serially read out, processed and restored once per minute. During each memory readout the initiate time portion of each flash time word is incremented by binary one; when a particular time portion contains all binary ones a flash sequence is initiated.

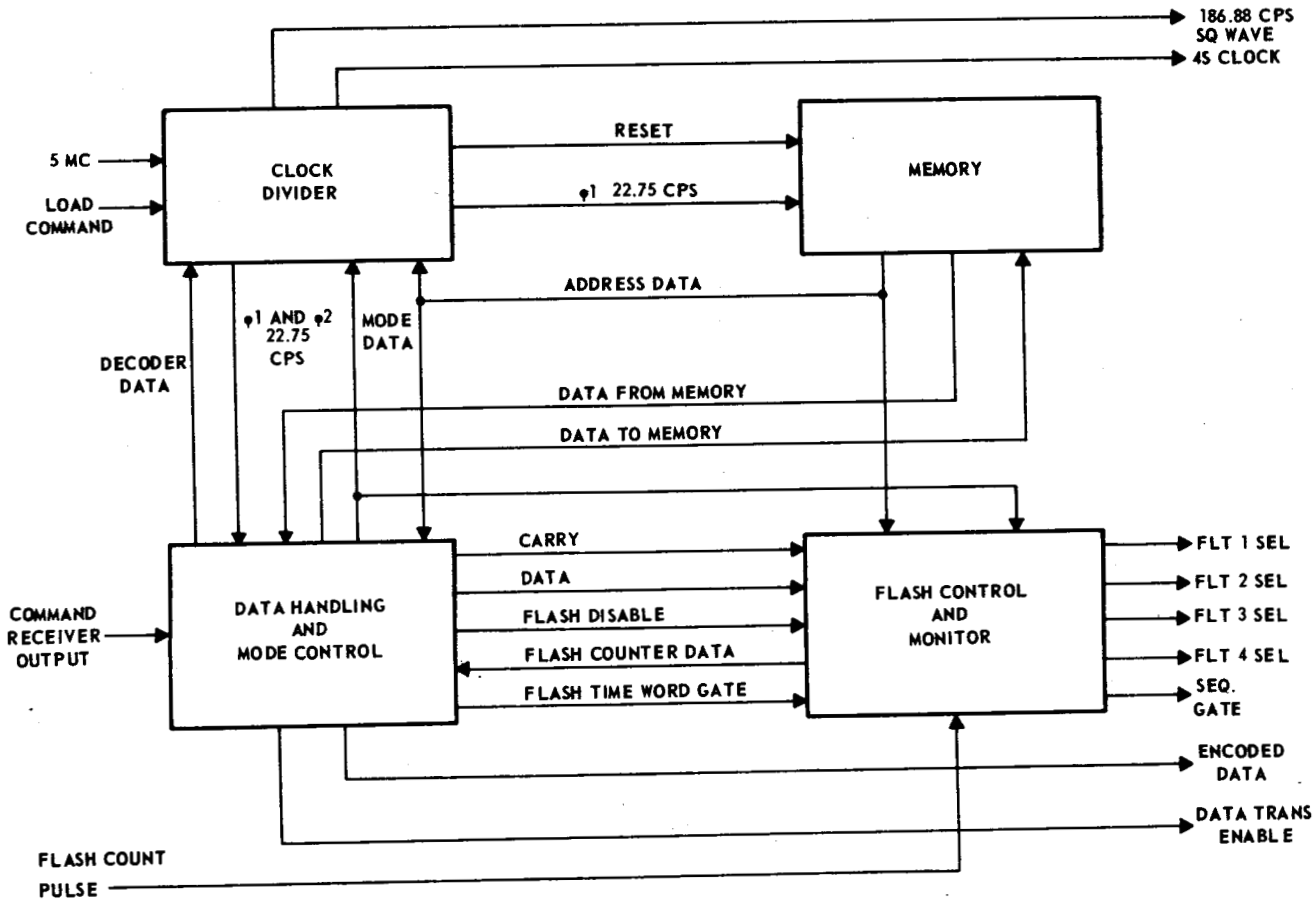

Fig. 1 GEOS OPTICAL MEMORY AND CONTROL UNIT, BLOCK DIAGRAM

Physically each GEOS Optical Memory and Control Unit (Figures 2, 3 and 4) is contained in two and one-half standard books (occupying 191.9 cubic inches), weighs 4.53 pounds and consumes 1.68 watts of power. Each GEOS satellite contains two complete optical memory and control units connected so that only inputs and outputs are in parallel. Power is switchable between the two units so that only one is in operation at a time with the other unit in unpowered standby. Input and output circuits are designed so as to minimize interaction between the operating and standby units. Operation has been successfully proved over the temperature range of $-50^{\circ}C$ to $+70^{\circ}C$ with a ±15% variation in supply voltage.

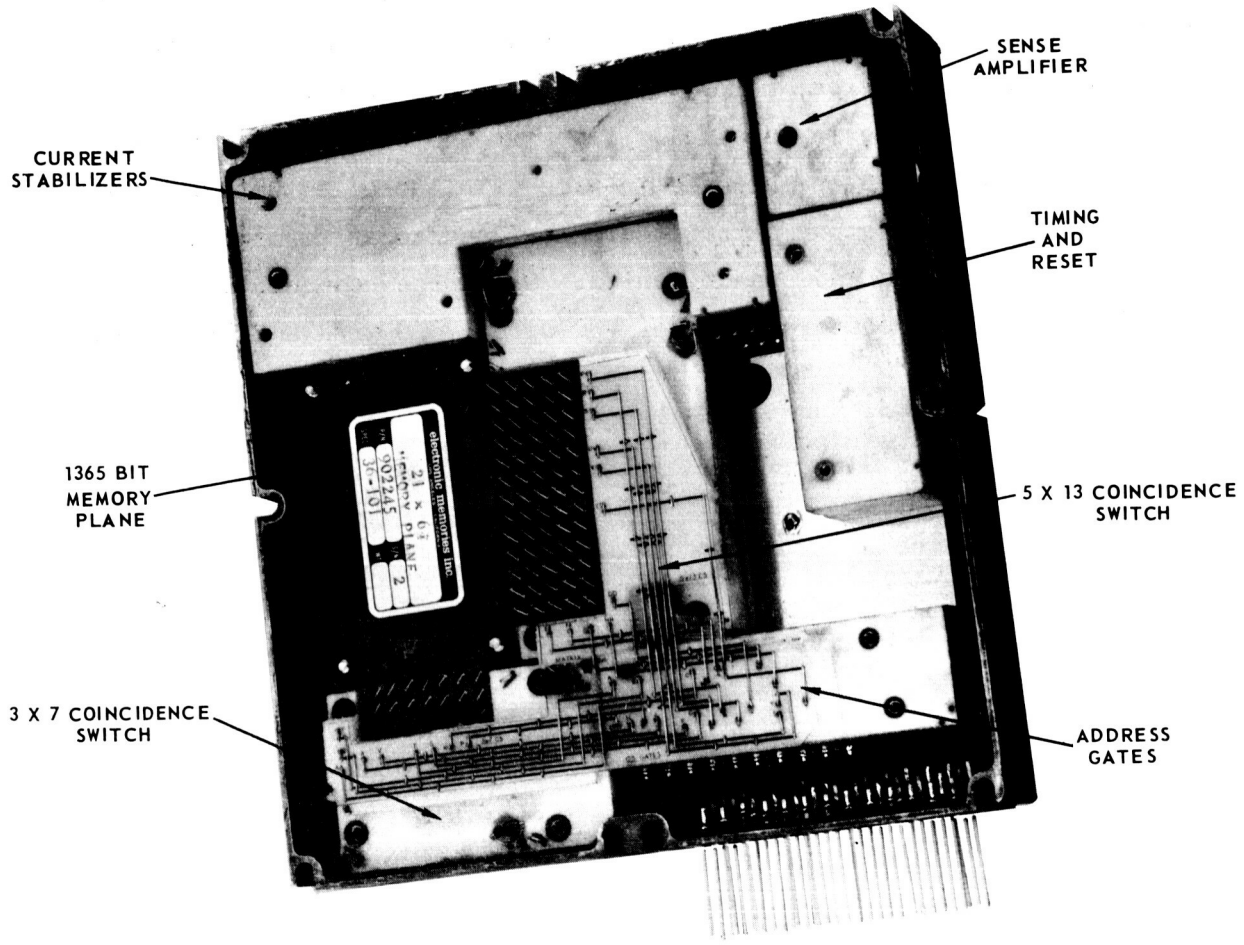

Fig. 2 GEOS OPTICAL MEMORY AND CONTROL UNIT, BOOK 1

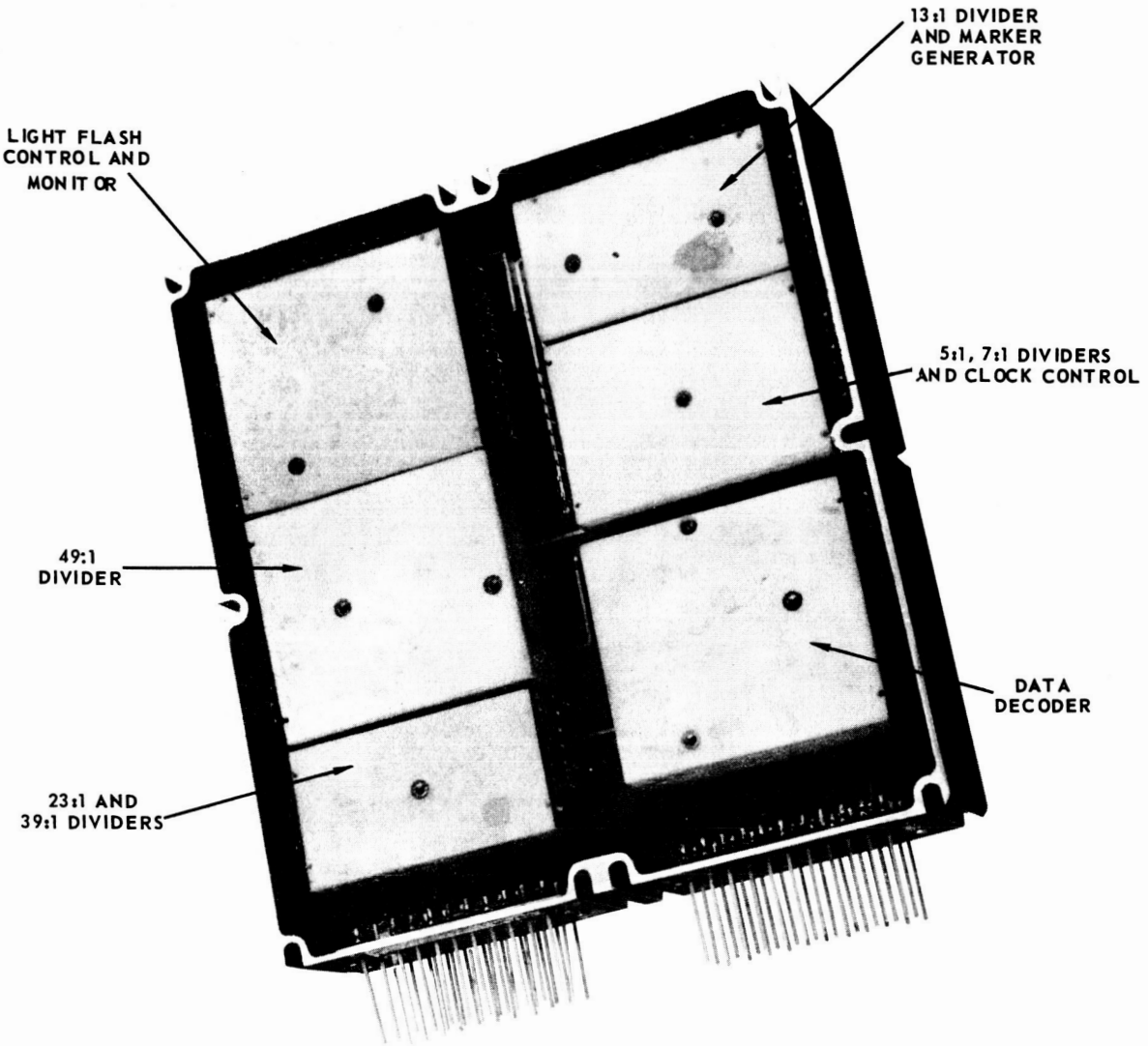

Fig. 3 GEOS OPTICAL MEMORY AND CONTROL UNIT, BOOK 2

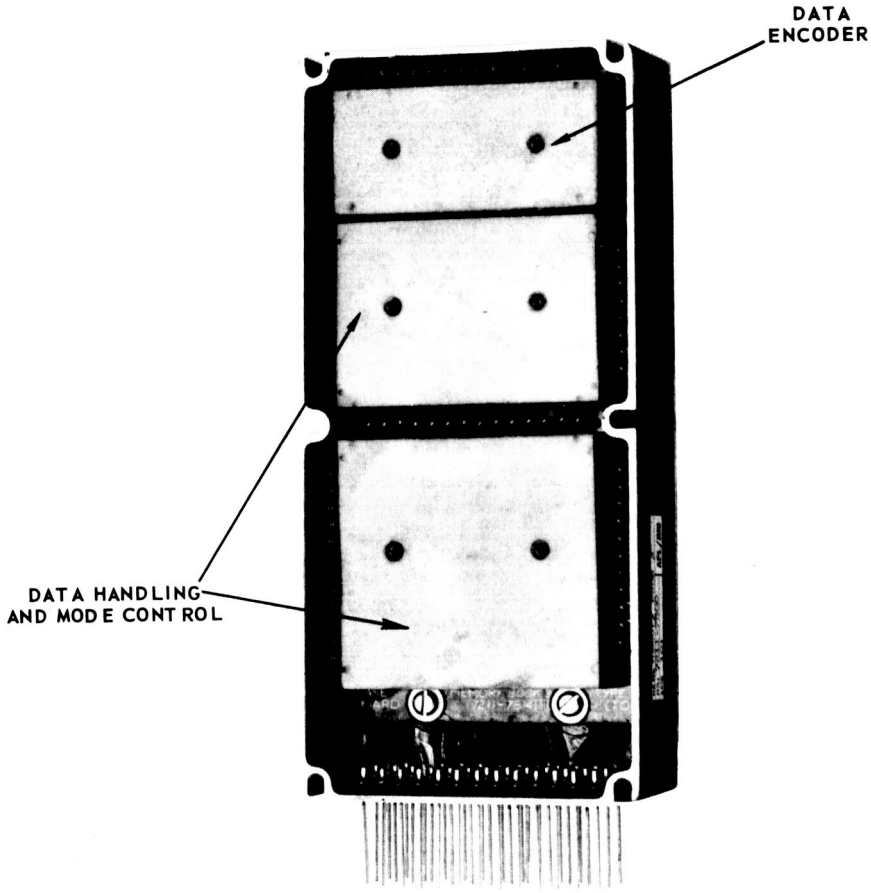

Fig. 4 GEOS OPTICAL MEMORY AND CONTROL UNIT, BOOK 3

II. SYSTEM DESIGN

A. Word Format

The magnetic core memory contents of 1365 bits is treated as 65 twenty-one bit words. The memory is organized with four different word formats as follows:

Words 1 to 59 — Flash Time Words (Figure 5A) -- Stores four forms of data: time to initiate flash sequence, lamp bank complement designation, flash sequence length, time normalization delete bits. The first twelve bits store in 2's complement binary form a number which represents the particular number of minutes after completion of the load scan for the flash sequence to commence. Thus the number stored in the first 12 bits is the binary equivalent of $2^{12} - T$, where T is the number minutes from the completion of the load scan. For example, if a flash sequence is to commence five minutes after the completion of the load scan, we would store the binary equivalent of 4096 - 5 or 4091 (110111111111). Bits 13, 14, 15 and 16 are associated with flash tubes 1, 2, 3 and 4 respectively. A data one bit in any of these positions will include the associated flash tube in the flash tube complement for that particular flash sequence. Bit 17 determines whether the sequence will be 5 or 7 flashes in length; data 1 for 7 flashes, data 0 for 5 flashes. The remaining four bits are used by the time normalizer (refer to Section III-B.

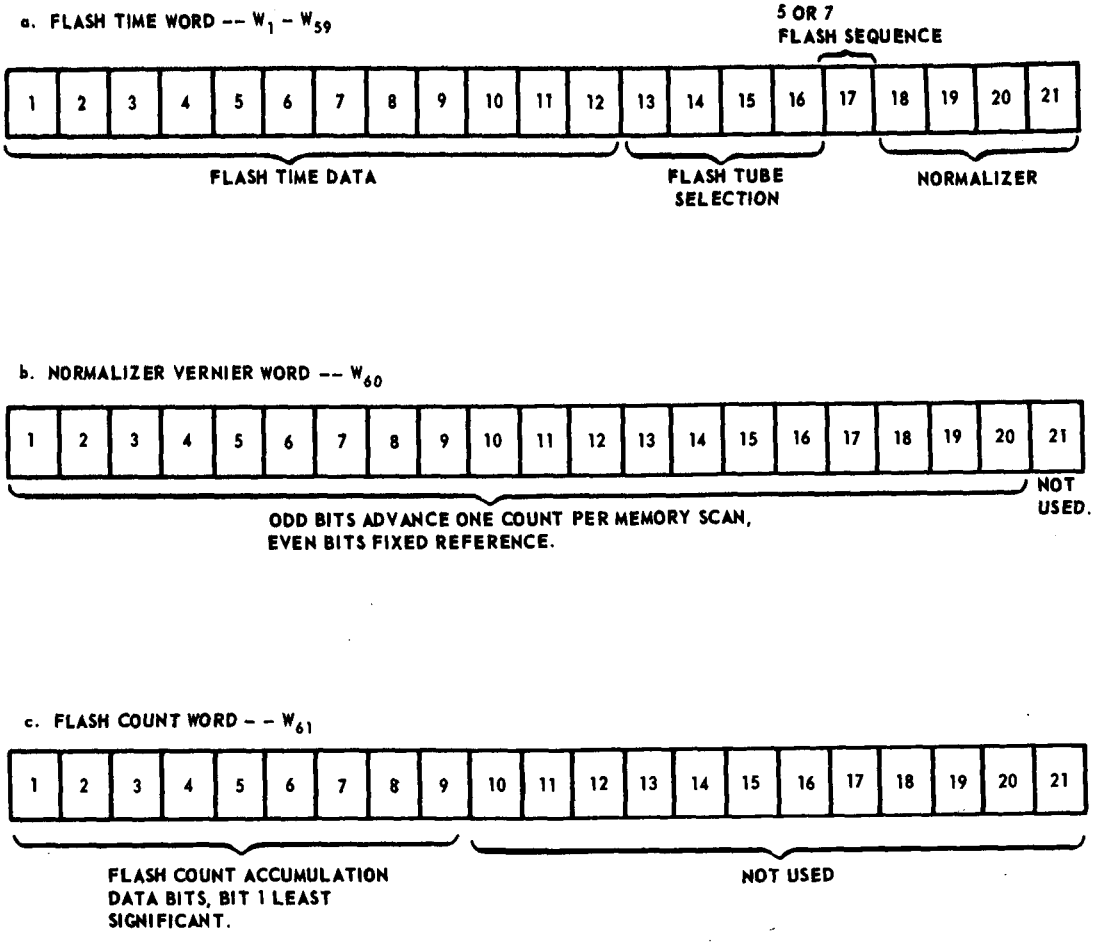

Fig. 5 MEMORY WORD FORMAT

Word 60	Normalizer Vernier Word (Figure 5B) -- Provides a fine time correction beyond that provided by the normalizer bits for the flash time word. The even bits of this word form a fixed reference group, while odd bits form a variable group (refer to Section III-B.
Word 61	Flash Count Word (Figure 5C) -- Accumulates the total number of light flashes which have occurred since the last injection. This word uses only the first 9 bits, with bit 1 as the least significant.
Words 62 to 65	Not presently used.

The entire contents of the 1365 bit memory is serially read out and restored, with modifications, once every minute. The flash time words are each modified by adding binary one to the number contained in the first twelve bits of the word, while the rest of the word is restored unchanged. If the first twelve bits are all "ones" a flash sequence will be initiated with the first flash occurring at the next minute marker. The normalizer vernier word has binary one added to the number contained in the odd bits, while the even bits are restored unchanged. The flash count word is serially added with the flash count accumulated during the previous minute before restoration to the memory.

B. Injection Sequence

The injection sequence is conducted by the satellite memory ground station GEMTU (Geodetic Explorer Memory Terminal Unit). GEMTU is designed to perform as the ground terminal of the two-way data link with the satellite optical memory and control unit. In performing its task GEMTU must transmit the 1365 bit injection message and monitor both the pre-load and post-load readouts of the memory. It also must be capable of maintaining close synchronization with UT2 and produce hard copy records of the data received and transmitted.

At the preselected injection time a load command is transmitted by GEMTU thereby causing the encoded memory data to appear as modulation on one of the TM subcarriers. Beginning at the next minute marker this data is decoded, error checked and recorded. At the second minute marker GEMTU modulates the command transmitter with the encoded memory injection message. At the third minute marker GEMTU again decodes, error checks and records the memory readout data. Each GEMTU injection tape consists essentially of three parts: the first is an estimate of what the memory contents should be based upon the last message and the elapsed time since injection; two, the new injection message and three a repeat of the new injection message. The first and third parts are thus used to check for proper memory operation.

It should be noted that injection into the memory is a synchronous operation which in no way disturbs satellite timing. If, however, it is desired to reset the clock epoch GEMTU would transmit a data "1" tone upon completion of the load command. At the next 4 second clock pulse the memory clock will stop and will be inhibited until the tone is released. The memory will then proceed through the previously described load cycle.

III. LOGIC DESIGN

The GEOS Optical Memory and Control Unit consists of the following functional sub-units: 1365 bit magnetic core memory with time and drive circuits, synchronous clock divider, data handling and mode control, light flash control and monitor. These sub-units are described in the following sections:

A. Magnetic Core Memory (Figure 6)

The GEOS memory consists of a 1365 bit magnetic core memory operated in the coincident current mode with addressing circuits which cause it to scan serially as a sequential buffer. Since the memory plane axes are mutually prime (21 x 65) a complete diagonal scan is accomplished for each one minute cycle.

Each axis of the core plane is driven by a magnetic coincidence switch matrix (CS). The CS outputs drive the half-select current pulses to the individual memory lines. The drive for each CS is obtained from square loop magnetic core blocking oscillator drivers, connected in a ring counter fashion. Since each axis of each CS is also mutually prime (3 x 7 and 5 x 13) the blocking oscillator drivers will cause the CS to be diagonally scanned. The transistor and square loop core characteristics determine the half-select pulse width. Constant current stabilizers used for driving the blocking oscillator drivers, accurately regulate the half-select current amplitude.

The memory timing (Figure 7) is determined by the basic 22.750 cps clock. Internal timing circuits turn on the Y axis CS 2.5 μs after the clock pulse, and the X axis 1.5 μs thereafter. Since the CS output pulses are 350 ma in magnitude, this results in a coincident current of 700 ma for a duration of 2.5 μs. Therefore each memory bit is read approximately 4 μs after the 22.750 cps clock pulse.

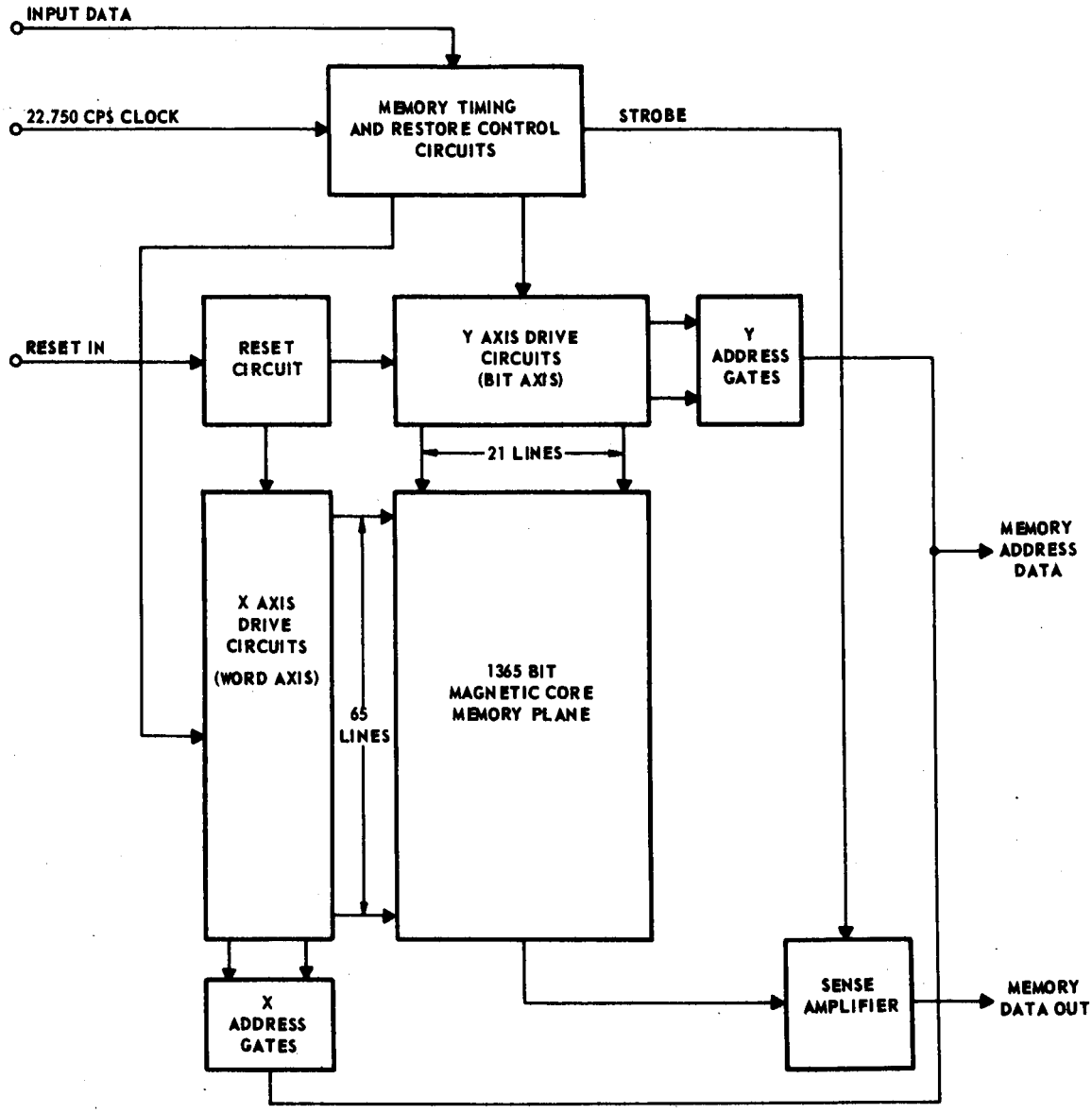

Fig. 6 MEMORY BLOCK DIAGRAM

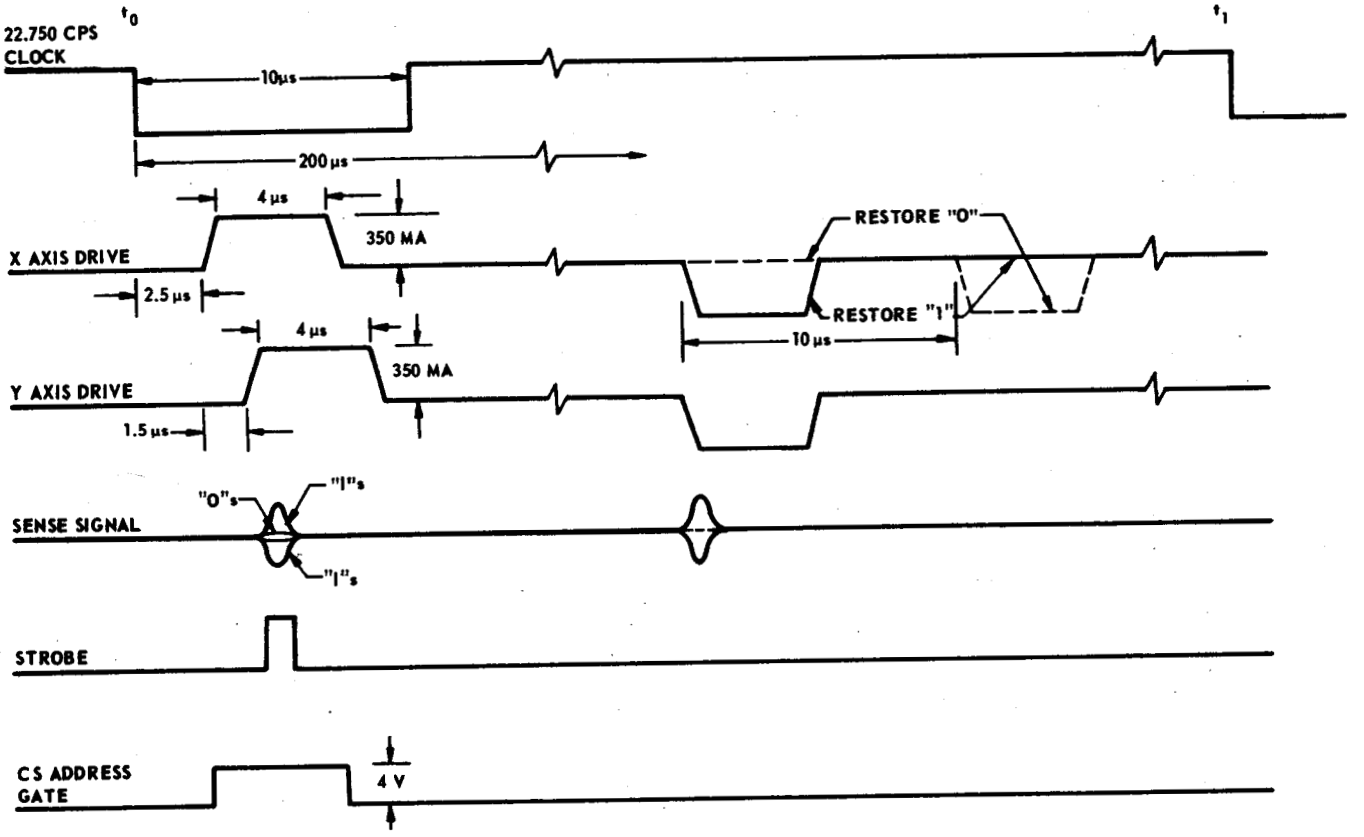

Fig. 7 MEMORY TIMING DIAGRAM

The sense amplifier rectifies and amplifies the read signal to useful logic levels. A gate pulse "strobes" the sense amplifier at the proper time to protect against unwanted noises or shuttle pulses on the sense lines.

The restore cycle is initiated approximately 200 μs after each read cycle. The memory restore operation is controlled by the input data. If a logical "1" is to be restored in the memory, both the X and Y axes are restored simultaneously. If a logical "0" is to be restored, the Y axis is first restored and 10 μs later the X axis is restored.

The reset circuit is necessary to set the memory address to word 1 bit 1. This operation would normally be done only when the system clock is reset.

Individual logic gates driven by the X CS and Y CS are used to provide memory address data (Figure 8) to the control logic. These gates are diode transistor integrated circuits which sense the CS current through a 10 ohm resistor. A typical CS gate output will be 4 μs wide and 4 volts in amplitude.

B. Clock Divider (Figure 9)

All timing signals in the GEOS Memory Optical Unit are referenced to the buffered 5MC-50ppm crystal oscillator output. The oscillator sinewave output is first amplified and shaped into a pulse train clock signal for the 49:1 shift register divider. The output of the 49:1 divider (102.04 kc nominal) is passed through the clock control and delete circuit where it is normalized and buffered. This normalized and buffered signal is then used to clock a 4485:1 (23 x 5 x 39) shift-register divider to generate the two phase memory data bit clock at 1365 pulse/min. The $\phi 1$ bit clock is then further divided 91:1 (7 x 13) in a shift-register divider to provide the 15 pulse/minute clock for use by the optical system.

Word No.	Bit 1		Bit 21		Word No.	Bit 1		Bit 21	
	X-Axis	Y Axis	X-Axis	Y-Axis		X-Axis	Y Axis	X-Axis	Y-Axis
1	1	1	21	21	34	44	1	64	21
2	22	1	42	21	35	65	1	20	21
3	43	1	63	21	36	21	1	41	21
4	64	1	19	21	37	42	1	62	21
5	20	1	40	21	38	63	1	18	21
6	41	1	61	21	39	19	1	39	21
7	62	1	17	21	40	40	1	60	21
8	18	1	38	21	41	61	1	16	21
9	39	1	59	21	42	17	1	37	21
10	60	1	15	21	43	38	1	58	21
11	16	1	36	21	44	59	1	14	21
12	37	1	57	21	45	15	1	35	21
13	58	1	13	21	46	36	1	56	21
14	14	1	34	21	47	57	1	12	21
15	35	1	55	21	48	13	1	33	21
16	56	1	11	21	49	34	1	54	21
17	12	1	32	21	50	55	1	10	21
18	33	1	53	21	51	11	1	31	21
19	54	1	9	21	52	32	1	52	-21
20	10	1	30	21	53	53	1	8	21
21	31	1	51	21	54	9	1	29	21
22	52	1	7	21	55	30	1	50	21
23	8	1	28	21	56	51	1	6	21
24	29	1	49	21	57	7	1	27	21
25	50	1	5	21	58	28	1	48	21
26	6	1	26	21	59	49	1	4	21
27	27	1	47	21	60	5	1	25	21
28	48	1	3	21	61	26	1	46	21
29	4	1	24	21	62	47	1	2	21
30	25	1	45	21	63	3	1	23	21
31	46	1	1	21	64	24	1	44	21
32	2	1	22	21	65	45	1	65	21
33	23	1	43	21					

Figure 8. Memory Address Allocation

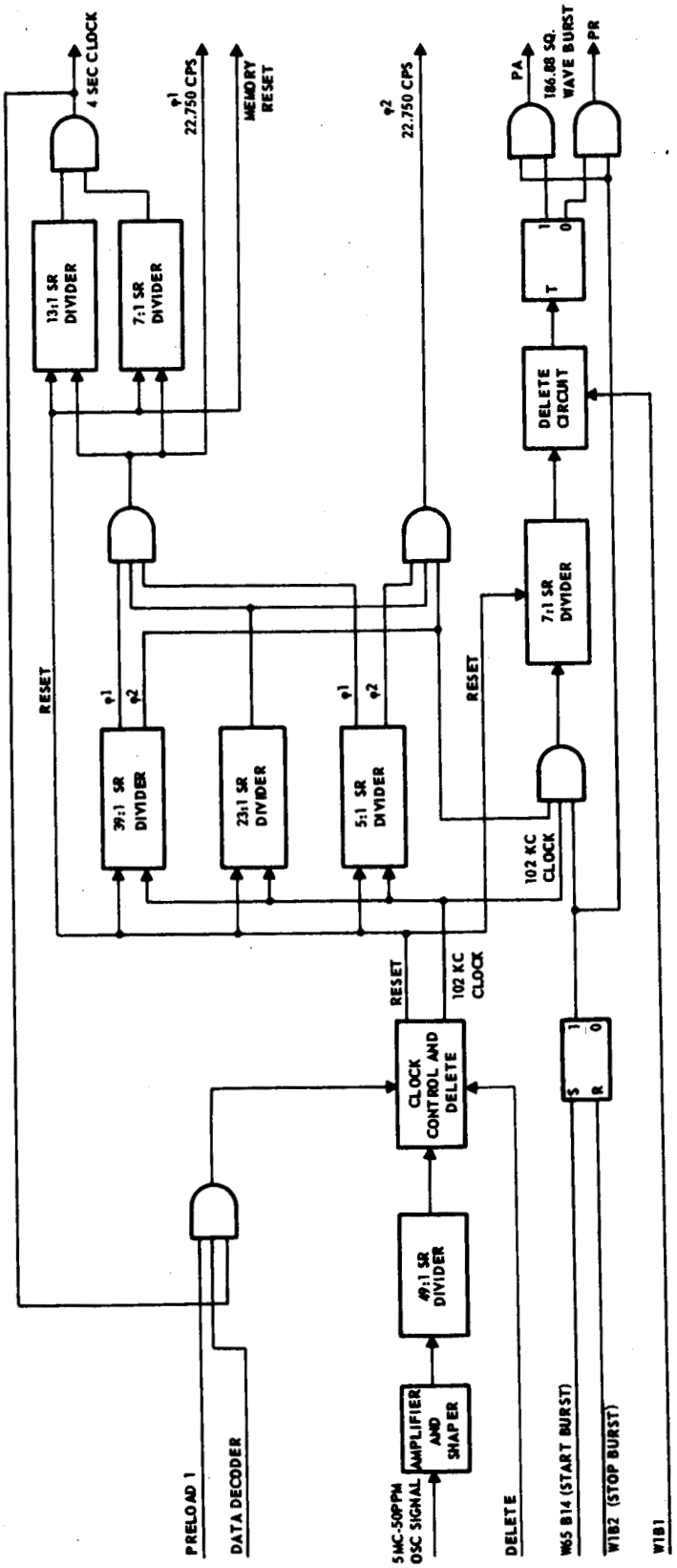

Fig. 9 CLOCK DIVIDER, SIMPLIFIED LOGIC DIAGRAM

The 4485:1 divider which provides the data bit clock consists of three parallel synchronous shift-registers, each with a feed-back loop. The feedback loop is such that each register cycles through a fixed series of states and by decoding one particular state a frequency division by the cycle length is achieved. Since 5, 23 and 39 are mutually prime and the shift-registers are clocked in parallel, feeding one decoded state of each register to an AND gate results in a division of the clock by 5 x 23 x 39 (4485). The two phases of the bit clock are achieved by decoding one state of the 5:1 and 39:1 dividers for $\phi 1$ and another state for $\phi 2$. Each phase of the bit clock consists of a negative going 9.8 μs wide pulse every 43.956 MS, with the $\phi 1$ clock occurring 30.207 MS prior to the $\phi 2$ clock.

The 15 pulse/minute clock is obtained by dividing the $\phi 1$ clock by 91:1 in a divider consisting of a 7:1 and a 13:1 shift-register divider similar to that used in the 4485:1 divider. One state of each divider is decoded and fed to an AND gate, since 7 and 13 are mutually prime they will both be in the decoded state once every 91 pulses (7 x 13). The 15 pulse/minute clock consists of a positive going 9.8 μs wide pulse.

The minute marker burst (Figure 10) is derived by gating the 39:1 divider $\phi 2$ output signal into a 7:1 shift register divider which in turn drives a toggle flip-flop at the marker burst frequency of 186.8786 cps $\pm$ .0036[1] cps. The marker is initiated at memory time W65B14 (word 65, bit 14) and ends at W1B2 with a phase reversal occurring just after W1B1. There are 66 full cycles prior to the phase reversal and 8 cycles thereafter. The phase reversal is achieved by deleting the first pulse out of the 7:1 divider after W1B1. The time delay between W1B1 (the satellite internal one minute mark) and the phase reversal is $1540.1 \begin{smallmatrix}+8.4\\-1.4\end{smallmatrix}$ μs for a properly normalized 5MC-50ppm $\pm$ 19.2ppm oscillator. In measuring timing the following formula must be used to determine the time of occurrence of W1B1:

[1]NOTE: In all time and frequency calculations the figure quoted is for an oscillator exactly at 5MC-50ppm, with the $\pm$ limits taken at 5MC-69.2ppm or 5MC-30.8ppm which are the time normalizer range limits.

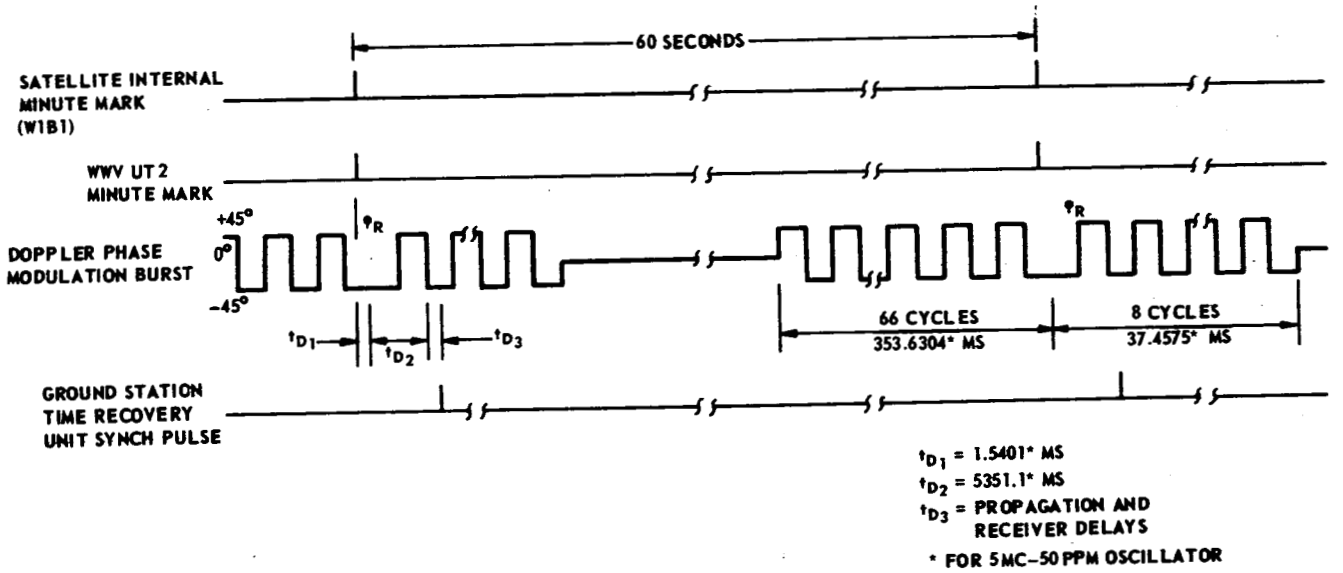

Fig. 10 GEOS TIME MARKER

$$T_{W1B1} = t_{sync} - (t_{D_1} + t_{D_2} + t_{D_3})$$

where

t_{sync} is the measured time of synchronization pulse occurrence as determined by the time recovery unit.

t_{D_1} is the memory internal delay of $1540.1 \begin{smallmatrix}+8.4\\-1.4\end{smallmatrix}$ μs.

t_{D_2} is transmitter and receiver equipment delay + one cycle of the marker (5351.1 ± 0.1 μs).

t_{D_3} is signal propagation delay.

In order to maintain accurate satellite timing and to remove the effect of integrated timing errors a time normalizer capability is provided. The time normalizer consists of a pulse deletion circuit on the output of the 49:1 divider and a decision circuit. Upon each command of the decision circuit a single pulse is deleted from the output pulse train of the 49:1 divider. Thus the period of all timing signals is increased by a nominal 9.8 μsec per deletion command.

The time normalizer correction data upon which the time decision circuit operates is updated and stored in the memory after each injection. This data is supplied in two forms; bits 18 through 21 of the 59 flash time words (236 bits) and the even bits of the normalizer vernier word (10 bits). For each logic level one bit stored in the normalizer portion of the flash time words a single pulse is deleted from the output pulse train of the 49:1 divider. Thus the maximum number of constant deletion commands is 236 or a variation of 37.4 ppm (nominal) may be achieved. The formula for determining the required number of normalizer bits is:

$$N = \frac{60\ f_{act}}{49} - 4485 \times 1365 \qquad f_{act} = \text{actual measured oscillator frequency in cps}$$

The result of the above equation is rounded off to the next lower integer and this number of deletion bits is evenly distributed in the 236 slots available.

The normalizer vernier word serves to remove residual integrated time error by providing a fine time adjustment. The first twenty bits (bit 21 is not used) in the normalizer vernier word are divided into two groups of ten; the odd bits forming a variable group, the even bits forming a fixed reference group. The fixed reference bits are determined by the fractional remainder after the constant normalizer bits are determined. The reference normalizer vernier group is the binary fraction equivalent of the normalizer bit remainder. The odd bits are initially all zeros and are advanced by one count for each memory scan. A deletion command is generated when a carry is stored and the next even bit is a one.

The following is a sample calculation:

$$N = \frac{60 \times 4{,}999{,}750}{49} - 4485 \times 1365 \qquad f_{actual} = 4{,}999{,}750 \text{ cps}$$

$$= 117.85645$$

N_c = 117 constant normalizer bits

N_r = 0.85645 remained

Thus the 117 constant normalizer one bits are evenly distributed in the 236 slots available and the even fixed reference bits of the normalizer vernier word are 1101101101.

Using the above time normalization method the one minute markers will be transmitted within ± (50 μs + measurement error + oscillator drift in 24 hours) of the UT2 minute markers. With after the fact calculations a correction factor can be generated

on a minute by minute basis for correction to ± (10 μs + measurement error + oscillator drift in 24 hours). Variation in the time interval between the 15 pulse/minute clocks will not exceed ±157 μs during a flash sequence. The first 15 pulse/minute clock of each minute will always occur coincident with W1B1 (word 1, bit 1). Again the variation in time between 15 pulse/minute pulses can be calculated and corrected for.

Since the normalizer vernier correction varies minute by minute predictable time errors will occur. A correction factor can be calculated to reduce the ±50 μsec maximum error caused by this factor. In order to make the calculation the following parameters are necessary:

f_{actual}	Actual oscillator frequency.
N_K	Number of constant normalizer bits.
N_{v_i}	Number of vernier normalizer bits deleted during the i^{th} minute after the completion of the load one minute interval.
E_o	Initial corrected time error at the completion of the load one minute interval.

The time error between the $i - 1^{th}$ and i^{th} minute markers is then given by

$$\epsilon_i = \left\{ \frac{49}{f_{actual}} \left[4485 \times 1365 + N_K + N_{v_i} \right] - 60 \right\} \text{ usec for } i \geq 1$$

$$= E_o \text{ for } i = 0$$

The procedure can be simplified by noting that a constant error in ϵ_i is carried through all calculations since N_K is always fixed. Thus we have

$$\epsilon_i = \epsilon_K + \frac{49}{f_{actual}} N_{v_i} \quad \mu s \text{ for } i \geq 1$$

$$= E_0 \text{ for } i = 0$$

where

$$\epsilon_K = \left[\frac{49}{f_{actual}} (4485 \times 1365 + N_K) - 60 \right] \mu sec$$

The integrated error at M minutes after the completion of the one minute load interval is equal to the algebraic sum of the individual minute marker errors or

$$E_M = E_0 + \sum_{i=1}^{i=M} \epsilon_i = E_0 + M\epsilon_K + \frac{49}{f_{act}} \sum_{L=1}^{M} Nv_i$$

The following is a sample calculation

f_{actual} = 4,999,750.00 cps

N_K = 117

E_0 = +15.90 μs

M = 8

N_{v_1} = 0

N_{v_2} = 1

N_{v_3} = 0

N_{v_4} = 2

N_{v_5} = 0

N_{v_6} = 1

N_{v_7} = 0

N_{v_8} = 2

etc.

$$\epsilon_K = \left[\frac{49}{4,999,750} (4485 \times 1365 + 117) - 60 \right] = -8.43 \mu s$$

The total integrated error at the end of minute 8 is equal to:

$$E_M = 15.90 + 8(-8.43) + \frac{49}{4999750} \times 6 = +7.26 \mu s$$

The clock dividers and the memory coincidence switches may be stopped and reset to W1B1 to synchronize with UT. This is accomplished by the ground station transmitting and holding a data one tone during the first preload readout. In order to provide a small time window to decrease susceptibility to spurious reset commands the input to the reset circuit is strobed by the 9.8 μs wide 15 pulse/min. (4 second clock) pulse train. Thus the clock is liable to reset only during these pulses. The clock divider will remain reset until the data one tone is released; the satellite will then transmit a full preload memory readout preparatory to load. During the preload and load scans for a time change injection the normalizer function is inhibited.

C. Data Handling and Mode Control (Figures 11 and 12)

The data handling and mode control unit performs three main functions; it receives serial memory data along with address information and processes this data for restoration to the memory, it provides the proper gating signals for the light flash control, and it controls the mode of memory and control unit operation. Operation is best described by starting at the beginning of a memory scan in the normal mode of operation and by assuming all flip-flops are in the reset condition. Address data from the memory is supplied in the form of short pulses (4 μs nominal) coincident with memory data for that bit. Thus the reference W1B1 refers to the address pulse coincident with word 1, bit 1.

The data in the first 59 21-bit words is serially distributed by the flash time word data distributor as follows: the first 12 bits (B1 - B12) are fed to the full adder, the next five bits (B13 - B17) are restored unchanged to the memory, and the next four bits (B18 - B21) are restored unchanged to the memory as well as used as normalizer bits. At W1B1 the flash time word gate FF1 is set, thereby enabling the flash time word data distributor. Coincident with the first bit of every flash time word, a logic level one pulse is applied to the Y input of the full

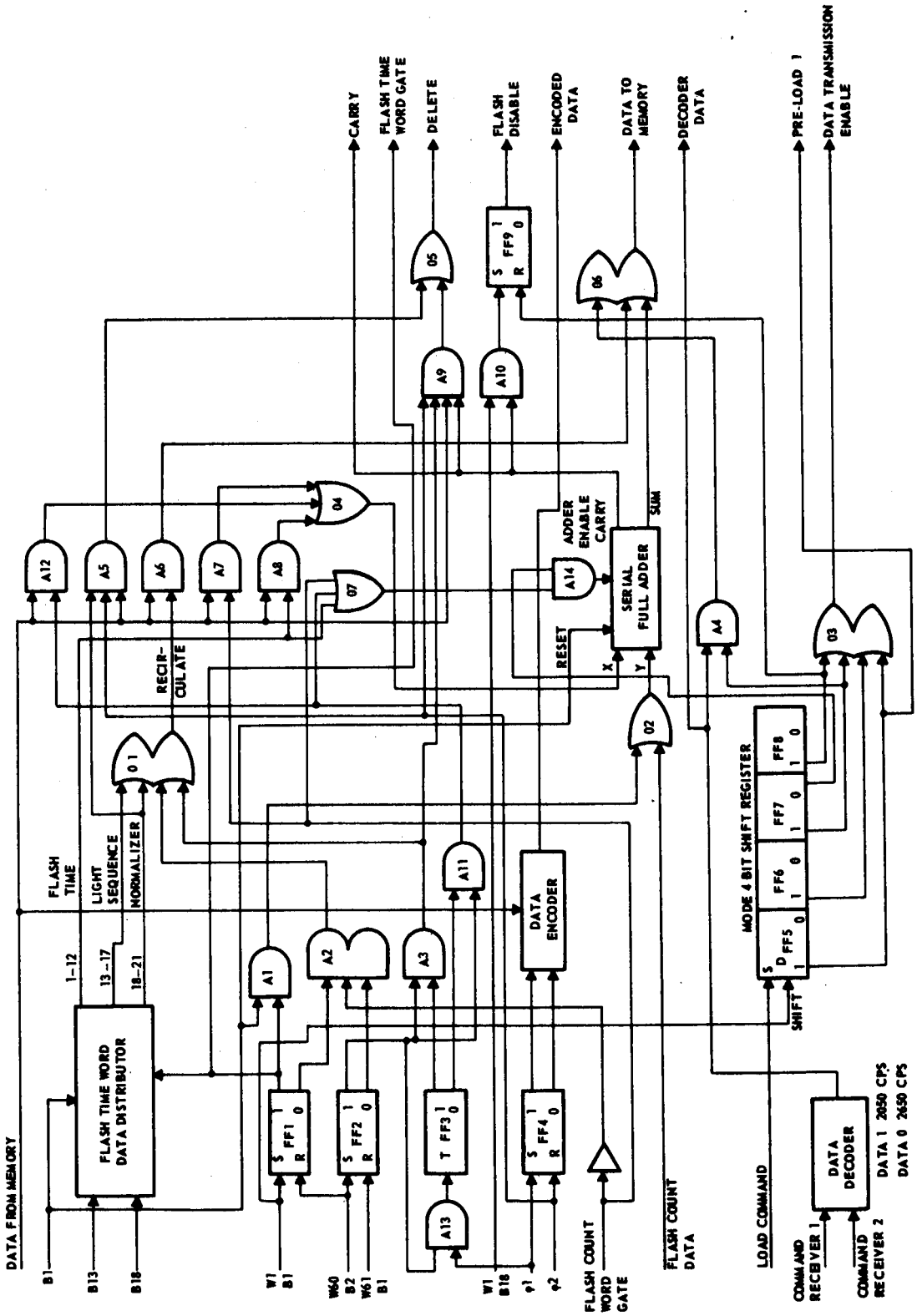

Fig. 11 DATA HANDLING AND MODE CONTROL, SIMPLIFIED LOGIC DIAGRAM

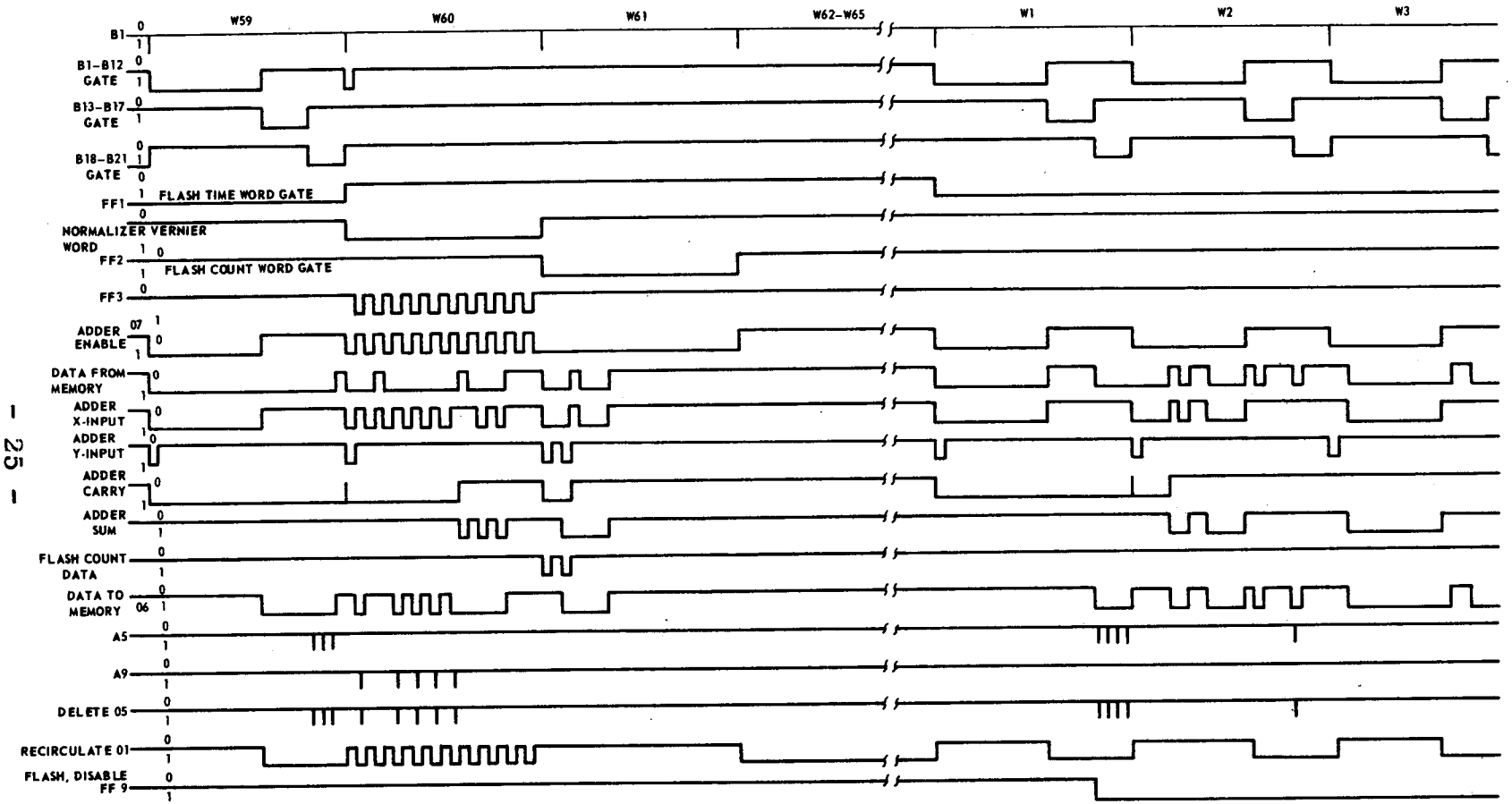

Fig. 12 DATA HANDLING AND MODE CONTROL, SIMPLIFIED TIMING DIAGRAM

adder via A1 and 02. Since A8 is enabled to the data for bits 1 - 12, memory data bits 1 - 12 are serially applied to the full adder X input via A8 and 04. The sum output of the X and Y signals is then restored to the memory via 06. This has the effect of adding binary one to the least significant bit (B1) of each flash time word for each one minute scan. If a carry logic level one is stored after B12, this state is maintained for the duration of that word independent of the data in bits 13 through 21. The carry storage is reset at B1 of each word. Bits 13 - 21 are then restored to the memory unaltered; this is accomplished by 01 enabling A6 to the data line and thereby feeding the data to the memory via 06. The delete commands for the time normalizer are generated by a data one in bit positions B18 - B21, gate A5 passes the data in these bit positions to 05 and then to the time normalizer circuit.

The normalizer vernier word (W60) consists of a fixed reference group (refer to IIA) made up of the even bits, and a variable group made up of the odd bits. The variable group is incremented by binary one for each memory scan just as the first twelve bits of the flash time words are, while the reference group is restored unchanged to the memory. The addition of binary one to the first bit is accomplished in the manner previously described. At bit 2 of W60, however, FF1 is reset with FF2 being set, thus allowing toggle flip-flop FF3 to control the data flow. On even bits FF3 is set and the even bit data is restored unchanged to the memory by A3 enabling A6 via 01. On odd bits FF3 is reset and the odd bit data is fed to the X line of the full adder by A11 enabling A12. The adder is enabled only for the odd bits of W60 by A11 via 07. If a carry logic level one is generated during an odd bit and if the next even bit is a one then delete command is generated via A9 and 05.

At W61B1 FF2 is reset and the flash count word gate is generated by the light flash monitor and control unit. For the duration of the

flash count word gate the memory output is fed to the full adder X input via A7 and 04, while flash count data is supplied to the Y input, with the adder is enabled via 07. This causes the new flash count data to be added to that already accumulated. The flash count word gate is removed at W62B1 and the data in words 62 through 65 is restored unchanged to the memory.

The data line from the memory is connected to the data encoder along with the output of FF4. The data encoder takes these signals and provides the proper voltage levels for the RZ encoded data.

The flash disable circuit, made up of A10 and FF9, is triggered by a carry logic level one during W1B18. This can only occur when W1 has caused a flash sequence to be initiated. The disable is removed during the post load readout of an injection.

Upon receipt of a properly encoded load command from the ground station an injection sequence is initiated. The injection sequence, taking from three to four minutes, consists of the following: partial to full preload readout 1, full preload readout 2, load, full post load readout. The decoded load command sets FF5 storing 1000 in the mode SR, and denoting a preload 1 readout. During the preload 1 readout the Memory and Control Unit clock may be reset as described in IIIB. At W1B1 (the minute mark UT) the SR shifts right one bit and stores 0100 denoting a preload 2 readout. The SR again shifts right one bit at the next minute mark thus storing 0010 and going into the load scan, where new memory data is injected. During the load scan the output of the data decoder is fed to the memory restore circuit via A4. At the completion of the load scan the SR again shifts, thus storing 0001, denoting a post-load readout. The end of this one minute scan marks the conclusion of an injection sequence. Throughout this sequence the SR enables data transmission to the ground by controlling the signal into one of the TM

subcarrier oscillators via 03. The bipolar RZ encoded data signal then modulates the subcarrier oscillator for the entire load operation.

D. Flash Control and Monitor (Figures 13 and 14)

The flash control and monitor is the interface buffer between the Optical Sequence Controller and the Memory and Control Unit. It controls when and which flash assemblies are to be flashed and accumulates the actual number of flashes that have taken place.

When the first 12 bits of a flash time word are all logic level one a carry logic level one is stored for the duration of that word and a flash sequence is initiated, provided three initial conditions are met. These are: first, that no flash sequence be in process; second, that the flash inhibit circuit has not been triggered; third, that a preload 1 readout not be in progress. If a flash sequence is initiated, the contents of memory bits 13, 14, 15 and 16 for the word initiating the sequence are stored as flash tube complement data in the four flip-flop buffer register consisting of FF1-FF4. A logic level 1 in FF1, FF2, FF3 or FF4 causes its associated buffer circuit to generate a +10V (nominal) gate level to select a flash tube assembly for that sequence. Bit 17 of the initiating word sets FF5, the seven flash gate, if it is a logic level one, or FF6, the five flash gate, if it is a logic level zero. Setting of either FF5 or FF6 inhibits the input of new data into the buffer register until the end of the sequence, enables gate A3 for sequence gate generation and gate A1 for a seven flash sequence reset or gate A2 for a five flash sequence reset. At 4.835 seconds (W61B3) before the UT one minute mark, FF8 is set via A3, thus causing BF5 to generate the sequence gate signal to allow the sequence controller to respond to the 15 pulse/minute clock. The first 15 pulse/minute clock occurring within the sequence gate does not trigger the flash tubes. At 16 seconds after the UT minute mark (W18B8) for a five flash sequence or at 24 seconds after the UT minutes mark (W27B1) for a seven flash

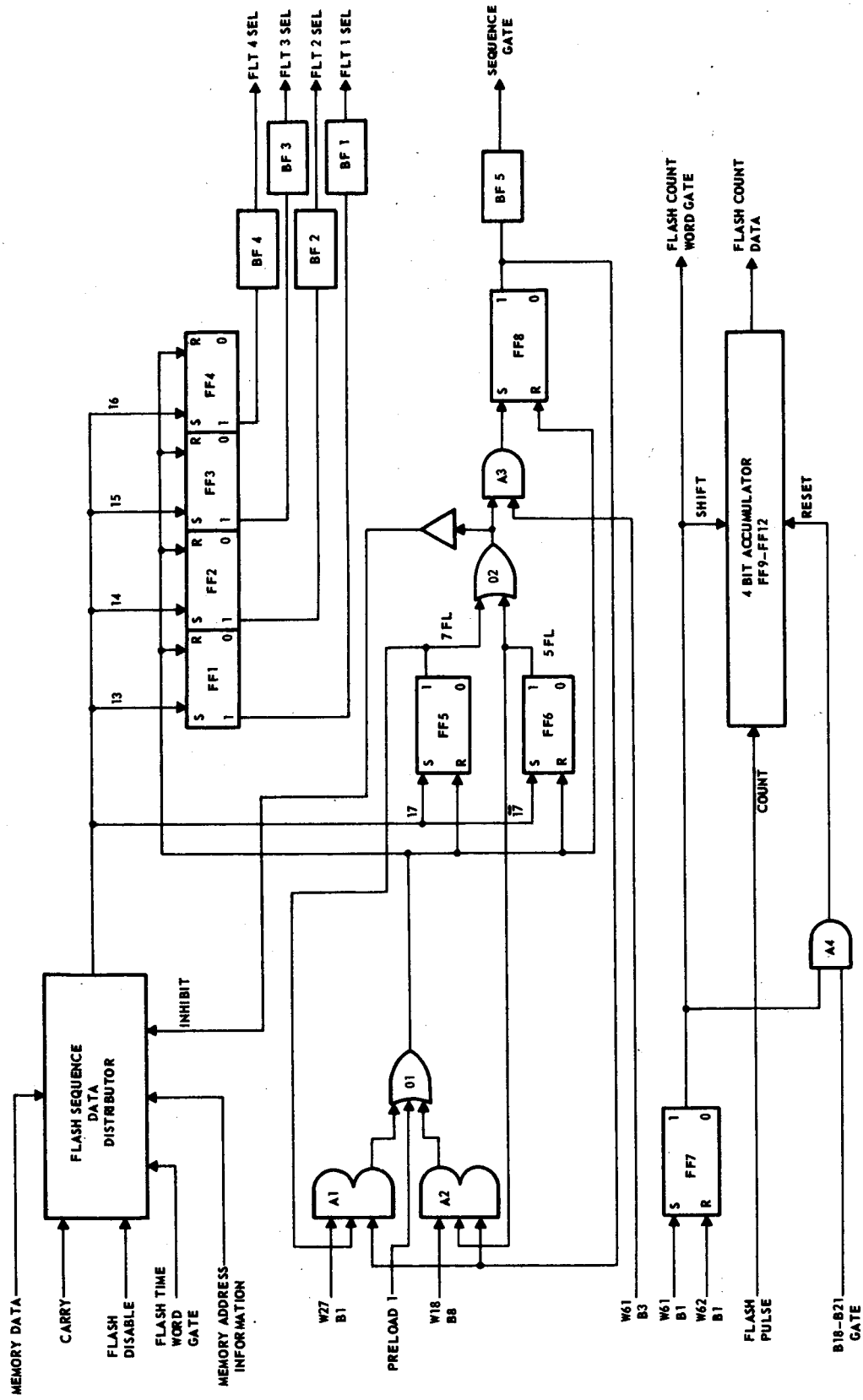

Fig. 13 FLASH MONITOR AND CONTROL UNIT, SIMPLIFIED LOGIC DIAGRAM

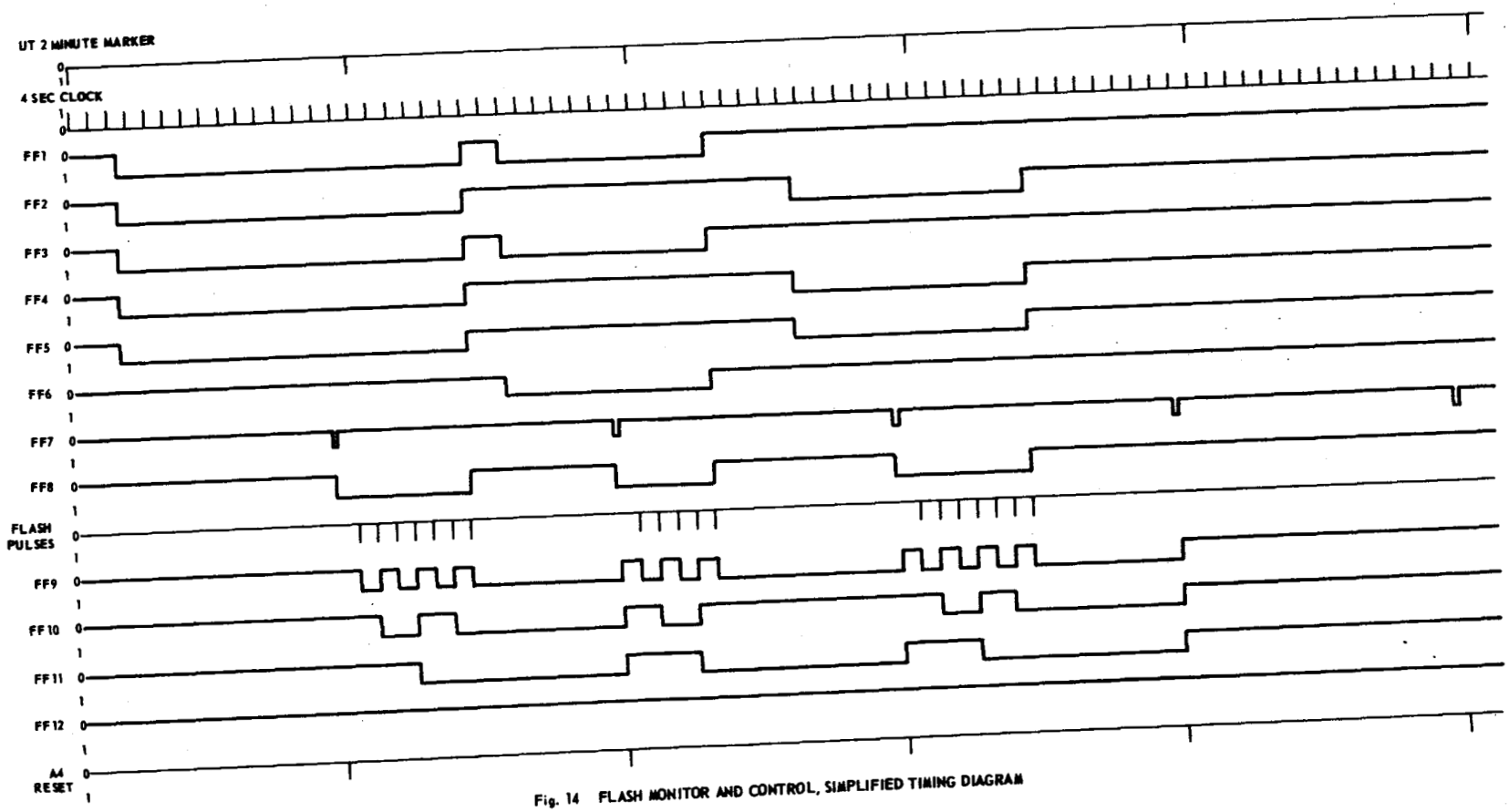

Fig. 14 FLASH MONITOR AND CONTROL, SIMPLIFIED TIMING DIAGRAM

sequence FF1-FF8 are reset via O1 and the flash sequence is complete. To guard against a hang-up state in the flash control flip-flops when power is first turned on, during a memory injection sequence FF1-FF8 are reset by the preload 1 gate signal.

It should be noted that two restrictions are placed on flash time word usage. First, if two or more light flashes are to occur spaced at the minimum time interval of one minute apart, the flash time words used for the second and subsequent light flashes must be between words 32 and 59 inclusive. This is due to the fact that during word times 1 to 31 of a flash sequence the flash control may be in use and is not available for read-in of new data on the next flash sequence. Second, that word 1 must be used as the last flash sequence of the memory load. After full usage of the injected message initiation of further light flashes is inhibited. This inhibit signal is generated by initiation of a flash sequence by word 1. Reloading of the memory removes the light flash sequence inhibit signal.

Each time a flash tube or group of flash tubes is flashed a pulse is generated by flash sensors installed near the tubes. This pulse is used to increment the four-bit binary accumulator consisting of FF9-12. During word 61, the data in the accumulator is shifted out and added to the data already in word 61. Thus during each scan the data in the memory is updated to account for light flashes during that scan. Although the longest sequence initiated per scan is seven flashes, a four bit accumulator is used to provide sufficient counting capacity to monitor light flashes in the case of malfunction.

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