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HANDBOOK
FOR
COMPUTERIZED RELIABILITY ANALYSIS METHOD (CRAM)

October 1965

Prepared for Use on
Contract NAS8-11087
National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama

ARINC RESEARCH CORPORATION

HANDBOOK
for
COMPUTERIZED RELIABILITY ANALYSIS METHOD
(CRAM)

October 1965

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PREFACE

This instruction manual was written for personnel who are using, or anticipate using, the Computerized Reliability Analysis Method (CRAM). As stated in ARINC Research Corporation Monograph 11*, "...CRAM, the concept, is a method for analyzing reliability by the use of computers". Since CRAM is a reliability prediction method that does not use any mathematical concept that would not be used if the prediction were manually performed, this manual discusses only subjects that are pertinent to the computer program, not reliability theory.

The manual has four purposes:

(1) To explain CRAM as simply as possible

(2) To specify procedures, with examples, for originating the computer inputs in the required form

(3) To set forth some guidelines concerning the advantages of CRAM

(4) To present examples of CRAM's use on several projects

Accordingly, Section 1 contains a brief description of CRAM from the standpoint of the reliability engineer who is interested in using a computer facility for the qualitative or numerical solution of <u>complex</u> reliability functions. Its purpose is to state in general terms what CRAM is and does, and what is required from the engineer in the way of raw data inputs for a computer solution.

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* David E. Van Tijn, Description of the Computerized Reliability Analysis Method (CRAM), ARINC Research Publication 294-02-4-444, 13 November 1964.

The remaining sections give more detail as to certain aspects of CRAM programing preparations. The particular illustrations used have deliberately been kept simple so that both hand and computer calculations can be shown together in the text. Actually, such simple problems are more economically solved by manual procedures. However, the reader should always keep in mind what the situation might be if there were perhaps as many as 200 individual parts that involved 90 individual failure rates and up to 12 operating modes.

The final section of this manual takes into account that the reliability engineer must also be able to understand and interpret the computer's outputs, i.e., either the final output or an intermediate output at any point in the processing program. Accordingly, a detailed explanation of the three sequential CRAM programs is provided, including how the computer processes, its outputs, and how those outputs should be interpreted.

The appendixes provide a coding dictionary and details for certain special considerations such as relay calculations or time-dependent system configurations.

Reliability engineers associated with organizations that do not have the computer programs or tapes necessary to utilize CRAM may request copies by contacting ARINC Research Corporation, Annapolis Science Center, Annapolis, Maryland.

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GLOSSARY OF TERMS

Active redundancy. A system has active redundancy if it can perform its function in two or more separate ways, and if all of the equipment operates at the same time.

Acyclic. Without cycles (series-parallel).

And. An operation that simply adds two propositions together to make a new proposition (one entirely independent of any symbolic or syllogistic result). For example, the two separate propositions, "Socrates is a Greek," - "two is greater than one" are two propositions that, entirely independent of any apparent connectivity, can be joined by an "and" to yield the single proposition, "Socrates is a Greek, and two is greater than one." The new proposition, as a pure proposition, is then true if, and only if, both of the original propositions are true; and this is independent of any consideration as to whether a logically valid syllogism can be formed from them.

Application factor. Same as K factor.

Class (also element class or part class). The type of element named in a block on the reliability diagram, e.g., wire-wound or carbon film resistor, miniature relay or power contactor, or a specific type of diode.

Circuit. An electrical cycle, not necessarily maximal, in which only one element is repeated (see Cycle, electrical).

Conjunctive term. A term consisting of propositions connected only by ands.

Convenience block. A block on the reliability diagram that represents all of its predecessors. A convenience block may also represent an element, or it may be inserted in a line of the diagram.

Cutting, cut. An operation performed to convert the diagram of a feedback system into a tree diagram.

Cycle, electrical. Any group of elements, each of which is its own predecessor.

Designator. A symbol or number used as a name for an element represented by a block on a diagram.

Distinct circuits. Two circuits are distinct if at least one of them contains an element that is not in the other.

EDP. Electronic data processing.

Element (also element name or name). The smallest pieces of a system to be considered in a particular diagram. Also the entity (physical item or signal) whose name appears in a block on the reliability diagram, e.g. R21, K14, AMP2, SS4, SIG3. Elements may be subsystems, sub-subsystems, parts, or even parts of parts.

Element class. The type of part (or element) named in a block of the block diagram.

Entrance. An element of a cycle that has an immediate predecessor outside the cycle.

Exclusion. Permissible element modes are mentioned by exclusion when the modes which cause the system to fail are mentioned, each with an overbar; for example, $\overline{op}$, $\overline{sh}$ (not open, not short).

Exclusive or. A connective that makes a proposition out of two other propositions. The resultant proposition is true if either of the original propositions is true, but the original two propositions cannot both be true; e.g., "Two is greater than one or (exclusive) one is greater than two".

Exit. An element that has an immediate successor outside the cycle.

Failure-mode-and-effect analysis (FMEA). A listing of all element failure modes and the effects on system operation if they occur.

Feedback. Feedback occurs when, in a chain of elements, say A_0, ..., A_n, A_0, each element is its own predecessor.

Floating point. A way of writing numbers for use in computers. The numbers are written as a decimal fraction followed by a power of ten. For instance, 345.5 is written $345500\overset{+}{0}0\overset{+}{3}$, where the last two digits represent the exponent of the power of ten (3). The *sign* of the *number* is written over the eighth digit, the *sign* of the *exponent* over the tenth digit.

Header card. A card, used as part of the input to a computer program, which defines the format of the inputs, and which also contains the name of the system.

Inclusion. Permissible element operating modes are mentioned by *inclusion* when the modes that allow the system to function are mentioned; for example, op, ok.

Inclusive or. See *or*.

Junction Block. A block on a diagram with more than one immediate predecessor, i.e., a block where several branches join.

K factors. Those factors which are used to adjust the part failure rates to account for stresses and environmental conditions.

Maximal cycle. A cycle to which no other element can be added without destroying the cyclic property.

Mode (also *failure* mode or *operating* mode). The possible ways in which an element can operate or fail. For example, in a diode the *valid operating* modes *might* be: operating, not open, short, and arc. The valid *failure* modes might be: not operating, open, not shorted, not arc.

Multimode system. A system that can perform different functions or the same function at different levels of effectiveness. The functions or levels are called operating modes; and, in general a slightly different set of elements is required for operation in each mode. Hence, each mode requires a separate diagram.

Not Slct. Part of the computer symbolism that represents a block on a reliability diagram on the computer. It indicates whether the mentioned element operating modes are excluded or permitted.

Optional rule. The rule for constructing diagrams that covers the use of convenience blocks.

Or. An operation that makes a single proposition out of two other propositions and which is independent of any syllogistic implications, e.g., "Socrates is Greek or two is greater than one." The new proposition is true if either or both of the original propositions are true.

Part 1 program. This computer program accepts inputs that represent the blocks of a diagram, and it produces a propositional function that represents the conditions for system success.

Part 2 program. This computer program accepts the output of the Part 1 program, and it produces the expression for the system reliability in terms of element reliabilities.

Part 3 program. This computer program accepts the output of the Part 2 program, the element list, and the failure information table, and it produces the system reliability.

Path. A chain of elements, each of which is an immediate successor of the preceding one, and in which no element is repeated.

Piece parts. The smallest piece of equipment that can be replaced, e.g., a tube, a diode, a gear.

Predecessors. A block B on a diagram is a predecessor of another block C, if the path from B to the terminal block of the diagram passes through C.

Program deck. The cards that contain the computer program.

Propositional calculus. That part of symbolic logic which deals with statements. A statement is a declarative sentence, e.g., "Socrates is Greek", "Two is larger than one."

Propositional function. A proposition made up of simpler propositions and connectives, e.g., "Socrates is Greek and two is greater than one." And is a connective. The other connectives used are "or" and "either, or".

Reliability block diagram. A graphical representation of the conditions for successful system operation.

Series system. A system that operates correctly only if all the elements operate correctly.

Standby redundancy. A system has standby redundancy if it can perform its function in two or more separate ways, and if the equipment for one of these modes is not switched on until the equipment(s) for the other mode(s) has (have) failed.

System modes. See multimode system.

Tag. The part of the computer symbolism, which represents a diagram block on the computer, that mentions the element operating modes that are excluded (the number 1 entered in the Not Slot) or permitted (a zero entered in the Not Slot).

Terminal block. The last block on a reliability block diagram. It usually represents system success.

Tree diagram. A diagram in which each block has only a single successor (except the terminal block, which has none).

Utility routines. Computer programs that can be used to solve a wide variety of problems without requiring alteration of the program.

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1. WHAT CRAM IS

In simplest terms, CRAM is a computer program that is specially designed to eliminate the tedious and time-consuming effort of reliability calculation for complex systems.

More specifically, CRAM is a set of three computer programs that perform the following reliability calculations:

(1) CRAM Program 1 is able to take sequentially ordered information (that duplicates a reliability block diagram drawn to CRAM specifications) and process this information into a reliability formula, and at the same time automatically create the processing "instructions" for Program 2.

(2) CRAM Program 2 is the process whereby the computer expands (or reduces) the reliability formula so that it is capable of accepting numerical data. This is done in three discrete steps called PHASES 1, 2, and 3. It also creates the "instructions" necessary for itself to process Program 3, including all the variations different operating modes may impose.

(3) CRAM Program 3 is the process of final computation, and it results in one or more answers in the form of "numbers" for the system, its modes, and its subsystems.

Aside from the computer aspects, CRAM introduces no mathematical concepts that are not used in conventional reliability prediction methods, and it is assumed here that the reader is at least conversant with the conventional methods of predicting the reliability of complex systems.

Since CRAM is a method to analyze a system's reliability by the use of a computer, the data inputs to the computer must be in a specified form and so ordered that the computer correctly processes the data. Accordingly, this section will provide the reliability engineer with information as to the data and ordering instructions he must provide the data processing department.

1.1 The CRAM Computer Facility

Since the reliability engineer will not be required to operate or program the computer, or be responsible for the actual card-punching operation, it is sufficient at this juncture to remind him only of the following:

(1) A digital computer is a device that can perform certain mathematical operations, given the proper raw data and "instructions" as to which operations, and in which sequence it is to perform the operations.

(2) The raw data upon which the computer operates also has to be given to the computer and stored in the computer "memory" (sometimes called "storage"). This storage can be in the form of ordered IBM punch cards (in trays), or it can be in the form of similar information processed onto rapidly scannable magnetic tape.

(3) The actual sequence of mathematical operations that the computer performs also must be in the form of precise, step-by-step instructions. These "instructions" are also fed to the computer as an ordered set of punched cards.

1.2 CRAM Requirements

It is the reliability engineer's task to supply sufficiently detailed raw system and reliability information so that a data processing department can properly punch and order the input cards for the computer. These data can be supplied in the form of diagrams and tables (forms for the tables illustrated can be preprinted and filled in by the engineer). Essentially, the raw information the reliability engineer is required to supply consists of the following:

(1) An Element Table that lists all of the elements (or parts) of the system under consideration (see Figure 1-4 and Section 5)

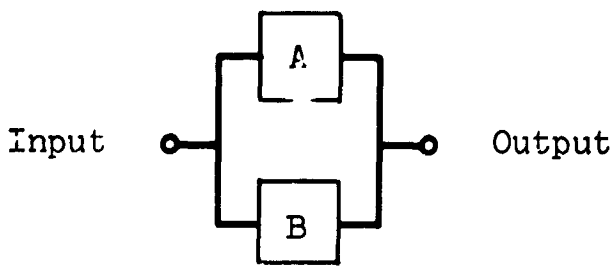
(2) A special CRAM Reliability Block Diagram, very similar to (and often simpler than) ordinary block diagrams (see Figures 1-1, 1-2, and 1-3, and Section 1.6)

(3) A Part-Class Failure Table that is sometimes able to replace the Element Table (see Figure 1-5 and Section 6)

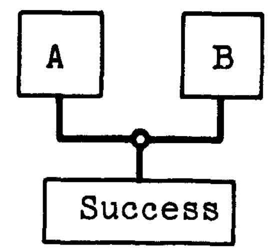
(4) A Mode Table (see Figure 3-1 and Section 3)

(5) Special instructions as to what readouts are required and any special computations desired (see Section 1.9)

The ordering of the above list also approximates the sequential steps the reliability engineer should take in preparing the data for the computer. The Part-Class Table, however, can often be prepared almost simultaneously with the Element Table. The exact preparation of the CRAM diagram and the three tables, moreover, is the chief element to be discussed in the remainder of this text.



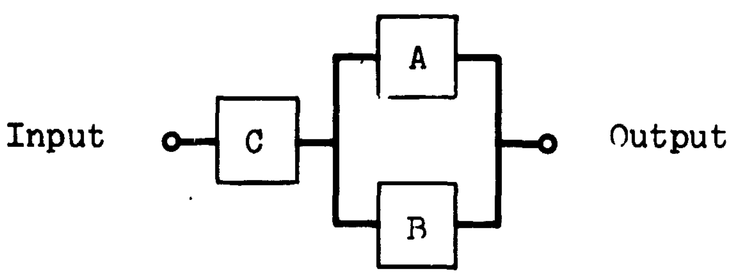
(a) Conventional Diagram



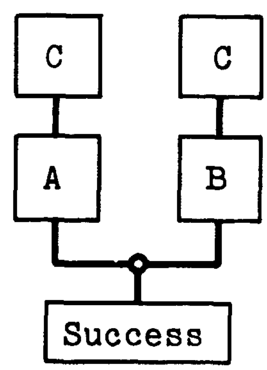
(b) CRAM Diagram

FIGURE 1-1

CONVENTIONAL AND CRAM DIAGRAMS
FOR A SIMPLE PARALLEL SYSTEM



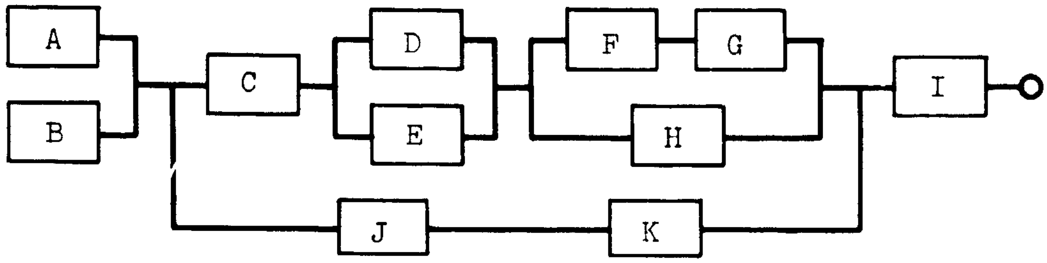
(a) Conventional Diagram



(b) CRAM Diagram

FIGURE 1-2

CONVENTIONAL AND CRAM DIAGRAMS
FOR A SIMPLE SERIES-PARALLEL SYSTEM



(a) Conventional Diagram

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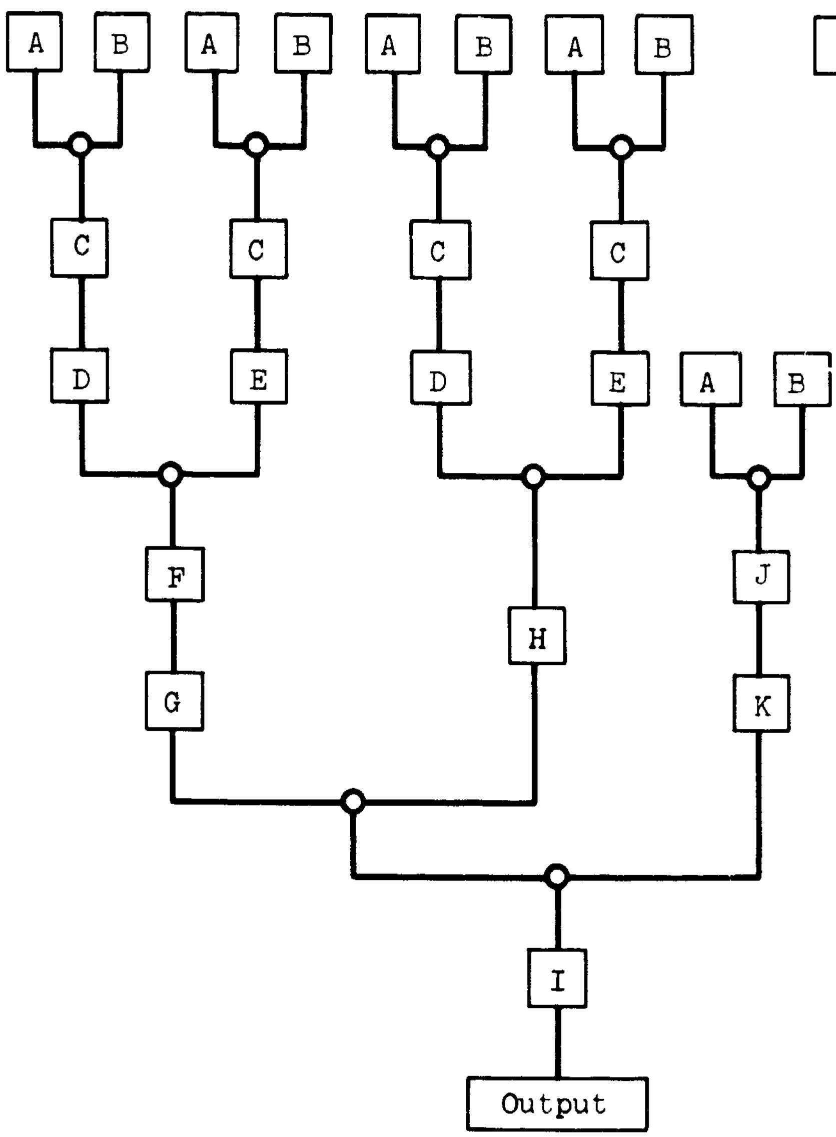
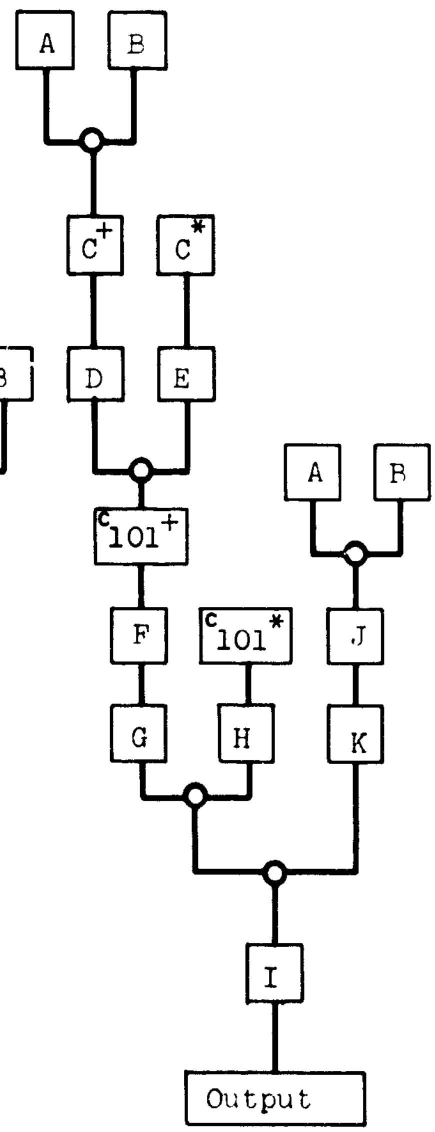


(b) CRAM Diagram
without Convenience Blocks



(c) CRAM Diagram
with Convenience Blocks

FIGURE 1-3

CONVENTIONAL AND CRAM DIAGRAMS FOR A REDUNDANT SYSTEM

System/Subsystem Description					
Diagram Name	Figure 1-3	No. of Elements on Table = 11	Checked	(initials)
Length of Element Name		Part-Classes Checked		(initials)

Class	Element	Class	Element	Class	Element
A	A				
B	B				
C	C				
D	D				
E	E				
F	F				
G	G				
H	H				
I	I				
J	J				
K	K				

OP-80, 3-8-65

FIGURE 1-4

TITLE: ELEMENT TABLE FOR FIGURE 1-3

p.__of__

System/Subsystem Description		
Use With Table No.	Diagram Name-Figure 1-3	No. of Operating Modes (Less OK) = 1
Checked for Completeness (initials)		Numbers Checked (initials)

Operating Modes	Designation	NG														
	No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Class	Mode No.	P/ Blank	Probability/ Rate	K_1	K_2	K_3 †	t
A	1						
B	1						
C	1						
D	1						
E	1						
F	1						
G	1						
H	1						
I	1						
J	1						
K	1						

† Any number of K factors may be shown.

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FIGURE 1-5

PART-CLASS FAILURE INFORMATION TABLE

1.3 Element Names and the Element Table

Within the CRAM program, an element is designated by a five-character "name," and this name is entered in the Element Table. Thus input signal number 1, diode number 3, and relay 12 would be entered in the Element Table (and later punched on cards by the data processing department) as follows:

SGN10
CR300
K1200

Note carefully that the alphabetical part of the name may be either one, two, or three letters long and the remaining four, three, or two character spaces are for the element's number. The procedure for assigning numbers used in this handbook lets the "1" immediately following the "SGN" indicate that this is signal number one. The zero following the "1" is a "dummy" number to indicate that the fifth character place is a blank. The zero should not be read in conjunction with the "1", that is, as "signal 10". "Signal 10" is indicated as SGN01. If a number other than zero were in the fifth character place, for example, SGN76, then this would properly mean signal number 76.

1.4 The Relations Between Elements and Part-Classes

In order to reduce both key punch and computer processing time, a simple process has been devised to recognize identical failure rates for similar parts. For example, if a circuit under analysis contains a large number of carbon film resistors, but with possibly different values (1, 10, 100, 10K, 10M ohms for five-watt loads), in general it can be recognized that all of these resistors will have identical failure rates. They therefore can be grouped as a single class or part-class.

Thus if resistors R1, R8, and R16-37 were all carbon film resistors that have an identical failure rate, they could all be assigned a single part-class code, namely RFC (which can be found in the Part Class Dictionary in Appendix A).

1.5 Part-Class Codes and the Part-Class Failure Information Table

All part-class codes are three letters long. Typical of such codes are the following:

RFC Resistor, carbon film

CGL Capacitor, glass

KCM Relay, coil structure, miniature, general purpose

Other codes can be found in the Part-Class Dictionary in Appendix A.

A distinctive characteristic of all parts listed by any one of these three letter codes is that they will all have the same failure rate. Thus, instead of having to punch separate failure rate cards for each element to be considered in an analysis, one simply assigns all identical elements the proper three-letter part-class code. Then only one part-class card needs to be punched and delivered to the computer. The computer, while processing, refers only to the part-class failure rate of any element that belongs to this part-class.

(The ARINC Research Corporation IBM 1401 computer already has in storage the failure rates for the part-classes indicated in Appendix A.)

The Part-Class assignment is done on the Element Table. A Part-Class Failure Information Table then needs to be filled in on the basis of the part-classes determined from the Element Table.

1.6 CRAM Reliability Diagrams

Although the manual is intended as a reference book, the rules it presents do not lead to the preparation of only one correct CRAM reliability diagram for a particular physical configuration. Rather, as is true with conventional reliability diagrams, it may be possible to prepare more than one diagram that will lead to the correct solution. Only one basic approach, however, will be followed in this manual.

CRAM diagrams are made up of blocks. Each block represents an entity (physical item or signal) in a system. Such entities are called elements. The major difference between conventional and CRAM reliability diagrams is that CRAM diagrams do not have split outputs; i.e., every block, except the last, has just one successor block.

CRAM diagrams do have advantages over conventional diagrams that are not readily apparent to an analyst who is not familiar with both types. An engineer, moreover, need not be conversant with reliability techniques in order to be trained to draw CRAM diagrams. CRAM diagrams are also generally easier for a second analyst to check because they are drawn in a serial, or step-by-step, manner that simulates the path along which a signal or current flows.

Figures 1-1 and 1-2 are examples of conventional diagrams and their equivalent CRAM diagrams. Reliability equations derived from either diagram (in any one figure) will be equivalent. However, a comparison of the two types of diagram reveals three major differences:

(1) In a conventional diagram, the signal flows from left to right; in a CRAM diagram, from top to bottom (these are conventions, not mathematical requirements).

(2) In a CRAM diagram, inputs to parallel branches are not connected, and outputs of parallel branches are connected by a special symbol, -ϙ- , called the "or" symbol. If a single block precedes two or more parallel branches, it must be drawn in series with each branch in the CRAM diagram.

(3) CRAM diagrams tend to be larger than conventional diagrams, a condition that can be alleviated by the judicious use of convenience blocks.

1.7 Convenience Blocks

Convenience blocks are used if branches of the diagram must be repeated in order to avoid the split outputs of conventional diagrams. A convenience block, therefore, represents an entire branch.

The convenience block designation for the branch to be represented, if the branch ends in an element, is that element (with a "+" added); or the branch may be represented as a "fictitious" block, with a "+" added, if the branch does not end in an element. In either case, the convenience block represents all of the elements that feed into a line.

In Figure 1-3 (c), C^+ is a convenience block that represents element "C" and its predecessors, all of which are shown in Figure 1-3 (b). Likewise, 101^+ is an example of a fictitious convenience block inserted into the diagram, and it represents the branch above element "F" in Figure 1-3 (b).

Both types of convenience blocks are used in the same way. The first time a convenience block is used, it is shown in the diagram with all its predecessor blocks, and a "+" is added to the name of the first convenience expression. (This causes the computer to put the block and its predecessors into a special storage.) The next time the branch is needed as an input, the same element or fictitious name is repeated, but with a "*" added to it. The "*" sign will cause the computer to call the entire expression for the branch from the special storage.

Lastly, a "c" (lower case) is added in the upper left corner of any convenience block that does not represent real system elements (see Section 4, Coding Instructions). This tells the computer that the expression is fictitious. The computer's printed output will not contain the name of this fictitious block, since the computer automatically eliminates the fictitious block while processing.

The overall effect of convenience blocks may be seen by a comparison of Figures 1-3 (b) and 1-3 (c).

1.8 More About The Tables, Including The Mode Table

Until now, it has been assumed that only one failure mode, "not OK" (NG)**, exists for the elements in Figure 1-3. Therefore, the only mode indicated in Figure 1-5 is "NG". The greater problem, then, is a familiar one: "Given the reliability of the components, what is the reliability of the system?" It should be obvious here that numerous operating modes may be applicable to the elements of a single diagram, and that these modes also must be accounted for in the system's reliability.

** Since the computer is not equipped to print the "not" bar over (OK), the symbol "NG" is used instead, and means "no good" or "not OK" ($\overline{\text{OK}}$).

A list of Operating Modes, therefore, must be supplied with each diagram. This list is an aid for the data processing clerks and not a computer input. A separate Operating Mode list is not required if a Part-Class Failure Information Table is supplied with the diagram, since the table includes space for the same information. The list of Operating Modes is described in Section 3, and samples are shown in Figure 3-1.

Examination of the Element Table (Figure 1-4) may lead to the belief that it is not required. Indeed, for this particular example the only requirement is that the information be put into the computer. The current computer program is capable of accepting a maximum of 200* part-class failure rates for a given computer run. Since a complex system diagram can contain many elements with the same failure rate, and it is probable that element types will be repeated, the concept of Element Table and Part-Class Failure Information Table is used to conserve storage space. Thus, during the reliability calculation in the CRAM III computer program, the computer looks up the element in the appropriate section of storage, determines the part-class to which it belongs, and then looks up the probability for that part-class in the part-class failure information section of storage.

Consequently, for any case where no two elements are of the same class, the engineer need only compile the Failure Information Table. Since the information must be put into the computer, the electronic data processing (EDP) analyst will originate the Failure Information Table according to the engineer's instructions.

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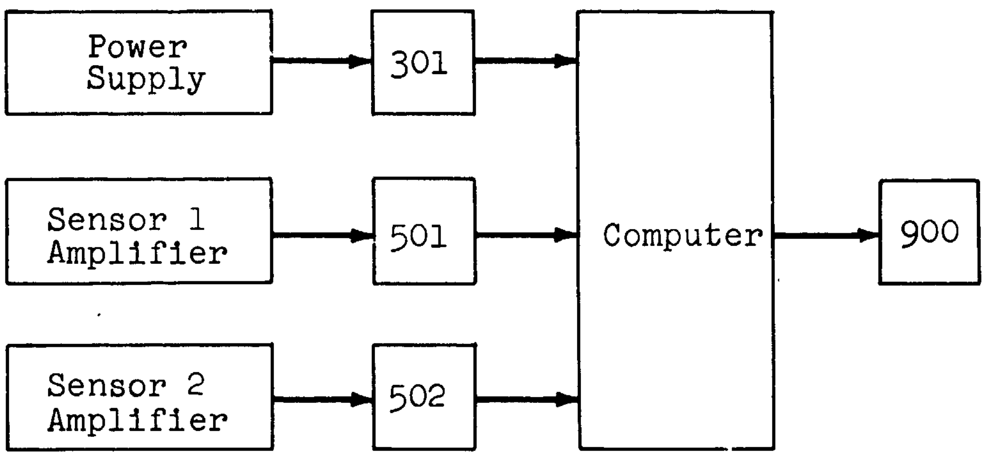
* The limitation in the number of class failure rates is restricted by the computer storage capability. It is controlled by the number of symbols allowed for the element name, the number of elements assigned per part-class, and the number of failure modes per part-class

1.9 Special Instructions

Under certain circumstances, the engineer may want an evaluation to be performed in a particular manner or in several different ways. Requests for the evaluation of portions of the system, or substitution of the output of one system as the input of another, should accompany the CRAM reliability diagram. A signal flow chart or a simplified functional diagram that shows signal numbers can be very helpful to the EDP analyst.

For example, Figure 1-6 shows the functional diagram and the special instructions that might accompany the diagram and its associated tables.



Evaluate Signal 900 using:

(1) Predicted values for signals 301, 501, and 502

(2) An assumed reliability for signal 301, including the assumption that the reliabilities of 501 and 502 are each unity

FIGURE 1-6

EXAMPLE OF SPECIAL INSTRUCTIONS

1.10 Advantages and Limitations of CRAM

An analyst who has evaluated redundant circuits knows that the derivation of reliability equations can be tedious and time-consuming. An original purpose of CRAM was to simplify the evaluation of complex electrical circuits that contain numerous identical parts (i.e., many parts but few part types) in redundant or voting-logic arrangements. However, while CRAM has certain such advantages, it also has limitations. Both are outlined below:

Advantages:

(1) CRAM frees engineers from the often time-consuming tasks of deriving reliability equations and calculating probabilities.

(2) A permanent system reliability model is established.

(3) Once the computer program cards have been punched for a system, slight modifications can easily be made and the computer programs rerun. This advantage is especially important for large, complicated systems, and for rapidly obtaining comparisons of the effects of several changes.

Limitations:

(1) The diagram must be drawn in a specified manner, and data must be furnished in a specified format.

(2) For small, simple systems, CRAM can be more costly and time-consuming than conventional methods.

(3) A system composed of many different parts in series is more easily handled by computing the element probabilities for any given time and summing the element failure rates. If more than 200 failure rates (the maximum number that the present computer program

can store) are required, the diagram must be divided into two or more smaller diagrams in order to utilize the computer.

(4) Personnel must be trained to convert the diagrams and tables to the keypunch format.

1.11 Summary

For a complete reliability evaluation, the required computer inputs are:

(1) Reliability Diagram Data

(2) An Element Table

(3) A Part-Class Failure Information Table

The Element Table need not be supplied by the engineer if no two elements are of the same class; it can be compiled by the EDP analyst according to written instructions from the engineer.

If the Part-Class Failure Information Table does not accompany the diagram, either because it is not completed at the same time, or because a qualitative analysis is required (i.e., the CRAM III program to calculate the reliability value is not required), then the engineer must supply a list of Operating Modes.

In other words, the engineer will supply either a reliability diagram, an Element Table, and a Part-Class Information Table, or a reliability diagram and a list of Operating Modes. Any special instructions must accompany the diagram and applicable table(s).

2. PROCEDURAL RULES

2.1 The Rules

Most of the rules presented in this section will apply to a conventional reliability evaluation as well as to a CRAM evaluation. However, two terms, element and element class, should be defined again:

Element - The entity (physical item or signal) whose name appears in a block on the CRAM reliability block diagram, e.g., resistor, relay coil, relay contact set, amplifier, or subsystem.

Element Class - The type of element named in a block, e.g., wirewound or carbon-film resistor, miniature relay or power contactor, or a specific type of diode.

The following five procedural rules (PR's), which are explained in greater detail in the next section, are applicable to CRAM:

PR 1. No two elements in the system may have the same name, and a particular element must have the same name every time it appears.

PR 2. No two diagrams may have elements in common; i.e., elements in common between two diagrams should be broken out as a separate subsystem on a common diagram.

PR 3. Before starting the subsystem analysis, construct a system diagram that contains each system operaating mode which is to be evaluated, e.g., success or failure, correct signal or false signal. These will be shown as elements in the system diagram and will be subsystem inputs, outputs, or functions.

PR 4.1. Diagrams should be checked against the system description by a second analyst.

PR 4.2. Lists of element names vs. element classes should be checked:

(a) Against the diagram for completeness and accuracy

(b) Against the original system description as a second check on names and the element class to which each element belongs

PR 4.3. Element class failure information lists should be proofread against the original source.

PR 4.4. Diagram punched cards should be proofread against the diagram. Element cards (and their order) should be proofread against class tables.

2.2 Explanation of the Rules

Procedural Rules 1 and 2 apply to any type of reliability evaluation, conventional or CRAM. When the term of a reliability equation contains a factor multiplied by itself (e.g., A^2), the exponent does not affect the meaning, because A cannot properly operate twice. Therefore, by Boolean algebra, $A \cdot A = A$. Of course, other combinations such as A and not-A($\bar{A}$) are possible, but it should be apparent that terminology must be consistent and that a single element must not appear on two different diagrams if the correct equation is to be derived.

The computer programs operate on the <u>names</u> of elements. If two elements (that appear on the same diagram) are given the same name, the programs will treat them as different occurrences of the same element and derive the model accordingly. Conversely, if the same element appears twice on a diagram, but under different names, the program will treat this element as two distinct elements.

The same principle applies to subsystems. Thus if two subsystems have a group of elements in common, but with different names, the computer will act as if the common group of elements represents two separate groups.

Procedural Rule 3 is not a requirement, yet it is obviously a good rule to follow for any type of project since it ensures an orderly analysis.

The final subrules listed under PR4, which are good ones to follow in any analysis, should be self-explanatory.

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3. CODING THE OPERATING MODES

In Section 1 it was stated that numerous operating modes are possible for each element, though in the example of Figure 1-4 only one successful operating mode for each element is shown, namely, "OK". However, an element may be successful even if it fails in one or more particular ways.

This possibility establishes the requirement to identify additional operating modes for each element and to assess each mode with a failure rate or probability of occurrence. The intent is to allow the engineer to use probability values for particular types of operating modes as well as for mere success or failure. For example, it may be necessary to assess the probability of an open, a short, or an unstable condition for a relay coil instead of just the coil's probability of failing. The former assessment would be required if a quantitative comparison of the probability of occurrence for certain effects were needed.

Element operating modes are coded and must be entered into the blocks of a reliability diagram. For elements that are parts, this recording is best done by a mnemonic code, such as:

op for "open"
sh for "short"
le for "leak"
un for "unstable"
OK for "OK"
$\overline{\text{OK}}$ for "not OK"

A complete, standardized list of mnemonic codes has not been developed at this time, but this is not a deterrent to utilizing CRAM since the codes can be developed and documented for a particular system by the reliability engineer.

The operating modes of systems or subsystems will be represented by the terminal blocks of different diagrams; and when they appear as elements in other diagrams, the indication "$\overline{\text{OK}}$" or "OK" will suffice.

It is important that all operating modes to be used on a diagram be recorded, and that a list of these modes be attached to the diagram. A form for such a list, which must be completed for each diagram, appears as Figure 3-1. The

1. Diagram for ____________________

2. Diagram name† ____________________

3. Operating modes: ____________________

Mode Number	1	2	3	4
Mode Name				
Mode Designator††				
	5	6	7	8
	9	10	11	12

† This is the name in the last block of the diagram.

†† These are the mnemonic codes used to indicate modes on the blocks.

FIGURE 3-1

LIST OF OPERATING MODES

last two modes used must always be $\overline{OK}$ and OK, and in that order. (As explained in Section 1, a separate List of Operating Modes is not required if the Part-Class Failure Information Table accompanies the diagram, because the table includes the same information.)

Operating modes can be indicated on a diagram's blocks in two ways: by inclusion or by exclusion. Inclusion is used when all the modes that allow success of the path are shown. For example, if the function of diode A is to conduct current, this situation can be shown as,

A/OK,sh

which indicates that success can be obtained in that path with A either shorted or working perfectly.

If "open" is the only failure mode of interest for this diode, an equivalent statement would have been:

"A must not open"

When this verbalization is used, it can be shown on the block as an indication by exclusion. To indicate an excluded mode, a bar is drawn over the name of the mode; thus,

A /$\overline{op}$

Either method may be used in any block. However, methods may not be mixed in one block. Thus,

A/$\overline{op}$, OK

would not be acceptable.

This rule is required because exclusion and inclusion have different logical interpretations when several mode designators follow the element name in the block. If two or more modes appear without bars (inclusion), the interpretation is that any one of these modes will allow success. If several mode names appear, each with a bar over it (exclusion), the interpretation is that all the mentioned modes are excluded. These interpretations are consistent with the actual operations of the computer program.

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4. CODING INSTRUCTIONS

The coding instructions (CI) listed in this section of the manual are to be considered the rules by which codes are assigned to elements and operating modes. These rules are directly associated with the mechanics of using CRAM as explained in Section 8.

CI 1. Element names and element class names are limited by the computer program to not more than five (5) spaces or symbols. For example, a set of relay contacts might be coded K4A12, meaning they are contact numbers 1 and 2 in Panel A and are part of Relay (K) Number 4. Any reference to these contacts in the diagram should always use the same five symbols.

CI 2. For parts, the name that appears on the original description (or a mnemonic) should be consistently used on the diagram wherever possible.

CI 3. To avoid name duplication between elements on different diagrams, a prefix code is used in front of the part name code.

CI 4. Any rational system may be used to assign names to elements that are subsystems, sub-subsystems, or convenience blocks. These names should be carefully recorded on the diagrams in which such elements appear. Any continuing policy concerning such nomenclature should be documented.

CR 5. Convenience blocks are coded as follows:

(a) For convenience blocks that represent branches ending in element names, add a "+" to the element name on its first appearance, and a "*" on each subsequent use of the block.(see Figure 1-3).

(b) For convenience blocks that represent branches which do not terminate in elements, any convenient, fictitious symbol name may be used. The letter "c" (lower case) is entered in the upper left-hand corner of the block to designate that the element is fictitious (see Figure 1-3).

CI 6. For each diagram, a list of operating modes must be prepared and codes assigned to each mode. The minimum number of spaces to be used is three, and the maximum is fifteen.

CI 7. The operating modes that allow success to the path in which the block appears must be indicated in the block. Both inclusion or exclusion may be used within a diagram, but only one form within any one block of the diagram. The mode indication may appear either under the element name or to the right of it with a slash mark (/) separating the name from the mode indication (e.g., $\frac{K4}{sh}$ or K4/sh for Relay Coil No. 4 shorted).

The indicators for different modes will be separated by commas.

(a) If inclusion is used, the indicators of all allowed modes will appear (without bars over them).

(b) If exclusion is used, the indicators of all prohibited modes will appear, each with a bar over it.

CI 8. Convenience blocks that correspond to branches that end in an element will carry the mode indication of the element. Convenience blocks that correspond to branches that do not end in an element are designated by a fictitious symbol and will carry no mode indication; however, they will carry a "c" (lower case) in the upper left-hand corner.

CI 9. For identical parts within a part-class, and using the five spaces allocated for a part-class:

(a) If identical parts differ in their application and require different K factors for the same operating mode, use one symbol to code the application factors (see Figure 1-5).

(b) If identical parts are used for different periods of time, use one symbol to code the time periods.

(c) Use the remaining spaces for a mnemonic code of the part-classes.

(d) For elements which themselves have diagrams, use diagram names wherever possible.

CI 10. Use the same part-class code throughout the system analysis.

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5. INSTRUCTIONS FOR THE ELEMENT TABLE

This section of the manual lists the instructions for completing an Element Table in the working order of element entry. Such tables are shown in Figures 1-4 and 5-1.

(1) The Heading

(a) "System/Subsystem Description" is completed with the full English name of the system or subsystem.

(b) "Diagram Name" refers to the name in the last block of the diagram.

(c) "Page Number" and "Number of Pages in the Table" are entered in the upper right corner.

(d) The maximum number of symbols used for an element name is entered in "Length of Element Name."

(2) The second, fourth, and sixth columns are completed from the diagrams.* The fourth and sixth columns are used as needed. If additional space is required, a second sheet is used and the information described under (1), above, is recorded on the second sheet. Convenience blocks that do not correspond to elements (i.e., represented by a fictitious symbol) are not entered in the table.

(3) The number of elements (excluding convenience blocks that do not correspond to elements) are then counted. This number is entered in the heading of the table

*The PHASE 2 computer program prints out a list of elements in alphabetic order; this can be used to fill out these columns.

System/Subsystem Description					
Diagram Name		No. of Elements on Table		Checked	(initials)
Length of Element Name		Part-Classes Checked			(initials)

Class	Element	Class	Element	Class	Element

FIGURE 5-1

ELEMENT TABLE

entitled "No. of Elements on Table." Other than the above-noted exclusion, the number should be the same as the number of elements shown on the diagram.

(4) The part-class information is obtained from the system description, and the prearranged part-class codes are entered in Columns 1, 3, and 5, as needed.

(5) On completion of the table, the work is checked, preferably with the help of the second analyst who checked the diagram, and the checked tables are initialed.

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6. INSTRUCTIONS FOR CONSTRUCTING THE FAILURE INFORMATION TABLE

This section of the manual lists the instructions on how the Failure Information Table is constructed. Samples of the table are shown in Figures 1-5 and 6-1.

(1) Table Heading Information

(a) "System/Subsystem Description" is completed with the full English name of the system or subsystem.

(b) There often are several diagrams with the same element-classes. In that case, only the extra classes are entered, and the referenced table is used as a second sheet to the one filled out.

(c) "Diagram Name" refers to the name in the last block of the diagram.

(d) "No. of Operating Modes" gives the total number of operating modes <u>less</u> the OK mode.

(2) The operating-mode coding is entered from the list of operating modes described in Sections 1 and 3. The order of the modes must be the same as that on the mode list.

(3) The columns are filled out as follows:

(a) Class -- the name of the element's class as it appears on the element list (Figure 5-1).

(b) Mode No. -- for each element class the corresponding number [from (2), above] for each of the modes in which it can operate are listed, in order, and in columnar form.

System/Subsystem Description		
Use With Table No.	Diagram Name	No. of Operating Modes (less OK)
Checked for Completeness (initials)		Numbers Checked (initials)

Operating Modes	Designation															
	No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

CLASS	Mode No.	P/ Blank	Probability/ Rate	K_1	K_2	K_3 †	t

† Any number of K factors may be shown.

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FIGURE 6-1

PART-CLASS FAILURE INFORMATION TABLE

(c) P/Blank -- if the information is a <u>failure probability</u>, a "P" is entered in this column; if the information is a <u>failure</u> <u>rate</u>, the column is left blank.

(d) Probability/Rate - the probability or rate value is entered here.*

(e) K_1, ..., K_5 - application factors [needed if (d) is a rate]*.

(f) t -- the time during which the part-class is required [needed if (d) is a rate].* Time must be stated in the same units of time as those for the failure rate value; e.g., time must be in hours if the failure rate is a per-hour value.

(4) The completed form is checked against the element list for completeness, and against the original information for accuracy of the numbers entered. If at all possible, a second analyst is employed to help with the checking. The checked blocks are initialed as the checks are made.

*Probabilities, rates, application factors, and times may be entered in conventional notation or floating-point notation. An explanation of the floating-point notation used in existing computer programs is presented in Section 8.

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7. THE COMPUTER PROGRAMS

The total CRAM computer program is divided into three programs -- CRAM I, CRAM II, and CRAM III. This section presents simple descriptions of these programs but does not include any rules or requirements for their use. Section 8 describes the inputs required to exercise the programs and to interpret the results.

7.1 CRAM I - Diagram-to-Boolean Formula

The first computer program accepts the diagram and produces a formula. It works serially in that it constructs a formula step by step, adding to it on the basis of the last card it has read; it then reads the next card, which represents the next block, and continues making the formula. This process is possible only if the cards are so ordered that, when a block is reached, the blocks for each of the predecessors of this block are already available in the machine.

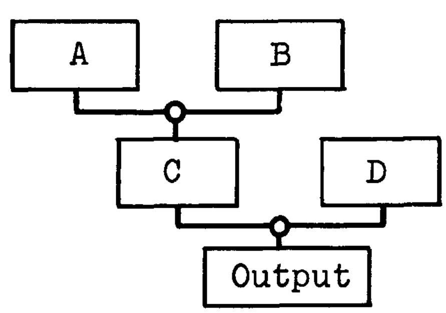

FIGURE 7-1

EXAMPLE OF A SIMPLE CRAM DIAGRAM

For example, the output of CRAM I for the diagram shown in Figure 7-1 would be

$$[(A \vee B)\ C \vee D]$$

which can be read as:

A or B, and C; or D is Success

7.2 CRAM II - Boolean to Probability Formula

The second computer program, Cram II, is divided into three parts called, in the order in which they are run, PHASE 1, PHASE 2, and PHASE 3.

Elements of the input formula are changed to two-digit numbers by PHASE 1. For the formula of Figure 7-1 this assignment would be as follows:*

01	A
02	B
03	C
04	D

The formula is then stored as [(01 v 02) × 03 v 04]. Next, 05 is substituted for (01 v 02) and written as 05 = + 01 + 02 - 01 × 02 (the formula is now [05 × 03 v 04)]. The next substitution is 06 = + 05 × 03 [which yields (06 v 04)] and finally 07 = + 06 + 04 - 06 × 04.

The output of PHASE 1 is arranged in the following order and used as the input to PHASE 2: 07, 06, 05, 01, 02, 03, 04. The computer expands the 07 number by substituting for 06 to obtain: + 05 × 03 + 04 - 05 × 03 × 04. The next substitution is 05 and, after appropriate multiplications, the original

---

* On the card program, these assignments were punched on cards; on the tape program, they were written on a tape and automatically used for the next phase.

nomenclature (i.e., A, B, C, and D) is substituted. The output of PHASE 2 is then in the form: $+ A \times C + B \times C - A \times B \times C + D - A \times C \times D - B \times C \times D + A \times B \times C \times D$.

Two-digit numbers are substituted for element names to conserve space in storage; otherwise, the computer storage would quickly be filled if each branch were composed of several elements.

The PHASE 2 output is operated on by PHASE 3 in the computer. During PHASE 3, operating modes of elements that appear more than once in each term are compared and are appropriately evaluated. If, for example, the same element appears in a term twice as G_1, one will be eliminated (i.e., $G_1 \times G_1 = G_1$). Also, a term will be eliminated if it contains the same element in two or more mutually exclusive modes (i.e., $G_0 \times G_1 = 0$ where G_0 cannot occur at the same time as G_1).

The formula is now in the correct form for substitution of probabilities for each element and, as such, is identical to the formula that would be derived manually.

7.3 CRAM III - Formula to Probability Value

The probability value of the circuit being evaluated is computed by the CRAM III program. Inputs to this computer program are the failure rates, or probability of failure or success, for each part-class; the element list which relates element names to part-classes; and the output of CRAM II. As each element in the formula is read by the computer, the element name is locked up in the element list and the part-class determined. The failure rate for the part-class is converted to a probability, or the probability is used directly, and the probabilities for the elements in each term are multiplied together. Probabilities for each term are then added or subtracted as required by the formula, and the answer is printed out.

7.4 Summary

After this section is read, it should be apparent to experienced reliability engineers that CRAM involves the same steps that would be manually performed in a conventional evaluation. Since the computer is able to evaluate complicated circuits faster and more accurately, it has definite time-saving advantages in evaluating complex systems. Also, once the program is established for a system, changes in the system can be quickly evaluated for their effect on system reliability.

8. COMPUTER INPUTS AND READOUTS - THE MECHANICS OF USING CRAM

As indicated in Section 7, it is possible to utilize the outputs of CRAM I and II without using CRAM III. The output of CRAM I is the system's reliability mathematical model in a Boolean format. The output of CRAM II is the functional expression of the system's mathematical model in the expansion necessary to accept the probability values for each element (i.e., the input form for CRAM III). The output of CRAM III is the quantitative analysis of the system. It is obvious that, to obtain the output of any one of the CRAM programs, it is necessary to provide the inputs which have the same format as the outputs of the preceding program.

8.1 CRAM I

The required input to CRAM I is the CRAM reliability diagram, the previously described tables, and the key punch instructions. The inputs are converted to IBM cards by computer personnel. The computer constructs the formula step by step by going through the cards serially, adding to the formula on the basis of the last card it has read. The emphasis here is on the fact that the cards must be presented in their proper order.

CRAM I can be accomplished manually, which, for the less complex systems, is often the most economical method. Since the output of CRAM I is the input to CRAM II, the input format for the manually constructed CRAM I output is presented. When CRAM I is performed by the computer, the output is recorded on tape instead of IBM cards. (If a tape capability is not available, the computer output will also be on cards.)

8.1.1 CRAM II Input Format

Before the expression for the CRAM II PHASE 1 input can be written, the length of the element names must be chosen and the number of failure modes determined. The length of the element names must not exceed five symbols and may be as short as one symbol. For the example of Figure 8-1, a single symbol would suffice for the 11 different elements. However, five symbols will be used in the example so that the name in the expression can be more easily recognized as the element, and because five symbols have been used for most CRAM studies. Since all element names for this example must occupy five spaces, one or more zeros must be entered to the right of a name that contains less than five descriptive symbols; i.e., K 3 must be written K3000 or K0300.

The example can be recognized as the basic configuration of Figure 7-1 expanded to include several elements in each branch, which shows that some elements are common to more than one branch. This expanded configuration is as shown in Figure 8-1. In each block, the name of the element represented is indicated in the upper portion of the block, and the condition of the element that leads to success is shown in the lower portion. The descriptions of the names and conditions are as follows:

Symbol	Description
Signal 1, Signal 2, Signal 3	Relay-Energizing Signals
Bus 1	Power Bus
CR1, CR2, CR3	Diodes
K12, K3	Relay Coils
K12A, K3A	Relay Contacts

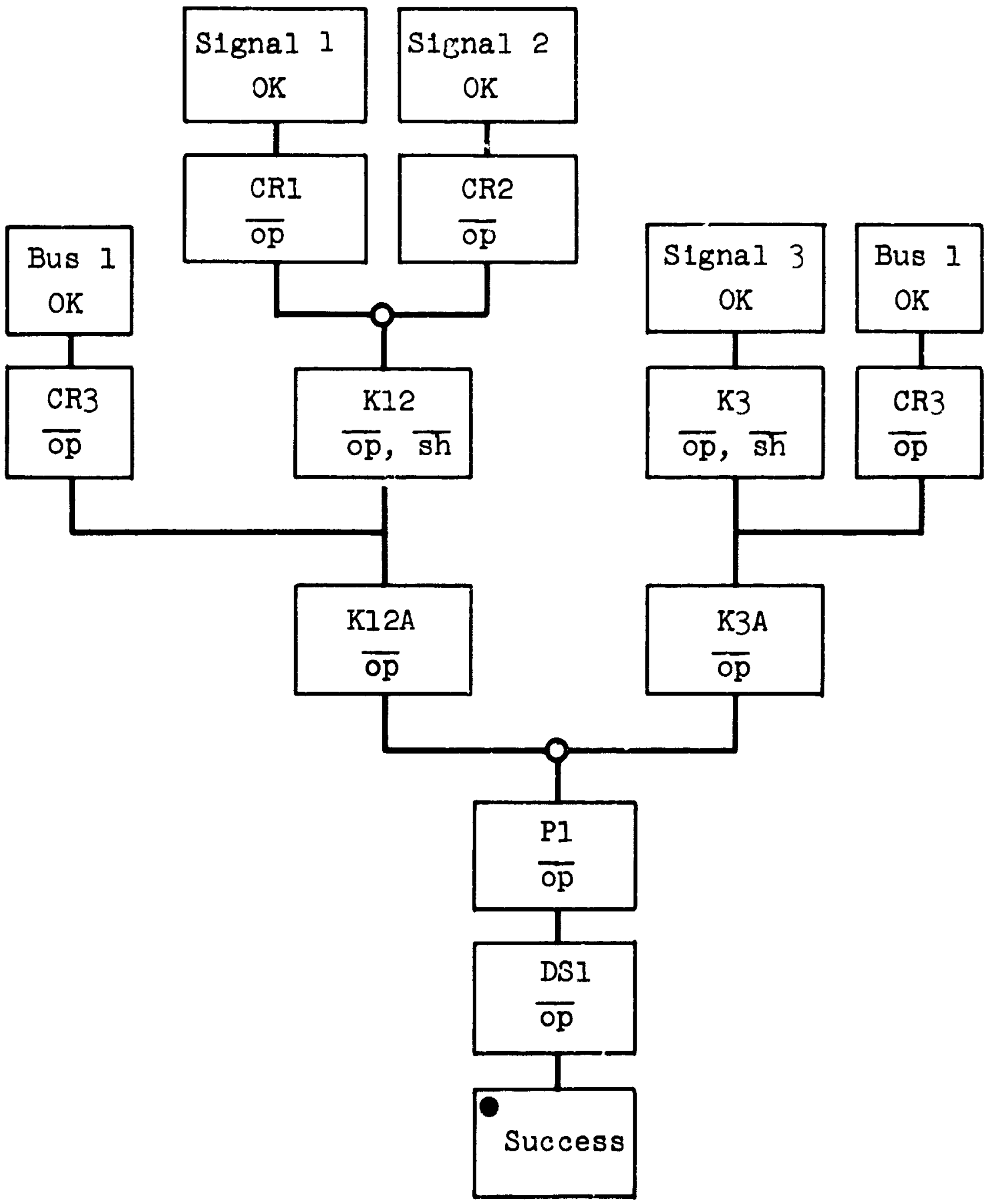

FIGURE 8-1

CRAM DIAGRAM FOR A RELAY CIRCUIT

P1	Connector
DS1	Indicating Lamp
OK	Not failed
$\overline{op}$	Not open
$\overline{sh}$	Not shorted

The required condition or mode of the element then must be noted after the element name. The minimum number of spaces that can be used is three, and the maximum is fifteen. The first space after the element name is called the "not slot", and the last two spaces must correspond to "$\overline{OK}$" and "OK", respectively. The remaining spaces can be used to represent any one or more (up to 12) failure conditions in any combination, provided only that they are consistent for a paritcular analysis.

For the example, four modes are considered and entered on the IBM sheet in this order: "open", "short", "no good" (or "not OK"), and "OK" Success probabilities for each mode then are determined from the entries made on the Part-Class Failure Information Table. The CRAM III computer program calculates the probability of success for each part-class from the given failure rates or failure probabilities, and the mode "no good" is used as the probability of failure for signals and busses.

On the IBM sheet and punched cards, a one (1) is used to show that the mode is to be considered, and a zero (0) is used to show that the mode is not to be considered. Each operating mode or combination of modes used in this example is shown in Table 8-1 (also see Appendix B).

TABLE 8-1

SAMPLE DISPLAY OF OPERATING MODES

Operating Mode	Spaces after Element Name				
	1 Not Slot	2 Open (op)	3 Short (sh)	4 Not OK (ng)	5 OK (OK)
Not open	1	1	0	0	0
Not open, not short	1	1	1	0	0
OK	0	0	0	0	1

The codes used in this example are:

Symbol and Condition	Code Element Name | Operating Mode
Signal 1 - OK	SGN1000001
Signal 2 - OK	SGN2000001
Signal 3 - OK	SGN3000001
Bus 1 - OK	BUS1000001
CR1 - not open	CR10011000
CR2 - not open	CR20011000
CR3 - not open	CR30011000
K12 - not open, not short	K120011100
K3 - not open, not short	K300011100
K12A - not open	K12A011000
K3A - not open	K3A0011000
P1 - not open	P100011000
DS1 - not open	DS10011000

8.1.2 Operational Symbols

Before the input formula can be written, certain operational symbols must be defined. The meanings and IBM card codings of these symbols are shown in Table 8-2. On IBM cards, the 12 possible hole locations, from top to bottom, are: 12 punch, 11 punch, and zero through 9.

TABLE 8-2

SYMBOLS FOR LOGICAL SIGNS

Logical Sign	Meaning	IBM Symbols			Card-Punch
		Key-Punch	Interpreter	Computer	
(	Left Paren	(	U	%	0,4,8
)	Right Paren	)	D	¤	12,4,8
&	"and"	+	(blank)	ε	12
v	"or"	,	T	,	0,3,8

The IBM symbols shown in Table 8-2 are those presently available on machines at ARINC Research Corporation. Keypunch and interpreter symbols are printed on the top of each card. Each keypunch symbol is printed above its corresponding column. Interpreter symbols start with the symbol for Column 1 at the left and continue to Column 60 along the extreme top of the card; symbols for Columns 61-80 are printed below the symbols for Columns 41-60.

By use of the element, operating-mode, and logical symbols, the CRAM I output for Figure 8-1 is as shown in Figure 8-2. The only requirement for writing CRAM I outputs is:

WORK ORDER NO.______

ARINC RESEARCH CORPORATION

SHEET NO.____ OF____
DATE ______

FIGURE 8-2
CRAM II INPUT FOR FIGURE 8-1

```
    12345678901234567890123456789012345678901234567890123456789012345678901234567890
 1  P1000110008DS10011000&((SGN1000001&CR10011000&K1200111008&BUS1000001&CR30011000&K
 2  12A0110003SGN2000001&CR20011000&K1200111008&BUS1000001&CR30011000&K12A011000)3SGN
 3  3000001&K3000111008&BUS1000001&CR30011000&K3A0011000)
 4
 5
 6
 7
 8
 9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
```

Start in Column 1 on the first card and continue with each column (leave no spaces) to the end of the formula.

For simplicity, the CRAM I output has been written with P1, the connector, and DS1, the indicating lamp, as the first terms.

8.2 CRAM II

The cards containing the coded formula for the CRAM I output (i.e., CRAM II input) are run with the PHASE I program and appropriate header card. Machine operating personnel must be informed of the element length and number of operating modes. For this example, the length of the element name is five symbols, and the number of operating modes (including the "Not slot") is five.

8.2.1 CRAM II Phases

Figure 8-3 shows the input to CRAM II - PHASE 1 and the outputs of PHASE 1, PHASE 2, and PHASE 3, in that order. It should be remembered that the output of PHASE 1 is the input to PHASE 2, the output of PHASE 2 is the input to PHASE 3, and the output of PHASE 3 is the input to CRAM III.

Output cards from PHASE 1 are printed in the order in which they were punched. Used as the inputs to PHASE 2, they are arranged as 07, 06, and 05. The computer expands the expression and stops; then the remaining, or dictionary, cards are fed into the computer in the order shown in Figure 8-3(a).

A comparison of the PHASE 2 and PHASE 3 outputs (Figures 8-3a and 8-3b) shows that duplicate elements have been deleted from certain terms in the output of PHASE 2. The output of PHASE 3 is then the expression for the probability of success for the circuit shown in Figure 8-1.

FIGURE 8-3

CRAM II PRINTOUTS

FIGURE 8-3(a)

IBM PRINTOUT OF CRAM II - PHASE 1 INPUT AND
OUTPUT CARDS FOR FIGURE 8-1

```
          RELAY CIRCUIT        INPUT TO CRAM II - PHASE 1

P100011000&DS10011000&ZZSGN1000001&CR10011000&K120011100&BUS1000001&CR30011000&K
12A011000,SGN2000001&CR20011000&K120011100&BUS1000001&CR30011000&K12A011000=,SGN
3000001&K300011100&BUS1000001&CR30011000&K3A0011000=

          RELAY CIRCUIT        OUTPUT OF PHASE 1 - INPUT TO PHASE 2

01   1    P100011000
01   1    DS10011000
02   1    SGN1000001
02   1    CR10011000
02   1    K120011100
02   1    BUS1000001
02   1    CR30011000
02   1    K12A011000
03   1    SGN2000001
03   1    CR20011000
03   1    K120011100
03   1    BUS1000001
03   1    CR30011000
03   1    K12A011000
04   1    SGN3000001
04   1    K300011100
04   1    BUS1000001
04   1    CR30011000
04   1    K3A0011000
05        &02&03-02X03
06        &05&04-05X04
07        &01X06
```

FIGURE 8-3

CRAM II PRINTOUTS

FIGURE 8-3(b)

IBM PRINTOUT OF CRAM II - PHASE 3 INPUT AND OUTPUT CARDS FOR FIGURE 8-1

```
        RELAY CIRCUIT       OUTPUT OF PHASE 2 - INPUT TO PHASE 3

0001    &P10001100ODS10011000SGN1000001CR10011000K120011100BUS1000001CR30011000
0001     K12A011000
0002    &P10001100ODS10011000SGN2000001CR20011000K120011100BUS1000001CR30011000
0002     K12A011000
0003    -P10001100ODS10011000SGN1000001CR10011000K120011100BUS1000001CR30011000
0003     K12A011000SGN2000001CR20011000K120011100BUS1000001CR30011000K12A011000
0004    &P10001100ODS10011000SGN3000001K300011100BUS1007001CR30011000K3A0011000
0005    -P10001100ODS10011000SGN3000001K300011100BUS1000001CR30011000K3A0011000
0005     SGN1000001CR10011000K120011100BUS1000001CR30011000K12A011000
0006    -P10001100ODS10011000SGN3000001K300011100BUS1000001CR30011000K3A0011000
0006     SGN2000001CR20011000K120011100BUS1000001CR30011000K12A011000
0007    &P10001100ODS10011000SGN3000001K300011100BUS1000001CR30011000K3A0011000
0007     SGN1000001CR10011000K120011100BUS1000001CR30011000K12A011000SGN2000001
0007     CR20011000K120011100BUS1000001CR30011000K12A011000
0007     CR20011000K120011100BUS1000001CR30011000K12A011000

        RELAY CIRCUIT       OUTPUT OF PHASE 3 - INPUT TO CRAM III

0001    &P10001100ODS10011000SGN1000001CR10011000K120011100BUS1000001CR30011000
0001     K12A011000
0002    &P10001100ODS10011000SGN2000001CR20011000K120011100BUS1000001CR30011000
0002     K12A011000
0003    -P10001100ODS10011000SGN1000001CR10011000K120011100BUS1000001CR30011000
0003     K12A011000SGN2000001CR20011000
0004    &P10001100ODS10011000SGN3000001K300011100BUS1000001CR30011000K3A0011000
0005    -P10001100ODS10011000SGN3000001K300011100BUS1000001CR30011000K3A0011000
0005     SGN1000001CR10011000K120011100K12A011000
0006    -P10001100ODS10011000SGN3000001K300011100BUS1000001CR30011000K3A0011000
0006     SGN2000001CR20011000K120011100K12A011000
0007    &P10001100ODS10011000SGN3000001K300011100BUS1000001CR30011000K3A0011000
0007     SGN1000001CR10011000K120011100K12A011000
0007     SGN2000001CR20011000
```

8.2.2 Explanation of Floating-Point Notation

Failure rates and/or probabilities may be entered on the Part-Class Failure Information Table in conventional notation or floating-point notation. Whatever method is used by the engineer, the EDP analyst must enter the numbers in floating-point notation on the IBM sheets from which the key-punch operator will then punch the cards. Therefore, the instructions in the remainder of this section may or may not be followed by the engineer but must be followed by the EDP analyst.

The form in which the numbers are to be entered on IBM sheets is a so-called floating-point form. Any number, P, can be expressed as a fraction 0.a times a power of ten;

$$P = \pm\ 0.a_1\ a_2\ a_3\ a_4\ a_5\ a_6\ a_7\ a_8 \times 10^{\pm n_1\ n_2}$$

Thus the number illustrated is written on IBM coding sheets and punched as

$$a_1\ a_2\ a_3\ a_4\ a_5\ a_6\ a_7\ \overset{\pm}{a}_8\ n_1\ \overset{\pm}{n}_2$$

where the decimal point preceding a_1 is implied.

Floating point notation, as used in CRAM, is a method of writing a number in 10 spaces without loss of accuracy in eight places (eight most significant digits), irrespective of the position of the decimal point within the number. In floating point notation the most significant digit immediately follows the decimal point (implied on cards, printed on computer outputs), and the exponent (power of 10) indicates the number of places that the decimal point must be moved if the number is to be written in conventional notation. The eight, or less, most significant digits are entered in the first eight places, and the exponent is written in the last two places.

The algebraic sign over the eighth place is the sign of the number, and the sign over the tenth place is the sign of the exponent. If the exponent is zero, the decimal point is not moved ($10^0 = 1$); if the exponent is positive, the decimal point is moved to the right; and if the exponent is negative, the point is moved to the left. As examples, 0.00397 would be written as $3970000\overset{+}{0}0\overset{-}{2}$, and -397 would be written as $3970000\overset{-}{0}0\overset{+}{3}$.

This form is used on IBM cards that constitute an <u>input</u> to the computer program because it uses exactly ten digits for each number. For ease of reading, the computer outputs use a slightly different form of the floating-point notation:

$$(-)\ a_1 a_2 a_3 a_4 a_5 a_6 a_7 a_8 E\ (-)\ n_1 n_2$$

Only minus signs are printed; therefore, if the two numbers in the above example were machine outputs, they would appear as 0.39700000 E-02 and -0.39700000 E 03, respectively. At most, eight significant figures can be carried. The final zeros need not be entered on the IBM sheets, but they must be punched.

The computer must be programmed to print the values in the form noted above. If cards with failure rates or probabilities punched in floating-point notation are printed by the use of a standard program, the results are somewhat different. In this example, the numbers would be printed on the computer as 3970000& OK and 3970000-0C.

The explanation for this type of printout is very simple. IBM cards contain 12 rows. A hole in the top row (called a 12 punch) corresponds to a plus sign (&), a hole in the second row (called an 11 punch) corresponds to a minus sign (-), and a hole in the remaining rows (0 through 9, in that order) corresponds to a number. Then, for example, the combination of a plus sign and zero is ξ, and a plus sign and 1 is A. Symbols that might appear if CRAM card information is printed by the use of a standard program are shown below.

Punch in Row*	Punch in One Row of 0-9 Rows and 12 Punch (+)	11 Punch (-)
0	ξ	-
1	A	J
2	B	K
3	C	L
4	D	M
5	E	N
6	F	O
7	G	P
8	H	Q
9	I	R

8.3 Inputs to CRAM III

The inputs to CRAM III consist of five parts, arranged in the following order:

(1) Program deck

(2) Header card

(3) Probability/failure rate deck

(4) Element list

(5) Output of CRAM II

These inputs are presented as they are required for IBM card usage. The addition of tape capability to the machines eliminates much of the manual handling of the card decks and improves the speed and efficiency of the analysis. The actual functions that are performed, whether by computer tape or by card deck, are the same.

Layouts of Parts 2, 3, and 4 are shown in Figure 8-4. These parts are described in the following sections in the order in which they will most likely be completed by the engineer and EDP analyst.

8.3.1 Element List

A possible Element Table for Figure 8-1 is shown as Figure 8-5. This table is not the only one that could be compiled, since neither the order of the elements or class codes are specified by the rules. Figure 8-6 shows the elements listed on an IBM sheet compiled by the EDP analyst for ease of key punching [see also Figure 8-4(d)]. The part-class is entered in Columns 1-3, and the element name in 11-15. All element names must be shown exactly as they were shown in the

(a) Header Card List (one card)

Card Column	1-3(1,2)	4-6	7-9	10-12 (1,3)	13-50	51-78	79,80
Content	n-1	Number of Part-classes	Number of elements[1]	M	Any heading to be printed on output page	Mode descriptions. Maximum of 14 different modes (two letters each) of which "OK" is always last.[4]	Blank

(b) Probability/Rate List

Card Column	1-5	6-9	10	11-20	21-30	...(use additional blocks of 10 columns each[7]) 71-80
Content	Part-class name	Blank	P, if probabilities; blank, if rates	Probability or rate for first mode[5]	Probability or rate for second mode	etc.

(c) Application Factor/Time for Above Cards[6]

Card Column	1-5	6-10	11,12	21-30	31-70	71-80
Content	Part-class name	Blank	Mode Number[1]	Application factor (or 1)[5]	etc.	Operating time[5]

(d) Element List

Card Column	1-5	11+m
Content	Part-class name	Element name

(1) Use leading zeros for one- and two-diget numbers, e.g., 001, 021.
(2) n-1 is the number of operating modes excluding OK.
(3) m is the number of symbols in an element name (maximum of five).
(4) See Section 8.3 for further explanation.
(5) Floating-point notation:

$$\pm 0.abcdefgh \times 10^{\pm ij} = abcdefgh\overset{\pm}{i}\overset{\pm}{j}$$

(6) If Column 10 in the b card is blank, then one c card must be punched for each operating mode for which the b card has a rate. If no application factor has been given, a floating point 1 is entered in Columns 21-30.
(7) If more than seven probabilities or rates are used, continue on a new card in Columns 21-30.

FIGURE 8-4

SHEETS FOR FAILURE INFORMATION

System/Subsystem Description					
Diagram Name	Figure 8-1	No. of Elements on Table = 13		Checked	(initials)
Length of Element Name	5	Part-Classes Checked			(initials)

Class	Element	Class	Element	Class	Element
ZXA	SGN1				
ZXA	SGN2				
ZXB	SGN3				
ZZA	BUS1				
DXX	CR1				
DXX	CR2				
DXX	CR3				
KCM	K12				
KCM	K3				
KSM	K12A				
KSM	K3A				
JYS	P1				
MLP	DS1				

OP-80, 3/18/65

FIGURE 8-5
ELEMENT TABLE FOR FIGURE 8-1

WORK ORDER NO. ____________

ARINC RESEARCH CORPORATION

SHEET NO. ______ OF ______
DATE ____________

FIGURE 8-6
IBM SHEET FOR PUNCHING ELEMENT LIST FOR FIGURE 8-1

Line	Columns 1–3	Columns 11–15
1	ZXA	SGN10
2	ZXA	SGN20
3	ZXB	SGN30
4	ZZA	BUS10
5	DXX	CR100
6	DXX	CR200
7	DXX	CR300
8	KCM	K1200
9	KCM	K3000
10	KSM	K12A0
11	KSM	K3A00
12	JYS	P1000
13	MLD	DS100
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		

the computer input formula (CRAM II or CRAM III), and five symbols must be used. (Part-class codes that should be used for CRAM analyses of Saturn systems are listed in Appendix A.)

8.3.2 Probability/Failure Rate Deck

Figure 8-7 shows the Part-Class Failure Information Table for Figure 8-1 as it might be filled out by the engineer. Only modes of interest need be entered on this table. It should be noted that probabilities are distinguished by entering a "P" in the third column, and that no "K" factors may be used with probabilities.

However, the EDP analyst must include probabilities or rates for all modes on the IBM sheet from which the cards will be punched. This sheet is shown in Figure 8-8. The floating-point notation values for Modes 1 and 2 for the probabilities are entered as zero in Columns 11-20 and 21-30 [refer also to Figure 8-4(b)]. The value for Mode 3 is entered in Columns 31-40.

The failure rates for each mode of the remaining part classes are entered in columns 11-20 for Mode 1 and columns 21-30 for Mode 2; and zeros are entered in columns 31-40 for Mode 3 [see Figure 8-4(b)]. In addition, a K factor card for each mode must be punched [see Figure 8-4(c)]. A two-digit mode number must be entered in Columns 11 and 12, and factors (or floating-point notation 1) must be entered in Columns 21-30, 31-40, etc. Since at least one K factor is required, the failure rate for Mode 3 is zero times 1. An additional requirement is that the operating time (in floating-point notation) must be punched in Columns 71-80 on the K Factor cards.

System/Subsystem Description		
Use With Table No.	Diagram Name Figure 8-1	No. of Operating Modes (Less OK) = 3
Checked for Completeness (initials)		Numbers Checked (initials)

Operating Modes	Designation	op	sh	ng											
	No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14

Class	Mode No.	F/ Blank	Probability/ Rate	K_1	K_2	K_3 †	t
ZXA	3	P	14×10^{-6}				
ZXB	3	P	8×10^{-6}				
ZZA	3	P	3×10^{-6}				
DXX	1		0.141×10^{-6}	0.25	62		0.30
DXX	2		0.028×10^{-6}	0.25	33		0.30
KCM	1		0.165×10^{-6}	1.5	47		0.30
KCM	2		0.041×10^{-6}	1.5	32		0.30
KSM	1		0.112×10^{-6}	1.5	47		0.30
KSM	2		0.095×10^{-6}	1.5	32		0.30
JYS	1		0.34×10^{-6}	2.0	19		0.30
MLD	1		0.16×10^{-6}	1.0	26		0.30

† Any number of K factors may be shown.

FIGURE 8-7

PART-CLASS FAILURE INFORMATION TABLE FOR FIGURE 8-1

WORK ORDER NO.________

ARINC RESEARCH CORPORATION

SHEET NO._____ OF_____
DATE ________

FIGURE 8-8
IBM SHEET FOR PUNCHING PROBABILITY/FAILURE RATE CARDS FOR FIGURE 8-1

Line	Cols 1–3	Cols 10–20	Cols 21–30	Cols 31–40	Cols 71–80
1	ZXA	P0000000+00+0	0000000+00+0	1400000+00−4	
2	ZXB	P0000000+00+0	0000000+00+0	8000000+00−5	
3	ZZA	P0000000+00+0	0000000+00+0	3000000+00−5	
4	DXX	1410000+00−6	2800000+00−7	0000000+00+0	
5	DXX	01	2500000+00+0	6200000+00+2	3000000+00+0
6	DXX	02	2500000+00+0	8300000+00+2	3000000+00+0
7	DXX	03	1000000+00+1		3000000+00+0
8	KCM	1650000+00−6	4100000+00−7	0000000+00+0	
9	KCM	01	1500000+00+1	4700000+00+2	3000000+00+0
10	KCM	02	1500000+00+1	3200000+00+2	3000000+00+0
11	KCM	03	1000000+00+1		3000000+00+0
12	KSM	1120000+00−6	9500000+00−7	0000000+00+0	
13	KSM	01	1500000+00+1	4700000+00+2	3000000+00+0
14	KSM	02	1500000+00+1	3200000+00+2	3000000+00+0
15	KSM	03	1000000+00+1		3000000+00+0
16	JYS	3400000+00−6	0000000+00+0	0000000+00+0	
17	JYS	01	2000000+00+1	1900000+00+2	3000000+00+0
18	JYS	02	1000000+00+1		3000000+00+0
19	JYS	03	1000000+00+1		3000000000
20	MLD	1600000+00−6	0000000+00+0	0000000+00+0	
21	MLD	01	1000000+00+1	2600000+00+2	3000000+00+0
22	MLD	02	1000000+00+1		3000000+00+0
23	MLD	03	1000000+00+1		3000000+00+0
24					
25					

Three rules must be followed for the entry of notations on the IBM sheets.

(1) Part-classes must be exactly as shown in the Element List (Figure 8-6).

(2) All numerical values must be in floating-point notation (see Section 8-2).

(3) Probabilities and failure rates must be in numerical order, by mode number, for each part-class.

8.3.3 Header Card

After the Element Table and Part-Class Information Table are completed, it is relatively simple to originate the header card [Figure 8-4(a)]. The IBM sheet for the header card for Figure 8-1 is shown in Figure 8-9. The information required for this sheet is:

(1) Columns 1-3: number of operating modes less OK (from Part-Class Failure Information Table)

(2) Columns 4-6: number of part-classes

(3) Columns 7-9: number of elements (from Element Table)

(4) Columns 10-12: number of symbols in the element names (from Element Table)

(5) Columns 13-50: any heading desired (or blank)

(6) Columns 51-78: mode descriptions (two symbols each), as shown on Part-Class Failure Information Table, and "OK" as the last mode

WORK ORDER NO. ______________

ARINC RESEARCH CORPORATION

SHEET NO. ______ OF ______
DATE ______________

FIGURE 8-9
IBM SHEET FOR PUNCHING CRAM III HEADER CARD FOR FIGURE 8-1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
1	0	0	3	0	0	8	0	1	3	0	0	5											R	E	L	A	Y		C	I	R	C	U	I	T																Ø	P	S	H	N	G	Ø	K																						
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8.3.4 Printout of Cards

Figure 8-10 shows the cards described in Sections 8.3.1 through 8.3.3 as they were printed by the computer. In practice, the title cards would not be in the deck, but the header, probability/failure rate deck, and element cards would be set up in the order shown.

8.4 Output of CRAM III - The Answer

The format of a CRAM III printout is shown in Figure 8-11, and a reproduction of the output for Figure 8-1 appears in Figure 8-12. A printout contains the following information:

(1) A list of element classes, which lists for each mode (failure or success) the probability of an element in that class being in that mode

(2) A list of elements, with the element class to which each element belongs

(3) A list, in order, of the terms that compose the expansion of the formula. These terms have the form

$$+ A \times B \times C \times D$$

where the letters represent the elements and the conditions in which the elements operate in certain modes. The printout lists the element names in columnar form and shows for each:

(a) The requirements on its modes

(b) The probability that each requirement is <u>not</u> met for each term and the probability that the conditions are all met are both printed with the sign of the term. That is, if p is the probability that all conditions were met, then p is printed as if the term had a + sign, and -p as if the term was, for example, -ABCD. This printout (as described in Step 3) is fairly time-consuming and it can be suppressed.

(4) The system probability of success is printed separately. All numbers are printed in floating-point form (explained in Section 8.2).

Examination of the CRAM III output (Figure 8-12) shows that each term is composed of the elements in each term of the CRAM II output [Figure 8-3(b)]. Now the CRAM II and CRAM III computer programs can be traced from beginning to end. By the use of the last three terms from the PHASE 1 output of Figure 8-3(a), the expression expands to:

$$01 \times 02 + 01 \times 03 - 01 \times 02 \times 03 + 01 \times 04$$
$$-01 \times 02 \times 04 - 01 \times 03 \times 04 + 01 \times 02 \times 03 \times 04$$

Substituting elements for 01 and 02 for Term 1 in the above expression gives the elements in Term 1 of the CRAM III output. Each of the other six terms may be similarly checked for both content and arithmetic sign. (Note: it must be remembered that the computer has deleted duplicate elements in each term.) Then, the answer is the arithmetic sum of the values for each term (Note: the sign of the term must be accounted for).

FIGURE 8-10

PRINTOUT OF COMPUTER CARDS

```
          RELAY CIRCUIT        CRAM III HEADER CARD

003008013005          RELAY CIRCUIT             OPSHNGOK

          RELAY CIRCUIT        FAILURE RATES

ZXA       P0000000&0&0000000&0&1400000&0M
ZXB       P0000000&0&0000000&0&8000000&0N
ZZA       P0000000&0&0000000&0&3000000&0N
DXX        1410000&002800000&0P0000000&0&
DXX        01         2500000&0&6200000&0B                        3000000&0&
DXX        02         2500000&0&8300000&0B                        3000000&0&
DXX        03         1000000&0A                                  3000000&0&
KCM        1650000&004100000&0P0000000&0&
KCM        01         1500000&0A4700000&0B                        3000000&0&
KCM        02         1500000&0A3200000&0B                        3000000&0&
KCM        03         1000000&0A                                  3000000&0&
KSM        1120000&009500000&0P0000000&0&
KSM        01         1500000&0A4700000&0B                        3000000&0&
KSM        02         1500000&0A3200000&0B                        3000000&0&
KSM        03         1000000&0A                                  3000000&0&
JYS        3400000&000000000&0&0000000&0&
JYS        01         2000000&0A1900000&0B                        3000000&0&
JYS        02         1000000&0A                                  3000000&0&
JYS        03         1000000&0A                                  3000000&0&
MLD        1600000&000000000&0&0000000&0&
MLD        01         1000000&0A2600000&0B                        3000000&0&
MLD        02         1000000&0A                                  3000000&0&
MLD        03         1000000&0A                                  3000000&0&

          RELAY CIRCUIT        ELEMENT LIST

ZXA        SGN10
ZXA        SGN20
ZXB        SGN30
ZZA        BUS10
DXX        CR100
DXX        CR200
DXX        CR300
KCM        K1200
KCM        K3000
KSM        K12A0
KSM        K3A00
JYS        P1000
MLD        DS100
```

(a) Part-Class Probabilities[1]

Column	1	2	3	4
Content	Part-class[2] name	Mode number	Mode designator	Probability that the part class is in designated mode[3]

(b) Element List

Column	1	2
Content	Part-class	Element name

(c) Term List Probabilities[4]

Column	1	2	3	4	5	6
Content	Term number[5]	Element name	Must be/must not be in	Numbers of included/excluded modes	Probability that element does not satisfy condition in Columns 3 and 4[3]	Probability that the term satisfies all its conditions[6]

(1) System probability of success is printed on a separate sheet.
(2) A space is left between part-classes.
(3) In floating-point notation.
(4) This printout can be suppressed.
(5) Three spaces are left between terms.
(6) The sign on the probability is the sign of the term ("+" signs are not printed).

FIGURE 8-11

FORMAT OF CRAM III PRINTOUTS

FIGURE 8-12

CRAM III OUTPUTS

FIGURE 8-12a

CRAM III OUTPUT FOR FIGURE 8-1

RELAY CIRCUIT

LISTING OF PROBABILITIES PART CLASS BEING IN SPECIFIED STATES

PART CLASS ID.	MODE NO.	MODE DESIG.	PROB. OF MODE
ZXA	001	OP	.00000000 E 00
ZXA	002	SH	.00000000 E 00
ZXA	003	NG	.14000000 E-04
ZXA	O K		.99998600 E 00
ZXB	001	OP	.00000000 E 00
ZXB	002	SH	.00000000 E 00
ZXB	003	NG	.80000000 E-05
ZXB	O K		.99999200 E 00
ZZA	001	OP	.00000000 E 00
ZZA	002	SH	.00000000 E 00
ZZA	003	NG	.30000000 E-05
ZZA	O K		.99999700 E 00
DXX	001	OP	.65564973 E-06
DXX	002	SH	.17429998 E-06
DXX	003	NG	.00000000 E 00
DXX	O K		.99999917 E 00
KCM	001	OP	.34897439 E-05
KCM	002	SH	.59039982 E-06
KCM	003	NG	.00000000 E 00
KCM	O K		.99999591 E 00
KSM	001	OP	.23687971 E-05
KSM	002	SH	.13679990 E-05
KSM	003	NG	.00000000 E 00
KSM	O K		.99999626 E 00
JYS	001	OP	.38759924 E-05
JYS	002	SH	.00000000 E 00
JYS	003	NG	.00000000 E 00
JYS	O K		.99999612 E 00
MLD	001	OP	.12479992 E-05
MLD	002	SH	.00000000 E 00
MLD	003	NG	.00000000 E 00
MLD	O K		.99999875 E 00

FIGURE 8-12 (Continued)
CRAM III OUTPUTS

FIGURE 8-12b

RELAY CIRCUIT

DEFINITIONS OF ELEMENTS TO PART CLASSES

PART CLASS ID.	ELEMENT SYMBOL
ZXA	SGN10
ZXA	SGN20
ZXB	SGN30
ZZA	BUS10
DXX	CR100
DXX	CR200
DXX	CR300
KCM	K1200
KCM	K3000
KSM	K12A0
KSM	K3A00
JYS	P1000
MLD	DS100

FIGURE 8-12 (Continued)

CRAM III OUTPUTS

FIGURE 8-12c

RELAY CIRCUIT

LISTING OF CONJUNCTIONS AND PROBABILITIES OF THEIR OCCURRENCE

MODE DICTIONARY 1 2 3 4
OP SH NG OK

TERM NO.	ELEMENT	REQUIREMENT	PROB. REQ. IS NOT MET	PROB. CONJUNCTION OF REQ. MET
1	P1000	MUST NOT BE IN MODE 1	.38759924 E-05	
1	DS100	MUST NOT BE IN MODE 1	.12479992 E-05	
1	SGN10	MUST BE IN MODE 4	.14000000 E-04	
1	CR100	MUST NOT BE IN MODE 1	.65564978 E-06	
1	K1200	MUST NOT BE IN MODE 1 2	.40801437 E-05	
1	BUS10	MUST BE IN MODE 4	.30000000 E-05	
1	CR300	MUST NOT BE IN MODE 1	.65564978 E-06	
1	K12A0	MUST NOT BE IN MODE 1	.23687971 E-05	
				.99997011 E 00
2	P1000	MUST NOT BE IN MODE 1	.38759924 E-05	
2	DS100	MUST NOT BE IN MODE 1	.12479992 E-05	
2	SGN20	MUST BE IN MODE 4	.14000000 E-04	
2	CR200	MUST NOT BE IN MODE 1	.65564978 E-06	
2	K1200	MUST NOT BE IN MODE 1 2	.40801437 E-05	
2	BUS10	MUST BE IN MODE 4	.30000000 E-05	
2	CR300	MUST NOT BE IN MODE 1	.65564978 E-06	
2	K12A0	MUST NOT BE IN MODE 1	.23687971 E-05	
				.99997011 E 00
3	P1000	MUST NOT BE IN MODE 1	.38759924 E-05	
3	DS100	MUST NOT BE IN MODE 1	.12479992 E-05	
3	SGN10	MUST BE IN MODE 4	.14000000 E-04	
3	CR100	MUST NOT BE IN MODE 1	.65564978 E-06	
3	K1200	MUST NOT BE IN MODE 1 2	.40801437 E-05	
3	BUS10	MUST BE IN MODE 4	.30000000 E-05	
3	CR300	MUST NOT BE IN MODE 1	.65564978 E-06	
3	K12A0	MUST NOT BE IN MODE 1	.23687971 E-05	
3	SGN20	MUST BE IN MODE 4	.14000000 E-04	
3	CR200	MUST NOT BE IN MODE 1	.65564978 E-06	
				-.99995546 E 00
4	P1000	MUST NOT BE IN MODE 1	.38759924 E-05	
4	DS100	MUST NOT BE IN MODE 1	.12479992 E-05	
4	SGN30	MUST BE IN MODE 4	.80000000 E-05	
4	K3000	MUST NOT BE IN MODE 1 2	.40801437 E-05	

FIGURE 8-12 (Continued)

CRAM III OUTPUTS

FIGURE 8-12c (continued)

RELAY CIRCUIT

LISTING OF CONJUNCTIONS AND PROBABILITIES OF THEIR OCCURRENCE

MODE DICTIONARY 1 2 3 4
OP SH NG OK

TERM NO.	ELEMENT	REQUIREMENT			PROB. REQ. IS NOT MET	PROB. CONJUNCTION OF REQ. MET
4	BUS10	MUST BE IN MODE	4		.30000000 E-05	
4	CR300	MUST NOT BE IN MODE	1		.65564978 E-06	
4	K3A00	MUST NOT BE IN MODE	1		.23687971 E-05	
						.99997677 E 00
5	P1000	MUST NOT BE IN MODE	1		.38759924 E-05	
5	DS100	MUST NOT BE IN MODE	1		.12479992 E-05	
5	SGN30	MUST BE IN MODE	4		.80000000 E-05	
5	K3000	MUST NOT BE IN MODE	1	2	.40801437 E-05	
5	BUS10	MUST BE IN MODE	4		.30000000 E-05	
5	CR300	MUST NOT BE IN MODE	1		.65564978 E-06	
5	K3A00	MUST NOT BE IN MODE	1		.23687971 E-05	
5	SGN10	MUST BE IN MODE	4		.14000000 E-04	
5	CR100	MUST NOT BE IN MODE	1		.65564978 E-06	
5	K1200	MUST NOT BE IN MODE	1	2	.40801437 E-05	
5	K12A0	MUST NOT BE IN MODE	1		.23687971 E-05	
						-.99995566 E 00
6	P1000	MUST NOT BE IN MODE	1		.38759924 E-05	
6	DS100	MUST NOT BE IN MODE	1		.12479992 E-05	
6	SGN30	MUST BE IN MODE	4		.80000000 E-05	
6	K3000	MUST NOT BE IN MODE	1	2	.40801437 E-05	
6	BUS10	MUST BE IN MODE	4		.30000000 E-05	
6	CR300	MUST NOT BE IN MODE	1		.65564978 E-06	
6	K3A00	MUST NOT BE IN MODE	1		.23687971 E-05	
6	SGN20	MUST BE IN MODE	4		.14000000 E-04	
6	CR200	MUST NOT BE IN MODE	1		.65564978 E-06	
6	K1200	MUST NOT BE IN MODE	1	2	.40801437 E-05	
6	K12A0	MUST NOT BE IN MODE	1		.23687971 E-05	
						-.99995566 E 00
7	P1000	MUST NOT BE IN MODE	1		.38759924 E-05	
7	DS100	MUST NOT BE IN MODE	1		.12479992 E-05	
7	SGN30	MUST BE IN MODE	4		.80000000 E-05	
7	K3000	MUST NOT BE IN MODE	1	2	.40801437 E-05	
7	BUS10	MUST BE IN MODE	4		.30000000 E-05	

FIGURE 8-12 (Continued)

CRAM III OUTPUTS

FIGURE 8-12c (continued)

RELAY CIRCUIT

LISTING OF CONJUNCTIONS AND PROBABILITIES OF THEIR OCCURRENCE

MODE DICTIONARY 1 2 3 4
OP SH NG OK

TERM NO.	ELEMENT	REQUIREMENT	PROB. REQ. IS NOT MET	PROB. CONJUNCTION OF REQ. MET
7	CR300	MUST NOT BE IN MODE 1	.65564978 E-06	
7	K3A00	MUST NOT BE IN MODE 1	.23687971 E-05	
7	SGN10	MUST BE IN MODE 4	.14000000 E-04	
7	CR100	MUST NOT BE IN MODE 1	.65564978 E-06	
7	K1200	MUST NOT BE IN MODE 1 2	.40801437 E-05	
7	K12A0	MUST NOT BE IN MODE 1	.23687971 E-05	
7	SGN20	MUST BE IN MODE 4	.14000000 E-04	
7	CR200	MUST NOT BE IN MODE 1	.65564978 E-06	
				.99994101 E 00

FIGURE 8-12 (Continued)
CRAM III OUTPUTS

FIGURE 8-12d

RELAY CIRCUIT

PROB. OF SUCCESS IS .99999115 E 00

APPENDIX A

UNIVERSAL PART-CLASS CODES FOR CRAM

In the CRAM III program, the computer searches a dictionary to determine the part-class of an element, and then searches another part of its storage for the applicable probability of that part-class (refer to Sections 1.2, 7.3, and 8.3).

These universal part-class codes have been originated for use with CRAM, and they are listed in Table A-1. Most of the codes are for parts which were coded in previous studies, and some of the part descriptions apply primarily to parts used (and then standardized) in Saturn systems. These codes now should be used if possible, and any codes that must be originated -- because existing codes are inadequate -- should be added to the list.

The part-class codes in Table A-1 consist of three symbols and, since five is the maximum number of symbols per part-class in the present CRAM program, one space remains to identify the part location in the vehicle, and another space remains to identify the component's operating time. It is recommended that a part-class code precede location and operating-time modifiers.

Codes have been assigned with several goals in mind, as follows:

(1) An ease of recognition by the use of standard symbols or symbols which indicate the part-class name, as much as possible; e.g., Q for transistor, D for diode, R for fixed resistor, P for variable resistor (or potentiometer), N for "Not otherwise defined", and Z for signals and power busses.

(2) A decrease in the incidence of key punch errors caused by incorrect interpretation of the data written on IBM sheets, specifically by not using the letters I and O, which might be punched as numbers 1 and 0, respectively. The letters X and Y, respectively, now are used in place of the letters O and I.

(3) A decrease in key punching time by the use of all alpha (no numerical) characters. Goals (2) and (3) tend to be a check on each other.

(4) An ease of adding new codes in a logical manner, by the inclusion of one or more X's in some class codes, and where expansion to a more specific class is probable.

The large number of diode types now available makes the assignment of universal diode codes impractical, if not impossible, even though relatively few diode types may be used in a particular equipment. Here, therefore, second and third place symbols for particular diodes are only listed as examples (i.e., they are not fixed). The same type of coding should also be applied to particular transistors and vacuum tubes, as also illustrated in the table.

TABLE A-1

UNIVERSAL PART-CLASS CODES FOR CRAM

Part Code	Part
CGL	Capacitor, glass
CMA	Capacitor, mica
CPA	Capacitor, paper
CTE	Capacitor, tantalum, etched foil
CTS	Capacitor, tantalum, solid electrolytic
CXX	Capacitor
DXA	Diode, 1N645 (example only)
DRA	Diode, rectifier, 1N677 (example only)
DZA	Diode, zener, 1N473, 1N755 (example only)
DXX	Diode, general purpose
DRX	Diode, rectifier
DZX	Diode, zener
GRX	Gyro, rate
JYS	Connector, interstage
KCG	Relay, coil structure, miniature, magnetic latch
KSG	Relay, switching mechanism, miniature, magnetic latch
KCL	Relay, coil structure, miniature, mechanical latch
KSL	Relay, switching mechanism, miniature, mechanical latch
KCM	Relay, coil structure, miniature, general purpose
KSM	Relay, switching mechanism, miniature, general purpose
KCX	Relay, coil structure, general purpose
KSX	Relay, switching mechanism, general purpose
LWX	Inductor, power
LPU	Inductor, pulse
MED	Meter, electrical, dc
MLD	Lamp, indicator, dc
NPP	Transducer, variable resistance potentiometer (precision)
NST	Thrust-OK switch (calips and noncalips)
NTV	Microsyn
PWP	Resistor, variable, wirewound, precision

TABLE A-1 (continued)

Part Code	Part
QXX	Transistor, general purpose
QSW	Transistor, switching, high level
QWX	Transistor, power
RCY	Resistor, fixed, composition, insulated
RFC	Resistor, fixed, carbon film
RFM	Resistor, fixed, metal film
RFX	Resistor, fixed, film
RWX	Resistor, fixed, wirewound
RWW	Resistor, fixed, wirewound, power
RXX	Resistor, fixed
SMX	Switch, switch mechanism, manual/contact set
TSS	Transformer, signal, subminiature
TWX	Transformer, power
VXX	Tube, electron
ZXX	Signal
ZZX	Bus

APPENDIX B

MODE CONDITION COMBINATIONS
(Reference: Section 8)

In certain types of reliability studies, terms that include the same element more than once, but with the same or a different mode description, can occur. These element-condition combinations are the result of an element's being shown in more than one branch of a parallel diagram, and then being multiplied together when the terms are combined in a reliability expression.

The resultant of two or more operating mode combinations is determined in the CRAM II PHASE 3 computer program. Combinations of "not" slot and operating-condition codes and their resultants are shown in Table B-1. Positions to the right of the "not" slot have no special meaning other than to show the resulting code for each combination of operating modes.

TABLE B-1

RESULTS OF OPERATING MODE COMBINATIONS

	"Not" Slot	Operating Mode Codes			
Input 1	1	1	0	0	1
Input 2	0	1	0	1	0
Output	0	0	0	1	0
Input 1	1	1	0	0	1
Input 2	1	1	0	1	0
Output	1	1	0	1	1
Input 1	0	1	0	0	1
Input 2	0	1	0	1	0
Output	0	1	0	0	0

Under certain conditions, the result (i.e., excluding the "not" slot column) consists of all zeros. When this happens, the entire term is deleted because the operating conditions are not compatible. For example, this would happen if the same element appeared twice in the same term, with one set of conditions coded "not open" and the other set coded "open".

To illustrate operation of the PHASE 3 program, hypothetical terms were originated. Cards representing input terms are shown in Table B-2 (a), and cards representing the output of PHASE 3 are shown in Table B-2 (b). In each case, element names are five symbols in length and operating modes are "open, short, not ok", and "ok", shown here in that order (see Table 8-1) Terms containing incompatible combinations have been deleted.

TABLE B-2

EXAMPLES OF TERMS CONTAINING THE SAME ELEMENT MORE THAN ONCE

(a)

OPERATING CONDITION COMBINATIONS - CRAM II PHASE 3 INPUT

```
0001    &BUS1000001K1A0011000K1A0011000
0002    &BUS1000001K1A0011100K1A0011000
0003    &BUS1000001K1A0011000K1A0000100
0004    &BUS1000001K1A0010100K1A0001000
0005    &BUS1000001K1A0011000K1A0001000
0006    &BUS1000001K1A0010100K1A0000100
0007    &BUS1000001S1G1000001S1G1000001
0008    &BUS1000001S1G1000010S1G1000010
0009    &BUS1000001S1G1000010S1G1000001
```

(b)

OPERATING CONDITION COMBINATIONS - CRAM II PHASE 3 OUTPUT

```
0001    &BUS1000001K1A0011000
0002    &BUS1000001K1A0011100
0003    &BUS1000001K1A0000100
0004    &BUS1000001K1A0001000

0007    &BUS1000001S1G1000001
0008    &BUS1000001S1G1000010
```

APPENDIX C

PROBABILITY OF A RELAY CONTACT CONDUCTING CURRENT WHEN NOT REQUIRED

One CRAM problem encountered during some studies at ARINC Research Corporation was the evaluation of the probability of a false signal. In numerous cases, a false signal is caused by current flowing through a shorted relay contact, or through a contact closed by a false signal from another circuit or component. A representative circuit for which an evaluation might be performed is shown in Figure C-1, and its "false signal" CRAM diagram is shown in Figure C-2. A correct output signal for the circuit shown in Figure C-1 is generated when Signal #1 energizes K1, closing K1A.

FIGURE C-1

REPRESENTATIVE RELAY CIRCUIT

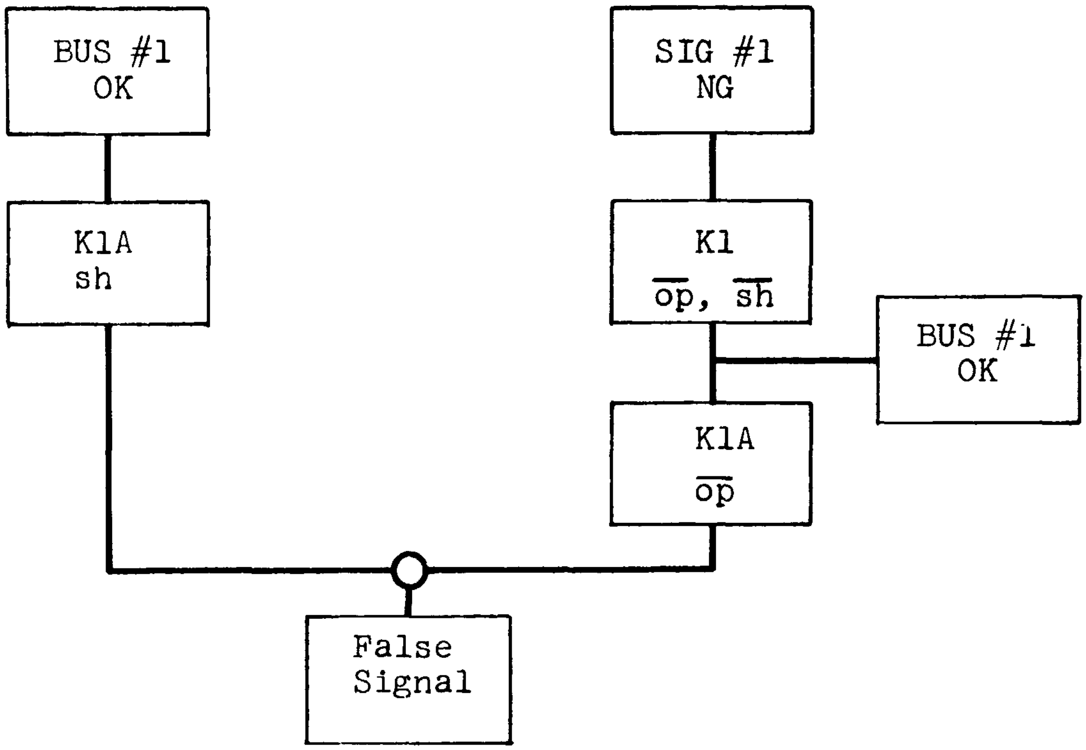

FIGURE C-2

"FALSE SIGNAL" CRAM DIAGRAM FOR FIGURE C-1

The nomenclature used in Figure C-2 is:

BUS #1/OK	BUS #1 must not fail
K1A/sh	Relay contact must fail short
SIG #1/NG	Signal #1 must be false
$K1/\overline{op},\overline{sh}$	Relay coil must not be open or short
$K1A/\overline{op}$	Relay contact must not be open

The derivation of the probability expression for the false signal is easier to discuss if Figure C-2 is simplified. The blocks representing BUS #1 will be temporarily ignored since they are in both branches, and the probabilities of the remaining components will be defined as follows:

$$\text{Prob (K1A/sh)} = P_{sh}$$

$$\text{Prob (K1A/}\overline{op}) = P_{\overline{op}}$$

$$\text{Prob (Sig \#1/NG)} \times \text{Prob (K1/}\overline{op}, \overline{sh}) = P_F$$

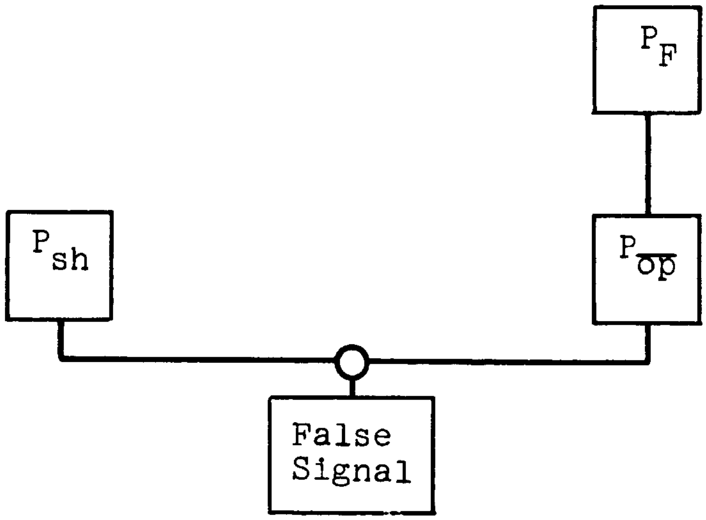

FIGURE C-3

SIMPLIFICATION OF FIGURE C-2

Since P_{sh} and $P_{\overline{op}}$ are probabilities for the same item (i.e., K1A), and since the "short" mode is included in the "not open" mode (i.e., $P_{\overline{op}} = P_{sh} + P_{OK}$), these probabilities are not mutually exclusive. To apply basic probability theory that involves a combination of events, the following mutually exclusive events are defined:

F	Signal #1 is available falsely
$\overline{F}$	Signal #1 is not available falsely
OK	Contact K1A does not fail
op	Contact K1A fails open
sh	Contact K1A fails short

With these definitions, the following combinations of mutually exclusive events can occur:

(1)	F and OK
(2)	$\overline{F}$ and OK
(3)	F and op
(4)	$\overline{F}$ and op
(5)	F and sh
(6)	$\overline{F}$ and sh

Combinations 1, 5, and 6 lead to a false output signal and any one gives

the Probability of a False Signal

$$= P(F,OK) + P(F,sh) + P(\overline{F},sh)$$
$$= P_F P_{OK} + P_F P_{sh} + (1-P_F) P_{sh}$$
$$= P_F (P_{OK} + P_{sh}) + P_{sh} - P_F P_{sh}$$
$$= P_{sh} + P_F P_{\overline{op}} - P_F P_{sh} \qquad (1)$$

It is obvious that Expression (1) can be written in several forms. However, the form shown above is the form of the CRAM output. This output is determined in the following manner. The CRAM II input is

$$P_{sh} \vee (P_F \times P_{\overline{op}})$$

which is expanded to

$$P_{sh} + P_F \times P_{\overline{op}} - P_{sh} \times P_F \times P_{\overline{op}} \qquad (2)$$

The last, or negative, term is reduced to

$$P_{sh} \times P_F \qquad (3)$$

in the computer, and thus the correct expression has been derived.

The last term of the expression could have been determined by replacing $P_{\overline{op}}$ in the last term of (2) with its equivalent. That is,

$$P_F \times P_{sh} \times P_{\overline{op}}$$

$$= P_F \times P_{sh} \times (1 - P_{op})$$

$$= P_F \times P_{sh} - P_F \times P_{sh} \times P_{op} \qquad (4)$$

Since contact K1A cannot fail short and open at the same time,

$$P_F \times P_{sh} \times P_{op} = 0$$

and Expression (4) reduces to Expression (3). Similarly

$$= P_F \times P_{sh} \times P_{\overline{op}}$$

$$= P_F \times P_{sh} \times (P_{OK} + P_{sh})$$

$$= P_F \times P_{sh}$$

because K1A cannot fail short and be OK at the same time.

To return to the original circuit and the CRAM diagram of Figure C-2, the CRAM II input is shown in Figure C-4 when the following codes apply:

BUS #1/OK	BUS1000001
K1A/sh	K1A0000100
SIG #1/NG	SIG1000010
K1/ $\overline{op}$, $\overline{sh}$	K100011100
K1A/ $\overline{op}$	K1A0011000

The computer operations can now be followed to the output of CRAM II by an analysis of the IBM printouts shown in Figure C-4. The computer performs the selective cancelling operation by comparing the operating-condition codes for the identical elements. This operation is explained in Appendix B.

If the required operating mode of K1A (in the right-hand branch of Figure C-2) is changed from "not open" to "not open, not short", the expression for the probability of a false signal will be the same as Expression (1). To show this:

The Probability of a False Signal

$$= P_{sh} + P_F \times P_{\overline{op},\overline{sh}} - P_{sh} \times P_F \, P_{\overline{op},\overline{sh}}$$

FIGURE C-4

CRAM II INPUTS AND OUTPUTS FOR PHASES 1-3

```
          FALSE SIGNAL          INPUT TO CRAM II - PHASE 1

%BUS1000001&K1A0000100,SIG1000010&K100011100&BUS1000001&K1A0011000¤

          FALSE SIGNAL          OUTPUT OF PHASE 1 - INPUT TO PHASE 2

02  1     BUS1000001
02  1     K1A0000100
03  1     SIG1000010
03  1     K100011100
03  1     BUS1000001
03  1     K1A0011000
04       &02&03-02X03

          FALSE SIGNAL          OUTPUT OF PHASE 2 - INPUT TO PHASE 3

0001     &BUS1000001K1A0000100
0002     &SIG1000010K100011100BUS1000001K1A0011000
0003     -BUS1000001K1A0000100SIG1000010K100011100BUS1000001K1A0011000

          FALSE SIGNAL          OUTPUT OF PHASE 3 - INPUT TO CRAM III

0001     &BUS1000001K1A0000100
0002     &SIG1000010K100011100BUS1000001K1A0011000
0003     -BUS1000001K1A0000100SIG1000010K100011100
```

But the last term reduces to "O" because K1A cannot fail "short" and be "not short" at the same time. Then, since

$$P_{\overline{op},\overline{sh}} = 1 - (P_{op} + P_{sh}) = 1 - P_{op} - P_{sh} = P_{\overline{op}} - P_{sh},$$

the probability of a False Signal

$$= P_{sh} + P_F \times P_{\overline{op},\overline{sh}}$$

$$= P_{sh} + P_F \times (P_{\overline{op}} - P_{sh})$$

$$= P_{sh} + P_F \times P_{\overline{op}} - P_F \times P_{sh} \qquad (5)$$

which is equal to Expression (1).

Close examination of the CRAM II PHASE 1 output in Figure C-4 might lead to the assumption that one or more cards corresponding to element series 01 have been lost. However, no cards were punched with 01 in the first two columns (since this coding is reserved for elements in series with the output). Since no elements are shown directly in series with the output in Figure C-2, the first series of elements is coded 02.

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APPENDIX D

RELAY-ENERGIZING SIGNAL-RELAY CONTACT COMBINATIONS

1. Introduction

Relay circuits can be designed with several combinations of energizing and output signals. For example, a relay may be energized by some sensor that senses a signal, and the relay contacts may then either connect or disconnect an electrical power source from an indicator. Four combinations of energizing signals and relay contact arrangements are listed in Table D-1, and a representative circuit is shown in Figure D-1. In Table D-1, 0 represents the desired absence of a signal; 1 represents the desired presence of a signal.

TABLE D-1

RELAY-ENERGIZING SIGNAL-RELAY CONTACT COMBINATIONS

Combination	A	B	C	D
Normal Sensor Output	0	0	1	1
Activated Sensor Output	1	1	0	0
Relay Contact	NO	NC	NO	NC
Normal Circuit Output	0	1	1	0
Circuit Output with an Activated Sensor	1	0	0	1

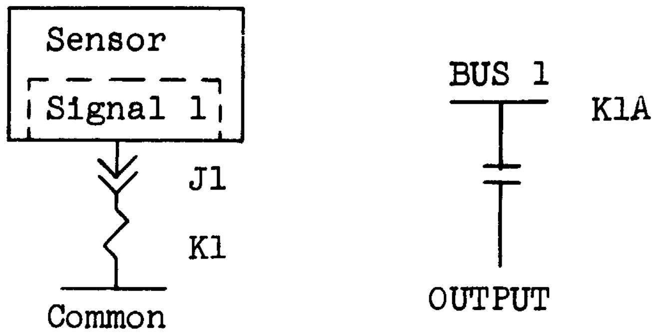


FIGURE D-1

EXAMPLE OF A RELAY CIRCUIT

If the only operating modes that are considered for each element are success and failure (i.e., only a single failure rate is to be applied to each element), then the probability for successful operation of the circuit is simply the product of the success probabilities for each element. However, when various operating modes or failure states (e.g., open, short, etc.) are to be considered, the analysis can be much more complicated. For the analyses in this appendix, failure modes "open" and "short" will be considered for physical (hardware) items (except that only "failed open" will be considered for J1), and failure mode "no good" will be considered for the sensor signal and bus.

Such an analysis can be complicated by the use of operating modes and the requirement to analyze two types of signals. Just such an analysis is presented here, however, to standardize the procedure to be followed. Problems of this type have been encountered in previous studies in which the probability of obtaining a correct signal and the probability of obtaining a false signal were analyzed and computed. A separate diagram was drawn for each case, and the probability for each case was computed separately.

2. <u>Combination of a Normally Open Contact Closed by a Sensor Signal</u>

A circuit represented by Combination A, of Table D-1, will have an output if a nonfailed bus is connected to the output by relay contact K1A. A correct signal results when a proper sensor signal causes K1A to be closed, and a false signal results if K1A shorts or if K1A is caused to close by an improper sensor signal. CRAM diagrams for these two cases are shown in Figure D-2.

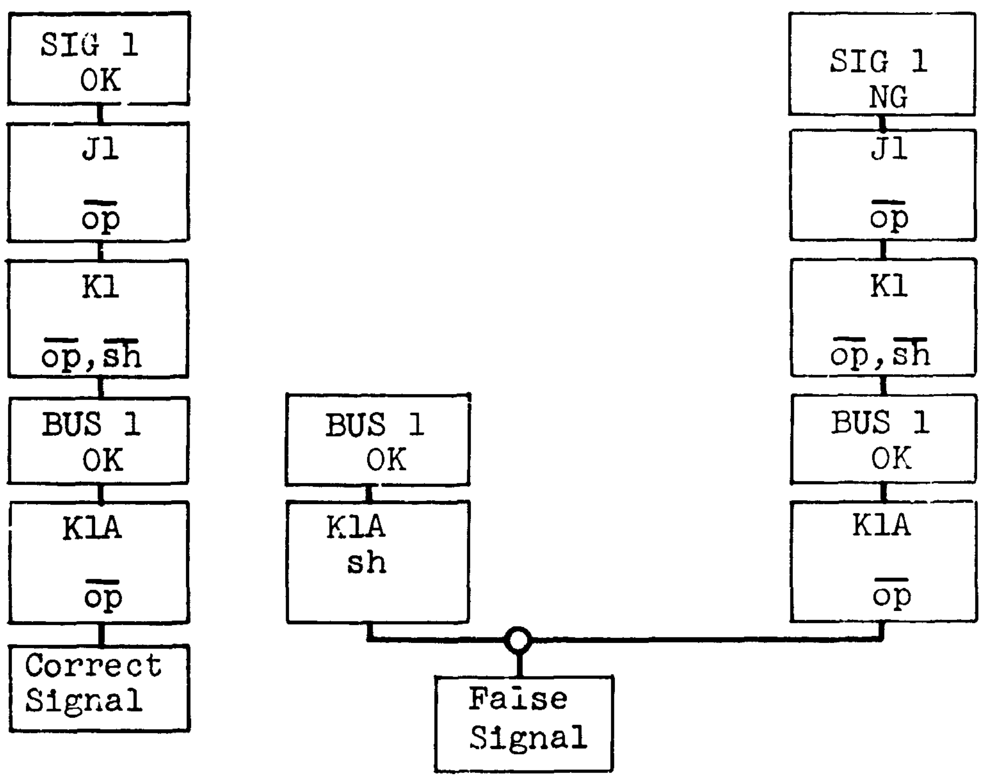


FIGURE D-2

COMBINATION A--NORMALLY OPEN CONTACT CLOSED BY APPLICATION OF SENSOR SIGNAL

The analyst starts by drawing the output block representing the correct or false signal. The first question then is:

"What element outputs are needed to enable the system to operate?"

Next, "What combination of inputs does this element need to be able to function?"

Finally, since the input to one element is the output of a preceding one, the question is, "How must this (preceding) element operate to provide the outputs required as inputs to the element just examined?"

By asking this sequence of questions for each element, the analyst is automatically guided into the construction of reliability diagrams in which the blocks define explicitly the permissible operating modes of elements, and in which all series-parallel systems produce tree diagrams.

For the correct signal case, it is obvious that the relay contact K1A must not fail open if the bus is to be connected to the output. A block is drawn above the output block and the name, K1A, and its required condition are entered in it. Each preceding element is evaluated and represented by a block in this sequential manner.

The false signal case for combination A is similar to that discussed in Appendix C, and it will not be discussed here.

3. <u>Combination of Normally Closed Contact Opened by the Sensor Signal</u>

The correct output of a circuit represented by Combination B, Table D-1, is the removal of the output voltage when Sensor 1 applies a signal energizing K1. A false output signal can occur if Bus 1 fails, the relay contact fails open, or a false Sensor 1 signal is applied to the relay coil. CRAM diagrams for correct- and false-signal cases are shown in Figure D-3. The correct-signal diagram is shown as it would be drawn by use of the rules set forth in Section 1 of this appendix.

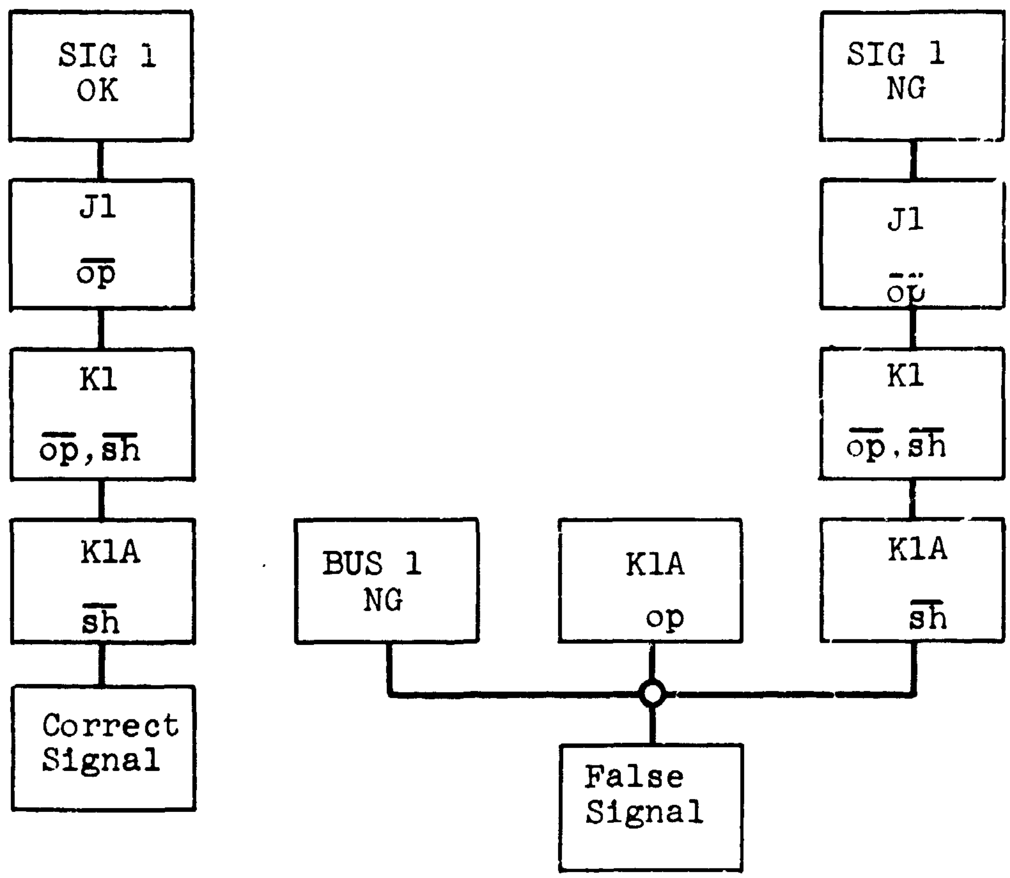


FIGURE D-3

CRAM DIAGRAMS FOR COMBINATION B -- NORMALLY CLOSED CONTACT OPENED BY APPLICATION OF SENSOR SIGNAL

The false-signal diagram for Combination B is more complicated than the false-signal diagram for Combination A. A BUS failure, or an open failure of K1A, will originate a false-signal regardless of the condition of any other element. Therefore, blocks that represent failure of BUS 1 (BUS1/NG), and an open failure of K1A (K1A/op), are shown such that either can cause a false signal. The false signal can also be generated by a false Sensor 1 signal (SIG1/NG), energizing K1 and opening K1A. This event is shown as the third, or right-hand, branch in the false-case diagram.

The probability of a false signal is derived by the use of the following terminology:

$$P_{\bar{B}} = \text{Probability of BUS 1/NG}$$

$$P_{op} = \text{Probability of K1A/op}$$

$$P_{\overline{sh}} = \text{Probability of K1A}/\overline{sh}$$

$$P_F = \text{Probability of SIG 1/NG} \times \text{Probability of J1}/\overline{op} \times \text{Probability of K1}/\overline{op},\overline{sh}$$

Then the Probability of a False Signal

$$= P_{\bar{B}} + P_{op} + P_F\, P_{\overline{sh}} - P_{\bar{B}}\, P_F\, P_{\overline{sh}} - P_{op}\, P_F\, P_{\overline{sh}} - P_{\bar{B}}\, P_{op} + P_{\bar{B}}\, P_{op}\, P_F\, P_{\overline{sh}}$$

$$= P_{\bar{B}} + P_{op} + P_F\, P_{\overline{sh}} - P_{\bar{B}}\, P_F\, P_{\overline{sh}} - P_F\, P_{op} - P_{\bar{B}}\, P_{op} + P_{\bar{B}}\, P_F\, P_{op}$$

$$= P_B + P_{op} + P_F\, P_{\overline{sh}} - (1-P_B)\, P_F\, P_{\overline{sh}} - P_F\, P_{op} - P_{\bar{B}}\, P_{op} + (1-P_B)\, P_F\, P_{op}$$

$$= P_{\bar{B}} + P_{op} + P_F\, P_{\overline{sh}} - P_F\, P_{\overline{sh}} + P_B\, P_F\, P_{\overline{sh}} - P_F\, P_{op} - P_{\bar{B}}\, P_{op} + P_F\, P_{op} - P_B\, P_F\, P_{op}$$

$$= P_{\bar{B}} + P_{op} + P_B\, P_F\, P_{\overline{sh}} - P_{\bar{B}}\, P_{op} - P_B\, P_F\, P_{op} \qquad \text{(D1)}$$

where

$P_{op}\, P_{\overline{sh}} = P_{op}$, as shown in Appendix C.

To show that this is the correct answer, the following terms are defined:

B	BUS 1/OK
$\bar{B}$	BUS 1/NG
F	SIG 1/NG
$\bar{F}$	1 - F
OK	$K1A/OK = K1A/\overline{op}, \overline{sh} = 1 - K1A/op - K1A/sh$
op	K1A/op
sh	K1A/sh

Then Table D-2 can be set up to show all mutually exclusive combinations and the circuit output for each combination.

TABLE D-2

TABLE OF OPERATING-CONDITION COMBINATIONS
COMBINATION B

[Minus (-) in the B and F columns signifies "not"]

Condition			Output		Condition			Output	
B	F	K1A	Yes	No	B	F	K1A	Yes	No
		OK		x	-		OK		x
		op		x	-		op		x
		sh	x		-		sh		x
	-	OK	x		-	-	OK		x
	-	op		x	-	-	op		x
	-	sh	x		-	-	xh		x

Combinations that lead to a false signal are those for which the "No Output" column is checked. Furthermore, it can be shown that the sum of all combinations for which the B column has a minus (-) reduces to the probability of $\frac{2}{B}$ or $P_{\bar{B}}$, since all combinations of the other elements are included, that is,

$$P(\bar{B}, F, OK) + P(\bar{B}, F, op) + P(\bar{B}, F, sh)$$
$$+ P(\bar{B}, \bar{F}, OK) + P(\bar{B}, \bar{F}, op) + P(\bar{B}, \bar{F}, sh)$$

$$= P_{\bar{B}} P_F P_{OK} + P_{\bar{B}} P_F P_{op} + P_{\bar{B}} P_F P_{sh} + P_{\bar{B}} P_{\bar{F}} P_{OK} +$$

$$P_{\bar{B}}\, P_{\bar{F}}\, P_{op} + P_{\bar{B}}\, P_{\bar{F}}\, P_{sh}$$

$$= P_{\bar{B}} \left[P_F \left(P_{OK} + P_{op} + P_{sh}\right) + P_{\bar{F}} \left(P_{OK} + P_{op} + P_{sh}\right) \right] =$$

$$= P_{\bar{B}} \left(P_F + P_{\bar{F}}\right)$$

$$= P_{\bar{B}}$$

Then the Probability of a False Signal

$$= P(B,F,OK) + P(B,F,op) + P(B, \bar{F}, op) + P_{\bar{B}}$$

$$= P_B\, P_F\, P_{OK} + P_B\, P_F\, P_{op} + P_B\, P_{\bar{F}}\, P_{op} + P_{\bar{B}}$$

$$= P_B\, P_F \left(P_{OK} + P_{op}\right) + P_B\, P_{op} \left(1-P_F\right) + P_{\bar{B}}$$

$$= P_B\, P_F\, P_{\bar{sh}} + P_B\, P_{op} - P_B\, P_{op}\, P_F + P_{\bar{B}}$$

$$= P_B\, P_F\, P_{\bar{sh}} + (1-P_{\bar{B}})P_{op} - P_B\, P_{op}\, P_F + P_{\bar{B}}$$

$$= P_B\, P_F\, P_{\bar{sh}} + P_{op} - P_{\bar{B}}\, P_{op} - P_B\, P_{op}\, P_F + P_{\bar{B}} \qquad \text{(D2)}$$

It is obvious that Expression D2 is equal to Expression D1.

It also is interesting that the correct expression for a false signal will be determined from a CRAM diagram that is similar to Figure D-3, except that BUS 1 is considered in the right-hand branch.

Then the Probability of a False Signal

$$= P_{\bar{B}} + P_{op} + P_F\, P_B\, P_{\bar{sh}} - P_{\bar{B}}\, P_{op} - P_{\bar{B}}\, P_F\, P_B\, P_{\bar{sh}}$$
$$- P_{op}\, P_F\, P_B\, P_{\bar{sh}} + P_{\bar{B}}\, P_{op}\, P_F\, P_B\, P_{\bar{sh}}$$

However, $P_B\, P_{\bar{B}} = 0$, since these probabilities are not compatible (both conditions cannot occur at the same time), and $P_{op}\, P_{\bar{sh}} = P_{op}$, as shown in Appendix C.

Then the Probability of a False Signal

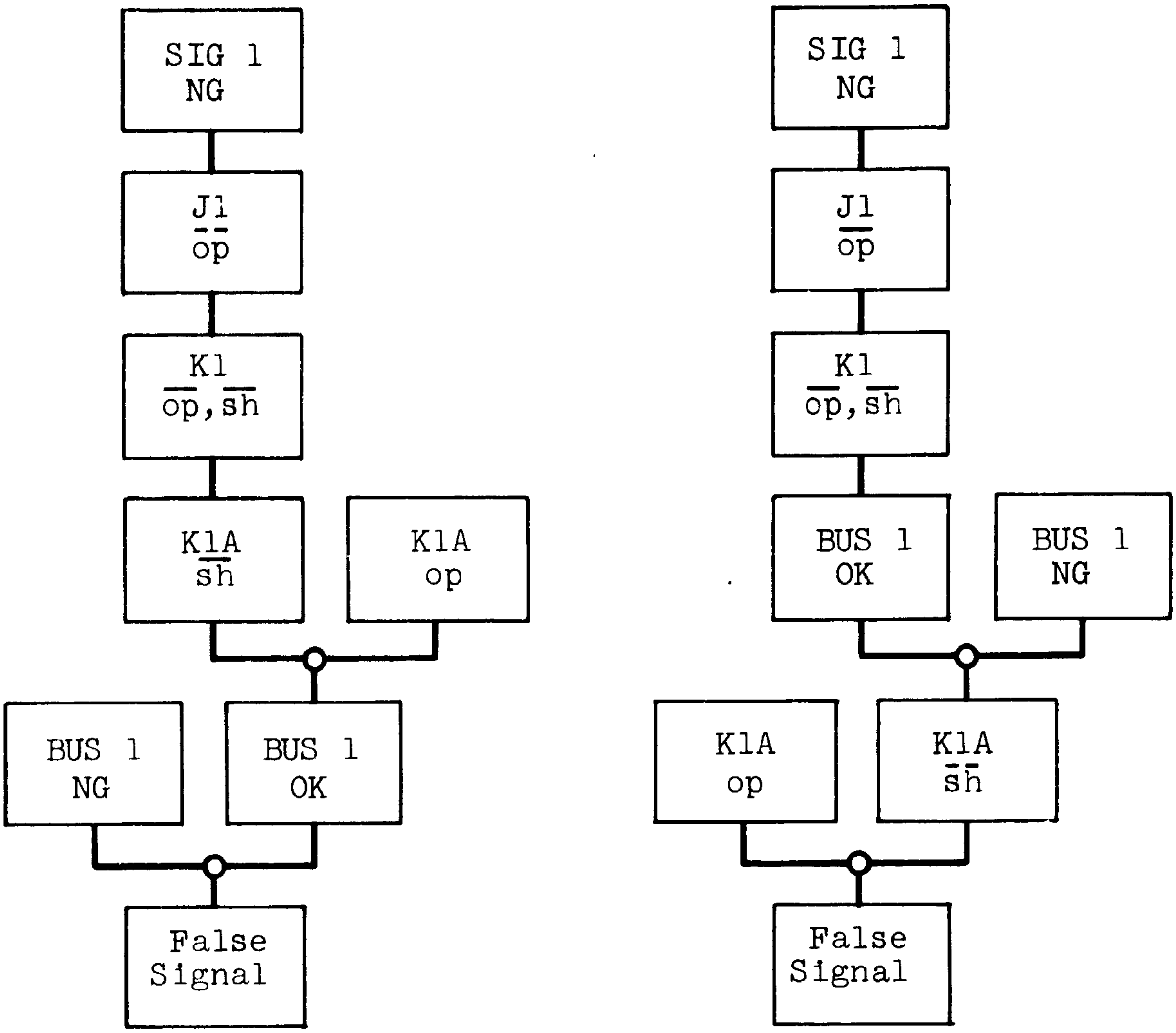
$$= P_{\bar{B}} + P_{op} + P_F P_B P_{\bar{sh}} - P_{\bar{B}} P_{op} - P_{op} P_F P_B$$

Computer operations on the terms that lead to expression D1 are basically as shown above. Terms that include P_B and $P_{\bar{B}}$ appear as follows (refer to Appendix B):

	MODE CONDITION CODES				
Condition	"Not"	op	sh	NG	OK
BUS 1/OK	0	0	0	0	1
BUS 1/NG	0	0	0	1	0
$P_B \times P_{\bar{B}}$	0	0	0	0	0

Since the result contains 0's for each condition, the term is equal to 0 and is deleted. Terms that include P_{op} and $P_{\bar{sh}}$ are analyzed by the computer as shown in Appendix C.

Other CRAM diagrams can be drawn to portray the false-signal case for Combination B. However, care should be taken that all eventualities are accounted for in the diagram. Examples are shown in Figure D-4; one leads to a correct answer, and one leads to an incorrect answer. It can be shown that the expression derived from Figure D-4(b) will have a negative term of the form $P_{\bar{B}} P_{sh}$. This term is the result of not considering the event that BUS 1 fails and K1A fails short.



(a)

This diagram leads to a correct solution.

(b)

This diagram leads to an incorrect solution

FIGURE D-4

OTHER CRAM DIAGRAMS FOR COMBINATION B

4. Combination of Normally Open Contacts Released by the Sensor Signal

A circuit represented by Combination C, Table D-1, operates properly when an activated sensor de-energizes the relay and allows a normally open contact to disconnect the power source from the output. A false signal is generated by almost any single failure, or combination of failures, of an element. CRAM diagrams for correct- and false-signal cases are shown in Figure D-5.

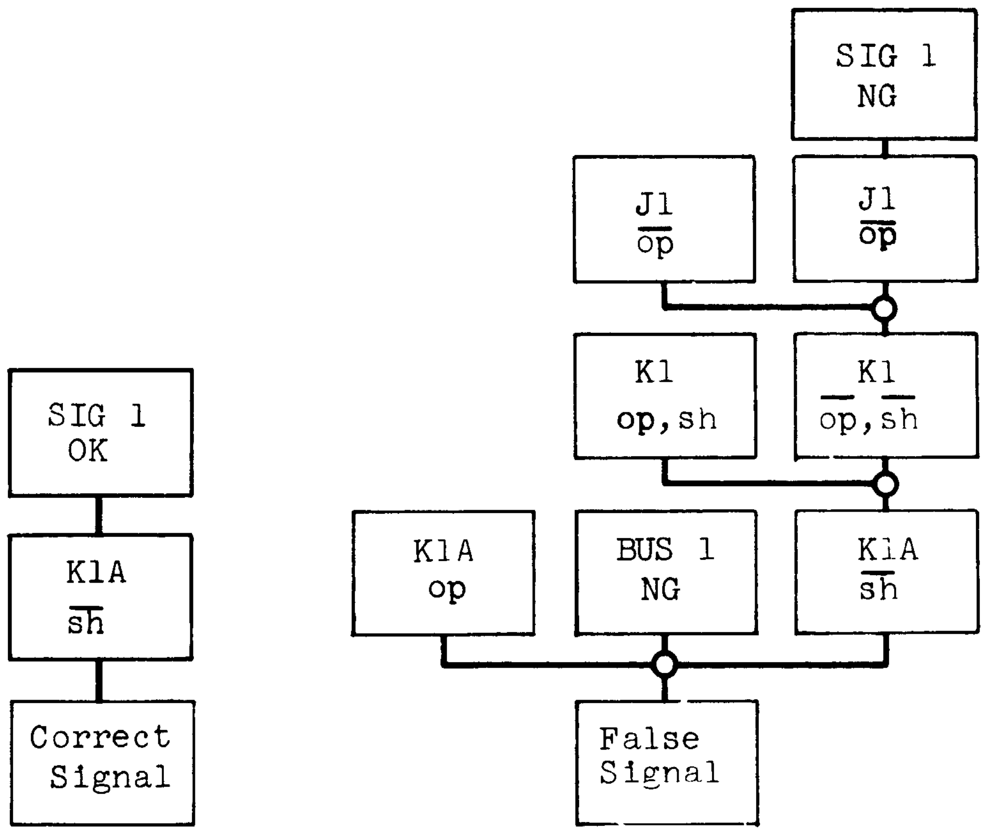


FIGURE D-5

CRAM DIAGRAMS FOR COMBINATION C -- NORMALLY OPEN CONTACT RELEASED BY APPLICATION OF SENSOR SIGNAL

The false signal diagram is drawn to show that a failure of BUS 1, or an open failure of K1A, or K1A caused to open by another failure will generate a false signal. Relay contact K1A will open (if it has not failed short) if K1, J1, or Signal 1 fails. Blocks for K1 and J1 are drawn as shown because if either of these elements fails, elements preceding them (above them in the diagram) can fail or operate properly to give a false signal.

It can be shown that the expression for the false signal case of Figure D-5 is:

Probability of False Signal

$$= P(K1A/op) + P(BUS\ 1/NG) + P_F \times P(BUS\ 1/OK) \times P(K1A/\overline{sh}) - P(K1A/op) \times P(BUS\ 1/NG) - P(K1A/op) \times P(BUS\ 1/OK) \times P_F \qquad (D\text{-}4)$$

where

$$P_F = P(Sig\ 1/NG) \times P(J1/\overline{\overline{op}}) \times P(K1/\overline{\overline{op}}) \times P(K1/\overline{op}, \overline{sh}) + P(J1/cp) \times P(BUS\ 1/NG) - P(K1/op,sh) \qquad (D\text{-}5)$$

If the conditions for K1A in the right-hand branch of Figure D-5 are changed to "not open, not short," or if BUS 1 is considered in the right-hand branch, or if both of these changes are made to Figure D-5, then the revised diagram will still lead to Expression D-4.

It can also be shown that Expression D-4 is correct by the use of a table of all mutually exclusive events similar to Table D-2 in Section 1 (except that Signal 1, J1, and K1 must be considered separately).

However, if relay coil K1 must be held energized during failure-free conditions (by current flowing through numerous connectors, diodes, or other elements), it is apparent that the number of "or" branches will equal the number of elements. As the number of "or" branches increases, the number of terms that comprise P_F in Expression D-5 increases. If more than six "or" symbols appear in the CRAM II input expression, the CRAM II computer operating time increases greatly, at least if cards are used as outputs of the subprograms. (Operating time for complicated diagrams is decreased by as much as 70% when tape programs are used.) To circumvent this operating time problem, however, the false case for Combination C usually is drawn as shown in Figure D-6.

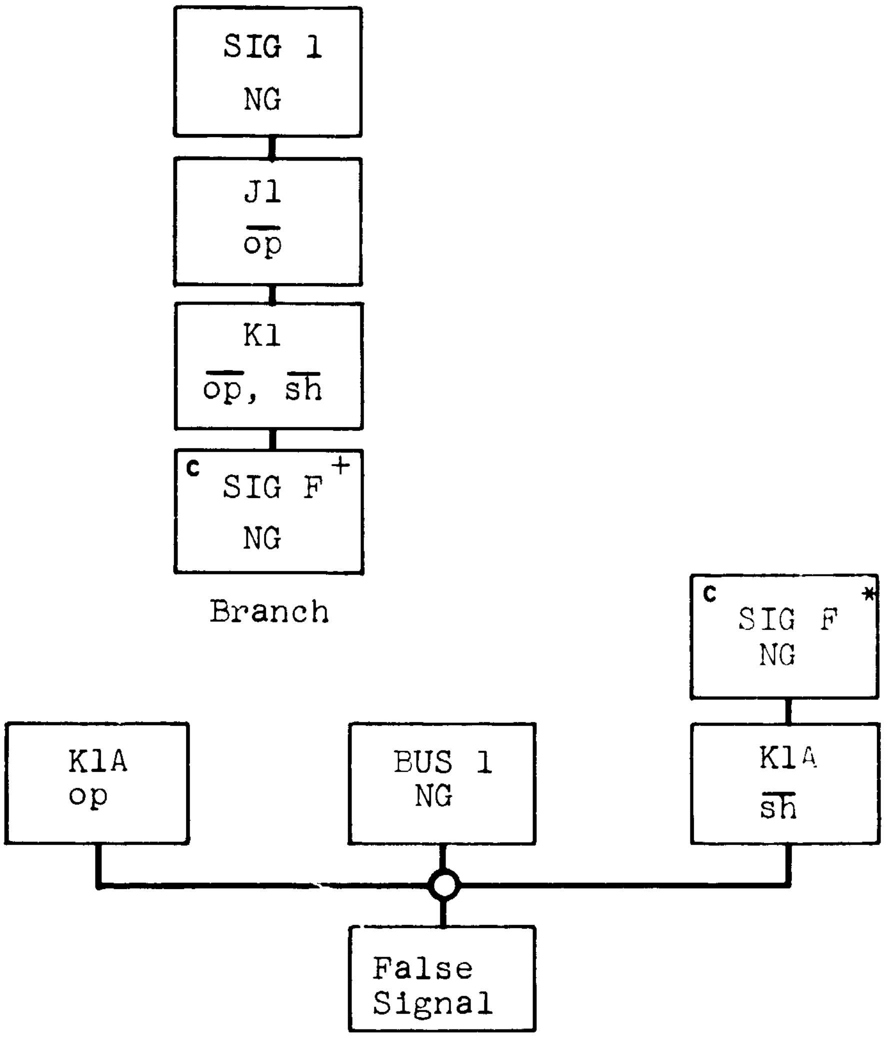


FIGURE D-6

AN ALTERNATE METHOD OF DRAWING THE CRAM DIAGRAM FOR THE FALSE-SIGNAL CASE OF COMBINATION C

The right-hand branch of Figure D-6 is drawn in response to the question, "What combination of element conditions will hold relay K1 energized"? Then, since the contacts K1A must be allowed to close, the complement of the probability that the contacts will be held open must be substituted into the expression for the false signal. In this manner, all combinations of events that will cause de-energization of the relay will be included, but the computation of the probability expression is greatly simplified. With this combination of elements, the fictitious convenience signal block (in this case SIGF) and its complement are effectively placed between the relay coil and its contact.

To show that Figure D-6 leads to Expression D-4, it must be shown that

$$
\begin{aligned}
P(\text{Sig } F/NG) &= P_F \\
&= 1 - P(\text{Sig } F/OK) \\
&= 1 - P(K1/\overline{op},\ \overline{sh},) \times \\
&\qquad P(J1/\overline{op}) \times P(\text{Sig } 1/OK)
\end{aligned}
$$

is equal to Expression D-5. Then

$$
\begin{aligned}
P_F &= 1 - P(K1/\ \overline{op},\overline{sh}) \times P(J1/\overline{op}) \times P(\text{Sig } 1/OK) \\
&= 1 - P(K1/\overline{op},\overline{sh}) \times P(J1/\overline{op}) + P(K1/\overline{op},\overline{sh}) \times P(J1/\overline{op}) \\
&\qquad \times P(\text{Sig } 1/NG) \\
&= 1 - P(K1/\overline{op},\overline{sh}) + P(K1/\overline{op},\overline{sh}) \times P(J1/\overline{op}) + P(K1/\overline{op},\overline{sh}) \\
&\qquad \times P(J1/\overline{op}) \times P(\text{Sig } 1/NG) \\
&= P(K1/op,sh) + P(K1/\overline{op},\overline{sh}) \times P(J1/op) + P(K1/\overline{op},\overline{sh}) \times \\
&\qquad P(J1/\overline{op}) \times P(\text{Sig } 1/NG).
\end{aligned}
$$

Since this expression is equal to Expression D-2, Figure D-6 leads to the correct expression.

Although this type of CRAM diagram is simpler to draw, and the correct expression is easier to derive for circuits with many elements in series, the computer cannot handle it in a single step. Therefore, the value for P(Sig F/OK) must be computed, and its complement substituted into the expression for the false signal. Consequently, the analyst must be careful that elements in the series string do not appear in other branches, or are not otherwise considered in the complete probability expression. If the same elements do appear in other branches, the reliability expression will not be correct unless all branches are represented in a single expression that is the input to the CRAM II computer program. If possible, however, the false-signal case for circuits with elements arranged as Combination C of Table D-1 should be drawn as shown in Figure D-6.

5. Combination of Normally Closed Contacts Released by the Sensor Signal

CRAM diagrams for the circuit represented by Combination D, Table D-1, are shown in Figure D-7. This circuit arrangement, and the CRAM diagrams that represent it, will not be elaborated upon because the reasons for drawing the diagrams as shown, and the derivation of the probability expressions, are similar to those discussed in Sections 3 and 4 of this appendix.

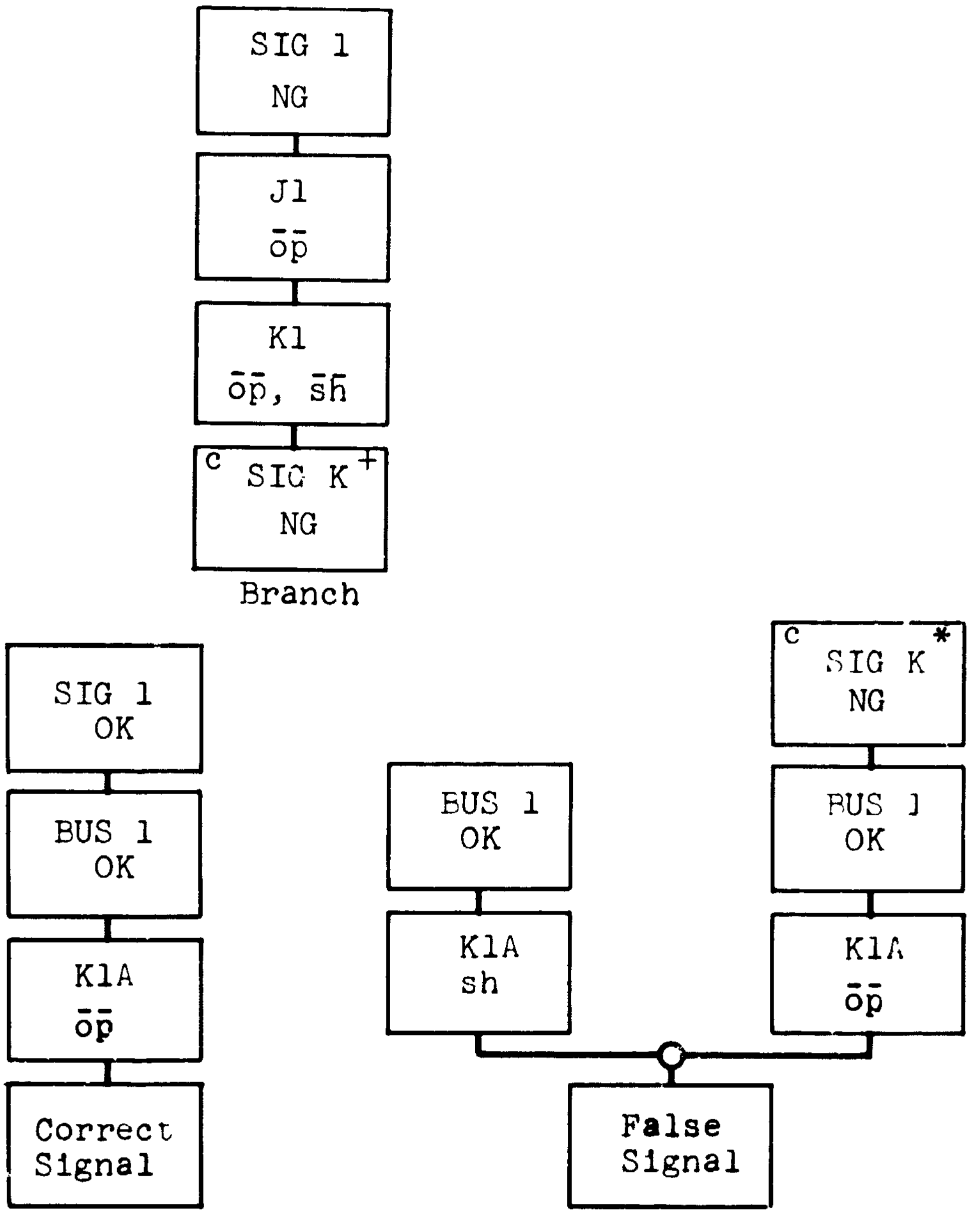


FIGURE D-7

CRAM DIAGRAM FOR COMBINATION D--NORMALLY CLOSED CONTACT RELEASED BY APPLICATION OF SENSOR SIGNAL

6. Summary

Although several CRAM diagrams can be drawn for some combinations of elements shown in Table D-1, diagrams should be drawn in a consistent manner if possible. In all cases, however, the diagrams should be constructed according to the basic CRAM rules stated in Section 1 of this appendix: drawing diagrams so that only required elements and their modes are shown, and using the complement of the probability of circuit parts when that procedure is applicable for simplicity. Table D-3 lists the figure numbers that show the suggested diagrams for the various element combinations.

TABLE D-3

FIGURE NUMBERS OF SUGGESTED CRAM DIAGRAMS FOR RELAY-ENERGIZING SIGNAL-RELAY CONTACT COMBINATION

Combination	A	B	C	D
Correct-Signal Case	D-2	D-3	D-5	D-7
False-Signal Case	D-2	D-3	D-6	D-7

APPENDIX E

USE OF CRAM FOR SYSTEMS THAT CHANGE THEIR CONFIGURATION WITH TIME

Systems that change their configuration with time have been evaluated by CRAM techniques and CRAM computer programs.

A representative study for this type of problem was the electronic system of a military fighter aircraft. Diagrams were drawn for each configuration, and the required operating times entered on failure rate cards; i.e., operating time included total cummulative "on" time up to the end of the period for which the diagram was drawn. As an example, the IFF subsystem and UHF communication set might be required to operate properly during the various flight phases shown in Table E-1.

TABLE E-1

EXAMPLE OF SUBSYSTEM REQUIREMENTS

Flight Phase	System ON Time (Hours)	Subsystem Must Operate For Total ON Time		Required Operating Time on FR Cards (Hours)	
		IFF	UHF	IFF	UHF
1	0.20	Yes	Yes	0.20	0.20
2	0.35	Yes	No	0.35	0.20
3	0.48	No	Yes	0.35	0.48
4	0.55	Yes	Yes	0.55	0.55

For this case, the problem is relatively simple because the subsystems are in a series configuration. If, however, the system is expanded to include a Data Link subsystem, and if correct system operation requires operation of <u>either</u> the UHF <u>or</u> the Data Link during some period of time, the solution is more complicated.

This alternate example might require the type of operation shown in Table E-2.

TABLE E-2

A MORE COMPLICATED EXAMPLE OF SUBSYSTEM REQUIREMENTS

Flight Phase	Subsystems Must Operate		
	IFF	UHF	UHF or Data Link
1	Yes	Yes	N/A
2	Yes	N/A	Yes
3	No	Yes	N/A
4	Yes	N/A	Yes

Given this type of operation, the next task is to define the following terms:

101 = the probability that the IFF operates during Phase 1

102 = the probability that the UHF operates during Phase 1

103 = the probability that the Data Link operates during Phase 1

201 = the probability that the IFF operates <u>to the end</u> of Phase 2

202 = etc. . . . .

.   .
.   .
.   .

Then the probability of system operation to the end of Phase 2

$$= 101 \times 201 \times 102 \times (202 \vee 203)$$
$$= 101 \times 201 \times 102 \times (202 + 203 - 202 \times 203)$$
$$= 101 \times 201 \times 102 \times 202 + 101 \times 201 \times 102 \times 203 - 101$$
$$201 \times 102 \times 202 \times 203.$$

But

$$201 = 101 \times 201$$

and

$$202 = 102 \times 202$$

201 is the probability that the IFF operated to the end of Phase 2 and, as such, this equation includes the probability that the IFF operated during Phase 1. This equality can also be shown by defining:

B02 = the probability that UHF operates during Phase 2. (Note: B02 is different from 202 by definition).

Then

$$202 = 102 \times B02$$

and

$$101 \times 202 = 102 \times 102 \times B02$$
$$= 102 \times B02$$
$$= 202$$

In a like manner,

$$201 = 102 \times 202$$

Then the probability of system operation to the end of Phase 2

$$= 201 \times 202 + 201 \times 102 \times 203 - 201 \times 202 \times 203 \qquad (1)$$

To show that Expression 1 is the correct answer, list all mutually exclusive combinations and then note those which lead to success, such as is done in Table E-3. For simplicity, subsystem 01 (IFF) is not shown on Table E-3, because the IFF must operate to the end of Phase 2. Also, if a subsystem fails during Phase 1, it cannot operate during Phase 2.

TABLE E-3

MUTUALLY EXCLUSIVE COMBINATIONS TO THE END OF PHASE 2

Proper Subsystem Operation				Success	Failure
102	103	202	203		
Yes	N/A	Yes	Yes	X	
Yes	N/A	Yes	No	X	
Yes	N/A	No	Yes	X	
Yes	N/A	No	No		X
No	N/A	No	Yes		X
No	N/A	No	No		X

If all the combinations in Table E-3 that lead to success are added, and the probabilities are combined so that

$$202 = 102 \times 202, \text{ etc.,}$$

the probability of operation to the end of phase 2

$$= 201 \times [202 \times 203 + 202 \times (1-203) + 102 \times (1-202) \times 203]$$
$$= 201 \times [202 \times 203 + 202 - 202 \times 203 + 102 \times 203 - 202 \times 203]$$
$$= 201 \times 202 + 201 \times 102 \times 203 - 201 \times 202 \times 203,$$ which is equal to Expression 1.

In a similar manner,

the probability of proper operation to end of Phase 3

$$= 201 \times 302 \times (202 \vee 203)$$
$$= 201 \times 302 \times (202 + 203 - 202 \times 203)$$
$$= 201 \times 302 + 201 \times 302 \times 203 - 201 \times 302 \times 203$$
$$= 201 \times 302,$$

which proves that the Data Link need not operate if the UHF must operate at some later period.

To utilize CRAM programs to determine the expression for configurations that change with time, letters are used to indicate the phase of the flight and the phases are evaluated in the reverse order. For example, A is used for the phase being evaluated, B for the elements in the next previous phase, etc. Then, for system operation to the end of Phase 2, the input to CRAM II is of the form

$$A01 \times B02 \times (A02 \vee A03)$$

and the output of CRAM II is of the form

$$A01 \times B02 \times A02 + A01 \times B02 \times A03 - A01 \times B02 \times A02 \times A03.$$

The CRAM II output is then processed by a computer program that eliminates element names (in each term) that refer to the same subsystem but for some previous period. The output of the computer program for <u>Phase 2</u> of the flight would then read

$A01 \times A02 + A01 \times B02 \times A03 - A01 \times A02 \times A03$, which also is equivalent to Expression 1.

This output, with the appropriate element list and failure rate cards, is then processed with the CRAM III computer program to evaluate the system probability.

In a like manner, the input to CRAM III for Phase 3 of the flight will be

B01 × A02 + B01 × A02 × B03 - B01 × A02 × B03

In this case, the equal terms are not canceled from the expression, because the computer programs do not compare terms, but only element names, within terms. Numerically, however, these terms are canceled by the CRAM III program.

In practice, the complete element name that is used in the evaluation is six symbols: three to identify the element, one for the "not" slot, and two for the operating mode codes. Operating modes were NG (No Good) and OK. A complete description, for example, would be A01001 because if the element name is included, the element must be OK or not failed. The element failure rate is listed on the failure rate card as condition 01 and, with the time, it determines the probability for condition 01 (failed) and its complement, which is condition 02, or OK. In other words,

$$P_{02} = P_{OK} = 1 - P_{01} = 1 - P_{NG}$$

because NG and OK are the only conditions considered.