Semi-Annual Report on

Computer-Aided Circuit Analysis

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Semi-Annual Report of the Research on
Digital Computer-Aided Circuit Analysis
under the NASA Grant NGR-39-023-004
covering period from May 15 to November 14, 1966

I. Bibliography Updating

A continual effort is maintained to update the "Bibliography on Computer-Aided Circuit Analysis and Design"* which was prepared in 1965 and included with revisions in the 1966 Annual Report** of this research. New entries of the titles since then are listed as follows:

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II. Evaluation Study of Available Programs -- STANPAK

The General Electric Company at Phoenix, Arizona, has developed a reliability prediction and tolerance analysis and adjustment program called STANPAK, Statistical Tolerance Analysis Package. Given a set of functions and parameters data, the program may be used to compute the nominal output values and the mean, the variance and tolerance limit for the dependent variable. It can determine the principal sources of variation, relax or tighten component tolerances until given specifications are met at a reliability level. In addition, a Monte Carlo analysis can be performed. The component values are selected randomly from their distribution and the dependent variables are computed. This procedure is repeated for a prescribed number of times and the distribution of the result is tabulated.

Because the time sharing computer facilities have been established between Villanova University and the Space Technology Center of General Electric Company at King of Prussia, Pa. for some time, a reduced version of STANPAK was put into test via the Desk Side Computer at the Villanova input terminal this summer. Operational difficulties were first experienced and then resolved. In the original writeup of STANPAK program, it has the capability to handle thirty parameters and seven different functions, a function being defined as an algebraic expression in which every variable except the dependent variable is either an input variable or a previously computed variable. In essence, each function is an equation in one unknown.

In the adaption of the program to our local operation, the control and print-out procedures have been modified. A paper entitled "A Survey of Application of Digital Computers to General Circuit Analysis", which examines STANPAK in the light of other available programs of circuit analysis such as ASAP, CIRCUS, ECAP, and NET-1, was prepared and issued as a separate technical memorandum to NASA in October, 1966. The detailed description of the changes made on the program, special notes or hints and kinks for new users, and illustrative working examples will be included in a later report.

III. Signal Flow Graphs -- Signal flow graphs (SFG) were introduced by Mason[1], and further developed by Lorens[2], Happ[3] and others.

The problem under study is the solution of network responses in the time domain using the theory of the SFG with the aid of a small digital computer (IBM-1620).

Primitive Signal Flow Graph -- Mason[1] developed the procedure for determining the primitive signal flow graph (PSFG), which was later modified by Happ[4] for digital computer programming. The PSFG is developed by considering all elements of the network under study to be composed of voltage generators and current generators. For example, a transistor circuit, base resistance, would be classified as a current generator if the base resistance current I_B develops the dependent current source BI_B. The PSFG appears better suited for development by digital computer programming, than the usual procedure of writing appropriate circuit equations and developing the SFG from these equations.

The procedure for determining a PSFG is as follows: 1) designate all elements of the network as either current generators or voltage generators; 2) choose a tree of the network topology containing all of the voltage generators, but none of the current generators; 3) determine each link-branch voltage in terms of tree-branch voltages; 4) determine each tree-branch current in terms of link-branch currents; 5) for each circuit element use two nodes, a voltage node and a current node; 6) the voltage and current transmittances are determined from steps 3 and 4; 7) the link-branch elements are connected between respective V and I nodes by admittance transmittances and the tree-branch elements by impedance transmittances. An example is given to illustrate the development of the PSFG, with some comments to indicate the algorithm used to aid in writing a digital computer program.

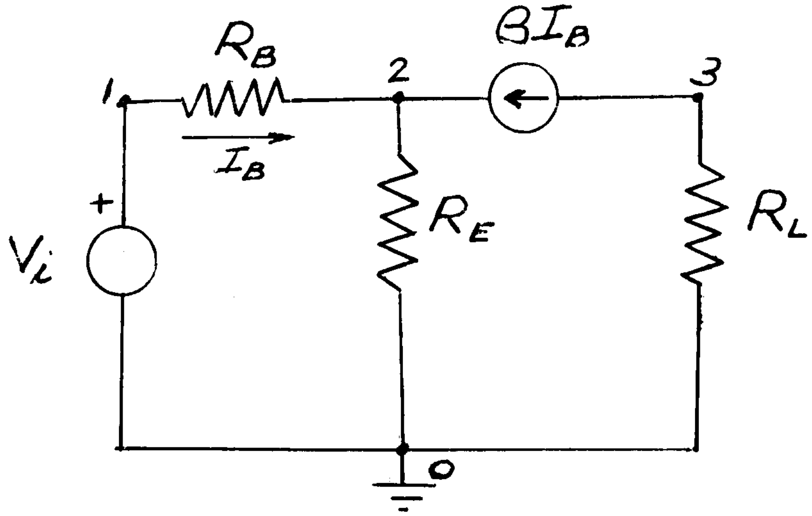

Fig. 1. Common emitter transistor amplifier circuit

The network topology is shown in fig. 2a for the equivalent circuit of fig. 1, and the tree (solid lines) and cotree (dotted lines) of fig. 2b, indicate the elements designated as voltage and current generators respectively. Each element of the network is

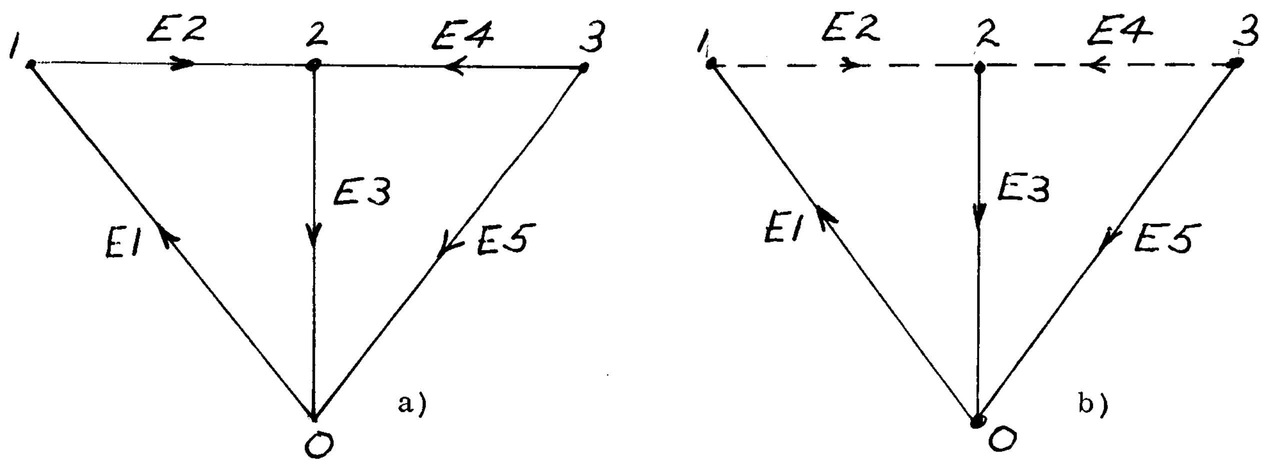

Fig. 2 Topological diagrams of Fig. 1

numbered, and the arrow indicates the direction of current with the voltage being positive on the node of the arrow head. Note that edge E2, the base resistance, is a link branch as mentioned above. Two approaches have been considered for writing a program to determine a tree. One is to select at random a combination of edges and check that it is a tree. The other approach is to search through the edges for all vertices, checking that no closed loops are formed during the search. In general many trees can be formed from a network, but restricting some of the branches to link or tree branches will reduce the number of possible tree selections.

To construct the PSFG, voltage nodes and current nodes for each circuit element are drawn as in fig. 3.

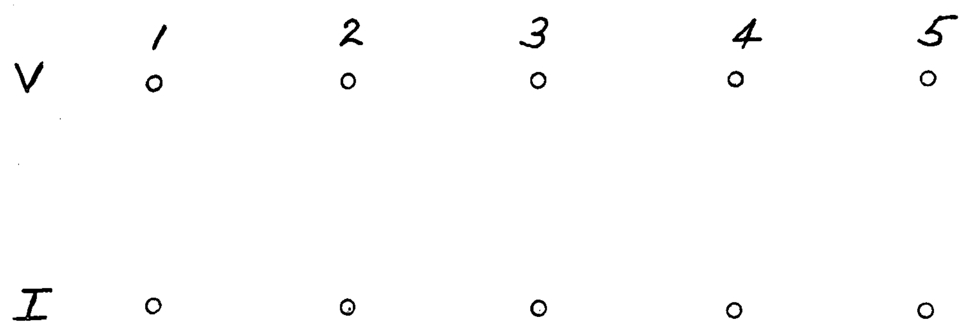

Fig. 3 Voltage and current nodes for the PSFG.

Then Kirchoff's constraints for the link-branch voltages in terms of tree-branch voltages are determined by loop equations

(1) $V_2 = -V_1 - V_3$

(2) $V_4 = V_5 - V_3$

The equations for the tree-branch currents in terms of link-branch currents are

(3) $I_1 = I_2$

(4) $I_3 = I_2 + I_4$

(5) $I_4 = BI_2$

(6) $I_5 = -I_4$

A program has been written to develop these equations, based on the concept of the incidence matrix of a circuit.

Actually since the two sets of equations are related, it is only necessary to determine one set of equations. Fig. 4 shows the nodes with the constraint transmittances added.

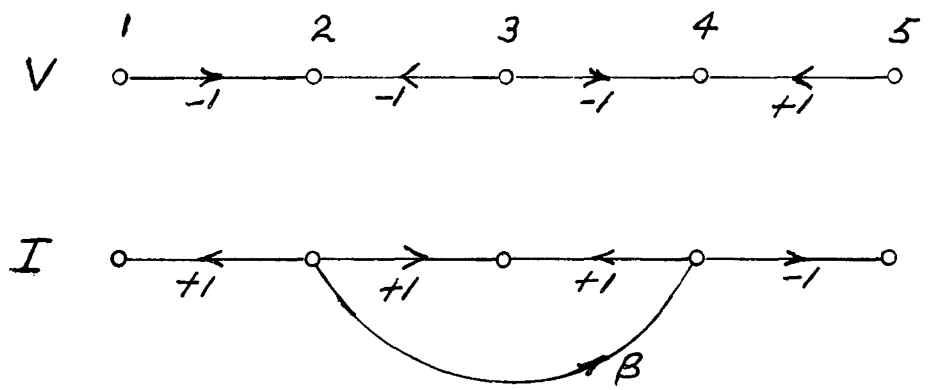

Fig. 4 Flow graph with Kirchoff's constraints

Next the passive element transmittances are added to the diagram as shown in fig. 5. The tree-branches are impedance transmittances and the link branches are admittance transmittances with the former oriented from I-nodes to V-nodes and the latter from V-nodes to I-nodes. Note that nodes V_4 and I_1 are the terminating nodes since V_1 and I_4 are sources.

The reduction of the PSFG will be done according to the node absorption procedure. A program developed by Abrahams[5] which reduces nodes consisting of transmittances that are real numbers has been modified to process transmittances that are a function of complex frequency using the non-numerical algebra.

The inverse Laplace transform to obtain the time domain response of the circuit will be done by a program based on Liou's[6] method.

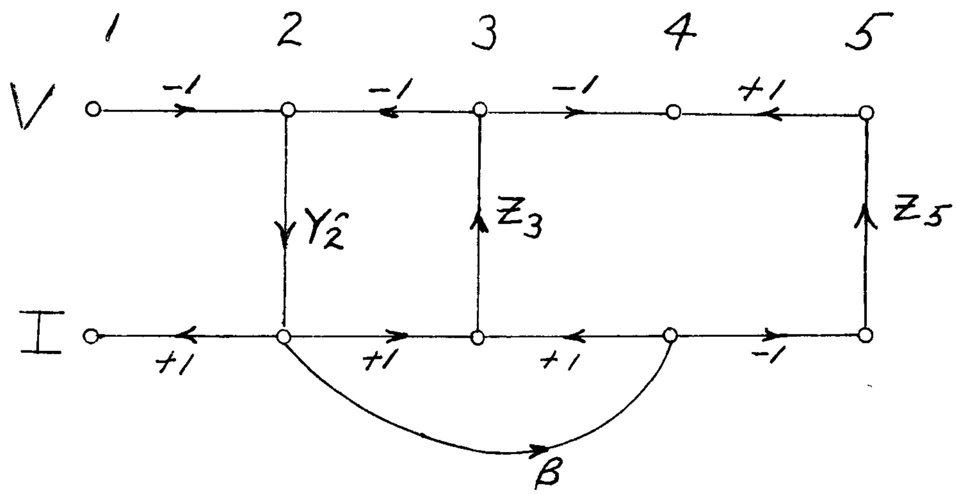

Fig. 5. The Primitive Signal Flow Graph.

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IV. Future Plans

1. Continue the signal flow-graph approach of circuit analysis within the constraints of a moderate size computer. There are three essential steps to the complete solution:

(a) development of signal flow-graph from the network topology.

(b) reduction of signal flow-graph to obtain the transfer function, and

(c) time-domain solution of the desired output quantity.

The second and third steps have been considered and they present no special difficulties. The first step seems to be the most challenging of all three in the implementation by computer programs. Inherently, the problem of realizing a proper signal flow-graph from circuit diagram possesses the same elusive features as other pattern recognition problems. It is expected that research effort will be directed toward gaining more insight into this intuitively simple problem and uncovering a method of its solution

2. Non-numerical manipulation by digital computers is an area of growing interest to the computer users. The August, 1966 issue of the Communication of the Association for Computing Machinery was devoted entirely to the papers on Symbolic and Algebraic Manipulations. As far as the circuit analysis and design is concerned, the symbolic manipulation would be useful in reducing the accumulated errors in iterative computation and optimizing the dependent variable with respect to a given set of parameters. In the method of signal flow graph analysis the non-numerican formula, once implemented in the program, will enable the analysis of a circuit to be carried out in the most generalized manner. Initial attempt on polynomial manipulations, root finding and other simple mathematical operations will gradually lead us to more interesting explorations.

3. Since the transient response of a network is the ultimate objective of circuit analysis, development and examination of new techniques in transient solution is always of direct consequence to circuit designers. The novel method proposed by Liou in

the Proceedings of the IEEE, January, 1966, deserves our serious attention and experimentation. Application of Liou's method to general circuit problems has been started and will be continued through the months to come. Eventually it will be critically compared with other classical methods of solution of ordinary differential equations as to its mertis or demertis.