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Technical Report 32-1034

Bipolar Analog-to-Pulse-Width Converter

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JET PROPULSION LABORATORY

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Abstract

This Report describes the design and application of a bipolar analog-to-pulse-width converter circuit module that was developed for the implementation of analog-to-digital conversions in spacecraft systems. The converter module, along with appropriate digital logic, has unique application in performing analog-to-digital conversions in environments where low-level measurements must be made in the presence of system noise.

Sufficient electrical and mechanical design details are given to allow the fabrication of spacecraft-quality circuit modules. The design presented has been qualified for use on the *Mariner* spacecraft and on the OGO-E and Bioscience satellites.

Bipolar Analog-to-Pulse-Width Converter

I. Introduction

This Report describes the design, development, and system implementation of a bipolar analog-to-pulse-width (A/PW) converter module for use in the analog-to-digital (A/D) portions of flight data handling systems. This design is an improved version of the A/PW converter (Ref. 1) that was used successfully in the science subsystem of the *Mariner* Mars 1964 spacecraft. The improvements to the *Mariner* Mars 1964 module include

(1) increased linearity

(2) increased temperature stability

(3) increased stability with supply variations

(4) bipolar analog input

(5) improvement in calibration techniques during fabrication

(6) higher use of JPL Preferred or Hi-Reliability parts.

II. Description of Typical Encoding System Using Bipolar A/PW Converter

A. Background

The use of an A/PW converter module has merit in systems such as those encountered in spacecraft applications where low-level analog measurements of high accuracy are often required from transducers physically separated from the data encoding equipment. The conversion of the analog voltage to a pulse-width at the transducer allows for an all-transformer coupled interface between instrument and data encoder that circumvents many of the ground noise and magnetic interference problems that tend to produce errors in low-level measurements.

B. Operation and Functional Design

The operation of the A/PW converter is such that, upon receipt of a trigger command, two output pulses are generated on separate output lines with the time difference between them being directly proportional to the analog input. The order in which the two pulses occur determines the polarity of the analog signal. Figure 1 describes this relationship.

In Fig. 1(a) the analog signal is *positive* and, therefore, output A occurs *before* output G. (Neither output pulse is coincident with the trigger command.) In Fig. 1(b) the analog signal is *negative*, so that output A now occurs *after* output G.

To complete the A/D conversion, a stable oscillator, gating circuitry and counter-shift register are needed. The A/PW converter output pulses are used to actuate a gate which allows the oscillator pulses to advance the

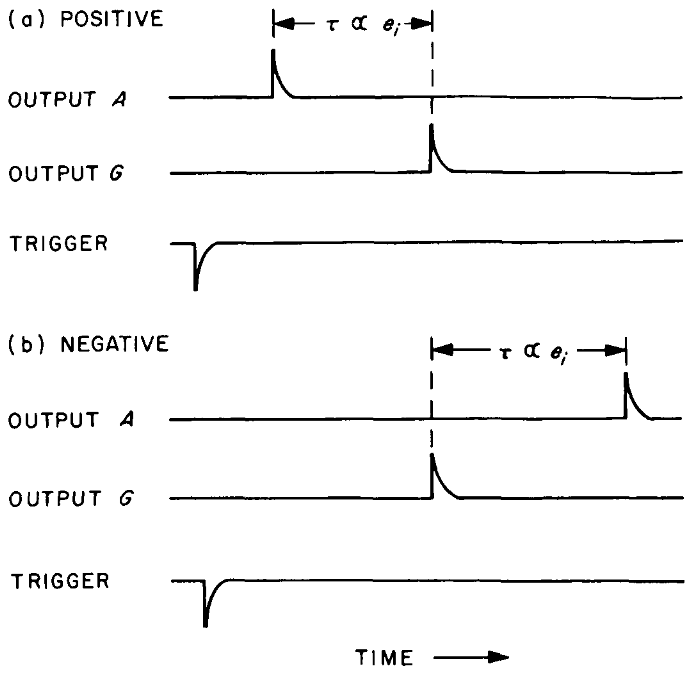


Fig. 1. Bipolar A/PW converter output relationship for analog input voltage: (a) positive; (b) negative

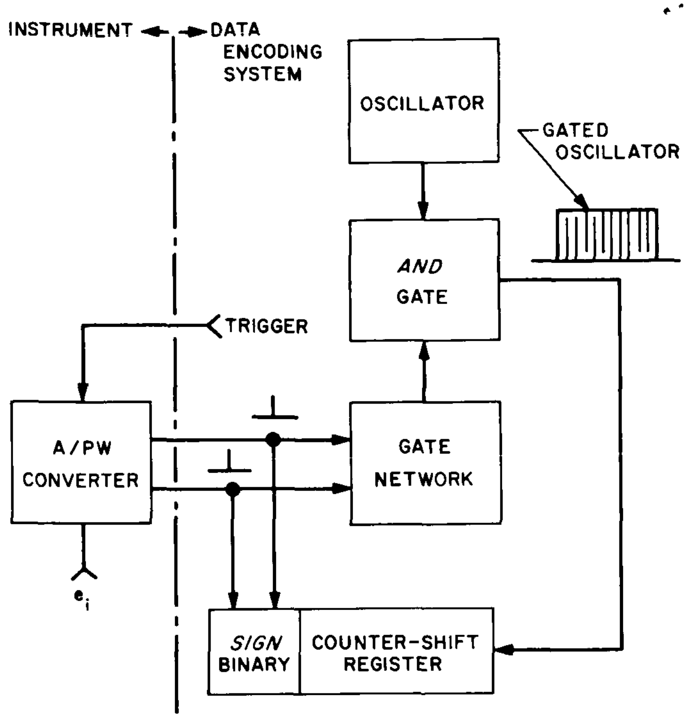


Fig. 2. A/D converter using bipolar A/PW conversion technique

counter. At the close of the gate interval, the counting operation is stopped, leaving in the counter a count which is proportional to the analog voltage being measured. The binary data may then be shifted serially out of the register.

Figure 2 shows a block diagram of an encoding system using an A/PW converter. In this illustration, the A/PW conversion is made at the analog source and only the output pulses are coupled across the interface to the data encoding logic. The gate network and oscillator are combined in a logical *and* operation to form the gated-oscillator input to the counter-shift register. The method of polarity determination shown here relies on the final pulse from the A/PW converter to establish the state of the *sign* flip-flop. The *sign* data would be shifted out serially with the accumulated count.

The output pulses from the A/PW converter do not occur synchronously with the trigger command. This characteristic leads to a problem in that the total system quantizing error will be plus or minus one count, in the least significant digit, instead of the usual plus or minus one-half count that one finds in most digital systems. This error occurs because the leading and trailing edges of the gate are not synchronous with the oscillator, hence it is possible for a full *bit* error to occur at either edge. This problem may be overcome in one of two ways:

(1) Provide a separate oscillator for the A/D conversions and use the leading edge of the gate to turn the oscillator on at a predetermined point in the cycle to achieve synchronization.

(2) For an n *bit* conversion accuracy, encode to $n + 1$ but shift out only the n *bits* that are most significant. This can be accomplished very simply by inserting a scale-of-two circuit between the gated oscillator and counter-shift register input as shown in Fig. 2.

III. Description of the Bipolar A/PW Converter

A. Functional Design and Operation

The A/PW converter uses the familiar "ramp comparison" technique to implement the conversion. Figure 3 shows a functional block diagram of the converter. The description of operation is as follows: Upon receipt of a trigger command, the control circuitry, by "enabling the bootstrap circuit", allows the sweep to begin. The sweep voltage is compared with the analog input voltage in the analog comparator and with zero volts in the ground comparator. When equivalence is detected, an output pulse is generated in the appropriate channel. The sweep will continue to decrease linearly until the voltage reaches −6.5 v. At this time, the control circuitry is reset

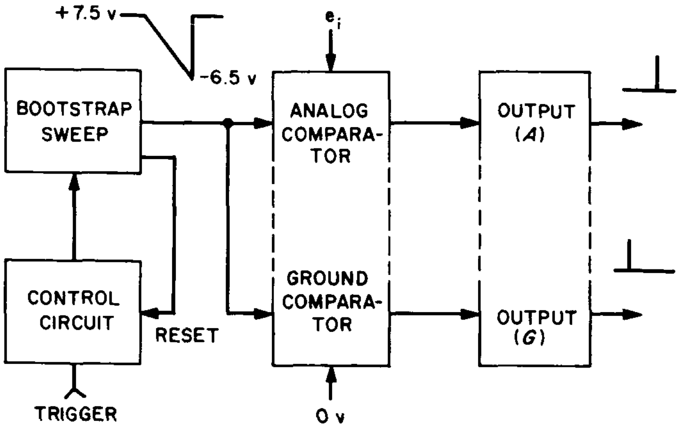


Fig. 3. Functional block diagram of the bipolar A/PW converter

and, in turn, resets the bootstrap sweep to its quiescent state. The converter will then remain reset until the next trigger command.

It is clear that a positive analog input will produce an output from Channel A before that of Channel B, and vice versa if the input is negative. The time difference between the two outputs is proportional to the absolute value of the ratio of analog input voltage to sweep slope.

$$\tau = \left| e_i \frac{\Delta t}{\Delta e_c} \right| \qquad (1)$$

where

τ = time difference

e_i = analog input voltage

$\dfrac{\Delta e_c}{\Delta t}$ = sweep slope

The terminal characteristics and general specifications of the A/PW converter are listed in Table 1.

Table 1. Bipolar A/PW converter specifications

Characteristics	General specifications
Analog input	+6 to −6 v
Data output	Data output is the time difference measured between two voltage pulses occurring on separate output lines. Polarity of the analog input is determined by noting order in which pulses occur. Full-scale output from several hundred microseconds up to approximately ten milliseconds is attainable through proper component selection during fabrication process.
Conversion accuracy	±0.05% of full-scale
Conversion stability	±0.3% of reading ± 2.5 mv over the temperature range −10 to +80°C
Linearity	0.05%
Trigger	2.5 v min negative step, $t_f \leq 0.3 \mu$sec
Supply voltage	+15 and −15 v ± 10% tolerances
Power consumption	75 mw (approximate)
Operating temperature	−10 to +80°C
Sample rate	500 samples/sec max
Component count	75

B. Electrical Design and Operation

1. Control circuitry. The function of the control circuitry shown in Fig. 4 is to (1) initiate the sweep, (2) detect the end of the conversion cycle, (3) reset the pulse-forming network in the output stage, and (4) reset the bootstrap sweep.

Transistors Q6 and Q7 form a flip-flop network while Q5 serves as a reset driver to the sweep and output circuits. Upon receipt of a negative trigger command, Q6 is switched off and Q7 is switched on. This in turn switches Q5 from a saturated state to a nonconducting state. The result is a change in the output of the reset driver from +15 to 0 v that allows the sweep cycle to begin.

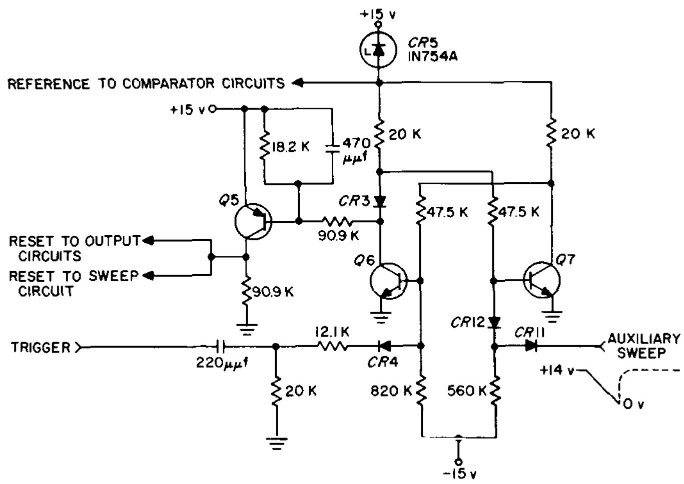


Fig. 4. Bipolar A/PW converter control circuitry

An auxiliary output from the sweep circuit is used to reset the control flip-flop at the end of the sweep cycle. This auxiliary sweep is offset from the main sweep by about 7 v in the positive direction and serves to turn transistor $Q7$ off by diverting $Q7$ base current through $CR11$ and $CR12$ as the sweep potential passes through ground. With the resetting of the control flip-flop, the output of the reset driver returns to a +15 v state. This condition drives the sweep circuit to its quiescent state and recharges the pulse network in the output stage.

2. ***Bootstrap sweep.*** The function of the sweep circuit is to provide a linear voltage ramp for comparison with the analog input voltage. A bootstrap circuit was chosen for this application because of its excellent linearity, and because of the simplicity and ease of temperature compensation to which the design lends itself.

Figure 5 shows a simplified functional diagram of the bootstrap circuit. When the positive 15-v clamp from the control circuitry is removed, the capacitor C is allowed to discharge through the resistor R. The rate of discharge, hence the slope of the ramp, is determined by the potential across R. Inspection will show that this potential is nearly V_Z, the reference potential provided by the zener diode in the output stage. Since the zener is driven from a current source, and since the zener cathode is returned to e_c through the unity gain amplifier, the potential across R will remain constant at V_Z even as e_c decays. This constant potential across R results in a constant discharging current for the capacitor C. Thus, due to the bootstrap action of the resistor R and the associated feedback network, an extremely linear ramp voltage is achieved at outputs V_{s1} and V_{s2}.

If we assume that the amplifier input draws negligible current $\left(\text{i.e., } \frac{ia}{ic} \cong 0\right)$, the expression for e_c during linear discharge can be written as follows:

$$e_c(t) = \int \frac{i_c}{C}\, dt = \int \frac{-\left[e_c - (Ke_c - V_Z)\right]}{RC}\, dt$$

$$= \frac{-\left(e_c - Ke_c + V_Z\right)}{RC}\, t + \text{constant}$$

For $K = 1$

$$e_c = -\frac{V_Z}{RC}\, t + \text{constant}$$

For this application, the constant is approximately +14 v,

$$\therefore\ e_c = 14 - \frac{V_Z}{RC} t \qquad (2)$$

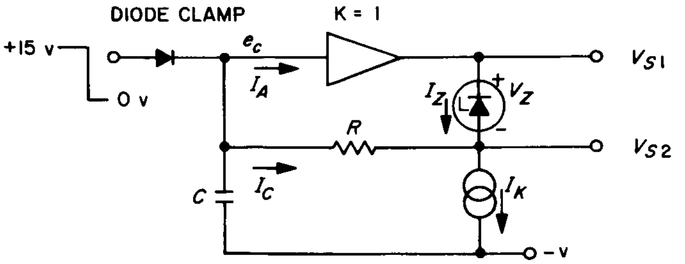


Fig. 5. Simplified functional diagram of bootstrap circuit

Figure 6 is a schematic diagram of the actual bootstrap sweep circuitry. Transistors $Q1$, $Q2$, and $Q3$ form the unity gain amplifier, while transistor $Q4$ and associated circuitry form the constant current generator. The variable resistor $R4$ allows for making five adjustments to the sweep slope after the components have been selected and fabricated into a module.

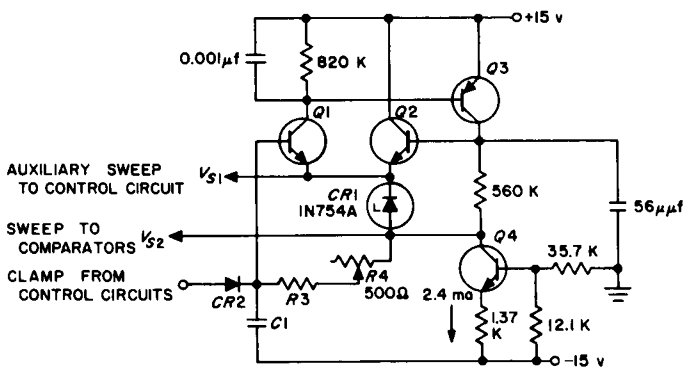


Fig. 6. Bipolar A/PW converter bootstrap sweep circuit

The expression for e_c, derived earlier, is only approximate since, in the actual circuit, there is a DC offset in the unity gain amplifier owing to the V_{BE} of transistor $Q1$. If the offset is included and the other influencing parameters taken into account, then Eq. 2 becomes

$$e_c = 14 - \left[\frac{V_{BE} + V_Z}{(R3 + R4)\, C1}\right] t \qquad (3)$$

where

V_{BE} = base emitter potential of $Q1$

V_Z = zener potential

This expression assumes that the amplifier gain is unity, and that the amplifier input current is negligible. For the practical circuit of Fig. 6, these assumptions are considered valid.

The predominant effect of amplifier gain error would be to decrease the linearity of the sweep. Thus, for maximum linearity, one desires an amplifier with a gain as close to unity as possible (Ref. 2).

The expression for e_c in Eq. 3 clearly expresses the independent variables that determine the accuracy and stability of the sweep slope. When V_{BE} and V_Z have been determined for a given sweep circuit, the value of $(R3 + R4)$ and $C1$ can be determined to yield the desired full-scale voltage input. Combining Eqs. 1 and 2 gives

$$\tau = \left| \frac{(R3 + R4)\, C1\, e_i}{V_{BE} + V_Z} \right| \tag{4}$$

for a full scale e_i of 6 v,

$$\tau_{fs} = 6 \left[\frac{(R3 + R4)\, C1}{V_{BE} + V_Z} \right] \tag{5}$$

Figure 7 is a graphic display of Eq. 5 with $(R3 + R4)$ and $C1$ as the variables.

3. ***Bootstrap sweep temperature compensation.*** The single factor that contributes most to the stability and accuracy of the converter is the slope of the sweep. Equation 4 expresses the time difference output (τ) in terms of the circuit parameters. These parameters each have a measurable temperature coefficient; and thus they make a direct contribution to the temperature stability of τ. In practice, resistors $R3$ and $R4$ and capacitor $C1$ are selected to have negligible temperature coefficients (less than $\pm$ 25 ppm/C°). Since the parameters V_{BE} and V_Z do not necessarily have selectable low temperature coefficients, the crux of the temperature compensation problem centers around these two parameters. To achieve the best overall temperature stability, it is necessary to have the change in V_{BE} offset the change in V_Z. That is

$$\Delta T \times (TC1) = -\Delta T \times (TC2)$$

where

ΔT = change in temperature expressed in degrees Centigrade

$TC1$ = V_{BE} temperature coefficient expressed in mv/C°

$TC2$ = V_Z temperature coefficient expressed in mv/C°

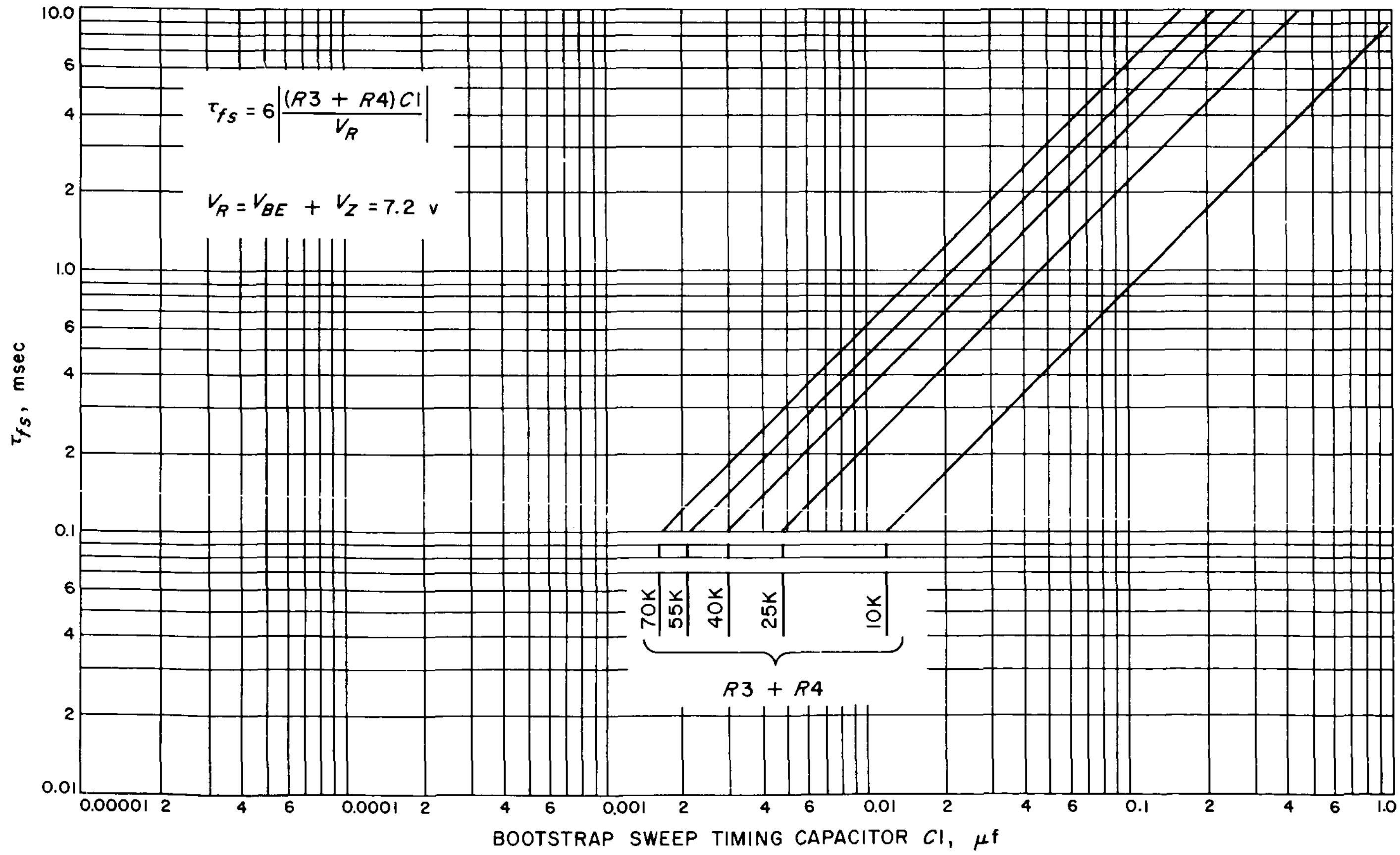


Fig. 7. Bootstrap sweep output vs timing components R3, R4, and C1

The temperature coefficient of V_{BE} is not the familiar -2 mv/C° normally associated with silicon transistors. It is somewhat more complex because of the low current region in which $Q1$ operates and the change in that current region as the amplifier loop gain varies with temperature. To determine the temperature coefficient of V_{BE}, an actual circuit was measured in the laboratory. Figure 8 shows the results of the measurement for a zener current of 2.2 ma. This curve is sensitive to zener current levels because the different zener bias currents flowing from the amplifier give rise to different transistor operating points.

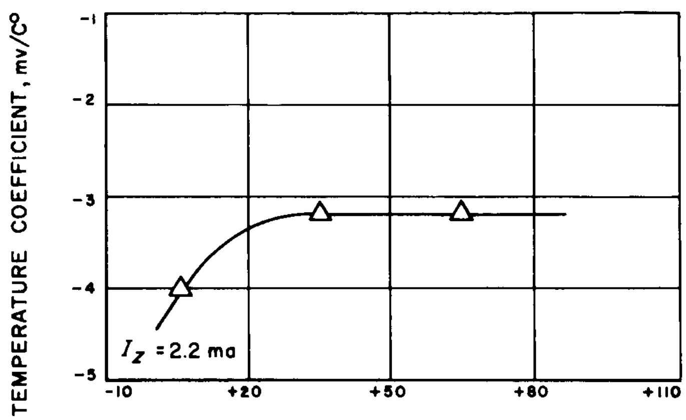


Fig. 8. Typical temperature coefficient of Q1, V_{BE}

To compensate for the temperature variation of V_{BE}, V_Z is required to have a temperature coefficient that is equal and opposite to V_{BE}, i.e., approximately +3 mv/C°.

It is well known that the temperature coefficients of zener diodes are a function of the zener voltage and, further, that zener potentials greater than 5 v possess positive temperature coefficients (Ref. 3). The zener diode having an approximate temperature coefficient of +3 mv/C° at a base current of 2.2 ma is a 1N754A, 6.8 v device. Laboratory measurements show that the 1N754A has a typical temperature coefficient between +2.9 and +3.3 mv/C° in the low milliampere region. The 1N754A diode was, therefore, selected as the reference element in the bootstrap sweep circuit. The operating current of 2.2 ma was selected because it was the lowest bias current that would still allow a reasonable compensation of the $Q1$ V_{BE}. Figure 9 shows a family of curves of the temperature variation of $V_{BE} + V_Z$ for several bias currents. The measurements were made on an actual circuit using a 1N754A diode.

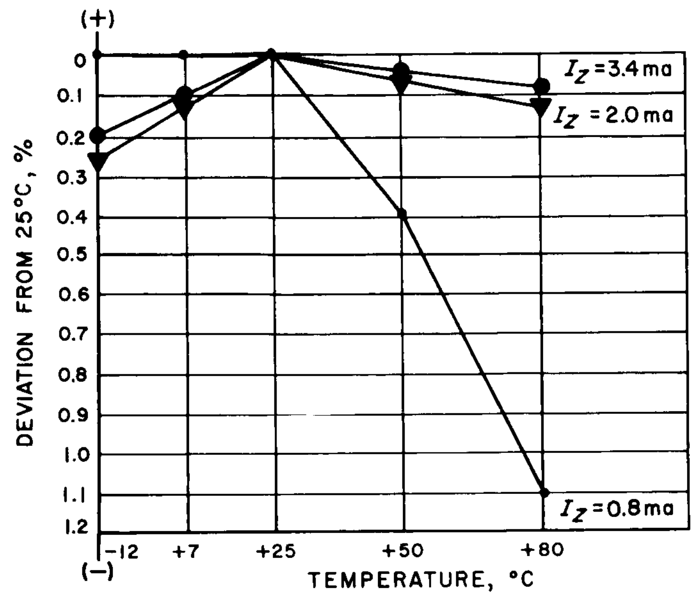


Fig. 9. Bootstrap sweep reference voltage ($V_{BE} + V_Z$) temperature variation

An overall temperature stability of ±0.2% can be achieved throughout the temperature range -10 to +80°C by a proper selection of the bootstrap sweep circuit elements. A procedure for selecting these components is outlined in Appendix A.

4. Comparator circuits. The purpose of the comparator circuits is to compare the bootstrap sweep voltage with the analog input signals and to provide an output indication at crossover. Figure 10 shows the comparator circuits. The circuit forms two identical diode comparators with emitter follower coupling between the analog source and the diodes. Diode $CR8$A and -B, and transistors $Q8$, $Q10$A, and $Q11$ form the analog comparator; diodes $CR8$C and -D, and transistors $Q9$, $Q10$B, and $Q12$ form the ground comparator.

At the beginning of the conversion cycle, the sweep voltage is high; therefore, the constant 100μa current supplied by $Q8$ and $Q9$ will be switched through diodes $CR8$A and $CR8$C, respectively. This action will maintain transistors $Q10$A and $Q10$B in an off condition until the sweep voltage decreases to the point where the constant current is switched to $CR8$B or $CR8$D. The switching will occur when either the analog voltage at the base of $Q10$A, or the zero voltage at the base of $Q10$B, is equal to the sweep voltage.

The point of actual comparison occurs when only half of the 100μa available has been switched. This point is

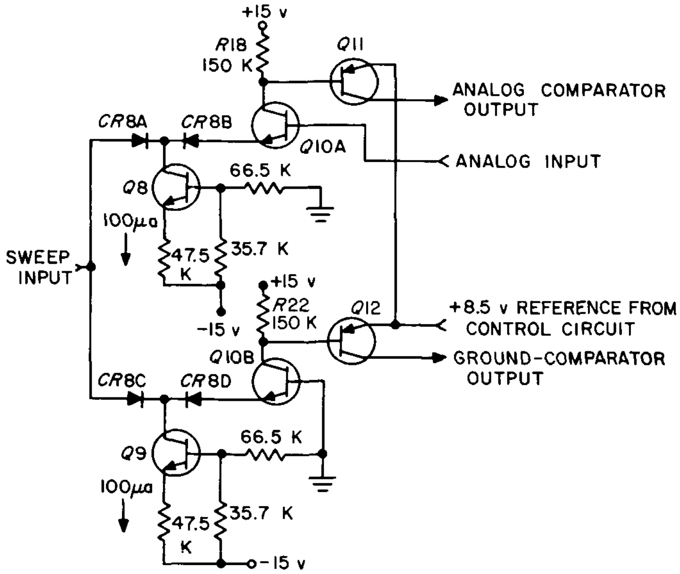


Fig. 10. Bipolar A/PW converter comparator circuits

determined by the 150-K resistor in the collectors of $Q10A$ and $Q10B$ and the reference potential at the emitters of $Q11$ and $Q12$. Both $Q11$ and $Q12$ will turn on to produce the output when their base potentials are driven sufficiently negative to forward-bias their emitter-base junctions. It requires approximately 50μa of current through $R18$ or $R22$ to accomplish the turn-on.

The difference in component characteristics between the two comparators, and the drift in their parameters with temperature, produce offset errors in the converter output: i.e., a zero analog input voltage may not produce a zero time difference in the comparator outputs. The offset is minimized, however, by designing the two comparators identically. This design feature provides an advantage in that drift tendencies in the analog comparator tend to track those in the ground comparator. Further offset errors are minimized by selecting matched components for the critical functions in the circuit. For instance, $CR8A$, -B, -C, and -D are a matched diode quad, and $Q10A$ and -B are a matched transistor pair in a single TO-5 can. Tables 2 and 3 list the pertinent matched characteristics of the devices.

5. Output stage. The output stage shown in Fig. 11 serves to buffer the output of the comparator circuit and to provide a low-impedance driver for the system interface lines. Identical circuits are provided for both analog and ground channels. The discussion presented here will refer to the analog channel but will be applicable to the ground section as well. The circuit consists of a silicon-

Table 2. Matched characteristics of the 2N2642 dual transistor

Parameter	Test condition	Min	Max
h_{FE1}/h_{FE2}	$V_{CE} = 5$ v, $I_C = 10$ ma	0.9	1.0
$\lvert V_{BE1} - V_{BE2} \rvert$	$V_{CE} = 5$ v, $I_C = 10$ ma		5 mv
$\dfrac{\Delta \lvert V_{BE1} - V_{BE2} \rvert}{\Delta T_A}$	$V_{CE} = 5$ v, $I_C = 10$ ma; $\Delta T_A = \begin{matrix} +25 \text{ to } -55°C \\ +25 \text{ to } +125°C \end{matrix}$		10μv/C°

Table 3. Matched characteristics of the FA4310U diode quad

Parameter	Test condition	Min	Max
ΔV_F (forward voltage drop difference)	$I_F = 10\mu a - 1$ ma; $T_A = -55$ to $+100°C$		3 mv

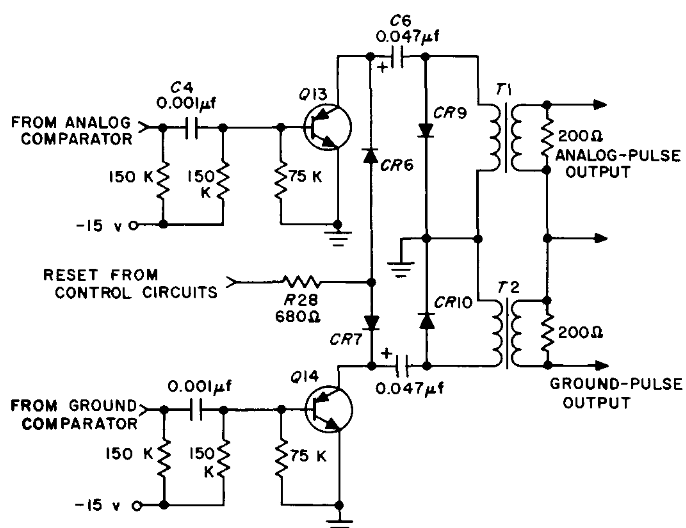


Fig. 11. Bipolar A/PW converter output stage

controlled switch[1] ($Q13$) and an LC pulse-forming network consisting of $C6$ and $T1$. Normally, $Q13$ is turned off and $C6$ is charged positively through $CR6$ and $R28$ when the control circuit reset output is high. When a conversion is to be made, the reset line returns to ground, back-biasing $CR6$ and leaving $C6$ with a positive charge. When crossover occurs in the analog comparator, a positive pulse is coupled through $C4$ to the base of $Q13$,

[1]A bistable PNPN device similar in operation to a silicon-controlled rectifier, with the additional advantage that it can be turned off from the base circuit with a relatively small current pulse (Ref. 4).

switching it to the *on* condition. In the *on* state, $Q13$ discharges $C6$ through its own low internal impedance and the primary of transformer $T1$. The result is a 10μsec voltage pulse appearing on the analog output line. The pulse has the characteristics shown in Fig. 12.

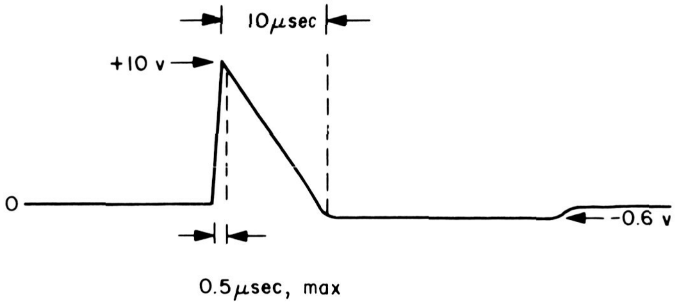


Fig. 12. Characteristics of bipolar A/PW converter output pulse

The only current source for $Q13$ is the capacitor $C6$. When the discharge is nearly complete and the current level reduced to a few hundred microamperes, the silicon switch ($Q13$) will automatically turn off.

At the end of the conversion cycle, the reset line returns to +15 v and allows $C6$ to again establish a positive charge. The circuit then remains in this condition until a new conversion cycle is initiated.

IV. Summary

The design and system implementation of a bipolar A/PW converter for use in performing the A/D conversion in a spacecraft science subsystem has been described.

The A/PW converter will find application in many systems in which high resolution and moderate accuracy are required to perform low-level measurements at relatively slow sampling rates. Resolutions in the order of 9 bits are easily achieved while accuracies of 8 and 9 bits are possible through careful component selection. Sampling rates up to 500/sec are within the design capabilities.

The A/PW converter has been packaged in a welded cordwood module by the Advanced Packaging Group of the Electro-Mechanical Engineering Support Section of Jet Propulsion Laboratory (JPL). Five modules have been fabricated. All have performed well within the electrical specifications, and will be subjected to further electrical and mechanical environmental stresses as part of the plan to thoroughly qualify them for flight use. Figure 13 shows a photograph of the prototype of the bipolar A/PW converter module. Electrical and mechanical design drawings of this module are provided in Appendix B.

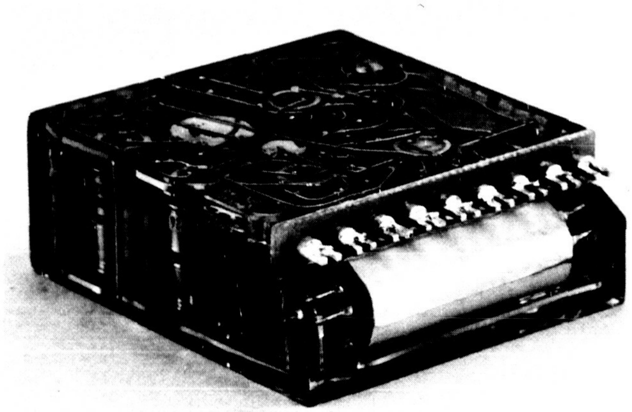


Fig. 13. Bipolar A/PW converter module

Appendix A

Procedure for the Selection of System Parameters and Bootstrap Sweep Components

1. Selection of system parameters. To properly select the system oscillator frequency, a knowledge of the *bit* accuracy requirement and the maximum sampling rate is needed. Figure A-1 has been constructed to show the relationship between clock frequency, bit accuracy, A/PW converter full-scale output, and maximum sampling rate.

To illustrate the use of Fig. A-1, suppose that the application required a 100/sec sample rate. From the graph, one can see that a maximum full-scale output of 3.3 msec would be allowed. If the full-scale output chosen were 3.3 msec, and the bit accuracy requirement were 7, then a clock frequency of approximately 37 KC would be necessary. (The frequency must be doubled if the method of *encoding to one extra bit* is used. This method overcomes the quantizing error problem associated with the asynchronous operation of the A/PW converter.)

The maximum sampling rate shown in Fig. A-1 is based on a total sweep-time plus recovery-time of three times the full-scale output.

2. Selection of zener diode CR1. To obtain proper temperature compensation in the bootstrap circuit, *CR*1 must be measured and selected for the particular circuit in which it will be used.

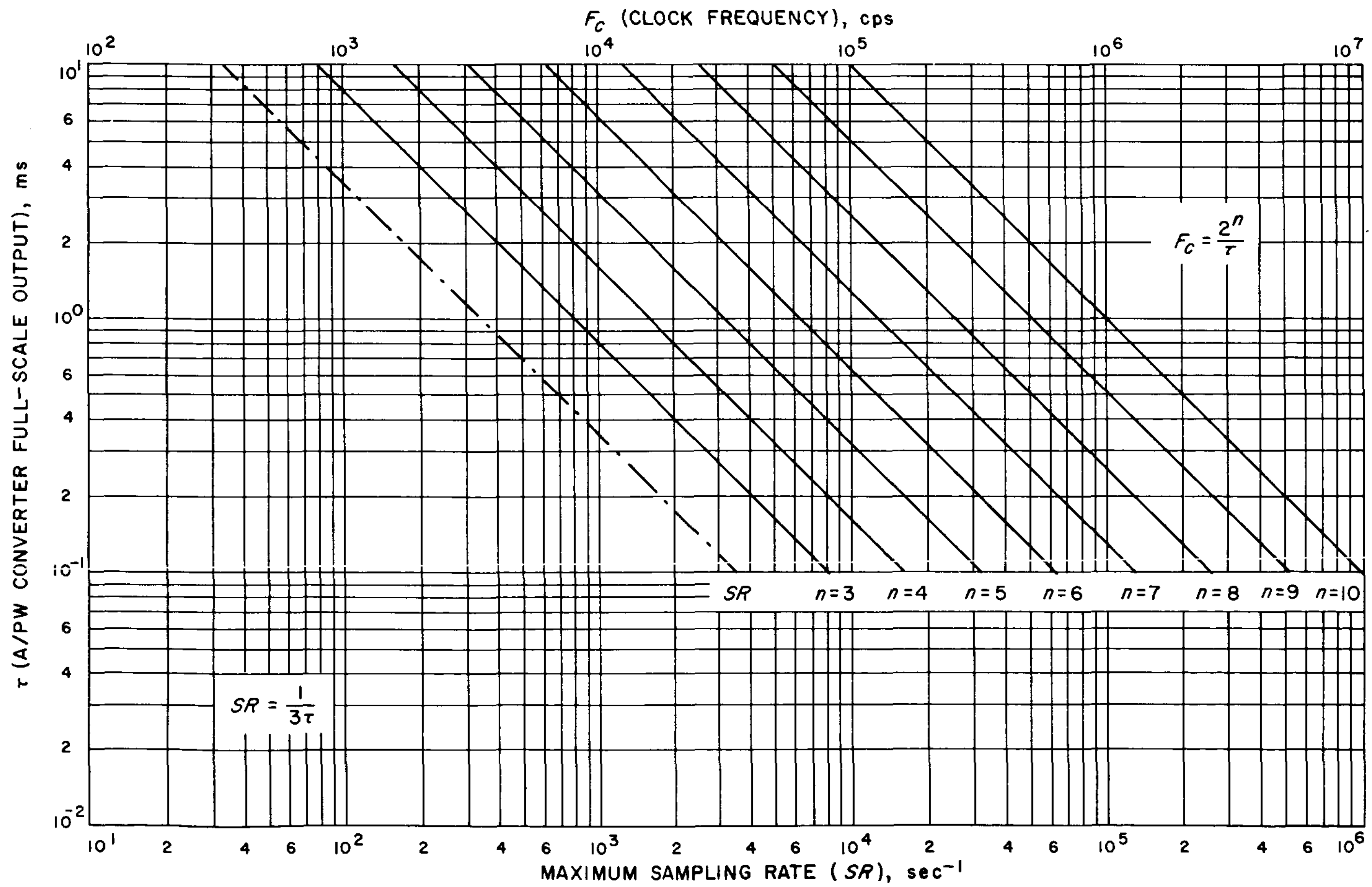


Fig. A-1. Bipolar A/PW converter system parameter relationships

The PSI 1N754A zener diodes will exhibit the necessary temperature coefficient, for compensation in the bipolar A/PW converter bootstrap sweep circuit, when the diode exhibits a given impedance as measured about the operating current. The procedure for screening and selecting the zener diodes is outlined below.

Diode Screening. The circuit operating current for the diode is nominally between 2.0 ma and 2.6 ma. The screening procedure simply consists of measuring the zener voltages at the two current levels and noting the ratio of voltage change to current change. The value of $\Delta V_Z/\Delta I_Z$, which indicates the approximate *TC* necessary for compensation, is 8–14. Those diodes falling within this range can be segregated for further testing in the bootstrap circuit. Those diodes falling outside the range can be used in other parts of the converter.

Bootstrap circuit compensation. The diodes segregated in the preceding screening process are those diodes which will most probably compensate the bootstrap circuit. For the final selection, these diodes must be placed in an actual circuit and the temperature effects measured. The circuit for this measurement is indicated in Fig. A-2.

The components used in this measurement should be components acceptable for module fabrication, since they will be serialized and retained, as a group, in the event that the results of the tests are acceptable. For a group of components to be acceptable, the measured reference voltage should not exceed ±0.3% of nominal[2] between −10 and +80°C. A preferred tolerance is a maximum of ±0.2%.

3. Selection of timing components R3 and C1. The graph of Fig. 7, in the A/PW converter description section, shows the values of *R*3, *R*4, and *C*1 necessary for a given full-scale output. The preferred value of *C*1 to be chosen is one which provides for an *R*3 + *R*4 value between 20 and 50 K. Once *C*1 is selected, the precise value of *R*3 for producing the desired full-scale output must be calculated.

Calculation of R3. Calculation of *R*3 requires that all the other system parameters be known. The expression for *R*3 (as derived from Eq. 4 in the A/PW converter description section of this Report) is

$$R3 = \frac{(\tau_{fs})\ |V_{REF}|}{(C1)\ |e_{fs}|} - R4$$

[2]The nominal reference voltage is the value measured at 25°C.

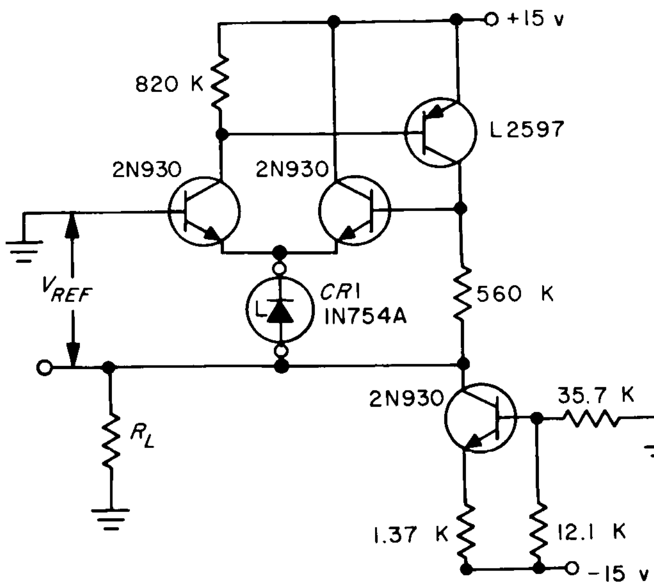


Fig. A-2. Bootstrap sweep test circuit

where

τ_{fs} = full-scale converter output

$V_{REF} = V_{BE} + V_Z$ (determined by measurement)

e_{fs} = full-scale analog input

$C1$ = timing capacitor

$R4$ = Value of the resistance from a center setting of the linearly variable resistor in series with *R*3

The value of τ_{fs} should be derived from the following relationship

$$\tau_{fs} = 2^n \left[\frac{1}{F_c}\right]$$

where

n = number of bits to be encoded

F_c = system clock frequency

The calculated value of *R*3 will not be a standard resistor value and will require a 0.1% tolerance. It is recommended, therefore, that a nominal value for *R*3 be calculated, based on nominal values of V_{REF} and *C*1, and that groups of resistors spaced at 1%-intervals to *R*3 nominal be purchased before fabrication. A ±4%-range should be sufficient to cover the variations in V_{REF} and *C*1. The nearest resistor value to the calculated *R*3 should be used, and the final adjustment for full-scale made with the variable resistor *R*4 after fabrication.

Appendix B

Electrical and Mechanical Design Drawings of the Bipolar A/PW Converter Module

Table B-1. Bipolar A/PW converter parts list

Reference designation	Component description: Name	Value	Rating	Material	±%	Manufacturer or vendor's name	Component number
CR 1	Diode, zener		400 mw	Silicon	5	Pacific Semiconductors, Inc.	1N754A (Selected)
CR 2	Diode					Fairchild Semiconductor	FD643
CR 3	Diode					Fairchild Semiconductor	FD643
CR 4	Diode					Fairchild Semiconductor	FD643
CR 5	Diode, zener		400 mw			Pacific Semiconductors, Inc.	1N754A
CR 6	Diode					Fairchild Semiconductor	FD643
CR 7							FD643
CR 8A[a]							FA4310U
CR 8B[a]							
CR 8C[a]							
CR 8D[a]							FA4310U
CR 9							FD643
CR 10							FD643
CR 11							FD643
CR 12	Diode			Silicon	5	Fairchild Semiconductor	FD306
C 1	Capacitor	Selected	50 v	Teflon	1	Component Research Co., Inc.	05TJXXXF
C 2		470$\mu\mu$f	80 v	Cerafil	10	Aerovox Corp.	HMC80V471AK
C 3		220$\mu\mu$f	80 v	Cerafil		Aerovox Corp.	HMC80V221AK
C 4		0.001μf	80 v	Cerafil		Aerovox Corp.	HMC80V102AK
C 5		0.001μf	80 v	Cerafil		Aerovox Corp.	HMC80V102AK
C 6		0.047μf	50 v	Tantalum		Sprague Electric Company	350D473X90500A
C 7		0.047μf	50 v	Tantalum		Sprague Electric Company	350D473X90500A
C 8		0.001μf	80 v	Cerafil		Aerovox Corp.	HMC80V102AK
C 9	Capacitor	56$\mu\mu$f	80 v	Cerafil	10	Aerovox Corp.	HMC80V560AK
Q 1	Transistor					Texas Instruments, Inc.	2N930
Q 2						Texas Instruments, Inc.	2N930
Q 3						Sperry Products	L2597
Q 4						Texas Instruments, Inc.	2N930
Q 5						Sperry Products	L2597
Q 6						Fairchild Semiconductor	2N708
Q 7						Fairchild Semiconductor	2N708
Q 8						Texas Instruments, Inc.	2N930
Q 9	Transistor					Texas Instruments, Inc.	2N930
Q10	Dual transistor					Texas Instruments, Inc.	2N2642
Q11	Transistor					Sperry Products	L2597
Q12	Transistor					Sperry Products	L2597
Q13	Trigistor					Solid State Products, Inc.	2N897
Q14	Trigistor					Solid State Products, Inc.	2N897

[a]Matched quadruple—unencapsulated.

Table B-1 (contd)

Reference designation	Component description					Manufacturer or vendor's name	Component number
	Name	Value	Rating	Material	±%		
R 1	Resistor	820K	1/4 w	Carbon	5	Allen-Bradley Company	CB
R 2	Resistor	560K	1/4 w	Carbon	5	Allen-Bradley Company	CB
R 3	Resistor	Selected	1/8 w	Film	1	International Resistance Corp.	CCM-T9
R 4	Variable resistor	500Ω	1 w		5	Bourns, Inc.	3280W
R 5	Resistor	1.37K	1/8 w	Film	1	International Resistance Corp.	CCM-T0
R 6		35.7K					
R 7		12.1K					
R 8		18.2K					
R 9		20K					
R 10		20K					
R 11		47.5K					
R 12		47.5K					
R 13		90.9K					
R 14		90.9K					
R 15		20K	1/8 w	Film	1	International Resistance Corp.	CCM-T0
R 16		820K	1/4 w	Carbon	5	Allen-Bradley Company	CB
R 17		560K	1/4 w	Carbon	5	Allen-Bradley Company	CB
R 18		150K	1/8 w	Film	1	International Resistance Corp.	CCM-T0
R 19		47.5K					
R 20		66.5K					
R 21		35.7K					
R 22		150K					
R 23		47.5K					
R 24		66.5K					
R 25		35.7K					
R 26		150K					
R 27		150K	1/8 w	Film	1	International Resistance Corp.	CCM-T0
R 28		680Ω	1/4 w	Carbon	5	Allen-Bradley Company	CB
R 29		150K	1/8 w	Film	1	International Resistance Corp.	CCM-T0
R 30		150K	1/8 w	Film	1	International Resistance Corp.	CCM-T0
R 31		200Ω	1/4 w	Carbon	5	Allen-Bradley Company	CB
R 32		200Ω	1/4 w	Carbon	5	Allen-Bradley Company	CB
R 33		75K	1/8 w	Film	1	International Resistance Corp.	CCM-T0
R 34		75K	1/8 w	Film	1	International Resistance Corp.	CCM-T0
R 35	Resistor	21.1K	1/8 w	Film	1	International Resistance Corp.	CCM-T0
T 1	Transformer					Pulse Engineering, Inc.	6161, case style HA
T 2	Transformer						

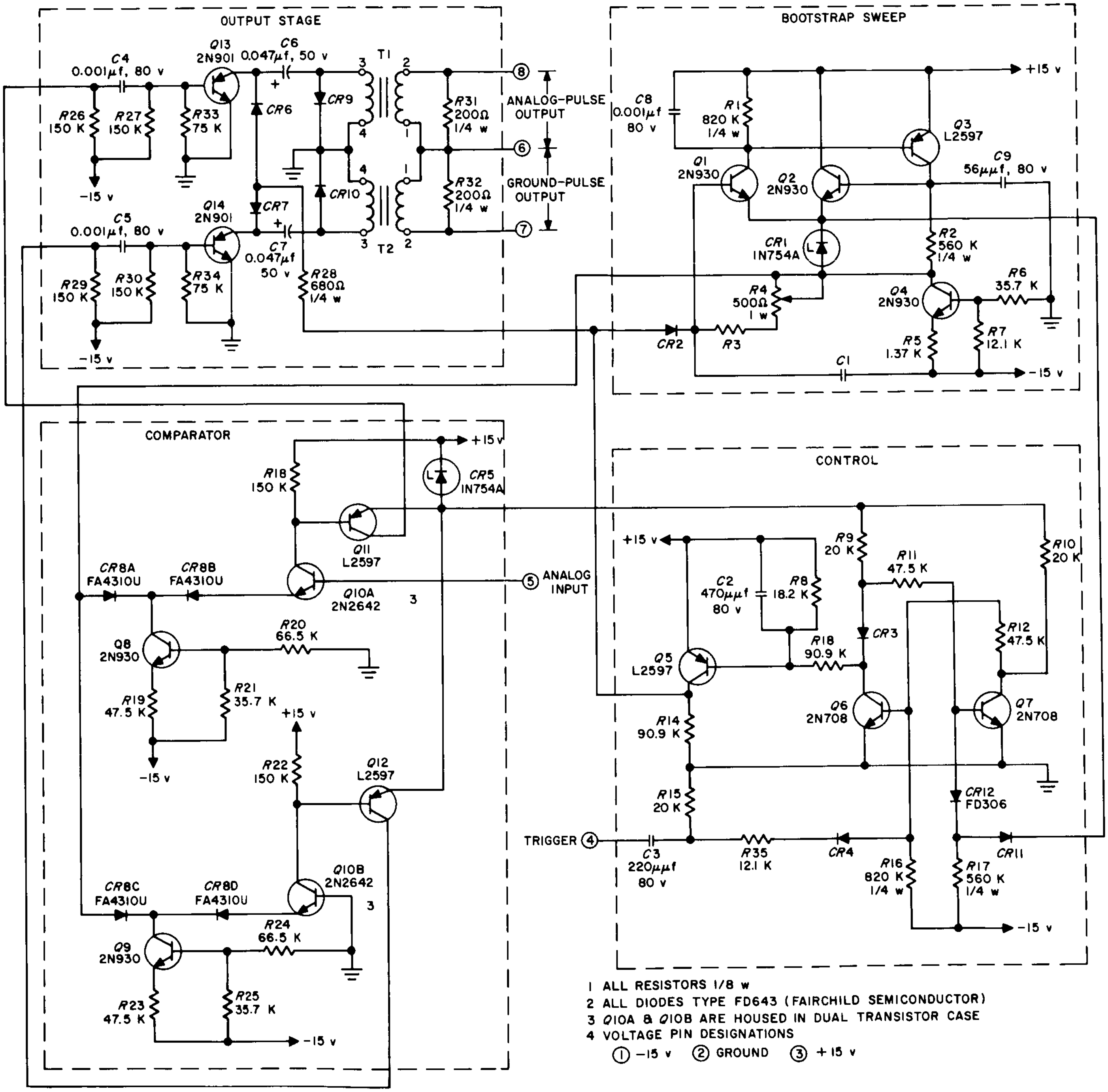
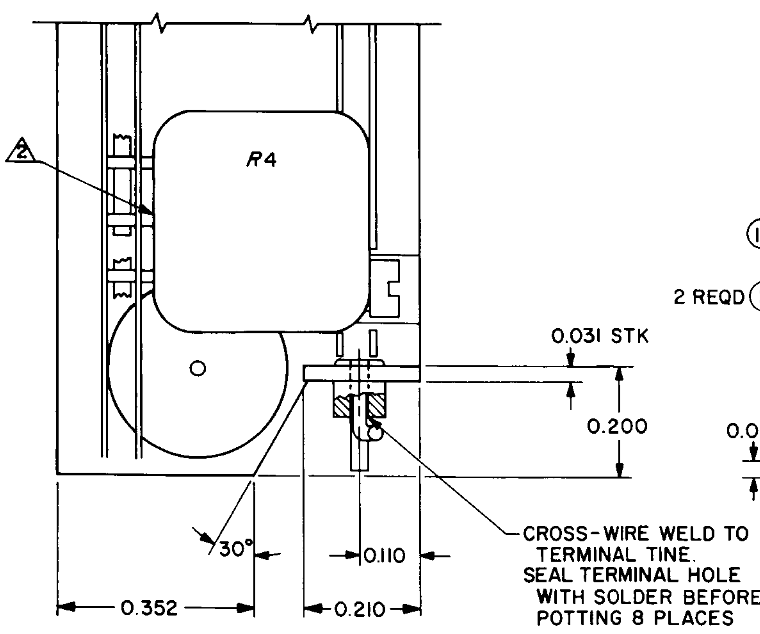
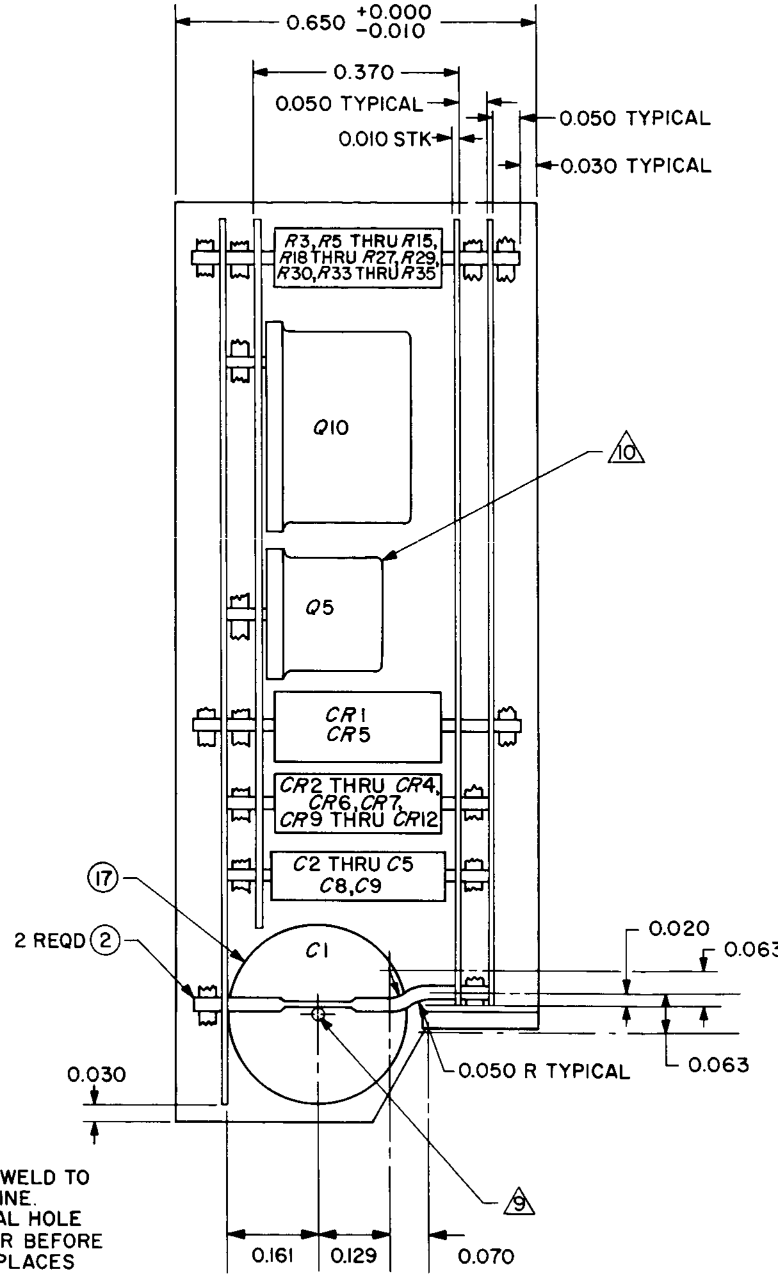


Fig. B-1. Electrical design of the bipolar A/PW converter

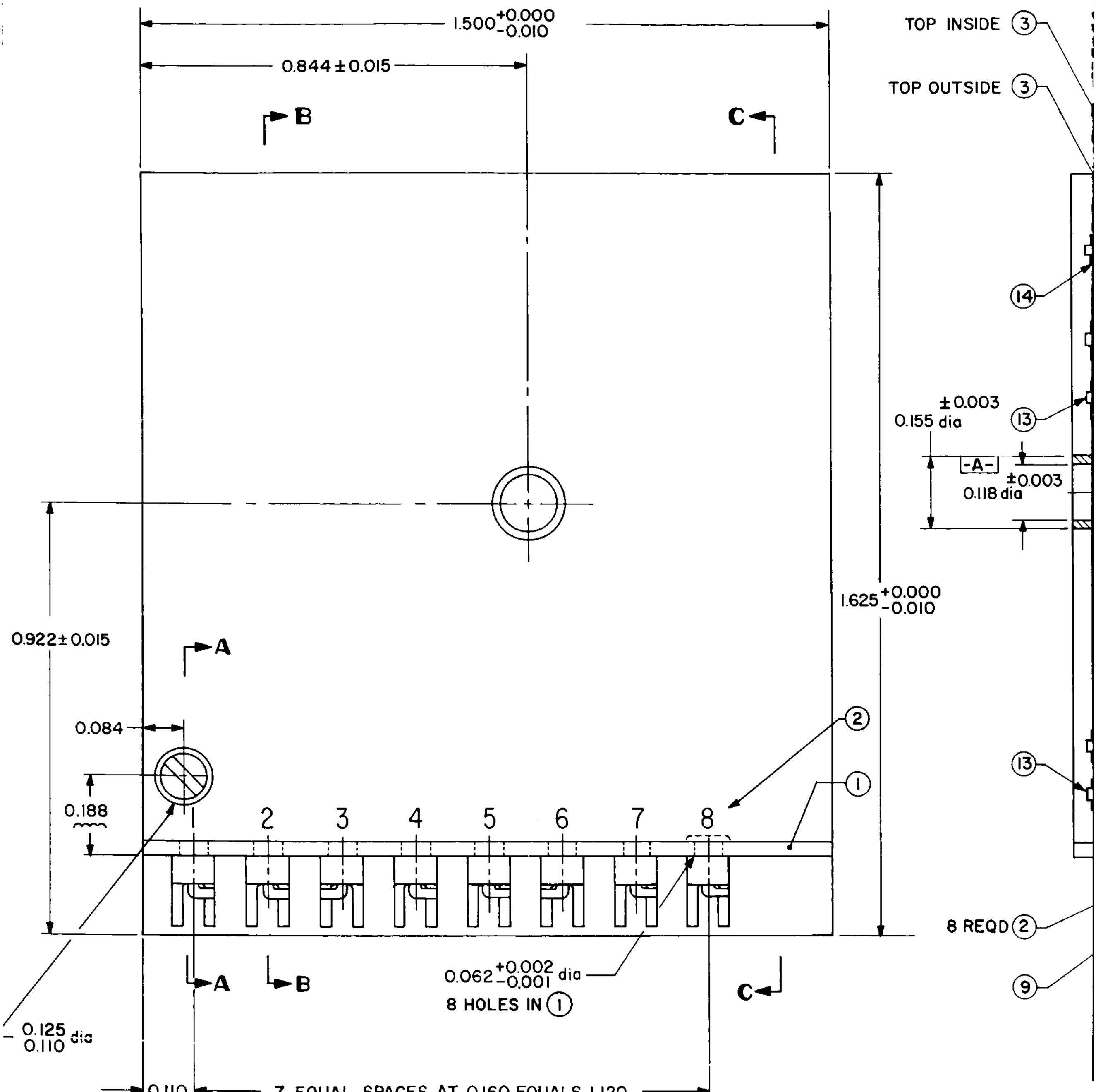


PARTIAL SECTION **A-A**



SECTION **B-B**

15



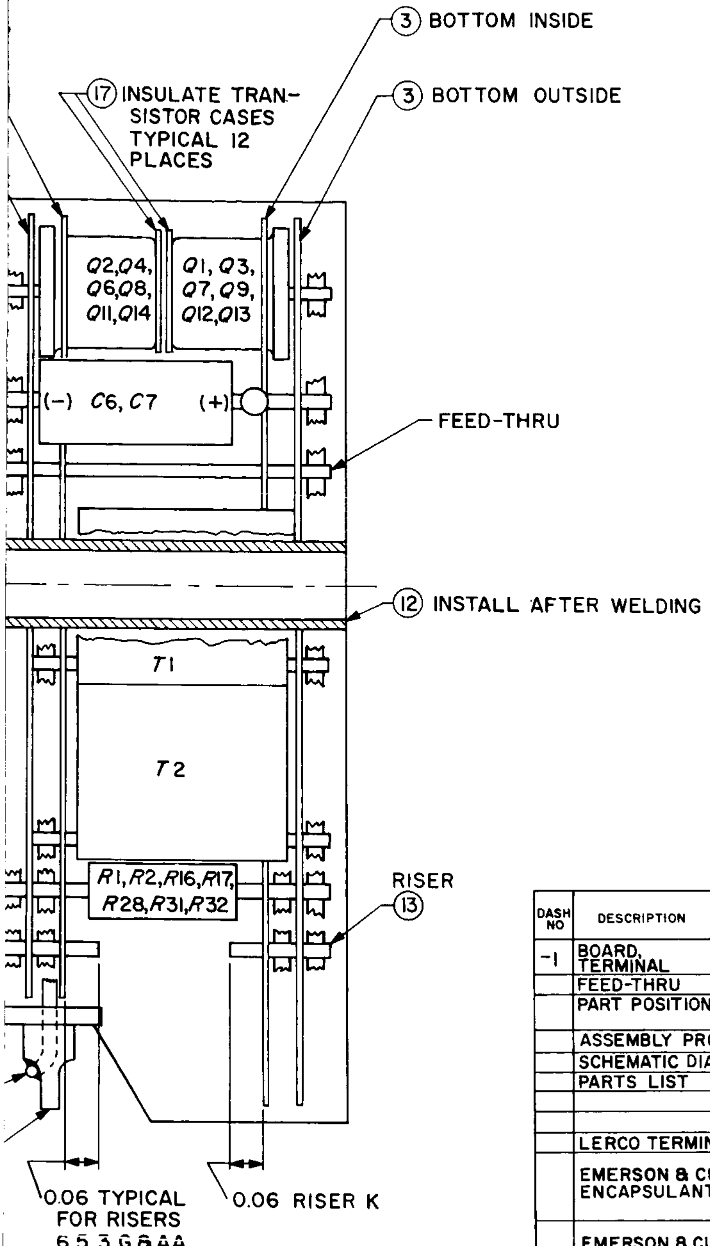
1 0.090 dia HOL
POSITIONER T
ED THAT NO
SUCH HOLES

ALL DIMENSIONS ARE IN INCHES

2 SEAL LEADS
INTO MODULI

3 GOLD PLATE

4 ENCAPSULAT
TO 100 PARTS
150 ± 5°F TH



SECTION C-C

.ES OR LARGER, MAY BE PLACED IN ANY PART
'O FACILITATE FLOW OF ENCAPSULANT PROVID-
DIRECT SHORT CIRCUIT PATH IS CREATED BY

OF TRIMPOT (R4) WITH (11) BEFORE ASSEMBLY
E

(13) PER MIL-G-45204, TYPE I, CLASS I

E WITH (10) USING 12 PARTS CATALYST NO. 11,
; NO. 1090 RESIN. CURE 10 TO 12 HOURS AT
EN 1 1/2 TO 2 HOURS AT 180 ± 5°F

DASH NO	DESCRIPTION	SPECIFICATION	STOCK SIZE / REF DESIGNATION ELEC DWG	MATERIAL	NO REQD	ZONE	FIND NO
-1	BOARD, TERMINAL	MIL-P-18177 TYPE GEE	1/32 STK X 2 1/4 X 1 5/8	FIBER GLASS, EPOXY	1		1
	FEED-THRU				10		2
	PART POSITIONER		0.007 STK X 3 1/8 X 1 5/8	CLEAR MYLAR	1		3
	ASSEMBLY PROCEDURE				–		4
	SCHEMATIC DIAGRAM				–		5
	PARTS LIST				–		6
							7
							8
	LERCO TERMINAL				8		9
	EMERSON & CUMING ENCAPSULANT			MICRO BALLOON FILLED AMINE CURED EPOXY	A/R		10
	EMERSON & CUMING ENCAPSULANT			MICRO BALLOON FILLED AMINE CURED EPOXY	A/R		11
	TUBING		5/32 dia X 0.016 WL X 3/4 LG	FIBER GLASS, EPOXY	1		12
	WIRE	QQ-S-502 TYPE OF, NO RESIDUAL DEOXIDANTS	0.025 dia X LENGTH REQUIRED	OXYGEN FREE COPPER, GOLD PLATED	A/R		13
	WELDING RIBBON	ASTM F 175 b	0.010 X 0.031 X LENGTH REQUIRED	NICKEL, ELEC GRADE A	A/R		14
	WARNOW PROCESS PAINT CO EPOXY INK				A/R		15
							16
	TAPE, PRESSURE SENSITIVE	MIL-I-15126F TYPE MF-25		MYLAR TAPE	A/R		17
	SOLDER, SOFT	QQ-S-571 Sn 63			A/R		18
	WELDING	GPO-30995-GEN			–		19

Fig. B-2. Mechanical design of the bipolar A/PW converter

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