Report No. 03-66-151

Third Quarterly Report

for

# PHOTON-COUPLED ISOLATION SWITCH

(1 July - 30 September)
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Contract No. 951340

Prepared by

E. L. Bonin

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Texas Instruments Incorporated
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Post Office Box 5012
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Jet Propulsion Laboratory
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## ABSTRACT

A new integrated circuit switch is being developed using photon coupling to provide a transistor output electrically isolated from the driving sources and all other terminals of the switch. The Isolation Switch combines a monolithic silicon integrated driver circuit supplying bias to a gallium arsenide photo-emitting diode. The emitting diode is optically coupled to an electrically-isolated silicon phototransistor.

The program is divided into two phases:

Phase I, design and breading of the driver circuit and development of the gallium arsenide emitting diode-silicon phototransistor pair.

Phase II, integration of the driver circuit and prototype production of the complete isolation switch.

In the first and second quarters of the program under Phase I, the design and breadboarding of the driver circuit were substantially completed. The silicon phototransistor, also designed and fabricated, demonstrated the desired current gain and breakdown voltage characteristics, but also high leakage currents at high temperatures. The latter was found to be due to inversion layer formation on the transistor surface after the GaAs emitting diode was bonded to the transistor with a coupling glass.

During the third quarter under Phase I, modifications were made to the transistor which eliminated the high leakage effects. Additional characterizations were made for the phototransistor current gain, the speed and emitting diode biasing for the driver circuit, and the bonding glass and encapsulation material.

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# SECTION I

## INTRODUCTION

The transformer function of isolation is not available in most integrated circuits, because it cannot be effectively provided with the conventional processing techniques used. Isolation offers the highly desirable abilities of coupling signals between circuits operating at different d-c potentials and minimizing ground-loop currents produced with direct connections. Isolation can be achieved in integrated circuits, however, by incorporating a solid-state light emitter-detector pair. Of the available materials, the most efficient signal coupling between the optical pair is obtained using a GaAs P-N junction photo emitting diode with a Si P-N junction detector. The 0.9 $\mu$m wavelength of light emission of the GaAs diode is near the peak response of the Si detector. The process technology for the GaAs and Si devices is also highly developed. Using this source-detector system, several types of optically-coupled devices have been fabricated. [1,2] These devices include an isolated input transistor, an isolated-gate P-N-P-N- type switch, a multiplex switch requiring no driving transformer, and an isolated-input pulse amplifier.

The present contract is concerned with the development of a three-chip isolation switch combining a monolithic Si driver circuit, a GaAs emitting diode, and a Si phototransistor. The input to the isolation switch is applied to the driver circuit which supplies bias to the GaAs diode. The emitting diode is coupled with a high-refractive index glass to the phototransistor electrically isolated from the driving sources and other terminals of the switch. This development program is divided into two phases. Phase I is concerned with the development of the emitting diode-phototransistor pair and design and breadboarding of the driver circuit. Phase II consists of integrating the driver circuit in a monolithic Si wafer and fabricating the complete isolation switch.

In the first two quarters of the program under Phase I, design criteria for the circuit were obtained from measurements of elements similar to those to be used in the integrated wafer. The design and breadboarding of the driver circuit were then substantially completed. Phototransistors were also designed and fabricated which demonstrated the desired current gain and breakdown characteristics. The phototransistor was designed to operate with the GaAs emitting diode currently used in the Optoelectronic Pulse Amplifier, Texas Instruments type SNX1304. Optical coupling, measured for the emitter-detector pair, met the design objectives. An objectionable characteristic of the coupled pair was discovered: that of excessive transistor leakage currents due to the formation of inversion layers on the transistor surface under some bias conditions. Several

modifications were made to the design of the phototransistor to eliminate the leakage effect.

This report describes work performed during the third quarter under Phase I. Phototransistors of the new design were fabricated which displayed the desired low leakage characteristics with no inversion layer formation. Also analyzed were the current gain characteristics of the phototransistor, the switching speed and emitting diode biasing for the driver circuit breadboard, and the characteristics of the bonding glass and encapsulation material.

## SECTION II

## TECHNICAL DISCUSSION

### A. TRANSISTOR EVALUATION

#### 1. Leakage Characteristics

As described in the second quarterly report[3], inversion layers could be induced on the collector and base surfaces of the Si phototransistor after the GaAs photo emitting diode was bonded to the transistor with a high-refractive-index glass. These inversion layers resulted in excessively large leakage currents. State-of-the-art technology for eliminating the effects of the inversion layers include the following:

1) Incorporating an $N^+$ diffusion (guard-ring) on the collector surrounding the base.

2) Providing a metal ring (field-relief electrode) over the collector oxide surrounding the base and contacting the guard ring.

3) Increasing the impurity concentration on the surface of the base.

The $N^+$ ring breaks the continuity of the collector inversion layer which would extend from the base to the edge of the wafer. The contact ring reduces the electric field on the oxide in the region of the collector-base junction, thereby expanding the inversion-free collector area. The increased base concentration reduces the probability of forming an inversion layer over the base.

Initial testing to determine if these modifications were sufficient to eliminate the effects of the inversion layers on the leakage characteristics were conducted on standard, commercially available Si transistors. The Texas Instruments type 2N2484 Si transistor is fabricated with surface passivation techniques similar to those above. Three of the 2N2484 transistors were fabricated with standard ball-bond connections, and GaAs emitting diodes were then bonded to the transistors using a Se-As-S coupling glass. These transistors are much smaller than the phototransistor. To prevent shorting of the GaAs wafer to the ball-bonded leads on the Si wafer, a glass thickness of about 3 mils was used, compared to 1 to 2 mils used for the phototransistor. Testing conditions were the same as those used for studying the leakage characteristics of the phototransistor: 0 to 100 V applied between the GaAs and Si wafers, a collector-emitter voltage between 3 and 35 V and an ambient temperature of 100° C. Collector-emitter leakage currents

$I_{CEO}$ were the same as before the GaAs diodes were mounted. This indicated that inversion-free leakage characteristics should also be obtained with the modified design of the phototransistor.

The new geometry for the phototransistor, incorporating the above features, was described in Figures 4 and 5 of the second quarterly report[3]. Diffusion masks for the new phototransistor were developed and new transistors processed. Leakage tests, as described above, were made for the new phototransistor. Low-valued leakage currents were obtained, without instabilities demonstrated previously with inversion layers.

Distributions of $I_{CEO}$ at 20 V and 100° C are shown in Table I. These include results for two batches of phototransistors having the original geometry, type A, and four batches having the new geometry, type B. Each tic mark indicates a device having an $I_{CEO}$ within the incremental current range indicated. Prior to these leakage measurements, devices were screened on the slice for a collector-emitter breakdown voltage greater than 40 V and, after separation of the transistor dice, the transistors were sorted for common-emitter forward current gain, $H_{FE}$. There was no prior test for leakage. For the tests, type A devices did not have GaAs diodes mounted, since this results in the inversion layers at higher temperatures.

The effect of supply voltage on $I_{CEO}$ and collector-base leakage, $I_{CB}$, at 100° C is shown in Figure 1 for representative type A and B devices. For the type A devices shown, $H_{FE}$ ranged between 400 and 500, as measured at $V_{CE} = 1$ V, $I_B = 0.1$ mA, and T = 25° C. For the type B devices, $H_{FE}$ ranged between 300 and 400. A study of the results in Figure 1 indicates that $I_{CEO}$ at the specified bias of 20 V is largely independent of $H_{FE}$ as defined above. Rather, $I_{CEO}$ depends on $I_{CB}$ and the particular influence of supply voltage. For state-of-the-art silicon small-signal planar transistors, $I_{CB}$ leakage typically ranges between 1 to 50 nA at 100° C. This closely agrees with the results obtained for the phototransistors, as shown in Figure 1. Life data of state-of-the-art transistors for high temperature storage, high humidity storage, and full power operating tests over several thousand hours indicate that for most all units, any increase in $I_{CB}$ is less than by a factor of 2. In a few cases, the increase is by as much as a factor of 4. This information, together with yield figures which can be obtained from Figure 1, can be used to establish the maximum acceptable limit for the initial measurements of $I_{CEO}$.

2. Current Gain Characteristics

For a GaAs diode current of 22 mA (100° C worst case minimum value), the relation between the phototransistor collector currents at 25° C and 100° C are shown in Figure 2 for 18 GaAs Switches. Included are devices having high and low values of $I_{CEO}$. No clear-cut correlation was observed between the change in $I_C$ with temperature and $I_{CEO}$, indicating that the change in $H_{FE}$ with temperature is approximately the same for both high and low leakage devices.

Table I. Distribution of $I_{CEO}$ for Phototransistor Having Initial Geometry (A) and New Geometry (B).

| Type | $H_{FE}$ $V_{CE}$ = 1 V $I_B$ = 0.1 μA T = 25° C | $I_{CEO}$ (μA), $V_{CE}$ = 20 V, T = 100° C | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | < 2 | < 4 | < 6 | < 8 | < 10 | < 12 | < 14 | < 16 | < 18 | < 20 | < 22 | < 24 | < 26 | < 28 | < 30 | ≥ 30 |
| A | 400-500 | 2 | 2 | 1 | 1 | | 2 | 2 | 3 | 1 | 1 | 1 | | | 1 | | 3 |
| | 500-600 | | | | 1 | 1 | 1 | 1 | 2 | 1 | | 1 | | 1 | | | 1 |
| B | 400-500 (Slice 1) | | | | | | | 1 | | | | | | 1 | | | 3 |
| | 300-400 (Slice 2) | 3 | 2 | 1 | 2 | 1 | | | 2 | | | | | | | | 2 |
| | 300-400 (Slice 3) | | | | 2 | | 2 | | | | | | | 2 | 2 | | 4 |
| | 300-400 (Slice 4) | | | | 3 | 3 | 1 | 1 | | | | 1 | | | | | 1 |

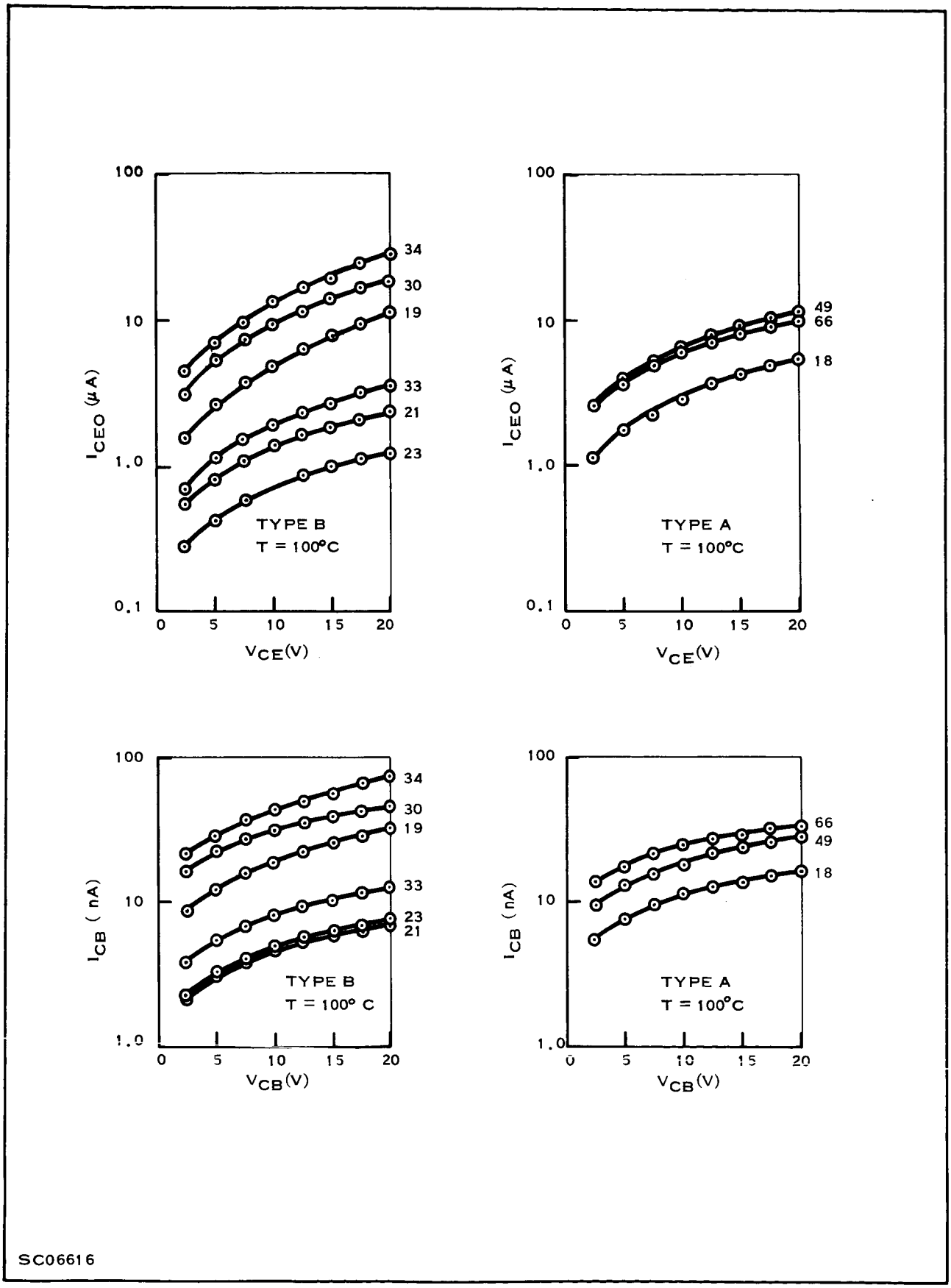


Figure 1. Leakage Characteristics of New (B) and Original (A) Geometry Phototransistors

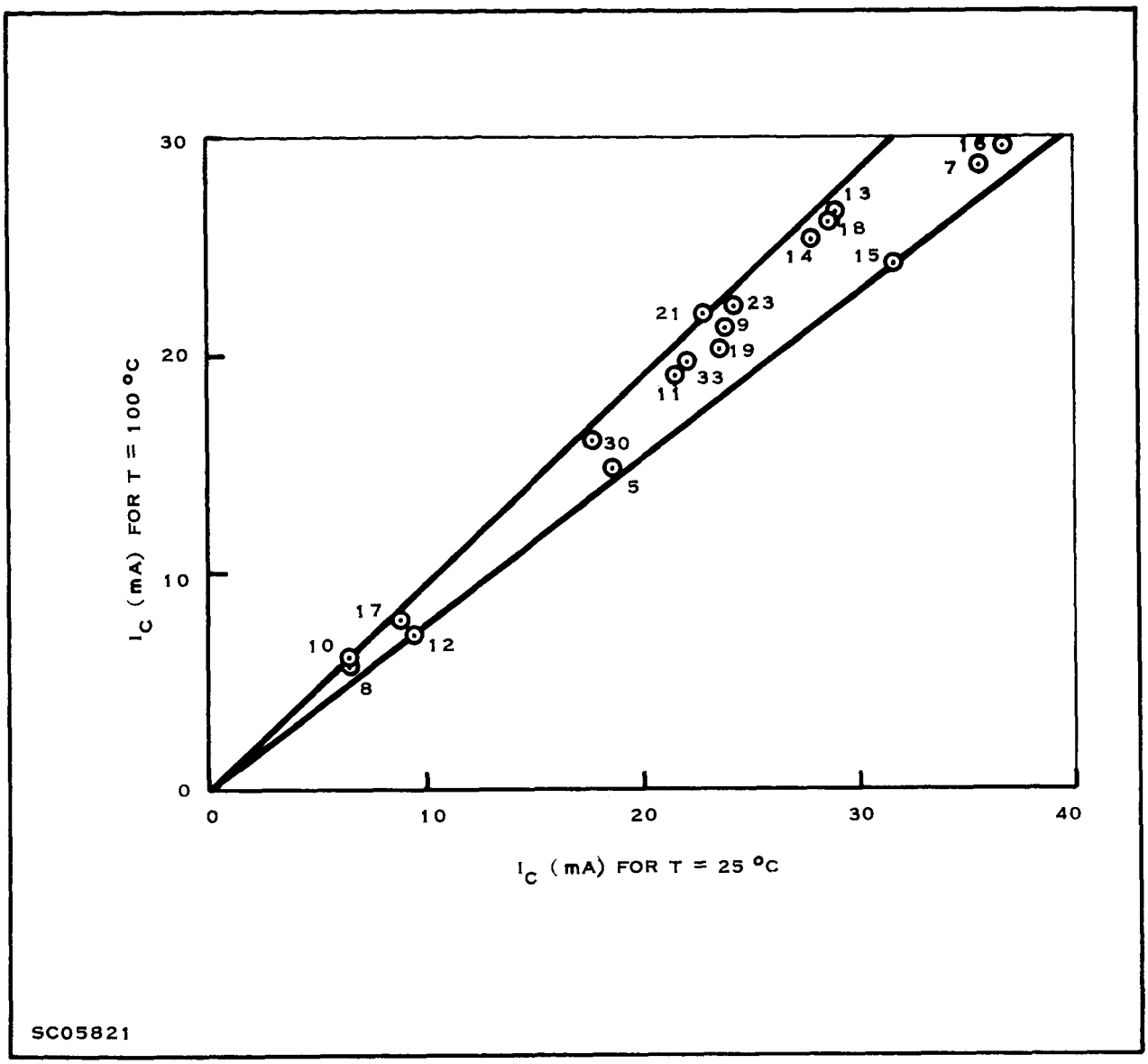


Figure 2. Phototransistor Collector Current, $I_C$, For GaAs Diode Current of 22 mA.
$I_C$ (100° C) vs. $I_C$ (25° C). $V_{CE}$ = 1 V.

The $H_{FE}$ characteristics at 25° C and 100° C is given as function of $I_C$ in Figure 3 for representative low leakage (Unit 23) and high leakage (Unit 19) devices. The fact that Unit 19 has nominally higher $H_{FE}$ is of no particular consequence. Applying the 25° C and 100° C values of $I_C$ for each device given in Figure 2, the ratio of $H_{FE}$ at 100° C to that at 25° C is about 1.50 for both devices. Also from Figure 2, the average ratio of $I_C$ at 100° C to that at 25° C is 0.85. The ratio of these values, $0.85 \div 1.5 = 0.57$, is the ratio of the efficiency of the GaAs diode at 100° C to that at 25° C. This is only slightly larger than the nominal value of 1/2 used previously[3].

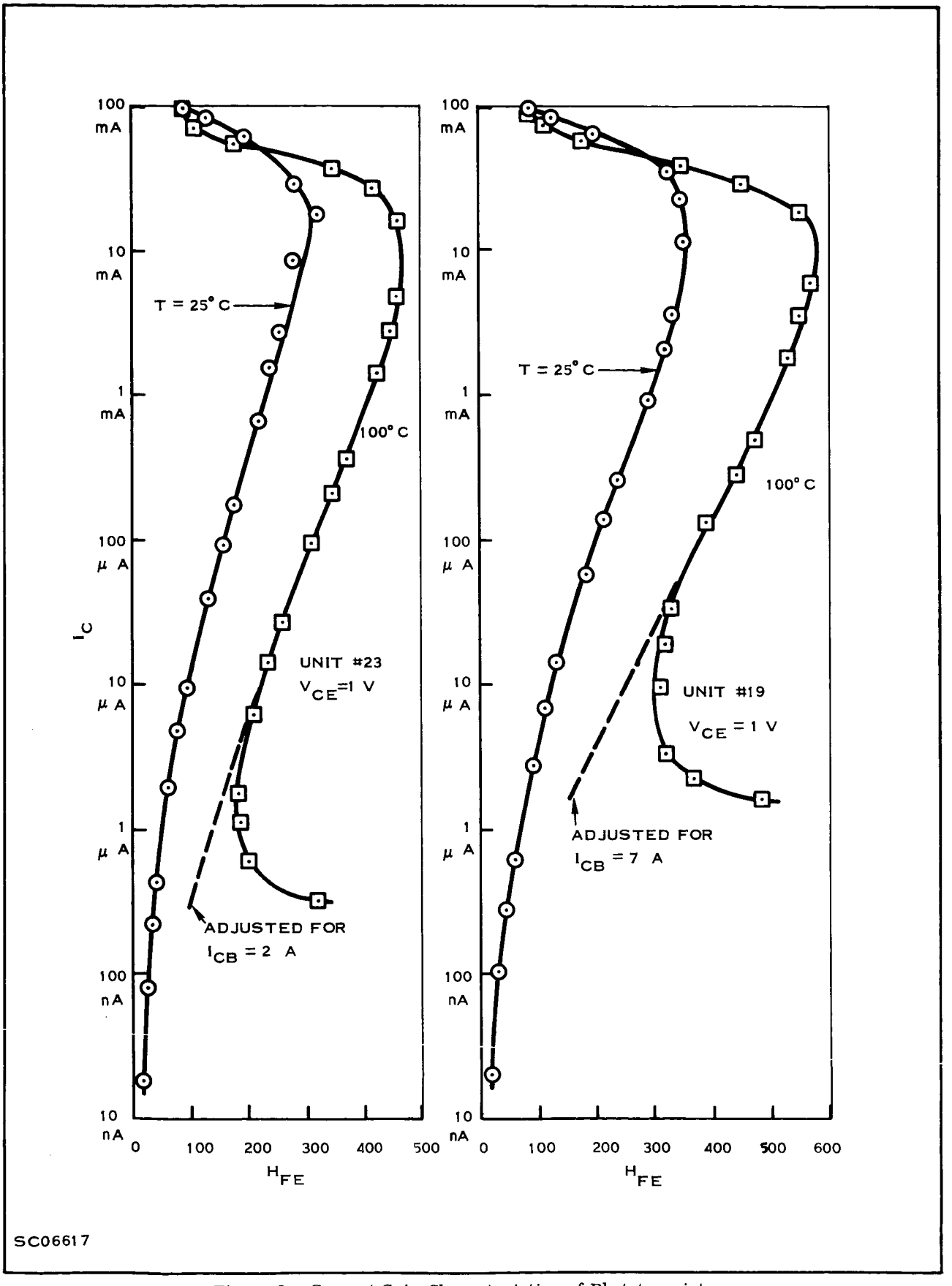


Figure 3. Current Gain Characteristics of Phototransistors.

## B. DRIVER CIRCUIT

### 1. Speed Measurements

The switching speed characteristics of the breadboarded driver circuit were studied. The supply voltage and the peak input voltage used were 4.0 V. For the phototransistor (of the original design), a supply voltage of 20 V and a load of 2 kΩ were used. Delay (0 to 10%), rise (10 to 90%), storage (100 to 90%), and fall (90 to 10%) times were measured as a function of capacitance added to, what will be, the common junction of the input diodes. Typically, the input diode capacitance is about 3 pF, or about 27 pF for 9 diodes having inputs at a constant potential. Measurements were made for capacitances of up to 200 pF.

Figure 4 describes the switching times for the voltage across the final collector resistor which is approximately that for the current in the GaAs diode. Figure 5 describes the switching times at the collector of the phototransistor. The total rise ($t_D + t_R$) and total fall ($t_S + t_F$) times for the phototransistor of 3.6 μs and 39.6 μs, respectively, at C = 27 pF are well within the maximum specifications of 10 μs and 100 μs.

The rise time of the phototransistor is given approximately by

$$t_R = \frac{\overline{C_{CB}}\ (V_{CC})}{I_\lambda} \tag{1}$$

where $\overline{C_{CB}}$ is the effective collector-base capacitance during the turn-on transient, $V_{CC}$ is the supply voltage, and $I_\lambda$ is the effective base current. For the particular peak current in the GaAs diode of 31.7 mA, $I_\lambda$ was measured as 127 μA. The measurement consisted of shorting the collector and emitter leads and determining the short-circuit current between this point and the base lead. The collector-base capacitance at 20 V was measured as 11 pF, but $\overline{C_{CB}}$ is greater due to the fact that the collector voltage varies between 20 V and about 0 V during the switching transient, and capacitance increases with decreasing voltage. Using the measured $t_R = 2.2$ μs, we obtain $\overline{C_{CB}} \doteq 14$ pF.

The fall time of the phototransistor is given approximately by

$$t_F = 2.2\ (H_{FE})\ (R_L)\ (\overline{C_{CB}}\,') \tag{2}$$

where $H_{FE}$ is the current gain, $R_L$ is the load resistance, and $\overline{C_{CB}}\,'$ is the effective C-B capacitance during the turn-off transient. For the measured $t_F = 32.0$ μs and $H_{FE} = 485$, we calculate (for $R_L = 2$ kΩ)

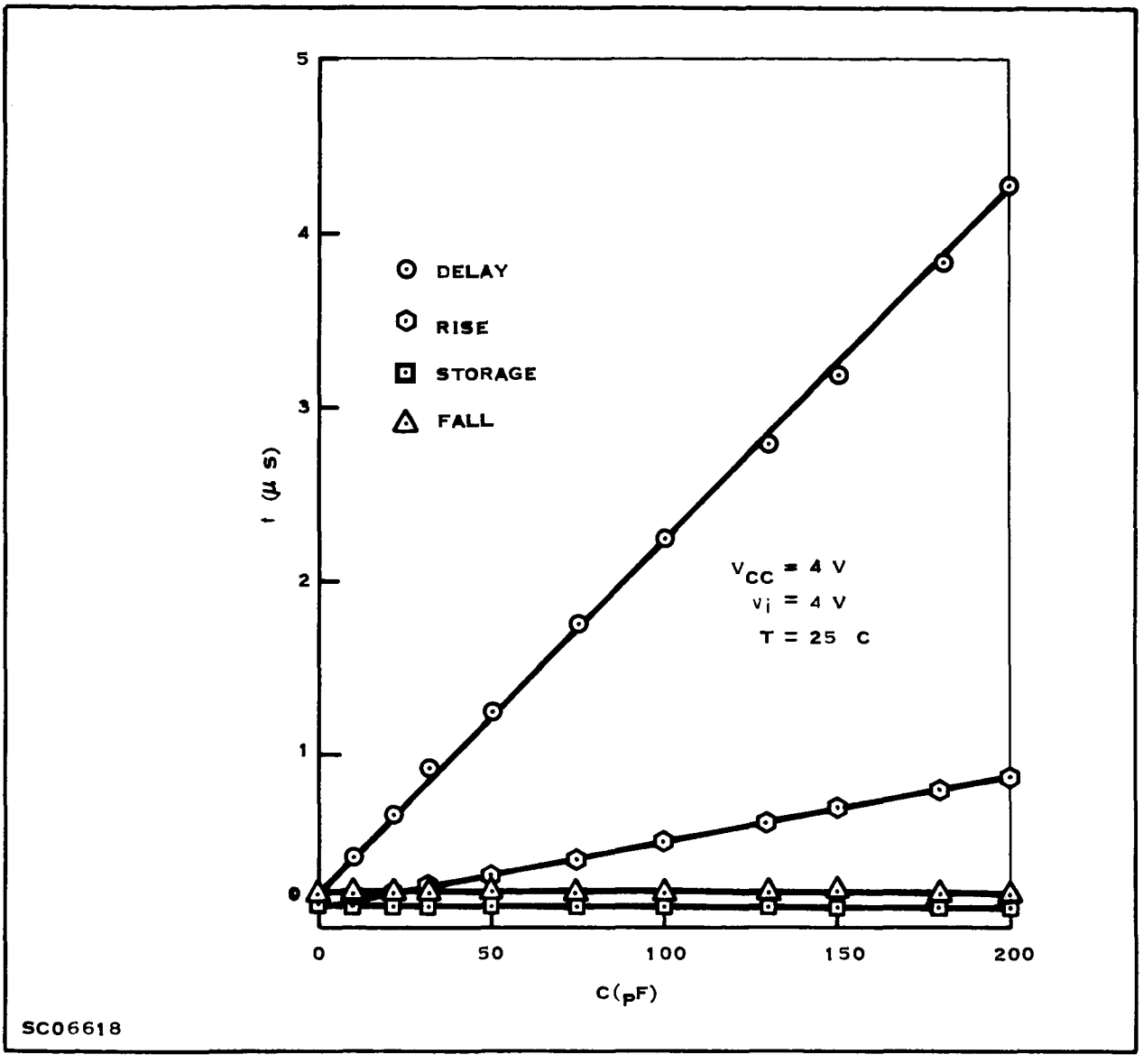


Figure 4. Switching Times at Driver Circuit Final Collector Resistor vs. Loading Capacitance.

we calculate (for $R_L = 2$ kΩ)

$$\overline{C_{CB}}' \doteq 15 \text{ pF}.$$

Analysis[4] of the effective capacitances for the rise and fall transients, with the assumption of a cube-law C-V relationship, indicates $\overline{C_{CB}} = 1.31\ C_{CB}$, where $C_{CB}$ is the value at 20 V. Thus $C_{CB} = 1.31$ (11 pF) = 14.4 pF. Similarly

$$\overline{C_{CB}}' = 1.55\ C_{CB} = 17 \text{ pF}.$$

These are fairly close to the previous values of 14 pF and 15 pF, respectively.

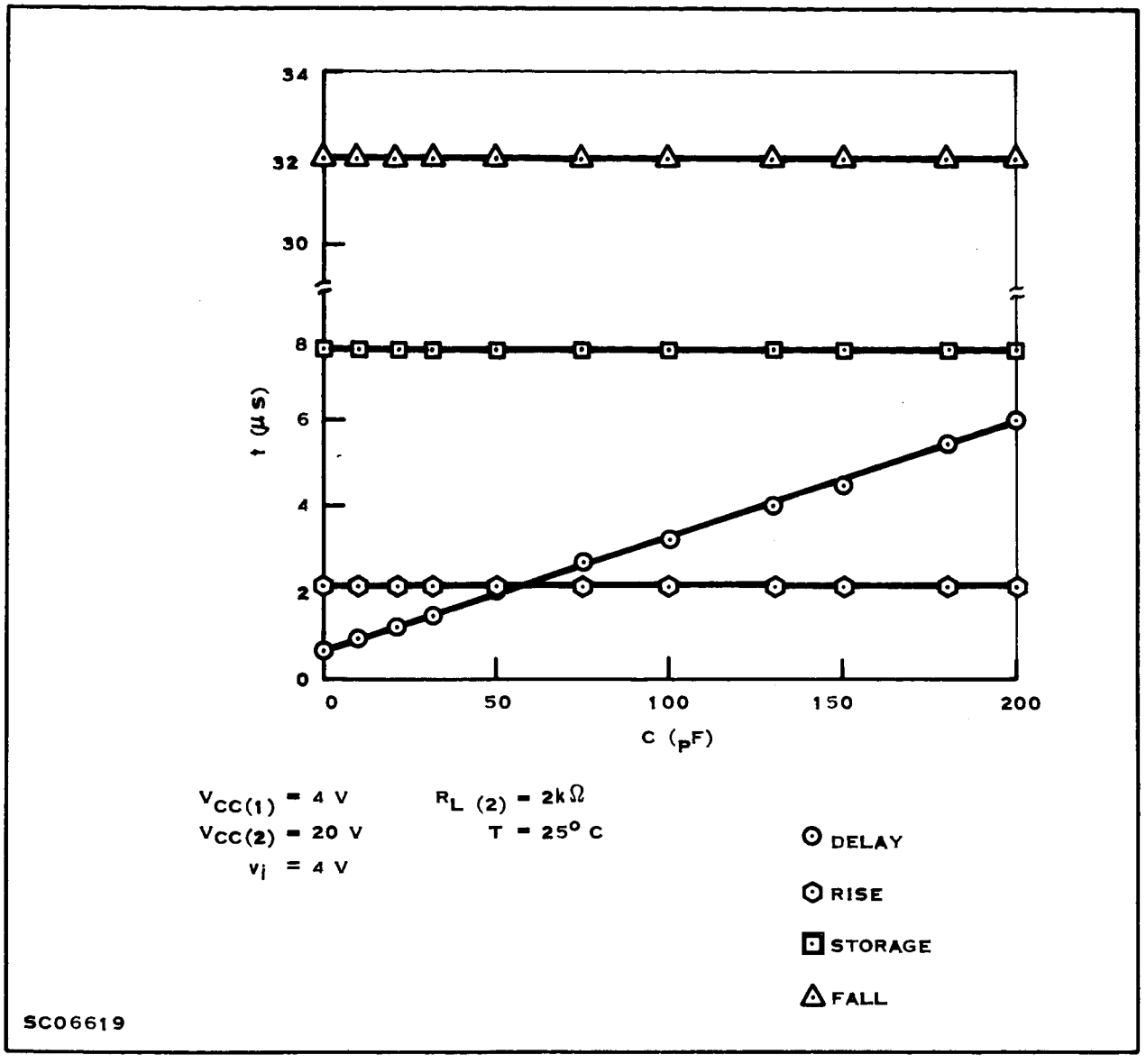


Figure 5. Phototransistor Switching Times vs. Driver Circuit Loading Capacitance

Additional speed measurements were made on the driver circuit breadboard using a diffused resistor between the power supply and base of the first transistor. The resistor consisted of one 17 kΩ or 2 series-connected 17 kΩ resistors from the Texas Instruments type SNX1304. Effects for other (diffused) driver circuit resistors are expected to be negligible.

For large additional capacitance applied to, what will be, the common junction of the input diodes, the delay and rise times of collector current in the driver circuit final transistor were found to be proportional to the resistance, regardless of whether the resistor was diffused or carbon-composition types. For small additional capacitance, delay and rise times at the transistor collector were slightly larger, which can be

accounted for simply by the capacitance of the diffused resistors. Time values were proportional to the resistance (and capacitance) value of the diffused resistors. Indicated delay and rise times with a 27 k diffused resistor are 360 and 180 ns, respectively, compared to 180 and 120 ns for the 27 k carbon resistor. Storage and fall times were the same for both resistance types.

For the switching times at the collector of the phototransistor, the delay time for the diffused resistor was about 600 ns and 900 ns for the 17 kΩ and 34 kΩ values, compared to 700 ns for the 27 k carbon resistor. Rise, storage, and fall times were identical for both types.

In conclusion, the distributed capacitance of the large value resistor in the driver circuit should have only a small effect on the switching time characteristics of the complete isolation switch.

For the modified phototransistor design, $C_{CB} \doteq 15$ pF, compared to the value of 11 pF for devices of the original geometry used in the previous measurements. Use of the new transistor should affect only the rise and fall times measured at the output of the phototransistor. For the same values of $H_{FE}$, both times should increase by the capacitance ratio of about 1.36, as described in Eq. (1) and (2). The total rise and total fall times for the new transistor would be about 4.4 μs and 51 μs, respectively, compared to the maximum specifications of 10 μs and 100 μs.

2. Light Emitting Diode Current

Measurements were made of the current available for the GaAs diode in the driver circuit breadboard as a function of input voltage at -20, 25, and 100° C with supply voltages of 3.5 and 4.5 volts. The results are shown in Figure 6 and 7, with the resistor values indicated (see Figure 5, first quarterly report[5]).

## C. COUPLING GLASS AND EPOXY ENCAPSULATION

The glass bonding medium used between the GaAs and Si wafers of the GaAs Switch is chosen according to its overall performance considering the following desired characteristics:

1) High refractive index relative to that of GaAs (3.6) and Si (3.4).

2) Good mechanical adhesion to GaAs and Si.

3) Good thermal expansion match to GaAs and Si.

4) High transparency to wavelength of emitter.

5) Bonding temperature compatible with fabrication and reliability.

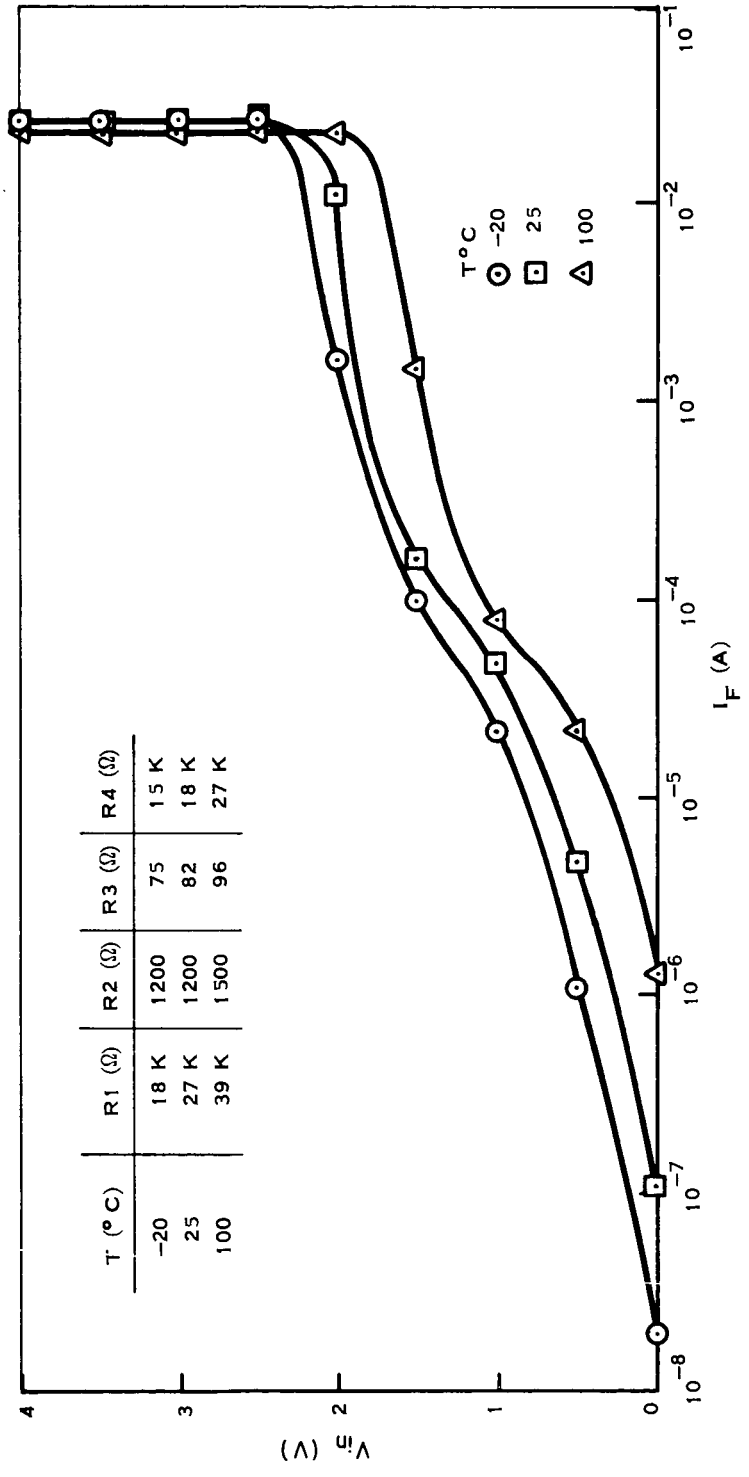


Figure 6. Driver Circuit Breadboard Test — GaAs Diode Current vs. $V_{in}$ for $V_{CC}$ = 3.5 V

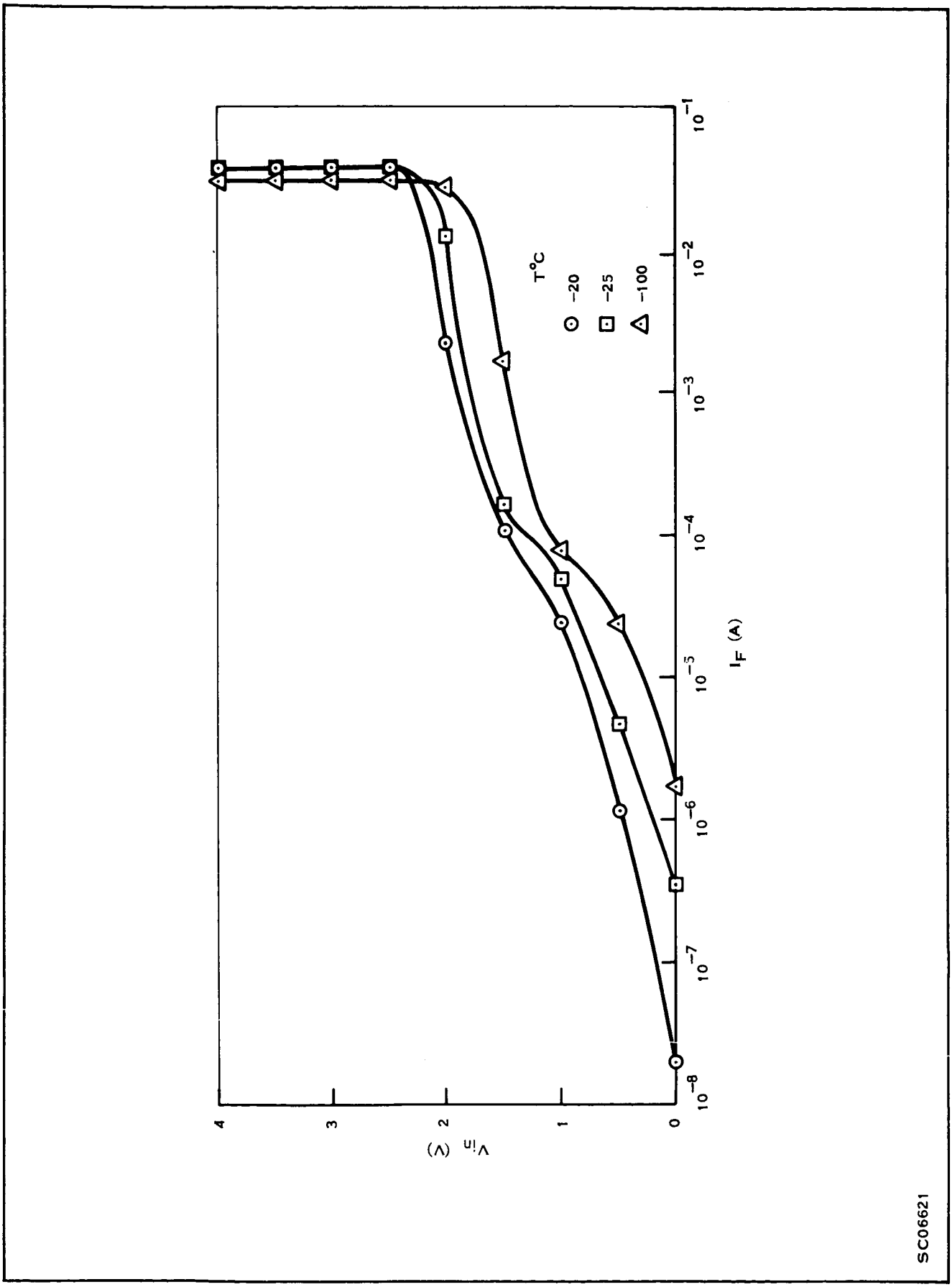


Figure 7. Driver Circuit Breadboard Test — GaAs Diode Current vs. $V_{in}$ for $V_{CC}$ = 4.5 V

These are highly restrictive requirements. Only a few types of glasses can be considered. The glass which, to date, has been found to best satisfy the requirements is in the Se-As-S family. The bonding operation is performed at approximately 210°C Tests were made to evaluate softening within the operating and storage temperature extremes of the GaAs Switch. At 100° C, the glass is only moderately soft, demonstrating no tendency to flow. However, there is some question as to whether this would be sufficient at this temperature in a highly vibrating environment. For this reason, encapsulation is desirable. At 150° C, the glass is fairly soft with some tendency to flow. The good wetting characteristics and surface tension of the glass tends to hold the wafers in stable positions at 150° C. Encapsulation can also ensure structural integrity at this temperature.

The coupling glasses tested tend to have about the same temperature range ($\Delta$ T) for satisfactory operating. The above glass previously exhibited highly stable low temperature coupling characteristics to below -55° C and is presently used in the SNX1304. Other glasses have shown tendencies of fracturing at the low temperature extremes, causing some variance in the coupling on temperature cycling.

The encapsulation used in the SNX1304 is a proprietary epoxy compound which wets the wafers, coupling glass and glass in the bottom of the header. The epoxy is cured to a very rigid state. It is quite firm at 100° C; at 150° C, when deformed under high pressure, it is elastic.

Tests show that application of this epoxy directly on the entire surface of the phototransistor results in no increase in high temperature leakage.

The Se-As-S glass and epoxy encapsulation are a highly desirable combination for the GaAs Switch.

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