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DESIGN AND DEVELOP A

MOS MAGNETIC MEMORY

FINAL REPORT OF STUDY PHASE

11 March 1966 through 11 September 1966

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1.0 FOREWORD

This is the final report for the six-month study phase of contract NAS8-20594 and covers the six-month period beginning 11 March 1966 and ending 11 September 1966.

2.0 REVIEW OF OBJECTIVES

The objective of this program is to determine the interface problems which exist between and within plated wire memories and MOS memory electronics, with an ultimate view of reducing the total number of such interfaces.

3.0 INTRODUCTION

Metal oxide semiconductor (MOS) integrated circuitry has been heavily investigated as a means of producing low cost, low power, highly reliable digital computer logic circuits.

Plated wire elements have been investigated in a similar manner to produce the identical goals within the memory area.

While these separate efforts have proven successful, the large gray area of memory electronics remained untouched. This interface area has been thoroughly investigated during the study phase of this contract and it has been shown feasible to design the memory electronics with MOS devices. A spaceborne computer constructed of MOS circuitry and a plated wire memory can provide considerable improvement in reliability over present day computers.

The interface problems between plated wire memories and MOS devices were determined, and solutions to these problems investigated and evaluated. The most important interface areas are:

1. Package compatibility between the plated wire stack and the MOS devices.

2. Interconnection of the memory and MOS devices.

3. Interconnection of the various MOS functional blocks.

4. Total reduction of interfaces and interface connections.

5. Manufacturing compatibility of the plated wire and the MOS devices.

6. Power and speed requirements.

Each of these areas is discussed in detail in the following sections of this report.

Brief descriptions of the plated wire element and the MOS devices are contained in the following paragraphs.

3.1 Plated Wire

A plated wire memory element consists of a plated wire with an orthogonal current drive strap, as shown in Figure 1. Since the magnetic film has a preferred orientation of magnetization in the circumferential or easy direction, and exhibits a rectangular hysteresis loop, the two remanent storage states are oriented either clockwise or counterclockwise. In the axial or hard direction, the magnetization is reversible and linear.

During the READ mode a current passed through the word strap produces a field which is parallel to the hard axis. This field rotates the stored remanent magnetization from its circumferential direction into alignment with the hard axis thereby inducing a voltage in the bit wire, which functions as a sense line during the read operation. The polarity of the induced voltage is dependent upon the direction of the remanent state. When the word field is less than the film anisotropy, H_k, the removal of the word current will permit the magnetization vector to fall back to its original position. This constitutes a nondestructive readout (NDRO).

The conditions necessary for magnetization reversal by the application of circumferential and axial fields to result in an NDRO memory may be understood by referring to Figure 2. This figure is the Stoner-Wohlfarth astroid[1] as corrected for the existing conditons of nonpure rotational switching. Outside the astroid, reversible switching occurs. In between are areas where the switching mechanism is not clearly defined, and the extent of this area is a measure of the quality of the film. The smaller the area, the better the film. For NDRO operation, the orthogonal components (h_w and h_b) of the applied field H must each be within the NDRO zone, and their simultaneous vector sum must also not exceed the inner curve of the astroid. Not shown in Figure 2 are the effects of

2

1063-248A

MAGNETIZATION VECTOR-ZERO
STORED-REST POSITION

MAGNETIZATION VECTOR-ZERO
STORED-POSITION
DURING WORD PULSE

HARD DIRECTION
OF MAGNETIZATION

WORD
CURRENT

h_w
WORD
FIELD

EASY
DIRECTION OF
MAGNETIZATION

h_b BIT FIELD FOR
ZERO

PLATED
WIRE

BIT
CURRENT h_b BIT FIELD
FOR ONE

WORD
STRAP

MAGNETIZATION VECTOR-ONE
STORED-REST POSITION

MAGNETIZATION VECTOR-ONE
STORED-POSITION
DURING WORD PULSE

FIGURE 1.   INFORMATION STORED ON PLATED WIRE

3
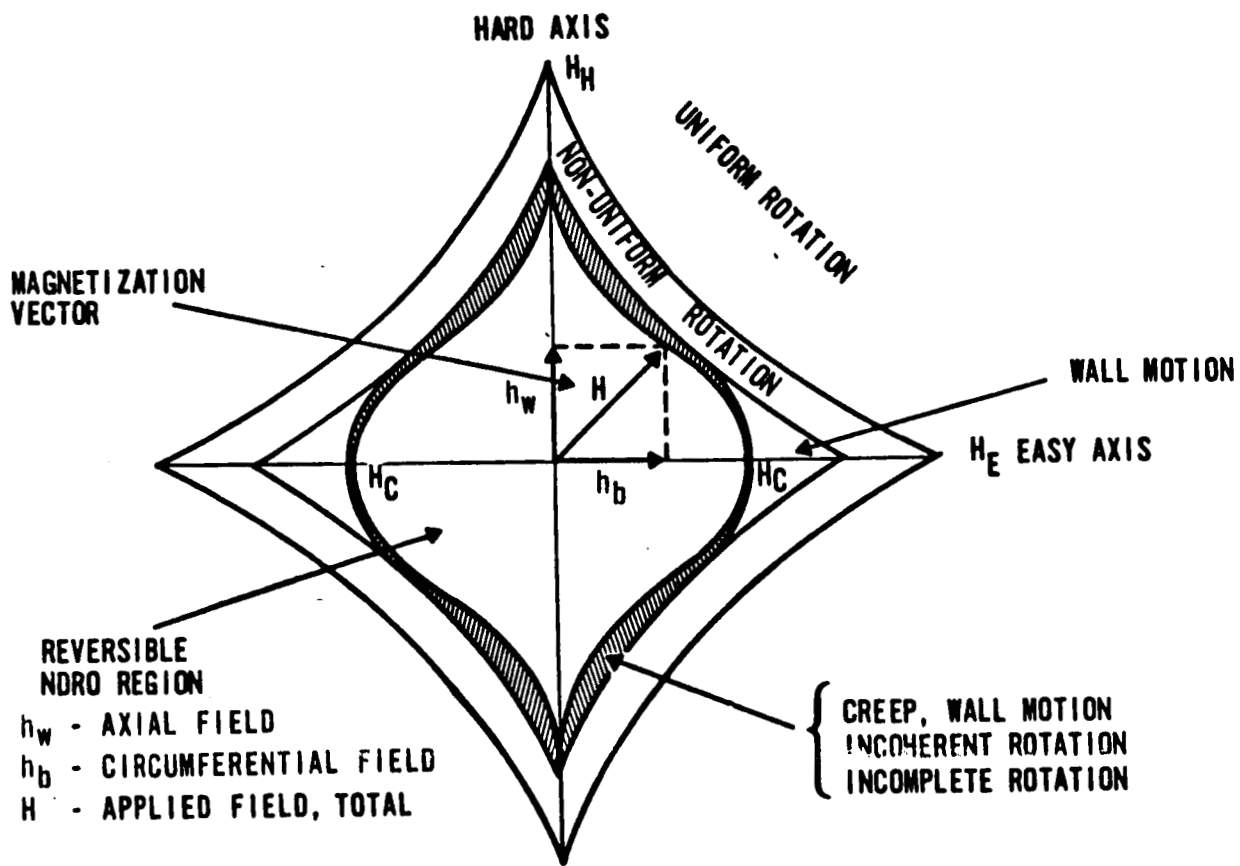
FIGURE 2. STONER-WOHLFARTH ASTROID

skew and dispersion which occur to some extent with all films. Skew is the term used for the angle between the easy axis distribution median value and some reference direction, while angular dispersion refers to the angular dispersion around this median. Both these effects are undesirable, and in effect reduce the effective working area for reversible switching.

The output of a single plated wire bit is shown in Figure 3.

During the WRITE mode the bit current produces a circumferentially oriented field. This field, when applied in coincidence with the word field, will incline the magnetization in an axial magnitude and polarity of the bit field. Subsequent removal of the word field aligns the net magnetization in the proper bit field direction. The removal of the bit field then completes the write cycle.

Figure 4 illustrates the write switching cycle using the idealized hysteresis loops of the easy and hard directions. The outer large loop results from solely applying a bit current, and is the easy direction loop. The inner linear curve results from the application of only an axial or word field. The remaining third curve represents the magnetization characteristics when both an axial and circumferential field are applied.

Assuming an initial condition of remanence at point 1, a circumferential bit field (H_b), less than the disturb value (H_d), is applied resulting in a flux change to point 2. With the addition of an axial field (H_w), less than the film anisotropy field (H_k), the magnetization vector is inclined in a direction established by the resultant field (H_r). This is indicated by a flux change to point 3 on the inner loop. Removal of the axial field aligns the magnetization in the circumferential direction established by the bit field, and is shown as point 4 on the easy direction loop. Subsequently, the circumferential field is removed and point 5 represents the new remanent flux state. Flux reversal from point 5 to point 1 can be described in an identical manner.

3.2 MOS Devices

Switching circuits are normally designed with enhancement mode MOS transistors. These devices are normally off with zero gate voltage; therefore, they act as on-off switches and require only a single supply voltage.

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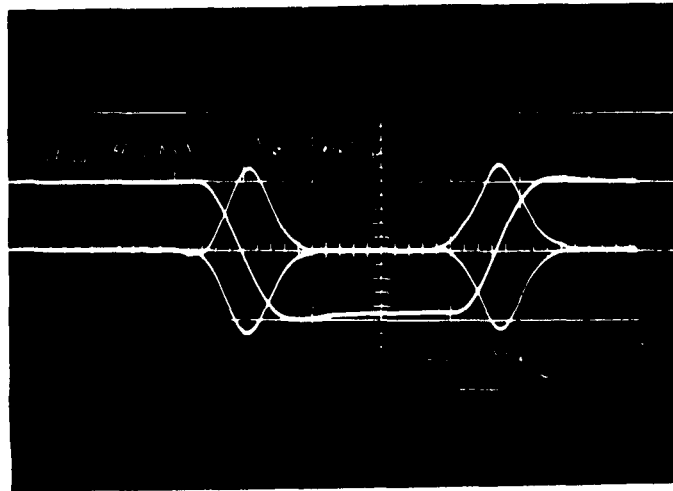
SWITCHING CURRENT & VOLTAGE OUTPUT:
1 BIT: PLATED WIRE
$I\omega$ - WORD CURRENT: ma
V_0 - VOLTAGE OUTPUT: mv

HORIZONTAL SCALE: 50 nsec/DIVISION
VERTICAL SCALE: 5 mv/DIVISION

FIGURE 3. CURRENT AND VOLTAGE OUTPUT
OF PLATED WIRE
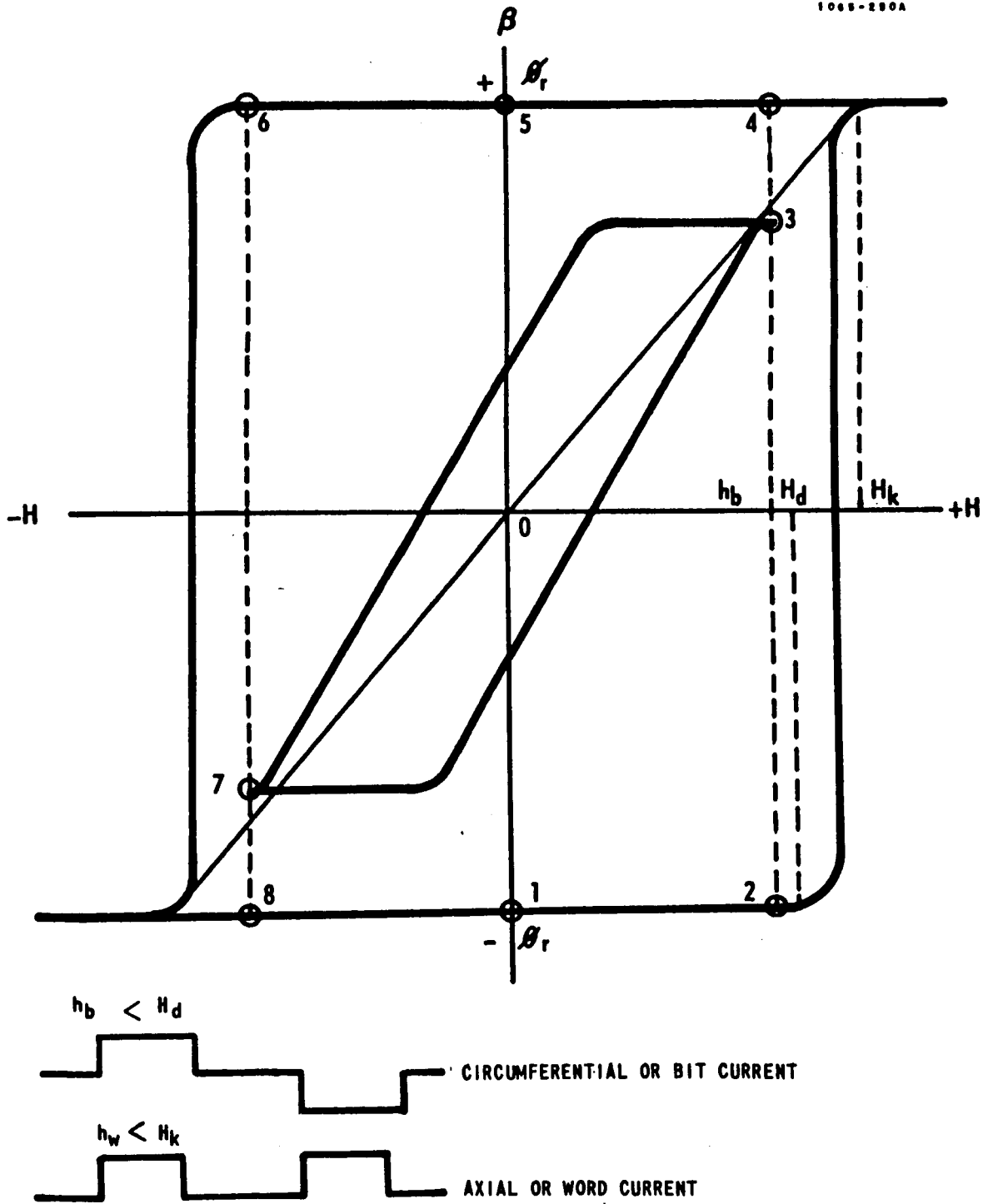
FIGURE 4. IDEAL MAGNETIZATION CURVES

Figure 5a shows the cross-section of a single MOS transistor. It consists of a block of N type silicon called the "body" or "substrate", into which P^+ impurities have been diffused in two parallel strips called, respectively, the "source" and the "drain". In operation, an induced P-region known as the "channel" connects source and drain. The surface of the silicon is covered by a protective layer of silicon dioxide formed during the silicon planar process and etched away along the longitudinal axes of the source and drain, exposing the silicon beneath. Metallic contacts are deposited over the exposed silicon area in the source and drain. The "gate" is a metallic conductor deposited over the oxide between the source and drain and separated from the source, drain, and substrate by the oxide.

If the gate, source, and substrate are grounded and a negative voltage is applied to the drain, no current will flow between source and drain since the drain-to-body P-N junction is reverse-biased. As a result, the source and drain are isolated from each other. However, if a negative voltage is also applied to the gate, electrons are repelled from the surface region of the silicon immediately beneath the gate and holes are attracted to it. As the gate-to-source voltage, V_{GS}, becomes more negative, this surface region finally changes or "inverts", becoming P-type instead of N-type. This inverted region, called the "channel", provides a path for conduction of the charge carriers between the source and drain so that, if the drain voltage is made appreciably more negative than the source, current flows from source to drain. Before the surface can be inverted to form a channel, the gate voltage must reach a certain threshold value V_T sufficient to neutralize surface charges. Typical processing can achieve a V_T of approximately -5V. Turn-on characteristics of a typical MOS FET are shown in Figure 5b.

As the gate voltage V_{GS} becomes more negative than V_T, the channel depth-- and hence conduction-- increases. For low currents, the channel behaves like a normal ohmic resistance, and the device operates in the linear region of its characteristic curve (Figure 5c), where the drain-to-source current I_{DS} is proportional to the drain-to-source voltage V_{DS}. As V_{DS} becomes more negative, however, the current eventually levels off or "saturates". The magnitude of current flow is now relatively independent of the drain-to-source voltage.

Depletion mode MOSTs operate in a similar manner except for the condition of zero gate voltage. Under this condition, the depletion mode MOST is turned on and conducts a finite value of drain current. This is due to the method of fabrication; a channel is formed in the device during

0466-268A

SOURCE   GATE   DRAIN

ALUMINUM
SOURCE
CONTACT

ALUMINUM
GATE
CONTACT

ALUMINUM
DRAIN
CONTACT

t_{ox}

OXIDE

W

N⁻   P+

CHANNEL

P+

SUBSTRATE

ℓ

w: GATE WIDTH
ℓ: GATE LENGTH
t_{ox}: GATE OXIDE THICKNESS
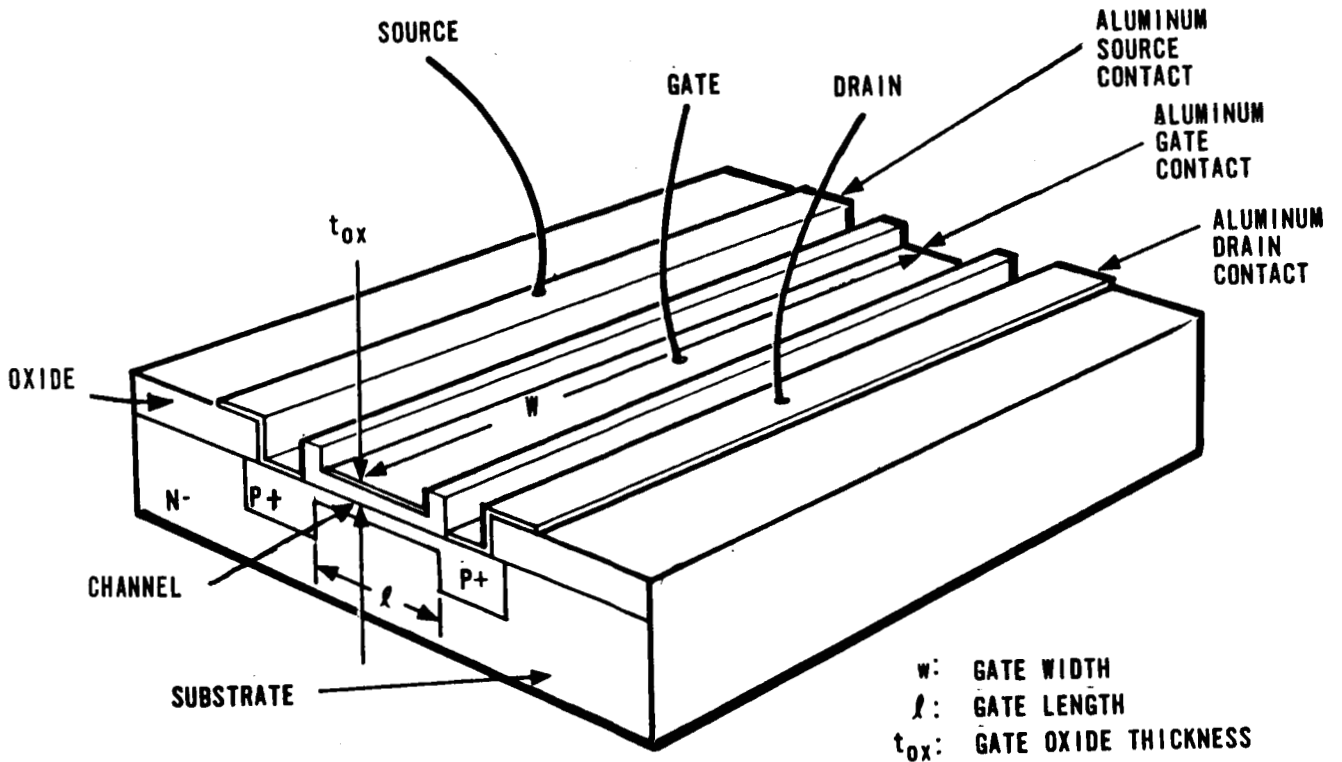
(a)

TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)

−20   −10   0

I_D(mA)

−50

−100

(b)

DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)

−20   −10   0

$V_{GS} = -5$
−6
−7
−8
−9
−10
$V_{GS} = -11$

I_D(mA)

−50

−100
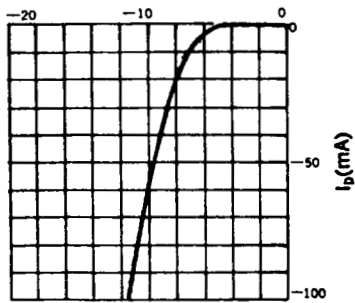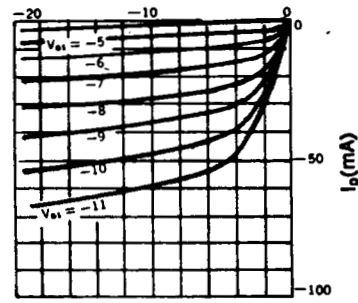
(c)

FIGURE 5. CROSS-SECTION OF MOS TRANSISTOR
AND ASSOCIATED CHARACTERISTIC CURVES

the manufacturing process. It becomes necessary to reverse bias the gate in order to reduce the drain current to zero. This reverse bias causes the cross-sectional area of the channel to be reduced to zero; hence the source and drain regions become back-to-back diodes and only diode leakage current is present. The depletion mode device has certain characteristics which make it more useful as an amplifier.

The more detailed characteristics of both the enhancement mode and the depletion mode MOSTs are discussed in other sections of this report.

4.0 SUMMARY

A comparison of address selection methods using MOS transistors was made. The interconnections were minimum where individual word drivers were used for each line. The complete selection circuitry and the associated word drivers are located on the same memory plane as the word lines, hence reducing the stack interconnections considerably.

The circuitry interfacing with the plated wire elements was investigated extensively. This consisted of the word driver and sense amplifier circuits. The limitations of the MOS transistor as a high current switching device were analyzed in terms of its geometry and operating parameters. Data were presented to demonstrate that the projected improvement in geometry and processing of the MOS transistor could enable it to be used effectively as a word driver for a plated wire memory element.

The detailed analysis of an all-MOST differential amplifier was performed to determine its limitations as a memory sense amplifier. The common mode rejection capability, utilizing present devices, does not appear to be sufficient for large common mode voltages, although the future fabrication of devices with better control of g_m and r_d will certainly show considerable improvement.

Both the word driver and the sense amplifier functions can be accomplished with MOS devices as will be demonstrated by the feasibility memory to be fabricated during the next phase of the contract.

The reduction of interfaces within a monolithic MOST logic function was investigated. Interconnections and crossovers are accomplished by the

utilization of common diffused regions, diffused "tunnels", and multilayer conductors. Materials and techniques for performing the interconnection and insulation of conductors was investigated also. An additional reduction of interconnection interfaces can be accomplished by the utilization of monometallic interconnection systems. The two most promising approaches appear to be either an all aluminum system or an all gold system. Interface interconnections are further reduced by the utilization of the interconnection concepts developed under a separate contract for use in the MICPAK packaging technique.

The complete selection circuitry for 16 word drivers was designed and a possible chip layout configuration investigated. The selection circuit consists of a four-stage F/F address register, decoding logic, word drivers, and clock circuits.

The fabrication processes of single type MOSTs, and combinations of MOSTs and bipolar transistors were investigated. The major process steps are outlined within the text of this report. As the number of types of devices increases, the complexity of the fabrication processes also increases. The plated wire manufacturing process is discussed briefly, showing the nonexistence of any manufacturing incompatibilies between MOS Devices and plated wires.

The advantages of complementary MOST logic circuitry were investigated. The major advantages over single type MOSTs are a significant increase in operating speed and a considerable reduction in power dissipation.

The cycle time of a 1,000-word plated wire memory utilizing P channel logic and N channel amplifier MOSTs was calculated to be 2.5 microsecond with a power dissipation of approximately 45 watts.

5.0 PACKAGE COMPATIBILITY BETWEEN THE MEMORY AND THE MOS DEVICES

The plated wire memory elements and the MOS functional blocks are physically smaller than ferrite toroids and discrete transistors hence, they can be very compatible when contained in the same package. During the course of the study phase of this contract, no aspects of the overall package revealed any incompatibilities between the memory and the MOS devices. The memory organization and package configuration is discussed in more detail in the following paragraphs.

Several approaches to the memory organization were discussed in the third monthly report. The most efficient organization is shown in Figure 6. A 512-word 28-bit (26 active and 2 spares) is used for illustration. The nine address bits from the processor are broken into two groups. The five lower bits are used for word selection in each of the 16 selection circuits. The remaining four bits are decoded and used to select the individual selection circuit. Each selection circuit module contains a five-bit storage register, a decoding tree, and 32 word driver MOSTs. Each word line has its own word driver device instead of the normal selection diode. Each complete plane contains 128 memory words and all the associated selection circuitry. There is one multilayer board for each stack which contains the timing and control, module select, sense amplifiers, bit drivers, and any necessary buffer circuitry required between the memory and processor.

The size of the memory stack is dictated by the following parameters:

1. Sense wire spacing

2. Word line size and spacing

3. Sense line replaceability

4. Memory word expansion

5. External interface requirements

6. Grounding requirements.

The solution to the optimization of these parameters led to the design of a multilayer memory plane on each side of two multilayer substrate boards as in Figure 7. The substrate boards are hinged on the frame to provide direct accessibility to the MOS functional blocks and sense wires.

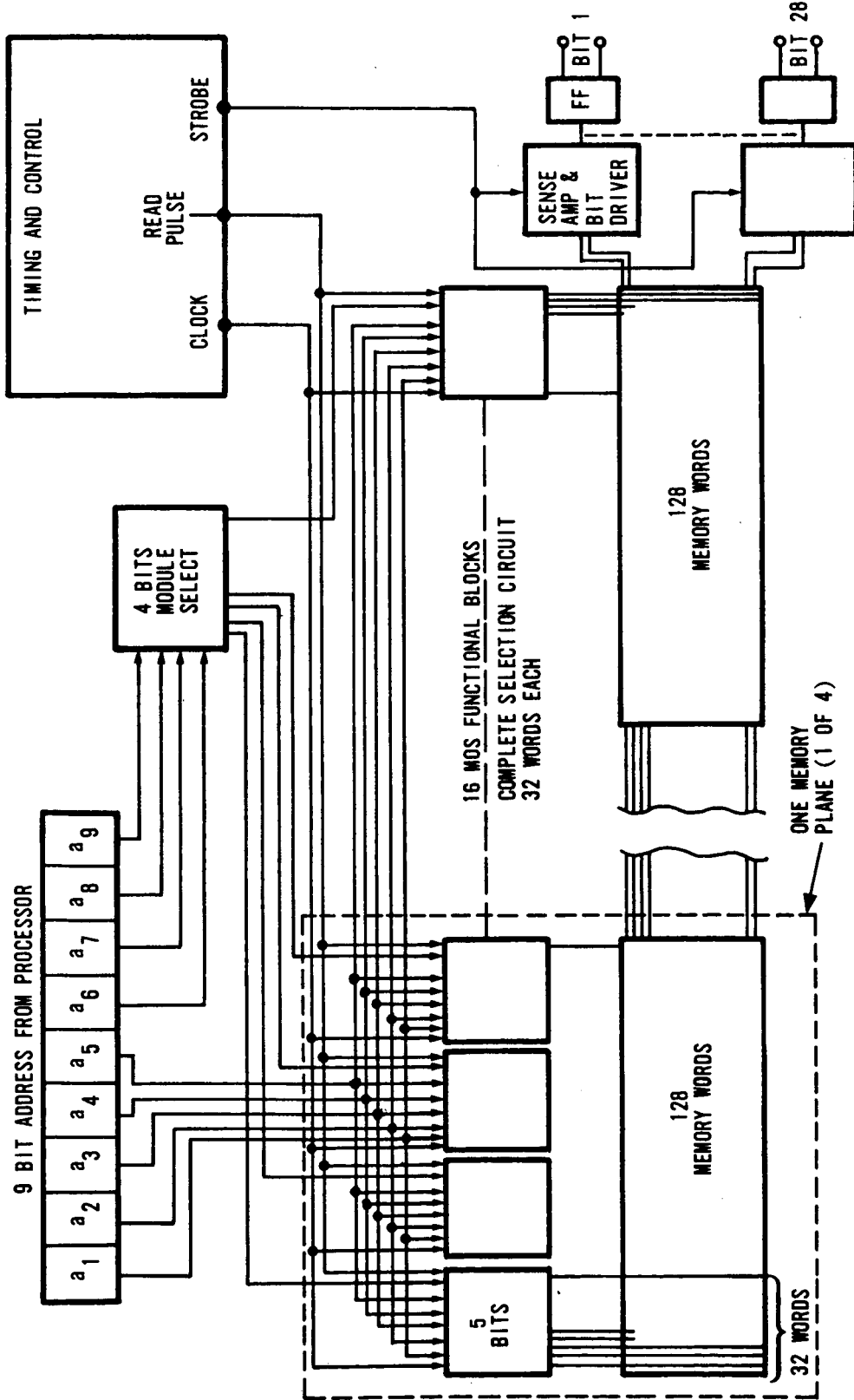FIGURE 6. MOS PLATED WIRE MEMORY - 512 WORDS 26 BITS EACH

13
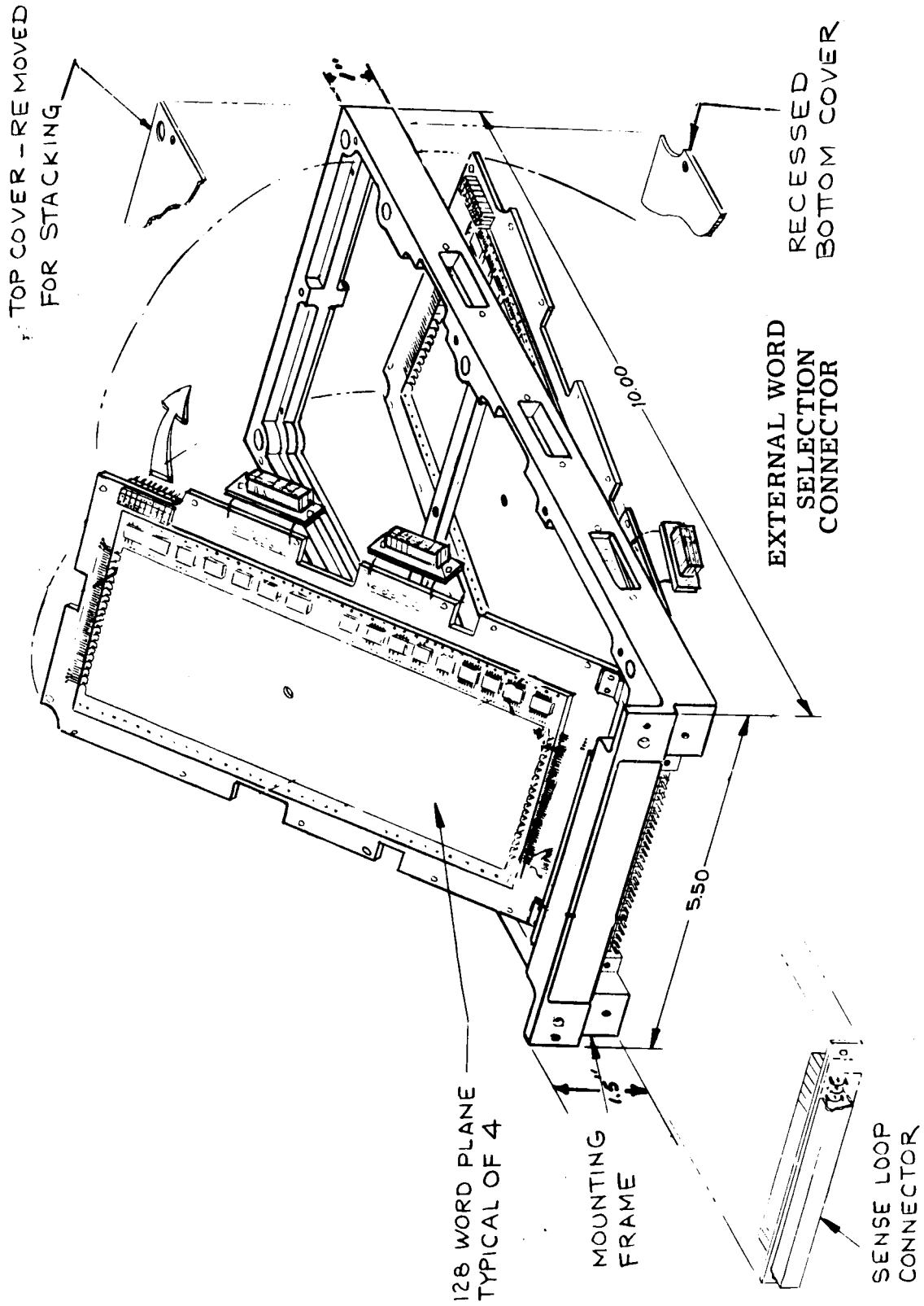
FIGURE 7. MEMORY STACK CONSTRUCTION

TOP COVER – REMOVED FOR STACKING

RECESSED BOTTOM COVER

EXTERNAL WORD SELECTION CONNECTOR

10.00

5.50

1.5

128 WORD PLANE TYPICAL OF 4

MOUNTING FRAME

SENSE LOOP CONNECTOR

6.0 INTERCONNECTIONS OF MEMORY TO MOS DEVICES

The interconnection of the memory and the MOS devices involves both electrical and mechanical interfaces.

The two major areas of electrical interfacing is the Word Driver and the Sense Amplifier. The MOS word driver circuit has the responsibility of generating current pulses of relatively large magnitude (200 to 400 ma) and with fast rise times (typically 50 nanoseconds). The MOS sense amplifier has the responsibility of detecting a very small signal (typically 5 millivolts) which occurs simultaneously with noise in the range of 50 to 200 millivolts and amplifying it to the voltage level required of the logic circuitry. These two functions can be accomplished with MOS transistors as will be shown in this section of the report.

The mechanical interface involves the reduction of interconnections and the reduction of the intermetallic interfaces present in the remaining interconnections. These are discussed in Sections 7 and 8.

6.1 MOS WORD DRIVER

The limitations of the MOS transistor as a high current switching device can be analyzed in terms of its geometry and its operating parameters.

Any device used as a word driver must be capable of supplying a pulse of 200 to 400 ma of current with a rise time or fall time of 50 nanoseconds, since the readout of an NDRO plated wire memory element occurs during both the rise and fall time of the word current pulse. The output can be sampled at either time. The magnitude of the output is a direct function of rise time or fall time which is about 50 nanoseconds for a reasonable output. The word driver device considered during this phase of the program is an enhancement type P channel MOS transistor.

The MOS transistor parameters which have the greatest effect on the word driver performance are as follows:

- Drain current: I_D

- Input capacitance: C_i

- Drain-to-Source "On" resistance: R_{on}

- Power dissipation

- Device Size (area)

- Breakdown voltages.

The drain current must be of the magnitude of 200 to 400 ma to drive a plated wire memory element. It is desirable to keep the input capacitance as low as possible in order to obtain the fastest possible rise or fall time of the gate-to-source input voltage. The drain "On" resistance contributes to the $I^2 R$ losses, current regulator requirements, and switching speeds. The maximum operating voltages are limited by device breakdown voltages. The device size and power dissipation dictates how many of these devices can be contained in a single integrated circuit chip.

Drain Current

The equation for the drain current capability of a MOS transistor is given by Sah [2] as:

$$I_D = \frac{\mu_p C_G}{L^2} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \text{ in amperes} \qquad (1)$$

where:

μ_p is the surface mobility of holes in cm^2/volt-second.

C_G is the gate to channel capacitance in farads.

L is the gate length (separation of drain and source) in cm.

V_{GS} is the input gate-to-source voltage in volts.

V_T is the turn-on threshold of an enhancement type MOS transistor in volts.

V_{DS} is the drain-to-source voltage in volts.

The gate capacitance, C_G is the parallel plate capacitance of the gate electrode and the channel and is given as:

$$C_G = 0.08842 \frac{\epsilon_r L W}{t_{ox}} \text{ pf} \qquad (2)$$

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where:

ϵ_r is the relative dielectric constant of the oxide

L is the gate length: cm

W is the gate width: cm

t_{ox} is the oxide thickness: cm

Substituting for C_G, Equation 1 becomes:

$$I_D = 0.08842 \times 10^{-12} \frac{\mu_p \epsilon_r W}{L t_{ox}} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \text{amperes} \quad (3)$$

The properties μ_p, ϵ_r, t_{ox}, and L are limited by the materials and processing techniques used in manufacturing the MOS transistors. Surface mobility, μ, is a function of the conditions existing at the silicon surface and within the gate oxide, which are very hard to predict and control. [3, 4, 5, 6]

The cited references (2 through 6) indicate that the surface mobility of holes can vary from 94 to 204 $\frac{cm^2}{volt\text{-}sec}$ and the surface mobility of electrons can vary from 200 to 500 $\frac{cm^2}{volt\text{-}sec}$. Therefore, an N channel MOS transistor with similar geometry should be able to handle approximately twice the drain current.

The dielectric constant of the gate insulator is fixed as a result of the use of silicon dioxide which has a dielectric constant of approximately 4.0. Present processes use an oxide thickness, t_{ox}, of approximately 1000 Å, in order to obtain theoretical breakdown voltages up to 100 volts. The finished oxide surface is highly irregular, with many small areas which are considerably less than the desired 1000 Å thickness. These are the areas that limit the maximum usable gate voltage. This will also allow an increase in device drain current.

The gate length, L, of available devices is nominally 5 microns. This is an optimum value in keeping with present photolithographic techniques. Without pushing the state of the art gate lengths of 3 microns can be produced, and future processes should reduce this to 2 microns.

The gate-to-source threshold voltage, V_T, is not an inherent property of the basic material from which the MOS transistor is constructed, as is the case of the bipolar transistor. The bipolar base emitter threshold voltage is a function of the semiconductor material and doping. The MOS transistor threshold voltage is a function of the conditions existing at the semiconductor surface and within the gate oxide. Since these conditions are more a result of processing than material properties, the threshold voltage varies considerably from device to device [7]. (A typical MOS transistor will have a value of V_T equal to 5 volts with a ±1.0 to ±1.5-volt tolerance.) Therefore, the gate width, W, is by far the most practical method used today to control the final current handling capability of the MOS transistor.

The terminal characteristics of the optimum P channel word driver MOS transistor are:

Drain to source voltage: -25 Vdc

Gate to source voltage: -25 Vdc

Gate to drain voltage: -25 Vdc

Gate to source threshold voltage: -5 Vdc

Gate to source capacitance: 8 pf

Gate to drain capacitance: 5 pf

Drain to source capacitance: 5 pf

Drain to source "on" resistance: 12 ohms

This dictates a device with the following approximate geometrical dimensions:

L_{GC} = Length of channel = 2.0 microns

L_{SO} = L_{DO} = Length of entire overlap of gate metalization over source region = 2.0 microns

T_{GOX} = Thickness of gate oxide = 750 Å

W_G = Width of gate (channel = 180 mils)

Chip size: 15 mils x 15 mils

A presently available P-channel MOS transistor capable of handling a maximum of 250 ma dc was examined in order to become more familiar with the device geometry necessary to handle this magnitude of drain current. (This device can handle current pulses in excess of 400 ma with power dissipation being the limiting factor.)

The General Instrument Corp. MEM517A was chosen for this purpose. The most important features of this device, other than the large value of drain current are:

- Drain to source voltage: -30 Vdc

- Gate to source voltage: -25 Vdc

- Gate to drain voltage: -25 Vdc

- Gate to source capacitance: 16 pf

- Gate to drain capacitance: 10 pf

- Drain to source capacitance: 10 pf

- Drain to source "on" resistance: 30 ohms

- Gate length: 0.45 mil

- Gate width: 180 mils

- Chip size: 45 mils x 45 mils

Input Capacitance. The input capacitance of a MOS transistor, together with the driving source impedance determine, to a great extent, the maximum switching speed of the drain current.

As discussed in the previous paragraphs, a MOS transistor capable of handling the required word current will have a very wide gate region which results in a large value of input capacitance (15 to 25 pf). The input capacitance consists of the active gate capacitance, the drain and source overlap capacitances, and the stray capacitance associated with the gate metalization which extends out over the body where external contact to the chip is made.

The sum of these capacitances is given as:

$$C_i = C_G + C_{GS} + (A-1) C_{GD} + C_{GB} \qquad (4)$$

where:

C_i = total input capacitance

C_G = active gate capacitance (between gate and channel)

C_{GS} = capacitance between the source and that part of the gate electrode which overlaps the source region.

C_{GD} = Capacitance between the drain and that part of the gate electrode which overlaps the drain region.

$(A-1)C_{GD}$ = Miller feedback capacitance

C_{GB} = capacitance between that part of the gate electrode which extends out over the silicon body (substrate) and provides the bonding area for the external connection.

The locations of these capacitive elements within the silicon chip are shown in Figure 8. The input capacitance measures approximately 25 pf which is approximately equal to C_i of Equation 4, including the Miller effect. In current mode applications such as the word driver, the voltage gain is normally very low, hence the Miller effect becomes negligible. A MEM517A was cross-sectioned to determine its geometrical dimensions. A schematic diagram of the device cross-section is shown in Figure 9. The dimension designations and the measured values are:

L_{GM} = Length of gate metalization = 12.5 micron = 9.5 mils

L_{OX} = Length of gate oxide = 7.5 microns = 0.3 mil

L_{GC} = Length of channel = 3.5 microns = 0.14 mil

$L_{SG1} = L_{DG1}$ = Length of lateral diffusion of source and drain respectively under gate oxide = 2 microns = 0.08 mil

$L_{SG2} = L_{DG2}$ = Length of overlap of gate metalization over source oxide and drain oxide respectively = 2.5 micron = 0.1 mil

$L_{SO} = L_{DO}$ = Length of entire overlap of gate metalization over source and drain regions respectively ($L_{SG1} + L_{SG2}$ and $L_{DG1} + L_{DG2}$) = 4.5 microns = 0.18 mil.

T_{GOX} = Thickness of gate oxide = 1000 Å = 0.004 mil

T_{SOX} = Thickness of source oxide = 1000 Å = 0.004 mil

T_{DOX} = Thickness of drain oxide = 1000 Å = 0.004 mil

From these measurements, the capacitive elements were calculated and are:

C_{GC} = Gate to channel capacitance = 5.7 pf

C_{GS} = Gate to source overlap capacitance = 7.2 pf

C_{GD} = Gate to drain overlap capacitance = 7.2 pf

$C_{in} = C_{GC} + C_{GS} + C_{GD}$ = 20.1 pf

This value of C_{in} does not include the capacitance contributed by the gate protection zener. Taking the zener capacitance into consideration, the total input capacitance compares favorably with the measured value (25.5 pf). Since drain current is a function of gate to channel capacitance, C_{GC}, only a small part of the total input capacitance contributes to drain current. The remaining capacitances are parasitic and degrading to circuit performance and should be minimized as much as practical. Tolerances associated with present day photolithographic techniques result in the large values of overlap capacitances. Future improvements should reduce this considerably.

The rise and fall times of the word driver drain current are a direct function of the input capacitance C_i and the driving source impedance. MOS transistors normally have negligible storage and delay times, therefore the drain current follows the voltage applied to the gate electrode. Since the driving source impedance is normally much greater than the values of r_D, r_S, and r_C, the equivalent circuit shown in Figure 10 can be reduced to a lumped capacitance C_i, as expressed by Equation 4. The composite equivalent circuit of the driving source and the MOS transistor can be represented by a simple RC network as shown

in Figure 11. Once the word driver device characteristics have been defined, the input capacitance becomes fixed. The maximum allowable driving source impedance can now be determined. For example, to obtain a word current rise and/or fall time on the order of 50 nanosec with a single MEM517A requires a driving source impedance of:

$$R_{gen} = \frac{50 \text{ nsec}}{4 \, C_i}$$

$$= \frac{50 \times 10^{-9}}{4 \times 25 \times 10^{-12}} = 500 \text{ ohms}$$

This information can be used to define the geometry of the MOS transistor which drives the word driver device.

Word Driver Test Circuit. A word driver circuit was implemented as shown in Figure 12. The circuit was used to drive an actual plated wire memory element. Information was stored on the wire by use of a dc writing technique where a current is passed through the plated wire in either of two directions. A "1" or "0" is stored as a result of the direction of current flow. The NDRO mode of reading was utilized and the resultant output voltage waveform and the word current is shown in Figure 13. The magnitude of I_w was 400 milliamps and was controlled by adjusting the supply voltage V_{DD2}. The output voltage was approximately 17 millivolts. The value can be expected to be reduced to 8 to 10 millivolts under normal stack operating conditions where the stored bit becomes disturbed and the output signal becomes attenuated. The large rise time of the word current (I_w) was a result of the RC time constant associated with the 2.0 k ohm resistor and the input capacitance of the MEM517As. Since the "on" resistance of the MEM520 is typically 250 ohms, the capacitance discharges very rapidly, and a 50 nanosecond fall time of the word current is obtained. It is during this fast fall time that the output of the plated wire is sensed. This circuit illustrates the duty cycle problem inherent when only P channel devices are used. In order to obtain the proper output voltage swing, the load resistor must be at least 10 times as large as the "on" resistance of the active MOS device. This results in a long RC time constant, hence a low duty cycle. The use of complementary (N channel and P channel) enhancement mode MOS transistors allows a more efficient circuit to be mechanized as illustrated in Figure 14. The on resistance of both MOSTs is on the order of 250 ohms, providing a short RC time constant during both turn-on and turn-off of the word current transistor. The word current pulse

and the output signal are shown in Figure 15. As can be seen the use of complementary MOSTs allows the memory to operate at a faster cycle time. The overall cycle time (including address and decoding logic) of a large memory may be reduced from about 8 to 10 microseconds to about 2 to 4 microseconds.

6.2 MOS SENSE AMPLIFIER

The requirements of a circuit to amplify the small, high frequency output of a plated wire memory stack into a usable logic level signal, can be summarized as follows: Each data signal is typically a few millivolts in amplitude and generally contains a fundamental of at least 20 MHz. The amplifier must be capable of rejecting large common mode signals both during and before signal time. The largest transient signal occurs prior to "read-time" as a result of a preceding "write" or "store" operation. Naturally, the circuit must recover from these input transients in order to accept the next data output signal. Since the operating output signals from a memory sense line cannot be predicted on a repetitive basis, the amplifier requirements are more of a quasi-transient nature.

A common, straightforward approach to the design of this circuit is a dc-coupled, differential amplifier. This approach minimizes the number of associated discrete components, thus resulting in minimum interconnects and package size. Direct coupling the stages of the amplifier also improves the recovery characteristics of the circuit. This improvement is simply a result of the much lower inter-stage RC time constant. As usual, however, a trade-off between this advantage and the dc offset problem must be considered. Offset is a result of differences in the linear region characteristics of the individual stage devices, i.e., in the case of the FET's the quiescent levels of the drains are important. Naturally, the offset of one stage will affect the operating point of the following stage. In all direct coupled differential amplifiers this problem is minimized by matching devices; however, the remaining value is referred to the input in order to evaluate its significance in the application. The worst case memory stack output must be capable of overcoming the amplifier's input offset and provide enough signal to be amplified to the detector to the trigger level.

Typical Amplifier Specifications:

Operating temperature range: -55°C to 125°C

Voltage supply tolerance: ±5 percent

Voltage gain: 6000 to 8000 volts/volt

Operating frequency range: 0 to 20 mHz

Common mode rejection ratio: 1000 : 1 (to 1V)

Common mode frequency range: 0 to 20 mHz

Minimum input voltage range: 1 to 10 mv

Offset (referred to input): 1 mv

The most difficult specification to meet, using MOS devices, is the common mode rejection ratio. To obtain common mode rejection, a balanced circuit such as a differential amplifier is required. In a differential amplifier the first stage must provide the common mode rejection since differential signals at the output of the first stage that are caused by common mode input signals are indistinguishable from differential outputs caused by differential inputs. Therefore, the common mode rejection ratio of a differential amplifier depends upon the symmetry of the first stage of the differential amplifier. For the circuit shown in Figure 16, it was shown in the 5th monthly report that the common mode rejection ratio is limited by

$$\text{CMRR} = (1 + \mu)\left(\frac{\mu}{\delta\mu}\right)$$

where μ is the average voltage gain, $\delta\mu$ is the deviation of μ from the average in each side. For a common mode rejection ratio of 1,000 the change in voltage gain must be less than

$$\frac{1 + \mu}{1,000}$$

$$\frac{\delta\mu}{\mu} = \frac{\delta r_d}{r_d} + \frac{\delta g_m}{g_m} \leq \frac{1 + \mu}{1,000}$$

The μ is usually less than 30 so that

$$\frac{\delta\mu}{\mu} = \frac{\delta r_d}{r_d} + \frac{\delta g_m}{g_m} < 0.03$$

Obtaining a three percent match in voltage gain is unrealistic at the present time especially with an integrated MOST circuit. Other unbalances in circuit parameters will also decrease the common mode rejection ratio so that a slightly tighter specification on μ would be required in an actual circuit.

Another factor which affects the design is the bandwidth. For an MOS transistor the maximum bandwidth is approximately.

$$f = \frac{1}{2\pi R_L \left[C_{ds} + C_{dg} + C_i \right]}$$

where C_{ds} is the drain to source capacitance, C_{dg} is the drain to gate capacitance, C_i is the input capacitance to the next stage, and R_L is the load resistor. The approximate gain that can be obtained with one stage is:

$$G = g_m R_L$$

The gain bandwidth product is

$$GBW = Gf = \frac{g_m}{2\pi \left[C_{ds} + C_{dg} + C_i \right]}$$

Using typical values for C_{dg}, C_{ds}, and C_i of 0.5, 1.5 and 6 pf's respectively gives

$$GBW = (g_m)(2) 10^{10}$$

For a bandwidth of 20 MHz

$$G = g_m \times 10^3$$

At the present time the transconductance is between 5 and 10 millimhos for the values of capacitance that were assumed. The gain per stage is between five and ten and $R_L \cong 1 \text{ K}\Omega$. Thus at least four stages are required, and probably five will be necessary, to meet the gain requirements.

The above considerations indicate that a differential amplifier meeting all the requirements listed is not feasible at the present time. Additional effort in reducing the variations in the MOST parameters could lead to a practical differential type sense amplifier.

An approach to a sense amplifier which appears to be more practical is shown in Figure 17. In this approach the desired common mode rejection ratio is obtained with balum transformers. Obtaining the common mode rejection in this way permits the use of a single-ended amplifier. To obtain a gain of 8000, five stages are needed. Several features of the single-ended amplifier are:

Biasing - an enhancement mode MOS transistor is easy to bias with a single drain to gate resistor.

Drift - MOS transistors are noted for high drift rates. Therefore, the dc gain must be much less than the ac gain. Two methods are available for reducing the dc gain: ac coupling, and dc feedback. AC coupling is shown in Figure 17 since dc feedback has the disadvantage of requiring the feedback path to have a very low cutoff frequency. The low frequency break would occur at about 100 Hz. DC feedback around each stage is an alternative method that could be used, but it would require more parts that are more difficult to integrate.

Strobing - a five stage sense amplifier would present problems in strobing since each sense amplifier may have a different time delay. The strobe pulse must arrive at the amplifier at the proper time to block the read noise and pass the signal.

Recovery - an ac coupled sense amplifier requires time to recover from large differential signals that occur during the "write" mode. The recovery time depends upon the coupling capacitors and the saturation impedance levels.

Assuming the gain and bandpass requirements could be met, the remaining general problem areas are in interstage coupling, frequency stability, and threshold drift. If the drift characteristics cannot be more closely controlled, the amplifier would necessarily need to be RC coupled. As previously mentioned, this coupling technique is undesirable where large input transients can be expected. With the use of a more stable gate insulation such as silicon nitride, the device's drift characteristics may be more closely controlled.

The gain-bandwidth (GBW) product may be increased by the optimization of the device geometry. The gain-bandwidth product is given as [8].

$$GBW = \frac{g_m}{2\pi C_T} \tag{7}$$

where:

for a single stage amplifier: $C_T = C_{DG} + C_{DS}$

for several cascaded stages: $C_T = C_{DG} + C_{DS} + C_{GS}$

It can be shown that the GBW product is inversely proportional to the gate length. By reducing the gate length by a factor of 2; g_m, and as a direct result, GBW will be increased by a factor of 2. Other factors which can be used to increase the GBW product are: N channel transistors have a carrier mobility factor at the surface which is greater than that of a P channel device by at least a factor of 2; gate-to-source overlap capacitance can be minimized by the use of more accurate photolithographic techniques; the gate-to-drain capacitance (which is the familiar Miller feedback capacitance) can be minimized by using a depletion mode device which has the gate electrode offset from the drain region; and drain to source junction capacitance can be minimized by the reduction of the drain surface area. The implementation of all these factors tend to indicate that the GBW of a multistage MOS transistor amplifier could be increased by a factor of 2 to 5. This should provide an N channel device with the following parameters:

Breakdown voltages: 30 Vdc minimum

g_m, transconductance: 12,000 μmhos

C_{DG}, drain to gate capacitance: 0.1 pf

C_{DS}, drain to source capacitance: 0.8 pf

C_{GS}, gate to source capacitance: 3.4 pf
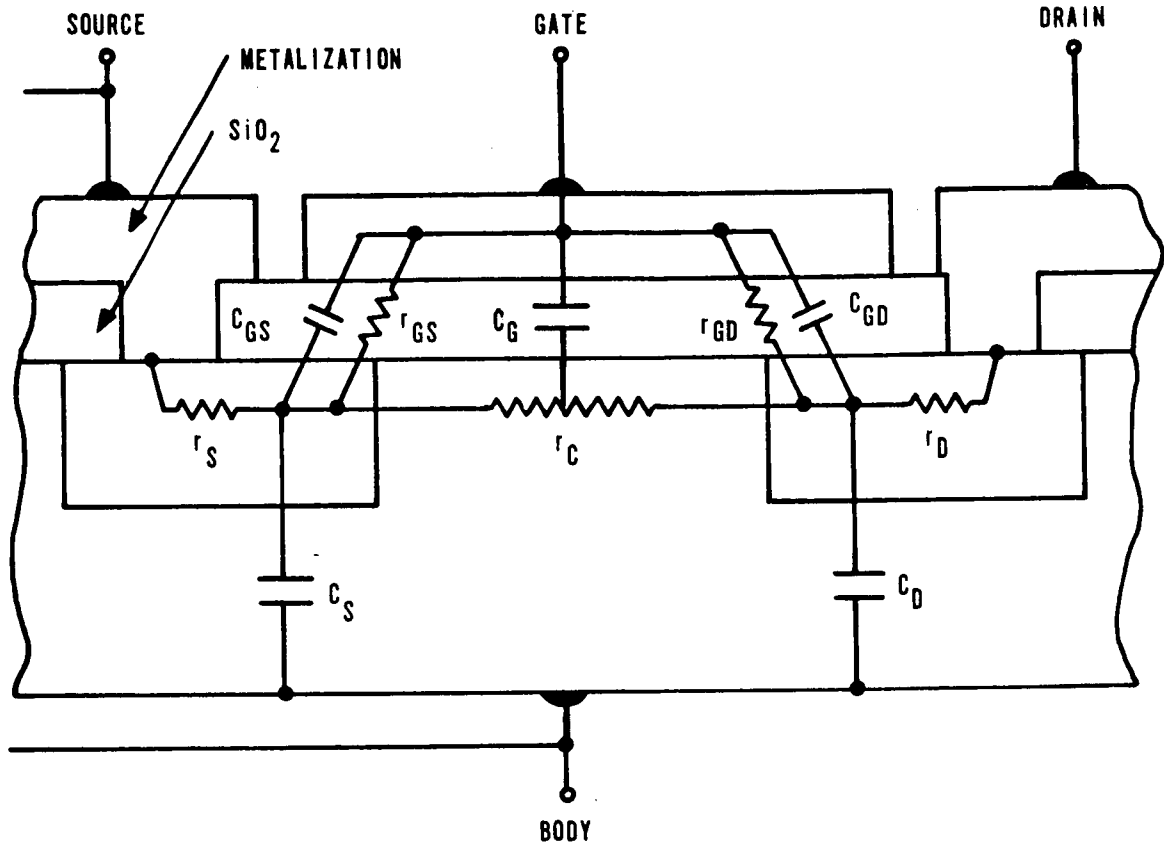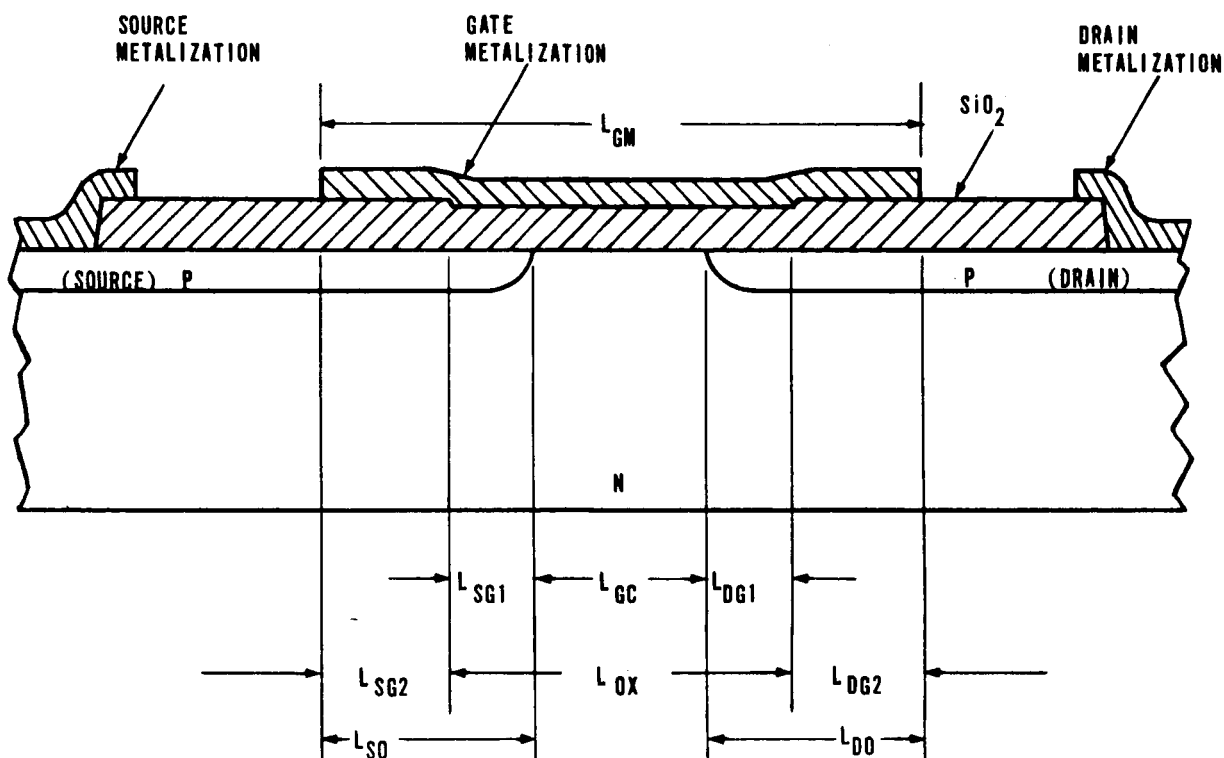
GBW, gain bandwidth product: 450 mc

1066-210A

SOURCE   GATE   DRAIN

METALIZATION

SiO_2

C_{GS} r_{GS} C_G r_{GD} C_{GD}

r_S r_C r_D

C_S C_D

BODY

FIGURE 8. CROSS-SECTIONAL SCHEMATIC DIAGRAM OF A
MOS TRANSISTOR CHIP SHOWING THE LOCATION
OF CAPACITIVE AND RESISTIVE ELEMENTS

0766-289A

L$_{GM}$ - LENGTH OF GATE METALIZATION.

L$_{OX}$ - LENGTH OF GATE OXIDE.

L$_{SG1}$ - LENGTH OF LATERAL DIFFUSION OF SOURCE UNDER GATE OXIDE.

L$_{DG1}$ - LENGTH OF LATERAL DIFFUSION OF DRAIN UNDER GATE OXIDE.

L$_{SG2}$ - LENGTH OF OVERLAP OF GATE METALIZATION OVER SOURCE OXIDE.

L$_{DG2}$ - LENGTH OF OVERLAP OF GATE METALIZATION OVER DRAIN OXIDE.

L$_{GC}$ - LENGTH OF CHANNEL.

L$_{SO}$ - LENGTH OF ENTIRE OVERLAP OF GATE METALIZATION OVER SOURCE REGION

L$_{DO}$ - LENGTH OF ENTIRE OVERLAP OF GATE METALIZATION OVER DRAIN REGION

FIGURE 9.   CROSS-SECTIONAL SCHEMATIC DIAGRAM OF
GENERAL INSTRUMENT'S MEM517A SHOWING GATE
METALIZATION OVERLAP OF SOURCE AND DRAIN

1066-208A
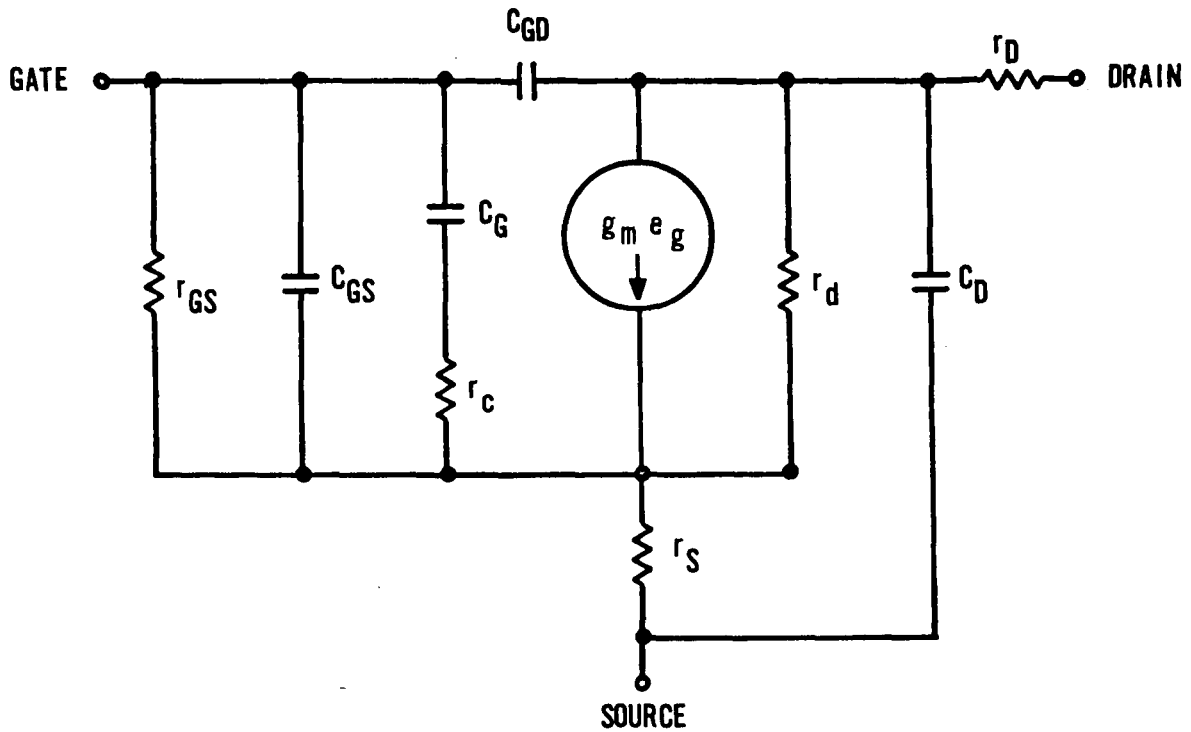
where: r_{GS} = Gate-to-Source oxide leakage resistance

C_{GS} = Gate-to-Source capacitance (includes the capacitance contributed by the extension of the gate contact region and over the body).

C_G = True Gate-to-Channel capacitance

r_c = Channel resistance

C_{GD} = Gate-to-Drain overlap capacitance

r_d = Dynamic drain resistance

r_S = Resistance of source region and ohmic contact

r_D = Resistance of drain region and ohmic contact

C_D = Drain-to-Body (or source) capacitance

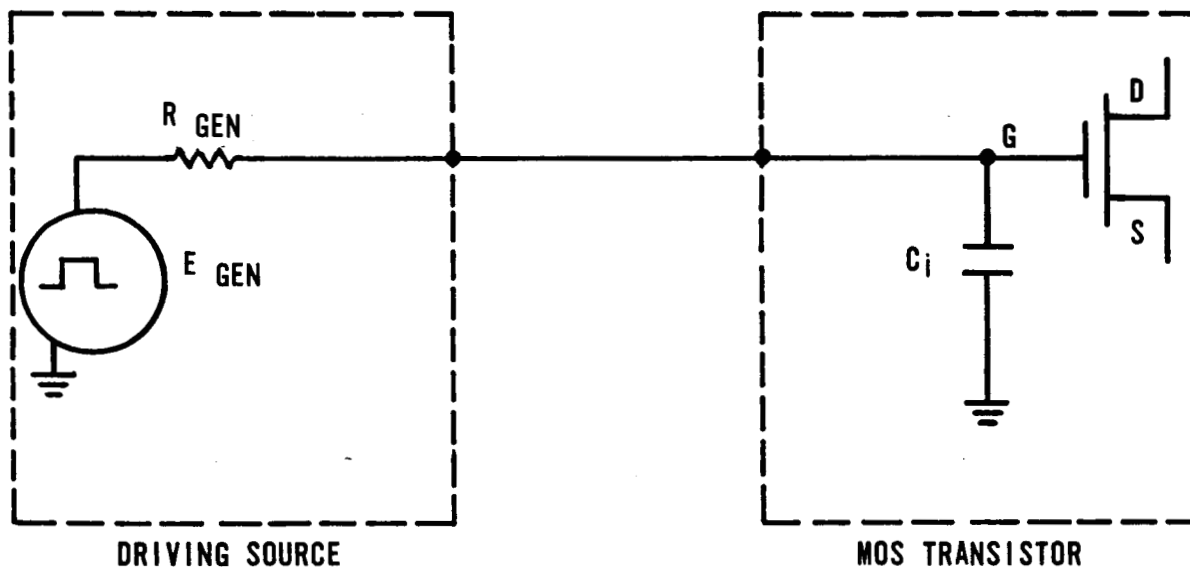FIGURE 10. EQUIVALENT CIRCUIT OF A MOS TRANSISTOR

1066-211A

FIGURE 11. COMPOSITIVE EQUIVALENT CIRCUIT OF A HIGH
CURRENT MOS TRANSISTOR AND ITS DRIVING SOURCE
IMPEDANCE USED TO DETERMINE OUTPUT
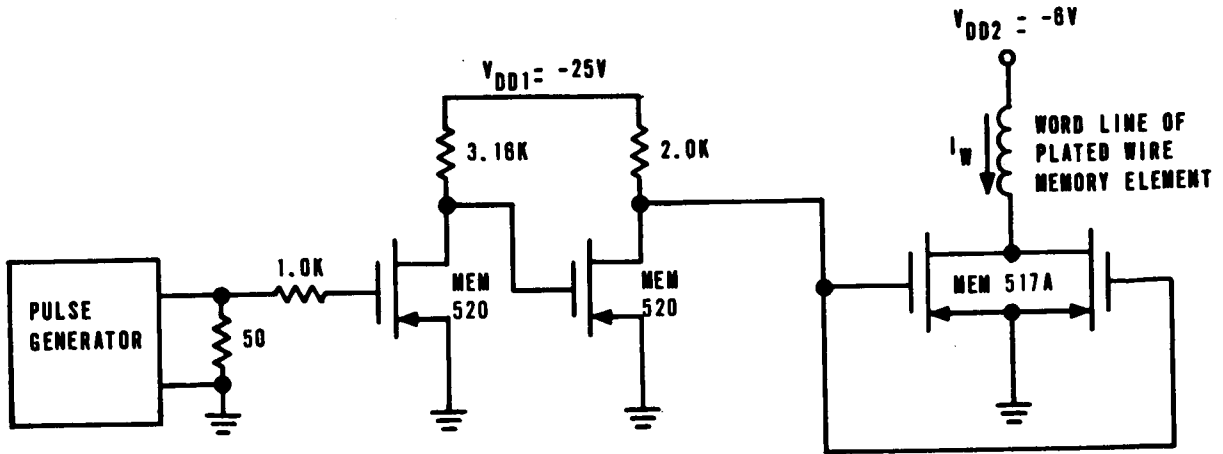CURRENT RISE AND FALL TIMES

0766-287A

FIGURE 12. SCHEMATIC DIAGRAM OF MOS TEST CIRCUIT USED
TO DRIVE THE PLATED WIRE MEMORY ELEMENT
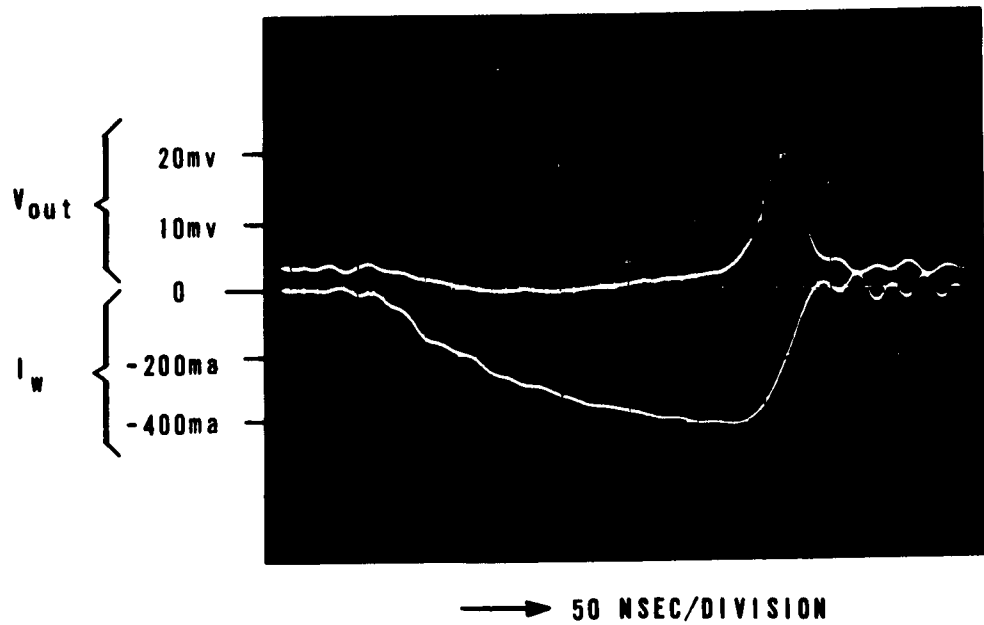

50 NSEC/DIVISION

FIGURE 13. PHOTOGRAPH OF WORD CURRENT WAVEFORM AND
SENSE VOLTAGE WAVEFORM OBTAINED WITH THE
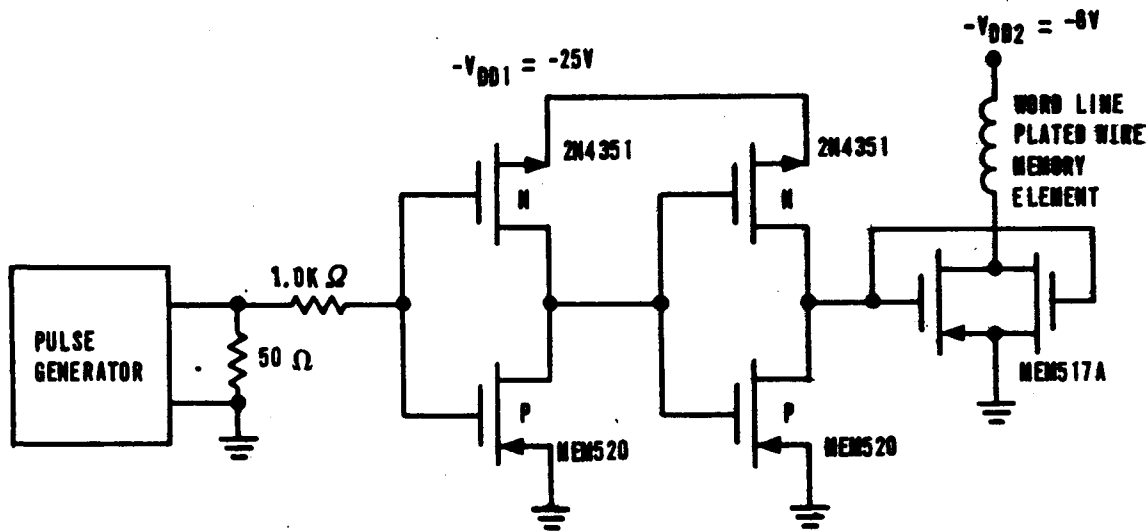ABOVE CIRCUIT

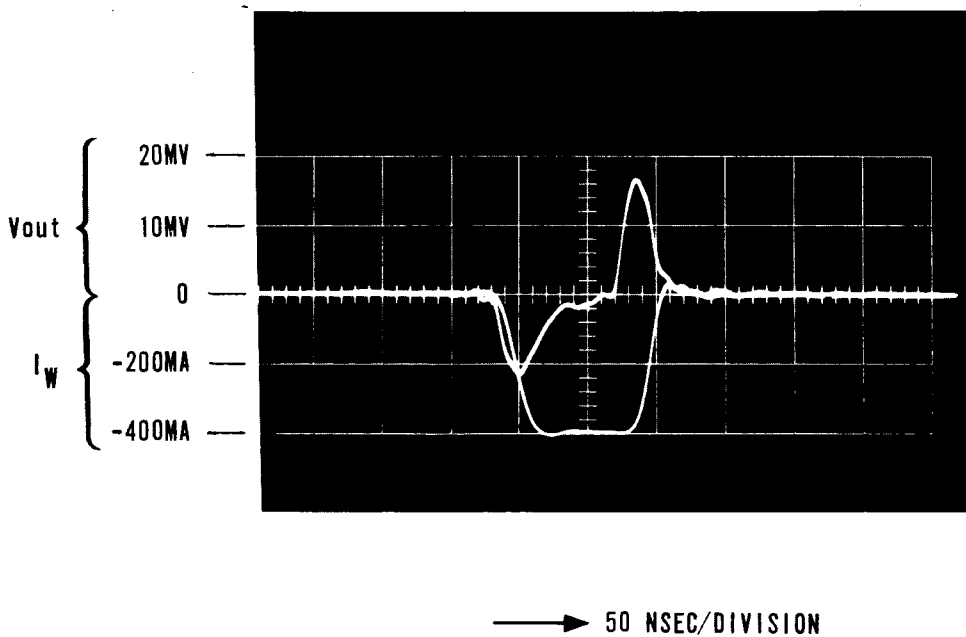FIGURE 14. SCHEMATIC DIAGRAM OF COMPLEMENTARY
MOS TRANSISTOR WORD DRIVER

50 NSEC/DIVISION

FIGURE 15. PHOTOGRAPH OF WORD CURRENT WAVEFORM
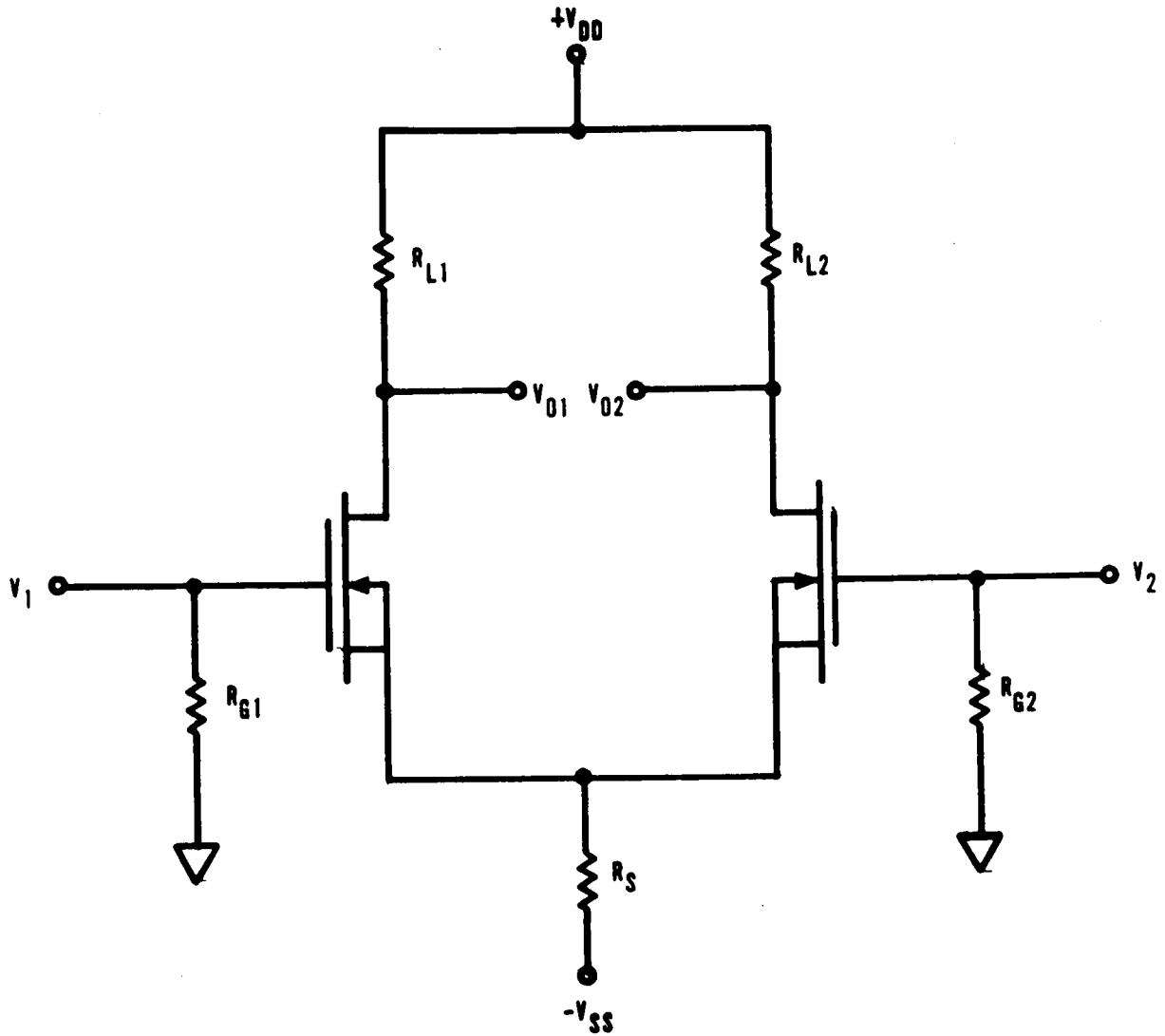AND SENSE VOLTAGE WAVEFORM OBTAINED
WITH THE ABOVE CIRCUIT
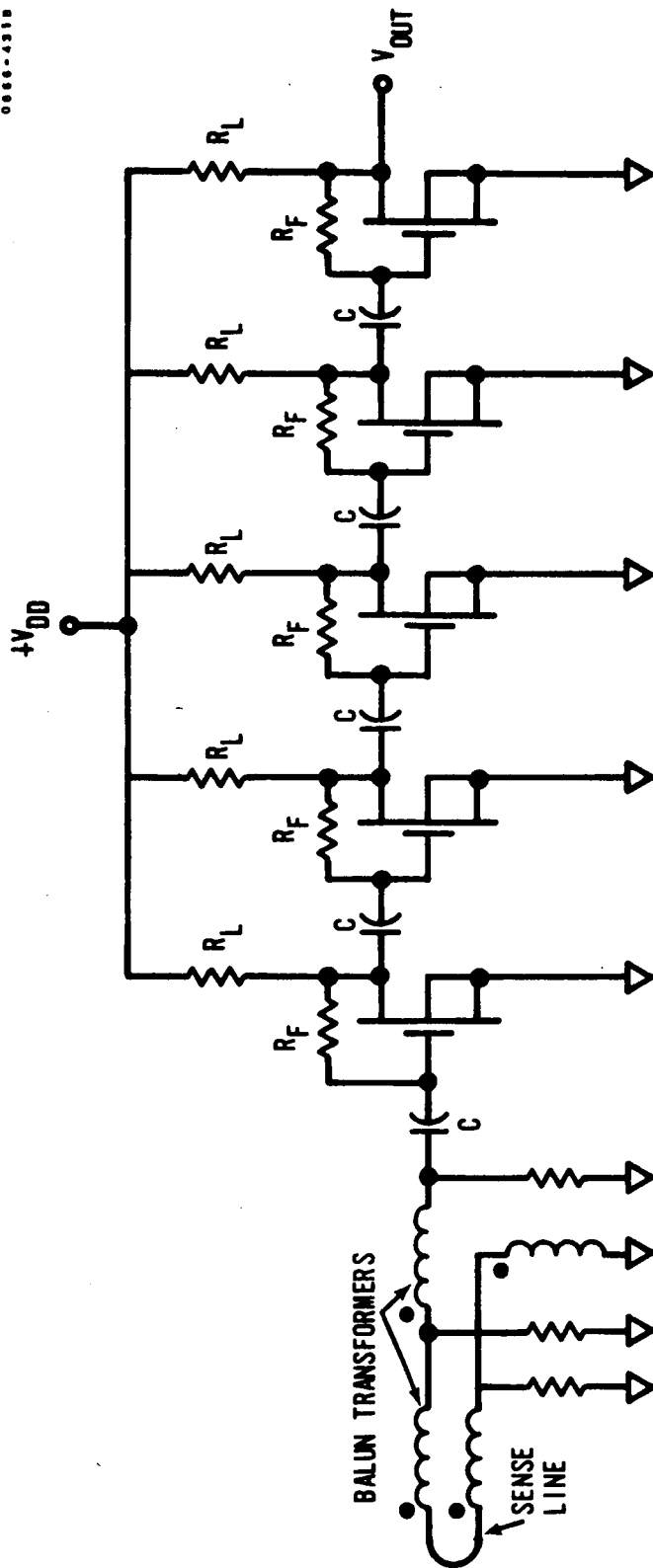
33

0066-4299

FIGURE 16.   MOST DIFFERENTIAL AMPLIFIER

FIGURE 17. AC COUPLED MOST SENSE AMPLIFIER

7.0 INTERCONNECTION OF MOST LSIs AND PLATED WIRE

Once the interconnection system has been solved at the LSI chip level, it becomes desirable to provide a compatible system of external inter-connections so that circuit continuity is provided with a minimization of metallic interfaces. The LSI interconnection system is discussed in more detail in Section 8. The technique presently being developed is compatible with an all-aluminum interconnection system.

Honeywell has developed a technique for depositing aluminum on a poly-imide, "H", film.* This development (partially funded by NADC and RADC development contracts) has proven the feasibility of using vapor-deposited aluminum conductors on a supporting polyimide film to perform this interconnection. Polyimide film is similar to Mylar in properties except it can withstand all process temperatures encountered in integrated circuit assembly. The application of this technique to the interconnection of integrated circuits is shown schematically in Figure 18. Briefly stated, the process is:

1. Evaporate the conductor onto the film.

2. Photoetch the desired interconnect pattern into the conductor metal in a manner analogous to making flexible printed circuits.

3. Bond the aluminum conductors on the film to the contact pads on the chip using thermo-compression or ultrasonic bonding.

4. Electrically test the chip/lead film assembly.

5. Package completed assembly.

6. Assemble the packaged circuits onto the anodized printed wiring board (PWB) and attach the lead film conductors to the pads on the substrate.

The use of a polyimide film as a lead support material is discussed in Section 8.

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* Manufactured by DuPont under the trade name of KAPTON.

COMPLETED FI'

66-4278

ADD GLASS-PASSIVATED SILICON CHIP

ENCAPSULATE SILICON CHIP

BONDING PADS

ALUMINUM CONDUCTORS

ASSEMBLY BONDED AND SOLDERED TO PRINTED CIRCUIT BOARD
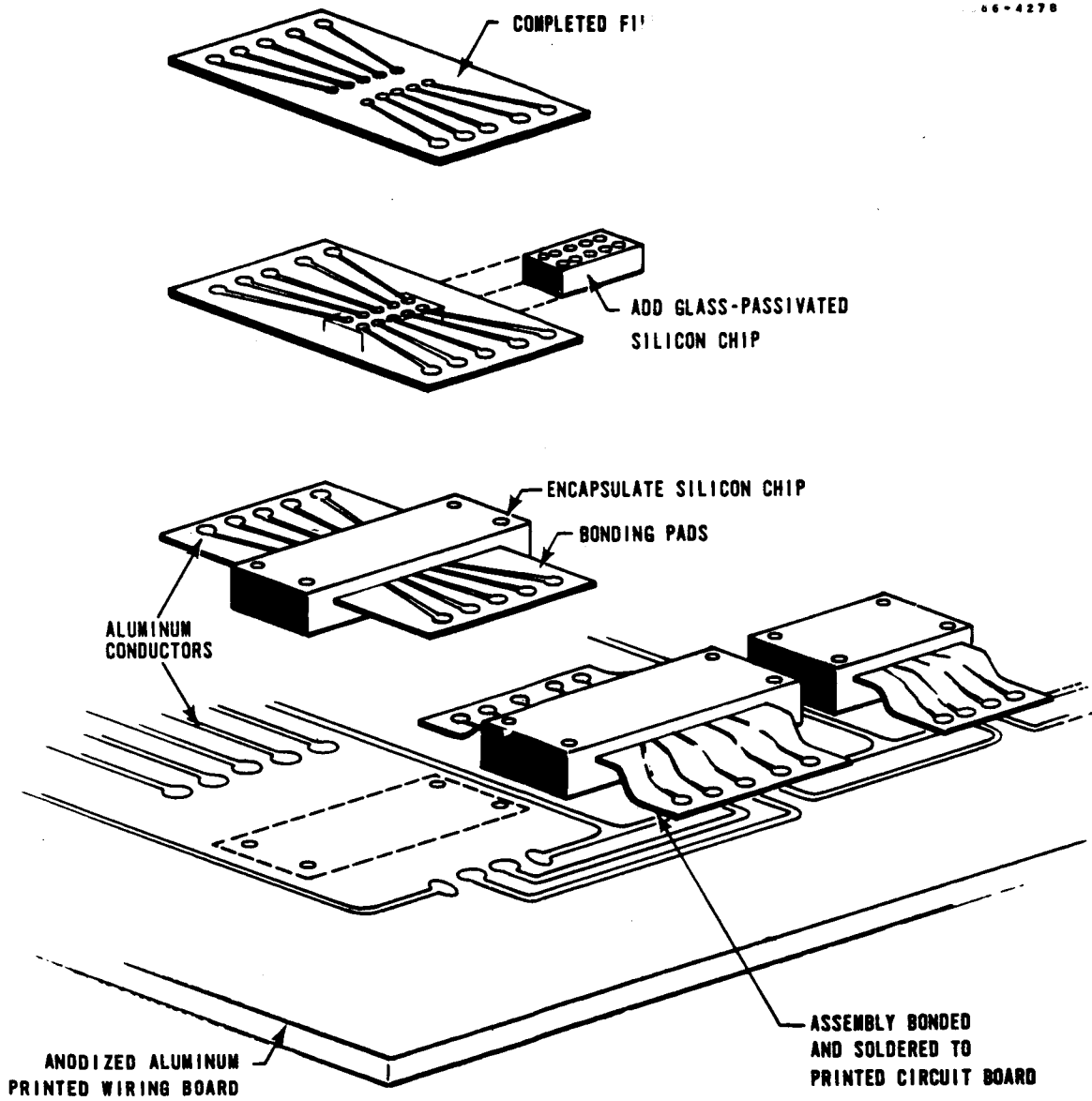
ANODIZED ALUMINUM PRINTED WIRING BOARD

FIGURE 18. MONOMETALLIC INTERCONNECTION TECHNIQUE FOR THE ELIMINATION OF CONDUCTOR INTERFACES

<u>Advantages of Film-Supported Leads</u> - The principal advantages of this technique are:

1. Elimination of flying leads gives support to leads.

2. Prepositioning of leads, eliminating alignment of each individual lead.

3. Testing before assembly is packaged will substantially reduce cost by eliminating rejects after packaging.

4. Several chips can be attached to the lead film with interconnections provided between chips as well as for external connections. Circuit crossovers are the major limitation on the number of chips that can be attached within a single package.

5. The film supported leads along with an anodized aluminum printed wiring board provide a completely monometallic interconnection system.

A plated wire memory plane can be assembled in the same manner as shown in Figure 18. Sufficient space may be allotted on the printed wiring board for the placement of the plated wires and word straps. All the LSIs required for the operation of a single plane can be mounted alongside the memory devices. The interconnection of the LSIs is provided by thin film aluminum conductors which have been deposited on the anodized surface of the aluminum plate. By plating the ends of the memory wires and word straps with a thin film of aluminum, an aluminum-to-aluminum bond can be made between the memory wires and the PWB. Therefore the interconnections between the MOST LSIs and the memory wires is performed by a system completely free of bimetallic interfaces.

8.0 TOTAL REDUCTION OF INTERFACES AND INTERFACE CONNECTIONS

The reduction of interfaces within the memory system envolves all of the following areas:

1. The circuit organization and layout

2. The interconnection of MOS devices within a single chip

3.   The circuit package

4.   The interconnection of MOS circuitry and the plated wire stack.

The first three areas are discussed in this section of the report and the fourth area is discussed in Section 7.

8.1   CIRCUIT ORGANIZATION AND LAYOUT

The area allowing the most progress toward the reduction of interfaces is the circuit organization and chip layout. Each MOS chip should contain as much circuitry as practical, being limited only by power dissipation and/or pinouts. The word driver selection circuitry is used to describe how interfaces and interconnections can be reduced at the chip level. The complete address selection circuitry (including address register, decoding logic, word drivers, and clock circuits) for 16 words is shown schematically in Figures 19 and 20. The selection circuitry can be expanded to 32 or 64 words by utilizing larger area chips. The circuit is constructed entirely of P channel MOSTs, all contained within the same silicon chip. The address decoding is mechanized with both series logic and parallel logic. The series decoding logic is illustrated in Figure 19 where the four MOSTs associated with each address are connected in series. The parallel decoding logic is illustrated in Figure 20 where the four MOSTs are connected in parallel. The series decoding has the advantage of requiring fewer MOSTs and less chip area for its implementation.

The four-stage address register has been included as part of the selection circuitry for two reasons: (1) the total number of conductors into the memory stack is reduced considerably and as a result the number of interfaces and interconnections is reduced, (2) the drive requirements imposed upon the address register are reduced considerably. A memory plane will contain one of these modules for each 16 words and only one wire for each address bit will be wired into the plane instead of one wire per word, hence reducing interconnections considerably. An additional logic signal will be required to select the proper module and this signal is coupled into the "Module Select/Read Pulse" circuit.

The decoding logic will be relatively slow due to the high impedance of the MOSTs used (the higher impedance MOSTs require less chip area), hence the turn-on time of the output word driver would be much greater

than the required 50 nanoseconds. The 50 nanosecond current fall time is accomplished by the use of a high speed Read pulse which is gated with the decoding logic and the module select signal to turn the word driver off.

The first approximation to the chip size for a 16-word function is shown in Figure 21. Each small block indicates the area required for the respective circuit. It appears entirely feasible that the complete selection circuitry could be contained on a chip 190 mils by 225 mils. A chip of this size can be produced with reasonable yields in the not too distant future. The larger area chips required for 32 and 64 words should become practical within the next two years.

The decoding logic was laid out into more detail as shown in Figures 22 and 23. The individual MOSTs are shown along with the address signal lines. The layout is not drawn to scale and is used for illustration only. It can be seen that the decoding logic can be mechanized with no crossovers, which reduces potential interfaces within the chip.

## 8.2 REDUCTION OF MOST INTERFACES

The advent of large scale integration (LSI) allows complete functions to be contained within a single chip. Chips containing 1,000 to 2,000 logic type MOS devices become feasible. This reduces the number of interconnections significantly. For example, consider the selection circuitry for 16 words shown in Figure 19. To implement this with normal integrated circuits would require approximately 23 flat-packs of 14 leads each. Fabrication of the complete circuit within a single chip reduces the number of external leads from 182 (for the 23 flat-packs) to 30 for the LSI version, which amounts to a reduction of approximately 85 percent. Increasing the complexity from 16 words to 32 words would allow an even greater reduction. The intraconnections within a device of this complexity is accomplished by a combination of:

Common diffused drain and source regions.

Diffused crossovers (crossunders or tunnels).

Multilayer interconnections on the passivated surface of the chip.
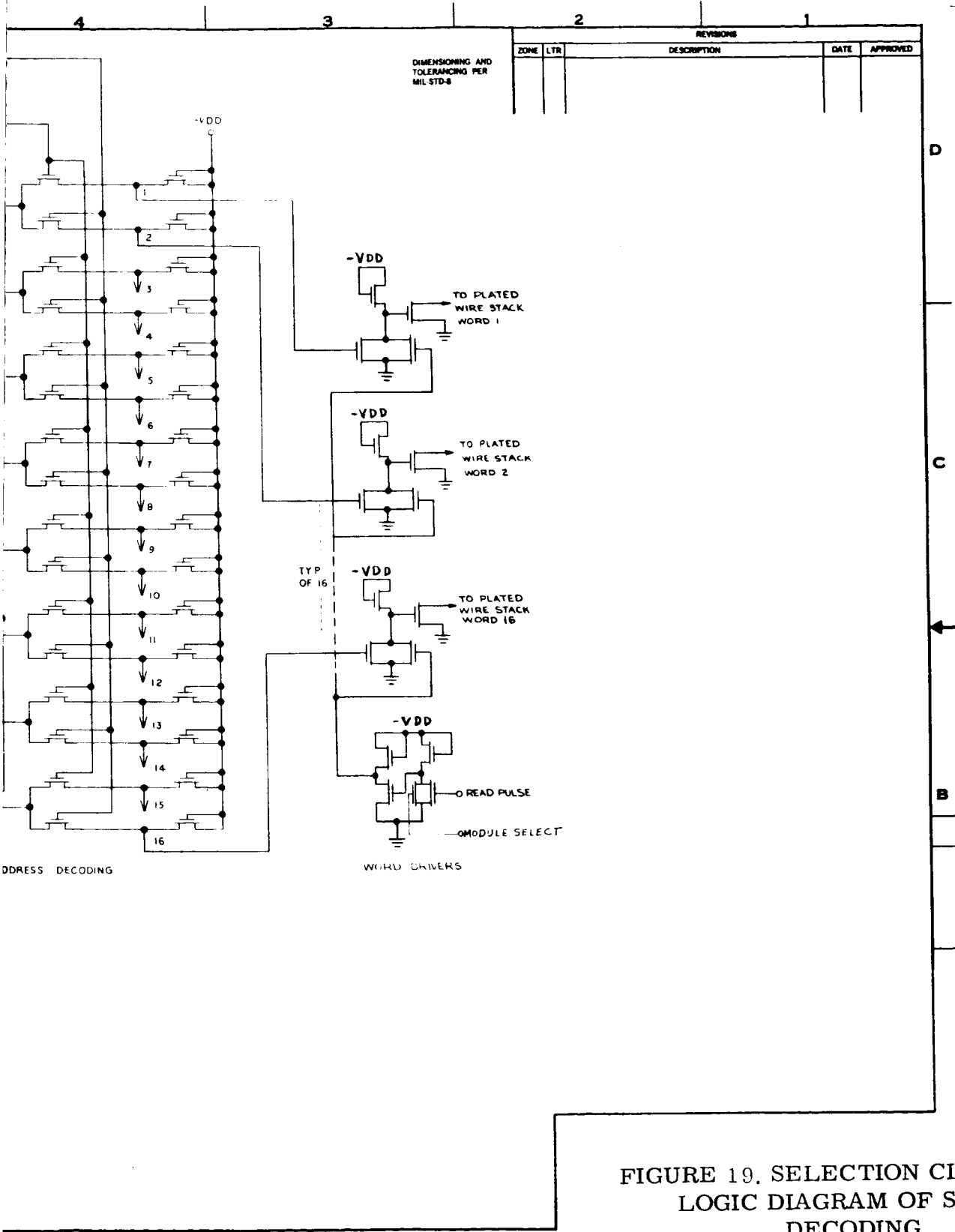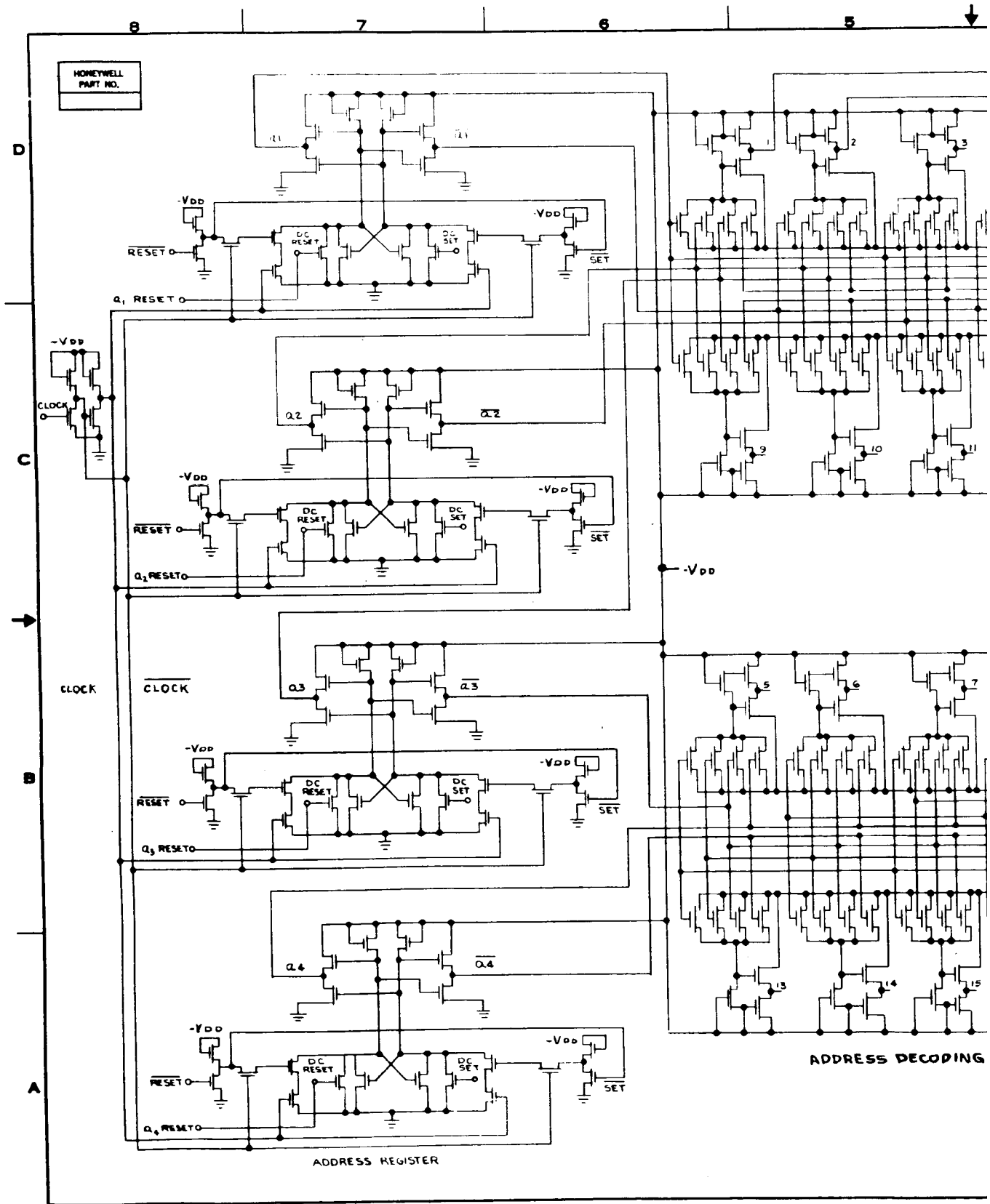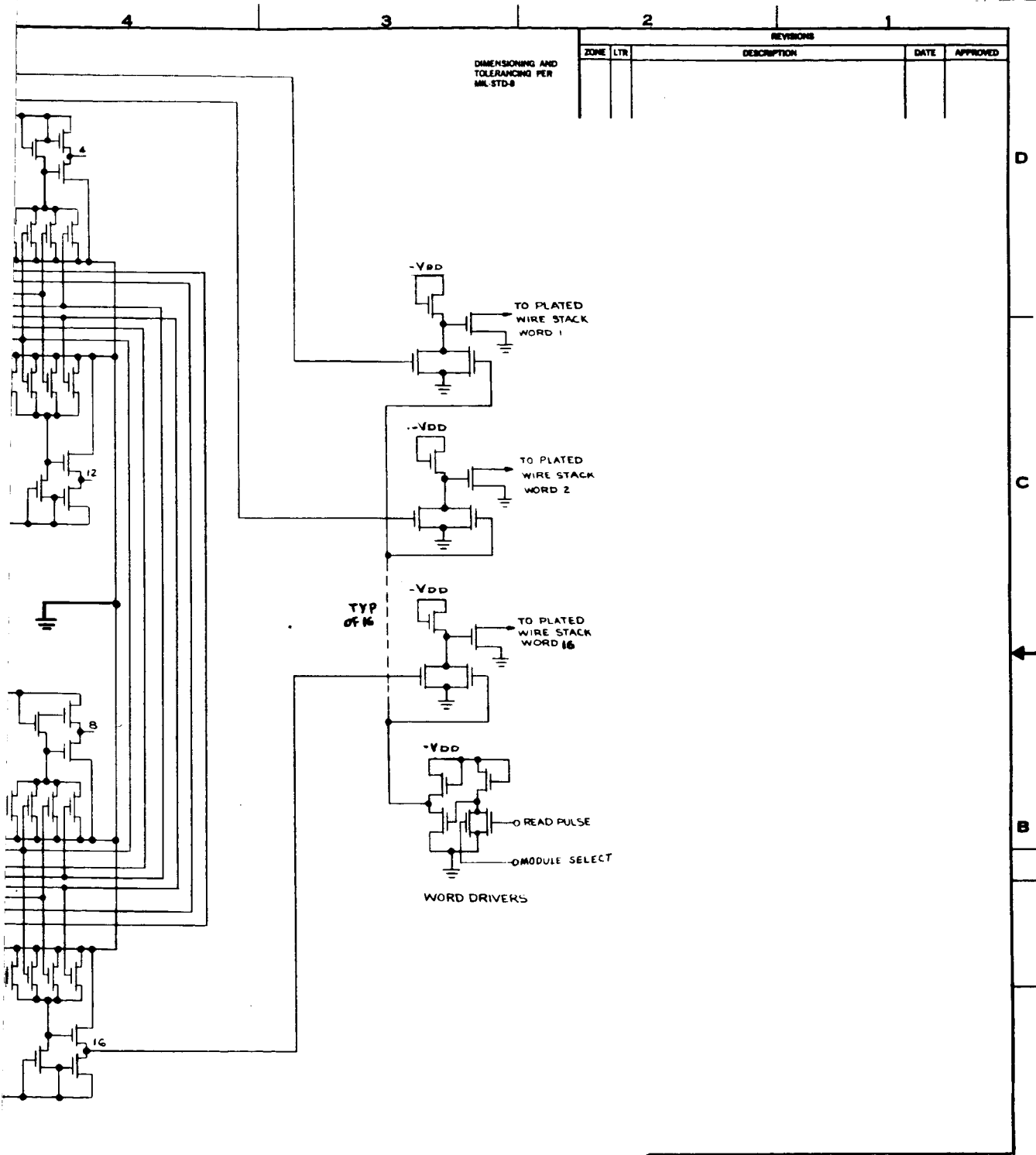
These are discussed in the following paragraphs.

ADDRESS REGISTER
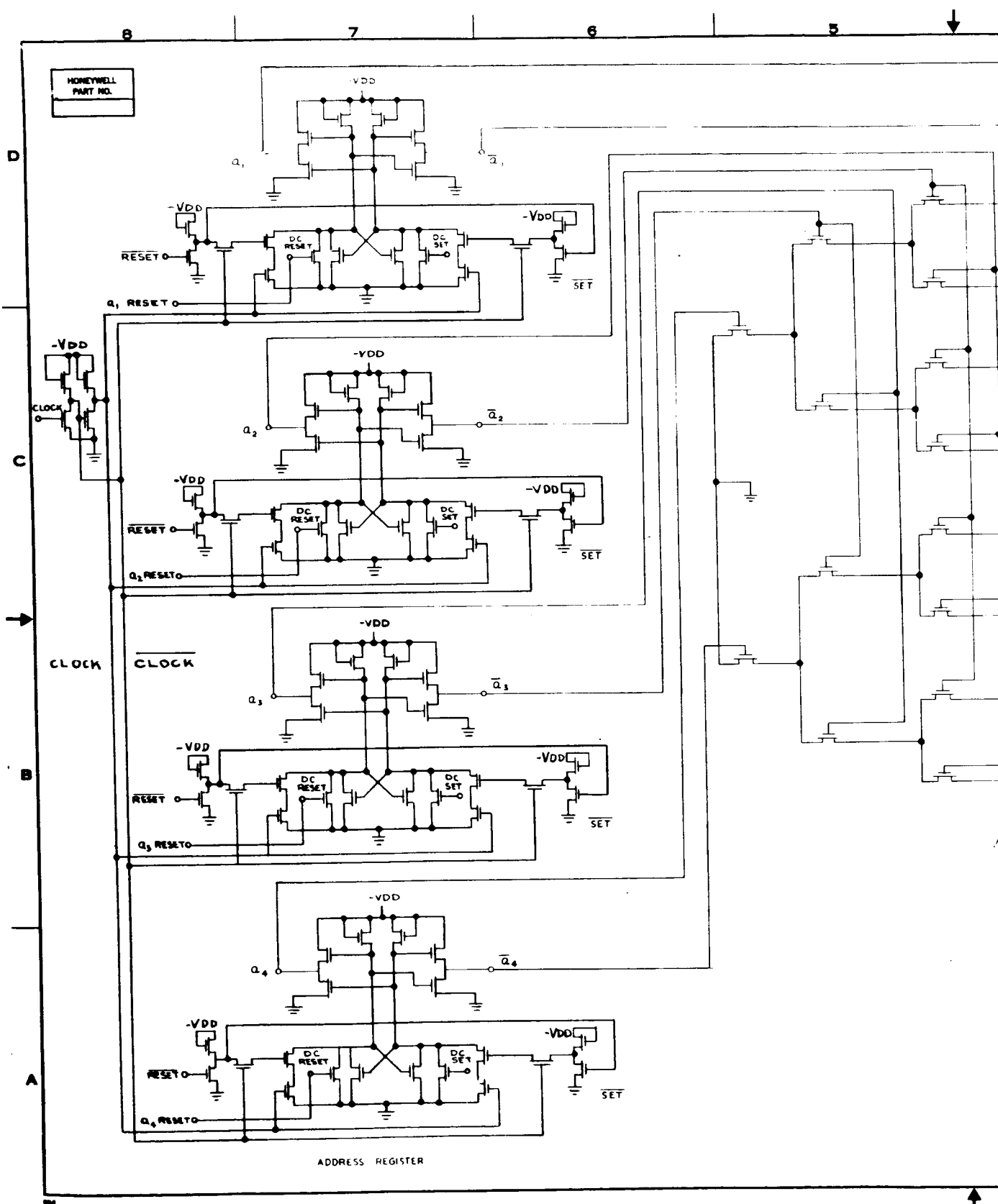
FIGURE 19. SELECTION CIRCUITRY -
LOGIC DIAGRAM OF SERIES
DECODING

ADDRESS REGISTER

ADDRESS DECODING

FIGURE 20. SELECTION CIRCUITRY -
LOGIC DIAGRAM OF PARALLEL
DECODING

0886-4248

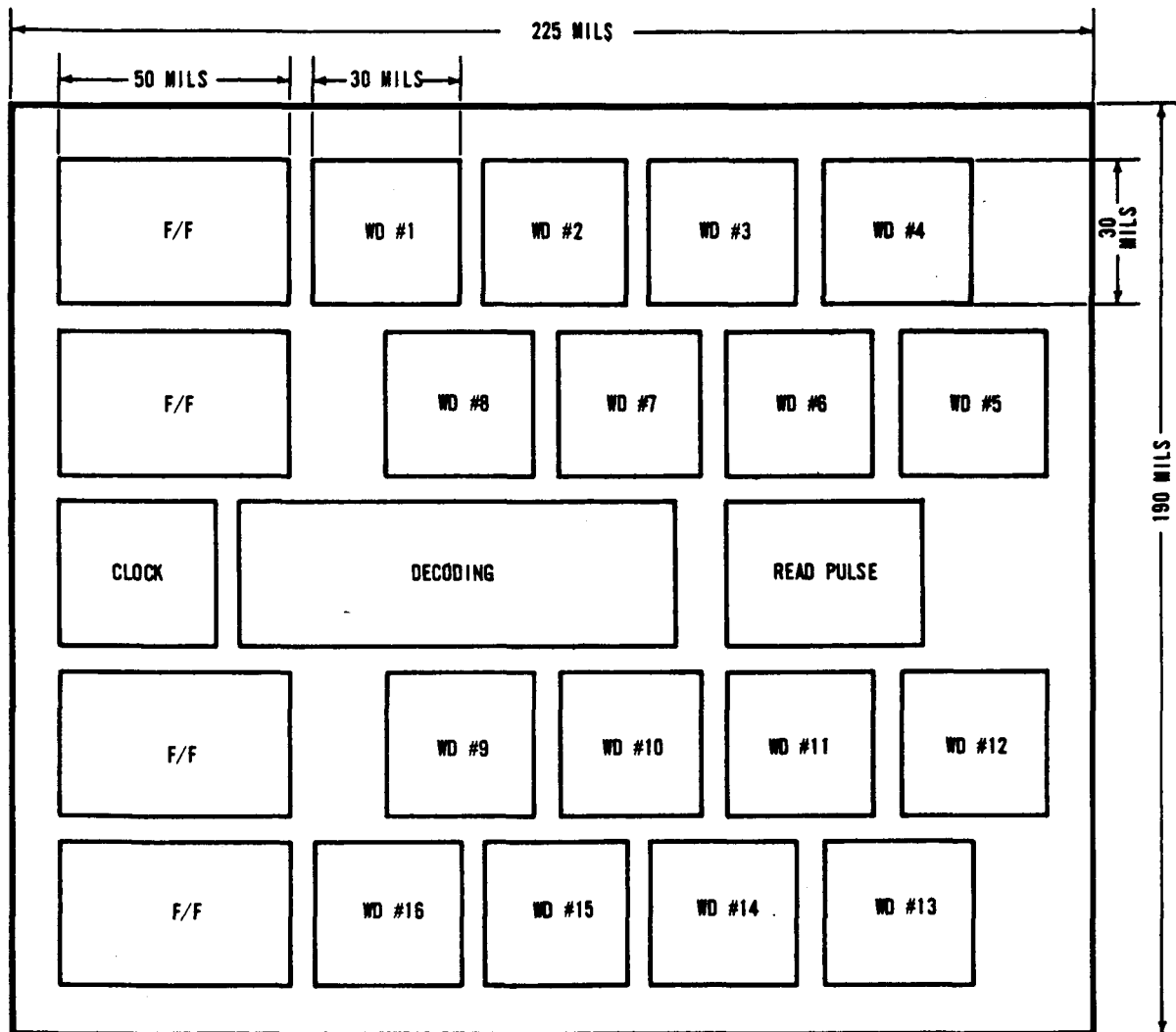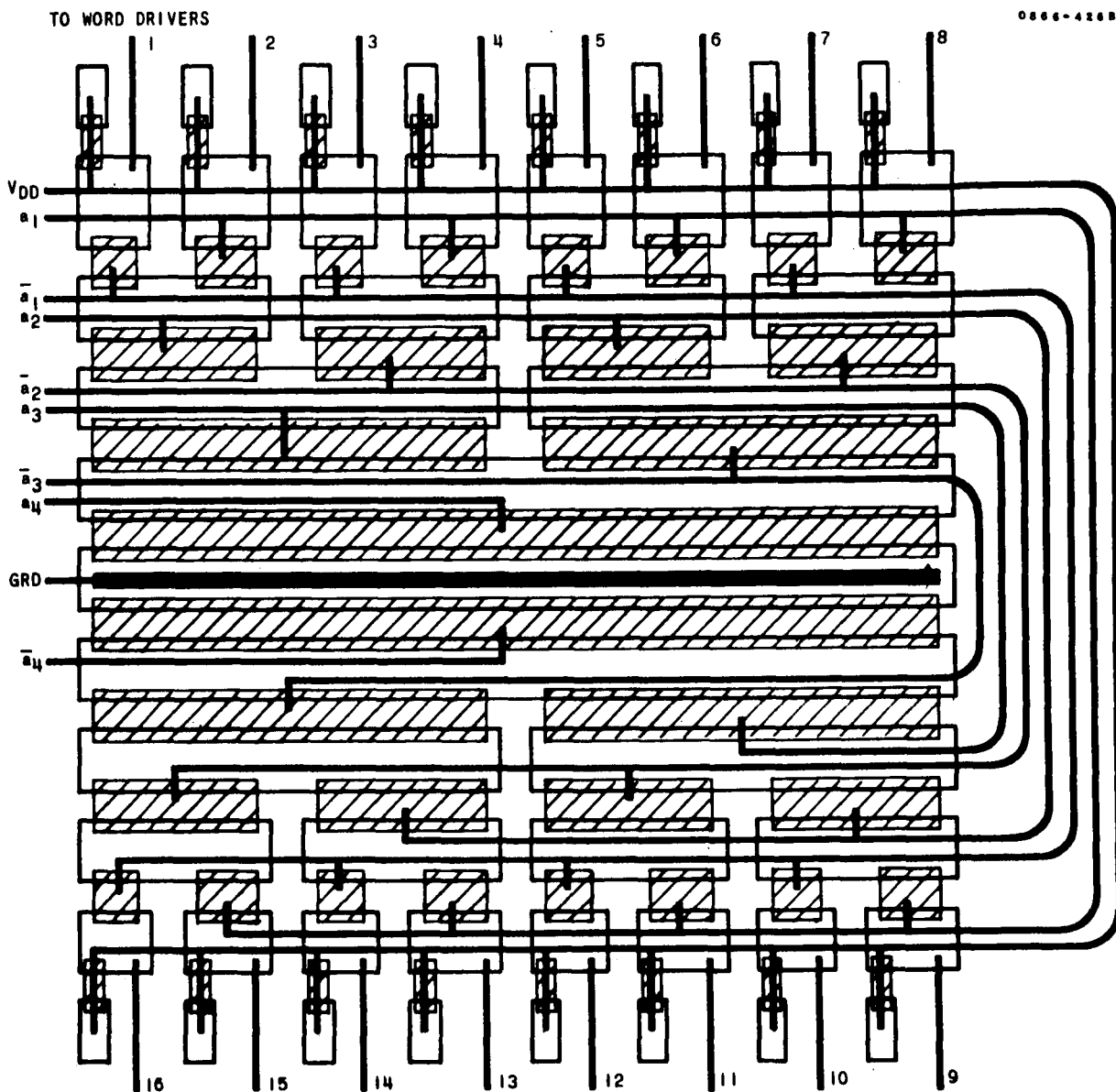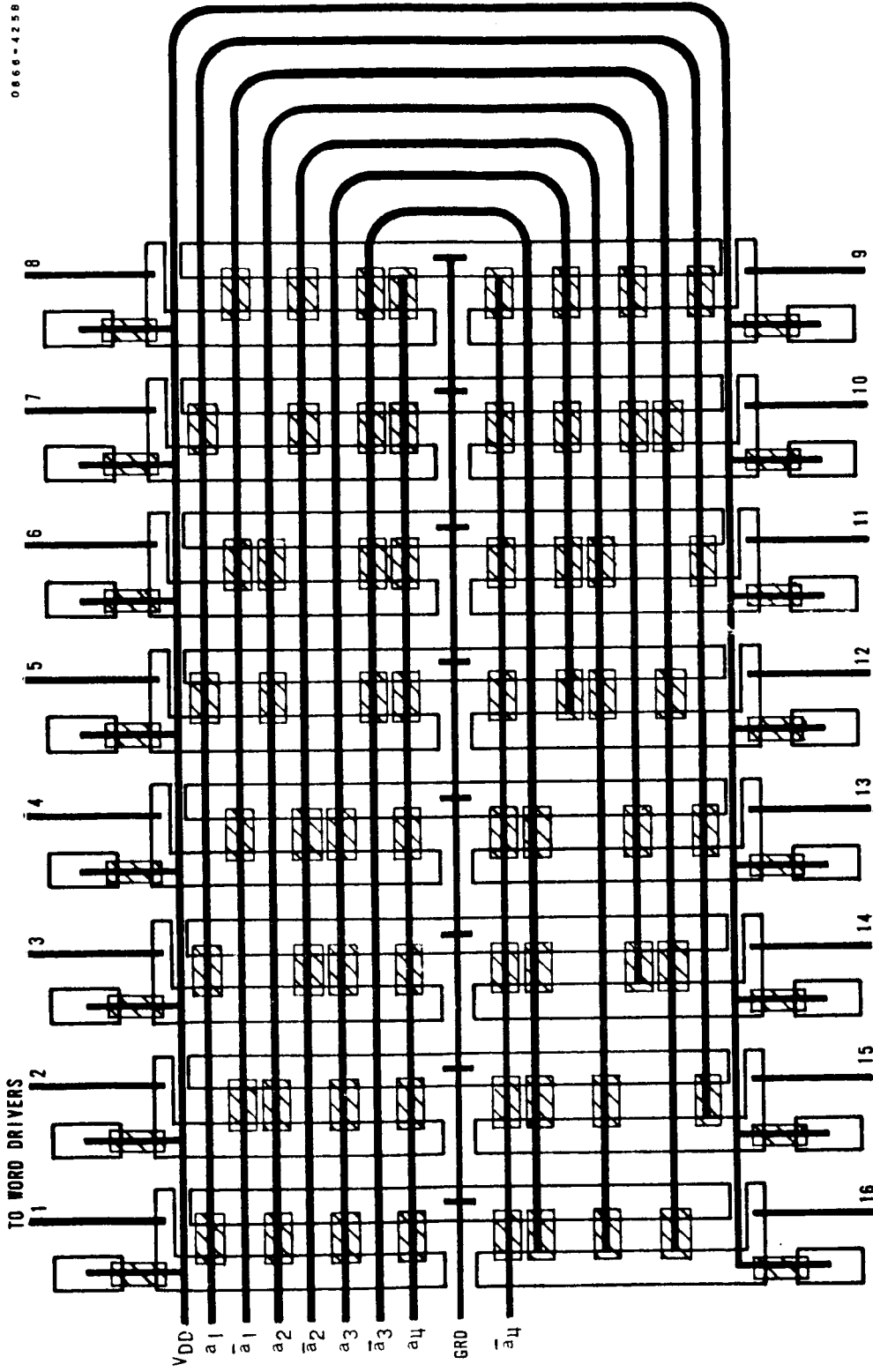
FIGURE 21. SELECTION CIRCUIT CHIP - 16 WORDS

FIGURE 22. CHIP LAYOUT OF FOUR-BIT SERIES DECODING

FIGURE 23. CHIP LAYOUT OF FOUR-BIT PARALLEL DECODING

47

Common Diffused Regions. The MOSTs within the same logic gate may be interconnected by a common diffused region. This is illustrated in Figure 24a where the drain of Q_4 and the source of Q_3 are contained within the same diffused region. This is also true of the drain and source of Q_3 and Q_2 and the drain and source of Q_2 and Q_1. This same figure compares the number of metal-to-silicon interfaces contained in a MOST integrated circuit chip to that of a similar bipolar chip (Figure 24b). There are three metal-to-silicon interfaces in the MOST chip and 18 in the bipolar chip. This is a significant reduction.

Diffused Crossovers. These are sometimes referred to as "crossunders" or "tunnels". In even the simplest integrated circuit it is not always possible to eliminate crossovers. This can be provided by a high concentration diffused region as illustrated in Figure 25. Two conductors, "a" and "b" must cross each other. A P-type isolated region is diffused in the chip during the source and drain diffusion. Contact windows are opened over the left-hand and right-hand sides of the P region in the SiO_2. Circuit continuity for conductor "a" is provided by the diffused P region, hence a "tunnel" is formed. Conductor "b" crosses over the P region as shown and the insulation between "a" and "b" is provided by a thin layer of SiO_2.

The disadvantages of the diffused crossover are increased series resistance and increased stray capacitance. The sheet resistance of a typical source and drain diffusion varies from approximately 100 to 200 ohms per square. This can be reduced to less than 10 ohms per square by an additional P+ diffusion step. The stray capacitance is contributed by the junction capacitance between the P region and the N type substrate. Both of these components tend to reduce circuit speed and increase power dissipation.

Multilayer Interconnections. As the circuit complexity of the chip increases all crossovers cannot be made with the above techniques. More than a single layer of crossovers is required. The interconnections within an LSI are comparable to those of present day multilayer boards. It then becomes necessary to develop a microminiature version of multilayer interconnections which can be deposited on the semiconductor surface and made an integral part of the completed circuit. This required a highly compatible system of metals and insulators.
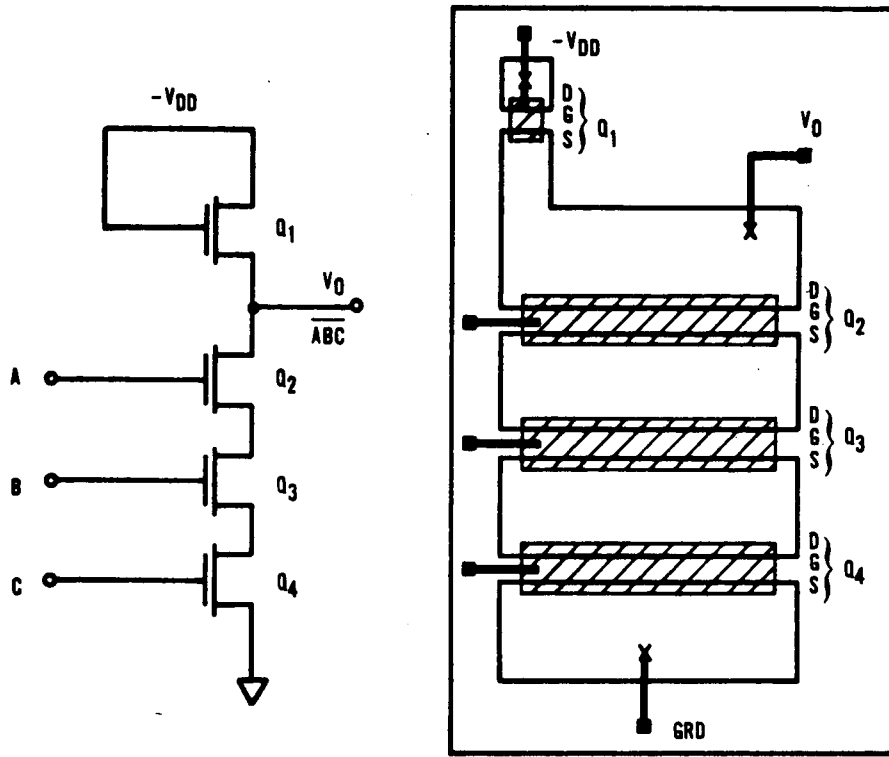
(a) MOST 3-INPUT NAND GATE
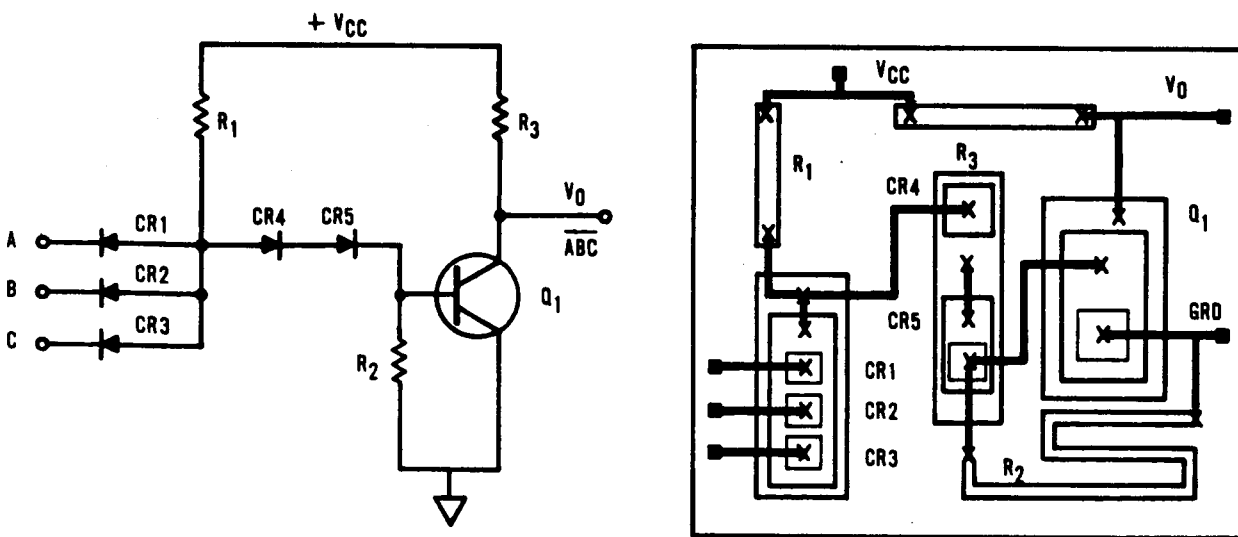
(b) BIPOLAR 3-INPUT NAND GATE

FIGURE 24. A 3-INPUT NAND GATE CONSTRUCTED WITH
BOTH BIPOLAR DEVICES AND MOS DEVICES. (THE METAL-
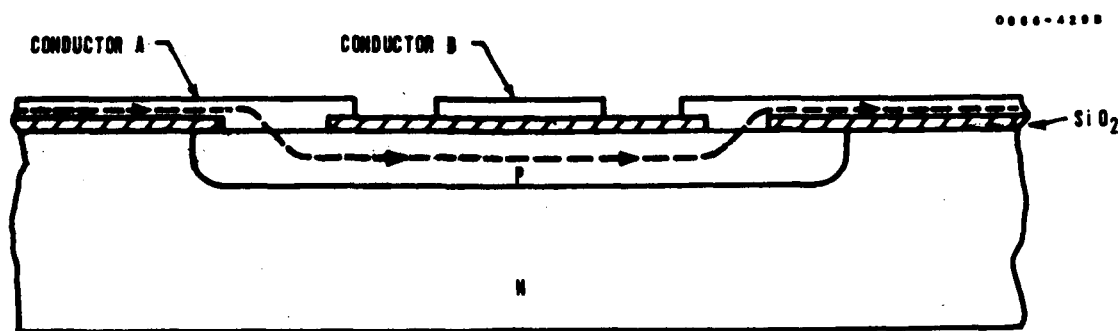TO-SILICON CONTACTS ARE MARKED WITH AN "X".)

FIGURE 25. CROSS-SECTION OF A SILICON MOST CHIP
SHOWING THE DIFFUSED CROSSOVER TECHNIQUE

The problems associated with utilizing the bimetallic system of gold and
aluminum in the interconnection and packaging of transistors and inte-
grated circuits has compelled the industry to develop monometallic
systems. A monometallic system becomes even more desirable in the
development of multiple layers of conductors on the surface of the silicon
chip. The two most practical monometallic systems are all-aluminum
and all-gold.

Both of these systems are presently being successfully used by the semi-
conductor industry in the fabrication of transistors and integrated circuits.
The following paragraphs discuss some of the properties of the above
systems and some of the methods for providing insulation between con-
ductor layers.

Aluminum has the advantages of adhering well to silicon and silicon
dioxide. It is easily evaporated to form a wide range of layer thicknesses;
it is a good electrical conductor. It is easily etched with conventional
photoresist techniques. It can be bonded by either wedge thermocompres-
sion bonding or ultrasonic bonding, and is fairly corrosion resistant. [9]
Aluminum also has some shortcomings. A thin layer of oxide rapidly
forms on the surface of the aluminum conductor and this requires the
bonding process to be very precisely established and controlled to obtain
strong bonds between the aluminum film and the aluminum wire. Alum-
inum requires a completely hermetically sealed package since continued
exposure to air, moisture, and other contaminants causes a gradual
deterioration of the bonds and thin film conductors. It reacts with the
silicon dioxide surface to create inversion layers in the underlying
silicon which could be a problem in MOS devices. (The thickness of the
SiO_2 layer can normally be made thick enough so that the inversion
effects are negligible.)

Gold has the advantages of being completely corrosion resistant, it is easily bonded by thermocompression techniques; it is easily evaporated or sputtered, it is a good electrical conductor; and it is easily etched. [9] Gold, too, has its shortcomings. It does not adhere well to SiO_2 and it reacts with silicon at the eutectic temperature of 370° C. These two problems make it necessary to have an underlying metal layer between the gold and/or silicon and silicon dioxide. Molybdenum and chromium are the two most practical choices. Either one forms a compatible system with gold and silicon. The gold system, using molybdenum as the underlying metal, is fabricated as follows. Molybdenum is deposited on the semiconductor surface by either electron beam evaporation or sputtering. Contact to the silicon is provided in those areas where openings have been opened in the silicon dioxide. Gold is next evaporated over the surface, making good contact with the previous layer of molybdenum. The interconnection pattern is formed by using conventional photoresist techniques and a two step etching process.

The gold interconnect system is presently being pursued for use in LSI circuitry requiring more than a single layer of conductors.

Types of insulating layers investigated and being pursued consist of both organic and inorganic materials. Specifically, they are photoresist, lead monoxide, and silicon monoxide.*

A limited amount of work was performed to determine the feasibility of using photoresist as an insulting medium. A three to four micron film of KTFR was applied to a standard metallized wafer and exposed without a mask. The coated wafer was vacuum baked at 250° C and then 20,000 Å of aluminum was evaporated over the surface. The completed wafer was stored at high temperature to determine if the photoresist would provide insulation between the aluminum layer on top and the metallized devices below. After three days at 300° C, the insulation was still good. The temperature was increased to 325° C, and at the end of 13 days short circuits began to appear as a result of the decomposition of the photoresist. The results indicate that multilayer conductors using photoresists for insulation are probably feasible at lower temperatures and thicker insulating films.

The effort to use lead monoxide (PbO) as the insulating medium was terminated because all of the etchants used to etch the aluminum conductors also attacked the PbO. Aluminum conductors were used in the above investigation because the process for the gold interconnection system has not been completely established.

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* This effort was supported by funds available under a separate contract.

The present multilayer interconnection system being developed consists of SiO as the insulating medium and gold as the conductors with chromium or molybdenum as the underlying metal. The development is in such an early stage that no conclusive results are available, but there are no apparent reasons that the system cannot be perfected.

8.3 AN INTERFACE-FREE PACKAGING CONCEPT

Introduction

A concept for the reduction of interface connections has been conceived and investigated. The concept was implemented in the form of a molecular integrated circuit package (MICPAK) which will interconnect many discrete integrated circuit elements on a single substrate without introducing undesirable interfaces normally found in more conventional packaging. *

In electronic circuit design, two dissimilar packaging interconnection problems are evidenced by digital and analog circuits. In digital circuitry the power requirements are usually low, but the quantity and complexity of interconnection systems can be very large.

Analog circuitry, however, frequently dissipates relatively large amounts of power and presents problems in feedback and shielding, while having straightforward simple interconnection systems.

In the MICPAK concept both of these areas are adequately considered. The substrate is designed with a built-in, low resistivity ground plane over which are routed the electrical circuit conductors formed by conventional photoetch techniques used in the semiconductor industry. This approach provides a comparable technology at the subsystem level to that previously provided at the device components level. The conductor lead inductance, capacitance to ground, resistance, etc., can be optimized for each specific conductor in the circuit.

The material used for the substrate is a high density magnesium oxide which has a layer of metal fused to it to form a ground plane and input/output termination pads. Over this metal film is deposited a dielectric film of silicon monoxide which serves to insulate the subsequent interconnection plane from the ground plane.

Processing of the various planes involved is accomplished by means of photoetching techniques similar to those of the semiconductor industry. A layout is made from which a graphic art drawing is cut to a high degree of precision. This graphic art work is made 50 to 100 times scale and reduced to photo emulsion on a glass plate. Figures 26 through 28 show the substrate, SiO and conductor layout drawings. The conductor plane

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A6604-69

.700

A

.0005-.0020 THK METAL

A

.950

.010±.002 R
16 PLACES

CHANNEL
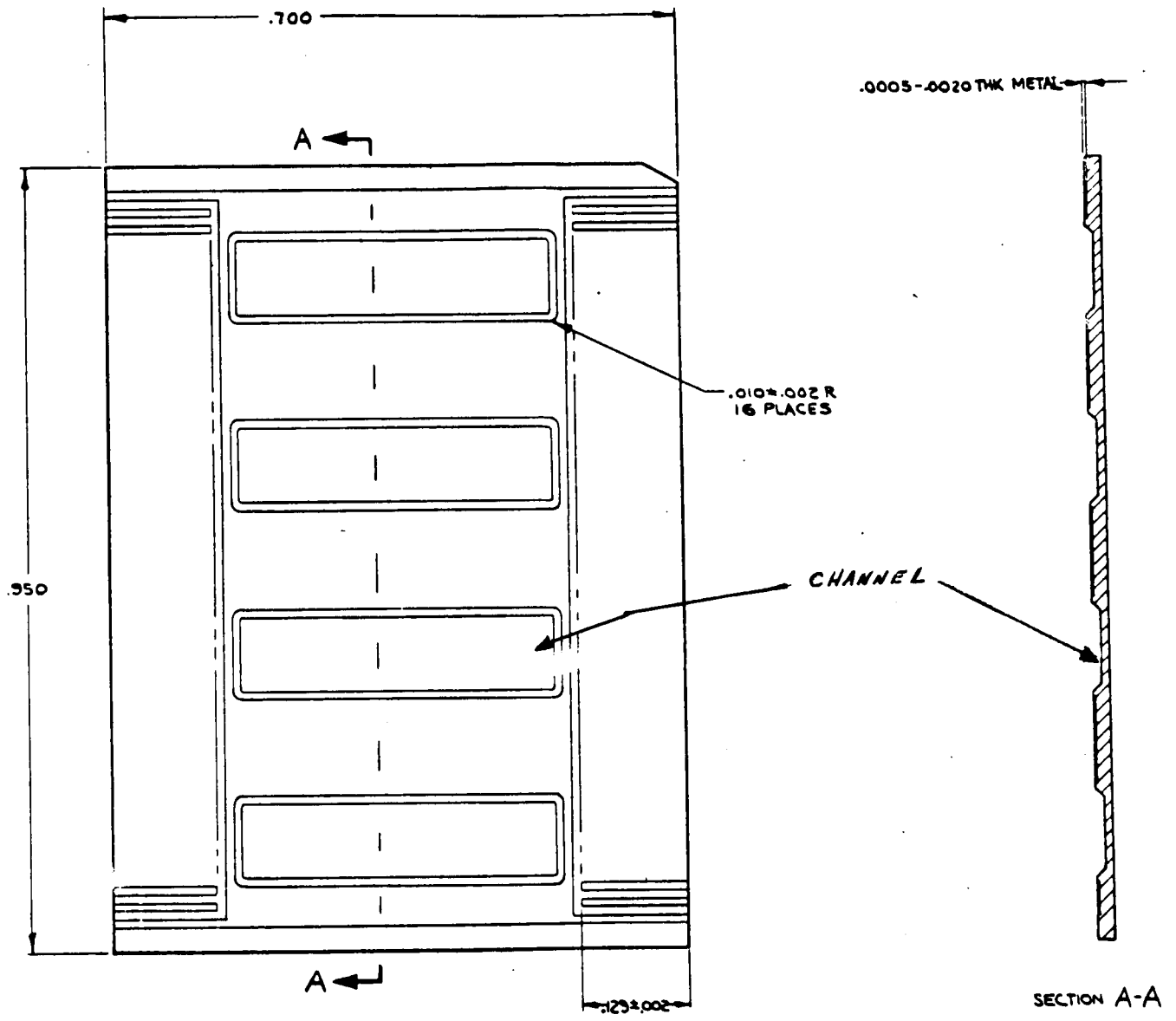
.129±.002

SECTION A-A

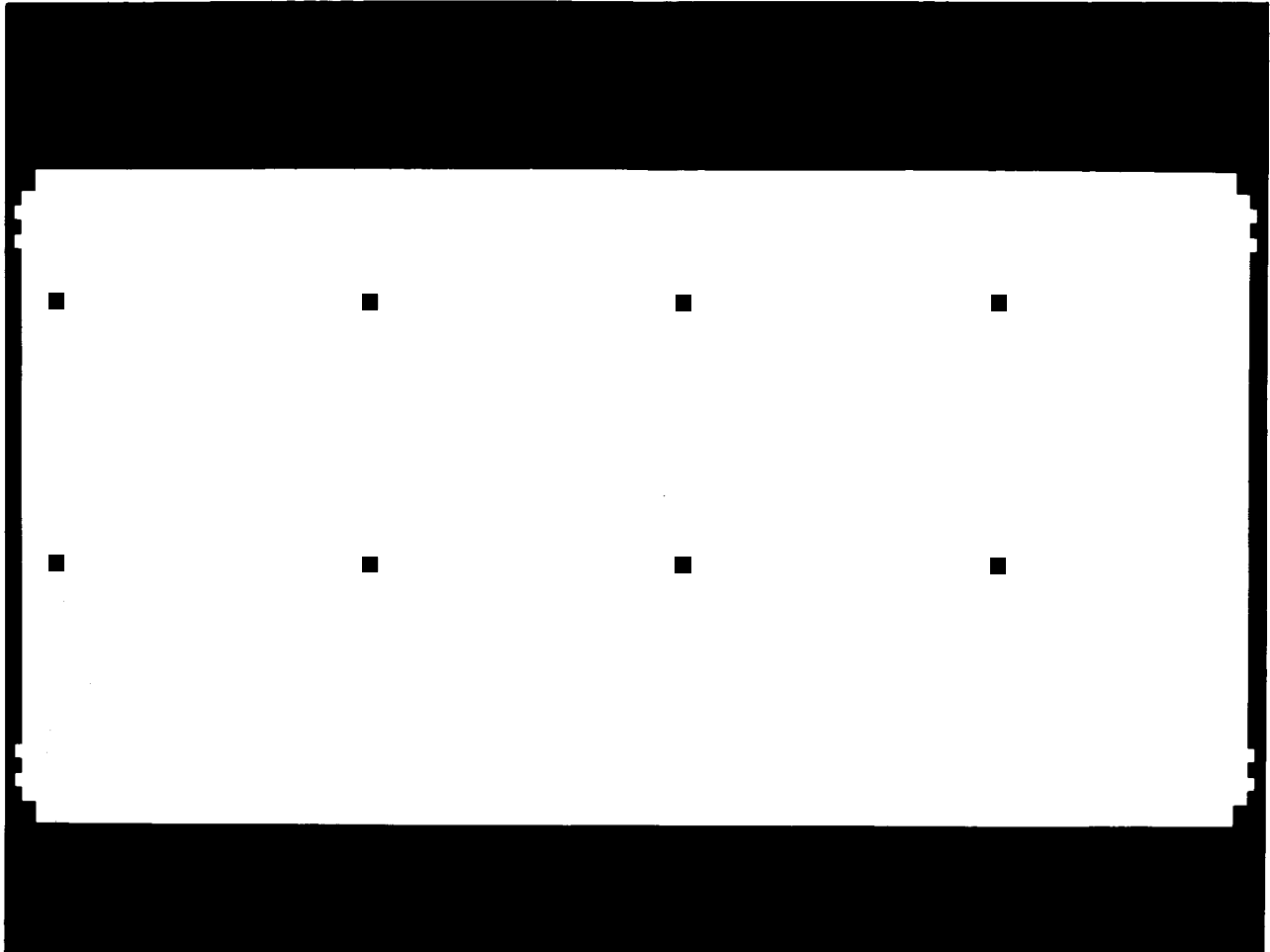FIGURE 26. SUBSTRATE SKETCH

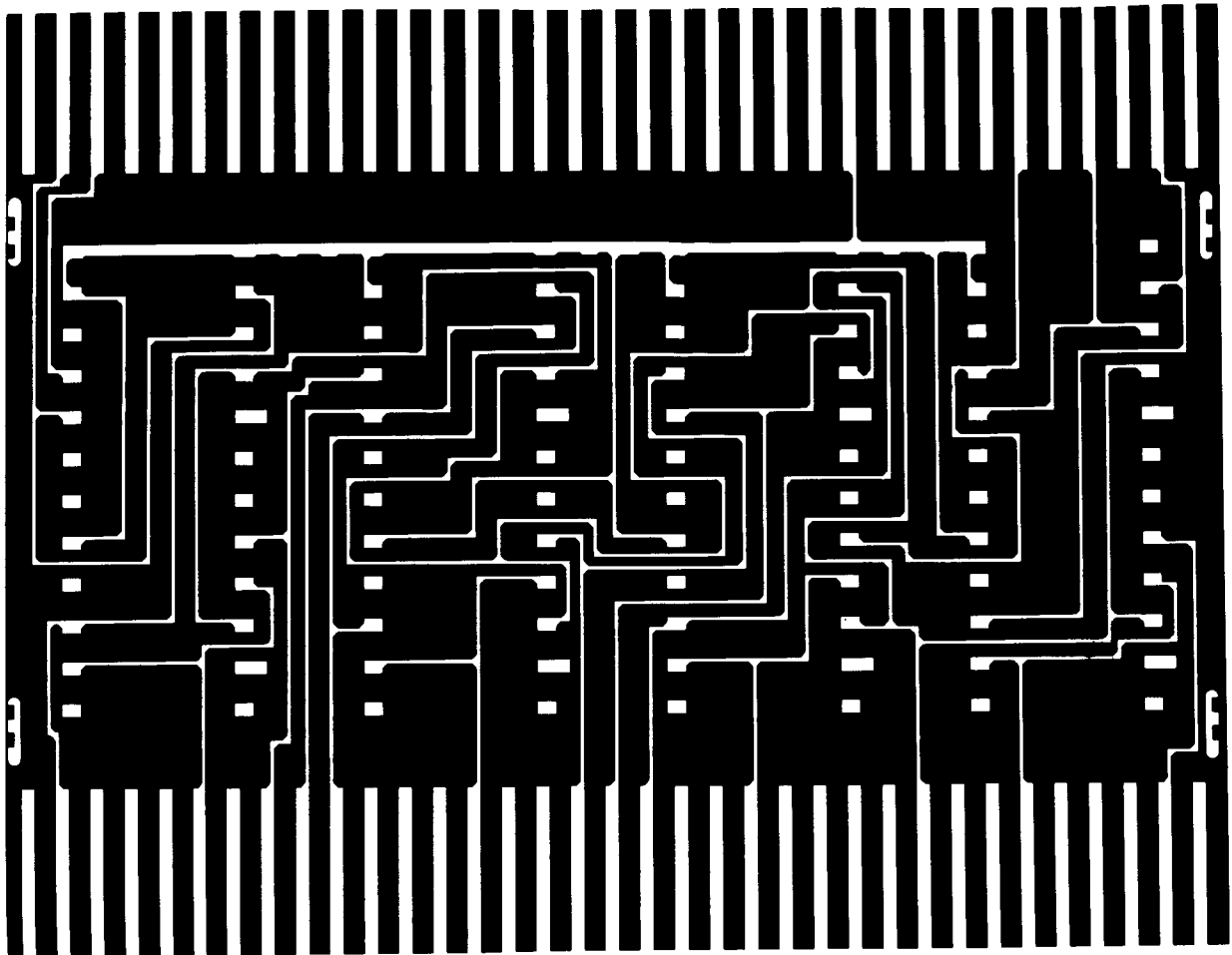A6604-071

FIGURE 27.   SiO MASK LAYOUT

A6604-070

FIGURE 28.   CONDUCTOR LAYOUT

is produced by evaporation of a metal film over the SiO which is then etched to the required configuration. Where connection to the ground plane is required the SiO will have previously been etched to produce a window, when the conductor film is evaporated over the SiO the windows will provide electrical connection from the circuit path to the ground plane. Reliability of this connection is assured by alloying the two metals at an elevated temperature.

The integrated circuit dice are mounted in the channels provided by the substrate. The substrate channels are shown in Figure 26 and a cross-sectional view of the mounted dice is illustrated in Figure 29. A feasibility package containing an 8-stage binary counter is shown in Figure 30.

Interconnection Interfaces

A significant failure mode in microcircuitry has been the connection interface between the circuit path and the interconnection lead or conductor. Although basic to electronic equipment fabrication, it is not always recognized that a typical solder connection (Figure 31 shows lead to printed circuit board conductor) has an interface between the conductor and the solder, and another between the solder and the component lead. In Figure 32 (which shows an actual photograph of an eyeleted pc board) there are interfaces between the conductor to solder to eyelet to solder to component lead. Since each interface constitutes a connection, it is the number of interfaces which affect the reliability.

The considerable reliability improvement which has resulted from the introduction of welded interconnection techniques is due in large measures to the reduction in the number of interfaces. Figure 33 shows the weld of a gold plated dumet wire and a nickel ribbon. Although a satisfactory joint was made, an interface can be seen completely across the junction and is typical for this type of interconnection technique. Thermal compression bonding, another microattachment technique, has character- istics similar to those of the welded technique as shown in Figure 34. The number and type of interfaces determines the reliability.

A single NAND circuit was analyzed for various interface connection techniques. For the soldered techniques, 130 interfaces existed; for the welded techniques, 94 interfaces; and for an integrated circuit device with thermal compression bonds, 14 interfaces were required to provide connection to associated circuitry.
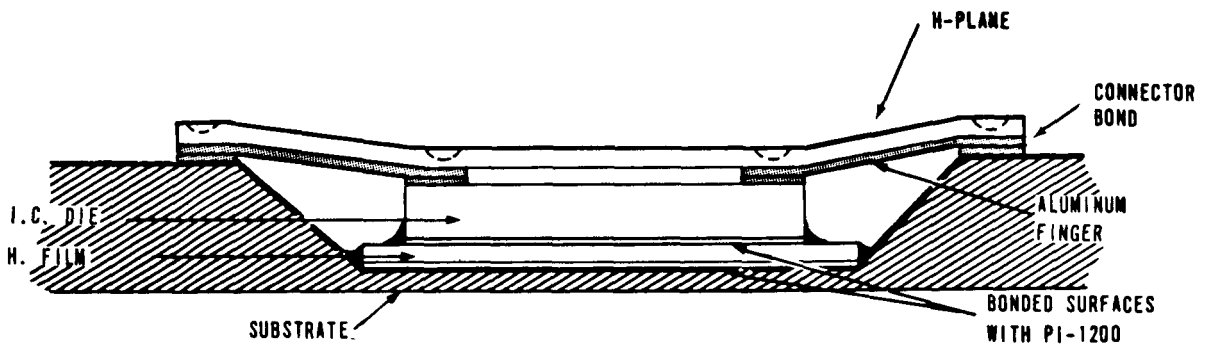
1066-341A

FIGURE 29. CROSS-SECTIONAL VIEW OF A
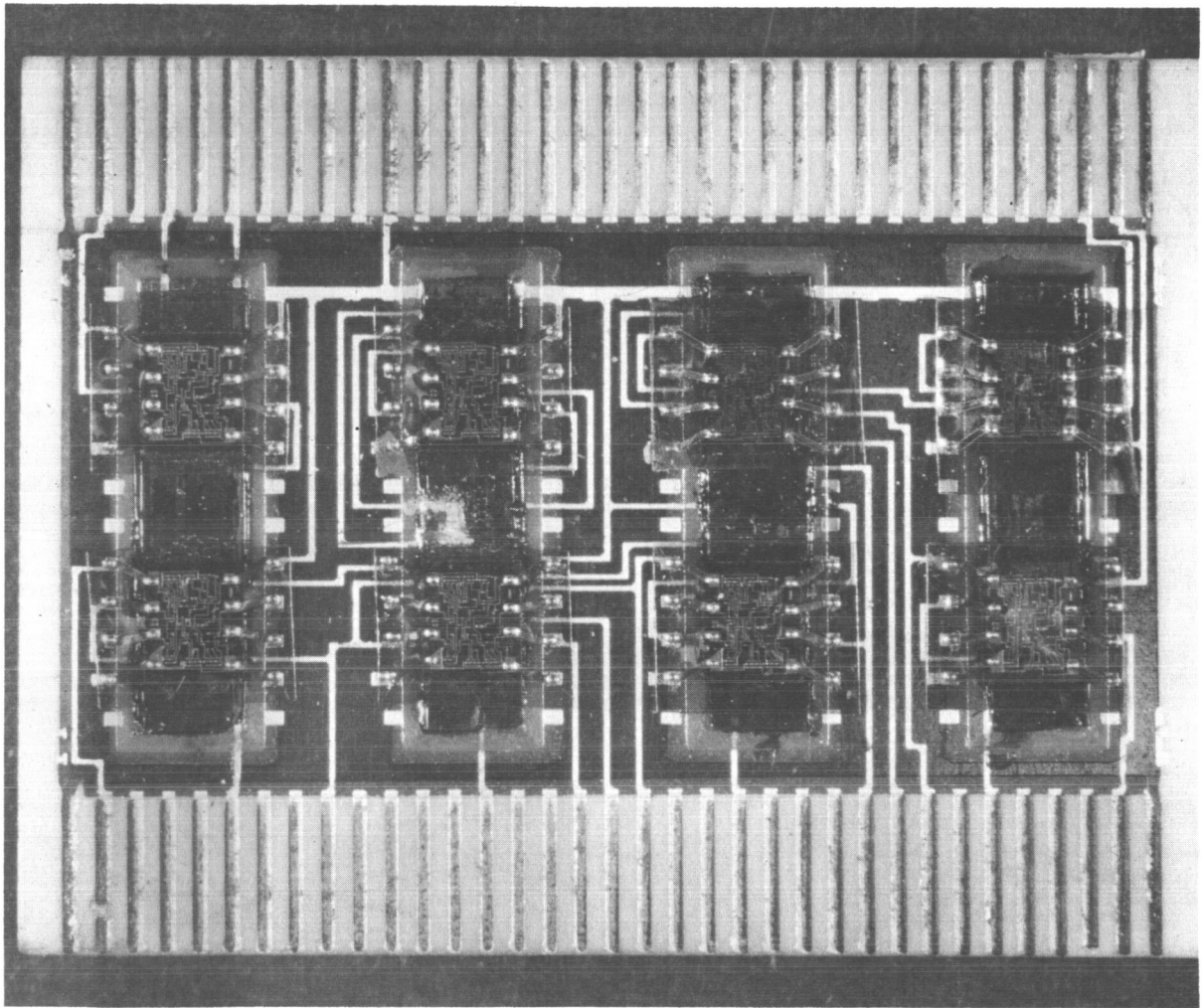SILICON DICE MOUNTED IN A CHANNEL OF THE SUBSTRATE

A6604-064

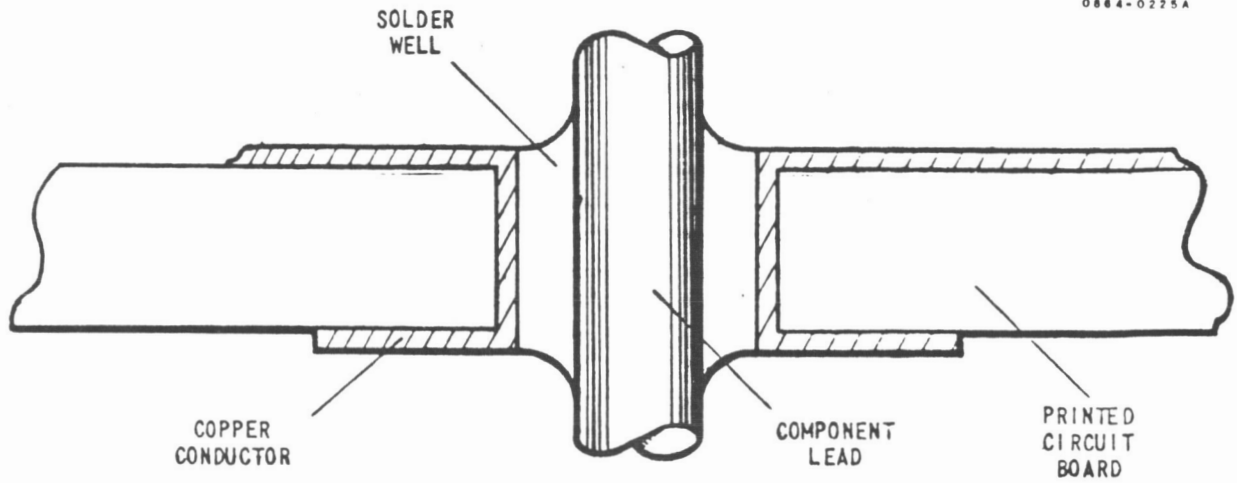FIGURE 30. COMPLETELY ASSEMBLED PACKAGE
PRIOR TO SEALING

0864-0225A

SOLDER WELL

COPPER CONDUCTOR

COMPONENT LEAD

PRINTED CIRCUIT BOARD

FIGURE 31. PRINTED CIRCUIT BOARD SOLDERED CONNECTION

A6402-181-1

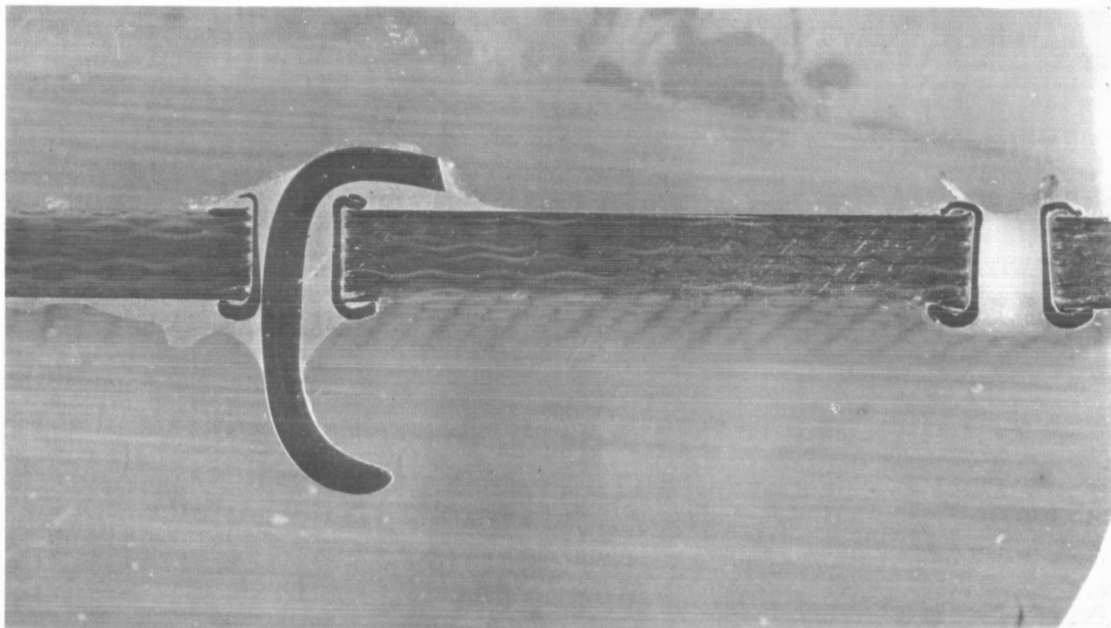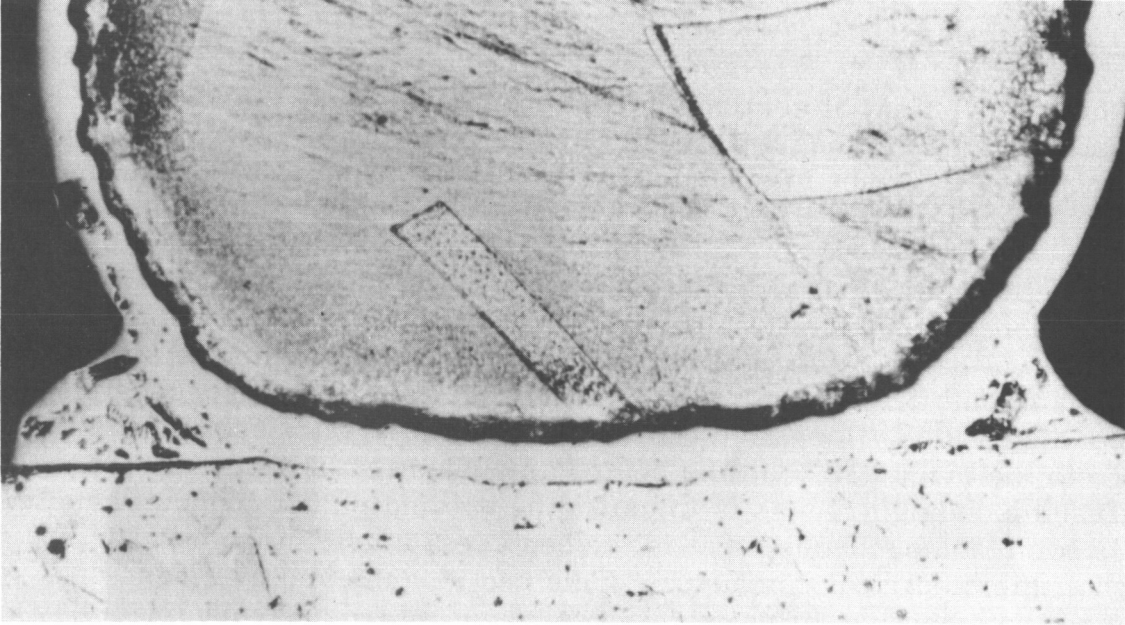FIGURE 32. EYELETED BOND

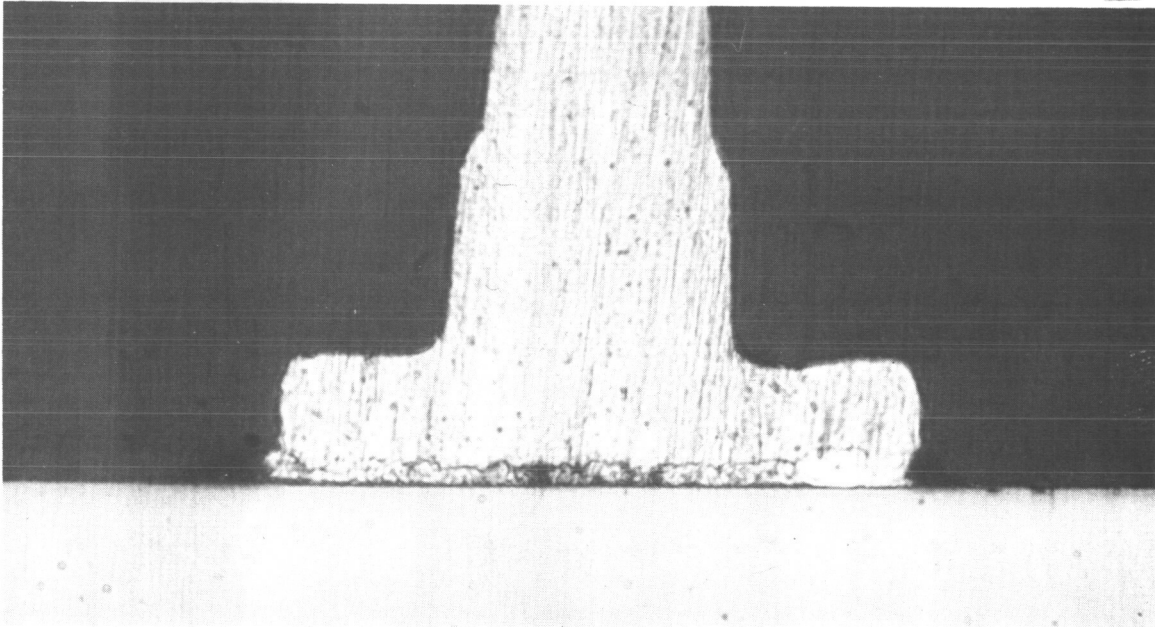FIGURE 33. WELD BOND

A6403-67

FIGURE 34.   THERMAL COMPRESSION BOND

Intraconnections

In the development of semiconductor technology, a new term, intra-connections, describes a process of connection of two or more points or elements in a circuit in such a manner that the separate connection elements are diffused with NO INTERFACE or change in material composition.

The application of intraconnection techniques to subsystem packages accommodating a variety of separate circuit devices or functions would result in ultra-reliability previously available only within the single integrated circuit device itself. This approach was pursued successfully by producing a highly localized diffusion of the metal film used as the lead wire to the circuit film on the device as substate. The object of the diffusion bonding process is to cause the two individual conductor materials to become homogeneous, that is, to become a single monometallic, monolithic electrical conductor. This can be achieved by means of a controlled selective diffusion process resulting from a very precisely controlled cycle, using relatively thin films (5,000 Å - 100,000 Å).

The conductor material used is a high purity aluminum that is coated onto a conductor support material. This is better understood by referring to Figure 35 which shows a typical diffused joining of the two materials. Figure 35a shows an aluminum conductor on a silicon substrate, and also an aluminum conductor coated onto a conductor support. When the conductor lead is molecularly joined to the conductor on the substrate, the two materials (Figure 35b) diffuse with no detectable interface or composition change. Figure 36 is a microphoto of an actual sectioning of a typical diffused junction produced at Honeywell by this method. No interface is detectable; the material support-lead aluminum coating and substrate conductor have fully diffused; and the lead-support material has also alloyed with the conductor lead. The result is a highly reliable and mechanically strong intraconnection.

Circuit Conductors

The interconnection problem can be largely related to the problem of providing simple reliable crossovers. A crossover requires that circuit paths occur on two planes. In a printed circuit board the two sides of a board with appropriate feedthroughs provide this; in some miniature packages a small wire jumper or flying lead provides the crossover. All of these techniques however require interface connections and additional processing steps. The circuit crossover is accomplished in MICPAK by conductors located in the substrate channels.

1164-366A
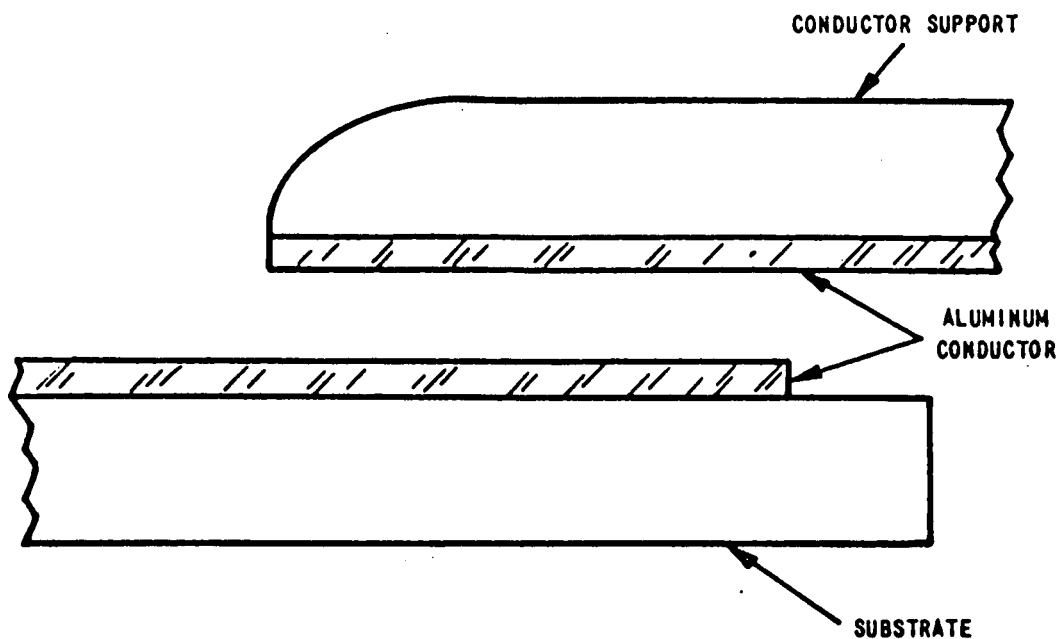
(a) PRIOR TO FUSION
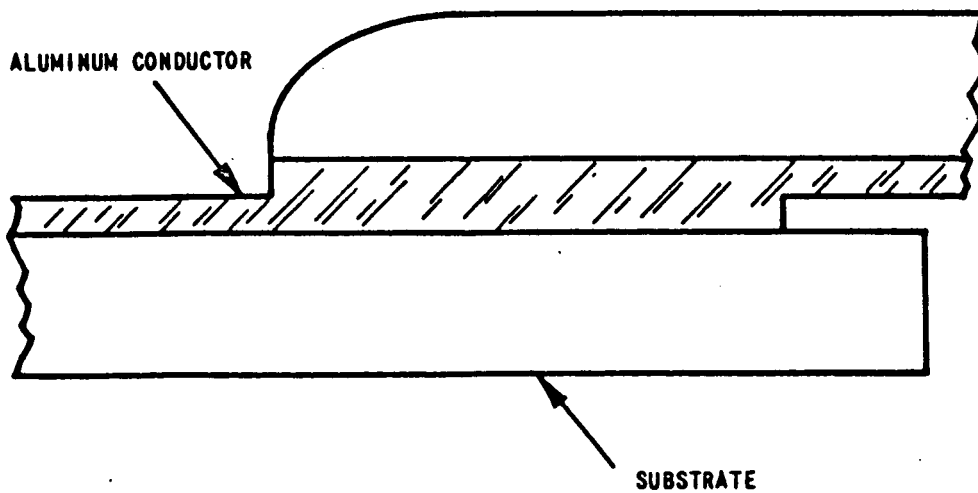
(b) AFTER FUSION
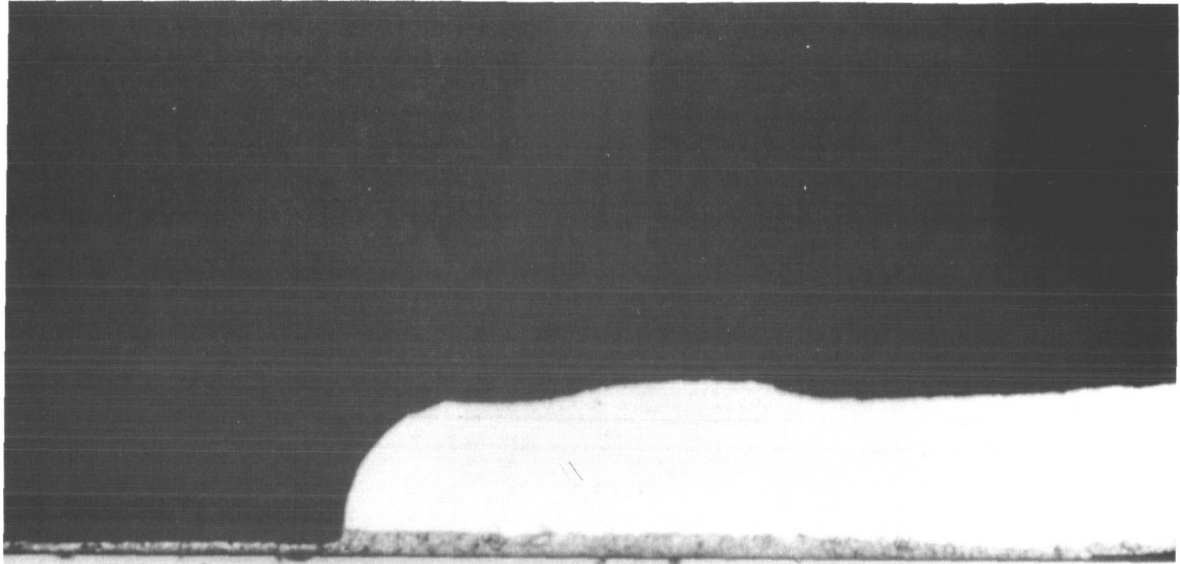
FIGURE 35. SKETCH OF MOLECULAR BOND

A6402-180-1

FIGURE 36. MICROPHOTO OF MOLECULAR BOND

The channels in the substrate are pressed with the sides formed to a 45-degree angle. This configuration allows the circuitry to be formed continuously both on the surface of the substrate and down into the channels. At each device lead connection the conductor terminates on the substrate at a termination pad. A crossover can therefore be effected by approaching the channel, dropping over the edge and coming back up at a suitable location. This way the circuit path actually occurs on two planes but as may be seen from a top view, from a fabrication viewpoint the circuit is produced in a single step operation with no requirement for an interface since the conductor is continuous.

Interconnection "H" Plane Circuitry

With the die located in a channel a gap exists between the circuitry terminal pads on the substrate and the terminal pads on the die. In practice this gap is approximately 0.010-inch in width and since the conductor films are so thin, requires that they be adequately supported over this area. The three major considerations are those of adequate alignment of the conductor circuitry to the die terminations (16 terminations on a die only 30 x 35 mils are possible), consideration of the thermal expansion characteristics, and diffusion bonding of the various conductors. The conductor support film consists of a polyimide film produced by DuPont called Kapton, or more frequently referred to as "H" film. This material is noted for its inertness and stable high temperature properties. The film is metallized and subjected to photo-processing techniques to produce conductor circuitry which will precisely align with that of the circuit die terminations and also those of the substrate. In general the assembly process consists of diffusion bonding the various die conductors to the "H" film, then mounting the "H" film-die assembly and bonding film conductors to the substrate. This assembly is illustrated in Figure 29. Although there are differences in the coefficients of expansion of "H" film and the other materials, the yield strength of the material permits its use over the temperature range.

Diffusion Bonding

The technique utilized for forming the interface-free bond between the dice and the interconnecting conductors is illustrated in Figure 37. It involves placing the aluminum film side of the metallized H-film in contact with the metallized silicon chip or substrate and simultaneously applying heat and pressure. It is virtually the same as the classic
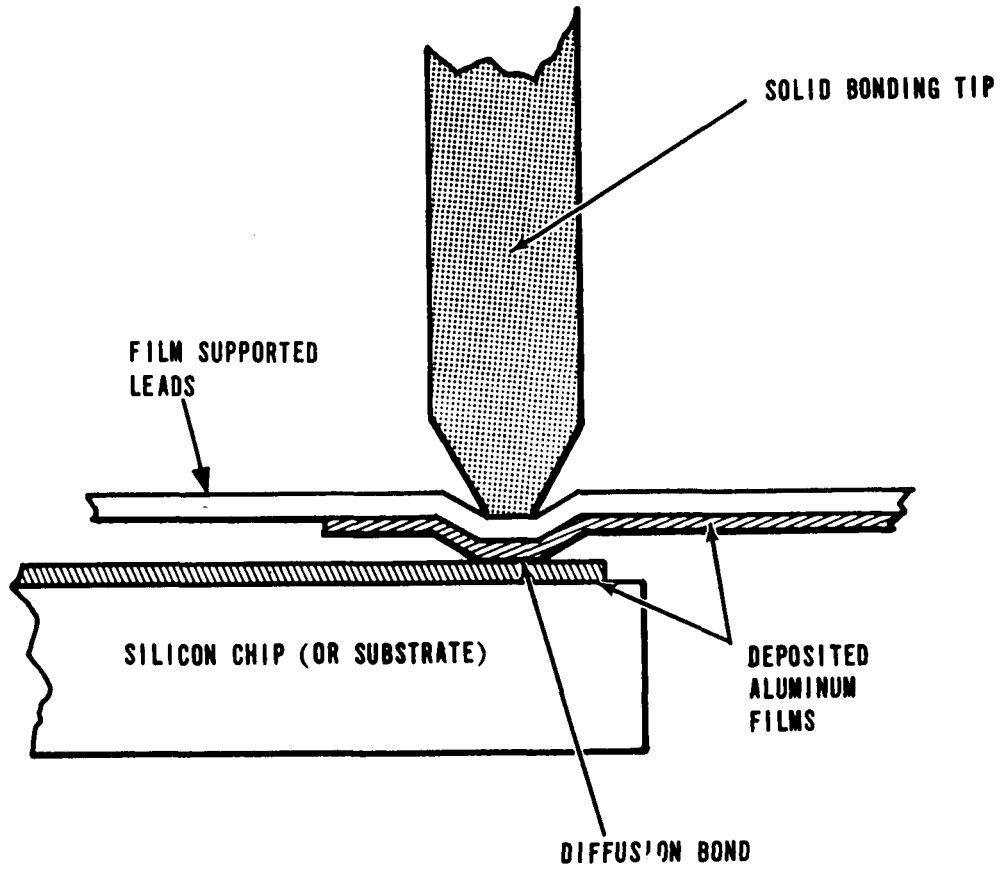
0666-423A

PRIMARY ENERGY SOURCE
SUBSTRATE HEATER

SOLID BONDING TIP

FILM SUPPORTED
LEADS

SILICON CHIP (OR SUBSTRATE)

DEPOSITED
ALUMINUM
FILMS

DIFFUSION BOND

FIGURE 37. H-PLANE DIFFUSION BOND CONCEPT

thermocompression bond. The control parameters were found to be as follows:

Substrate Temperature	360°C
Bonding Tip Geometry	0.004-inch diameter
Bonding Time	10 to 15 seconds

The only source of heat was the substrate heater.

Package Configuration

A complex subsystem package configuration will be defined primarily by: (a) the complexity of the circuit devices and therefore the inter-connection system, (b) the number of connections to the outside world (other subsystems or packages outside of the package proper), (c) the area required for the conductor circuitry itself (this includes void areas between circuit conductors). These three items form an optimized relationship to each other.

The complexity of the circuit device is related packaging-wise to the area of the device and the quantity of lead terminations to the device. These lead terminations will be related to the leads required to go to the outside world and will frequently run to 50 or 100 leads for a 1 by 3/4-inch size substrate. A consideration of individual wires or lead ribbons placed serious handicaps on the construction, bonding, and yield of the package. These lead terminations have been made an integral part of the substrate package, providing electrical continuities through the hermetic seal and since the metal is fused to the ceramic substrate there is no danger of the conductor lifting and allowing leakage of the package. A 70-lead package is illustrated in Figure 38.

Future Circuit Packaging

The interface-free techniques discussed above are applicable to the packaging of Large Scale Integrated (LSI) circuits. LSIs are monolithic integrated circuits containing typically 100 to 200 logic gating functions. These monolithic chips can vary in size from 50 mils in a side to 500 mils on a side. By utilizing diffusion bonding of aluminum to aluminum conductors deposited on "H" film complete LSIs can be packaged as shown in Figure 18. The illustration uses a typical integrated
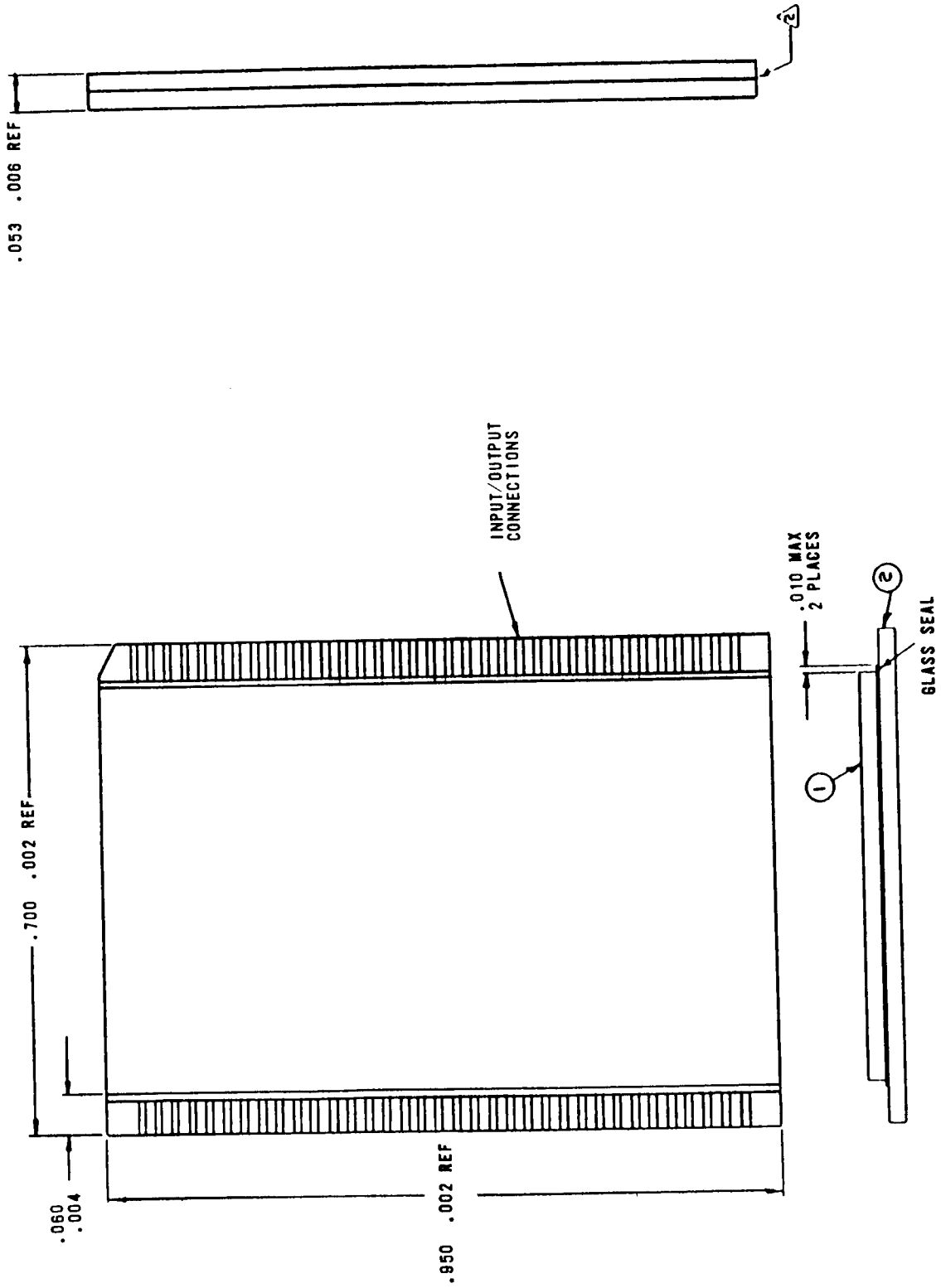
FIGURE 38. A 70-LEAD INTEGRATED CIRCUIT PACKAGE

circuit but the same concept applies to LSIs with 50 to 100 pinouts. The assembly process, briefly stated, is:

1. Evaporate the conductor onto the film.

2. Photoetch the desired interconnect pattern into the conductor metal in a manner analogous to making flexible printed circuits.

3. Bond the aluminum conductors on the film to the contact pads on the chip using thermocompression or ultrasonic bonding.

4. Electrically test the chip/lead film assembly.

5. Package completed assembly.

6. Assemble the packaged circuits onto the anodized printed wiring board (PWB) and attach the lead film conductors to the pads on the substrate.

The film supported leads along with the anodized aluminum printed wiring board provides a completely interface-free interconnection system.

The use of LSIs and film supported leads increases the reliability of the system considerably.

9.0 MANUFACTURING COMPATIBILITY OF THE MAGNETIC WIRE AND THE MOS DEVICES

The results of this contract have shown plated wire memories with MOS electronics to be entirely feasible. Nowhere do the results indicate the existence of any manufacturing incompatibilities between the plated wire and the MOS devices. Instead, their manufacturing methods indicate a very high degree of compatibility since each is produced by completely separate and isolated processes. Both the plated wire and the MOS devices are fabricated, tested, and assembled in their own subassembly prior to being integrated into a working memory system. Each of the manufacturing processes are discussed briefly in the following paragraphs.

9.1 MOS MANUFACTURING PROCESS

The processes involved in the fabrication of N and P channel MOSTs, and MOSTs with bipolar transistors are outlined briefly below. The discussion begins with a simple single-type device and progresses to a complex chip containing both N and P type MOSTs and isolated NPN bipolar transistors. All MOSTs are considered to be enhancement mode devices unless otherwise noted.

The basic steps in the fabrication of MOS monolithic subsystems and conventional double-diffused integrated circuits are the same except that (1) the sequence of steps is repeated less often in the MOS technology; (2) the growth of an epitaxial crystal layer is omitted in the MOS; and (3) only one diffusion is required rather than four as in the conventional double-diffused process.

P Channel MOST. The cross-section of a P channel MOST is shown in Figure 39. The N type starting material is normally in the range of
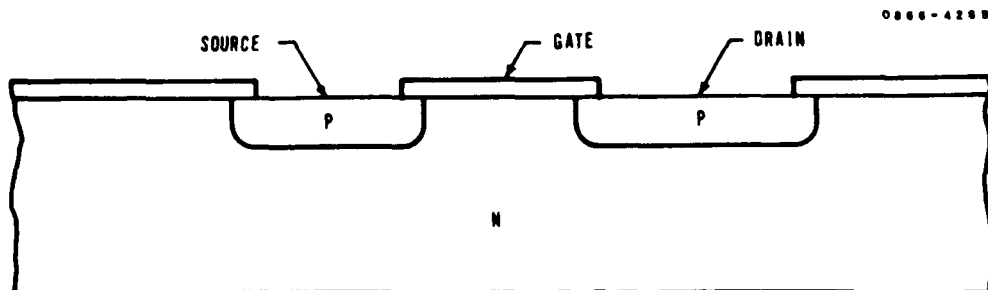

FIGURE 39. SKETCH OF P CHANNEL ENHANCEMENT MODE MOST CHIP

3 to 20 ohm-cm, and the drain and source is normally diffused to a surface concentration of 10^{17} to 10^{20} atoms/cm^3. The gate oxide is 1000 to 2000 Å thick and the gate threshold voltage varies from -3 to -6 volts. The threshold voltage is difficult to predict accurately because it is a function of the charges present at the surface and within the body of the silicon material. These charges are a result of fixed impurity ions within the body, the abrupt termination of the silicon crystalline structure at the surface, and ions contained within the silicon dioxide above the channel region. The process sequence for a P channel MOS device is described in the following paragraphs.

The process starts with an N-type silicon slice which is first oxidized to form a layer of silicon dioxide and then coated in a dark room with a photo-sensitive material. This material is exposed to light through a high-resolution mask. The portions not exposed are soluble and easily removed by a solvent rinse. An etch is used to dissolve the silicon dioxide from the areas not protected by the film of photosensitive material. The wafers are then placed in a special high-temperature furnace containing an atmosphere of gaseous boron (P-type impurity). The boron impurity diffuses into the surface of the silicon wafer only where the oxide has been removed, forming the P-type source and drain. Even at elevated temperatures the oxide protects the surrounding areas from the dopants. A new layer of oxide is formed over the exposed silicon areas of the source and drain during the diffusion.

The desired oxide thickness in the gate region is obtained by removing part of the oxide by the same masking and etching techniques. Portions of the source and drain are then exposed by masking and etching, and a layer of aluminum is deposited over the entire surface, contacting the exposed silicon at the source and drain. The metal surface is then selectively removed. Only the interconnection pattern, source and drain contacts, and gate metallization are left.

Briefly, the process steps and the number of masks required in the fabrication of the P channel MOST are:

1. Source and drain oxide removal (Mask No. 1).

2. Source and drain diffusion.

3. Gate oxide formation (Mask No. 2).

4.   Source and drain contact oxide removal (Mask No. 3).

5.   Metallization (Mask No. 4).

N Channel Enhancement Mode MOST.   The fabrication of enhancement
mode N channel MOSTs can be accomplished by either of two approaches:
(1) the starting material is relatively low resistivity (0.2 to 0.5 ohm-cm)
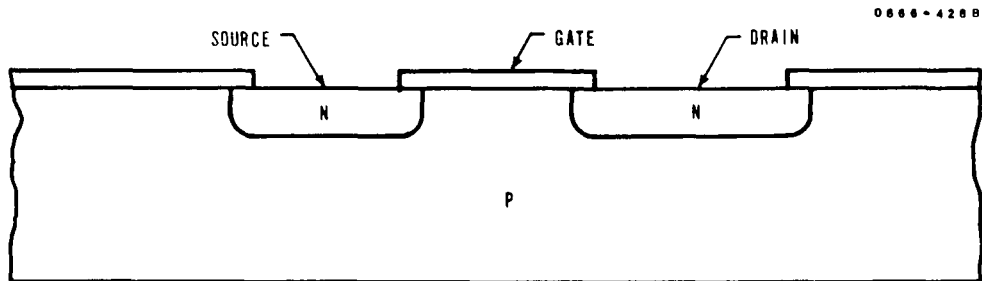and the source and drain are diffused as shown in Figure 40; (2) the

FIGURE 40.   SKETCH OF N CHANNEL ENHANCEMENT
MODE MOST CHIP USING P TYPE STARTING MATERIAL

starting material is high resistivity (10 ohm-cm) N type with diffused P
type isolation regions for location of the N channel MOSTs as shown in
Figure 41.   Both of these approaches provide a surface concentration in
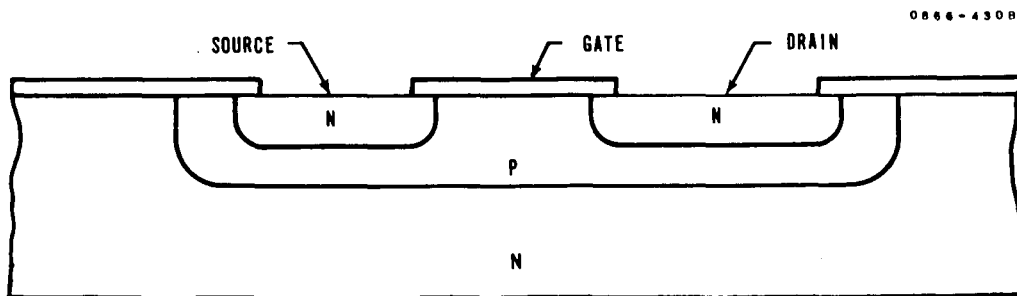

FIGURE 41.   SKETCH OF N CHANNEL ENHANCEMENT MODE
MOST CHIP USING N TYPE STARTING MATERIAL

the P regions greater than $5 \times 10^{16}/cm^3$, which is necessary to prevent
the formation of undesirable inversion layers.   The process steps for the
first approach (P type starting material) are:

1.   Source and drain oxide removal (Mask No. 1).

2. N type source and drain diffusion.

3. Gate oxide formation (Mask No. 2).

4. Source and drain contact oxide removal (Mask No. 3).

5. Metallization (Mask No. 4).

The process steps for the second approach (N type starting material) are:

1. Isolation region oxide removal (Mask No. 1).

2. P type isolation diffusion.

3. Source and drain oxide removal (Mask No. 2).

4. N type source and drain diffusion.

5. Gate oxide formation (Mask No. 3).

6. Source and drain contact oxide removal (Mask No. 4).

7. Metallization (Mask No. 5).

<u>N Channel Depletion Mode MOST</u>. The fabrication of depletion mode N channel MOSTs requires a P type surface concentration of $<< 5 \times 10^{16}/cm^3$. This allows the channel region to automatically invert to an N type surface, hence a depletion mode device is formed. The entire P type surface will also invert, generating leakage paths between source and drain of the same device and between devices on the same chip. This can be avoided by the fabrication technique illustrated in Figure 42. Here a P+ guard band with a surface concentration of greater than $5 \times 10^{16}/cm^3$ is diffused around each source and drain to terminate any inversion layers that may be formed. A P type concentration greater than $5 \times 10^{16}/cm^3$ is sufficient to prevent inversion of the surface to N type. The process for fabricating depletion mode N channel MOSTs is:

1. Guard band oxide removal (Mask No. 1).

2. P type guard band diffusion.

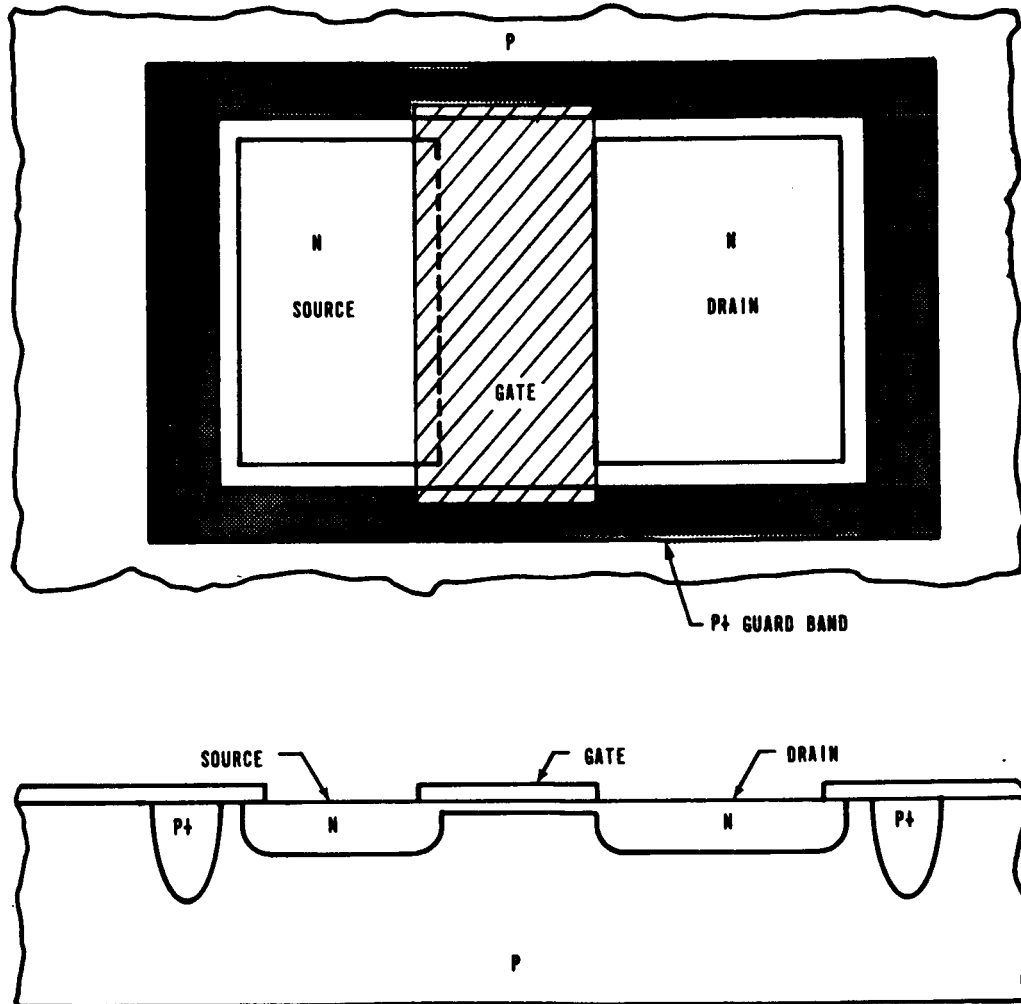3. Source and drain oxide removal (Mask No. 2).

FIGURE 42. A DEPLETION MODE N CHANNEL MOST
UTILIZING A P+ GUARD BAND FOR CONTROLLING
SURFACE INVERSION BETWEEN SOURCE AND DRAIN

4.   N type source and drain diffusion.

5.   Gate oxide formation (Mask No. 3).

6.   Source and drain contact oxide removal (Mask No. 4).

7.   Metallization (Mask No. 5).

P Channel MOST With Common Collector NPN.   The cross-section of a chip containing P channel MOSTs and common collector NPN bipolar transistors is shown in Figure 43.   Using N type starting material, the
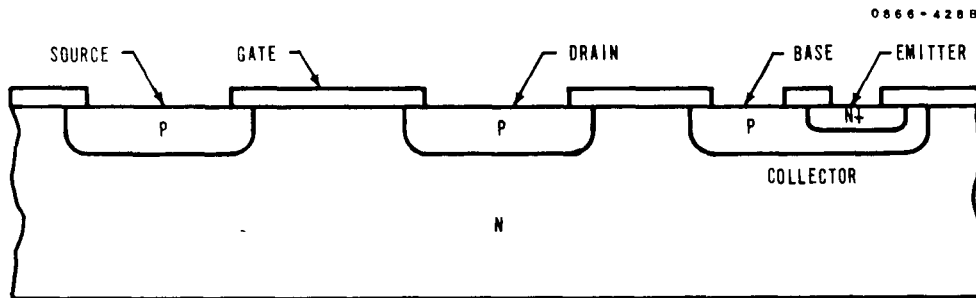

FIGURE 43.   SKETCH OF P CHANNEL MOST AND BIPOLAR NPN
TRANSISTOR (COMMON COLLECTOR) IN THE SAME CHIP

process steps for the fabrication of this device are:

1.   Source, drain, and NPN base oxide removal (Mask No. 1).

2.   P type source, drain, and NPN base diffusion.

3.   NPN emitter oxide removal (Mask No. 2).

4.   N+ emitter diffusion.

5.   Gate oxide formation (Mask No. 3).

6.   Contact oxide removal (Mask No. 4).

7.   Metallization (Mask No. 5).

P Channel MOST With NPN. A more versatile combination of MOSTs and bipolar transistors is illustrated by the chip cross-section shown in Figure 44. Here each bipolar transistor contains its own collector region.
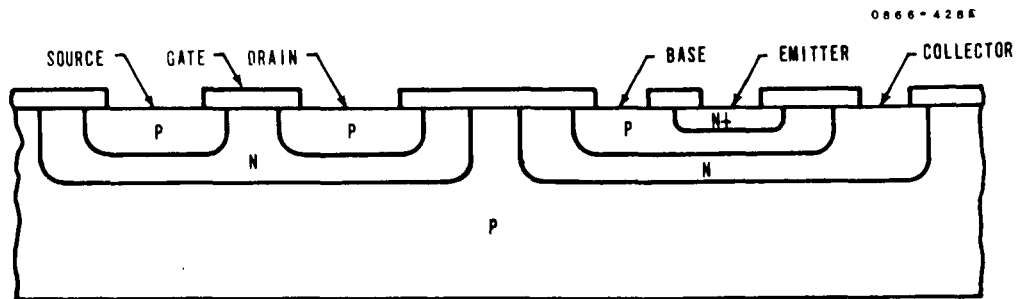

FIGURE 44. SKETCH OF ISOLATED P CHANNEL MOST AND
NPN BIPOLAR TRANSISTOR IN THE SAME CHIP

Using P type starting material and all-diffusion techniques, the process steps for the fabrication of this device are:

1. NPN collector and MOST isolation region oxide removal (Mask No. 1).

2. N type collector and MOST isolation diffusion.

3. Source, drain, and NPN base oxide removal (Mask No. 2).

4. P type source, drain, and NPN base diffusion.

5. NPN emitter oxide removal (Mask No. 3).

6. N+ emitter diffusion.

7. Gate oxide formation (Mask No. 4).

8. Contact oxide removal (Mask No. 5).

9. Metallization (Mask No. 6).

Complementary MOSTs. The integration of both N and P type MOSTs within the same chip is illustrated by the cross-section shown in Figure 45.
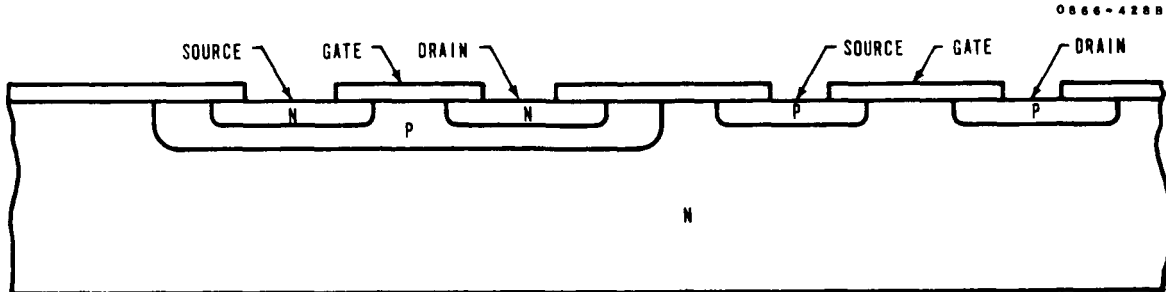

FIGURE 45. SKETCH OF COMPLEMENTARY P CHANNEL AND
N CHANNEL MOSTs IN THE SAME CHIP

The desirability of complementary MOSTs is discussed in another section of this report. The simplest fabrication process uses N type starting material and is:

1. N channel isolation region oxide removal (Mask No. 1).

2. P type isolation diffusion.

3. P channel source and drain oxide removal (Mask No. 2).

4. P type source and drain diffusion.

5. N channel source and drain oxide removal (Mask No. 3).

6. N type source and drain diffusion.

7. Gate oxide formation (Mask No. 4).

8. Contact oxide removal (Mask No. 5).

9. Metallization (Mask No. 6).

The parameters of each type of MOST can be improved at the expense of additional process steps in the formation of the channels, gate oxide, and the metallization. This would require at least two additional masking operations.

Complementary MOSTs and Bipolar NPNs. The fabrication of comple-
mentary MOSTs and bipolar NPN transistors within the same silicon chip
can be accomplished by either of two approaches:

All diffused.

Epitaxial diffused.

The all-diffused approach is shown in Figure 46. This process can provide
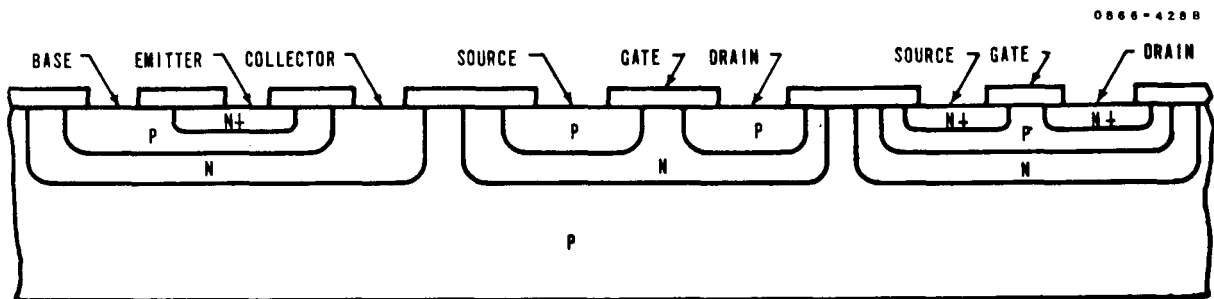

FIGURE 46. SKETCH OF COMPLEMENTARY MOSTs AND
NPN BIPOLAR TRANSISTOR IN THE SAME CHIP

functions with the capability of high operating speeds and low power dissi-
pation. The process uses a P type substrate and the steps are:

1. Oxide removal for NPN collector and MOST isolation (Mask No. 1).

2. N type diffusion.

3. Oxide removal for NPN base, N channel MOST isolation, and
   P channel source and drain (Mask No. 2).

4. P type diffusion.

5. Oxide removal for NPN emitter and N channel source and
   drain (Mask No. 3).

6. N+ type diffusion.

7. Gate oxide formation (Mask No. 4).

8. Contact oxide removal (Mask No. 5).

9. Metallization (Mask No. 6).

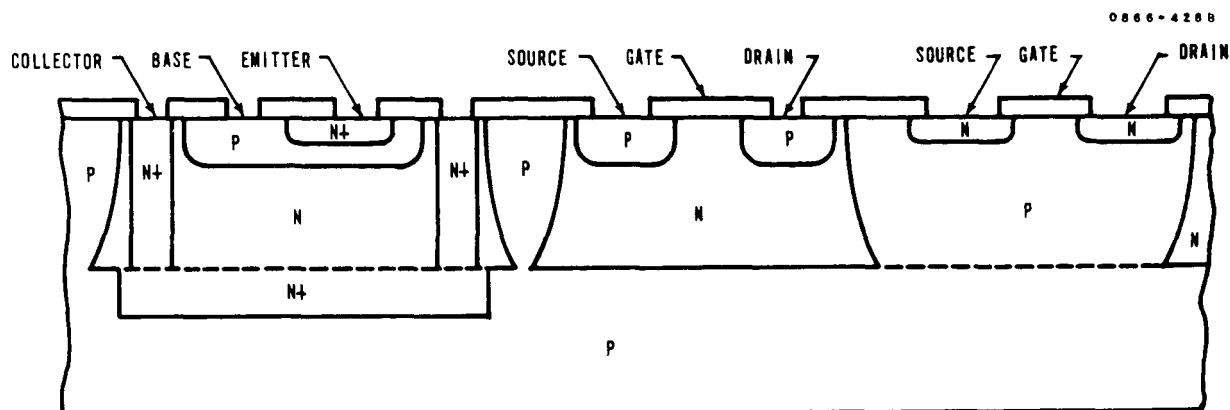The epitaxial diffused approach is shown in Figure 47. This approach

FIGURE 47. SKETCH OF COMPLEMENTARY MOSTs AND
A HIGH CURRENT NPN BIPOLAR TRANSISTOR IN
THE SAME CHIP CONSTRUCTED OF EPITAXIAL MATERIAL

provides a function with the capability of higher operating speeds, lower
power dissipation, and higher current NPNs than the all-diffused approach.
The process utilizes a P type substrate with an epitaxially grown N type
layer. An N+ buried layer and a deep N+ diffusion is used to reduce the
saturation resistance of the NPN. The process steps required for the
fabrication of this device are (starting with the P type substrate):

1. Remove oxide in N+ buried layer regions (Mask No. 1).

2. Diffuse N+ buried layer.

3. Grow N type epitaxial layer.

4. Grow oxide over entire surface.

5. Remove oxide for isolation regions (Mask No. 2).

6. P type isolation diffusion.

7. Remove NPN collector contact oxide (Mask No. 3).

8. Deep N+ diffusion.

9. Remove oxide for P channel source and drain, and NPN base (Mask No. 4).

10. P type source, drain, and NPN base diffusion.

11. Remove oxide for N channel source and drain, NPN emitter, and NPN collector contacts (Mask No. 5).

12. N+ type diffusion.

13. Gate oxide formation (Mask No. 6).

14. Contact oxide removal (Mask No. 7).

15. Metallization (Mask No. 8).

The parameters of each component can be improved at the expense of additional process steps in the formation of the channels, gate oxide, and the metallization. The fabrication of the above device presents a very difficult task in the area of process control, but the end result is a very efficient circuit.

The use of epitaxial material in the fabrication of any of the previous devices will result in considerable improvement in device parameters.

9.2 PLATED WIRE MANUFACTURING PROCESS

A flow chart of a plated wire manufacturing process is shown in Figure 48. The steps listed show a representative process, which is only one of numerous processes which can be utilized. A photograph of the Aero-Florida magnetic wire plater is shown in Figure 49.

The plating process begins with a spool of beryllium-copper (Be-Cu) wire 5 mils in diameter. The wire moves continuously through each process step and is cut into definite lengths after the final on-line anneal step.

The wire first goes through several surface conditioning and cleaning steps prior to receiving an electrodeposited film of pure copper. The wire is now ready for the plating of the magnetic film. This is accomplished by a Honeywell developed process which precisely controls the materials composition, rate of deposition, film thickness, and magnetic properties.
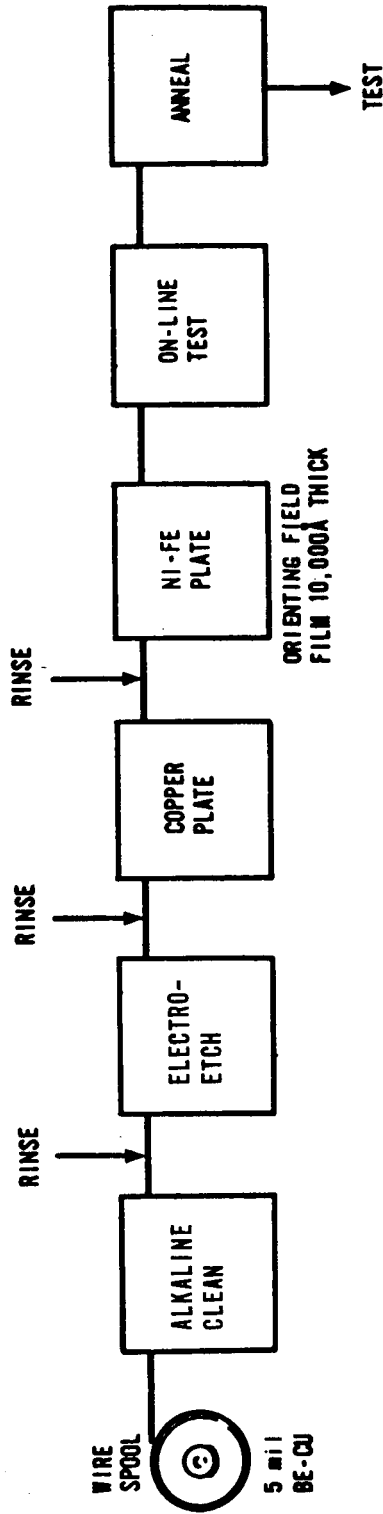
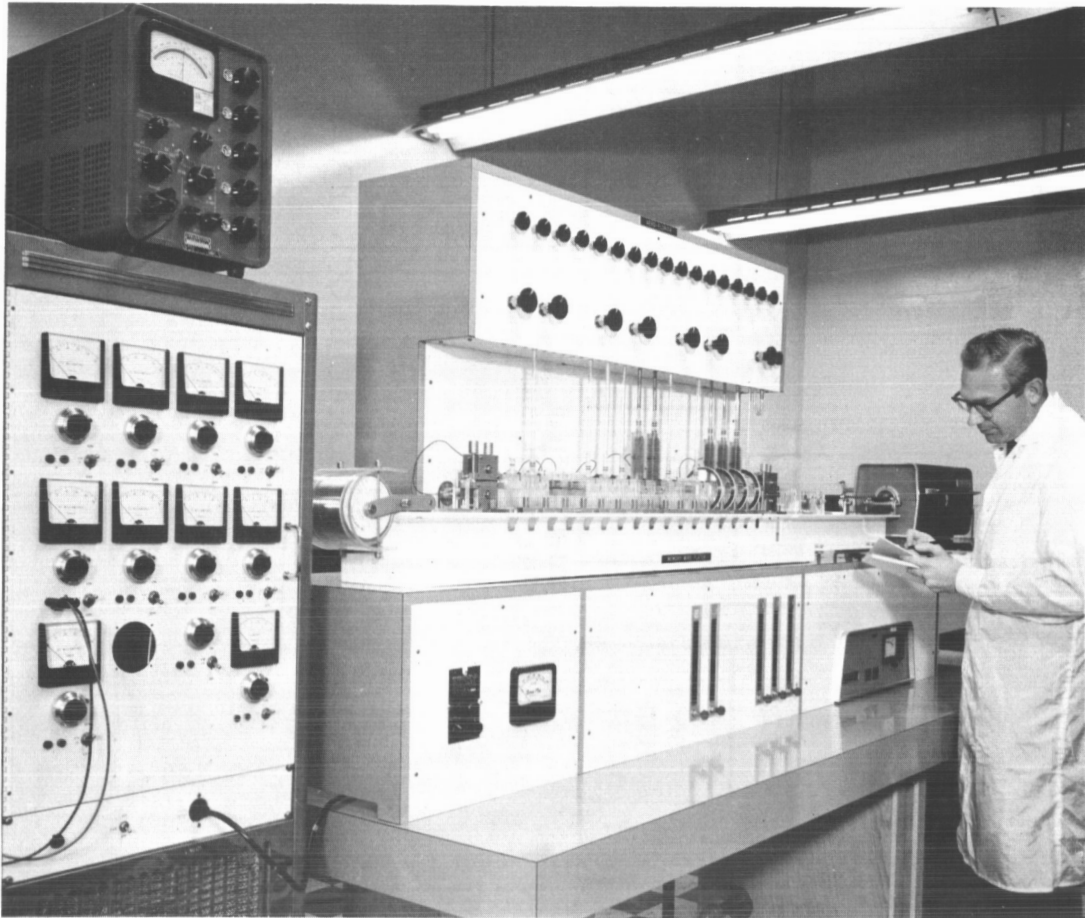FIGURE 48.   MAGNETIC FILM PLATER OPERATIONAL BLOCK DIAGRAM

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FIGURE 49.   MAGNETIC THIN FILM WIRE PLATER

Within the plating system, provisions are made for continuous testing of the magnetic properties. These tests include measurement of H_c (coercive force), H_k (anistropy constant), dispersion, and skew.

Honeywell can also perform pulse tests for storing information, digit disturb, and nondestructive readout level in an on-line tester which is part of the plating system. Post deposition anneal is performed after plating and initial test.

An off-line tester, Figure 50, consists of high quality commercial laboratory equipment for pulse testing the wire and selection of wire which meets the necessary parameters to satisfy the memory system requirements such as creep, digit disturb levels and specified output voltage.

Honeywell has developed a technique to measure the switching astroid of the plated wire. This test is significant in determining the NDRO capability of the wire. Honeywell designed instrumentation is used to perform the test.

A test facility, Figure 51, is available for measurement of H_c, H_k, skew and dispersion as a function of amount of stress and degree of twist. This test is also utilized as a measurement of the composition of the magnetic alloy.

An apparatus which facilitates the study of aging of plated wire has been developed by Honeywell. This equipment applies a temperature gradient to the wire for the purpose of accelerating any aging effects. This provides information applicable to the anneal cycle which assists in the prevention of aging problems in plated wire memory systems.

Upon completion of the off-line test program, the plated wire is ready for assembly into a memory plane and further testing as a complete sub-assembly.
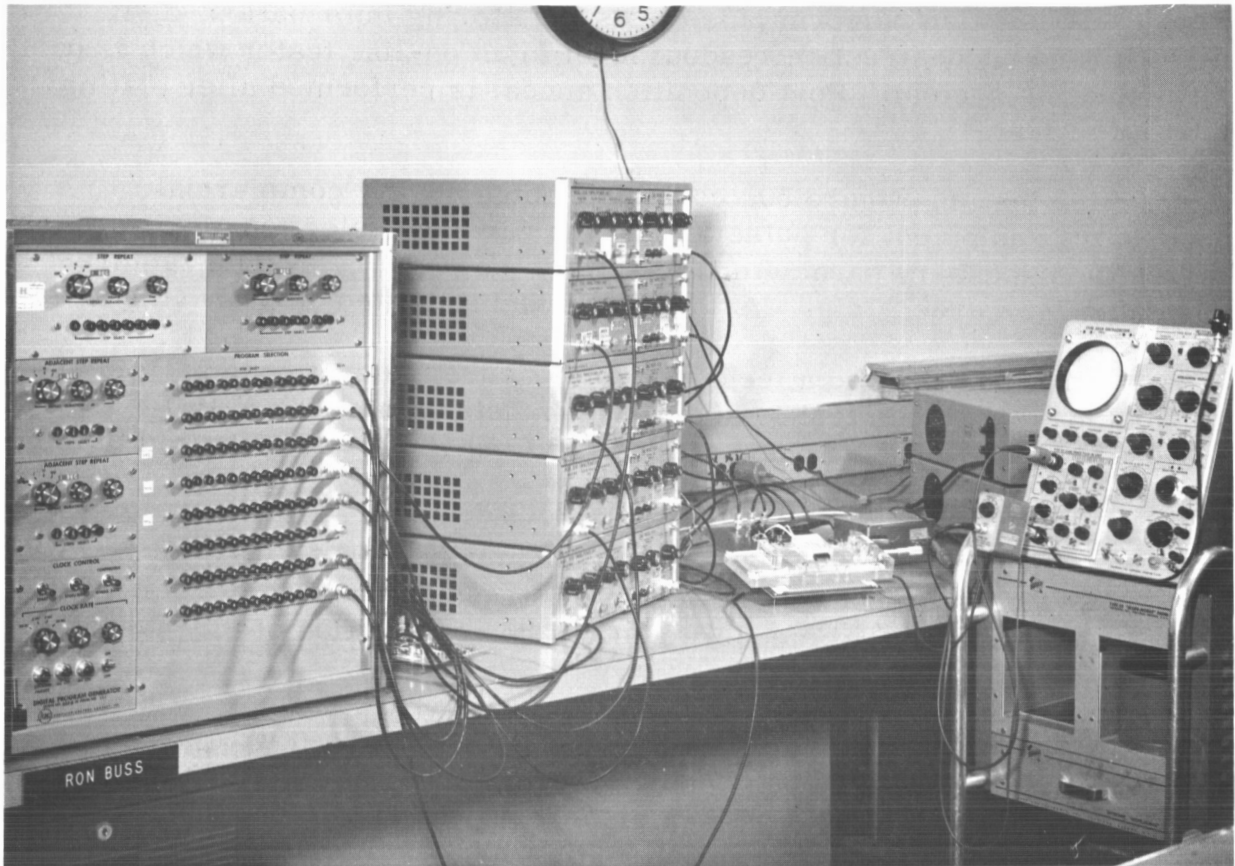
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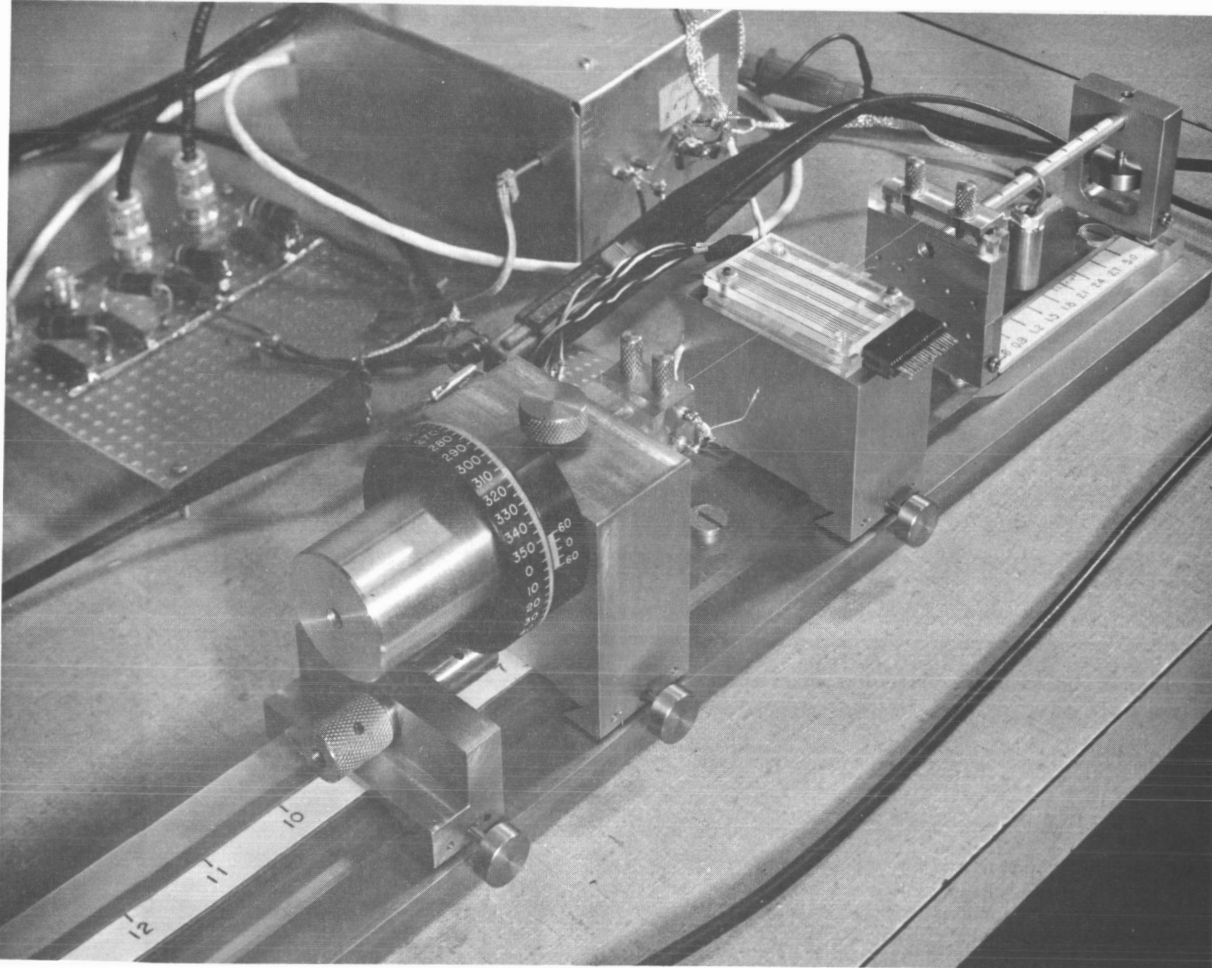

FIGURE 50.   PULSE TEST EQUIPMENT

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FIGURE 51.   TORSIONAL STRAIN - SKEW EQUIPMENT

10. 0 POWER AND SPEED REQUIREMENTS

10. 1 MEMORY CYCLE TIME

The cycle time of an MOS plated wire memory is determined by the total time required to address a word and receive the stored information as a logic output. The total time for one complete memory cycle is equal to the sum of the following: clock pulse width (t_{cw}), settling time of the address register (t_{ad}), delay time of the address decoding logic (t_{dl}), rise time of word drive selection (t_{ws}), rise time of word current (t_{wc}), delay time of sense line (t_{sl}), delay time of the sense amplifier (t_{sa}) and settling time of the information register (t_{ir}). Hence

$$t_{cy} = t_{cw} + t_{ad} + t_{dl} + t_{ws} + t_{wc} + t_{sl} + t_{sa} + t_{ir}$$

The address decoding network shown in Figure 52 will be used in calculating the delay time. The delay time associated with MOS circuitry is RC limited. The load MOST, Q_5, has a R_{on} of 25K ohms while the gate MOSTs, Q_1 through Q_4, have a R_{on} of 2. 5K ohms.

The output capacitance of the decoding gate is expressed as:

$$C_o = C_{DS(1-4)} + C_{im} + C_{in-6}$$

where

$C_{DS(1-4)}$ is the sum of the drain to source capacitance of Q_1 through Q_4

C_{im} is the interconnection metalization capacitance between the decoding gate and the input of Q_6

C_{in-6} is the gate input capacitance of Q_6

also,

C_{DS} is a p-n junction capacitance of approximately 0. 1 pf/mil^2

C_{im} is a thick oxide capacitance of approximately 0. 03 pf/mil^2

C_{in} is primarily a thin oxide capacitance of approximately 0. 25 pf/mil^2
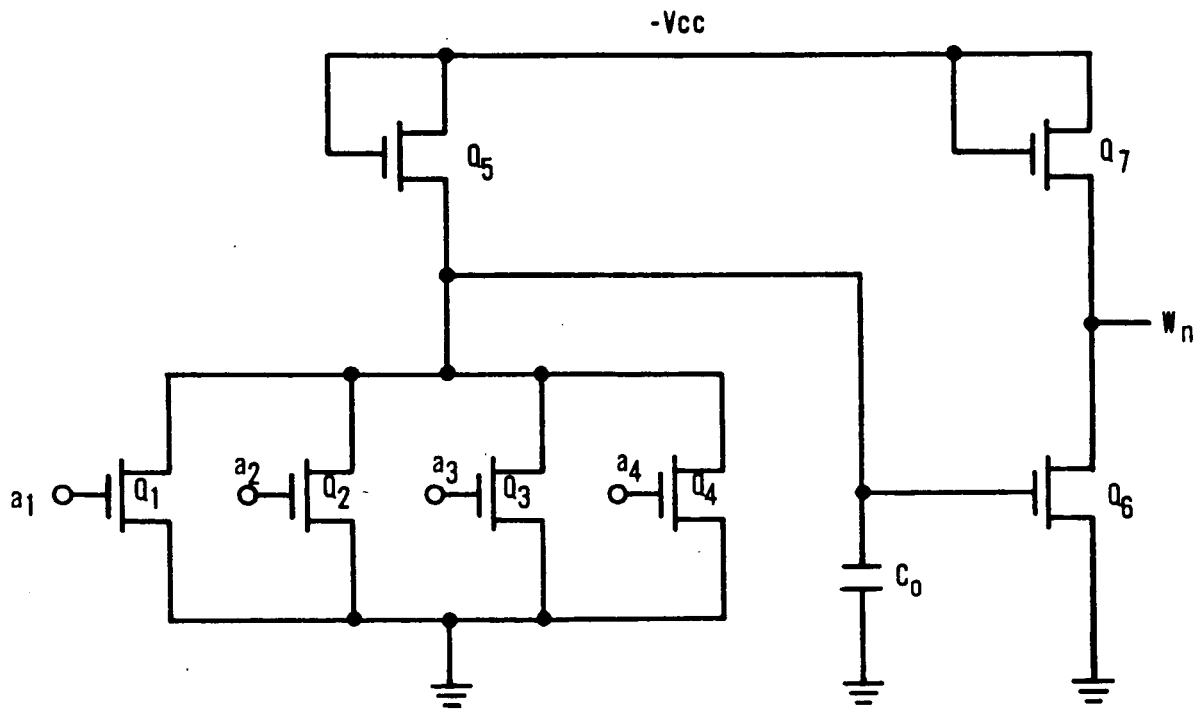
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FIGURE 52. SCHEMATIC DIAGRAM OF AN ADDRESS
DECODING NETWORK

Using these values, C_o becomes

$$C_o = (2.1 + 0.1 + 0.2) \text{ pf} = 2.4 \text{ pf}$$

Assuming three time constants for turn off time of the decoding logic t_{dl} becomes

$$t_{dl} = 3 R_{on} C_o = (3)(25 \times 10^3)(2.4 \times 10^{-12})$$

$$= 180 \text{ nanoseconds}$$

In a similar manner, the remaining delay times can be calculated. For a 1,000 word memory, the total cycle time for READ ONLY becomes:

$$t_{cy} = t_{cw} + t_{ad} + t_{dl} + t_{ws} + t_{wc} + t_{sl} + t_{sa} + t_{ir}$$

$$= \left[(500) + (800) + (180) + (300) + (50) + (10) + (100) + (600) \right] \text{ nanoseconds}$$

$$\cong 2.6 \text{ microseconds}$$

A 1,024 word 26-bit memory operating in a READ ONLY mode at a 2.6 microsecond cycle time would have a total power dissipation of approximately 45 watts. Both cycle time and power dissipation can be improved considerably by the use of complementary MOS devices. Complementary devices are discussed in the following paragraphs.

## 10.2 COMPLEMENTARY MOST LOGIC CIRCUITS

The most significant features of complementary MOST circuitry are:

Higher Switching Speeds

Lower Power Dissipation.

These can be discussed further by the examination of Figure 53. The use of a single type MOST, P channel in this case, for both the active device and the load resistor is shown in 53a. Complementary P channel and N channel MOSTs are illustrated in 53b.

The operation of the inverter circuit in Figure 53a is as follows. The input voltage swing is from near ground to a voltage near $-V_{DD}$. When

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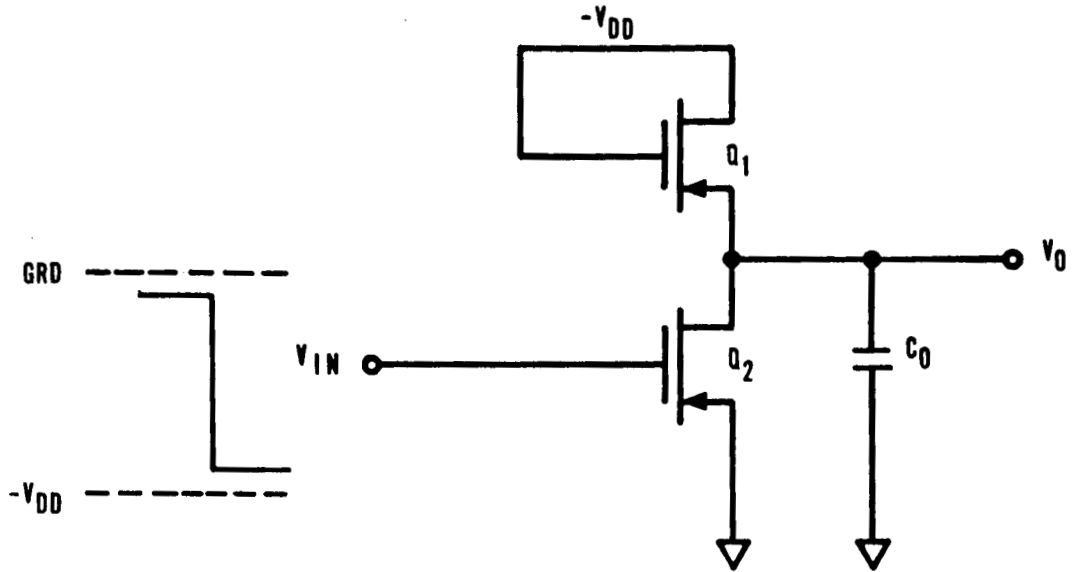
a. Inverter circuit using P channel MOSTs as both the active device and the load resistor.
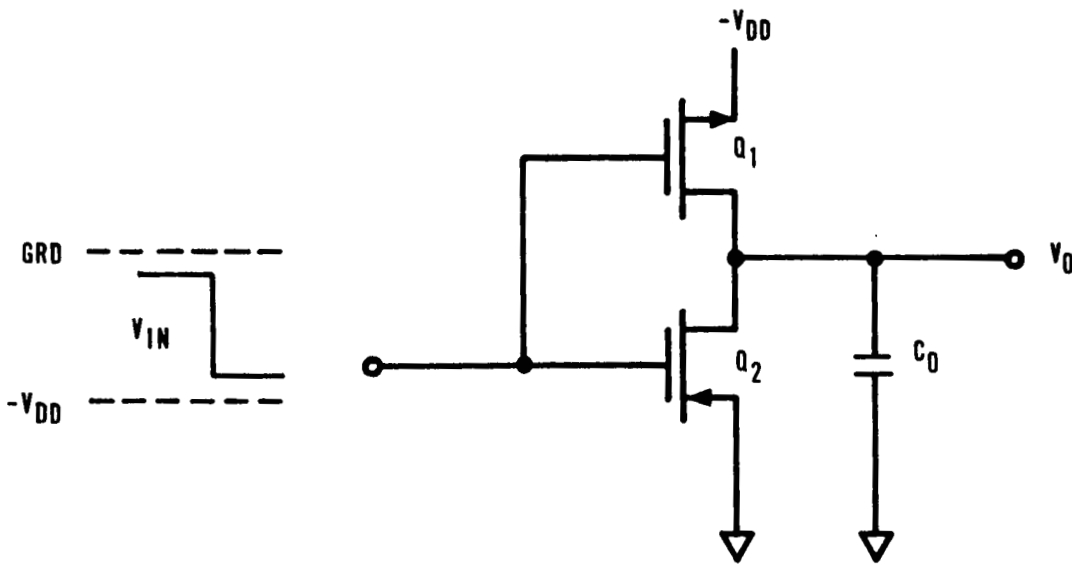
b. Inverter circuit using P channel MOST as the active device and an N channel MOST as the load resistor.

FIGURE 53.   MOST INVERTER CIRCUIT CONSTRUCTED AS (a) SINGLE TYPE MOSTs (b) COMPLEMENTARY MOSTs

the input is near ground the V_{GS} of Q_2 is below its threshold and Q_2 is off. The output then is more positive than the supply voltage by the magnitude of the threshold voltage of Q_1:

$$V_o = -V_{DD} + V_T$$

When the input is near the supply voltage, the threshold voltage of Q_2 is exceeded and it is turned on. The output voltage becomes equal to:

$$V_o = \frac{R_{on\,2}\,(-V_{DD})}{R_{on\,1} + R_{on\,2}}$$

The manner in which Q_1 is connected dictates that it is always turned on and, in this case, both Q_1 and Q_2 are on. The output voltage is a result of the resistor divider action of the "on" resistance of the two MOSTs. This means that the R_{on} of Q_1 should be approximately equal to 10 x R_{on} of Q_2 in order for V_o to be near ground. The resulting switching time will be a function of the output $R_{on}\,C_o$ time constant during turn-on and turn-off of Q_2. (C_o is defined as the total output capacitance loading the inverter.) The rise time during turn-off will be approximately ten times greater than the fall time during turn-on. The overall propagation delay time through a logic network is therefore limited by the "on" resistance of the load MOST. Power dissipation for a large network can become excessive as a consequence of both Q_1 and Q_2 being on at the same time.

The use of complementary MOSTs as shown in Figure 53b solves both of the above problems. With an N channel MOST as the load and a P channel MOST as the active device, the inverter circuit operates as follows. When the input voltage is near ground Q_2 is off and Q_1 is on. The output capacitance, C_o, charges through the "on" resistance of Q_1 with a time constant of $R_{on1}\,C_o$. During quiescent conditions either Q_1 or Q_2 is off, and this presents a very high resistance between the supply voltage and ground. The only current present is the leakage current of the drain junction. Both Q_1 and Q_2 must be enhancement mode devices in order for the input voltage to turn one or the other completely off. The gate of Q_1 is always more positive than its source and the gate of Q_2 is always more negative than its source, hence only enhancement mode devices will provide the required turn-off action. The "on" resistance of Q_1 and Q_2 can be made equal and as low as practical, hence the turn-on and turn-off times will be symmetrical. The total propagation delay time of a complete logic network will be approximately an order of magnitude less than for the single type MOSTs discussed previously. Since one of the MOSTs is normally off the stand-by power dissipation is reduced to a minimum. The total power dissipation becomes

a function of the repetition rate and the magnitude of C_o, because most of the power is used in charging and discharging this capacitance. It can be shown that the total power dissipation is equal to:

$$P_d = C_o V_{DD}^2 f + P_s$$

Where C_o if the total output capacitance, V_{DD} is the supply voltage f is the repetition rate, and P_s is the standby power (P_d was incorrectly given in the 5th report as $P_d = 2 C_o V_{DD}^2 f + P_s$). Power dissipation as a function of clock rate is illustrated by the curve shown in Figure 54. This curve indicates that complementary MOS devices are ideal for spacecraft systems where clock rates vary considerably as a function of each phase of the mission.

Therefore the use of complementary MOSTs for logic circuits offers a significant increase in speed and a considerable reduction of power dissipation. The mechanization of both a NAND gate and a NOR gate is shown in Figure 55.

In Section 6 complementary MOSTs were shown to reduce the delay time through the word driver circuit from 300 nanoseconds to 100 nanoseconds.

11. 0 PROGRAM FOR THE NEXT PHASE

The next phase of this contract consists of the fabrication and testing of the feasibility MOS-plated wire memory. This will be a 16 word 2 bit breadboard system using commercially available discrete MOS transistors.

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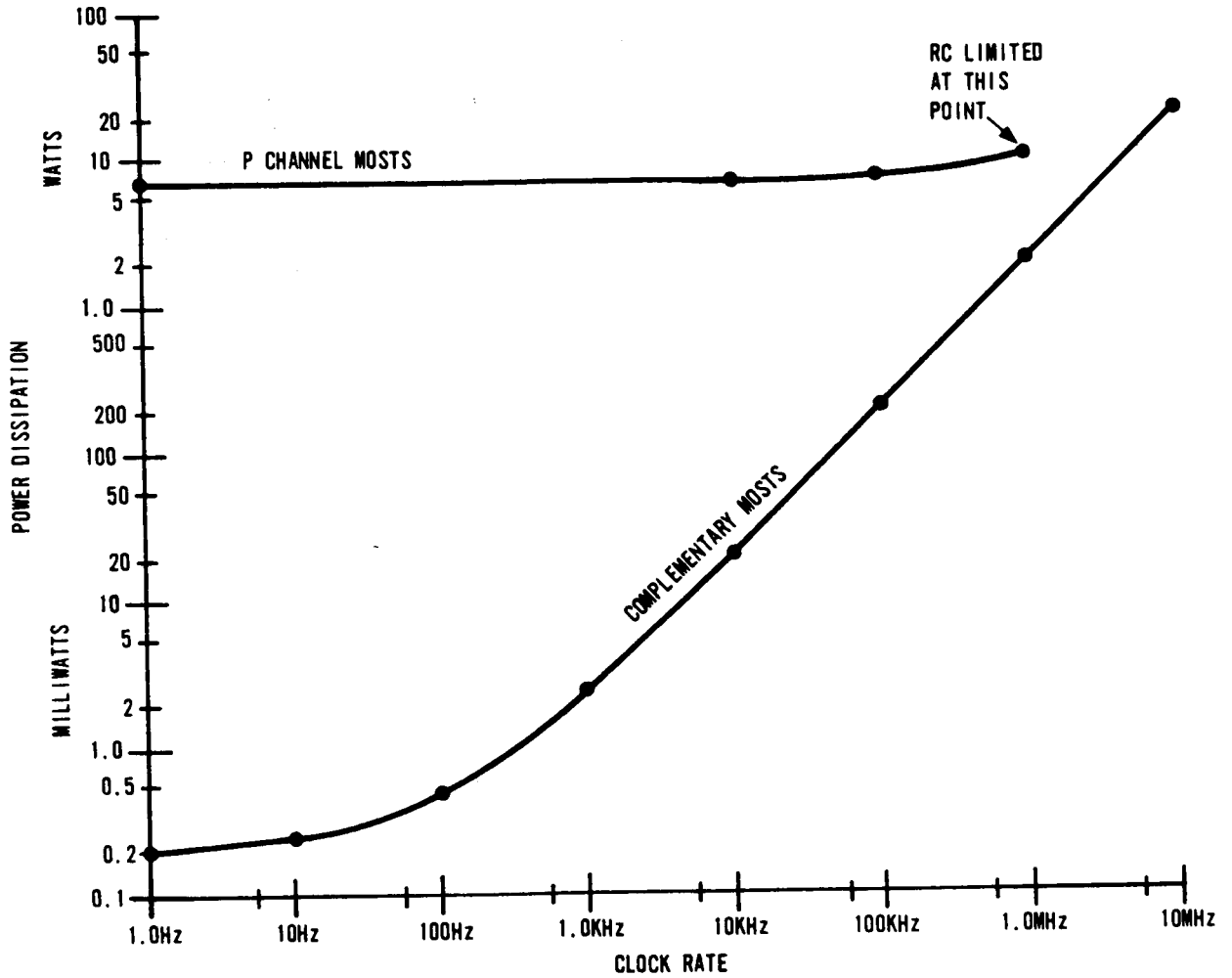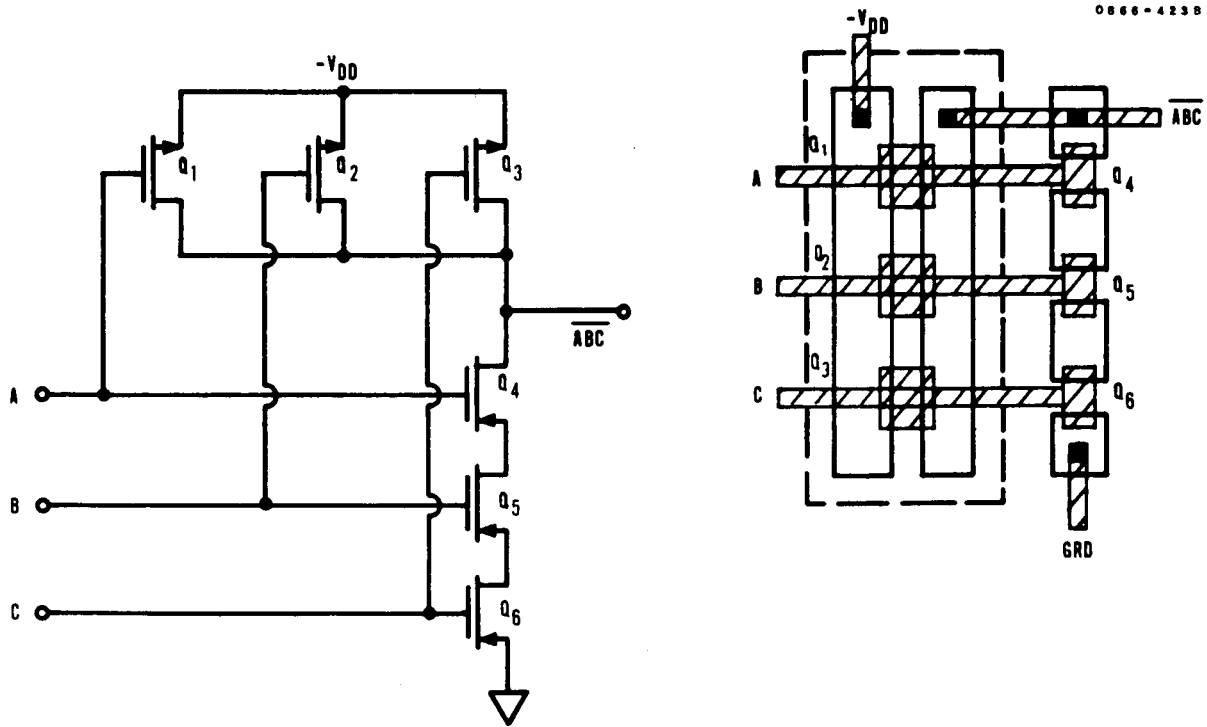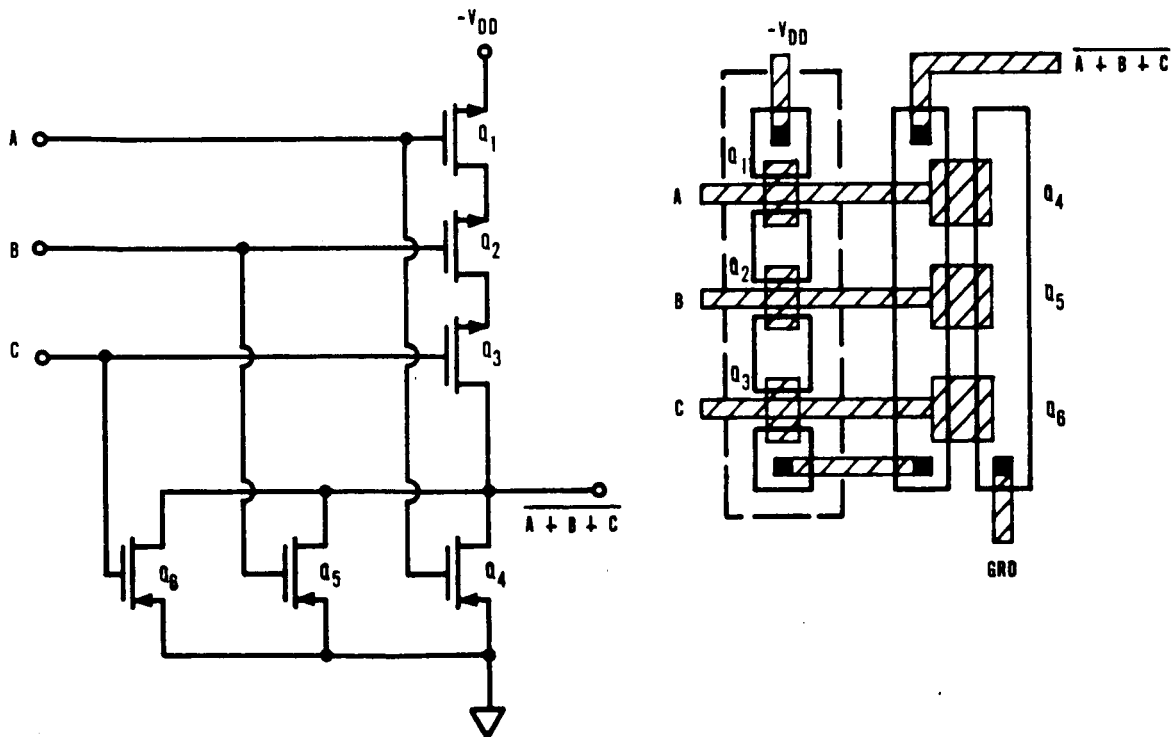
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FIGURE 54. COMPLEMENTARY MOST LOGIC POWER DISSIPATION AS A FUNCTION OF CLOCK RATE FOR A 1,000-CIRCUIT SYSTEM

(a) Complementary MOST NAND gate circuit and chip layout.

(b) Complementary MOST NOR gate circuit and chip layout.

FIGURE 55. COMPLEMENTARY N AND P CHANNEL MOST LOGIC MECHANIZATION

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