NAS 8-20514

ADDRESSABLE TIME DIVISION DATA SYSTEMS

FLYABLE PROTOTYPE EQUIPMENT

FINAL REPORT

NOVEMBER 1966

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GEORGE C. MARSHALL SPACE FLIGHT CENTER
HUNTSVILLE, ALABAMA 35812

Prepared by

MARTIN COMPANY
DENVER, COLORADO
AEROSPACE DIVISION OF MARTIN-MARIETTA CORPORATION

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CONTRACT NAS8-20514

DCN-1-6-41-51385(1F)

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GEORGE C. MARSHALL SPACE FLIGHT CENTER

HUNTSVILLE, ALABAMA 35812

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ADDRESSABLE TIME DIVISION DATA SYSTEM FLYABLE PROTOTYPE EQUIPMENT

FINAL REPORT

INTRODUCTION:

A study and breadboard program for the feasibility of an Addressable Time Division Data System was undertaken by the Martin Company during the period of July 1965 through March 1966 under MSFC-NASA contract No. NAS 8-20514. An operable breadboard and a final report (MARTIN CR-66-22) were submitted to NASA in March of 1966. At the conclusion of this program the contract was extended to cover the design of ten units of a flyable address identification module and one unit of a measuring source to monitor ten high-level data inputs. This report covers the design, construction, and testing of the prototype units.

SUMMARY

One measuring source (multiplexer) and ten separate address processors were designed and constructed to meet flight specifications per the requirement of ammended MSFC Contract NAS 8-20514. All of these items were tested for proper operation under normal ground environment conditions and a complete set of modules as assembled in the measuring source were subjected to various environmental tests. Specifically the measuring source was thermally tested, subjected to humidity, subjected to vibration, and evaluated in accordance with specific electro-magnetic interference requirements.

The operation of all modules appeared excellent from the very beginning of tests but there were some troubles with the power supply during tests. An initial power supply was encapsulated with a constructional high impedance short which could not be corrected so a new supply was built. The second power supply actually completed all tests but at the end of the temperature cycling a filter capacitor shorted. No design fault was found that explained the failure so a defective part must be assumed. A third power supply was constructed and the temperature cycle repeated twice without failure.

EMI tests revealed the need for further filtering of the input 28 volts to reduce the unit's potential as an interfering source at the 15 MHz to 50 MHz frequency range. The addition of two small ceramic capacitors at the input to the power supply alleviated this problem. While these capacitors were by necessity added external to the supply, future designs could incorporate these capacitors in the module.

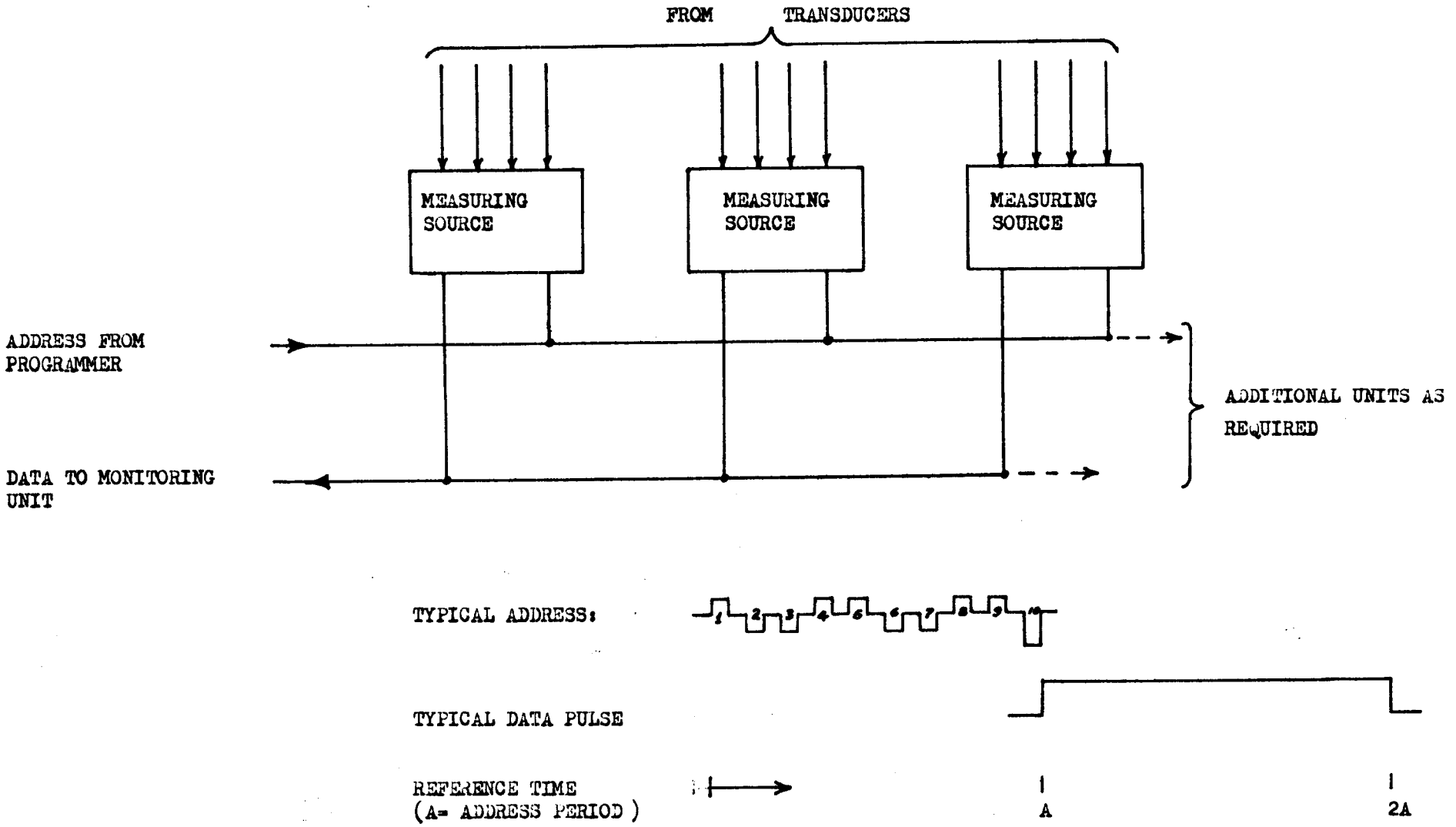
All performance of the measuring source appears to have equaled or exceeded the requirements of the specifications. Even the requirements for $\pm$ 10 mv $\pm$ 0.1% accuracy of data measurement was complied with as could be determined with the best instrumentation possible. In review, the program is considered to be a very successful demonstration of the distributed telemetry multiplexer concept where all multiplexers are interconnected to addressing and monitoring sources by a single address cable and a single data cable, respectively. The feasibility of such a system opens the door to the advent of very flexible instrumentation systems where instrumentation may be added or removed without much recabling or replanning.

I. ADDRESSABLE TIME DIVISION DATA SYSTEM DESIGN

Earlier study reports completely describe the Addressable Time Division Data System but a review appears in order. Figure No. 1 is a block diagram. The block diagram shows several measuring sources (otherwise called multiplexers). As shown by the diagram the measuring sources are addressed by a single address cable and commutate data from many transducers into a common data bus. Each measuring source functions as follows:

The address processor module receives a program of serial digital addresses from a specific programmer or a multipurpose computer. The addresses consist of ten binary bits of data where ones are represented by positive going pulses and zeros are negative going pulses. The tenth bit in each address is double amplitude for identification of an address completion. The address information is returned to zero voltage between each bit transition similar to the current wave-form of an RZ recording system. Therefore, the term bi-level RZ is used in describing the format hereafter. The address processor receives the addresses and stores each one of them for one ten-bit address period. If the stored address matches one of the diode decoders operating the commutating switches that switch will be closed and the related data transducer sampled. As the program of addresses is transmitted all of the commutating switches in the system will be addressed at the sample rate programmed for a complete cycle of the programmer.

The commutating switches simply perform time sampling of transducers as they are addressed. Data appears as a PAM pulse equal to an address time period in length and equal to the data amplitude in height within the linear range of the switch. The switches serve to isolate transducers from



BLOCK DIAGRAM

ADDRESSABLE TIME DIVISION DATA SYSTEM

FIGURE NO. 1

each other, and from the data bus except at the proper time of interrogation.

An amplifier module is used to buffer the outputs of the commutating switches from the data bus. High input impedance is provided to the data and low drive impedance is provided for the line. The amplifier module also contains a data bus switch which is open unless a commutating switch related to that amplifier is addressed. This isolates all measuring sources from the data bus except for the one through which data is being sampled.

The power supply provides power at correct voltages for the modules. Also, proper ground isolation is provided for low noise operation of the system.

The design and more detailed operation of each module is described in the following sections.

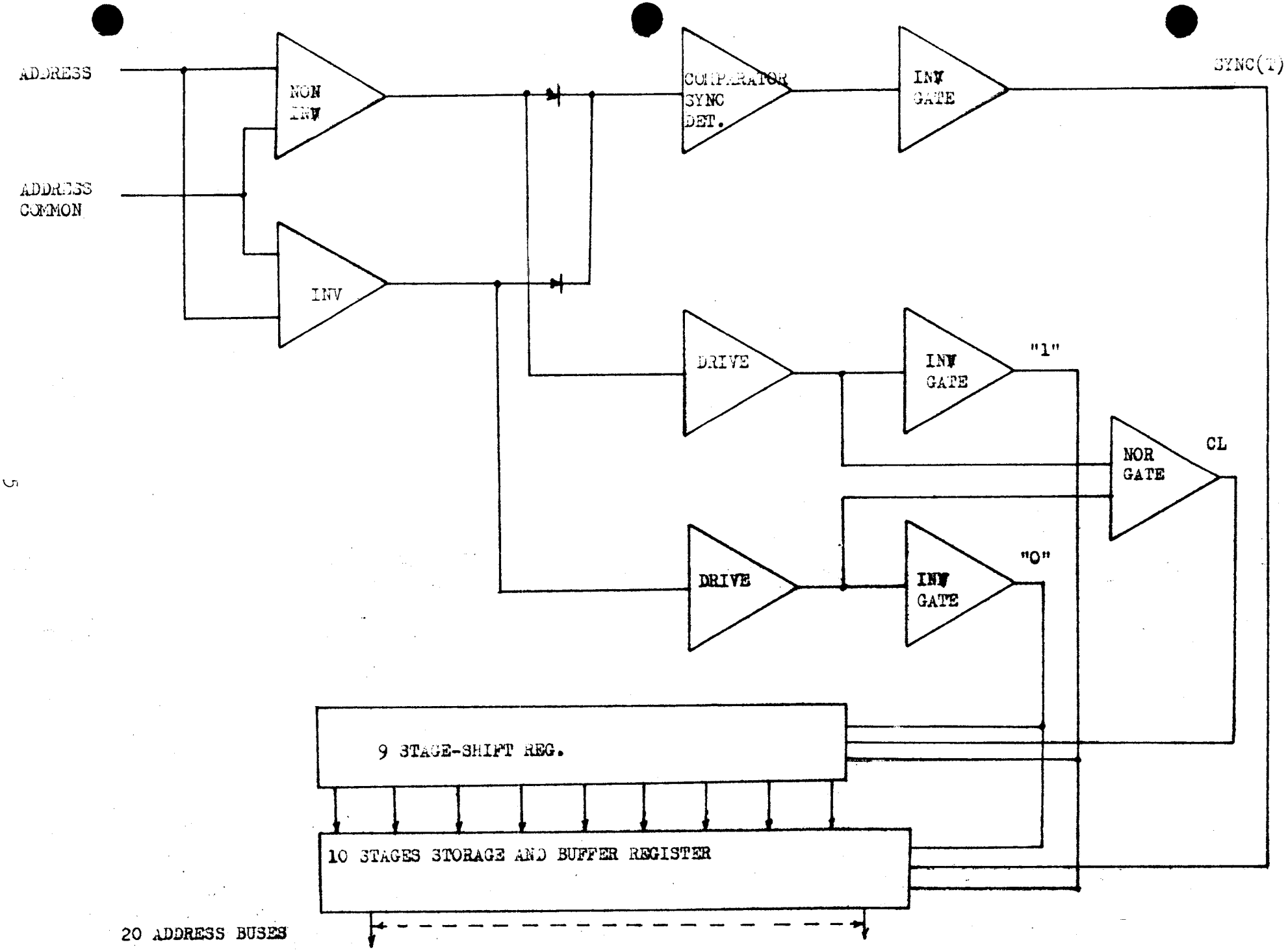
II. ADDRESS PROCESSOR MODULE

A. Operation.

Figure No. 2 is a block diagram of the address processor. The addresses are fed into two amplifiers, one inverting and one non-inverting. The output of the non-inverting amplifier is used to obtain ones. The output of the inverting amplifier provides zeros. Each amplifier drives a transistor buffer stage to convert the one and zero outputs to micro-logic reference levels. Binary summation of the zeros and ones at the micro-logic level provides a clock for timing purposes. In addition, the outputs of the amplifiers are summed through diodes to the input of a threshold amplifier. Consequently, either positive going or negative going double-amplitude pulses are detected for synchronization. Ones and zeros are shifted into a 9 bit serial shift register. Upon the receipt of the 10^{th} or sync pulse the nine bits in the serial register plus the 10^{th} bit are shifted into a ten bit storage register. The contents of the storage register are nanded at a two-bit level by buffer-nand circuits to provide twenty decoder buses. All possible ten bit addresses may be decoded by the use of 5-diode matrices connected properly to the buses. Each group of four buses represent all combinations of each two-bit groupings of the address. An address is held in the storage register for the period between two consecutive decode pulses. The 5-diode matrix decoders are not a part of the address processor but must be provided for each data point to be sampled.

B. General Electronic Design.

The criteria chosen for the design were simplicity, compactness, low power and high reliability - not necessarily listed in the order of importance. Since these criteria are in many respects conflicting, compromises in their usage are necessary. The compromises are frequently a matter of



BLOCK DIAGRAM ADDRESS PROCESSOR

FIGURE NO. 2

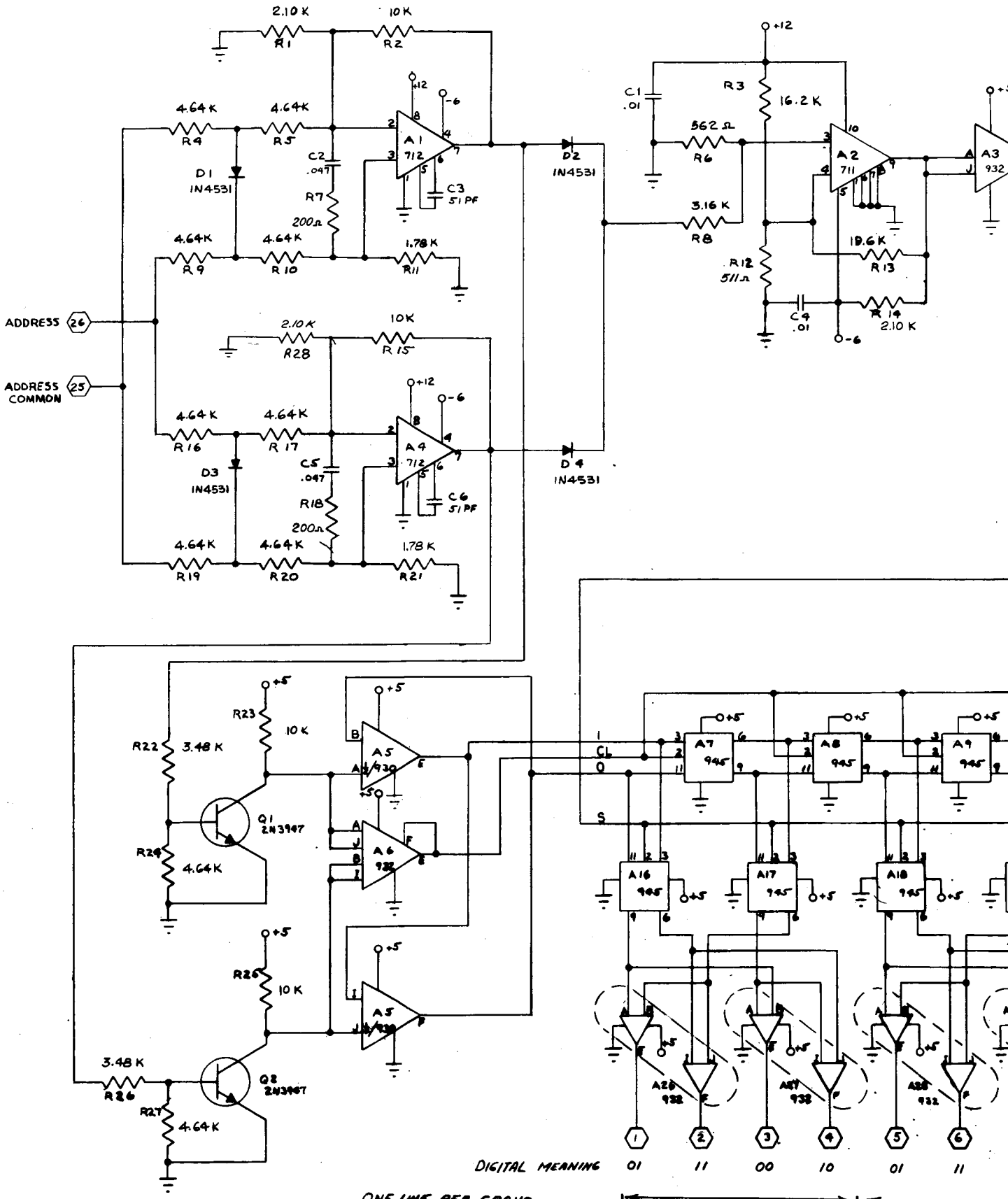
personal judgment and subject to revisions as experiences in the use of the end item may dictate.

To achieve simplicity and compactness integrated circuits are employed to the greatest extent consistent with reasonable development time and good economics. Lower power could be achieved with discrete components. Smaller size could be achieved by further application of integrated circuits. Reliability comparisons for the extremes in design is difficult. Generally, because of the reduced number of electrical connections the integrated circuits may be considered more reliable. Figure No. 3 is a schematic diagram of the address processor.

C. Address Input Circuitry.

The simplest form of input circuitry to detect and separate the ones and zeros in the address would be a transformer. The common mode rejection of this device could also be excellent but the design of a transformer for a large range of clock frequencies is almost impossible. Therefore, differential amplifiers were chosen instead of a transformer. The use of amplifiers, one inverting and one non-inverting, provides fullwave detection, impedance matching, and common mode noise immunity. The original breadboard used integrated amplifiers manufactured by Motorola, but the frequency response was a little lower than desired. Prior to the prototype design other amplifiers were evaluated and the Fairchild μA702A (now μA712) performed the best.

The overall input to output gain of the amplifier design is approximately one with micro-logic input voltage levels for the address signal. The μA712 amplifiers can be fed back to unity gain but the input bases are limited to +1.5 volts. With five volt input pulses and unity gain this requirement is violated. Consequently, the amplifiers A1 and A4 are fed


2.10 K
R1
10 K
R2
+12
-6
4.64 K
R4
4.64 K
R5
A1
712
C2
.047
D1
IN4531
R7
200Ω
C3
51 PF
4.64 K
R9
4.64 K
R10
1.78 K
R11
D2
IN4531
C1
.01
R3
16.2 K
562 Ω
R6
A2
711
A3
932
3.16 K
R8
R12
511Ω
19.6 K
R13
C4
.01
R14
2.10 K
ADDRESS
26
ADDRESS
COMMON
25
2.10 K
R28
10 K
R15
4.64 K
R16
4.64 K
R17
A4
712
D3
IN4531
C5
.047
R18
200Ω
C6
51 PF
D4
IN4531
4.64 K
R19
4.64 K
R20
1.78 K
R21
+5
R23
10 K
R22
3.48 K
Q1
2N3907
R24
4.64 K
A5
930
A6
932
R26
10 K
3.48 K
R26
Q2
2N3907
R27
4.64 K
A5
930
C
O
S
A7
945
A8
945
A9
945
A16
945
A17
945
A18
945
A26
932
A27
932
A28
932
1
2
3
4
5
6
DIGITAL MEANING
01
11
00
10
01
11
ONE LINE PER GROUP
TO EACH DIODE MATRIX
TO FORM AN ADDRESS

HIGHEST REFERENCE DESIGNATION USED		REFERENCE DESIGNATIONS NOT USED	
R28	A35		
C6			
D4			
Q2			

REFERENCE DRAWINGS

NAS8-20514 -21
-23
-31
-32
-33
-34
-35
-36
-1

REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPROVED
A		ADDED REF. -1	8-16	J.E.B.
B		CHANGED R21 TO 1.78K, CHANGED R2 TO 10K ADDED R28. REVERSED DIRECTION OF D3.	11/4/66	Goodwin

E
F

27 SYNC.
24 +12 VDC
23 +5 VDC
22 -6 VDC
21 GND

DIMENSIONING REF. MIL-STD-8
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
AND ARE AFTER PLATING
TOLERANCES ON: DECIMALS

FRACTIONS	.X	.XX	.XXX	ANGLES
±1/32	±.1	±.03	±.010	±1/2°

MACHINED SURFACES
REF: MIL-STD-10 ✓

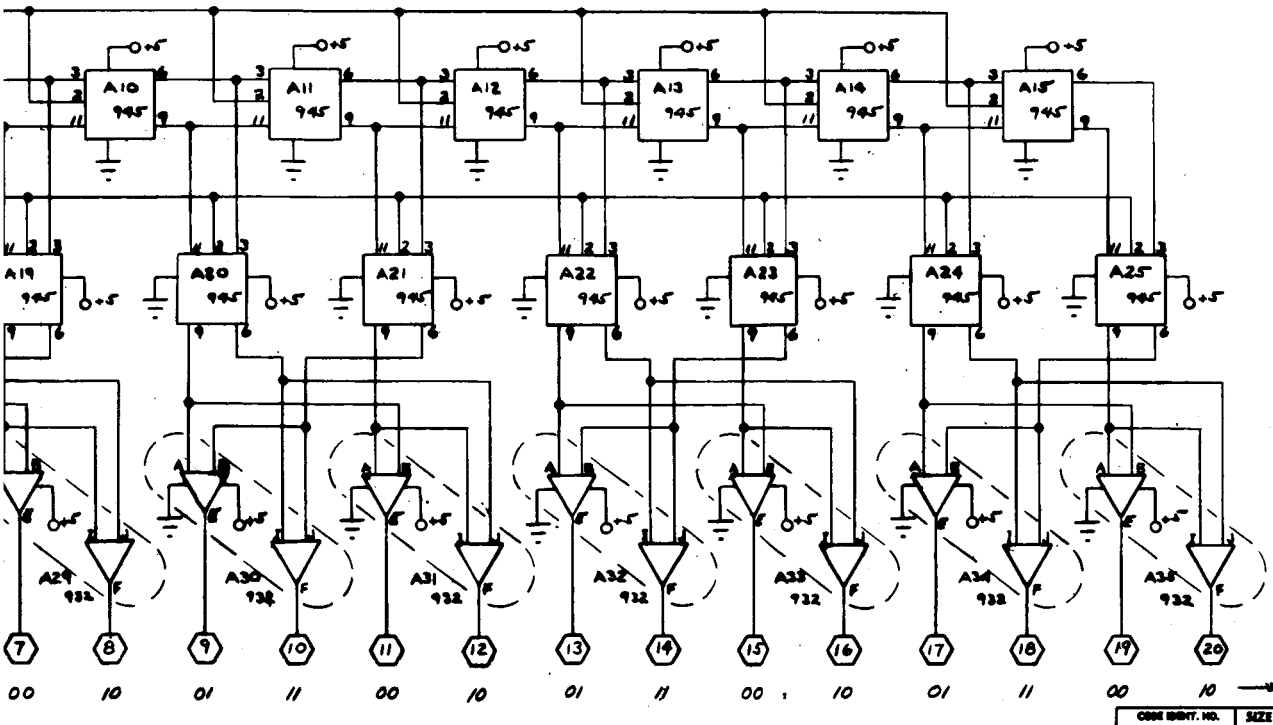
MIL-I-6900 STATUS
INTERCHANGEABLE
REPLACEABLE
UNCONTROLLED

DRAWN BY W.M. Caudle DEPT 0452 DATE 6/14/66
CHECKER W.M. Caudle 0452 7/15/66
STRESS ENGR.
WT. ENGR.
MATL. ENGR.
RELIABILITY
QR. ENGR.
PROJECT PROGRAM MGR. J. E. Goodwin
CUST. REP.

MARTIN COMPANY
THE AEROSPACE DIVISION OF MARTIN MARIETTA CORPORATION
FRIENDSHIP INTERNATIONAL AIRPORT, MARYLAND

SCHEMATIC DIAGRAM (ADDRESS MODULE)

CODE IDENT NO. 38597 SIZE
SCALE — SHEET



CODE IDENT. NO. 38597 SIZE D NAS 8-20514-22
CHG. SCALE SHEET

 Figure No. 3

back for a gain of six and the input signal is divided by six. This feedback arrangement reduces the overall dc zero stability with temperature variations but the design is still quite adequate.

The input amplifier resistors are divided into two parts with diode clamps D_1 and D_3 between inputs to clamp reverse input voltage. This is necessary to prevent saturating the amplifiers in the negative direction - the amplifiers being limited to about 2.5 volts in their negative output voltage swing with the specified load and no "pull down" resistor. The amplifiers are operated with differential inputs to minimize ground loops in a system installation and to minimize noise problems. Common mode rejection is much dependent upon input impedance matching. The use of 1% resistors will provide from 20 to 40 db rejection which is considered adequate for the application.

Each amplifier drives a normally cutoff transistor (Q_1 and Q_2) to saturation to provide zero and one drive circuits at voltage levels from 0 to +5 volts. Integrated circuit gates A_5 and A_6 are driven by the transistors to provide positive going zero and one and clock outputs.

D. Address Sync Detector.

The sync detector A2 is a Fairchild μA711 integrated circuit designed for fast recovery from saturation bias. The μA711 is a dual amplifier but only one half is used. While this appears as an inefficient application of the device, the single amplifier μA710 version does not have as high an output voltage swing and the μA711 is considered preferable. The threshold bias and positive feedback are set to saturate the amplifier in the positive direction. The amplifier has a differential input and the positive feedback and threshold are summed at the non-inverting input and the address signal is applied from the input amplifiers through two diodes as a positive

going waveform to the inverting input. When the address pulse (sync) is large enough the amplifier changes from positive to negative saturation. The positive feedback provides some hysteresis so that the amplifier will not turnoff until the input signal drops well below the threshold. This gives added noise immunity for the sync pulse. The output of the sync amplifier drives integrated circuit gates (A_3) to provide positive going sync pulses at the integrated circuit voltage level (0 to 5 volts).

E. Shift & Storage Registers and Decode Bus Drivers.

The shift and storage registers and the decode bus drivers are entirely integrated circuits. The registers A7 through A25 consists of J-K flipflops type 945 and the bus drivers A26 through A35 are 932 buffer-gates. The 900 series integrated circuits originally developed by Fairchild are made by various companies and different prefixes for each manufacturer will appear before the 900 series number.

The data is clocked into the serial register redundantly with information being supplied to both set and reset inputs. The data is then transferred in parallel from the serial to storage register. Really the storage register consists of ten independent flip-flops.

F. Address Processor Mechanical Design

While general principles must be followed in the mechanical design of an encapsulated electronic circuit the shape and type of component arrangement is much to the discretion of the designer. The design chosen here consists of both cordwood and printed board construction. All components are arranged in welded cordwood except integrated circuit flat packs which do not easily lend themselves to welded cordwood.

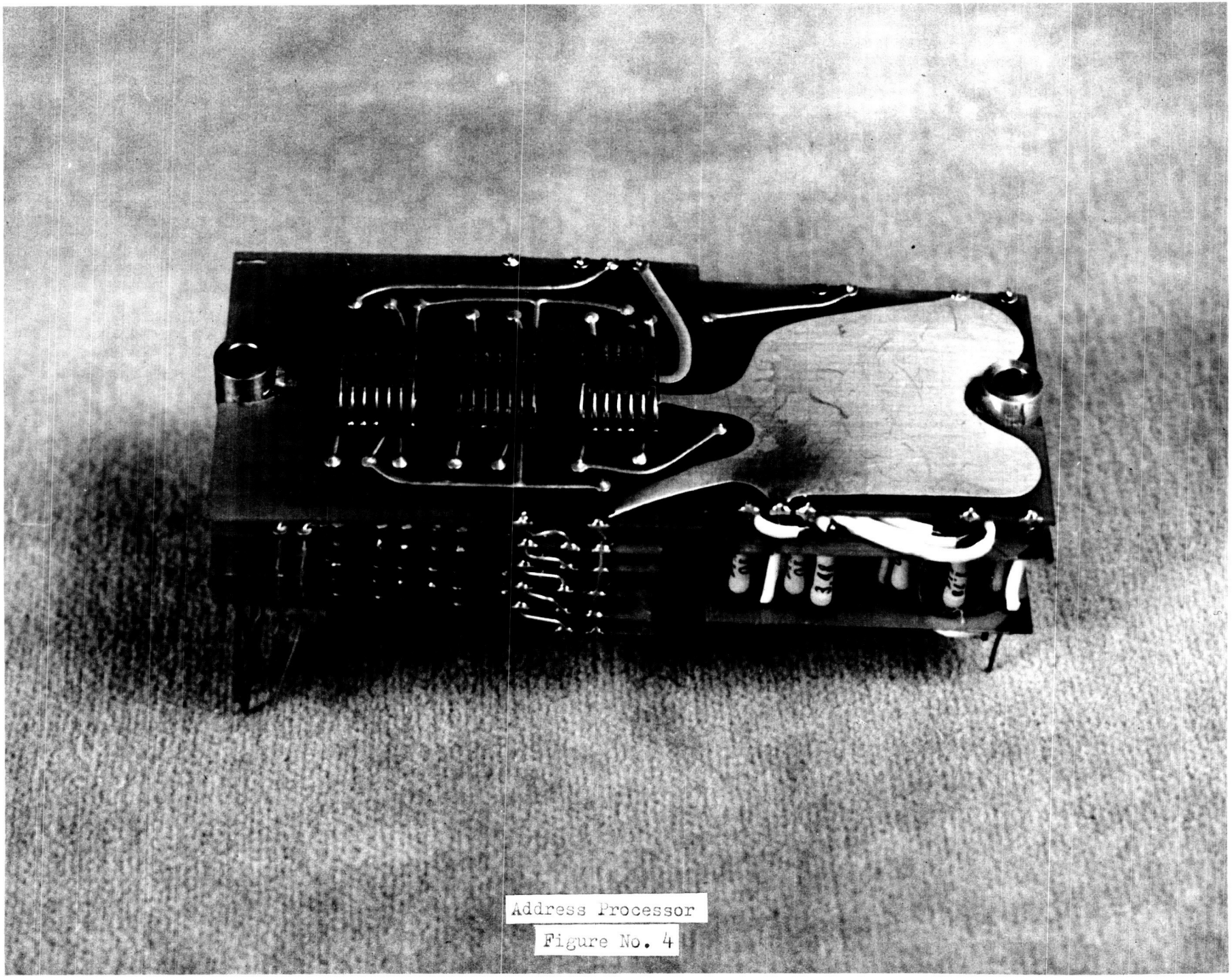
Cordwood construction consists of parts located by two position boards. Welding of the parts leads to interconnecting nickle ribbons on the outside of the position boards forms the circuit. A stack of six pc boards are

located at one end and tied into the cordwood submodule. These six boards contain all of the integrated circuits interconnected by buses inserted in edge plated slots in the boards. The slots were intended to facilitate assembly and repair, but the difficulty in production of the slots probably more than offsets gain. Ordinary plated-thru holes are recommended for the future.

There is a heat sink in the cordwood area to distribute heat to one mounting bushing and all flat-packs have heat sinks to remove heat to the other mounting bushing. This arrangement allows the use of low density eccosphere filled potting of the module. Figure No. 4 shows a module prior to potting.

G. Address Processor Specifications.

address input impedance:	7 K ohms approx.
address pulse amplitudes:	ones + 1.8 to 2.2 volts
	zeros - 1.8 to 2.2 volts
	one sync + 3.7 to 4.4 volts
	zero sync - 3.7 to -4.4 volts
number of decoder loads:	32
address bit frequency:	100 H to 1 MH
Supply voltages:	+5 volts $\pm$ 10% @ 300 ma
	-6 volts - 0, + 1 volts @ 20 ma
	+12 volts - 1 volt, + 0 @ 20 ma



Address Processor

Figure No. 4

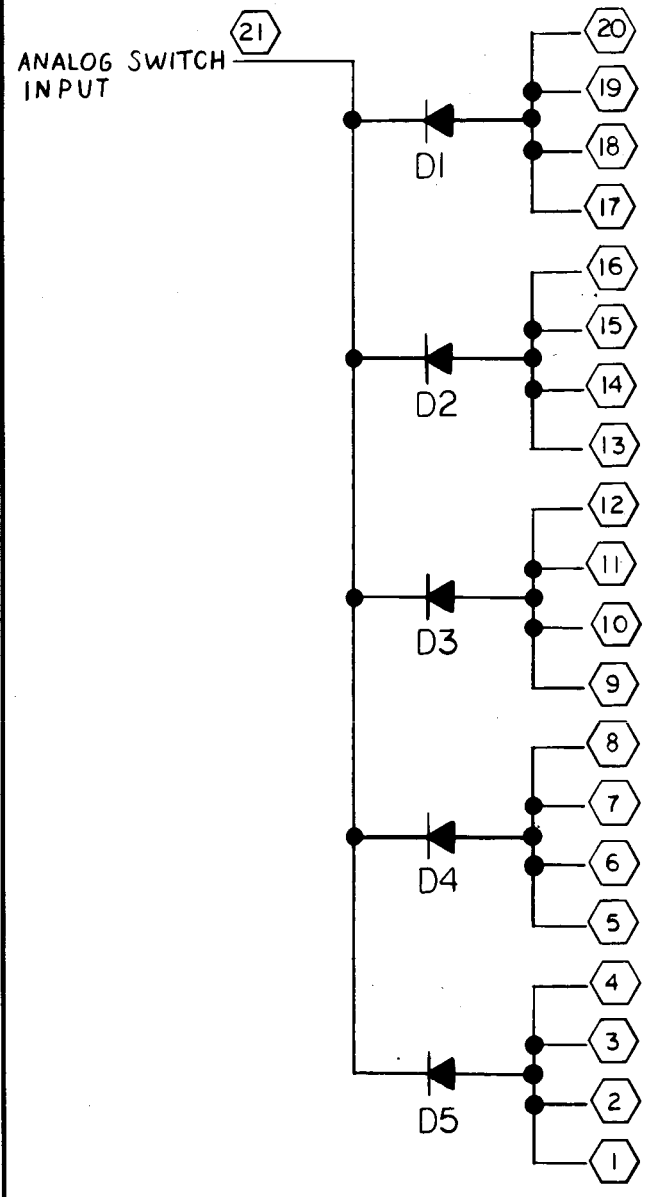
III. DIODE DECODERS.

A. Electronic Design and Operation.

Figure No. 5 is a basic achematic of a diode decoder module. The module consists of five diodes welded together as shown. It will be noted that each diode is shown connected to four decode buses. As previously implied each group of four buses represent all of the possible digital combinations of two stages of the address storage register. For any given 10-bit address each diode must be connected to only one bus so the means of address selection is to cut all bus connections to each diode except one. More precisely each group of four buses represents 00, 10, 01, and 11 so if a code of 0000110101 is desired only the 00 connection is left in each of the first two diodes, the 11 connection in the third and the 01 for the fourth and fifth diodes. For proper codes all inputs to a matrix must go low.

B. Mechnical Design.

The modules are arranged with diodes welded together on end. The anode end is connected to U-shaped wires which form four leads to be plugged into sockets in the decoder buses. The cathodes are connected to a common bus which bends to form another pin to plug into a socket in the decoder output bus. All buses and sockets are on the mother board to be described later. The corners of the U-shaped wires are all exposed for cutting in the finished module to determine the codes, the finished module is encapsulated in a poly urethane material. Figure No. 13 is a photograph of the measuring source which shows ten of these modules plugged in the mother board.



ALL DIODES-IN4531

SUPPLEMENTARY INFORMATION	
FIRST USED NAS 8-20514-1	
NEXT ASSEMBLY	REFERENCE
NAS 8-20514-81	

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND ARE AFTER PLATING
TOLERANCES ON:

FRACTIONS	DECIMALS .X	DECIMALS .XX	DECIMALS .XXX	ANGLES
± 1/32	± .1	± .01	± .010	± 1/2°

MACHINED SURFACES
REF: MIL-STD-10 ✓

MIL-I-8500 STATUS

INTERCHANGEABLE	
REPLACEABLE	
UNCONTROLLED	

DRAWN BY R. G BURNS DEPT. 0452 DATE 8-3-66
CHECKED 0452 8-12-66
STRESS ENGR.
WT. ENGR.
MATL. ENGR.
RELIABILITY
QR. ENGR.
PROJECT 8/17/66
CUST. REP.

AEROSPACE DIVISION - DENVER
P. O. Box 179 Denver 1, Colorado
MARTIN MARIETTA CORPORATION

DIODE MATRIX SCHEMATIC DIAGRAM

CODE IDENT NO.	SIZE	
38997	C	NAS 8-20514-82
SCALE NONE		SHEET

Figure No. 5

C. Address Codes.

The ten diode decoders supplied with the measuring source are composed of the codes listed below. The first bit listed from the left is the sync bit.

1011100001

0001010001

1101110001

1111110101

0101100001

1011011001

1001100101

0001001101

0010110101

IV. ANALOG SWITCH MODULES

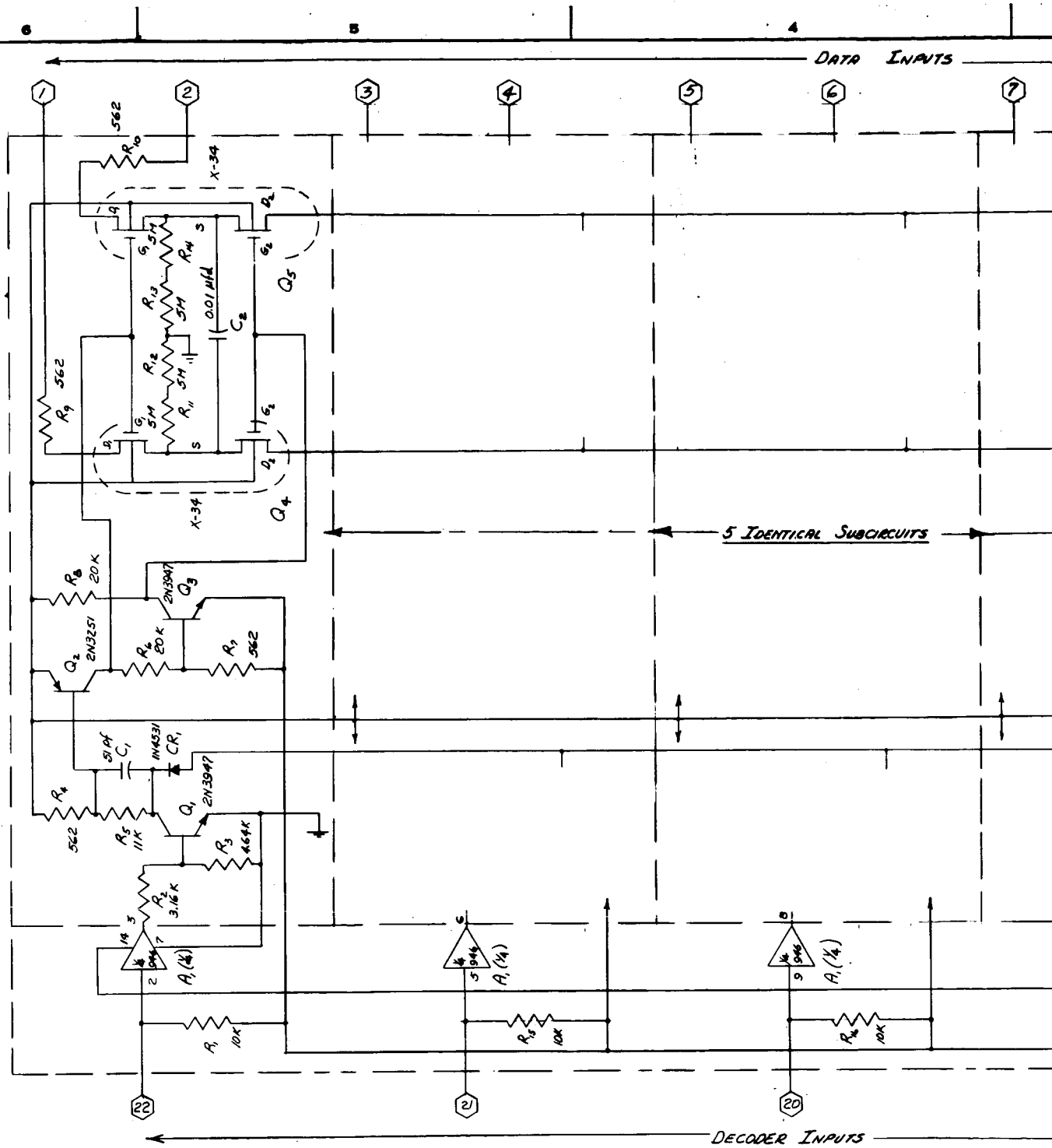
A. General Electronic Design and Operation.

The commutating switches used in this system are all intended to perform linear or analog functions and are hereafter referred to as analog switches. Commutation in the past has been done by various arrangements of mechanical and electronic switches. The switches chosen for this program are the relatively new insulated gate (MOS) transistors. These switches require low drive power, have high off to on impedances ratios, contribute low offset voltage errors and are normally "off" devices. They are physically small and require only the simplest of drive circuitry. Circuit operation is best defined along with circuit design as is done in the following paragraph.

B. Circuit Design and Operation

Figure No. 6 is a schematic diagram of the analog switch modules. Two modules are employed in the prototype measuring source. Each module contains five switch channels which could have been contained in a single module but physical proportions would not have matched other module sizes. Operation of each switch channel is as follows:

A transducer (or other data source) charges capacitor C_2 through one half each of switches Q_4 and Q_5 which are respectively located in each of the two tranducer lines. When a correct address is received at the decoder input from the decoder matrix (via address processor), gate A_1 biases Q_1 on, with resulting consecutive turn on of Q_2 and Q_3. The turn on of Q_2 turns off the input halves of Q_4 and Q_5 thus disconnecting C_2 from the transducer. This disconnects C_2 form all input common mode voltages leaving C_2 charged to the transducer voltage. As the input halves of the switches open the



A_2 Q_5 C_4 R_{18}			- 76 - 75 - 74
		NASB-20514-71	NASB-20514-73
		NEXT ASSEMBLY	REFERENCE
		FIRST USED	NASB-20514-1
HIGHEST REF. DESIGNATION	REF. DESIGNATION NOT USED	SUPPLEMENTRY INFORMATION	

output halves of Q_4 and Q_5 are turned on by Q_3 thus connecting the capacitor C_2 to the amplifier input leads. Consequently the amplifier can now sample the stored value of the transducer voltages without being connected to external ground loops. The capacitor is sampled for an address period and reconnected to the transducer at the end of the address. All ten channels are alike and may be addressed in any sequence but no two simultaneously.

The diode CR_1 is connected to an "OR" bus to provide a negative going pulse for any correct address; this pulse operates a one-shot multivibrator in the amplifier as explained in the amplifier section.

C. Mechanical Design.

As in the case of the address processor, the analog switch module is a combination of printed circuit and welded cordwood modules. The integrated circuit flat packs are soldered to printed circuit boards and the discrete parts are assembled in five identical submodules. Figure No. 7 is a photograph of the module prior to potting. The finished module is encapsulated in eccosphere filled epoxy.

D. Specifications

Sample voltage range -5 volts to +20 volts (-10 with reduced accuracy)

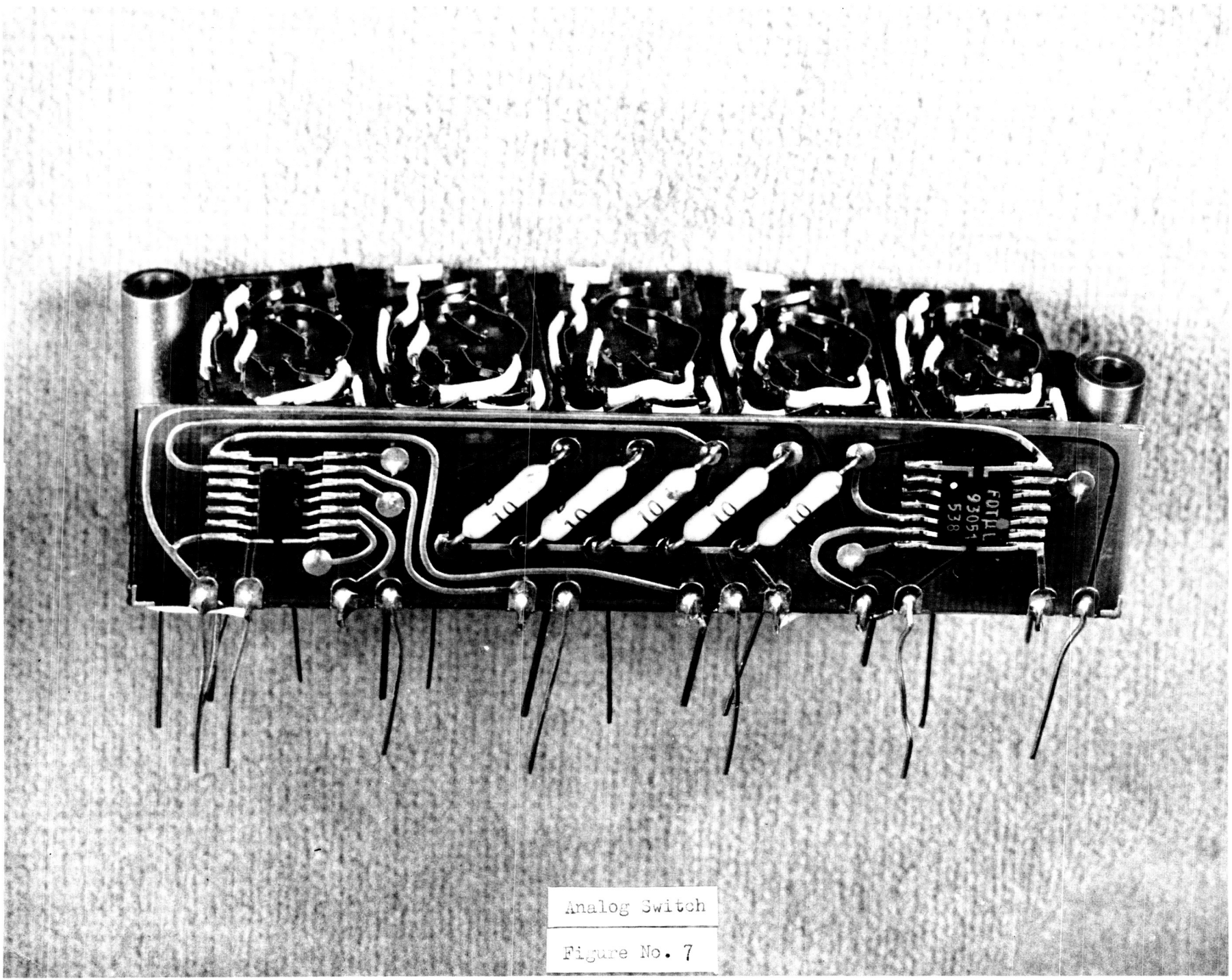
Sample frequency-1 kHz max with 10 K ohm source for ± 0.1% system accuracy - faster for reduced accuracy.

Sample time - 25 micro-seconds

Power supply: 5 volts ± 10% @ 16 ma

20 volts ± 10% @ 5 ma

-15 volts ± 10% @ 3 ma



Analog Switch

Figure No. 7

V. AMPLIFIER MODULE

A. Circuit Design and Operation

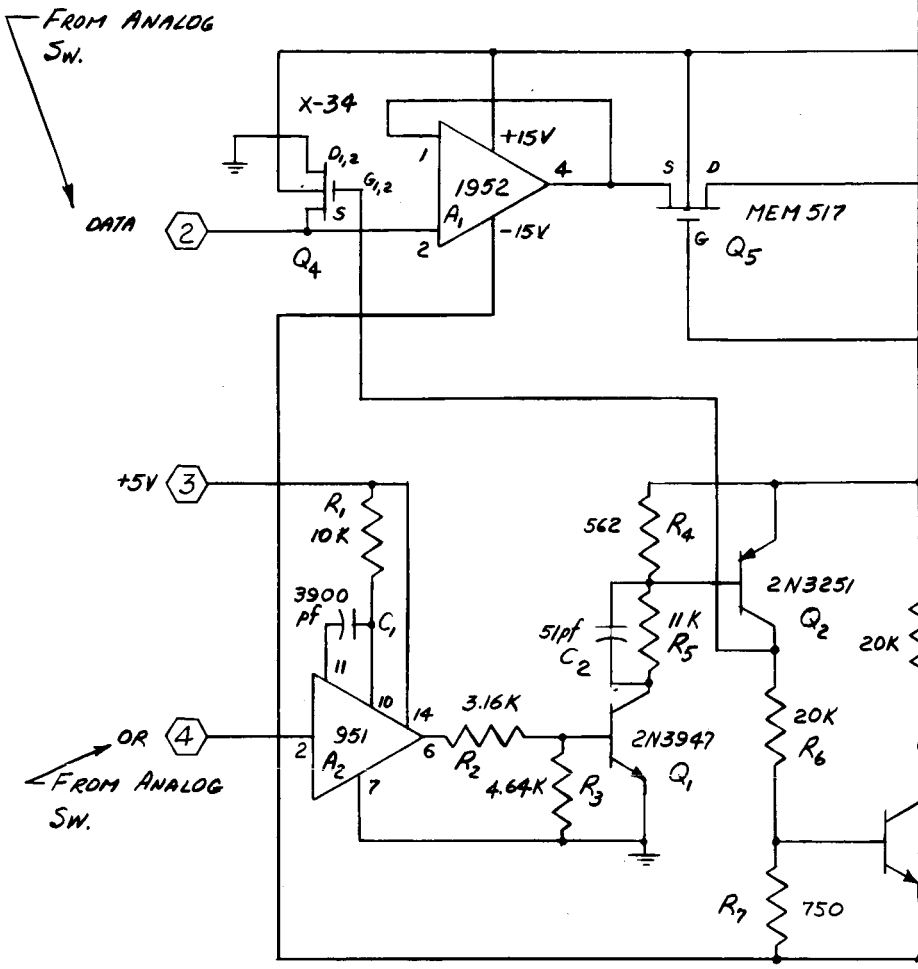
The amplifier module is constructed in accordance with the schematic diagram shown on Figure No. 8. The module contains not only an amplifier but an input shorting switch, a data bus disconnect switch and a multivibrator timing and switch driver circuit.

The amplifier A_1 is a discrete component submodule model No. 1952, manufactured by Burr-Brown. The internal schematic of this amplifier is not available but the device consists of an FET input stage and transistor output stages. This amplifier is designed for use with 100% negative feedback; that is, the inverting input can be connected to the output. This connection assures an overall unity gain for the application herein. The feedback not only stabilizes the amplifier gain but assures extremely low dc drift and high input impedance for the non-inverting input.

For the amplifier to have low dc-drift and offset the input impedances of the inverting and non-inverting inputs should be nearly equal. With 100% negative feedback, however, the non-inverting input impedance is high and the inverting input impedance is equal to the amplifier output impedance, which is low. If the non-inverting input is ground except for sampling periods the drift of the amplifier will approach a minimum. Therefore, MOS, Q_4 is a shorting switch normally grounding the non-inverting input of the amplifier. Q_4 is opened for data sampling periods and data is fed into the amplifier at the non-inverting input.

Since a measuring source may be used with other measuring sources connected to the same data bus a normally open switch "MOS" Q_5 connects the output of the amplifier to the data bus. The switch is closed only during sampling periods.

HIGHEST REFERENCE DESIGNATION
R_8
C_4
A_2
Q_5



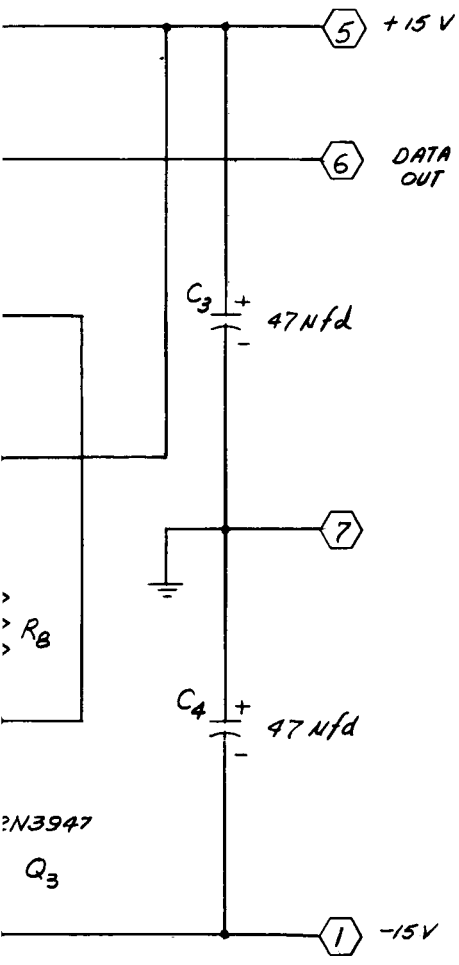
NCE	REF. DESIGNATION NOT USED

REFERENCE DRAWINGS

NASB-20514-1
NASB-20514-51

REVISIONS

SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		CHANGED C_3 & C_4 FROM 4.7 μfd TO 47 μfd	11/7/66	Goodwin
B		R7 WAS 562 Ω	11/19/66	Wilson



DIMENSIONING REF. MIL-STD-8 UNLESS OTHERWISE SPECIFIED				
DIMENSIONS ARE IN INCHES AND ARE AFTER PLATING				
TOLERANCES ON: FRACTIONS	DECIMALS .X	.XX	.XXX	ANGLES
±1/32	±.1	±.03	±.010	±1/2°
MACHINED SURFACES REF: MIL-STD-10	✓			
MIL-1-8500 STATUS				
INTERCHANGEABLE				
REPLACEABLE				
UNCONTROLLED				

DRAWN BY Goodwin	DEPT.	DATE 7-30-66
CHECKED BY Mc Candlish		8-12-66
STRESS ENGR.		
WT. ENGR.		
MATL. ENGR.		
RELIABILITY		
GR. ENGR.		
PROJECT E. E. Goodwin 8/17/66 Program Mgr.		
CUST. REP.		CNG.

MARTIN COMPANY
THE AEROSPACE DIVISION OF MARTIN MARIETTA CORPORATION
FRIENDSHIP INTERNATIONAL AIRPORT, MARYLAND

AMPLIFIER SCHEMATIC DIAGRAM (MEASURING SOURCE)

CODE IDENT NO.	SIZE	
38597	C	NAS8-20514-52
SCALE		SHEET

FORM DEN 081626 (1-63)

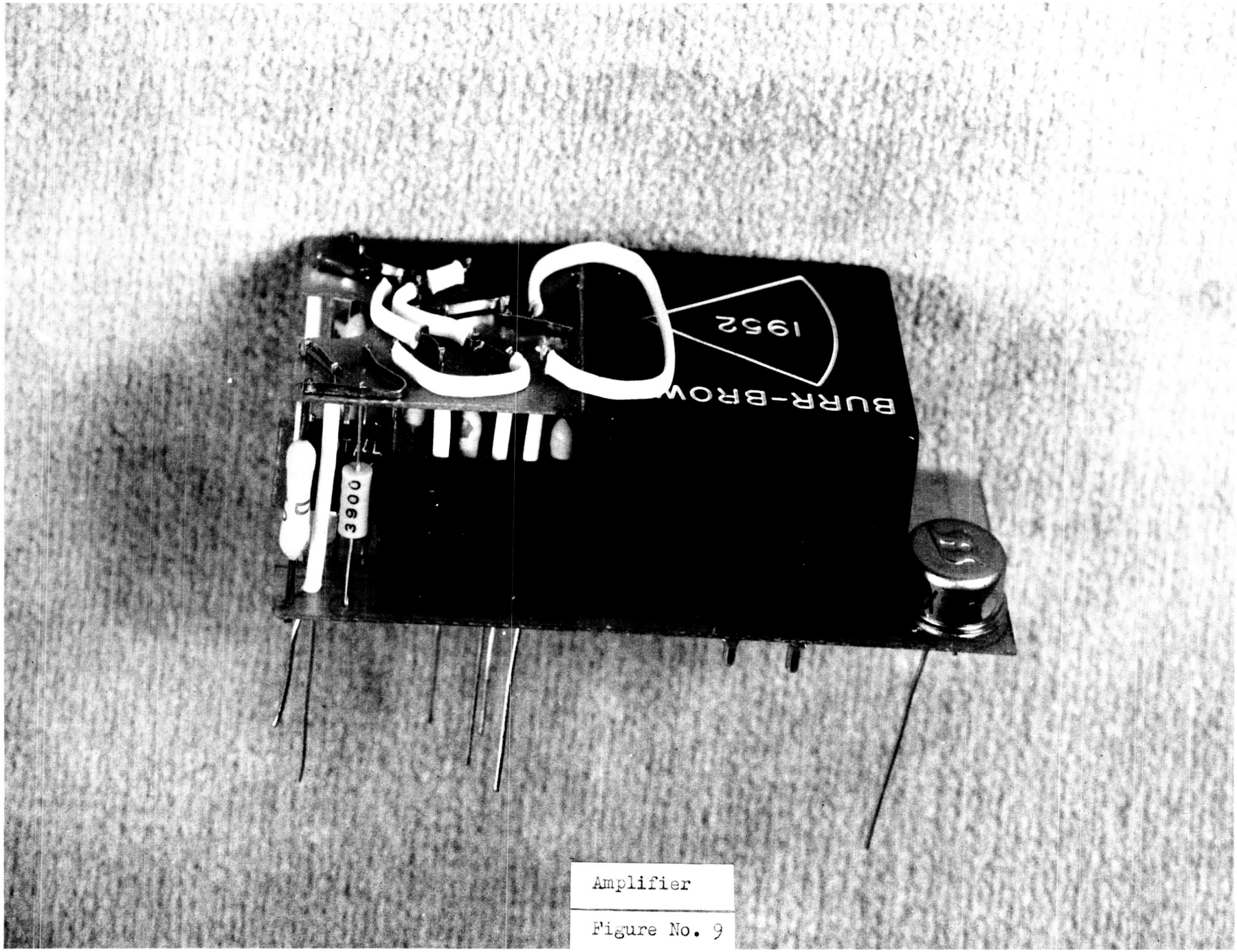
Control of the switching of shorting switch Q_4 and line switch Q_5 is performed by a Fairchild 951 one shot multivibrator A_2 and transistors Q_1, Q_2, and Q_3. When a correct address is present for any of the analog switches the pulse previously described present on the "or" bus from the analog switch modules will trigger the "one shot". The one shot saturates Q_1, Q_2 and Q_3 thus turning off Q_4, and turning on Q_5. The sample time determined by the "one shot" can be set to approach the length of an address pulse, but by making this period slightly shorter than the minimum address time ever encountered, switch Q_4 can serve to also dump the sample capacitor, thus eliminating possible feed back of current from a sampling capacitor into the transducer. The multivibrator also establishes a constant sample period for the system regardless of the programmer clock frequency. For this design the period is about 25 micro-seconds which limits the system clock rate to about 350 KC (10 bits = 28.5 micro seconds for an address time).

B. Mechanical Design.

Construction of the amplifier module is strictly welded cordwood with all of the parts arranged between two position-boards. Figure No. 9 is a photograph of the assembled module prior to potting. The finished module is potted in eccosphere-filled epoxy.

C. Specifications.

Input impedance	10^{10} ohms
Input voltage	$\pm$ 10 volts
Output voltage & current	$\pm$ 10 volts @ 20 ma
Slew rate	10 volts per micro-second
Power requirements:	+ 15 volts 12 ma typical - 15 volts 9 ma typical + 5 volts 7 ma typical



Amplifier

Figure No. 9

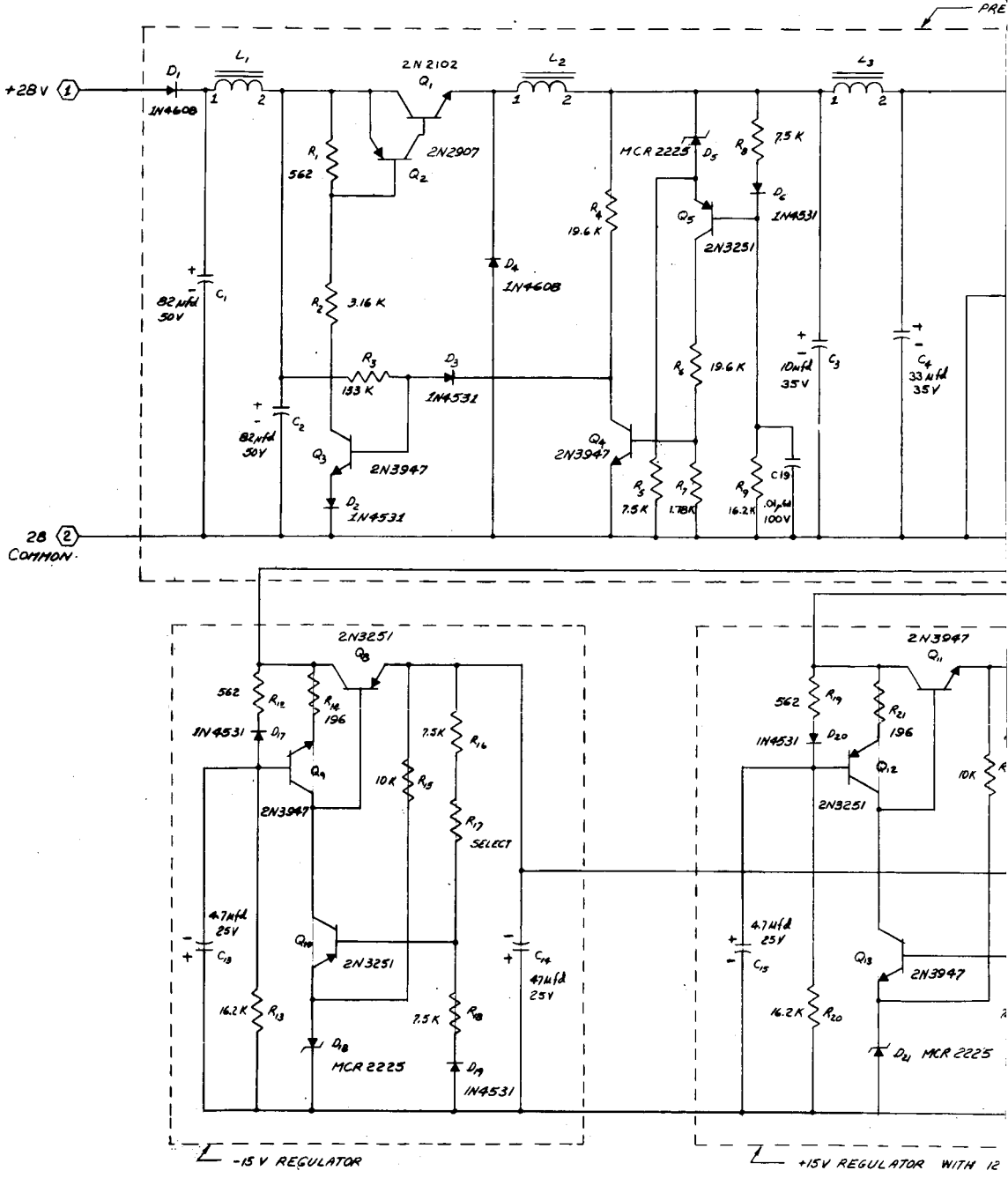
VI. POWER SUPPLY

A. General.

At first appearances the power supply shown by the schematic diagram in Figure No. 10 consists of a conventional series pre-regulator, a dc to dc converter, secondary rectifiers and filters and some secondary regulation. On closer analysis, however, it will be seen that the pre-regulator is not a conventional series regulator. The pre-regulator will be described first.

B. Pre-regulator.

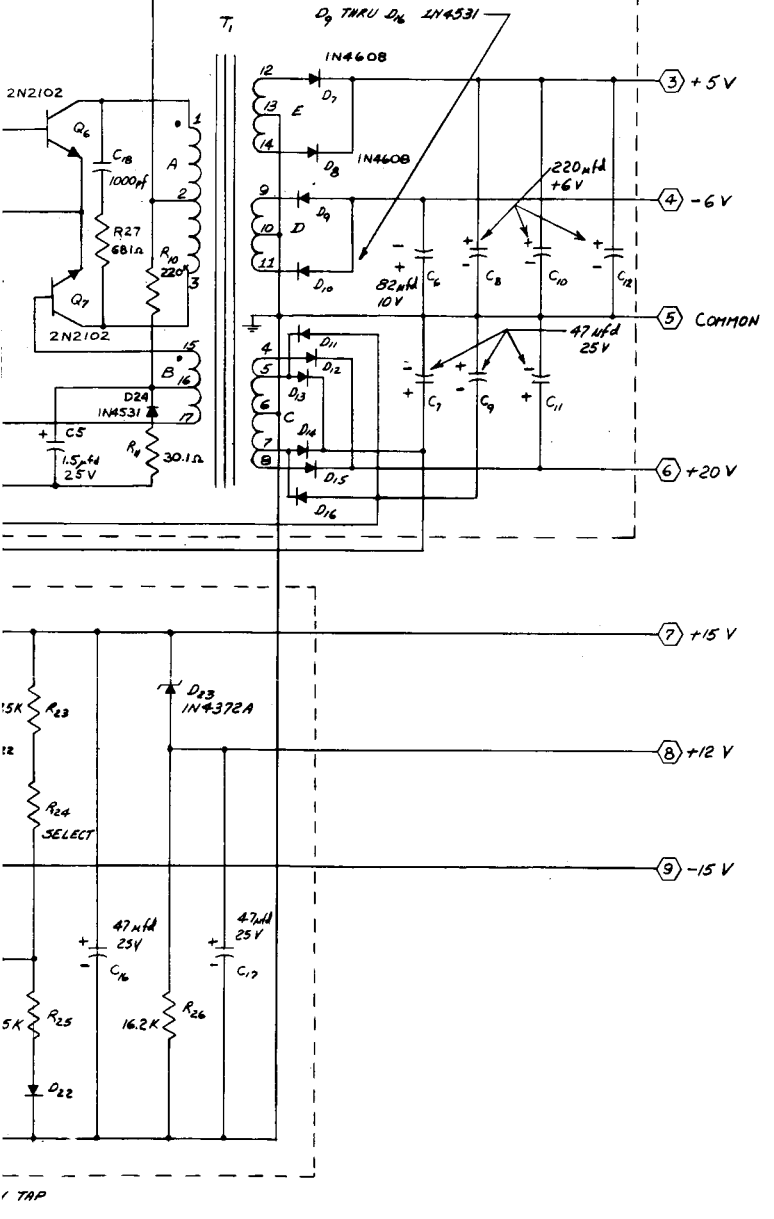
Transistors Q_1 and Q_2 perform the function of a simple series regulator, however, their action is not analog in nature. Instead, the transistors are either saturated or cutoff. This action is accomplished by a non-linear feedback amplifier consisting of transistors Q_3, Q_4, Q_5 and the associated circuits. Operation is as follows: With no voltage across C_3, Q_3 is saturated by bias resistor R_3 and in turn Q_2 and Q_1 are saturated. C_3 is thus charged exponentailly through L_2. When the voltage of C_3 is great enough to exceed the reverse bias voltage of Q_5 (provided by D_5), Q_5 and Q_4 saturate. The saturation of Q_4 essentially "grounds" R_3 through Diode D_3 effectively turning off Q_3, Q_2 and Q_1. These transistors remain turned off while C_3 discharges into the load until C_3 voltage is reduced below the threshold of Q_5. At this point Q_3, Q_2 and Q_1 are turned on and the cycle repeated. The combination of L_2 and C_3 is selected emperically to give the circuit some hysteresis for proper operation. Exact equations for the selection require computer solutions. Basically the circuit can be said to convert energy from the 28 volt level to energy at a lower voltage. In the case shown here the threshold of Q_5 is set to charge C_3 to approximately 20 volts. Figure No. 11 shows typical waveforms.


+28V
28 COMMON
D1
IN4608
L1
L2
L3
2N2102
Q1
2N2907
Q2
R1 562
R2 3.16K
R3 133K
D3 IN4531
D4 IN4608
C1 82μfd 50V
C2 82μfd 50V
Q3 2N3947
D2 IN4531
MCR2225
D5
R8 7.5K
D6 IN4531
R4 19.6K
Q5 2N3251
R6 19.6K
C3 10μfd 35V
C4 33μfd 35V
Q4 2N3947
R5 7.5K
R7 1.78K
R9 16.2K
C19 .01μfd 100V
2N3251
Q8
R12 562
R14 196
IN4531 D7
Q9 2N3947
R15 10K
R16 7.5K
R17 SELECT
C13 4.7μfd 25V
Q10 2N3251
R13 16.2K
R18 7.5K
D8 MCR2225
D9 IN4531
C14 47μfd 25V
-15V REGULATOR
2N3947
Q11
R19 562
R21 196
IN4531 D20
Q12 2N3251
10K
C15 4.7μfd 25V
Q13 2N3947
R20 16.2K
D21 MCR222'5
+15V REGULATOR WITH 12

HIGHEST REF. DESIGNATION	REF. DESIGNATION NOT USED	REFERENCE DWGS.
R_{27} C_{19} T_1 L_3 D_{24}		NAS8-20514-61 -1

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		DELETED C_5	11/4/66	[illegible]
B		ADD C 19, C3 WAS 25V, C4 WAS 47 μfd 25 V, DELETE R27 - 3.48 K, R10 WAS 3.48 K, ADD R27 BY C.18, ADD C5, ADD D24, R11 WAS 3.16K, D1 & D7, D8 WERE IN4002, R8 WAS 7.5 K, Q1 & Q6, Q7 WERE 2N3722	11/11/66	[illegible]

-REGULATOR & INVERTER



TAP

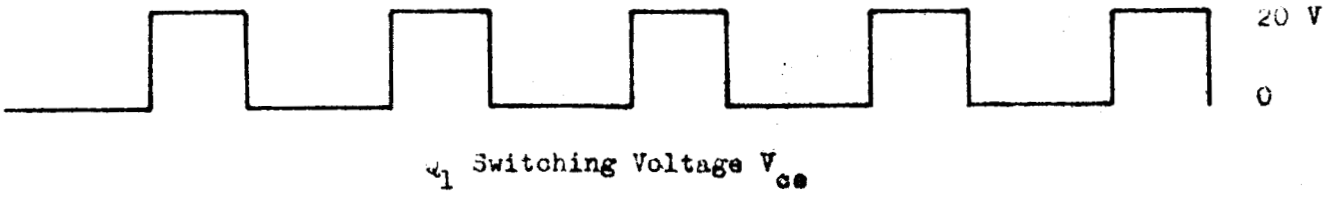
UNLESS OTHERWISE SPECIFIED	DRAWN BY	DEPT	DATE
DIMENSIONS ARE IN INCHES AND ARE AFTER PLATING	J. E. Hendricks		7-26-66
TOLERANCES ON: FRACTIONS ±1/32, DECIMALS .X ±.1, .XX ±.03, .XXX ±.010, ANGLES ±1/2°	[illegible]		8-12-66
MACHINED SURFACES REF: MIL-STD-10 ✓	STRESS ENGR.		
MIL-1-8950 STATUS: INTERCHANGEABLE, REPLACEABLE, UNCONTROLLED	WT. ENGR.		
DIN 96100 (1-63)	MATL. ENGR.		
	RELIABILITY		
	GR. ENGR.		
	PROJECT J. E. Hendricks		8/17/66
	CUST. REF. [illegible]		

MARTIN COMPANY
THE AEROSPACE DIVISION OF MARTIN MARIETTA CORPORATION
FRIENDSHIP INTERNATIONAL AIRPORT, MARYLAND

POWER SUPPLY SCHEMATIC DIAGRAM (MEASURING SOURCE)

CODE IDENT NO.	SIZE	
38397	F	NAS8-20514-62
SCALE		SHEET

[redacted] Figure No. 10.



Q_1 Switching Voltage V_{ce}

Q_1 Switching Current I_E

Output Ripple Voltage

Switching Pre-Regulator Typical Waveforms

Figure No. 11

If the input voltage is raised the periods of current flow shown in Fig. No.11 are reduced in time. Reduction in load will have the same effect. Consequently the voltage C_3 is held about constant. General design procedure is as follows:

Select Q_1 and Q_2 for high beta and adequate power handling relative to the load. Except for the poor selection of power silicon PNP's with low V_{CE} sat the NPN transistor shown would not be necessary. If desirable, the ground lead could be switched with a high power-high beta NPN. Availability of parts somewhat predetermined the design illustrated. Bias Q_3 to saturate Q_2 and Q_1 with the maximum charging current anticipated. Reverse bias Q_5 with a constant temperature zener diode. Forward bias Q_3 with a resistor divider network selected to overcome the reverse bias at the desired voltage of C_3. Diode D_6 is added to provide thermal compensation of V_{BE} for Q_5. Select L_2 and C_3 to provide almost continuous current flow at minimum input voltage and very short time current flow at max. input voltage. Calculations will establish the ballpark but many combinations are possible. A breadboard selection based on availability and size of parts is the shortest design route. Once the basic circuit is established other refinements can be added.

In the design shown C_1, C_2 and L_1 form an LC pi network to reduce RFI problems. D_1 prevents the application of damaging reverse voltage to the circuit. L_3 and C_4 form a decoupling network to reduce interaction between the pre-regulator and the converter. The design of these filters is rather arbitrary. The lowest frequency roll-off was selected compatible with small size of parts.

C. <u>DC to DC Converter</u>.

The dc to dc converter is quite conventional. Operation is strictly based upon saturation of a square-loop core in alternate directions. The

turns per/volt for the transformer are determined from the following equation:

$$N = \frac{10^8}{4.44 f \beta A}$$

f = oscillating frequency in Hertz

β = flux density in gauss

A = Area in sq. cm.

The frequency of oscillation is arbitrary but the higher the frequency the smaller the components. The upper frequency is limited by core losses and possible switching speed of the core material. Ferrite material as was used in the design herein, can operate satisfactorily to at least 10 kHz.

Transistors Q_6 and Q_7 perform switching of current through alternate halves of the winding and R_{10} provides starting bias for the transistors. D_{24}, R_{11} complete the base emitter drive current path and C_5 speeds up switching. Q_6 and Q_7 are selected for low saturation voltage, good speed, adequate current rating and a voltage (V_{CE}) rating of greater than twice the collector voltage. C_{18} and R_{27} reduce switching spikes.

D. Secondary Circuits.

All secondary rectification, filtering and regulation is conventional. All filtering is capacitive and has been found adequate. Regulation is employed on the secondary windings only when better than 3% regulation is required. The series regulators shown are designed for constant input voltage and as low series loss as possible. The series transistors can operate with about 2 volt V_{CE} but the gain will be low unless Q_9 (or Q_{12}) is used as a constant current load in the collector of Q_{10} thus providing a higher gain than could be obtained with a resistor.

E. Mechanical Design.

The mechanical design is completely welded cordwood construction. Two position boards align all of the parts. Although no photographs are available the construction is identical in type to the rest of the discrete modules. The finished module is encapsulated in silica filled epoxy. The silica provides high thermal conductivity. The entire module is encased in a Mu-metal box for electro-magnetic shielding. The entire module mounts separately from the rest of the modules in the finished multiplexer as shown in Figure No.13 which is a photograph of the measuring source.

F. Operating Specification

Input voltage = 22 to 40 volts DC

Input average current = 140 ma

Temperature Environment = - 55°C to + 85°C

Approximate Voltage pre-regulation = $\pm$ 2% @ 20 volts over the voltages and temperature range.

Secondary Voltage regulation: $\pm$ 3% unregulated, about 0.1% with regulation.

Overall efficiency: About 75% - the largest loss is at the integrated circuit voltage where diode rectification is the highest % loss.

The supply can handle about 250 ma average input current without design change. However, for larger currents, some change in R_2 and R_3 might be required for more drive. Some change in the L_2C_3 time constant may also be required if the current is much above 250 ma. In addition, the bias of Q_6 and Q_7 might need increasing for currents greater than 250 ma.

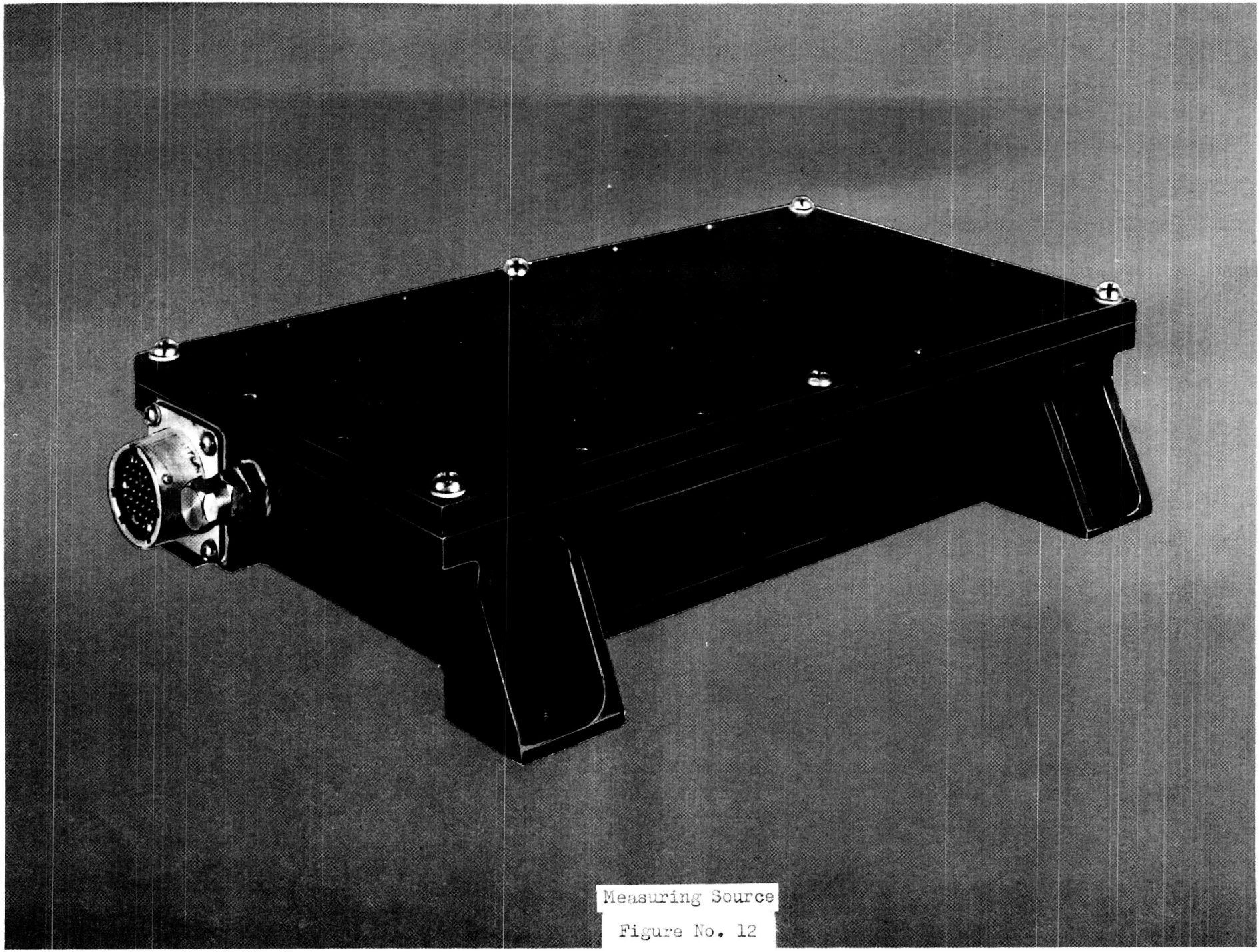
VII. THE ASSEMBLED MEASURING SOURCE

A. Electronic Design.

The electronic design of the entire measuring source has been primarily discussed under the design of each module but a few additional rules were applied to measuring source assembly. Modules were arranged so that data input and output leads are as short as possible to avoid noise pickup. All modules except the power supply were constructed to solder in a mother board. The power supply was mounted separate to keep input dc circuits from the mother board. Ground leads were made as large as practical for low noise. Digital circuits (primarily address) were placed close to the supply to minimize high ground current noise in analog circuits.

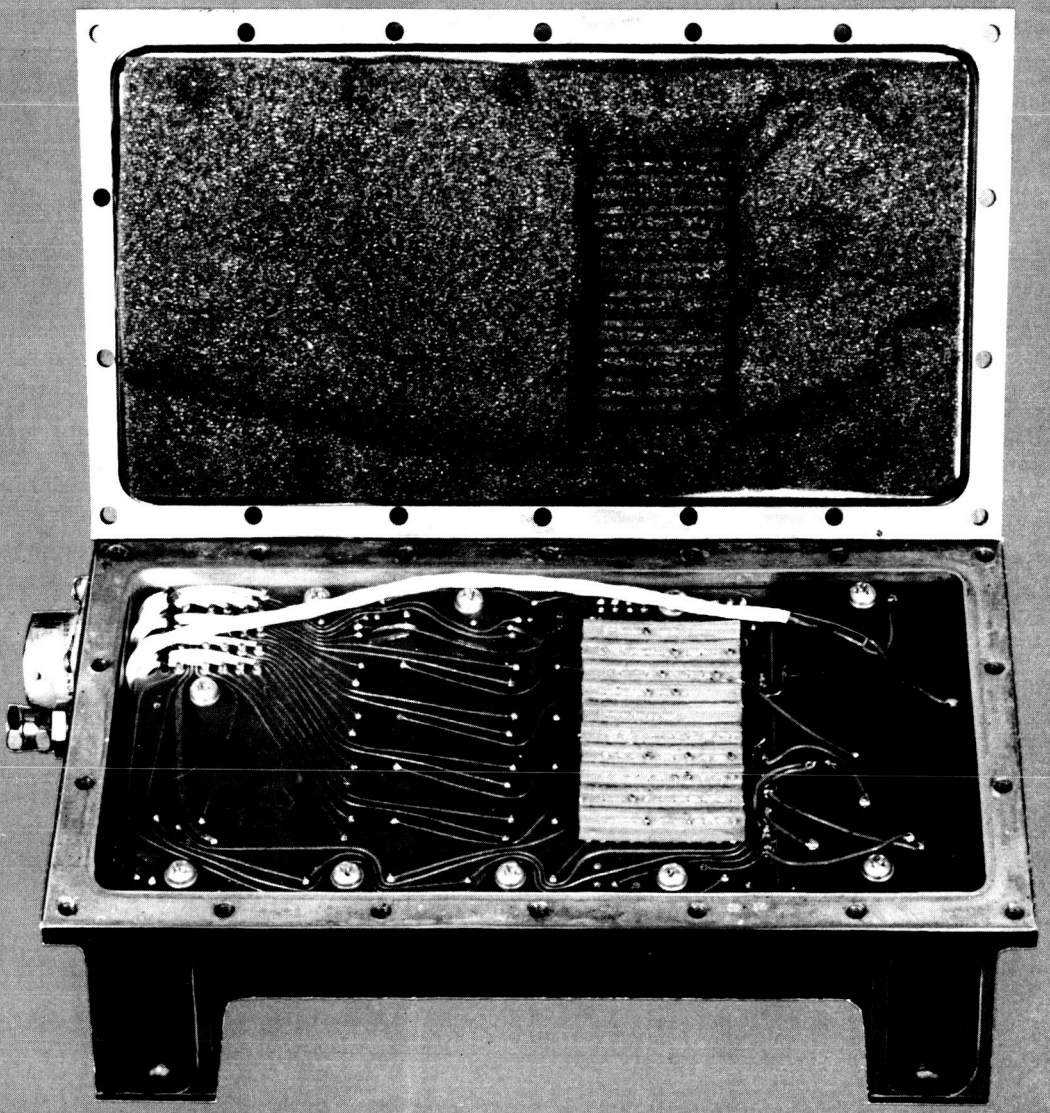
B. Mechanical Design

Figures No.12 and No.13 are photographs of the measuring source. The case is machined magnesium. The mother board is supported on top of the modules with each module being bolted through the mother board to the case furthest from the connector. All inputs are through a single connector bolted to the case with an "O"-ring seal. The box has a solid bottom and a removable top sealed with an "O"-ring. Input power leads and the diode modules are held in place by a poly-urethane foam pad. A pressure-fill valve is located by the connector. The mother board is a double sided 1/16th inch epoxy glass pc board. The entire unit weighs about two and three-quarter pounds.



Measuring Source

Figure No. 12



Measuring Source (cover removed)

Figure No. 13.

VIII. PERFORMANCE AND TEST RESULTS

A. General

At the first assembly of the measuring source all modules operated but there was excessive noise upon the data output. It was finally established that the power supply had a high impedance short from the primary side of the inverter to the secondary. Attempts were made to "de-pot" the module and analyze the trouble but all were unsuccessful. Finally a new power supply was built. The new module was encapsulated without problems. The basic noise observed in the first module was eliminated but the necessity for further reduction of noise required encasement of the module in a Mu-metal box. With this shield and capacity coupling of the inverter secondary ground to the measuring source case, virtually all noise was eliminated from the data pulse. All initial tests of the multiplexer were then excellent.

The accuracy requirements for the systems as best could be measured were met. There was a seven millivolt offset on the data bus that apparently resulted from encapsulation of the amplifier. This offset could be eliminated by potentiometer adjustments built in the circuit, but the external compensation of such errors is more reliable. Even without compensation for this offset the requirement for 0.999% absolute accuracy $\pm$ 10 MV appears to have been complied with. The absolute accuracy measurement was checked by differential comparison which could not be done with 100% assurance to better than about 0.25%. It is well to stipulate that data should be monitored with differential measurement of the data pulse output. This is absolutely necessary to eliminate common mode noise. Actual operation of the system will require the same technique.

It should be noted that only the middle portion of the data pulse is useable. About two and one-half micro-seconds of each end of the pulse

are disturbed by switching transients. This leaves about 20 micro-seconds of useable time for monitoring. For example, an A to D converter may be used as a monitor with a delay circuit to start conversion at the appropriate time after the initial rise of the data pulse.

B. Environmental Tests.

Temperature shock, temperature cycling, moisture resistance, and vibration were performed in accordance with MSFC specification JDM60303. EMI tests were performed in accordance with MIL-I-6181 D. The following paragraphs summarize the tests and results.

1. Temperature Shock.

The measuring source was exposed to two cycles of temperature change from - 10°C to + 75°C both operating and non-operating with temperature changing and remaining at the proper times specified (5 minutes to change 1 hour exposure for each of the 4 cycles). No degradation in operation was observed.

2. Temperature Cycling.

The measuring source was exposed to the complete cycle of temperature cycling. First the temperature was reduced to - 20°C at the rate of 10°C reduction per 5 minute interval and maintained for 1 hour; then the box was returned to room temperature at the same rate and maintained for another hour. Then the temperature was raised to 85°C at the same rate. During the first test the power supply in the unit failed at the end of the one hour at 85°C. A filter capacitor shorted. The circuit was completely re-examined and no cause for failure could be found but as a precautionary measure the power supply was rebuilt with a higher voltage capacitor at the point of failure. The temperature cycle was repeated with the new supply with no failure for two cycles.

3. Moisture Resistance.

The unit was exposed to elevated humidity and temperature for a 24 hour cycle as required. No degradation in unit operation resulted.

4. Vibration Tests.

The measuring source was exposed to sine and random vibration cycles on each axis in accordance with the specifications. Sinewave vibration was 10 g along curve B of specification 50M60303, and random vibration was in accordance with curve D at 20 g. During the sine test , resonances of 60g to 80 g were observed on the cover of the unit for all axes. The most resonant points were between one and two kHz. No degradation in performance was observed. The random vibration did not cause degradation in performance and no other peculiarities in performance were otherwise observed.

5. EMI Tests.

The measuring source was tested in accordance with MIL I-6181D as modified by the contract. Performance of the unit was not degraded by any conducted or radiated interference. However, the unit initially showed several points of conducted interference and more of radiated interference between 15 MHz and 50 MHz. The unit was, as a consequence, modified with 0.047 capacitors from +28 volts to the case and the 28 volt common to the case. These capacitors filtered the unit to meet all specifications. While these capacitors were added externally, on future construction they would be incorporated in the power supply.

6. Altitude Tests.

A requirement for vacuum testing to 10^{-7} mm Hg could not be performed with available equipment. The test could have been ultimately run to 10^{-4} mm Hg but conflicting useage of vacuum chambers would have delayed delivery

of the end item. The situation was discussed with the customer and it was concluded that all the tests, as specified, would specifically prove the operation of the circuits in a vacuum. Since all modules are encapsulated and no high voltages exist, successful results are almost completely predictable. With this knowledge it was mutually agreed that the test, as could be performed, did not merit delay of equipment delivery. A vacuum test, as really intended, will be performed at the option of the customer. The intent of this test will be to mount the equipment on available cold plates at MSFC and evacuate in accordance with some specification (possibly 10^{-7} mm Hg wasn't realistic) and test for proper thermal operation of the measuring source.

IX. CONCLUSIONS

The results of contract NAS 8-20514 are generally favorable to the construction of an Addressable Time Division Data System utilizing distributed measuring sources connected to a common address cable and to a common data bus. While original studies showed the greatest advantages of the system might be in weight saving of cabling, further study has shown the weight savings is likely secondary to flexibility. Great flexibility is realized in the respect that instrumentation can be modified to add or remove measurements rapidly without extensive recabling.

Phases I and II established the technical and practical feasibility of the system. Phase III has now established the constructability of flight hardware. The prototype hardware was shown to meet all of the design requirements tested to. The only module failure in the entire construction program was the power supply. Since fifteen total modules were constructed from commercial parts without a test program this success can be considered almost remarkable. If a production program were to be undertaken a high-reliability parts procurement program would have to be recommended.

One feature of the design that would not be repeated for another single item program is the encapsulation of any module in an almost indestructable material such as proved to be the case of the power supply. The use of silica-filled epoxy provided excellent and simple heat sinking and can be recommended for production programs where the throw-away of defective units is not disasterous. For a one-time occasion selective heat-sinking of "hot" parts appears more favorable.

The goal of a 0.1% system for high level monitoring appears entirely practical. Perhaps even more precision in the multiplexer is possible if the source of 7 mv offset voltage in the amplifier is further investigated.

This offset need not necessarily be removed by the addition of potentiometers or other circuitry or changing in potting techniques if the offset can be established constant for all modules. The test results performed on the representative unit indicated the offset is not thermally changed which is a favorable indication of its repeatability.

All goals of the contract are believed to have been accomplished.

APPENDIX A

PRECAUTIONS IN SYSTEM APPLICATION OF THE MEASURING SOURCE

Various precautions must be observed in the application of the measuring source if the potential accuracy capability is to be achieved. The instrument can be used in several system configurations but a penalty will be paid in increased noise and increased error if certain procedures must be violated. It will be up to the discretion of the user as to the application if all the rules are known.

The measuring source is designed for lowest noise error when a system of ground isolation is used. All transducer leads are normally isolated from the ground by the double bus switching of commutating switches. If desirable the common lead of all transducers can be grounded to the measuring source ground, but common mode noise errors can result. The address bus also has ground isolation achieved by the differential amplifiers. Again the system can be operated with address common input grounded but also with the probability of increased noise. The data bus common is the ground of the measuring source. For proper isolation this ground should be carried to a differential amplifier or transformed at the monitoring unit. Common grounds between these boxes can add noise to the data pulse.

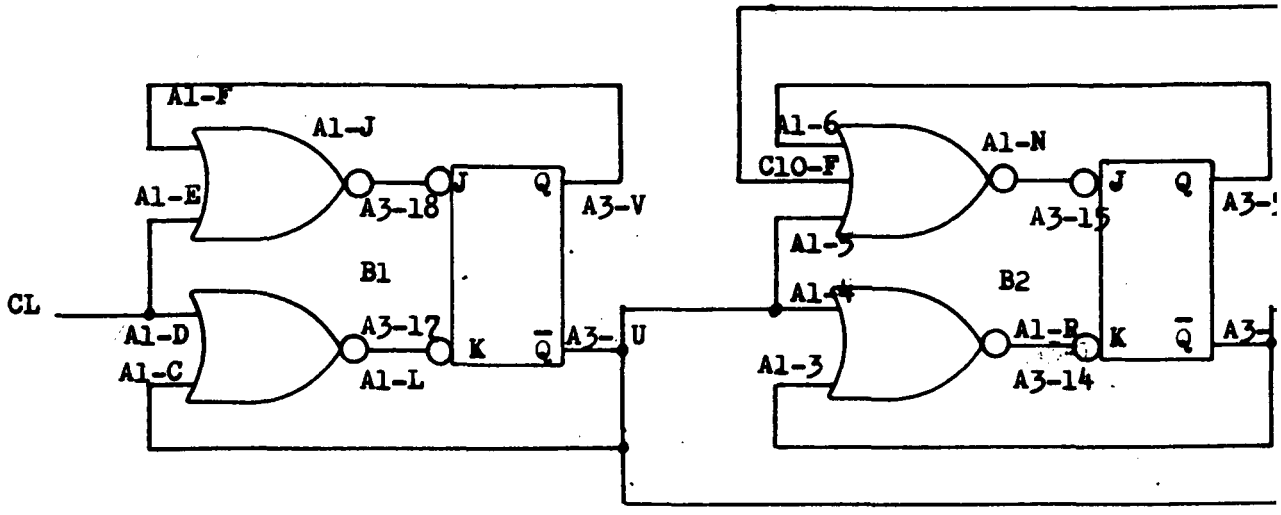
In addition to observing proper grounding, correct loading of the data bus is necessary. If 0.1% accuracy is required without calibration, the load should not be less than 30 k-ohms; however if calibration is permissible, the load may go as low as 10 K-ohms and accuracy will still be good over the temperature environment. The source impedance also cannot exceed 10 K-ohms without accuracy impairment at a 1-kHz sample rate. If the sample rate does not exceed 100 Hertz the transducer impedance may be as high as 100 k ohms.

APPENDIX B

BREADBOARD PROGRAMMER CONVERSION FROM EIGHT TO TEN BITS

A breadboard programmer was designed for the study portion of the contract. This programmer was designed to supply 8-bit addresses but the current prototype equipment requires ten bit addresses. While a completely flexible 10-bit conversion of the original programmer would require extensive modification, a modification to convert the programmer to limited ten-bit use is not difficult. The conversion results in a 256 address program wherein the ninth and tenth bits are the same for all addresses. All 1024 codes are possible by manually switching the last two bits; so the total program really consists of four individual 256 code programs.

Figure No. B-1 shows a ten bit counter to be constructed in place of the existing eight bit counter shown on Figure No. B-2. Figure No. B-3 shows an extension to the output shift register which must be inserted in existing circuitry, as shown by Figure No. B-4. Figure No. B-1 also tabulates all wiring changes. Figure No. B-5 is a new timing diagram.



ADD NEW CARDS

C9	Flip Flop
C10	GATE
C11	GATE
C12	GATE

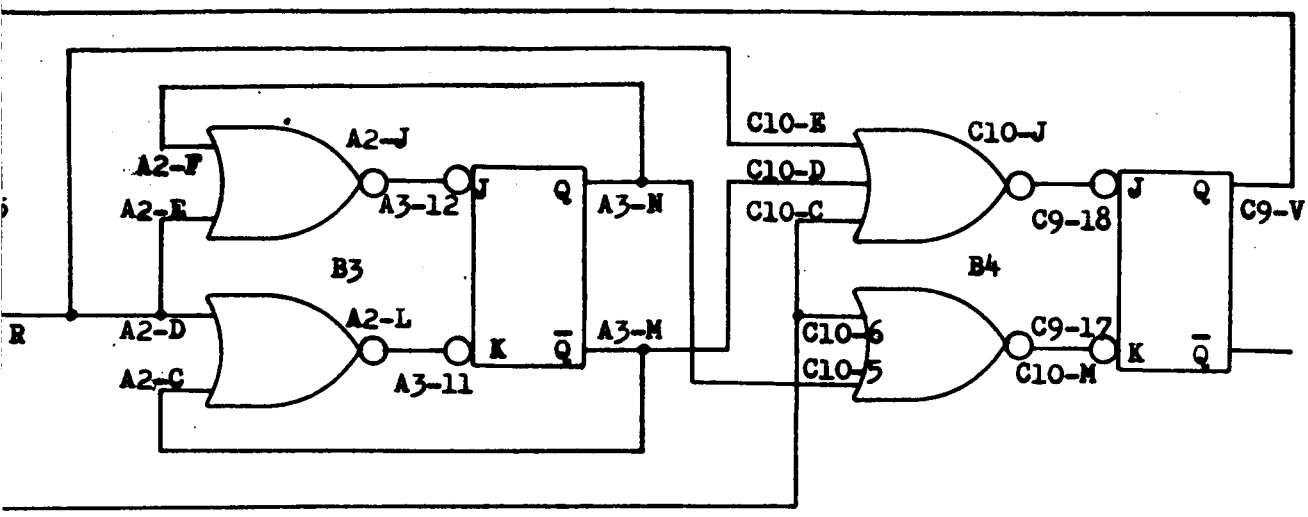
REMOVER WIRES

C5-J	C1-4
C5-H	B26-L

ADD WIRES

C10-F	C9-V	C10-16	C10-W	C10-3	C10-J	C11-K
A1-N	C10-H	C10-12	C10-A	C11-S	C11-W	C11-U
C10-8	C10-A	C10-13	C10-A	C11-H	C11-J	C11-6
C10-9	C10-A	C10-M	C9-17	C11-H	C9-14	C11-5
C10-10	C10-A	C10-N	C10-M	C11-8	C11-A	C11-12
C10-11	C10-A	C10-6	C10-C	C11-9	C11-A	C11-13
C10-T	C10-W	C10-5	A3-N	C11-F	C5-K	C11-M
C10-J	C9-18	C10-P	C10-R	C11-E	C5-J	C11-M
C10-K	C10-J	C10-18	C10-W	C11-D	C10-4	C11-16
C10-L	C10-J	C10-14	C10-A	C11-C	C9-R	C9-M
C10-E	A3-R	C10-15	C10-A	C11-10	C11-A	C11-14
C10-D	A3-M	C10-P	C9-15	C11-11	C11-A	C11-15
C10-C	A3-U	C10-4	C6-6	C11-K	C9-12	C11-P

PROGRA

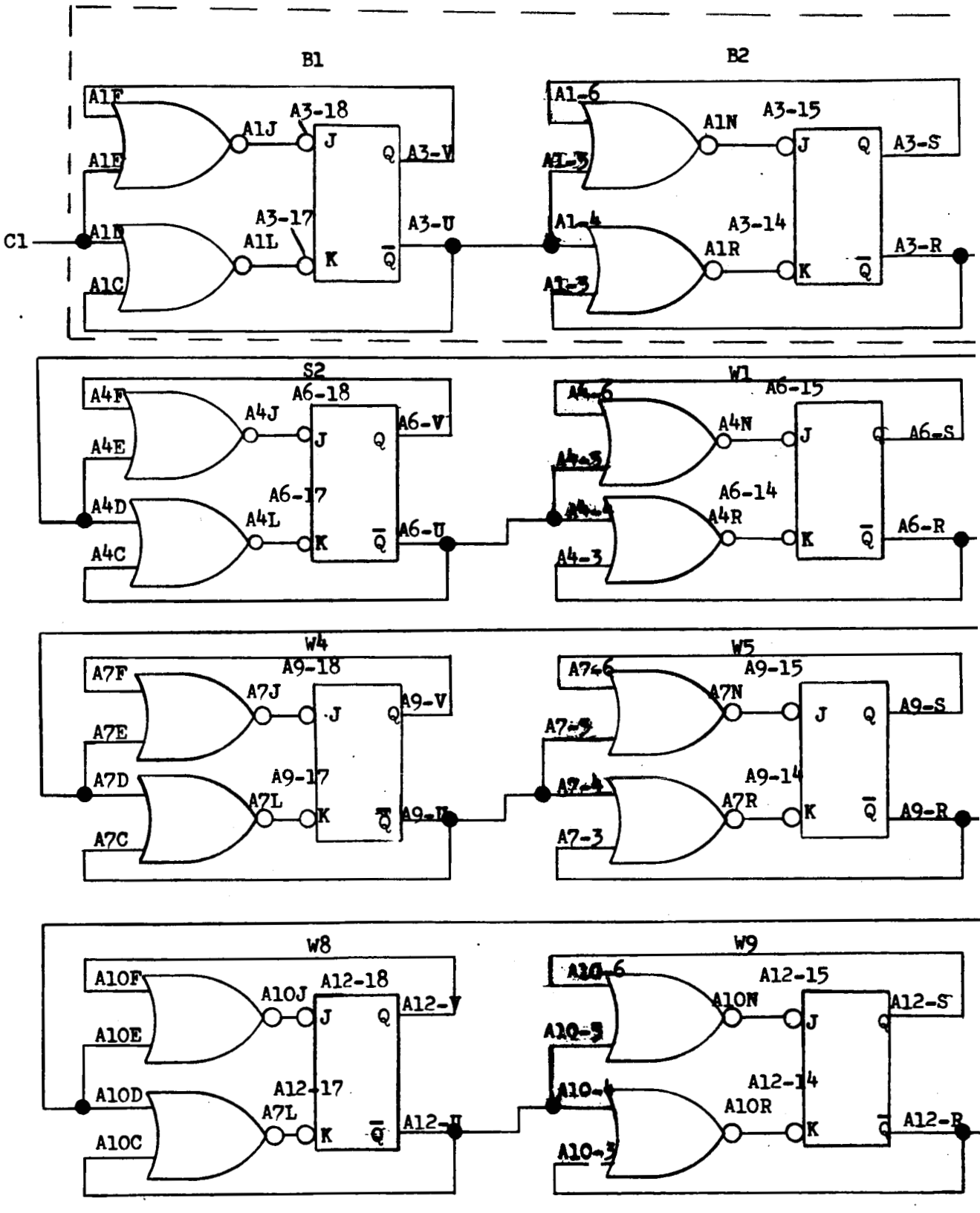


C11-L	C11-P	C9-13	C12-10	C12-A
C11-W	C11-18	C11-W	C12-11	C12-A
C9-S	C11-3	A23-N	C12-K	C12-L
C11-E	C11-4	Bit 9 SW.	C12-K	C9-L
C11-A	C12-8	C12-A	C12-U	C12-W
C11-A	C12-9	C12-A	C12-C	A23-N
C11-N	C12-H	C9-10	C12-D	C12-M
C9-11	C12-H	C12-J	C12-1b	C12-W
C11-W	C12-S	C12-W	C12-12	C12-A
C1-4	C12-F	C11-3	C12-6	C12-E
C11-A	C12-E	Bit 10 SW.		
C11-A				
C11-R				

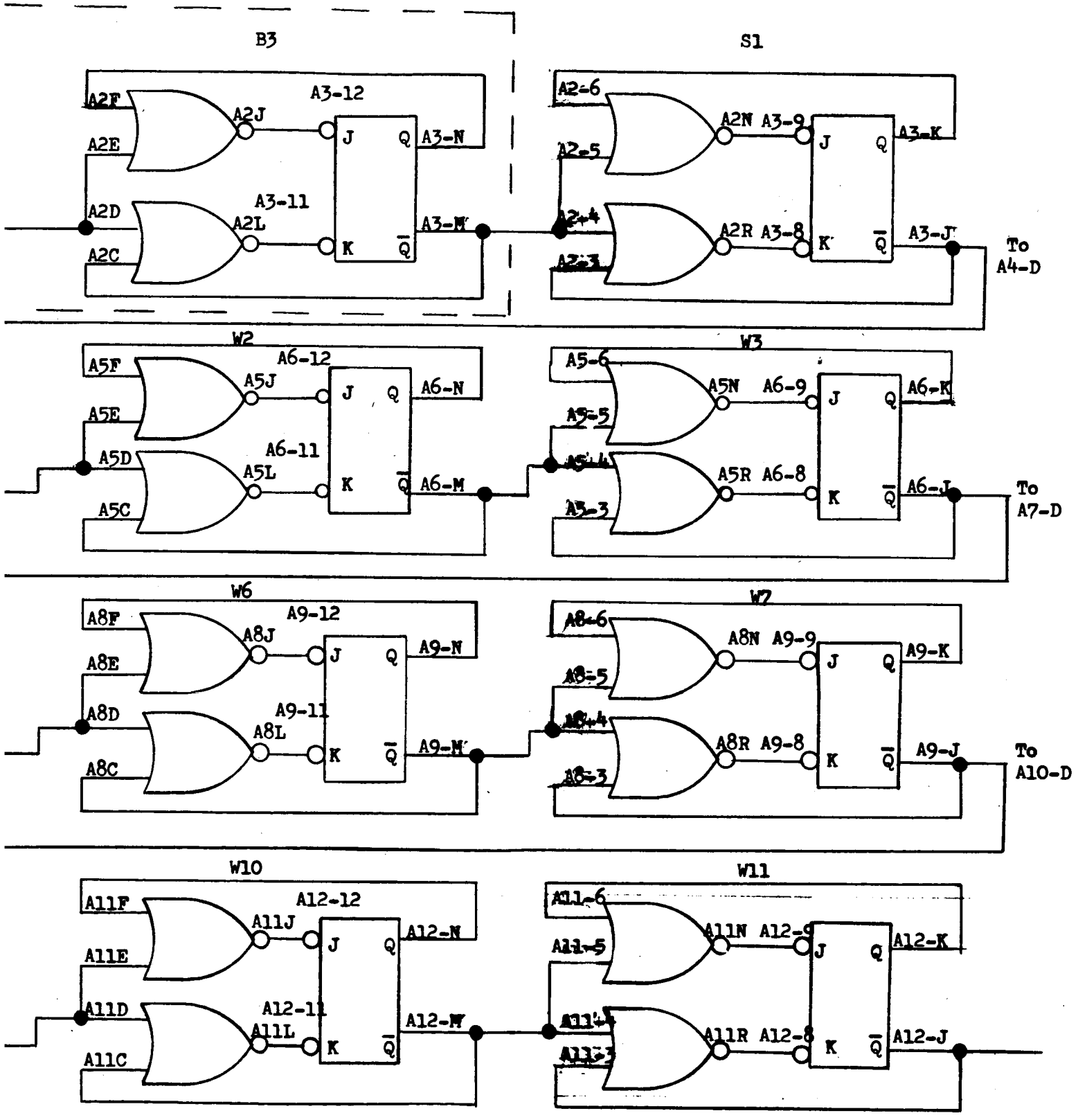
MER 8-BIT TO 10-BIT CONVERSION

FIGURE B-1

MODIFY PER FIGURE NO. B-1

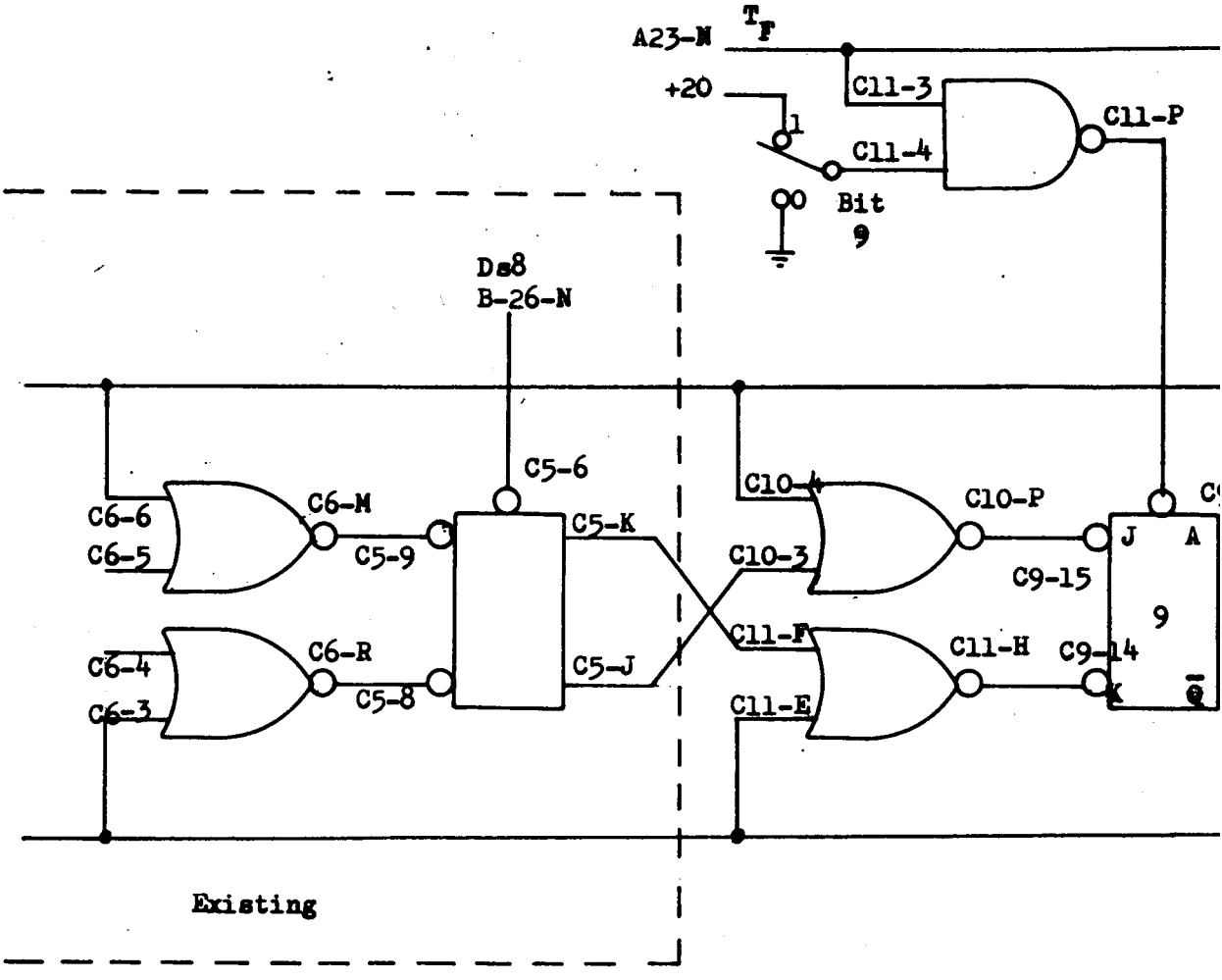


8-BIT



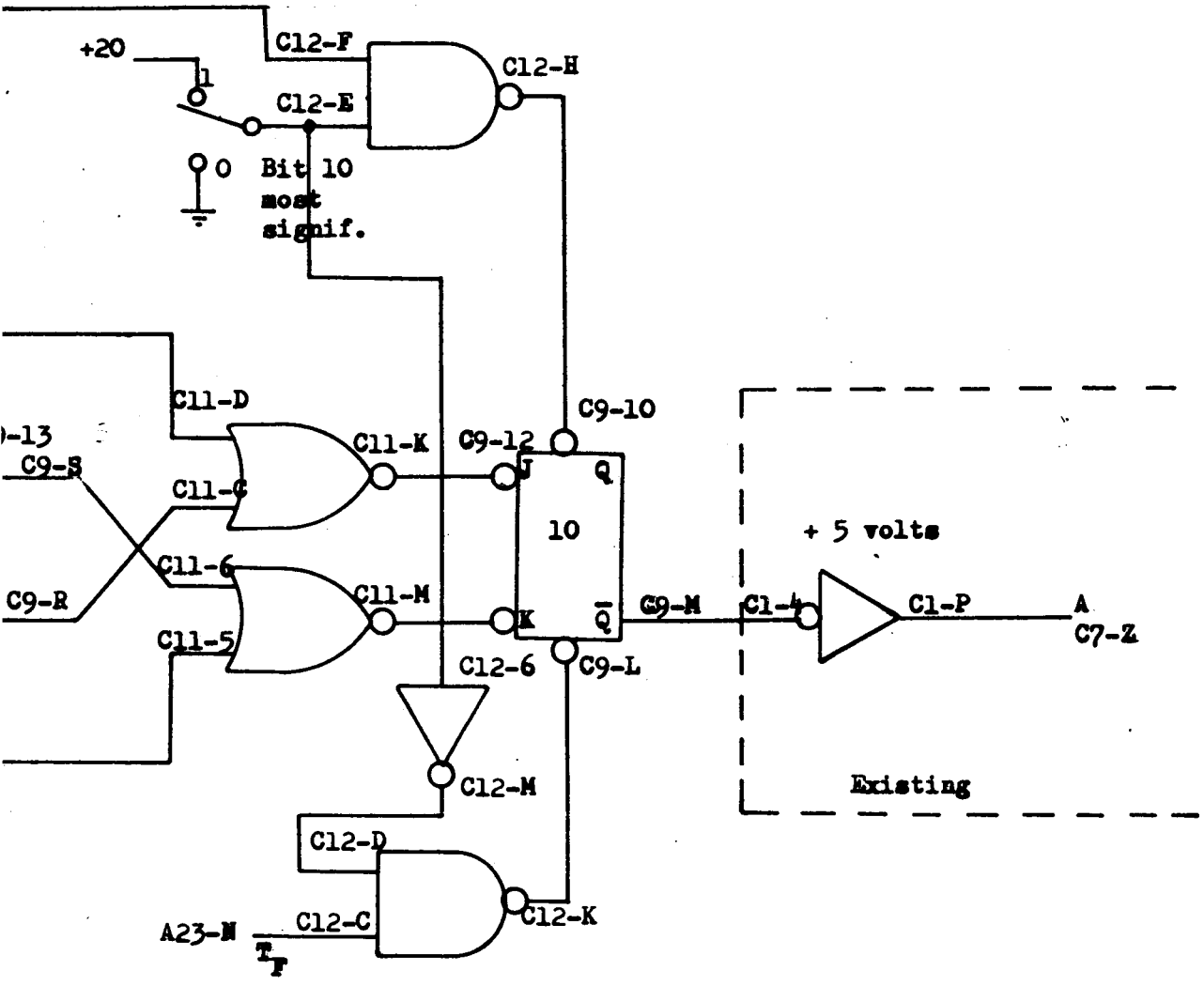
OGRAMMER MODIFICATION

Figure No. B-2



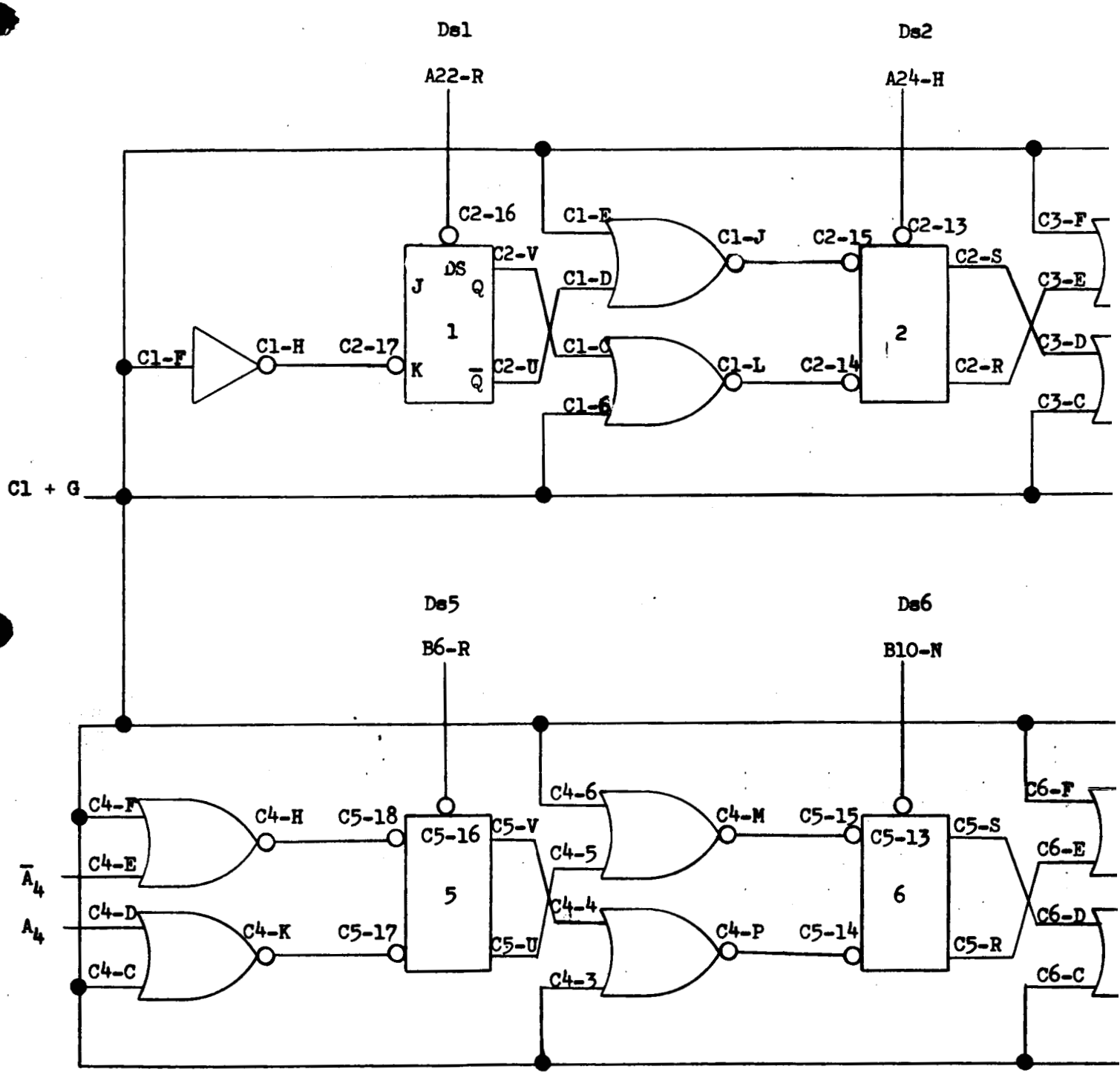
PROGRAMMER 8-BIT TO 10-

Figure 1



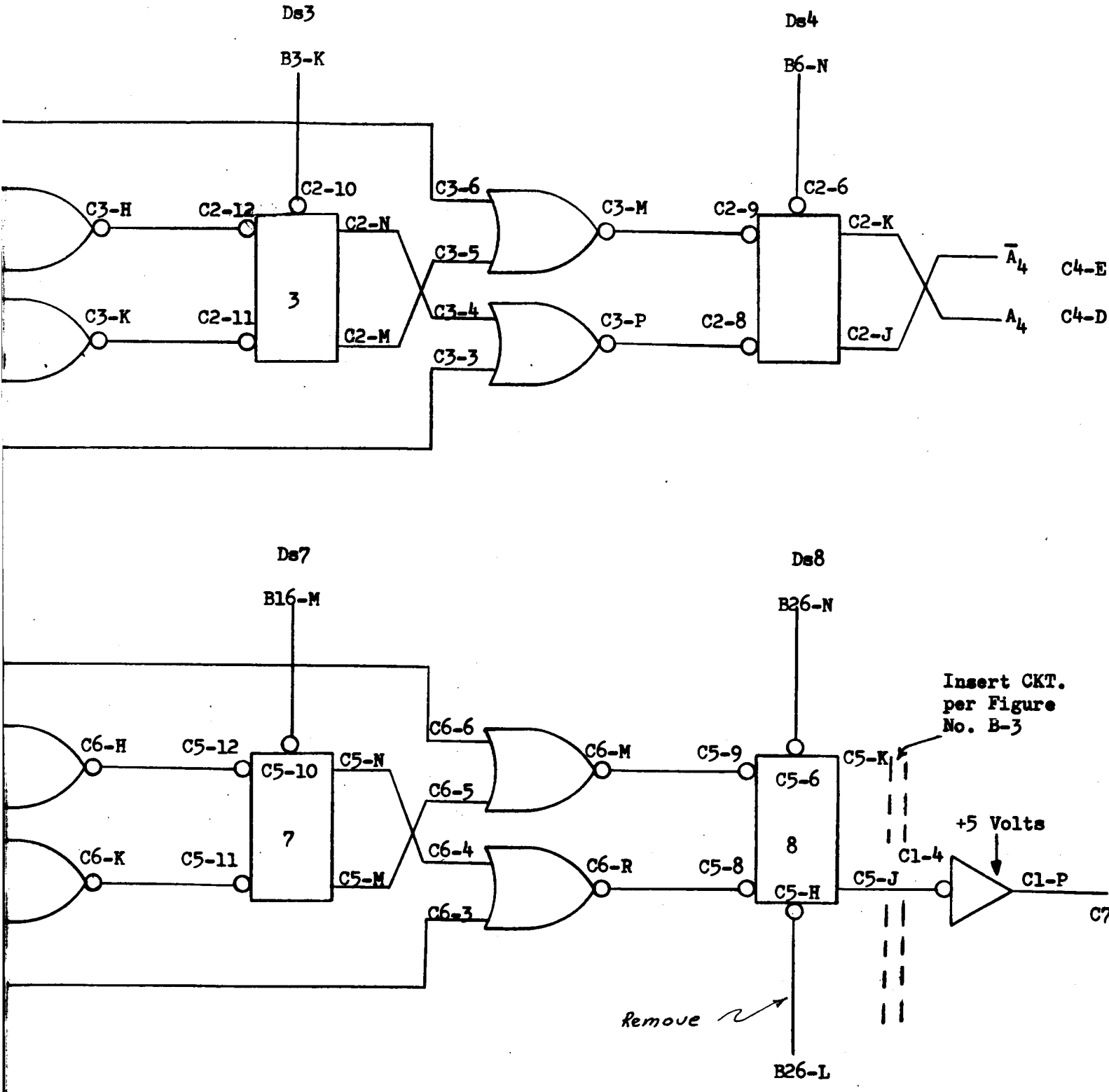
BIT CONVERSION

o. B-3



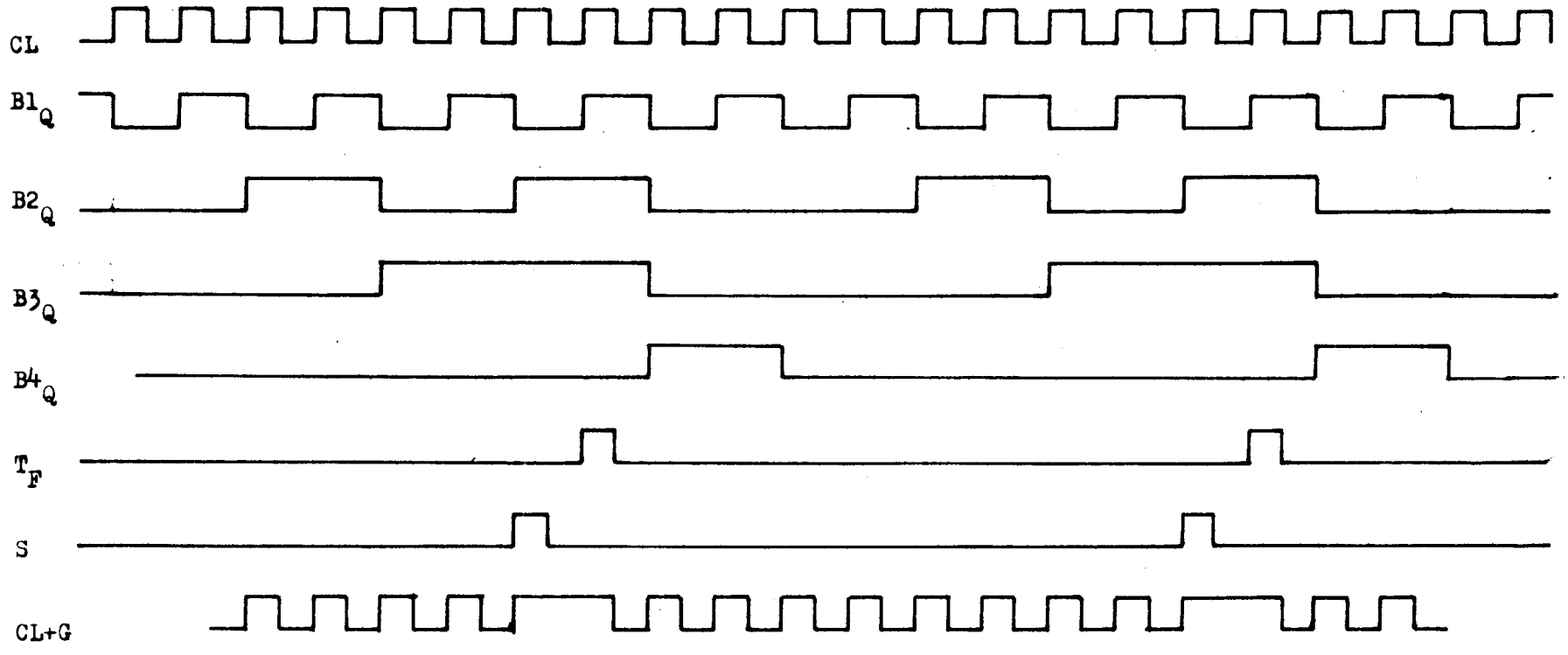
MODIFICATION TO

Figure



-BIT PROGRAMMER

o. B-4



TIMING DIAGRAM 8-BIT CONVERSION

FIGURE B-5

APPENDIX C

CONNECTOR PIN IDENTIFICATION

Appendix D references all production drawings which completely describe the measuring source. However, for a quick reference the following table identifies all connector pins of the measuring source.

Connector Designation	Pin No.	Function
J1	1	Data Input Inverter
	2	Non-Inverted
	3	INV
	4	NON-INV
	5	INV
	6	NON-INV
	7	INV
	8	NON-INV
	9	INV
	10	NON-INV
	11	INV
	12	NON-INV
	13	INV
	14	NON-INV
	15	INV
	16	NON-INV
	17	INV
	18	NON-INV
	19	INV
	20	NON-INV
	21	Data Bus
	22	Data Bus Common
	23	Address
	24	Address Bus Common
	26	+ 28 Volts
	27	+ 28 volt common
	28	Chassis Gnd.

APPENDIX D

REFERENCE DRAWINGS

The following is a list of production drawings for the construction of a measuring source. These drawings are not included as a part of this report.

NAS 8-20514 - 1	FINAL ASSEMBLY
11	CHASSIS
12	COVER
13	MOTHERBOARD
21	ASSY. - ADDRESS MODULE
23	WELDED MODULE-DETAIL ASSY. - ADDRESS
24	BUSHING A
25	BUSHING B
26	DETAIL ASSY. - HEAT SINK A
27	DETAIL ASSY.- HEAT SINK B
28	DETAIL ASSY. - HEAT SINK C
29	INSULATOR
31	ASSY. PRINTED WIRING BOARD NO. 1 - ADDRESS MOD.
32	ASSY. PRINTED WIRING BOARD NO. 2 - ADDRESS MOD.
33	ASSY. PRINTED WIRING BOARD NO. 3 - ADDRESS MOD.
34	ASSY. PRINTED WIRING BOARD NO. 4 - ADDRESS MOD.
35	ASSY. PRINTED WIRING BOARD NO. 5 - ADDRESS MOD.
36	ASSY. PRINTED WIRING BOARD NO. 6 - ADDRESS MOD.
41	PRINTED WIRING BOARD NO. 1 - ADDRESS MOD.
42	PRINTED WIRING BOARD NO. 2 - ADDRESS MOD.
43	PRINTED WIRING BOARD NO. 3 - ADDRESS MOD.
44	PRINTED WIRING BOARD NO. 4 - ADDRESS MOD.
45	PRINTED WIRING BOARD NO. 5 - ADDRESS MOD.
46	PRINTED WIRING BOARD NO. 6 - ADDRESS MOD.
54	MOUNT-FLAT PACK
61	WELDED MODULE-DET. ASSY.-POWER SUPPLY
63	INDUCTOR
64	TRANSFORMER
65	PLATE-HEAT SINK
73	WELDED MODULE-ANALOG SWITCH
74	INTERCONNECT BOARD-ANALOG SWITCH
75	PRINTED WIRING BD. ASSY. - ANALOG SWITCH
76	PRINTED WIRING BOARD - ANALOG SWITCH
93	THERMOSETTING CASTING RESIN - HIGH DENSITY
94	THERMOSETTING CASTING RESIN - LOW DENSITY