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SATURN INTEGRATED CIRCUIT
RELIABILITY TEST PROGRAM

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
George C. Marshall Space Flight Center
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On

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1.0 INTRODUCTION

This is the First Quarterly Report on the work performed under Contract NAS8-18018 "SATURN Integrated Circuit Test Program" which is being performed for NASA, George C. Marshall Space Flight Center, Huntsville, Alabama.

The goal of this program is to investigate the reliability characteristics of integrated circuits so that we may develop and identify effective screening test methods for the dominant failure modes and mechanisms as they occur in the type of devices studied in this program. The test sample in this program represents three basic manufacturing processes. One device type, the MC-1519, contains one compatible thin film die and one monolithic transistor die per device. The other devices (e.g. the MC-1525, MC-1530, and SN-526A) are of the single die all-diffused monolithic structure. Functionally, the MC-1519 and the MC-1525 represent a class of differential amplifiers, while the MC-1530 and SN-526A represent a class of operational amplifiers; and in the case of the SN-526A, possible use as a high gain differential amplifier. The SN-526A was procured from Texas Instruments, Inc. These particular circuits were chosen as being representative of the single types of processes which may be used to formulate integrated linear circuits.

This report contains a description of the test devices used in the program, as well as a detailed description of the test program. A detailed description of electrical parameter measurements is presented for the MC-1519. An analysis of the stress conditions on all elements within the integrated circuit is presented in Section 6. A similar analysis will be made for the other circuits in subsequent reports.

2.0 TEST DEVICES

2.1 Description of Test Devices

Four different integrated circuit amplifiers have been selected for this program. The three circuits manufactured by the Motorola Semiconductor Products Division are the MC-1519, MC-1525, and MC-1530. That manufactured by Texas Instruments, Inc. is the SN-526A. These circuits differ among themselves in their performance characteristics, manufacturing processes and methods of packaging (Table 2-1).

TABLE 2-1

COMPARISON OF TEST DEVICES

DEVICE TYPE	TYPE OF AMPLIFIER	MANUFACTURING PROCESS	TYPE OF PACKAGE
MC-1519	Differential	Monolithic P-N-P and Monolithic N-P-N w/thin Film Resistors	10-lead TO-5 Package
MC-1525	Differential	Monolithic w/diffused Resistors	10-lead TO-5 Package
MC-1530	Operational	Monolithic w/diffused Resistors	10-lead alumina Flat Package (1/4" x 1/4")
SN-526A	Operational	Monolithic w/diffused Resistors	10-lead welded Flat Package (1/4" x 1/8")

2.1.1 Differential Amplifier - MC-1519

The most important feature of a differential amplifier is its ability to amplify signals that are differential to its inputs, while rejecting signals which are common to its inputs. Common-mode signals not only are not amplified but are attenuated in a good

differential amplifier. A high impedance common to the emitters of the input transistors is necessary to obtain this characteristic. In the MC-1519, this high impedance is achieved by using a transistor operating in class A as a current source at this point (Figure 2-1). Design of this device permits its use in either the Common Emitter (CE) mode (Figure 2-2) or the Common Collector (CC) mode (Figure 2-3).

The MC-1519 is a monobrid circuit which has two dice housed in one package (Figure 2-4). One die is a compatible integrated circuit having three NPN transistors and two nichrome thin film resistors (Figure 2-5a). The other die is a monolithic integrated circuit having two PNP transistors (Figure 2-5b). Interconnections between the die and the posts of the header are shown in Figure 2-4. The devices procured for this program are housed in the TO-5 package.

2.1.2 Differential Amplifier - MC-1525

Motorola's differential amplifier series, MC-1525-8, are designed to provide system and circuit engineers with greater flexibility than was previously available in monolithic integrated circuitry. By using multiple biasing connections and compatible NPN-PNP amplifier cascades, a wide range of gain, impedance, power supply voltage and current drain constraints may be satisfied. The circuits incorporate diode temperature compensation and are geometrically oriented for good tracking. The MC-1525 is the member of this series that has been selected. Like the MC-1519, this device employs an active current source at the emitters of the input transistors to meet the requirements for a good differential amplifier (Figure 2-6).

The four resistors in the emitter of the current source transistor may be connected in a variety of ways. The resultant effective resistances, (R_e), in conjunction with a given value of

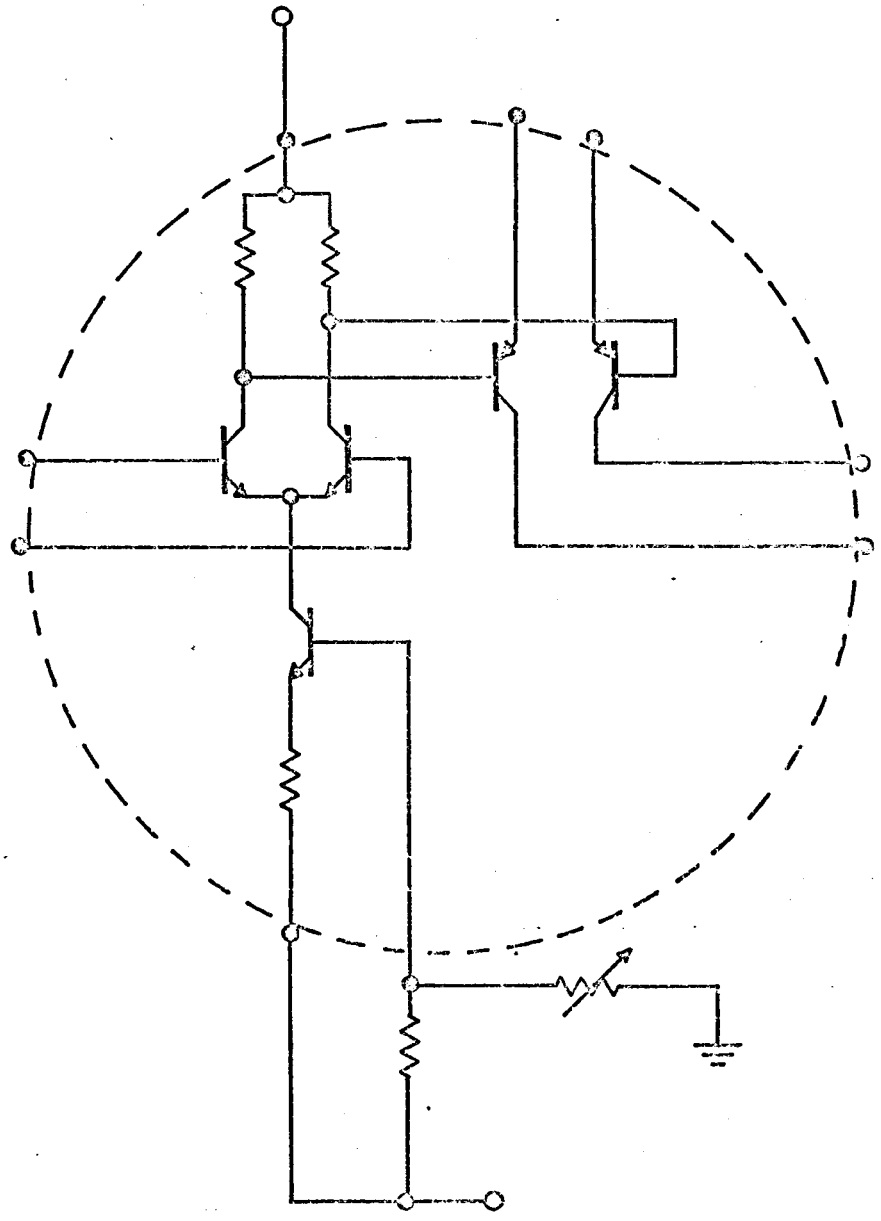

Figure 2-1. Schematic Diagram of MC-1519

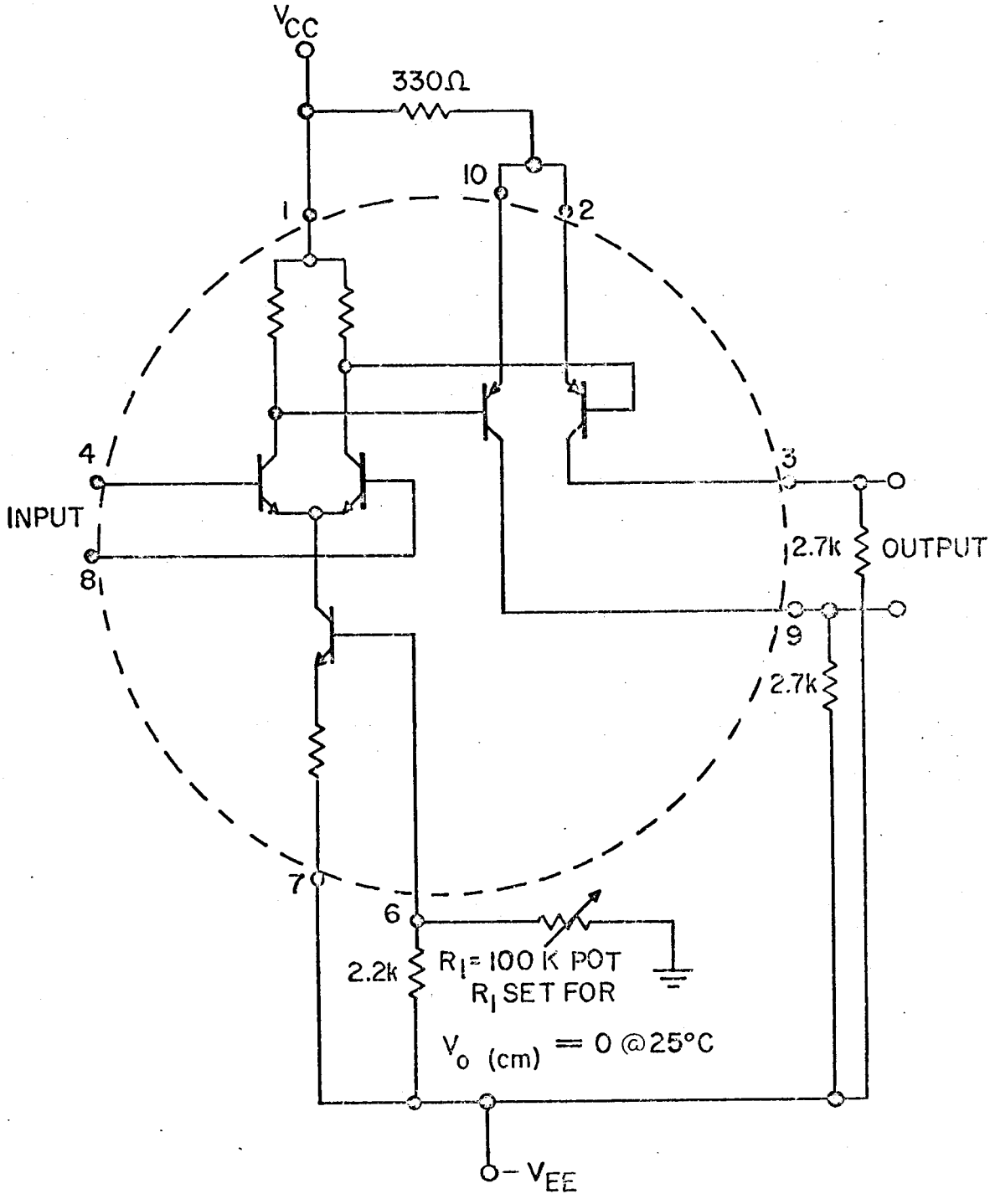

Figure 2-2. MC-1519 in Common Emitter (CE) Mode

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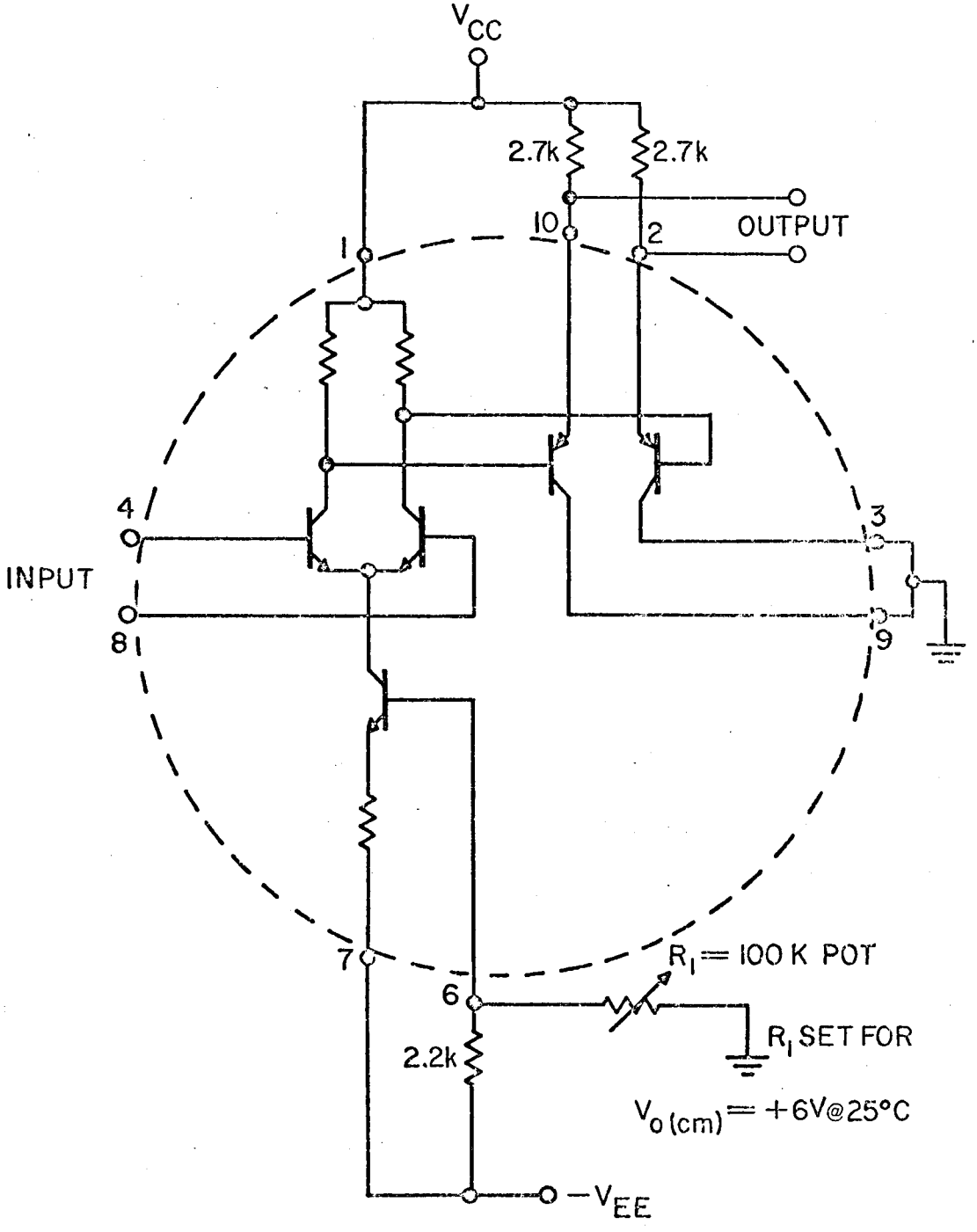


Figure 2-3. MC-1519 in Common Collector (CC) Mode

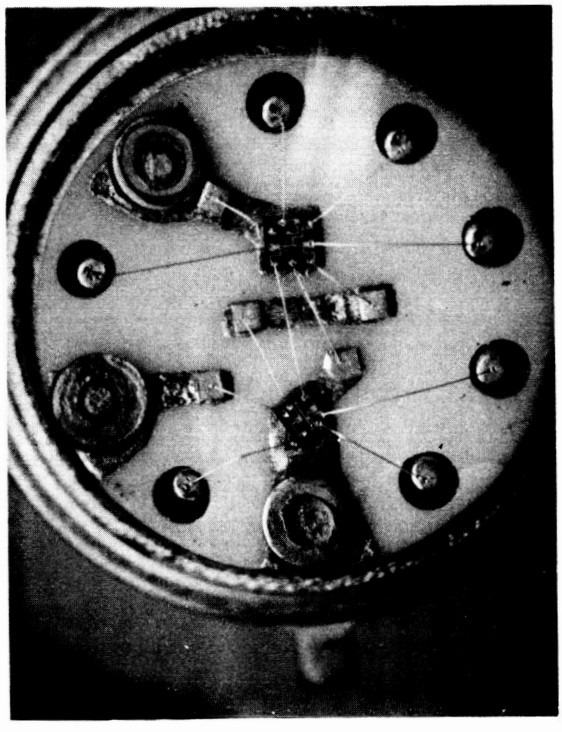
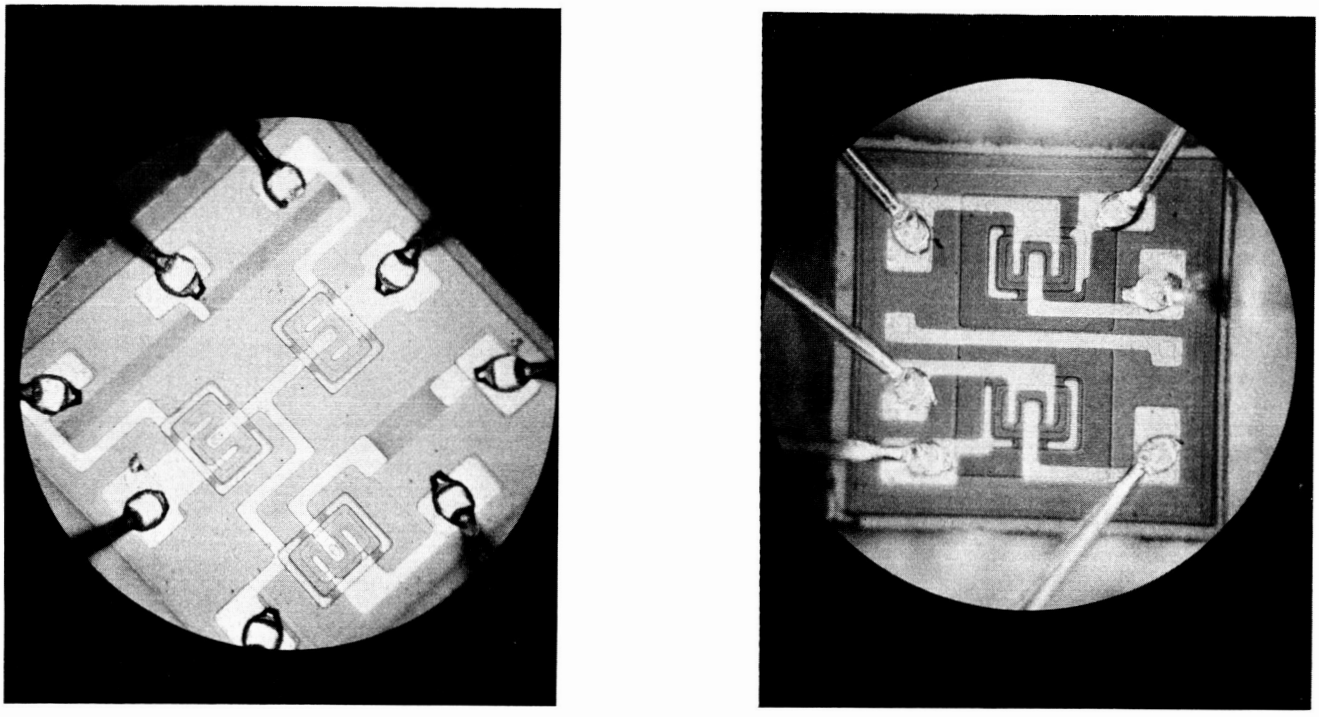


Figure 2-4. Photomicrograph of the MC-1519 Circuit



(a) Compatible Circuit Die (b) Monolithic Circuit Die

Figure 2-5. Photomicrograph of the MC-1519 Dies

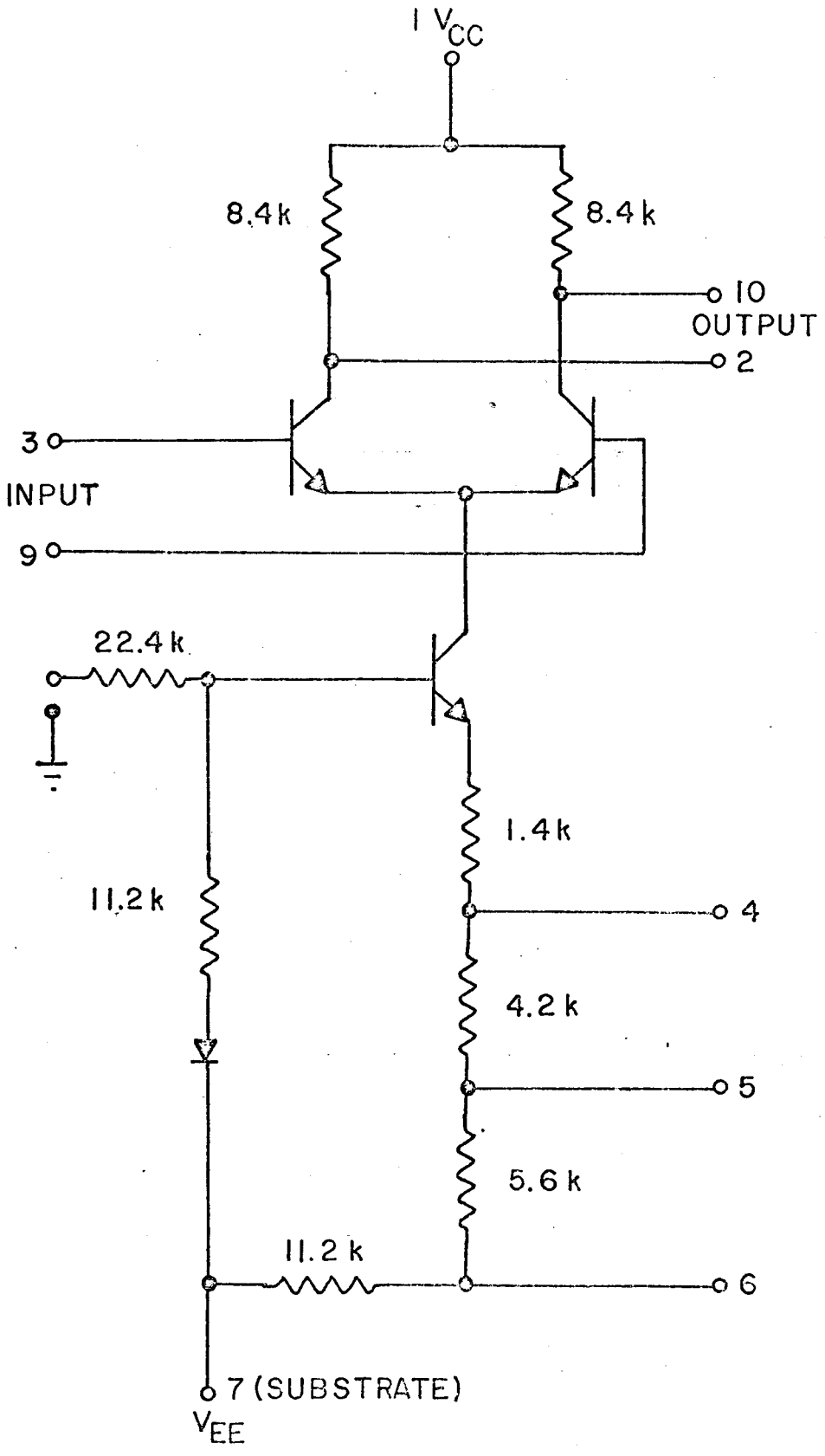


Figure 2-6. Schematic Diagram of MC-1525

V_{EE} make provision for selection of a current level appropriate to the intended use of the device (Figure 2-7).

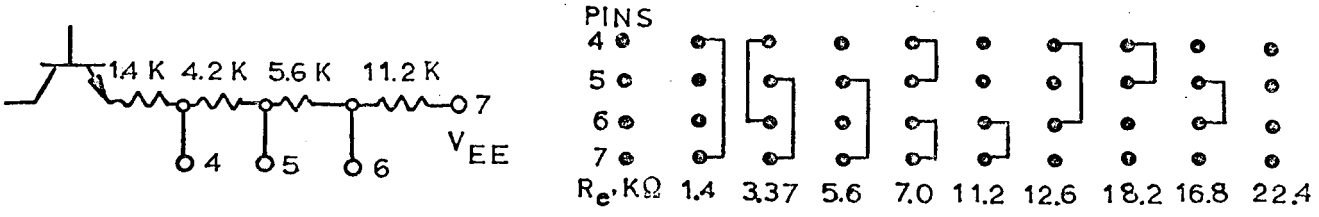


Figure 2-7. Effective Resistances in Current Source Emitter of MC-1525.

The MC-1525 is a monolithic integrated circuit having diffused resistors (Figure 2-8). The devices procured for this program are housed in the 1/4" x 1/4" alumina flat package.

2.1.3 Operational Amplifier - MC-1530

Such advantages as low offset voltage and current, excellent temperature tracking, increased reliability, small size and reduced cost make the integrated circuit operational amplifier more attractive than many discrete operational amplifiers now in use. On the other hand, many discrete operational amplifiers are of such high quality that their performance cannot yet be duplicated in the state-of-the-art of monolithic integrated circuit technology. For many operational amplifier applications, such as that of a summing amplifier, an integrator, a DC comparator or a transfer function simulator, the integrated circuit provides a reasonable compromise between desired performance and cost. Motorola's Operational Amplifiers, MC-1530 and MC-1531, are high performance, all-diffused integrated circuits, either of which may be fabricated from a single monolithic die by appropriate interconnections during manufacture. Like the MC-1525,

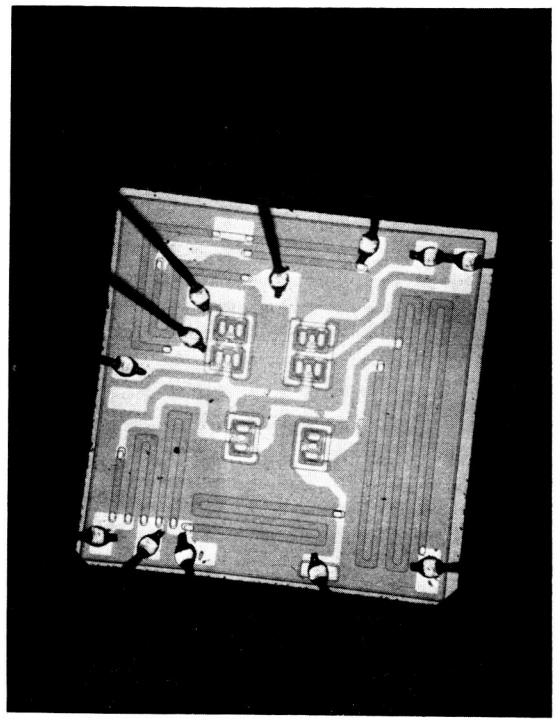


Figure 2-8. Photomicrograph of the MC-1525 Die

the circuits incorporate diode temperature compensation. Additionally, variation of the output voltage with temperature is reduced to a minimum because critical DC voltage levels within the circuits are a function of resistor ratios and are not dependent on the absolute values of any resistor or the beta of any transistor in the circuit. The MC-1530 has been selected for this program (Figure 2-9).

The MC-1530 is a monolithic integrated circuit having diffused resistors (Figure 2-10). The devices procured for this program are housed in the 1/4" x 1/4" alumina flat package.

2.1.4 Operational Amplifier - SN-526A

Texas Instrument's Amplifiers SN-525A and SN-526A are circuits either of which may be produced from a single "Master Slice" by appropriate interconnections during manufacture. The SN-526A has been selected for this program (Figure 2-11). It features Darlington high-impedance differential-input stages and a Class B output power amplifier. Differential amplifier outputs are also provided. These devices are packaged in a 1/4" x 1/8" welded package. More specific design detail will be included in later reports.

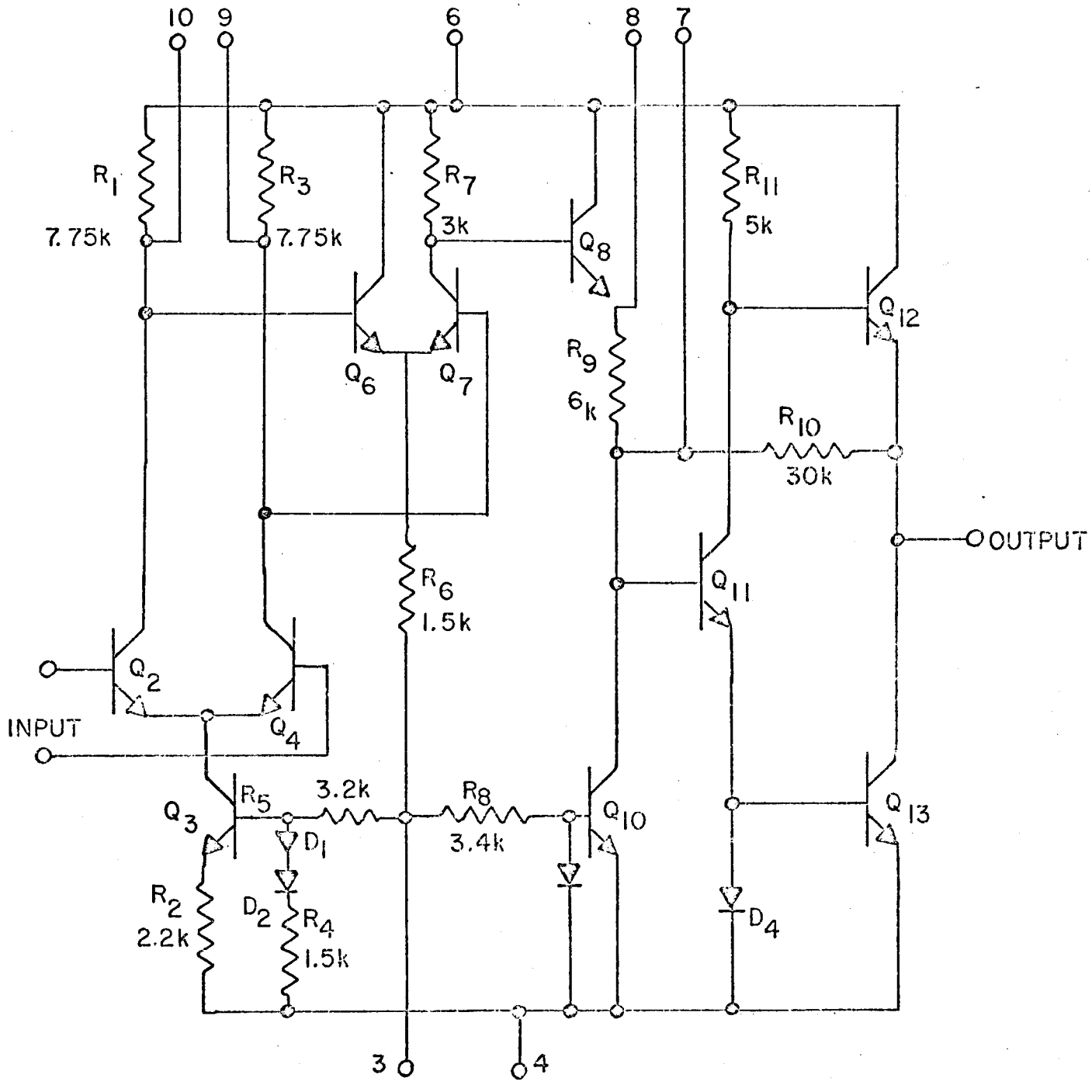


Figure 2-9. Schematic Diagram of MC-1530

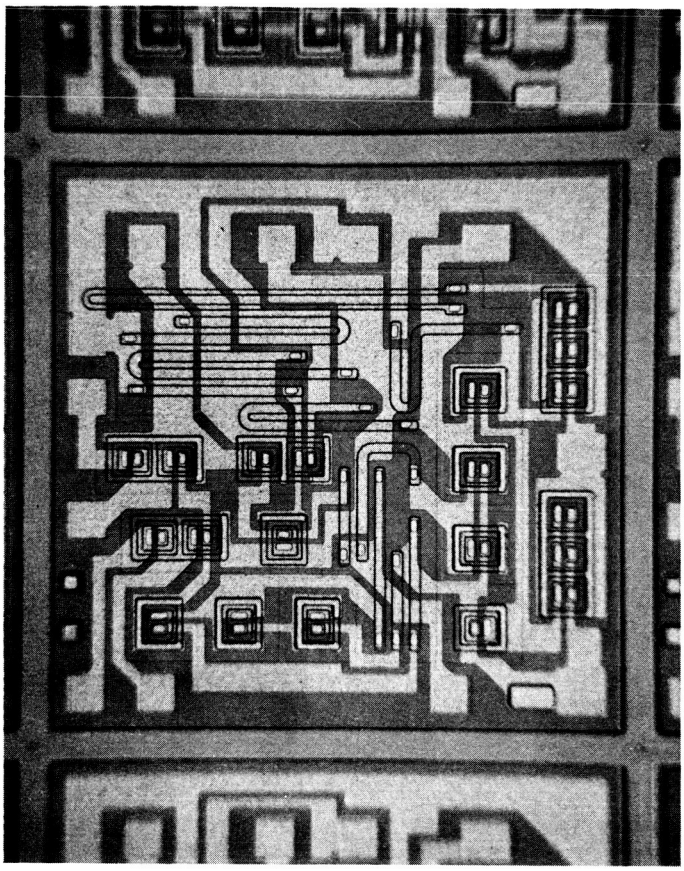


Figure 2-10. Photomicrograph of the MC-1530 Die

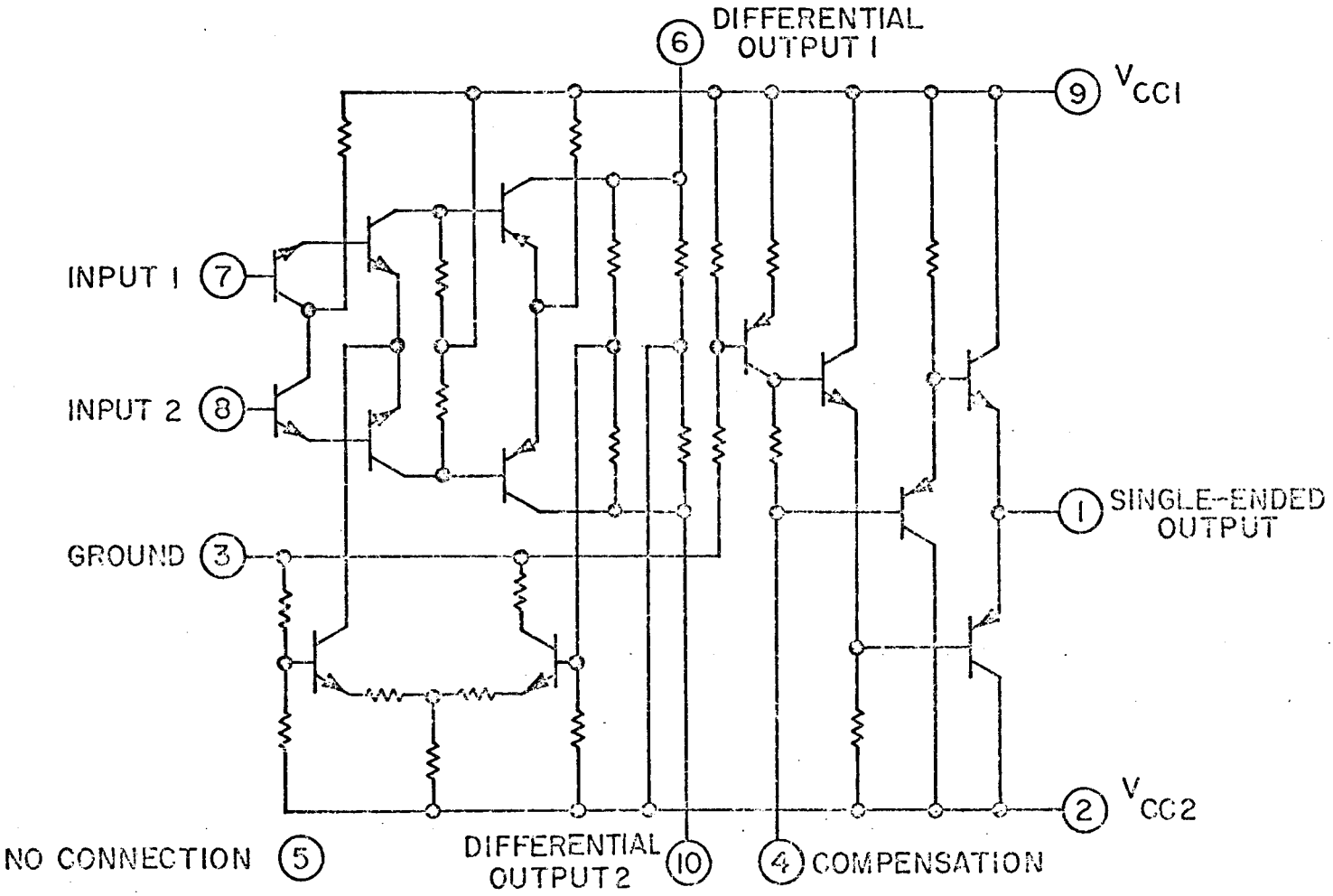


Figure 2-11. Schematic Diagram of SN-526A

3.0 ELECTRICAL CHARACTERISTICS

The configuration and constraints applicable to the measurement of the device electrical characteristics are discussed for the MC-1519 differential amplifier in this report. Similar information for the MC-1525, MC-1530, and SN-526A will be included in later reports.

3.1 Differential Amplifier - MC-1519

Figure 3-1 shows the circuit configuration employed in measuring the electrical characteristics of the MC-1519 in the common emitter (CE) mode. This circuit is incorporated in the the electrical test equipment used for performing the measurements except that the resistance bridge provided to supply base voltage at pin 6 has been replaced by an amplifier circuit which adjusts the voltage at pin 6 automatically. This adjustment provides the constant current flow through the input stage. This constant current then establishes the proper current and voltage levels in both the input (NPN) and the output (PNP) stages. For most parameter measurements in the CE mode, an output voltage of 0 Vdc is specified. When this condition is met, the constant current I_1 flowing through the current source has approximate values from 3.5 milliamperes for low-gain devices to 2.8 milliamperes for high-gain devices. Currents I_4 and I_5 are 4.45 milliamperes when pins 3 and 9 are at 0 Vdc to ground. Seven electrical characteristics of all devices are to be measured; two electrical characteristics of a limited sample are to be measured. In the measuring circuits described below, the amplifier symbol $\triangleright$ is used to designate the circuit as shown in Figure 3-1. The electrical characteristics are tabulated at the end of the description of the measuring circuits.

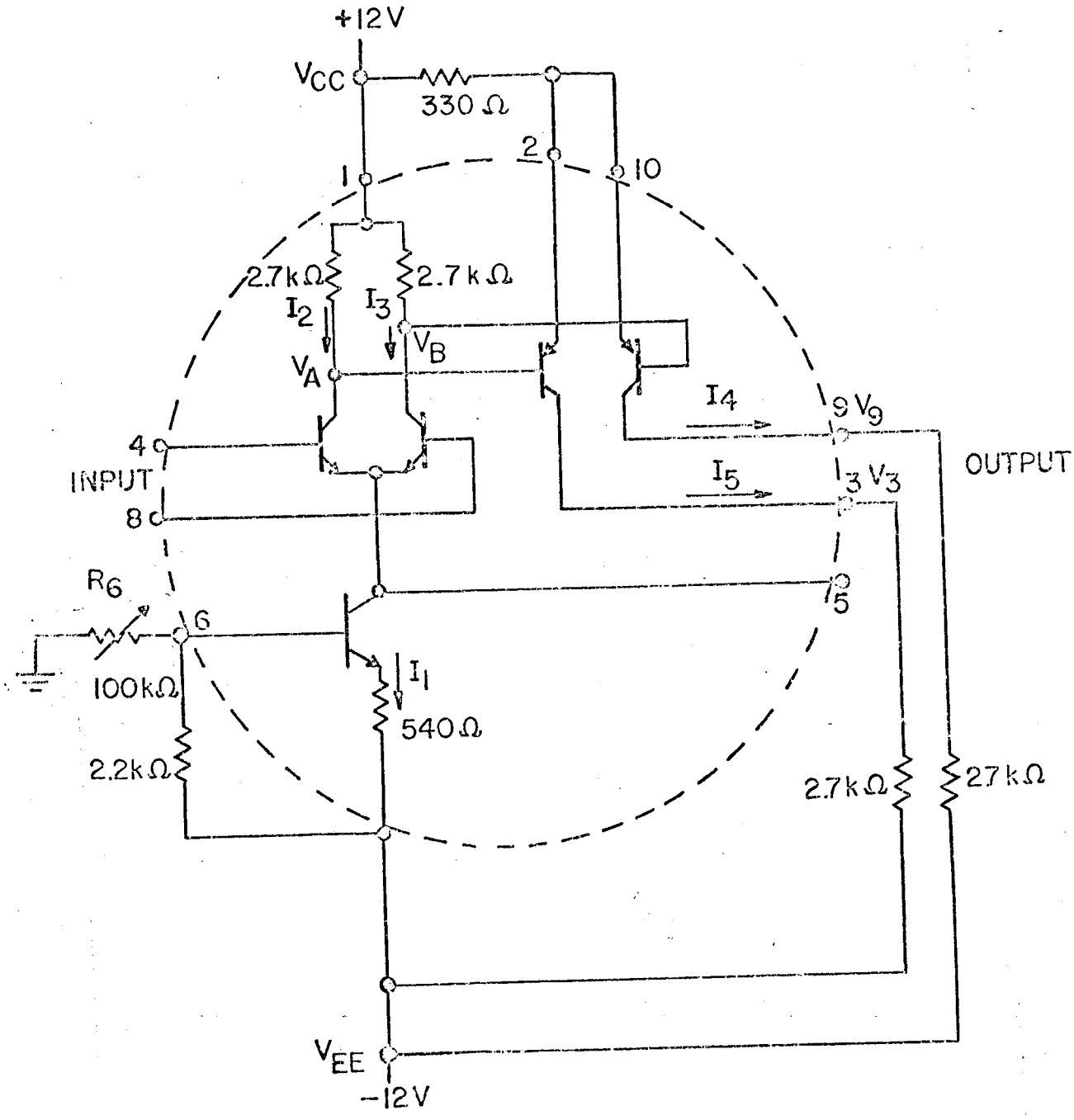


Figure 3-1. Schematic of MC-1519 in CE Mode

3.1.1 Input Current (I_i) and Input Offset Current (I_{io})

Figure 3-2 shows the circuit for measuring the base current of each input transistor. As shown, the base currents are measured individually and I_i and I_{io} determined by computation. These values will be determined for all devices.

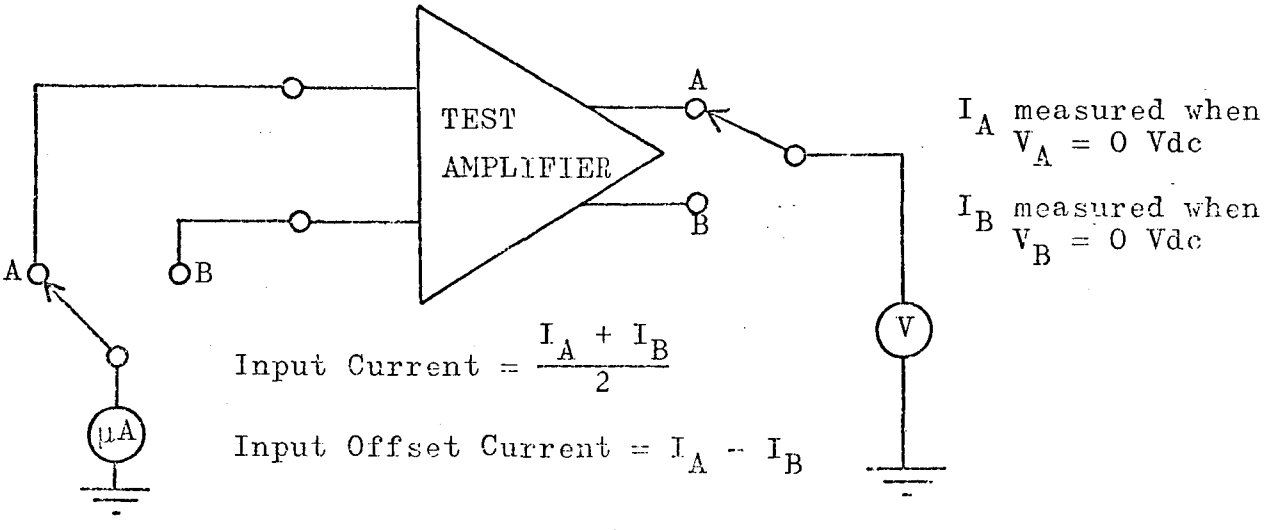


Figure 3-2. Input Current (I_i) and Input Offset Current (I_{io})

3.1.2 Input Offset Voltage (V_{io})

Figure 3-3 shows the circuit for measuring the input offset voltage. It is measured in mVdc. This value will be measured for all devices.

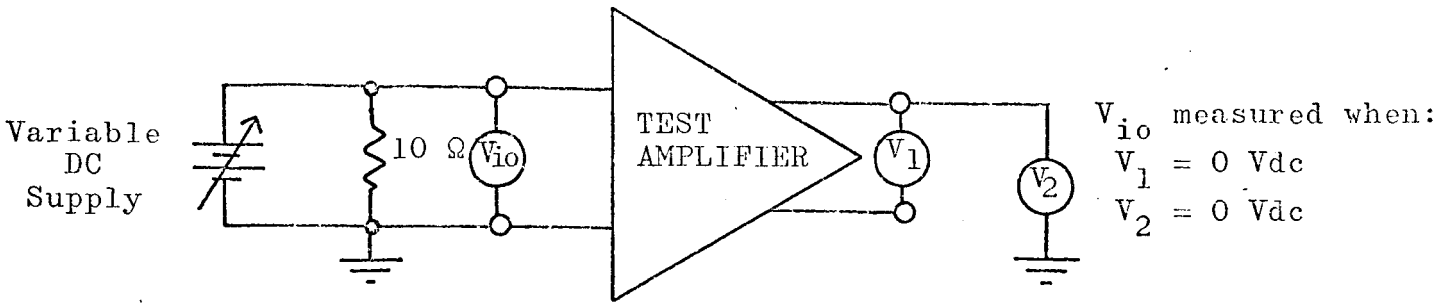
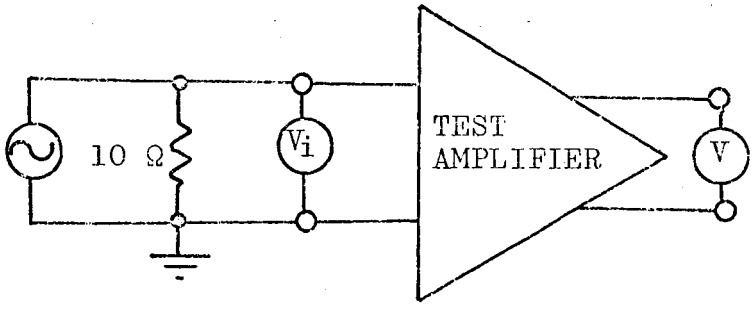


Figure 3-3. Input Offset Voltage (V_{io})

3.1.3 Differential Voltage Gain (A_{dd})

Figure 3-4 shows the circuit for measuring the output voltage from which the differential voltage gain is determined. V_{io} is applied before the oscillator is turned up. V is measured in volts rms. The other conditions of measurement are as shown in the figure. This value will be determined for all devices.



$$A_{dd} \text{ (ratio)} = \frac{V}{V_i}$$

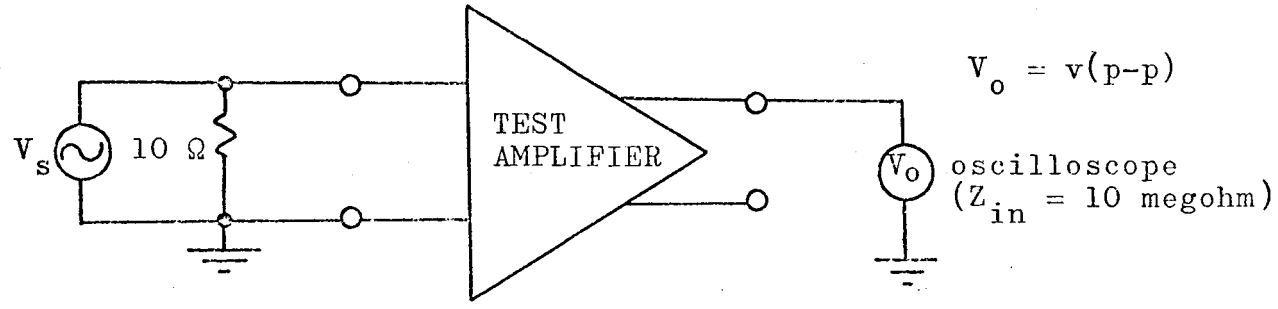
$$A_{dd} \text{ (db)} = 20 \log \frac{V}{V_i}$$

V_i = 1.0 mVrms at 1 kHz

Figure 3-4. Differential Voltage Gain (A_{dd})

3.1.4 Maximum Output Swing (V_o)

Figure 3-5 shows the circuit for measuring maximum output swing. V_{io} is applied before the oscillator is turned up. The other conditions are as shown in the figure. This value will be measured for all devices.

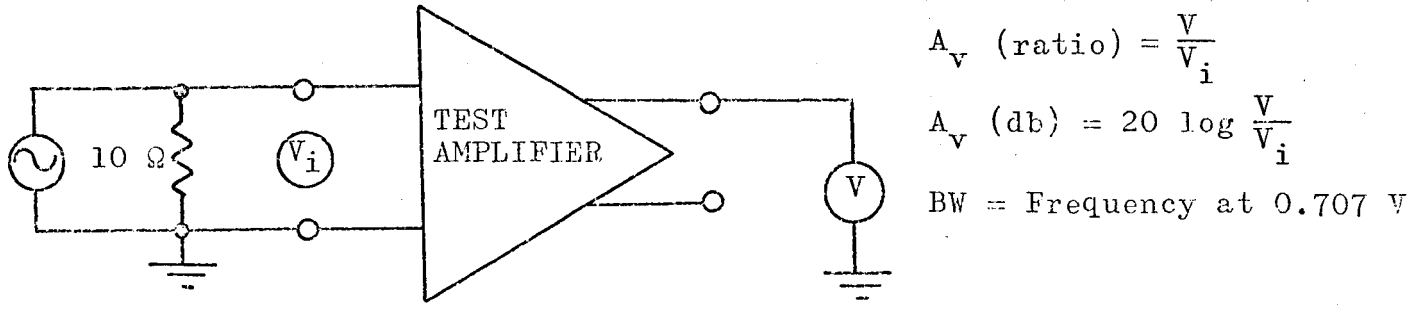


V_s increased until clipping of V_o observed at 1 kHz

Figure 3-5. Maximum Output Swing (V_o)

3.1.5 Single Ended Voltage Gain (A_v)

Figure 3-6 shows the circuit for measuring the output voltage from which the single ended voltage gain is determined. V_{io} is applied before the oscillator is turned up. V is measured in volts rms. The other conditions are as shown in the figure. This value will be determined for all devices.



A_v: V_i = 1.0 mV rms at 1 kHz

BW: Frequency increased until output voltage is 0.707 of value measured in A_v measurement (-3db)

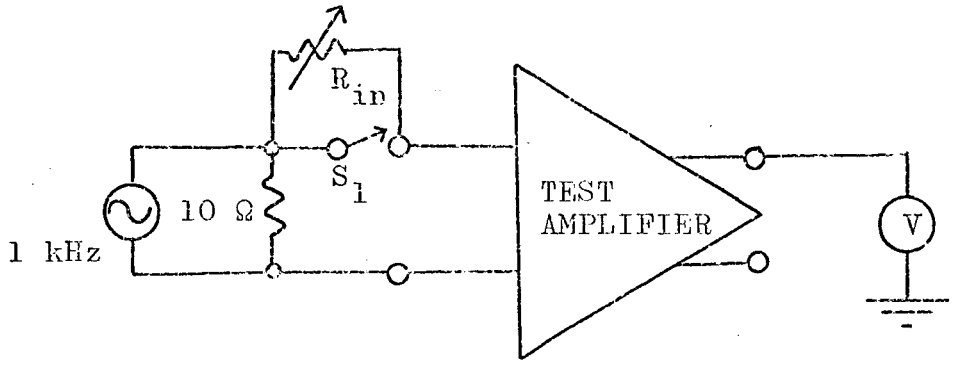
Figure 3-6. Single Ended Voltage Gain (A_v) and Bandwidth (BW)

3.1.6 Bandwidth (BW)

Figure 3-6 also shows the circuit for measuring bandwidth. If bandwidth is not measured in conjunction with the single ended voltage gain, all steps required for the A_v measurement are required to make this measurement except the computation of A_v. This value will be measured for all devices.

3.1.7 Differential Input Impedance (Z_{in})

Figure 3-7 shows the circuit for measuring the differential input impedance. V_{io} is applied before the oscillator is turned up. V_{io} is adjusted to maintain the proper input value as R_{in} is adjusted to achieve the 6 db loss of gain in output voltage. R_{in} is a decade resistor. The other conditions are as shown in the figure. This value is measured on a limited sample of devices.



$Z_{in} = R_{in}$ when R_{in} reduces V to 0.5 of value measured with S_1 closed (-6db)

Figure 3-7. Differential Input Impedance

3.1.8 Common Mode Rejection (CM_{Rej})

Figure 3-8 shows the circuit for measuring the output voltages from which the common mode gain (Acd) and the common mode rejection are determined. In making the measurements of output voltage, care must be taken to insure that the voltage at pin 6 is approximately the same value as the voltage at that point when making the V_{io} measurement. Two values of DC output voltage are measured and ΔV is found by subtraction. This value will be determined on a limited sample of the devices.

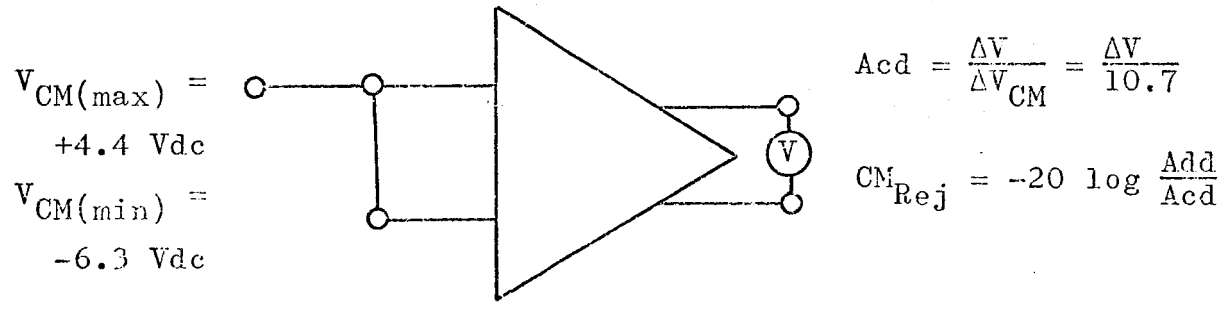


Figure 3-8. Common Mode Rejection

3.1.9 Electrical Characteristics to Be Measured

The electrical characteristics to be measured are tabulated in Table 3-1. Minimum, typical and/or maximum values are shown, where appropriate, for both the common emitter (CE) and the common collector (CC) mode.

3.1.10 DC Parameters

Several DC parameters of the MC-1519 will be measured during the test program. They are not discussed in detail or tabulated herein since they may not prove to be valid predictors of the reliability of linear integrated circuits. If the test results establish that the DC parameters can be correlated with the electrical characteristics

TABLE 3-1

ELECTRICAL CHARACTERISTICS OF MC-1519

(V_{CC} = +12 Vdc; V_{EE} = -12 Vdc; T_A = 25°C)

Characteristic	Figure No.	Symbol	Min.	Type	Max.	Unit
Input Current	5-2	I_i				μAdc
CE Mode				40.0	70.0	
CC Mode				60.0	90.0	
Input Offset Current	5-2	I_{io}				μAdc
CE Mode				1.0	4.0	
CC Mode				2.0	8.0	
Input Offset Voltage	5-3	V_{io}				mVdc
CE Mode and CC Mode				2.0	6.0	
Differential Voltage Gain	5-4	Add				db
CE Mode			67	73	79	
CC Mode			40	45	50	
Maximum Output Swing	5-5	V_o				v(p-p)
CE Mode			12.0	14.0		
CC Mode			8.0	10.0		
Single Ended Voltage Gain	5-6	A_v				db
CE Mode				67		
CC Mode				38		
Bandwidth (-3db)	5-6	BW				MHz
CE Mode			0.7	1.0		
CC Mode			5.0	8.0		
Differential Input Impedance	5-7	Z_{in}				kΩ
CE Mode			1.8	2.6		
CC Mode				1.2		
Common Mode Rejection	5-8	CM_{Rej}				db
CE Mode				89.0		
CC Mode				86.0		

or can be useful in the prediction of degradation or failure rates in reliability programs, the parameters will be described and reported in detail in later reports.

4.0 TEST PROGRAM

This program will be performed on the four integrated circuit amplifiers described in Section 2. The program includes 200 samples of each type. The tests that these samples will be subjected to are summarized in Table 4-1. A more detailed explanation of each test procedure is found in the following sections.

4.1 Operating Life Tests

Three operating life tests are listed in Table 4-1. Since each of Motorola's circuits can be operated at many circuit power levels, the specific test circuit for tests 1 and 2 will be a non-functional test with normal bias applied. Test 2 is considered to be a control sample. Test 3 will consist of testing these circuits at the maximum permissible temperature and at an accelerated power level. Each test will be performed for a minimum of 1000 test hours and will be extended to 4000 hours, time permitting. Each device under test will be, at regular intervals, removed from the stress test, allowed sufficient time to return to room temperature, and then read electrically for those parameters which are determined to be critical to the proper operation of the device. Regular test intervals will be at 125, 250, 1000 hours and at each 1000 hours thereafter. Failure analysis will be conducted immediately on verified catastrophic failures (opens and shorts). However, on samples exhibiting abnormal parameter degradation that is less than catastrophic, no failure analysis will be performed until enough readouts are accumulated to verify failure and to define the rate of degradation occurring.

An analysis of critical stresses on the circuit elements in the MC-1519 under the operating life test conditions is found in Section 6. Similar analyses on each of the remaining devices will be included in subsequent reports.

TABLE 4-1

PROGRAM TEST PLAN

TEST STRESSES	DEVICE TYPES			
	MC-1519	MC-1525	MC-1530	SN526A
	Number of Samples for Each Test			
OPERATING LIFE TESTS				
(1) Elevated Ambient	25	25	25	25
(2) Room Ambient	15	15	15	15
(3) Elevated Ambient Accelerated Power	25	25	25	25
STORAGE	15	15	15	15
STEP STRESS TESTS				
(5) Temperature	15	15	15	15
(6) Power ($T_A = 25^{\circ}C$)	15	15	15	15
(7) Temperature - Power	15	15	15	15
(8) Temperature Cycling	15	15	15	15
MIL-S-19500 TEST SEQUENCES				
(9) Mechanical	25	25	25	25
(10) Thermal	25	25	25	25
SPECIAL STUDIES	10	10	10	10

4.1.1 Test 1 - Elevated Ambient - Bias Life Test

Each Motorola circuit selected for this program has been evaluated electrically to determine its applicability to variable power stress testing. Each circuit can be stressed at power levels greater than normal operational would generally require. This test procedure is designed to determine the life reliability characteristics for each circuit at a minimum stress level.

4.1.2 Test 2 - Room Ambient - Bias Life Test

This test will be performed as a control test and the electrical bias conditions will be identical to those used in test 2. The test ambient will be maintained at room temperature.

4.1.3 Test 3 - Elevated Ambient - Accelerated Bias Life Test

The purpose of this test is to accelerate normal failure modes at junction temperatures in excess of the rated conditions for this package. Each circuit will be biased at the 300 mW power level (maximum power level for the MC-1525). The temperature of these tests will be maintained at the chamber temperature of 125°C.

4.1.4 Test 4 - Storage Life Test

This test will be performed at the ambient temperature of 150°C. It will consist of placing the devices, unbiased, in a test chamber and periodically withdrawing them from the chamber for parameter reading. A minimum of four hours will be allowed between the time the device removal from temperature stress to the time that the test sample's electrical parameters will be read.

4.2 Step Stress Tests

Step stress testing is a technique utilizing small samples, subjected to successively increasing levels of stress, to obtain a

maximum amount of reliability information in a relatively short period of time. The testing stress usually used in evaluations of this nature will be any combination of temperature or power or voltage. The technique is not restricted to these methods of testing and is often applied to mechanical tests as well.

The techniques that Motorola proposes in Table 4-1 are explained in this section. Intermediate readings will be taken after each step.

4.2.1 Test 5 - Temperature Step Stress Test

The devices to be stressed in this manner will be stored at each stress temperature for 48 hours. The initial step will be set at 150°C for the TO-5 package circuits and 200°C for the flat package circuits. After each stress, the surviving circuits will be stressed at a level 25°C higher than the previous step. Each test will be continued until more than 67 percent of the sample has failed.

4.2.2 Test 6 - Power Step Stress Test

Each circuit will be stressed at the room ambient temperature by varying the power dissipated in a controlled manner. The devices will be subjected to 48 hours of testing at each stress level. The initial power level will be zero milliwatts and each successive step will increase by 100 milliwatts. The test will continue until either 67 percent of the sample has failed, the equipment limitations have been reached, or the circuit limitations have been reached. All devices passing at one stress level will be subjected to the next programmed stress level.

4.2.3 Test 7 - Temperature - Power Step Stress Test

The procedure to be used in this test is identical with that defined for test number 6 except that the ambient temperature will be set at 125°C.

4.2.4 Test 8 - Temperature Cycling

Each sample will be subjected to 10 cycles of temperature cycling per the procedure listed in Mil-Std-202C except that the temperature extremes will be varied for each step in the program as follows:

Step 1	$-55^{\circ}C$ to $150^{\circ}C$
Step 2	$-55^{\circ}C$ to $+175^{\circ}C$
Step 3	$-55^{\circ}C$ to $+200^{\circ}C$
Step 4 to Step n	$-55^{\circ}C$ to T_n when less than 33 percent of the initial sample remains good or until equipment limit has been reached.

4.3 MIL-S-19500 Test Sequences

Standard integrated circuits are normally expected to pass the two environmental test sequences listed in Mil-S-19500. To verify that this capability still exists in this product, this sequence of testing is added to the test program. Intermediate readings will be taken after each test.

4.3.1 Test 9 - Mechanical Test Sequence

The mechanical test sequences and their detailed procedures are as follows:

4.3.1.1 Shock Test

The shock test is intended to determine the suitability of devices for use in electronic equipment that may be subjected to moderately severe shocks, resulting from suddenly applied forces or abrupt changes in motion produced by rough handling, transportation

or field operation. The shock test is usually performed by rigidly mounting the device under test in a fixture on a carriage between vertical guide rods. The carriage is raised and dropped. The height from which the carriage is dropped and the nature of the pad upon which it drops determine the shock level and period. This shock test is repeated five times along each of three axes, x_1, y_1, z_1, at a shock level of 1500 "G."

4.3.1.2 Constant Acceleration

The constant acceleration test is an "accelerated" test designed to detect types of structural and mechanical weaknesses not necessarily detected in shock and vibration tests. The device under test is mounted in a jig on the periphery of a rotating member. The rotational speed and radius from the devices under test to the rotational axis determine the acceleration level of 20,000 G.

4.3.1.3 Vibration Fatigue

The purpose of this test is to determine the effect of prolonged vibration on the device. The integrated circuit device under test is rigidly mounted on a vibration table, and then subjected to a simple harmonic motion at approximately 60 cps with a constant peak acceleration of 20 G minimum for a period of 32 hours in each of three mutually perpendicular orientations for a total of 96 hours.

4.3.1.4 Vibration Variable Frequency

This test is performed for the purpose of determining the effect on devices of vibration through a constantly varying frequency range. The integrated circuit is rigidly fastened to a vibration platform and then vibrated at a constant peak acceleration of 20 G. The vibration frequency is varied approximately logarithmically

between 100 and 2000 cps. The entire frequency range of 100 to 2000 cps and return to 100 cps is traversed in not less than 4 minutes. This cycle is performed four times in each of three mutually perpendicular planes.

4.3.2 Test 10 - Thermal Test Sequence

The thermal test sequence and the individual test procedures are as follows:

4.3.2.1 Solderability

This test is designed to determine both the ability of the integrated circuit to withstand the high temperature encountered during soldering and to determine how well the leads are wetted to solder. The test is performed by dipping the package leads into molten 60--40 lead-tin solder at 230°C to a point 1/6 inch from the body of the package for a period of 10 seconds. The circuits are tested for electrical parameters to determine if the test caused any characteristic changes and then are examined under a microscope to determine if the leads have been adequately coated with solder.

4.3.2.2 Temperature Cycling

The temperature cycling test is conducted to determine the resistance of the integrated circuit to repeated exposure to extremes of high and low temperature. A typical temperature cycling test for integrated circuits consists of 30 minutes at -65°C, 5 minutes at +25°C, 30 minutes at +175°C, 5 minutes at +25°C, and return to -65°C. This high and low temperature sequence is repeated five times.

4.3.2.3 Thermal Shock

This test is similar to temperature cycling, except that the transfer time from the extreme temperature is shorter. This test is often referred to as "glass strain." The standard test for evaluating integrated circuits used 0^{o} and $100^{o}C$ as extreme temperature limits. The transfer time must be less than 5 seconds. This test is run for five cycles.

4.3.2.4 Moisture Resistance

The purpose of the moisture resistance test is to evaluate, in an accelerated manner, the resistance of integrated circuits to high humidity and temperature conditions. The test period is 10 days, during which the integrated circuit in a chamber is subjected to temperature cycles between $+10^{o}$ and $+65^{o}C$ at a relative humidity of between 90 and 98 percent.

These test procedures are described in detail in Mil-Std-750 -- TEST METHODS FOR SEMICONDUCTOR DEVICES.

At the completion of these standard tests, the survivors from these samples (tests 9 and 10) will be equally divided into three samples and will be stressed, in steps, as fcllows:

A. Temperature Cycling Step Stress Test
Using the same time sequences performed in the standard test sequence, referred to in test 9, 10 cycles will be performed at each step, with parameter readings performed after each step, until more than 50 percent of the sample has failed or the equipment limitations have been reached.

1st Step	$-55^{o}C$ to $+175^{o}C$
2nd Step	$-55^{o}C$ to $+200^{o}C$
Ath	$+25^{o}C$

B. Shock Step Stress Test

10 shocks in each axis (x_1, y_1, z_1) will be performed in stress steps of:

3,000 G	0.2 millisecond
10,000 G	0.2 millisecond

with parameter readings to be made after each step.

C. Vibration Variable Frequency Step Stress Test

The sample will be subjected to increased steps of stresses using the same procedure as outlined to be performed in the variable frequency vibration test stress except that the stress levels at each step will be as follows:

Step 1	30 G
2	50 G
3	70 G
4	80 G
5	90 G
6	100 G

Such parameter readings as is necessary to determine whether the die and leads are intact will be taken after each step in the stress sequence. Complete electrical parameter data will be taken at the beginning and at the end of the program.

4.4 Special Studies

These samples are reserved for studies such as thermal electrical characterization through infrared techniques and other special investigations to be determined jointly by NASA-Huntsville and Motorola.

5.0 SURVEY OF RELIABILITY LITERATURE

The requirements of this program include a survey of published literature to determine the physical failure mechanisms that will most likely occur in an integrated circuit. Motorola is currently conducting this survey and, even though it is not complete, it has progressed far enough to utilize available cross sections of industrial knowledge in evaluating the methods of testing performed in this program. This research literature so far has spread to over 80 different publications, including the Physics of Failure Conference sponsored by RADC yearly for the last 4 years and the proceedings of the Second Physics of Failure Colloquium presented by Autonetics, Division of North American Aviation. The results of many other study programs, published articles, and reports on programs specifically applicable to integrated circuits are currently being reviewed. The results of this study will be summarized and tabulated in the Second Quarterly Report.

6.0 LIFE TEST CIRCUITS

This section presents the electrical circuit that will provide the electrical power in the operational life test and subsequent accelerated electrical stress testing. All life tests will be DC biased tests designed to accelerate known failure mechanisms historically proven to exist in integrated circuits, and to consider the methods of accelerating these failure modes that are the most compatible with quality assurance methods and can be acceptable to most integrated circuit manufacturers. Past experience has indicated, in the field of digital circuits, that in the vast majority of cases a combination of DC bias with temperature acceleration will provide the most significant amount of reliability data for these integrated circuits. It is true that, while the functional type of operating life test is more attractive to the circuit designer, as the circuits become more complex, basic decisions have to be made to compare what is known about the physics of the particular failure mechanism, the means to stress these physical failure mechanisms, with the cost factor in providing burn-in facilities if it is desired to obtain "high-rel" parts at an economical cost. Figures 6-1, 6-2, and 6-3 give general simplified schematic diagrams of the test circuit anticipated to be used for testing the MC-1525, MC-1530, and the SN-526A devices at the lower power levels. Analysis of the stress applied to each element within the integrated circuit has not been completed on all circuits at this time. This section presents a detailed analysis of anticipated stress levels within the MC-1519 differential amplifier. A similar analysis of the other circuits will be included in subsequent reports.

6.1 Analysis of the MC-1519 Operational Life Test Circuit

The circuit selected for the MC-1519 at the 100 and 300 milliwatt levels is a DC biased operational life test with controlled

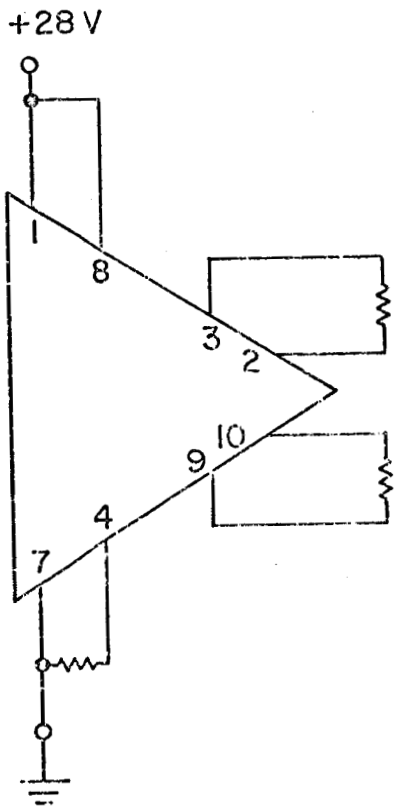


Figure 6-1. Life Test Circuit for MC-1525 Device (100 mW)

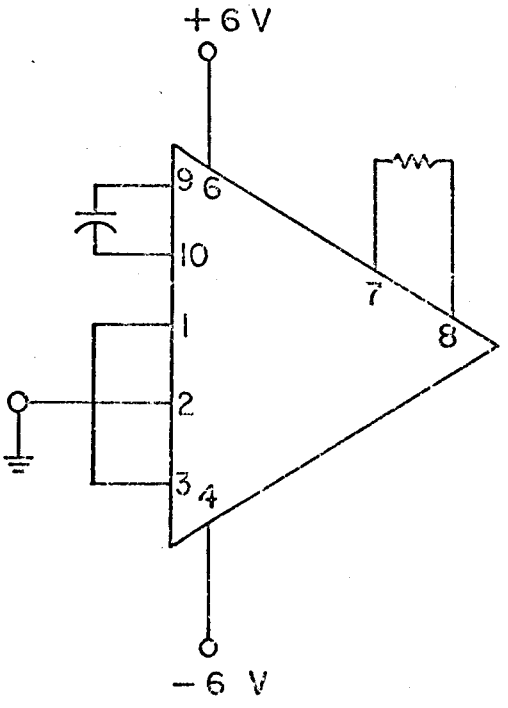


Figure 6-2. Life Test Circuit for MC-1530 Device

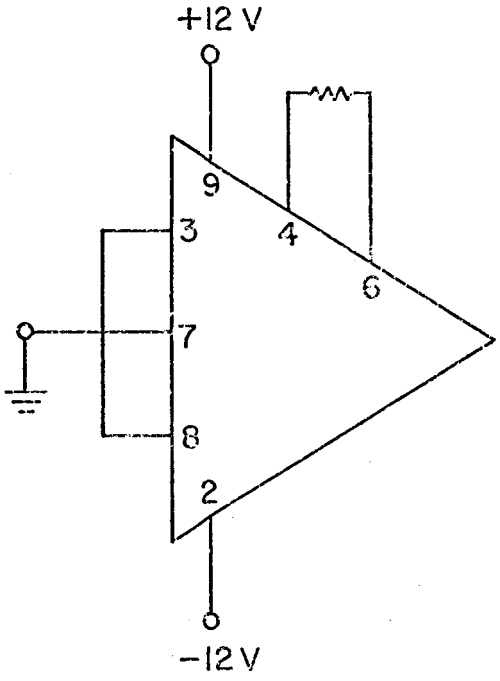


Figure 6-3. Life Test Circuit for SN526A Device

stresses applied to various regions in the devices. The basic technique utilized here fixes the stress levels by fixing the voltages at two different points in the circuit. The electrical schematics are shown in Figure 6-4 and 6-5. In these circuits we have identified each circuit element by notations that aid in the analysis that follows. One of the significant features in this test design is that it encompasses a considerable degree of simplicity and duplicates, statically, the stresses that the elements of the circuit are expected to see under normal operational performance. The circuits shown in Figures 6-4 and 6-5 are quite similar to the basic electrical parameter test circuit required to perform differential gain, input offset voltage, and other electrical measurements. Differences occur only in the sense that the collector of the differential pair of PNP transistors is connected to pin 5 instead of the V_{EE} supply, permitting circuit power control by the transistor labeled Q_5 in the diagram. This permits a logical extension in high power levels beyond 300 milliwatts for the power step stress bias conditions by extending these collector leads to the V_{EE} supply.

As is noted in these circuit schematics, the bias levels are controlled by grounding the base input terminal of transistors Q_1 and Q_2 (pins 4 and 8) and by establishing the proper bias level at pin 6 to control the total current flow through R_3. These factors permit, with minor modifications, the adaptation of this circuit to a high volume screen burn-in requirement. If the voltage at pin 6 is fixed at a level determined to give x milliwatts of power, assuming an absolute value of R_3 equaling 540 ohms, than the total distribution of power in any population of devices subjected to this burn-in stress will then see power conditions proportional to the distribution of resistance values for these circuits. Normally,

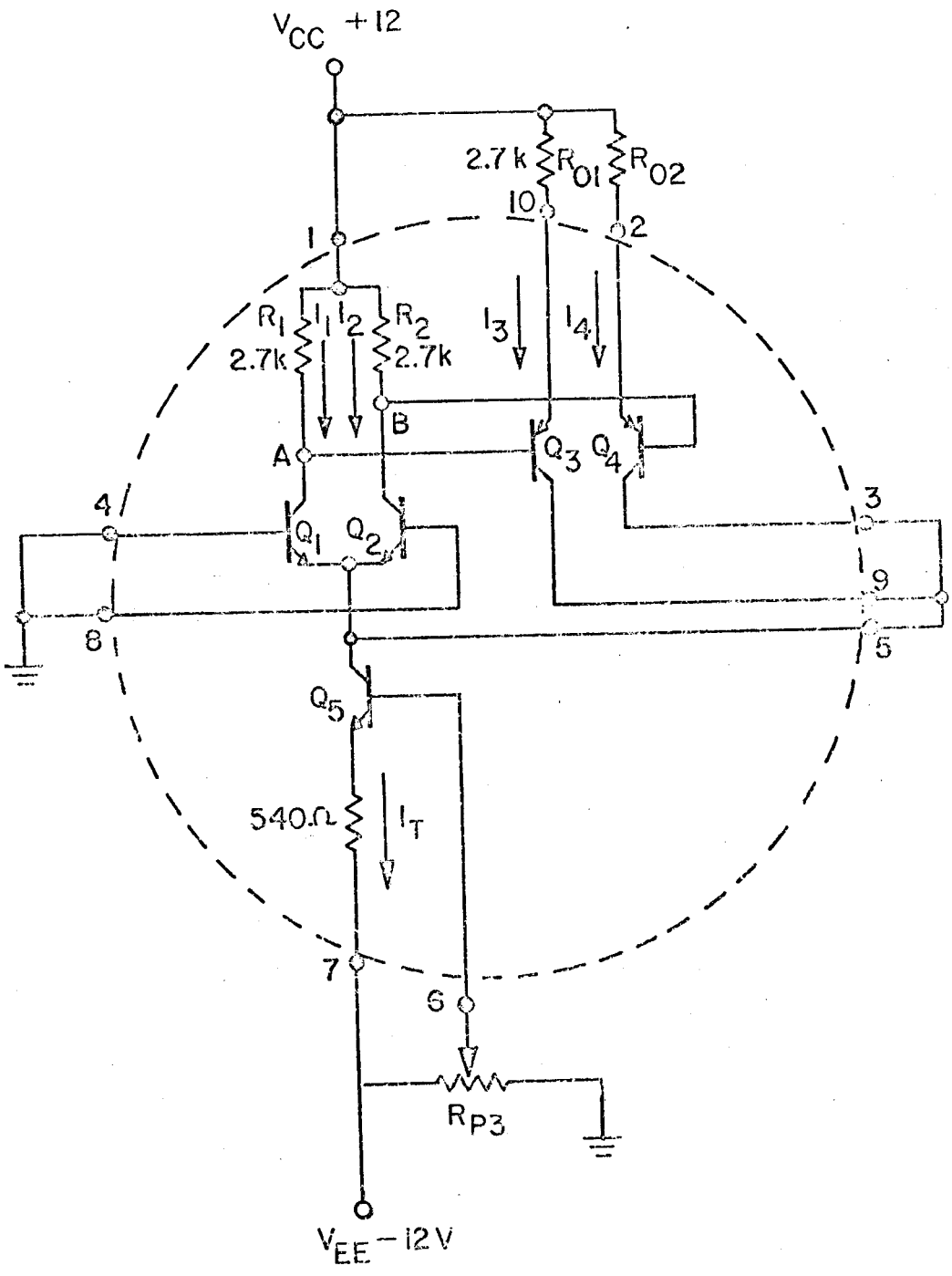


Figure 6-4. 100-Milliwatt Life Test Circuit for MC-1519

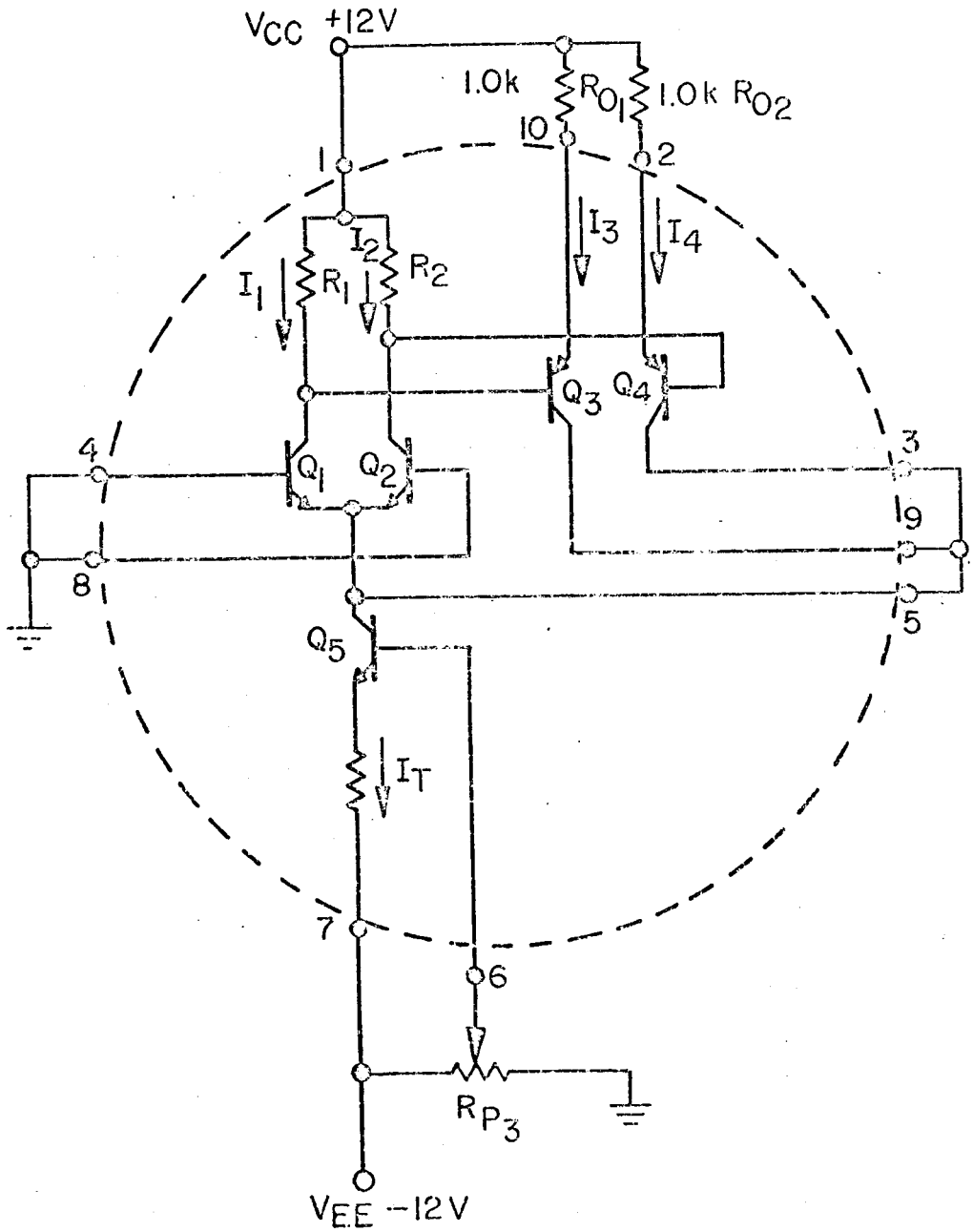


Figure 6-5. 300-Milliwatt Life Test Circuit for MC-1519

in the manufacture of integrated circuits, the diffused resistor tolerances are sought to be less than ±20 percent. In this circuit, because its resistors are nichrome deposited thin film, the distribution of power levels should be much better. However, this reliability study program will include a variable potentiometer in our network which will permit the final adjustment of the value of I_T for each circuit so that the total power of the circuit can be set at the exact level desired. A description of the circuit functions and a breakdown of the power dropped across each circuit component follows in the next two sections.

6.1.1 100 Milliwatt Life Test Circuit

The circuit for this test is shown in Figure 6-4. The power dissipated in this circuit is equal to the total circuit current flow (i.e., through R_3) times the applied voltage ($V_{CC} - V_{EE} = 24$ volts) minus the power consumed in the external load resistors Ro_1 and Ro_2. It can be defined as follows:

$$Pd_T = Pd_{Ro} + Pd_c$$

where Pd_T is total circuit power consumption

Pd_{Ro} is power lost in the load resistors

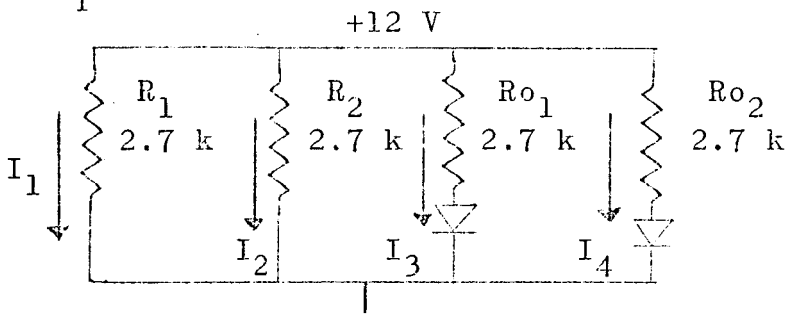
Pd_c is power used in MC-1519 circuit

$V_{CC} = +12$ Vdc

$V_{EE} = -12$ Vdc

$$Pd_T = I_T (V_{CC} - V_{EE}) = 24 I_T$$

Considering the load circuits of R_1, R_2, Ro_1, and Ro_2 to be as follows and equal to I_T



then it is seen that the current drain in the output load resistors will equal R_1 or R_2 minus a factor equal to:

$$\frac{V_{BE}}{2.7\ k\Omega} = 0.27\ mA$$

Since $I_1 + I_2 + I_3 + I_4 \approx I_T$

then $$I_T = 4I_3 + 0.54\ mA$$

and $$I_3 = \frac{I_T - 0.54\ mA}{4} \qquad (1)$$

$$Pd_{Ro} = I_3^2\ Ro + I_4^2\ Ro = 2I_3^2\ Ro$$

$$Pd_{Ro} = \frac{Ro}{8}\ (I_T - 0.54\ mA)^2$$

Then

$$Pd_c = 24I_T - \frac{Ro}{8}\ (I_T - 0.54\ mA)^2 \qquad (2)$$

In this circuit it is necessary to set Pd_c and control I_C by raising and lowering the voltage drop at pin 6. If it is assumed that

R_3 = 540 ohms
Pd_c = 100 milliwatts
$Ro = R_1 = R_2$ = 2.7 k ohms

Then equation (2) can be rearranged as follows:

$$\frac{Ro}{8}(I_T - 0.54\ mA)^2 - 24\ I_T + 100 = 0$$

$$I_T^2 - 2(0.54 \times 10^{-3})(I_T) + (0.54 \times 10^{-3})^2$$

$$-\frac{(24)8}{Ro}\ I_T + \frac{(0.1)8}{Ro} = 0$$

$$I_T^2\left[-2(0.54 \times 10^{-3}) + \frac{(24)8}{Ro}\right] I_T + (0.54 \times 10^{-3})^2 + \frac{(0.1)8}{Ro} = 0$$

$$I_T = \frac{\left[2(0.54 \times 10^{-3}) + \frac{(24)8}{Ro}\right] - \sqrt{\left[2(0.54 \times 10^{-3}) + \frac{(24)8}{Ro}\right]^2 - 4\left[(0.29 \times 10^{-6} + \frac{(0.1)8}{Ro}\right]}}{2}$$

$$I_T = \frac{72.19 \times 10^{-3}}{2} - \frac{\sqrt{5.211 \times 10^{-3} - 1.186 \times 10^{-3}}}{2}$$

$$= \frac{72.14 \times 10^{-3}}{2} - \frac{\sqrt{4.025 \times 10^{-3}}}{2}$$

$$= \frac{72.19 - 63.44}{2} \times 10^{-3} = \frac{8.75 \times 10^{-3}}{2}\ \text{Amps}$$

$$I_T = 4.37\ mA$$

From equation (1):

$$I_3 = \frac{I_T - 0.54\ mA}{4} = \frac{3.83}{4}\ mA$$

$$= 0.96\ mA$$

To calculate the theoretical value of the pin 6, it is only necessary to convert the equation for I_T in terms of V_6 (voltage at pin 6).

$$I_T = \frac{V_{EE} - (V_6 - 0.7\ V)}{R_3} = \frac{V_{EE} - V_6 + 0.72\ \text{volts}}{540\ \text{ohms}}$$

$$V_6 = V_{EE} + 0.72\ \text{volts} + 540\ I_T$$

$$= -12\ V + 0.72\ V + (540)(4.37\ mA)$$

$$= -11.28 + 2.36$$

$$= -8.92\ \text{volts}$$

In all these calculations, the voltage is referenced to the 0 voltage potential at pins 4 and 8 and that the forward voltage drop (base-emitter) V_{BE} is assumed to be 0.72 volt. Using the typical values for the circuit components and the calculated value of I_T, estimates of the power dissipated by each circuit element can be calcaulated. They are:

A. Resistor R_3

$$Pd_{R_3} = (I_T)^2\ R_3 = (4.37)^2\ (0.54) \times 10^{-3}\ mW$$

$$= 10.3\ mW$$

B. Transistor Q_5

$$V_{CE} = V_6 \text{ for all power levels}$$

$$Pd_{Q_5} = V_{CE} \times I_T = V_6 \times I_T = (8.92\ \text{volts})(4.37\ mA)$$

$$= 38.98\ mW$$

C. Transistors Q_1 and Q_2

Neglecting the incremental increase in collector currents resulting from the base currents of transistors Q_3 and Q_4 because they will contribute less than 2 percent of the transistor currents for Q_1 and Q_2

$$V_{CE_{Q_1}} = V_{CC} - (2.7\ k\Omega)(0.96\ mA + 0.27\ mA) + 0.72\ volt$$

$$= 9.4\ volts$$

$$Pd_{Q_1} = Pd_{Q_2} = I_1 \times V_{CE_{Q_1}} = (1.23\ mA)(9.4\ V)$$

$$= 11.6\ mW$$

D. Transistors Q_3 and Q_4

Because the collector voltages of transistors Q_1 and Q_2 are clamped by the V_{BE} diodes of the PNP transistor, it then follows:

$$V_{CE_{Q_3}} = V_{CE_{Q_4}} = V_{CE_{Q_1}} + 0.72\ V = 10.1\ V$$

Then

$$Pd_{Q_4} = Pd_{Q_3} = I_3 \times V_{CE_{Q_3}} = 10.1\ V \times 0.96\ mA$$

$$= 9.7\ mW$$

E. Resistors R_1 and R_2

$$I_1 = I_2 = 1.23\ mA$$

$$R_1 = R_2 = 2.7\ k\Omega$$

$$Pd_{R_1} = Pd_{R_2} = (1.23)^2(2.7) \times 10^{-3}$$

$$= 4.07\ mW$$

A summary of the power dissipation characteristics would be:

Transistor Q_1 = 11.6 mW
Transistor Q_2 = 11.6 mW
Transistor Q_3 = 9.7 mW
Transistor Q_4 = 9.7 mW
Transistor Q_5 = 39.0 mW

Resistor R_1 = 4.07 mW
Resistor R_2 = 4.07 mW
Resistor R_3 = 10.3 mW

In analyzing this 100 milliwatt test setup, it is noted that all transistors are set at such a level that they have a minimum of 9.0 volts collector to emitter, that the monolithic chip with the nichrome resistors is stressed with 80 percent of the power or 80.5 milliwatts and that this factor is very nearly in proportion to the ratio of the cross-sectional areas of the two die in question. This ratio being approximately equal to 3:1.

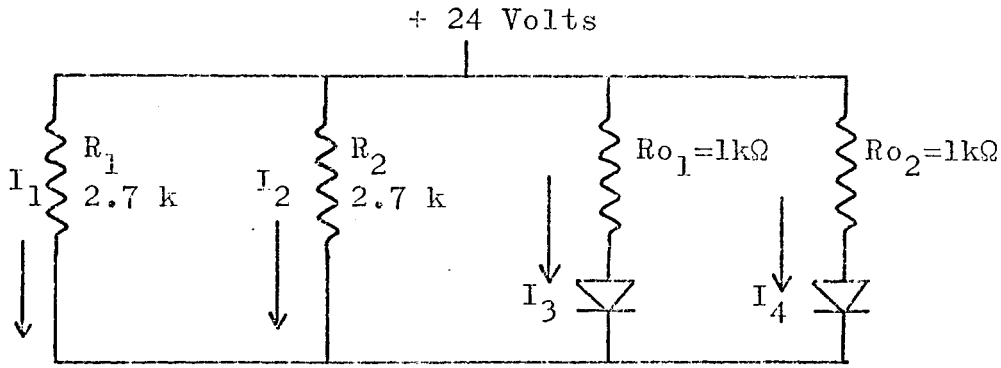
The analysis of the 300 milliwatt stress test setup will further verify that by minor adjustment in load resistor values and voltages applied to pin 6 this technique can be utilized for a variety of stress levels.

6.1.2 300 Milliwatt Operating Life Test

The analogy for this circuit is similar to that used for the 100 milliwatt life test circuit except that the external resistors have been decreased in value requiring the PNP transistors to take a larger share of the current load, thereby dissipating a large percentage of the power. For this circuit equation (1) has been modified to:

$$Pd_c = 24I_t - 2Ro\ I_3^2 \qquad (3)$$

Unlike the 100 milliwatt case where the resistances R_1, R_2, Ro_1, Ro_2 were equal to 2.7 k ohms, the simple DC analysis of power loss in the external load resistances requires a slightly different analysis. First, considering the load bridge to be:



and that

$$I_1 + I_2 + I_3 + I_4 + 2I_{B_{Q_1}} = I_T$$

ignoring the base current factors for pins 9 and 8 ($2\ I_{B_{Q_1}}$) because it should be less than 2 percent of the total current and assuming

that $Ro_1 = Ro_2$ and that $R_1 = R_2$ then it follows that the voltage drop across each line is the same (called V_{c1}) then

$$I_T = \frac{V_{c1}}{R_1} + \frac{V_{c1}}{R_2} + \frac{V_{c1}}{Ro_1} - \frac{V_{BE}}{Ro_1} + \frac{V_{c1}}{Ro_2} - \frac{V_{BE}}{Ro_2}$$

$$I_T = V_{c1}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{Ro_1} + \frac{1}{Ro_2}\right) - V_{BE}\left(\frac{1}{Ro_1} + \frac{1}{Ro_2}\right)$$

and since $Ro_1 = Ro_2 = 1\ k\Omega$

$$I_T + 2\left(\frac{0.72\ V}{1\ k}\right) = I_1 + I_2 + I_3' + I_4'$$

In this equation

$$I_3' = I_3 + 0.72\ mA$$

$$I_4' = I_4 + 0.72\ mA$$

and have no physical analogy being used for aid in the mathematical

$$I_1 = \frac{V_{c1}}{2.7\ k\Omega} \quad \text{and} \quad I_3' = \frac{V_{c1}}{1\ k\Omega}$$

$$V_{c1} = 2.7\ k\Omega\ I_1 = 1\ k\Omega\ I_3'$$

$$I_1 = \frac{1}{2.7} I_3'$$

$$I_1 = I_2,\ I_3' = I_4'$$

$$I_T + 1.44\ mA = 2I_1 + 2I_3'$$

$$= \frac{2}{2.7} I_3' + 2I_3' = 2\left(1 + \frac{1}{2.7}\right) I_3$$

$$= \frac{7.4}{2.7} I_3'$$

then $$I_3' = \frac{I_T + 1.44\ mA}{7.4}\ 2.7 \qquad (4)$$

$$I_3 = \frac{2.7}{7.4}\ (I_T + 1.44\ mA) - 0.72\ mA \qquad (5)$$

Now substituting equation 5 into equation 3

$$Pd_c = 24I_T - 2Ro\ \ (I_T + 1.44 \times 10^{-3})\ \frac{2.7}{7.4}\ - 0.72 \times 10^{-3}\ ^2$$

and I_T becomes equal to

$$I_T = \frac{91.71 \times 10^{-3} - 38.78 \times 10^{-4}}{2}$$

$$= \frac{91.71 - 62.27}{2} = \frac{29.44}{2}$$

$$= 14.7\ mA \quad \text{for Rc} = 1\ k\Omega$$

$$Pd_c = 300\ mW$$

This results in:

$$V_6 = -3.33\ volts$$

$$I_1 = I_2 = 2.18$$

$$I_3 = I_4 = 5.16\ mA$$

This results in the following calculation of component dissipations:

Transistor Q_1 = 14.9 mW
Transistor Q_2 = 14.9 mW
Transistor Q_3 = 39.0 mW

Transistor Q_4 = 39.0 mW
Transistor Q_5 = 48.9 mW

Resistor R_1 = 12.6 mW
Resistor R_2 = 12.6 mW
Resistor R_3 = 116.7 mW

At this stress level, the relative percentage of power consumed by the PNP transistor chips has increased to approximately 30 percent of the total circuit power. Since this is in proportion to the relative cross-sectional areas of the two silicon die, the assumption can be made that the average junction temperatures are nearly equal, a very important factor that must be considered whenever possible as the power levels are increased.

7.0 EFFORT FOR NEXT PERIOD

The effort for the next quarter will be concentrated on initiating the life tests on all circuits and analyzing the data generated by these tests.

It is expected that analyses of the power dissipation on the other circuits will be completed.

The bulk of the reference material obtained as a result of the literature survey will be reviewed and the results reported in the next quarterly report.