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# HIGH RELIABILITY SCREENING OF SEMICONDUCTOR AND INTEGRATED CIRCUIT DEVICES

*by J. Lombardi, L. McDonough, and H. Padden*

*Prepared by*
GRUMMAN AIRCRAFT ENGINEERING CORPORATION
Bethpage, N. Y.
*for Goddard Space Flight Center*

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# HIGH RELIABILITY SCREENING OF SEMICONDUCTOR AND INTEGRATED CIRCUIT DEVICES

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All questions and/or comments related to the work reported herein should be directed to either:

John Lombardi
Project Engineer
Grumman Aircraft Engineering Corp.
Plant 3, Dept. 852
Bethpage, New York 11714

or: Technical Director
Code 470
NASA/Goddard Space Flight Center
Greenbelt, Maryland 20771

## FOREWORD

The Program objectives were to investigate methods and techniques for high-reliability screening of semiconductor and integrated circuit devices. The basis of this study was to pinpoint the origin of potential failure mechanisms. Information thus gained was then used to determine the most effective techniques to screen those devices susceptible to failure. In the course of this program, Grumman has developed an integrated screening-acceptance test specification for semiconductor and integrated circuit devices to insure high-reliability requirements for NASA programs.

This report contains the results of a 10-month research program performed under NASA Contract NAS 5-9639 for Goddard Space Flight Center.

The report is organized into two distinct parts to separate the general specification from the rest of the text. The first part contains the general specification for digital integrated circuits which can be reproduced as is, while the second part contains a description of the development of the specification and the results of all tests performed during this program.

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## PART 1

## TEST SPECIFICATION

The complete Digital Integrated Circuit General Specification developed during this program is presented in Part 1. This specification contains the general provisions for the maintenance of an effective Quality Control and Reliability System, and defines the sub-contractor's and component manufacturer's responsibility for assuring compliance of materials, supplies and services with all the applicable requirements of the detailed screening-acceptance provisions.

It is recommended that this specification be implemented by NASA as an instrument in the procurement and acceptance of high-reliability digital integrated circuits for space system applications.

# GENERAL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS

## 1. SCOPE

This specification covers general requirements for all silicon monolithic digital integrated circuits used in NASA High Reliability Electronic Systems. Specific requirements for a particular type are contained in its detail specification.

This Document establishes requirements for an Integrated Circuits Quality Control and Reliability System, and defines the sub-contractor's and component manufacturer's responsibility for assuring compliance of materials, supplies, or services with applicable requirements. It is required that component manufacturers maintain an adequate, effective, and economical Quality Control and Reliability System for the implementation of this specification.

## 2. APPLICABLE DOCUMENTS

The following specifications, of issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein.

| | | |
|---|---|---|
| a. | MIL-S-19500 | Semiconductor Devices, General Specification For |
| b. | MIL-STD-750A | Test Methods for Semiconductor Devices |
| c. | NASA NPC-200-3 | Inspection System Provisions for Suppliers of Space Materials, Parts, Components and Services. |
| d. | MIL-R-38100 | Reliability and Quality Assurance Requirements for Established Reliability Parts, General Specification For. |
| e. | MIL-G-45204 | Gold Plating (Electro-deposited) |

## 3. PRECEDENCE OF DOCUMENTS

### 3.1 General

For purposes of interpretation in case of any conflicts, the following order of precedence shall apply:

3.1.1 Contract - The contract shall have precedence over any specification.

3.1.2 Detailed Specification - The detailed specifications shall have precedence over this general specification and other referenced specifications.

3.1.3 This Specification - This specification shall have precedence over all referenced specifications.

## 4. GENERAL PROVISIONS

### 4.1 Specification Requirements

Unless otherwise specified in the contract or purchase order, the sub-contractor shall be responsible for accomplishing the examinations and tests required by this Specification and the applicable detail specifications.

If the sub-contractor's or component manufacturer's facility is not adequate to perform the required tests, the services of an independent laboratory approved by NASA shall be engaged.

NASA also reserves the right to perform any of the inspections set forth in this specification, the detail specification, and the associated specification sheets, where such inspections are deemed necessary to assure that parts and services conform to prescribed requirements.

### 4.2 Quality Control and Reliability Assurance Provisions

The manufacturer shall establish and maintain a Quality Control and Reliability System designed to assure that all the requirements of this specification and the detail specifications are implemented and controlled.

### 4.3 Description of Production Processes and Controls

The manufacturer shall prepare, submit, and maintain a detailed description of the production processes, steps, and controls applied to parts currently produced and proposed for inclusion in this program. Requirements and tolerances shall be specified for all critical environments and utilities which come in contact with the production and test of established reliability parts. Process or geometry changes which affect the functional, electrical, mechanical, or environmental capabilities shall not be allowed until requalification and written consent is obtained from a NASA authorized representative. The addition of a vendor's type number to the source of supply list shall be based on the process and geometry submitted for approval. Changes in the process or geometry without written consent shall result in automatic loss of approval as a source of supply.

### 4.4 Procurement, Production, and Control Documentation

Prior to qualification, the manufacturer shall identify by name, number, release date, and latest revision date, all documents used in the procurement and processing of materials, production of parts, and methods of product assurance. This documentation must include purchase, process, and test specifications, as well as internal procedures and controls for the application of such documents.

### 4.5 Flow Charts

All documents and their interrelationships shall be identified in flow chart form.

4.5.1 Production Processes - The manufacturer shall identify the interrelationship of all documents on flow charts which include operations, processes, and environments related to materials and fabrication of parts.

4.5.2 Product Assurance - The manufacturer shall identify all product assurance documents, including specifications, in flow chart form. These shall be individually related to operator instructions, and to materials and process specifications covering parts being produced. Documents shall be identified in sequence on the production flow diagram.

4.5.3 Documentation Responsibility - These flow charts shall indicate the organizational group responsible for performing each function. There shall be a specific product assurance control indicated for each requirement in all documents relating to production processes, test, and specifications.

4.6 Handling, Packaging, and Shipping Procedures

Documentation of handling techniques, throughout the complete manufacturing and test sequence of operations, shall be provided. Handling and packaging requirements shall be prepared to cover storage in a controlled storage area, removal of parts, and preparation for shipment.

4.7 Surveillance

A designated agent of NASA may be assigned to the manufacturer's plant to perform surveillance functions in connection with products furnished under this specification. This representative shall have the prerogative to observe any inspections and the data resulting from any tests performed as a requirement of this specification.

The manufacturer will be required to provide these personnel with reasonable facilities and equipment required to conduct their business within the manufacturer's plant.

4.7.1 Initial Survey - Prior to the award of a contract, a facility survey may be conducted to ensure an overall capability for circuits to be procured. Upon completion of the initial survey, the subcontractor will be notified in writing of those areas of non-conformance. A reasonable period of time will be allowed for the supplier to make corrections.

4.7.2 Periodic Surveys - The subcontractor shall make his facilities available for periodic surveys which will be made by NASA during the execution of the contract to determine compliance with requirements of the contract and this document.

4.7.3 Source Inspection - NASA reserves the right to conduct inspection at subcontractor's plants. Such inspection can include performance or witnessing of or participation in, such examinations and tests as are considered necessary to determine compliance with relevant specifications during the process of manufacture, assembly, inspection, test, packaging, and shipment of material to be furnished to NASA.

4.7.4 Availability and Review of Documentation - All detail documents. such as specifications, test procedures, processes, and product assurance controls shall be available for review and acceptance by NASA.

4.8 Failure - Analysis Program

The manufacturer shall establish and maintain a failure-analysis program. Failed parts from all sources, such as production lines, testing, and use, shall be analyzed to determine the cause of failure. The failure analysis conducted shall be designed to yield adequate conclusions to initiate a plan for corrective action to eliminate the cause and prevent reoccurrence of the type failure-mode reported.

4.8.1 Failure Reporting - The manufacturer shall establish and document a failure-reporting system which will provide adequate data on all failures. All failure verification and analysis shall be performed under the direction of, or with the cognizance of, a Central Failure Analysis Group. All failures reported shall be verified by the manufacturer's responsible production, quality assurance, or engineering personnel. The report shall list the cause of failure and any corrective action taken or planned. A description of the failure analysis procedures used should be included. Copies of the Failure Analysis Report shall be submitted within 2 weeks of the date that the defect occurred to the NASA Technical Representative. The report shall include, as a minimum, the following information:

a. Date Defect Occurred

b. Lot Identification, Date Code, and Size of Lot

c. Device Type and Serial Number(s) of Failed Circuit(s)

d. Test and/or Inspection at Which Defect was First Noted

e. Failure-Mode Category

f. Actual Mode of Failure

g. Cause of Failure

h. Corrective Action Taken or to be Taken

i. Effect on Other Devices in the Lot

j. Purchase Orders or Contracts Affected.

4.9 Corrective Action

The manufacturer shall establish a plan-of-action for recommendation of corrective action on all defects and failures. Corrective action recommendations shall be supported by verifying data, or a proposed evaluation test plan. The manufacturer shall submit a report of each failure and proposed corrective action to NASA. If the recommended corrective action consists only of improvements in the control procedures and implementation, this may be instituted immediately and a copy of the revised procedure and failure report submitted for record. Other corrective action which affects the functional electrical, mechanical, or environmental capabilities shall not be implemented for production until improved prototype parts have been produced, evaluated, and approved by NASA.

4.10 Workmanship Requirements

It is the responsibility of the component manufacturer to adequately inspect each lot to insure that it contains only circuits which are of the workmanship quality required by this specification. The manufacturer shall develop, in conjunction with NASA, techniques for workmanship inspection where adequate techniques have not been available.

4.11 System Performance

Integrated circuits used in any system will not be considered acceptable if they fail because of poor process controls by the manufacturer at an average rate, after the first 3 months of system operation, in excess of 1 per 5,000,000 device hours. All detailed failure analysis reports of system failures will be delivered within 1 month of their date of issuance to NASA. Component manufacturers whose integrated circuits system performance does not meet the above requirement will be removed from the list of approved vendors until they certify evidence satisfactory to NASA of regaining their process control.

## 5. DETAIL SPECIFICATION PROVISIONS

The manufacturer shall be responsible for generating a detail specification which contains all of the following information. These requirements shall be subject to approval by NASA, and any deviations or exceptions shall be subject to review and re-negotiation. The integrated circuits shall be of the design, construction, and physical dimensions specified.

5.1 Heading

This section should include:

a. Type number of microcircuit. (ex. 6N XXXX)

b. Circuit function (ex. "J-K Flip Flop")

c. Type of logic (ex. DCTL or DTL)

d. Name of manufacturer (with address and phone number)

5.2 Description & Construction Features

This section should include:

a. Substrate material used.

b. Description of process (planar, diffused, epitaxial, buried layer, oxide isolated, etc.)

c. Circuit application (airborne, space, military, shipboard, ground, etc.)

d. List of transistor elements in circuit. State similarity to discrete equivalents.

e. List of diode elements in circuit with similar discrete types.

f. List of resistor elements in circuit stating process type, nominal values, and tolerances.

g. List of capacitor elements in circuit stating process type, nominal values, and tolerances.

h. Process for mounting of die to header.

i. Material used for bonding wires with thickness and bond type.

j. Maximum bond wire lead length of each lead.

k. Material used for internal filmed connections.

l. Size of substrate including thickness.

m. Internal atmosphere in micro package.

n. Process used to seal package top to package.

o. Materials used for external leads from package.

p. Package materials or standard package type.

q. Weight of microcircuit.

5.3 Case Dimension or Microcircuit Package Outline

A drawing should be included which is similar to those given on transistor specification sheets and gives the following:

a. Maximum package dimensions.

b. Lead orientation (numbered).

c. Lead spacing, width, and thickness with tolerances.

d. Flanges with tolerances, if applicable.

e. Any special notes concerning mechanical assembly of the microcircuit.

5.4 Microcircuit Internal Surface Topology

This section should show a photograph or drawing of the surface topological features of the microcircuit. Significant element areas should be identified.

5.5 Process Identification Flow Chart

This section should include a flow chart showing every step of production and test, the process title, the number and latest dated revision of the supplier's defining specification for each step, and the departmental responsibility for implementing each step of the process.

5.6 Schematic

A complete schematic should be included showing pin numbers and component nominal values and tolerances.

5.7 Absolute Maximum Ratings

This section should include the following information:

a. Maximum voltage from package lead to ground.

b. Maximum voltage between package leads (including polarity).

c. Minimum $V_{cc}$ breakover voltage (worst case for full operating temperature range).

d. Maximum and minimum operating temperature (ambient)

e. Maximum and minimum storage temperature.

f. Maximum allowable package lead temperature; minimum and maximum heating time for making connection of one external package lead; 1/2 total package leads; all package leads.

g. Maximum permissible package lead current.

h. Minimum acceptable hermeticity of package.

i. Maximum ICBO or ICEO of circuit at maximum operating temperature (if measurable).

j. Maximum power dissipation (at room temperature and at maximum operating temperature).

k. Maximum Fan-in/Fan-Out at $+25^{\circ}C$, maximum operating temperature, and minimum operating temperature.

5.8 Reliability Data

Existing data should be summarized giving reliability test information run specifically on the type microcircuit. The summary should include:

a. Total unit-test hours and the failures during this period.

b. Test conditions & assumed acceleration factors if any.

c. MTBF with % confidence (real, not extrapolated).

d. Total field system unit test hours.

e. Field data and MTBF including:

   1) System Designation

   2) Quantity of microcircuit used/system

   3) Government Agency

   4) Non Standard Part Designation

   5) Contract number and date

f. Percentage of this microcircuit production lot diverted from the production line for life testing and for destructive quality testing.

g. The number of working (good) microcircuits of this type already delivered to system users.

## SCREENING ACCEPTANCE PROVISIONS

Prior to qualification, the manufacturer shall submit complete screening procedures for NASA acceptance. These shall provide for a complete test report, including the conditioning methods utilized and the results of all screening tests.

It is recommended that the tests and their order of performance be consistent with Table 6-1. If no exception is taken by the manufacturer, all the tests listed in Table 6-1 shall be performed in their indicated order.

### 6.1 Internal Visual Inspection Before Sealing

To insure that the workmanship requirements of this specification and the detail specifications are carried out, internal visual inspection of all integrated circuits shall be performed in a dry-box prior to case sealing at the manufacturer's facility. The equipment required to perform this inspection is any magnifying apparatus of 50X power (or greater) with a collimated light source which provides circuit orientation and handling facility for visual ease in inspecting for these requirements. During this inspection, all of the following shall be evaluated. Devices which fail to meet any of the requirements listed below shall be immediately rejected and eliminated from subsequent testing. These examinations may be conducted in any order but all must be included.

6.1.1 Process Uniformity - A topological representation shall be provided for inspection, and all devices shall conform tc this topology. All devices of the same part number in each lot must be identical in appearance. There shall be no inconsistences in topology orientation, bond patterns and placement, etc., which causes a heterogeneous appearance.

6.1.2 Cleanliness - The active device shall be free from any chemical residues (including lacquer, varnish, or jelly) or discoloration resulting from device production and handling. Both the device and package shall also be free of any foreign particles greater than 0.5 mil (0.0005 inch) across the widest dimension. This includes extraneous encapsulated material, weld splatters, excessive build-up or flaking of gold preform , etc.

6.1.3 Bonds -

6.1.3.1 Metallized bonding pads shall be provided for each terminal where a bond is to be made on the substrate.

6.1.3.2 Any bond contact area made on the metallized interconnection shall cause the device to be rejected.

6.1.3.3 The entire bond, as defined by the bonding tool impression, shall be within the periphery of the bonding pad and there shall be at least 2 mils (0.002 inch) of interconnection material around the periphery of the bonding tool impression.

6.1.3.4 There shall be no evidence of loose, misplaced or open bonds, or bonds that have been partially stripped from the pad. There shall be no evidence of multiple attempts to perform a successful bond on any single bonding pad or lead. Any device exhibiting such rebonding/removal shall be rejected.

TABLE 6-1

SCREENING ACCEPTANCE TEST REQUIREMENTS

| TESTS | REF PARAGRAPH | LTPD | MAX. ACC.NO. | CONDITIONS (%) |
|---|---|---|---|---|
| 1. Internal Visual Inspection Before Sealing | 6.1 | -- | -- | 100 |
| 2. Marking Requirements | 6.2 | -- | -- | 100 |
| 3. External Visual and Mechanical Inspection | 6.3 | -- | -- | 100 |
| 4. Marking Permanency Test | 6.4 | 10 | 1 | |
| 5. Stabilization Bake | 6.5 | -- | -- | 100 |
| 6. Electrical Tests | 6.6 | -- | -- | 100 |
| a. D-C Parameter Tests | 6.6.1 | -- | -- | |
| b. Noise Immunity Tests | 6.6.2 | -- | -- | |
| c. Dynamic Parameter Tests | 6.6.3 | -- | -- | |
| d. Power Dissipation Tests | 6.6.4 | -- | -- | |
| e. Threshold Test | 6.6.5 | -- | -- | |
| f. Input Capacitance Test | 6.6.6 | -- | -- | |
| g. Insulation Resistance Test | 6.6.7 | -- | -- | |
| 7. Thermal Cycling (Shock) | 6.7 | -- | -- | 100 |
| 8. Centrifuge | 6.8 | -- | -- | 100 |
| 9. Variable Frequency Monitored Vibration | 6.9 | -- | -- | 100 |
| 10. X-Ray | 6.10 | -- | -- | 100 |
| 11. Burn-In (with variables data) | 6.11 | -- | -- | 100 |
| 12. Hermeticity Tests | 6.12 | -- | -- | 100 |
| 13. Final Electrical | 6.13 | -- | -- | 100 |
| 14. Lot Provisions | 6.14 | -- | -- | 100 |

6.1.4 Internal Bonding Wires - Internal bonding wires shall be inspected using the following reject criteria:

a. Internal wires exhibiting sufficient length (slack) such that there exists the possibility of shorting to another lead, die edge or surface, or to the package sides, bottom, or top.

b. Any wire exhibiting nicks, cuts, crimps, or scoring which cut into or deform the wire by more than 25% of the original diameter.

c. When viewed from above, leads which cross one another or which cross any metallization not electrically connected to the lead.

d. Lead material greater in length than 2 mils (0.002 inches) that is fixed on one end (pigtails). Lead wire shall not extend more than 2 mils (0.002 inches) beyond the normal termination.

e. Any extra wires present other than the ones connecting specified areas on the chip to the external leads. There shall be only one wire connected to a specified area of the chip or to an external lead except where the design of the integrated circuit calls for the use of additional wires, and has been previously approved by NASA.

f. Any internal bonding wire which is missing from its intended location.

g. Inadequate clearance. No wire shall be within 3 mils (0.003 inches) of another wire, ball bond, or the case.

6.1.5 Active Device Area

6.1.5.1 Substrate Defects - Substrates which exhibit cracking, fracture, pitting, chipping or other signs of physical damage in the active circuit, metallization, or bond areas greater than 1 mil (.001 inch) shall be considered a reject.

6.1.5.2 Diffusion Masking - Devices with diffusion irregularities and masking defects shall be rejected if any active junction is closer than 0.1 mil (0.0001 inch) to another active junction, or closer than 1.2 mils (0.0012 inch) to an isolation junction.

6.1.5.3 Metallic Interconnection - The metallic interconnections shall be deposited in accordance with the layout design. No two interconnections shall be closer than 0.5 mil (0.0005 inch) or 50% of the distance detailed in the layout design, whichever is smaller.

6.1.5.4 Metallization Voids - Voids in the metallization shall not result in the width of any lead, pad, or fillet being reduced to less than 50% of design width.

6.1.5.5 Tool Marks and Scratches - The following defects shall be considered a cause of rejection:

a. Scratches or tool marks which reduce the width of any metallization to less than 50% of design width, or which expose silicon dioxide along the scratch.

b. Any smear of metallization extending contiguously more than one lead width from the design lead path, or which reduces the spacing between adjacent leads to less than 50% of the design lead spacing.

6.1.5.6 Metallization Defects (Other) - Any one of the following metallization defects shall also be considered a cause of rejection:

a. Excessive peeling or bubbles

b. Corrosion (chemical reaction)

c. Metallization with less than two-thirds coverage of electrically active contact areas.

6.1.5.7 Oxide Damage - Oxide voids exposing an electrically active junction area or exposing a silicon surface to an electrically active lead which is not, by design, already in contact with the same surface shall be cause for rejection.

6.1.5.8 Periphery - The periphery of the circuit dice shall be well defined and encompass the entire active circuit. No active area of the circuit; bonds, bonding pads, or junctions (including under or side diffusion) shall be closer than 0.1 mil (0.0001 inch) to the dice periphery.

6.1.6 Package and Leads - Any one of the following physical defects to the package and leads shall be cause for rejection:

a. Physical damage to case and leads.

b. Cracks or voids in the glass-to-metal or ceramic-to-metal seal, greater than one lead thickness.

c. Bar (chip) tilted or loose in the header.

d. External terminals (leads) shorted to the case.

e. Contamination or conducting particles on external leads.

f. Other mechanical faults.

6.2 Marking Requirements

6.2.1 Marking - Marking shall be performed prior to testing to avoid mistakes in orientation. All markings shall be of a permanent type which is resistant to removal by handling and which is insoluble in trichlorethylene, water, or xylene.

6.2.2 Manufacturer's Designation - Each integrated circuit shall be marked with the manufacturer's identification. This identification shall consist of the manufacturer's name, initials, trademark, or EIA assigned code number.

6.2.3 Type Number - Each integrated circuit shall be marked with the manufacturer's type number as listed in the detail specification.

6.2.4 Serial Number - Each integrated circuit shall be marked with a unique serial number for each device.

6.2.5 Production Lot Number - Each integrated circuit case shall be marked with a production lot number. This number shall be assigned by the manufacturer such that duplication of production lot numbers cannot occur within any calendar year for any two production lots used in the systems delivered to NASA. This number shall consist of letters, numbers, or a combination thereof.

6.2.6 Acceptance Date - When specified, each integrated circuit shall be marked with a code indicating the date of acceptance. This date will be the day that the final acceptance test is performed by the manufacturer (within 10 days). A code adapted for this purpose will indicate the year and week that the unit was manufactured.

6.2.7 Date of Manufacture - Each integrated circuit shall be marked with a code indicating the date of manufacture. This will be representative of the date that the circuit was sealed into its package or encapsulant (within 10 days).

6.3 External Visual and Mechanical Inspection

The purpose of this examination is to verify that materials, design, construction, marking, and workmanship are in accordance with the applicable requirements.

The equipment required to implement the Visual Inspection consists of an optical microscope furnishing 20 power (or greater) with circuit orientation and handling facilities for ease in checking the following requirements.

6.3.1 Procedure - Each Integrated Circuit is to be inspected under 20-power magnification for the following.

6.3.1.1 Drawing Conformance - Each device must meet the general requirements for outline and dimensions as given in its detail specification.

6.3.1.2 Marking - Each integrated circuit shall be marked with the manufacturer's identification, part number, serial number, production lot number, date of manufacture, and the acceptance date (when specified). In addition, lead orientation shall also be indicated. All circuit symbolization and markings must be legible for identification. All markings shall be of a permanent type which is resistant to removal by handling.

6.3.1.3 Finish - There shall be no peeling, blistering, holes, or other imperfections of the gold plating on the leads which permit bare Kovar to show. The case finish shall have no flaking, spattering, chipping, or holes.

6.3.1.4 Contamination - There shall be no contamination (foreign substance) either on the device or in/on the protective carrier for the device. (Note: Contamination is defined as either solid, liquid, powder, or film which could cause soldering or welding difficulties.)

6.3.1.5 Homogeneity - All devices in each lot type should look exactly alike. There should be no inconsistency of symbolization placement, etc., which causes a heterogeneous appearance.

6.3.1.6 Seals - The glass-to-metal seal or ceramic-to-metal seal shall not contain cracks or voids which are greater than one lead thickness.

6.3.1.7 Leads - The leads shall be gold-plated, iron-nickel-cobalt (Kovar) alloy material in the bright annealed and soft condition. The leads shall be uniform in size, quantity, and condition; clear of oil and grease films, and free from chips, cracks or kinks. In addition, there shall be no broken, grooved, weak, or laterally bent leads. (Note: A grooved lead is one where a blemish occurs on one or more leads and causes a decrease or an offset in lead thickness. A weak lead is one where any defect could cause inferior strength of the lead. This includes excessive necking, nicks, cuts, etc.)

6.4 Marking Permanency Test

The purpose of this test is to verify that all markings are permanent and resistant to removal by handling. The required test samples shall consist of individually identifiable integrated circuits randomly selected from an inspection lot.

6.4.1 Procedure - Each Integrated Circuit shall be tested as follows:

a. Each device shall be immersed in trichlorethylene for a mininum of 3 minutes. After immersion, the markings on each device shall be scrubbed with a camel's hair brush (or similar soft-bristled brush) back-and-forth for a total of 10 cycles. The brush shall be immersed in trichlorethylene as needed to maintain wetness. Care must be taken to brush the markings only to avoid damaging the leads.

b. Using xylene instead of trichlorethylene, repeat the test procedure.

6.5 Stabilization Bake

Each circuit shall be stored at a minimum temperature of +150°C for a minimum time of 50 hours. The circuits shall be allowed to stabilize for at least 16 hours at +25°C before proceeding with the electrical measurements.

6.6 Electrical Testing

The following tests shall form the basis of the Electrical Test portion of the detail specification. Test conditions and limits shall be chosen to insure operation over the full range of temperature (-55 to +125°C), loading and power supply variations:

6.6.1 D-C Parameter Tests - These are comprised of input current characteristics and output voltage "high" and "low" levels, including worst-case combinations of $V_{CC}$, fan-out, fan-in, and temperature. Test conditions and limits contained in the detail specification shall be consistent with the format shown in Table 6-2.

6.6.1.1 Input Characteristics - With a voltage applied to each input separately, as specified in the detail specification, the input current shall not exceed the maximum permissible specified value.

6.6.1.2 Output Voltage Levels - With each input held at the minimum acceptable "1" level, and the nominal value of $V_{CC}$ applied, the output voltage level shall not exceed the specified maximum "0" voltage limit.

6.6.2 Noise Immunity Tests - These are comprised of tests for:

a. Worst-case D-C noise margins at both the "high" and "low" levels.

b. Worst case immunity to noise pulses which are A-C coupled into the ground and signal lines.

6.6.2.1 D-C Noise Margin - Ground and Signal - The noise margin for the worst case combination of $V_{CC}$, loading, and temperature must meet the limit specified in the detail specification. The following definitions of noise margins are preferred for these tests. If there are deviations from these definitions, the definition used should be stated. Test conditions and limits contained in the detail specifications must be consistent with the established definitions and with the format shown in Table 6-3.

TABLE 6-2

D-C ELECTRICAL PARAMETER TESTS

| TESTS | CONDITIONS | LIMITS | |
|---|---|---|---|
| | | Min. | Max. |
| D-C Logic Levels | | | |
| Low $V_{out}$ at +25°C | (Note 1) | (Note 2) | |
| Low $V_{out}$ at +125°C | | | |
| Low $V_{out}$ at -55°C | | | |
| High $V_{out}$ at +25°C | | | |
| High $V_{out}$ at +125°C | | | |
| High $V_{out}$ at -55°C | | | |
| $V_{in}$ (on) at +25°C | | | |
| $V_{in}$ (on) at +125°C | | | |
| $V_{in}$ (on) at -55°C | | | |
| $V_{in}$ (off) at +25°C | | | |
| $V_{in}$ (off) at +125°C | | | |
| $V_{in}$ (off) at -55°C | | | |
| Input Currents | | | |
| $I_{in}$ (on) at +25°C | | | |
| $I_{in}$ (on) at +125°C | | | |
| $I_{in}$ (on) at -55°C | | | |
| $I_{in}$ (off) at +25°C | | | |
| $I_{in}$ (off) at +125°C | | | |
| $I_{in}$ (off) at -55°C | | | |

NOTE 1: Specify worst case load conditions for each test.

2: Must provide limits which are applicable to any input terminal, unless otherwise specified. Where an expander input terminal is available, this shall be defined by a separate set of limits.

TABLE 6-3

D-C NOISE MARGIN TESTS

| TESTS | CONDITIONS | LIMITS | |
|---|---|---|---|
| | | Min. | Max. |
| High Noise Margin (HNM) +25°C | (Note 1) | (Note 2) | |
| HNM at -55°C | | | |
| HNM at +125°C | | | |
| Low Noise Margin (LNM) +25°C | | | |
| LNM at -55°C | | | |
| LNM at +125°C | | | |

NOTE 1: Specify worst case load conditions for each test.

2: Must provide limits which are applicable to any input terminal, unless otherwise specified. Where an expander input terminal is available, this shall be defined by a separate set of limits.

a. High Noise Margin (HNM) - The change of input voltage for an inverter over the "0" input value which forces the output voltage into the transition region.

b. Low Noise Margin (LNM) - The change of input voltage for an inverter under the "1" input value which forces the output voltage into the transition region.

c. For Gates

D-C High Noise Margin = $V_{out}$ High (Voh) - $V_{in}$ High (Vih)

D-C Low Noise Margin = $V_{in}$ Low (Vil) - $V_{out}$ Low (Vol)

d. For Inverter Gate

$V_{in}$ High is measured when $V_o$ is 10% (Voh-Vol)

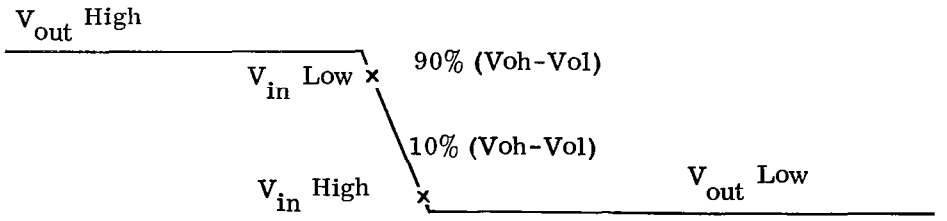
$V_{in}$ Low is measured when $V_o$ is 90% (Voh-Vol)

e. For Non-Inverter Gate

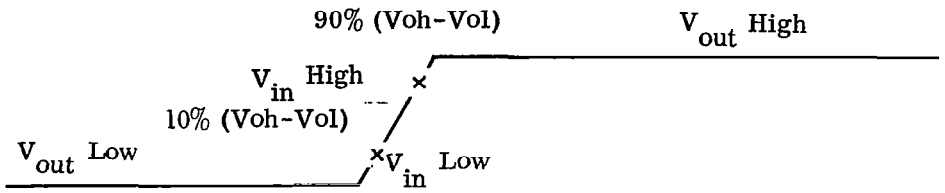
$V_{in}$ High is measured when $V_o$ is 90% (Voh-Vol)

$V_{in}$ Low is measured when $V_o$ is 10% (Voh-Vol)

f. Inverter Curve



g. Non-Inverter Curve




6.6.2.2 Pulsed Noise - A suitable noise pulse, as defined in the detail specification, will be A-C coupled to the integrated circuit ground terminal with the worst case specified D-C supply voltage, input voltage, and load connected to the circuit. The output voltage shall not enter the transition region in both high and low level cases.

6.6.3 Dynamic Parameter Tests - These are comprised of test for:

a. Switching characteristics including delay time ($t_d$), rise time ($t_r$), storage time ($t_s$), and fall time ($t_f$) as defined in MIL-S-19500D, at worst-case temperature, loading, $V_{CC}$, and line load capacity.

b. Propagation delay time, through a single circuit, from the 50% point of the input switching signal to the 50% point of the logic circuit output switching voltage, at worst-case conditions.

Test conditions and limits contained in the detail specification shall be consistent with the format shown in Table 6-4.

6.6.3.1 Switching Characteristics - The integrated circuit will have delay time, rise times, storage time, and fall time within the limits indicated in the detail specification. Where applicable to the actual system performance, worst case combinations of $V_{CC}$, loading, temperature, and line load capacity shall be used for these tests.

6.6.3.2 Propagation Delay Time - The integrated circuits will have a propagation delay time within the limits shown in the detail specification. The test will be performed through a single logic circuit with the measurements made from the 50% voltage point of the input switching signal to the 50% point of the logic circuit output switching voltage. The input pulse to the integrated circuits under test will have rise and fall times and waveshapes comparable to the average test circuit values indicated in the detail specification. Worst case values of $V_{CC}$, temperature, loading, and system line capacity will be used for this test as applicable to the actual system performance.

6.6.4 Power Dissipation Tests - Total power dissipation is defined as the summation of V-I products at all terminals at maximum specified fan-out (equivalent load); and using the power supply voltage, duty cycle, and temperature (within the specified range) which causes the maximum drain on the power supply.

Test conditions and limits contained in the detail specification shall be consistent with the format shown in Table 6-5.

TABLE 6-4

DYNAMIC PARAMETER TESTS

| TESTS | CONDITIONS | LIMITS | |
|---|---|---|---|
| | | Min. | Max. |
| Switching Characteristics | | | |
| Delay Time | (Note 1) | (Note 2) | |
| $t_d$ +25°C | | | |
| $t_d$ +125°C | | | |
| $t_d$ -55°C | | | |
| Rise Time | | | |
| $t_r$ +25°C | | | |
| $t_r$ +125°C | | | |
| $t_r$ -55°C | | | |
| Storage Time | | | |
| $t_s$ +25°C | | | |
| $t_s$ +125°C | | | |
| $t_s$ -55°C | | | |
| Fall Time | | | |
| $t_f$ +25°C | | | |
| $t_f$ +125°C | | | |
| $t_f$ -55°C | | | |
| Propagation Delay Time | | | |
| Propagation Delay | | | |
| $t_{pd}$ +25°C | | | |
| $t_{pd}$ +125°C | | | |
| $t_{pd}$ -55°C | | | |

NOTE 1: Specify worst case load conditions for each test. Show all significant test configurations used to obtain dynamic parameter values.

2: Must provide limits which are applicable to any input terminal, unless otherwise specified. Where an expander input terminal is available, this shall be defined by a separate set of limits.

TABLE 6-5

POWER DISSIPATION TESTS

| TESTS | CONDITIONS | LIMITS | |
|---|---|---|---|
| | | Min. | Max. |
| Power Dissipation (Pd) | (Note 1) | (Note 2) | |
| Pd at +25°C ckt. ON | | | |
| ckt. OFF | | | |
| Pd at -55°C ckt. ON | | | |
| ckt. OFF | | | |
| Pd at +125°C ckt. ON | | | |
| ckt. OFF | | | |

NOTE 1: Specify worst case load conditions for each test. A full statement of input, power supply, and loading factors is required to make parameter limits meaningful.

2: Must provide limits which are applicable to any input terminal, unless otherwise specified. Where an expander input terminal is available, this shall be defined by a separate set of limits.

6.6.5 Threshold Tests - These consist of breakdown voltage tests measured from output to ground with each input held at maximum "0" voltage, and from supply to ground. Test conditions and limits called out the detail specification must be chosen to insure that the maximum specified $V_{CC}$ shall be a minimum of twice the nominal operating $V_{CC}$ of the system.

6.6.5.1 Breakdown - Output to Ground - With each input held at specified maximum "0" voltage and $V_{CC}$ maximum applied, each output voltage shall exceed the minimum acceptable "1" voltage level.

6.6.5.2 Breakdown - Supply to Ground - The current drawn from $V_{CC}$ to ground terminals with maximum specified $V_{CC}$ applied shall be less than the value specified on the detail specification insuring that no circuit components are in the breakdown of their characteristics with the circuit either ON or OFF.

6.6.6 Input Capacitance - Input capacitance shall be measured at 1.0 mc using the bridge method. Prior to measurement, the capacitance bridge shall be nulled with the test circuitry connected to eliminate errors due to the stray capacitance of the test circuit. The integrated circuit shall then be inserted into the test circuit and capacitance shall be measured. All D-C conditions and A-C signal levels shall be indicated in the detail specification.

6.6.7 Insulation Resistance Test - Leakage current tests as indicated in the detail specification shall be performed to insure complete electrical isolation of the terminals and substrate from the circuit package.

6.7 Thermal Cycling (Shock)

The following thermal environmental tests are required to reveal mismatches in thermal expansion coefficients of materials, cracks in the substrate, or a high moisture content. The integrated circuits shall meet the limits shown in the detail specification after being subjected to the following tests. All integrated circuits delivered to this specification shall exhibit working performance over a -55 to +125°C temperature range.

a. Subject the devices to six cycles of temperature shock, between -65°C ±5°C and +150°C ±5°C, with 55 seconds at each temperature extreme and a 5 second transfer time at +25°C between extremes.

b. This test must be performed in either temperature chambers or liquid baths capable of maintaining the required temperature tolerances during this test.

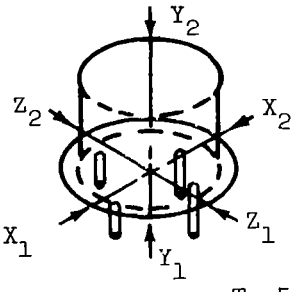
c. The integrated circuits shall be allowed to stabilize at +25°C ±3°C for a maximum of 2 hours before proceeding with any electrical measurements or follow-up stress testing.

6.8 Centrifuge (Acceleration)

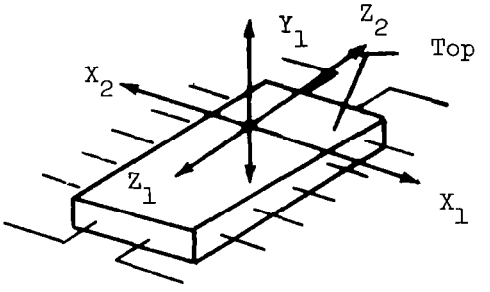
This test is designed to determine the effects of severe mechanical stresses on devices. Such stresses can cause loosening of bonds, cracked substrates, separation of substrate from package, shorting of bonding wires, and the movement of foreign particles within the packages. The integrated circuit shall show no visual mechanical damage and shall meet the limits specified in the detail specification after being subjected to the following tests.

a. Rigidly restrain the integrated circuits and their leads and subject them to a centrifugal acceleration of 20,000G for a period of 1 minute in each of two orientations ($Y_1$, $Y_2$,) as shown below.

Increase acceleration gradually to 20,000G in not less than 20 seconds and decrease gradually to zero acceleration in not less than 20 seconds. Acceleration at 20,000G for 1 minute in each orientation shall be in addition to the speedup and slow down time.



To-5 Package



Flat Package

b. Perform an inter-pin continuity check for shorts or opens following each of the $Y_1$ and $Y_2$ accelerations.

c. Complete the electrical tests indicated in the detail specification within 24 hours of the time that the integrated circuits are removed from the test circuit.

6.9 Variable Frequency Monitored Vibration

The purpose of this test is to monitor the amount of electrical noise produced by the device under vibration. The integrated circuit shall show no visual mechanical damage and shall meet the limits specified in the detail specification after being subjected to the following tests.

6.9.1 The device and leads shall be rigidly fastened to the vibration platform. The device shall be vibrated with simple harmonic motion with a constant peak acceleration of 30G minimum. The vibration frequency shall be varied logarithmically between 10 and 2000 cps. The entire frequency range of 10 to 2000 cps and return to 10 cps shall be traversed in not less than 4 minutes. This cycle shall be performed once in each of the orientations $X_1$, $Y_1$, and $Z_1$ (total of three times) so that the motion shall be applied for a total period of approximately 12 minutes. Output voltages shall be monitored in accordance with circuit topology and the circuit schematic diagram. Suitable detection circuits shall be provided to monitor noise of 100 mv peak-to-peak or greater. The measuring circuit will be delineated in the detail specification. A noise output of 100 mv peak-to-peak or greater shall be considered a failure.

6.9.2 Complete the electrical tests as required by the detailed specification within 24 hours of the time that the integrated circuits are removed from the test circuit.

6.10 X-Ray

This section establishes the procedure for the Radiographic Inspection of Integrated Circuits.

6.10.1 Equipment - An X-ray vidicon system which meets the following requirements or a system which provides equivalent magnification, resolution, and contrast shall be utilized:

6.10.1.1 X-Ray Source - The X-ray source shall have a focal spot smaller than 0.5 mm and shall be capable of operating at potentials up to 140 kv, with a minimum current of 4 ma.

6.10.1.2 Television System - The television system shall consist of an X-ray sensitive vidicon camera along with a 17-inch or larger television monitor.

6.10.1.3 Magnification - The image displayed on the television screen shall exhibit a nominal magnification of 30 power with respect to the object under view.

6.10.1.4 Resolution and Contrast - The X-ray vidicon system shall meet the following performance criteria:

a. Detect a 1.0 mil (0.001 inch) gold wire through a 7.0 mil (0.007 inch) thick nickel TO-5 transistor case.

b. Detect a 0.5 mil (0.0005 inch) tungsten wire of unspecified length. Recognition shall not be dependent on wire orientation or motion of the wire.

c. Resolve a 500 mesh stainless steel wire screen over the entire vidicon sensitive area.

6.10.2 Procedure - All devices shall be 100% X-rayed for conformance to workmanship standards. Unless otherwise specified in applicable procurement or engineering documents, any one of the following defects shall be cause for rejection:

a. Incorrect marking orientation.

b. Physical damage to case and leads.

c. Cracks or voids in the glass-to-metal or ceramic-to-metal seal, greater than one lead thickness.

d. Off-set covers by more than 10 mils (0.010 inch).

e. Contamination or conducting particles on external leads which could cause soldering/welding difficulties or shorts.

f. Extraneous encapsulated material exceeding 1 mil (0.001 inch) in any dimension.

g. Loose weld splatters.

h. Other miscellaneous mechanical faults.

i. Excessive build up or flaking of gold preform.

j. Voids in the die to case adhesive. Contact area voids shall not exceed one-half of the total contact area, and a single void shall not be equal to the length of a chip nor shall it traverse the entire width of the chip.

k. Bar (chip) tilted or loose in the header.

l. Substrates which exhibit cracking, fracture, pitting, chipping, or other signs of physical damage.

m. Misplaced or open bonds.

n. Double bonds (multiple attempts to bond on any single bonding pad or lead)

o. Bonds near the edge of bonding pads and leads. The entire bond, as defined by the bonding tool impression, shall be within the periphery of the bonding pad and there shall be at least 2 mils (0.002 inch) of interconnection material around the periphery of the bonding tool impression.

p. Weld particles on wires.

q. Inadequate clearance. No wire shall be within 3 mils (0.003 inch) of another wire, ball bond, or the case.

r. Internal wires exhibiting sufficient length (slack) such that there exists the possibility of shorting to another lead, the die edge or surface, or to the package sides, bottom, or top.

s. Any wire exhibiting nicks, cuts, crimps, or scoring, which cut into or deform the wire by more than 25% of the original diameter.

t. When viewed from above, leads which cross one another or which cross any metallization not electrically connected to the lead.

u. Lead material greater in length than 2 mils (0.002 inch) that is fixed on one end (pigtails). (Lead wire shall not extend more than 2 mils (0.002 inch) beyond the normal termination.)

v. Any extra wires present other than the ones connecting specified areas on the chip to the external leads. There shall be only one wire connected to a specified area of the chip or to an external lead except where the design of the integrated circuit calls for the use of additional wires.

w. Any internal bonding wire which is missing from its intended location.

x. External terminals (leads) shorted to the case.

y. Process non-uniformities. All devices of the same part number must be of a homogeneous construction.

6.11 Burn-In (with variables data)

All integrated circuits delivered to this specification shall exhibit working performance over a -55 to +125°C temperature range. The integrated circuits shall meet the limits specified in the detail specification after being subjected to the following tests:

a. Each circuit shall be operated at +125°C ±5°C for a minimum of 300 hours with the nominal value of $V_{CC}$ applied. During the operation period, switching voltages with a constant frequency in the range of 1 to 100 kc, with a 50% duty cycle, shall be applied so that the outputs of the device are switching between the logical "1" and the logical "0" at the corresponding frequency.

b. Stabilize the integrated circuits for a minimum of 16 hours at +25°C ±3°C.

c. Complete the specified electrical tests within 24 hours of the completion of test (6.11.a) above.

d. The pre-and post-burn-in variables data shall be recorded for each input for $I_{in}$, and the $V_{out}$ high, $V_{out}$ low, $V_{in}$ low, $V_{in}$ high noise immunity readings (described in Paragraph 6.6.2.1) at +25°C. The initial and final data shall be compared and the following rejection criteria will apply:

$\Delta V_{out}$ high > -10% will be rejected.
$\Delta V_{out}$ low > +10% will be rejected.
$\Delta V_{in}$ low > ±10% will be rejected.
$\Delta V_{in}$ high > ±10% will be rejected.
$\Delta I_{in}$ > ±10% will be rejected.

6.12 Hermeticity Tests

The integrated circuits shall meet the limits indicated when subjected to the following tests. The purpose of these three tests is to detect leaks in any portion of the surface area or seal of the circuit package. The detection of a leakage rate greater than $1 \times 10^{-8}$ std cc/sec shall constitute a failure. These tests shall be performed in the following order:

6.12.1 Helium (or Radiflo) Leak Test - All integrated circuits shall be subjected to a Helium Leak Test in accordance with MIL-STD-202C, Method 112, Condition C, and the requirements specified below. The circuits shall be placed in a sealed chamber that shall be pressurized to 50 psig with helium gas for a minimum of 4 hours. The chamber shall then be evacuated and connected to a mass spectrometer capable of detecting leakage at the rate of $1.0 \times 10^{-8}$ std cc/sec within 1/2 hour after the integrated circuits are subjected to helium pressure. A leakage rate of $1.0 \times 10^{-8}$ std cc/sec or more shall constitute a failure. An equivalent Radiflo Test, performed in accordance with MIL-STD-202C, Method 112, Condition C will be considered as an acceptable substitute for the Helium Test.

6.12.2 Nitrogen Bomb Test - All integrated circuits shall be subjected to a Nitrogen Bomb Test in accordance with the following procedure. The circuits shall be subjected to a nitrogen gas pressure of 150 psig for a minimum of 10 hours. Devices will then be removed from the pressure vessel and placed in an alcohol bath such that the top of the package is under a 3/8 to 1/2-inch depth of alcohol. The alcohol bath container shall be under a binocular microscope of 7 to 10 power magnification. The time interval from beginning of depressurization to examination of the packages under the microscope shall be no longer than 3 minutes. The packages shall then be examined through the binocular microscope in groups of no more than 25 per person observing. Care should be taken to insure that no package shall rest on another package body. The entire group of 25 packages shall be examined for a continuous period of 15 minutes. The criteria of a failure shall be the observation of a continuous or intermittent stream of bubbles emanating from package leak producing areas during any examination period.

6.12.3 Hot Glycerine Bubble Test - The Hot Glycerine Bubble Test shall be performed, testing units in accordance with MIL-STD-202C, Method 112, Condition A, with the following exceptions:

a. Glycerine shall be used instead of mineral oil.

b. The failure criteria shall be the observation of a growing bubble emerging from a sealed area, instead of observation of a continuous stream of bubbles emanating from the specimen.

c. All units shall be thoroughly washed in deionized water following this test.

6.13 Final Electrical Tests

All integrated circuits delivered to this specification should exhibit working performance over the full range of temperature (-55 to $+125^{o}$C), loading and power supply variations. All the tests of Paragraph 6.6 shall be repeated to insure compliance with the performance requirements of the detail specification.

6.14 Lot Provisions

6.14.1 Production Lot - A production lot shall be any total quantity of integrated circuits continuously produced and having all manufacturing operations completed by a process known to be "In Control". The period of production at any individual manufacturing step (i.e. diffusion, metallization, packaging, lead bonding, etc.) shall be no greater than 2 calendar weeks. Each circuit within a particular production lot shall be of homogeneous material. Any significant process changes during the production period affecting the homogeneity of the lot, shall require a new production lot number.

6.14.2 Lot Size Requirements - Minimum lot size for statistical sampling shall be 200 integrated circuits. Smaller lots shall require 100% testing. Maximum lot size shall be 5000 integrated circuits.

6.14.3 Resubmission - If the lot fails during acceptance testing, rework and resubmission for acceptance shall not be allowed until written consent has been obtained from NASA. NASA shall be notified in writing within 1 week of all failures to pass lot acceptance by the subcontractor. Failure to complete the above steps may result in the rejection and return of all such material and the removal of qualification approval. Each time the lot is rescreened, the rescreened lot shall be treated as a new lot. The original acceptance test devices may be included as part of the rescreened lot provided all special markings are removed. The test report shall contain information as to the need for and the results of such rescreening(s).

6.14.4 Qualified Lot - A qualified lot shall consist of a production lot which has successfully passed the requirements of the acceptance tests. Each circuit within a particular qualified lot shall be marked with a single date code as specified in the detail specification.

6.14.5 Shipment - A shipment may consist of a qualified lot or portion of a qualified lot. Shipments may be made against more than one purchase order provided the integrated circuits for each purchase order are separately packaged and identified.

6.14.6 Integrated Circuit Age - Integrated Circuits shipped to NASA under this specification shall have been manufactured within 9 months of the date of shipment.

6.14.7 Test Reports - The original copy of the Acceptance Test Report of a qualified lot shall be held by the manufacturer for a minimum period of 2 years from the date of completion of the acceptance tests. A copy of all acceptance test results shall be included with each lot shipment to NASA.

The test report shall include a summary sheet listing by attributes the results of all tests required. The summary shall contain a listing and explanation of all markings shown on the components covered by the test report. The report shall list the part number and manufacturer's type number, inspection lot size, test sample size (sampling plan only), manufacturing date, acceptance date, production lot number(s), data of the manufacturer and the purchase order number. If the test report includes test data from several production lots, each production lot size shall be included. If data is recorded in some form that does not permit a direct reading, an explanation of the system shall be provided with each test report. This explanation shall include information regarding location of decimal points, etc.

6.14.8 Preservation and Packaging - Each circuit furnished under this specification shall be protected and packaged to afford protection at all handling points between manufacturer's final inspection and user's final installation. Each circuit shall be packaged in a transparent rigid-plastic container using flexible foam inserts for cushioning, or the equivalent thereof, as to allow viewing the circuit markings without opening the container.

6.14.9 Rejection - NASA reserves the right to re-inspect and test any portion of the delivered lot in accordance with the Quality Assurance requirements of the detail specification. NASA shall also have the right to return any devices which fail to meet these requirements.

The manufacturer shall also be responsible for any damage to circuits resulting from faulty packing, preservation, or packaging, and shall replace such circuits with acceptable circuits without cost to NASA.

## 7. QUALIFICATION REQUIREMENTS

In addition to all the screening acceptance tests of Table 6-1, all integrated circuits shall be capable of meeting the full qualification requirements contained in Table 7-1. These procedures shall be performed on samples drawn from the initial lot, and must be completed by the manufacturer prior to approval as a source of supply by NASA. NASA also reserves the right to order this qualification requirement on any given future lot. (Sufficient advance notice will be given when this additional requirement is to be made.)

TABLE 7-1

QUALIFICATION REQUIREMENTS

| TEST METHOD | MIL-SPEC REFERENCE | LTPD | MAX ACC NO. | SPECIFIC CONDITIONS |
|---|---|---|---|---|
| Physical Dimensions | MIL-STD-750A Method 2066 | 10 | 1 | Per Detail Specification |
| Solderability | MIL-STD-750A Method 2026.1 | 20 | 1 | All Leads |
| Soldering Heat | MIL-STD-750A Method 2031.1 | | | One Cycle |
| Lead Fatigue | MIL-STD-750A Method 2036.1 | 20 | 1 | Condition E. Test all leads on each device up to a maximum of ten (corner leads on 14-pin flat packs not included). Use 8-oz weight for TO -5 Packages, and 2-oz weight for Flat Packages (Paragraph 6.8). Three $90^{o}$ arcs. |
| Lead Tension | MIL-STD-750A Method 2036.1 | 20 | 1 | Condition A. Test all leads on each device up to a maximum of ten (corner leads on 14-pin flat packs not included). One axial pull of 1 lb for 30 sec. |
| Weldability (Gold-Plating Thickness) | MIL-G-45204 | 20 | 1 | Type II Gold-Plating, all leads shall be plated to a thickness of 100 to 200 micro-inches of gold. |

TABLE 7-1 (Cont)

QUALIFICATION REQUIREMENTS

| TEST METHOD | MIL-SPEC REFERENCE | LTPD | MAX ACC NO. | SPECIFIC CONDITIONS |
|---|---|---|---|---|
| Moisture Resistance | MIL-STD-750-A Method 1021.1 | 10 | 1 | For initial conditioning use 8-oz weight for TO-5 Packages and 2-oz weight for Flat Packages (Paragraph 6.8) |
| Centrifuge | MIL-STD-750-A Method 2006 | 10 | 1 | 20,000 G's for 1 minute each orientation: $X_1$, $X_2$, $Y_1$, $Y_2$, $Z_1$, $Z_2$ |
| Shock | MIL-STD-750-A Method 2016.1 | | | 1500 G's, for 0.5 m sec, 25 blows in each of 4 directions: $X_1$, $Y_1$, $Y_2$, $Z_1$ min. Total 100 Blows. |
| Vibration Fatigue | MIL-STD-750-A Method 2046 | 10 | 1 | 30 G's, at 60 ±20 cps. for 32 ± 8 hr, in each orientation: $X_1$, $Y_1$, $Z_1$. Total 96 hr minimum. |
| Variable Frequency Vibration | MIL-STD-750-A Method 2056 | | | 30 G's, thru frequency range of 10 to 2000 cps and back to 10 (logarithmic sweep) for 4 minutes minimum each orientation: $X_1$, $Y_1$, $Z_1$. Total of 12 times for 48 minutes. |
| High Temperature Storage Life (Non-Operating) | MIL-STD-750A Method 1031.1 | 5 | 2 | $T_A$ = +150°C (minimum) t = 1000 Hr |

TABLE 7-1 (Cont)

QUALIFICATION REQUIREMENTS

| TEST METHOD | MIL-SPEC REFERENCE | LTPD | MAX ACC NO. | SPECIFIC CONDITIONS |
|---|---|---|---|---|
| Operating Life | MIL-STD-750A Method 1026.1 | 5 | 2 | $T_A$ = +125°C<br>t = 1000 Hr<br>with $V_{CC}$ applied and switching voltage applied at frequency in the 1 to 100 KC range, with 50% duty cycle, switching between logical "1" and "0". (Endpoint tests per Paragraph 6.11d) |
| Temperature-Altitude | MIL-STD-750A Method 1001.1 | 10 | 1 | Maintain the vacuum of MIL-STD-202C, method 105C, condition G throughout this test. Hold +125°C for 8 hr, -85°C for 8 hr, and +25 °C for 4 hr. All circuits shall be continuously operated and their performance monitored during the entire test. |

# PART 2
# SPECIFICATION DEVELOPMENT AND TEST RESULTS

A step-by-step description of the development of the General Specification, as well as the philosophy behind the choice of each test, is presented in this part of the report. The results of the test phase of this program are also included, with Section 2.0 containing detailed descriptions of the 100-percent non-destructive tests and Section 3.0 describing the destructive tests. Specific recommendations for the incorporation of these techniques into the General Specification are also described in these sections.

## 1.0 TEST SPECIFICATION DEVELOPMENT

In describing the development of the General Specification, each test or control is itemized in this section. A discussion is then presented on the factors which governed the selection of test limits for each method. This is followed by reasons for including each method in a particular schedule (qualification, screening, etc.) and for placing it at a particular point in the schedule, i.e., test sequence. The major portions of the specification which are discussed in this section are general provisions, acceptance test provisions, and qualification test requirements.

### 1.1 GENERAL PROVISIONS

It is axiomatic that high reliability in integrated circuits for space system applications must be built in through tight process controls. However, the only practicable means of enforcing these controls is through the application of screening tests, such as those contained in the General Specification presented in Part 1. Devices that have passed such a high reliability screening test possess an inherent reliability because the latent failures have been screened out and eliminated. The approach used for developing each portion of the general provisions follows.

#### 1.1.1 Materials, Processing and Workmanship

In the development of the General Specification, considerable stress was placed on the areas of materials, processes, and workmanship. These areas rightly belong in a General Specification since they represent factors common to all integrated circuit devices. Furthermore, the importance of these factors lies beyond that of routine performance tests. While performance tests are essential to show what the devices will do now, it is only by controlling device materials, processes, and workmanship that the user can insure their guaranteed future performance, i.e. long-term reliability.

#### 1.1.2 Standardization of Test Parameters and Acceptance Levels

One of the basic features of the General Specification is the proposed standardization of test parameters and acceptance levels for all digital integrated circuits. Significant benefits to be realized from this standardization are the direct functional and performance comparisons of devices procured from different sources.

There exists a great need for such direct comparisons between different integrated circuits. Currently, it is difficult to compare the performance of different microelectronic devices

because the standards by which performance is measured vary greatly between different manufacturers.

These differences can take subtle forms. For example, the same end point limits can be specified but different levels of circuits passing these limits may be allowed. By setting uniform allowable levels of circuits falling beyond the end points in the General Specification developed under this program, performance can be realistically expressed by the end points only. In this way, the circuit designer can rely upon end-point limits to realistically reflect the differences between device types.

### 1.1.3 User's Responsibility and Test Capability

Every attempt was made in the preparation of the General Specification to stress simplicity and to avoid creating unreasonable or unenforceable requirements. These precautions are considered a basic part of the user's responsibility. To fulfill his responsibility, it is also considered necessary for the user to develop sufficient test capability so that adequate but reasonable controls can be established and enforced. An optimum combination of test capability and specification controls is required to convince the vendor that the user can be expected to test for conformance whether the vendor does so or not, and that he reserves the right to reject lots on this basis. Throughout the specification, the heaviest emphasis has been placed on what the user should do to insure that the manufacturer performs to the specification, rather than placing the entire burden upon the judgment and integrity of the manufacturer.

### 1.1.4 Data Feedback

Data feedback from the manufacturer is essential for implementing this specification at an optimum level of operation in terms of cost effectiveness. For this reason, extensive provisions have been included for the establishment of Reliability and Quality Assurance systems by the manufacturer. These also include requirements for the generation of detail specifications, process flow charts, failure analysis procedures, and corrective action reports.

Furthermore, all detail specifications for integrated circuits must be consistent with the provisions of the General Specification. Any requests for deviations by vendors should be specifically referenced to the appropriate section and supported by sufficient data. Deviations, if granted, should then be "highlighted" in the detail specifications, and only the unmodified General Specification should be forwarded to other prospective vendors.

It is only in this manner that the General Specification can serve its intended function of continually directing the vendors toward the preferred process methods and controls.

### 1.1.5 System Performance

Finally, it should be stated that no specification can be considered complete unless its objectives are clearly specified in terms of the device's ultimate performance requirements. In meeting a high reliability integrated circuit specification, all parties involved must be made aware of the reliability requirements for actual system performance. The general specification was established to define circuits which will be consistent with a system performance requirement of 1 failure (maximum) per 5,000,000 unit hours of system operation, in which the circuits may be operating over a temperature range of -55 to +125°C.

The above considerations, along with the information contained in the detailed provisions following, are intended to emphasize that high reliability can only result from the joint efforts of both the integrated circuit manufacturer and the user.

## 1.2 ACCEPTANCE TEST PROVISIONS

The approach taken to develop a screening-acceptance test specification for Goddard Space Flight Center was to correlate all possible failure mechanisms for integrated circuits with state-of-the-art analytical techniques.

As the first step in the preparation of this correlation program, complete listings were made of the possible failure modes which could be encountered (Table 1-1). These were classified according to basic failure modes (opens, shorts, defective seals, and poor workmanship) with sub-classifications pin-pointing the specific failure mechanisms and a further subdivision indicating the cause.

The second step consisted of listing and categorizing the test methods which could be employed for failure detection. All the tests in MIL-STD-750 and MIL-STD-202 were considered for their applicability. In addition, a complete industry survey of advanced analytical techniques was made. It was also considered essential to the understanding of these techniques to provide a description of each method, as well as an evaluation of each in terms of cost, status of technology, and test limitations. This information is contained in Table 1-2.

Once an understanding of the basic failure mechanisms and test methods is achieved, it is possible to determine which method or methods are most suitable to detect a given failure mode. This was accomplished by a series of matrix plots. An initial matrix was constructed by plotting all the test categories against the four major failure mode classifications.

Following the elimination of test methods which are *not* applicable for certain failure modes, the initial matrix was expanded to detail each of the major failure mode classifications (Table 1-3).

It is evident from this correlation that the development of a high reliability screening specification must include a study of a number of test methods to determine their effectiveness and applicability in revealing latent failure mechanisms. During the study phase of this Program, Grumman visited selected LEM sub-contractors, microelectronic suppliers, and evaluation laboratories. The most up-to-date information available on microelectronic processing and evaluation techniques was compiled as a result of all the surveys made during the study phase. This represents the latest state-of-the-art technology and constitutes an essential contribution to the development of the General Specification.

On the basis of this Program, it was possible to generalize the manufacturing process for integrated circuits. Essentially, each manufacturer uses the same general processes as follows:

- Wafer Preparation (including etching and polishing)
- Circuit Formation (including oxide growth, diffusion, epitaxial growth, where applicable, and metallization)
- Electrical Probing of Wafer
- Scribing and Dicing
- Die Mounting Into Package
- Wire Bonding
- Internal Visual Inspection
- Final Sealing
- Acceptance Tests
- Classification, Marking, Packing, and Shipping.

TABLE 1-1 EXPECTED MODES OF FAILURE IN MICROCIRCUITS

1.0 Electrical Opens or High Resistance

- 1.1 Leads
  - 1.1.1 Lead Fatigue (broken lead)
  - 1.1.2 Nicked or Cut leads
- 1.2 Wire Bonded to lead inside case
  - 1.2.1 Underbonding
  - 1.2.2 Plague
  - 1.2.3 Overbonding
- 1.3 Bonding wire
  - 1.3.1 Nicked or Cut wires
  - 1.3.2 Poor bonding
  - 1.3.3 Overcurrent
  - 1.3.4 Stretched wire
- 1.4 Wire bonded to Metallized Interconnections
  - 1.4.1 Underbonding
  - 1.4.2 Plague
  - 1.4.3 Overbonding
- 1.5 Interconnections
  - 1.5.1 Metal scratches
  - 1.5.2 Oxide steps
  - 1.5.3 Corrosion
  - 1.5.4 Plague
  - 1.5.5 Overcurrent
  - 1.5.6 Overbonding
  - 1.5.7 Masking defect
- 1.6 Metallized Interconnections Evaporated on Substrate
  - 1.6.1 Poor adhesion
  - 1.6.2 Misregistration
- 1.7 Substrate (includes components and junctions)
  - 1.7.1 Cracked chip
  - 1.7.2 Poor oxide adhesion

2.0 Electrical Shorts or Low Resistance

- 2.1 Shorts to package
  - 2.1.1 Caused by overlong bonding wires
  - 2.1.2 Caused by deformed package

TABLE 1-1 EXPECTED MODES OF FAILURE IN MICROCIRCUITS (Cont)

- 2.2 Shorts to package leads or bonding wires
  - 2.2.1 Lead-to-lead short
  - 2.2.2 Wire-to-wire short
    - 2.2.2.1 Overlong wires
    - 2.2.2.2 Toe of bond touching other wire
    - 2.2.2.3 Extra leads
  - 2.2.3 Lead-to-wire short
  - 2.2.4 Interconnection to wire
    - 2.2.4.1 Overlong wires
    - 2.2.4.2 Extra leads
    - 2.2.4.3 Foreign matter
  - 2.2.5 Substrate to wire
- 2.3 Shorts to interconnections
  - 2.3.1 Interconnection-to-interconnection shorts
    - 2.3.1.1 Masking error
    - 2.3.1.2 Misregistration
    - 2.3.1.3 Scratching or smearing
  - 2.3.2 Substrate to interconnection
    - 2.3.2.1 Masking error
    - 2.3.2.2 Misregistration
    - 2.3.2.3 Poor oxide dielectric strength
- 2.4 Short to substrate/components
  - 2.4.1 Component-to-component short
    - 2.4.1.1 Overcurrent
    - 2.4.1.2 Overvoltage (breakdown)
    - 2.4.1.3 Leakage degradation
    - 2.4.1.4 Cracked chip
  - 2.4.2 Component-to-substrate

- 3.0 Defective Seals
  - 3.1 Crack in package
  - 3.2 Non-hermetic lead seal
  - 3.3 Non-hermetic package seal

- 4.0 Poor Workmanship and Mechanical Defects
  - 4.1 Failure to meet dimension criteria
  - 4.2 Incorrect marking orientation
  - 4.3 Substrate mounting to package
    - 4.3.1 Excessive voids
    - 4.3.2 Poor adhesion causing die to separate
    - 4.3.3 Substrate unsupported in bond area
  - 4.4 "Hot spots" resulting from irregular metallization or scratches

TABLE 1-1 EXPECTED MODES OF FAILURE IN MICROCIRCUITS (con't)

4.5 Excessive oxide pinholes
4.6 Excessive interconnection pinholes
4.7 Material defects
4.8 Contamination and foreign matter
4.9 Insufficient oxide thickness
4.10 Chemical residues on chip surface

TABLE 1-2 TEST METHODS FOR FAILURE DETECTION

1.0 Non-Destructive Tests

1.1 Visual Inspections

1.1.1 Internal Visual Inspection before sealing
1.1.2 Physical Dimension Tests
1.1.3 External Visual Inspection

1.2 Electrical Tests

1.2.1 Functional Test
1.2.2 D. C. Parameter Tests
1.2.3 Noise Immunity Tests
1.2.4 Dynamic Parameter Tests
1.2.5 Threshold Tests (Substrate Breakdown Tests)
1.2.6 Power Dissipation Tests
1.2.7 Insulation Resistance Test

1.3 Operating and Extended Life Tests

1.3.1 Operating Life Tests (sampling)

1.3.1.1 Operating life at room temperature (full rated power)
1.3.1.2 Operating life at high temperature (derated power)

1.3.2 Operating Burn-In Tests (100%)

1.3.2.1 Operating Burn-In Tests at room temperature (full rated power)
1.3.2.2 Operating Burn-In Tests at high temperature (derated power)

1.3.3 High Temperature Bake Tests (no power)

1.3.3.1 High Temperature Storage life (sampling)
1.3.3.2 High Temperature Stabilization Bake (100%)

1.3.4 Parameter Drift Tests

1.3.4.1 Can do as Pre-operating Life and Post-operating Life Tests
1.3.4.2 Can do as Pre-burn-in and Post-burn-in Tests
1.3.4.3 Can do as Pre-high Temperature Bake and Post-high Temperature Bake Tests

1.4 Environmental Tests

1.4.1 Temperature Tests

1.4.1.1 Temperature cycling
1.4.1.2 Thermal shock
1.4.1.3 Dew point

TABLE 1-2 TEST METHODS FOR FAILURE DETECTION (con't)

- 1.4.2 Mechanical Tests
  - 1.4.2.1 Centrifuge (constant acceleration)
  - 1.4.2.2 Shock
  - 1.4.2.3 Vibration (monitored or unmonitored)
    - 1.4.2.3.1 Vibration fatigue
    - 1.4.2.3.2 Vibration, variable frequency
    - 1.4.2.3.3 Random Vibration
- 1.4.3 Barometric pressure (altitude)
- 1.4.4 Thermal Vacuum

1.5 X-Ray Tests

1.6 Hermeticity (Leak) Tests

- 1.6.1 Oil Bubble (or Hot Glycerin) Tests
- 1.6.2 Helium Leak (or Radiflo) Tests
- 1.6.3 Nitrogen Bomb Tests

2.0 Destructive Tests

2.1 Internal Visual Inspection after sealing

2.2 Physical Tests

- 2.2.1 Bond Tension
- 2.2.2 Lead Tension
- 2.2.3 Lead Fatigue
- 2.2.4 Solderability
- 2.2.5 Resistance to soldering heat
- 2.2.6 Weldability

2.3 Environmental Tests (atmospheric)

- 2.3.1 Salt atmosphere (corrosion)
- 2.3.2 Salt spray (corrosion)
- 2.3.3 Moisture resistance
- 2.3.4 Humidity

2.4 Analytical Tests

- 2.4.1 High Power Microscopic Inspection
- 2.4.2 Electrical probing of circuit elements
- 2.4.3 Infrared scanning
- 2.4.4 Electron microprobe X-Ray analysis
- 2.4.5 Scanning electron microscopy
- 2.4.6 Anion Reaction Tests
- 2.4.7 Microsectioning

TABLE 1-3 TEST METHODS VS FAILURE MODES

| Method | Electrical Opens or High Resistance | Electrical Shorts or Low Resistance | Defective Seals | Workmanship |
|---|---|---|---|---|
| Visual Inspection | Y | Y | Y | Y |
| Electrical Tests | Y | Y | N | N |
| Operating Life Tests | Y | Y | N | N |
| Environmental (Temperature) | Y | Y | Y | N |
| Environmental (Mechanical) | Y | Y | N | Y |
| Environmental (Altitude) | N | Y | N | N |
| X-Ray | Y | Y | Y | Y |
| Hermeticity (Leak) Tests | N | N | Y | N |
| Physical Tests | N | N | N | Y |
| Environmental (Atmospheric) | N | N | Y | Y |
| High-Power Microscopic Inspection | Y | Y | Y | Y |
| Electrical Probing of Circuit Elements | Y | Y | N | N |
| Infrared Scanning | N | N | N | Y |
| Electron Microprobe X-Ray Analysis | N | N | N | Y |
| Scanning Electron Microscopy | N | N | N | Y |
| Anion Reaction Tests | N | N | N | Y |
| Microsectioning | Y | Y | Y | Y |

LEGEND: Y Yes, category is applicable and is expanded in Tables 1-4 through 1-7.

N No, category is not applicable and is eliminated from further consideration in this report.

TABLE 1-4 TEST METHODS VS FAILURE MODES TO DETECT ELECTRICAL OPENS OR HIGH RESISTANCE

| Method | Leads | Bond to Lead | Bonds | Bond to Inter-Connection | Inter-Connection | Inter-Connection to Substrate | Substrate |
|---|---|---|---|---|---|---|---|
| Visual Inspection | Y | Y | Y | Y | Y | Y | Y |
| Electrical Tests | Unable to differentiate and pin point | | | | | | |
| Operating Life Tests | Location of open without further analysis | | | | | | |
| Environmental (Temperature) | N | Y | N | Y | N | Y | Y |
| Environmental (Mechanical) | N | Y | N | Y | N | Y | Y |
| X-Ray | Y | Y | Y | Y | N | N | N |
| High-Power Microscopic Insp. | Y | Y | Y | Y | Y | Y | Y |
| Electrical Probing of Circuit Elements | Y | Y | Y | Y | Y | Y | Y |
| Microsectioning | N | Y | N | Y | Y | Y | Y |

TABLE 1-5 TEST METHODS VS FAILURE MODES TO DETECT ELECTRICAL SHORTS OR LOW RESISTANCE

| Method | Shorts to Package | | Lead to Lead | Wire to Wire | Lead to Wire | Intercon. to Wire | Substrate to Wire | Intercon. to Intercon. | Substrate to Intercon. | Component to Component | Component to Substrate |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Overlong Bond Wires | Deformed Package | | | | | | | | | |
| **Visual Inspection** | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| **Electrical Tests**<br>**Operating Life Tests**<br>**Environmental (Altitude)** | Unable to Differentiate and Pin Point Shorted Element Location Without further Analysis. | | | | | | | | | | |
| **Environmental (Temperature)** | N | N | N | N | N | N | N | N | N | Y | Y |
| **Environmental (Mechanical)** | Y | Y | Y | Y | Y | Y | Y | N | N | Y | Y |
| X-Ray | Y | Y | Y | Y | Y | Y | N | N | N | N | N |
| **High-Power Microscopic Inspection** | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| **Electrical Probing of Circuit Elements** | N | N | N | N | N | N | N | Y | Y | Y | Y |
| **Microsectioning** | Y | Y | N | N | N | N | N | Y | Y | Y | Y |

TABLE 1-6 TEST METHODS VS FAILURE MODES TO DETECT DEFECTIVE SEALS

| Method | Cracks in Package | Non-Hermetic Lead Seal | Non-Hermetic Package Seal |
|---|---|---|---|
| Visual Inspection | Y | Y | Y |
| Environmental (Temperature) | Y | Y | Y |
| X-Ray | N | Y | Y |
| Hermeticity (Leak) Tests | Y | Y | Y |
| High-Power Microscopic Inspection | Y | Y | Y |
| Microsectioning | N | Y | Y |
| Environmental (Atmospheric) | Y | Y | Y |

**TABLE 1-7 TEST METHODS VS FAILURE MODES TO DETECT POOR WORKMANSHIP AND MECHANICAL DEFECTS**

| Method | Dimensions | Marking Orientation | Substrate Mounting | Hot Spots | Pinholes | Material Defects | Contamination and Foreign Matter | Thin Oxide |
|---|---|---|---|---|---|---|---|---|
| Visual Inspection | Y | Y | N | N | Y | Y | Y | N |
| X-Ray | N | Y | Y | N | N | Y | Y | N |
| Physical Tests | N | N | N | N | N | Y | N | N |
| Environmental (Atmospheric) | N | N | N | N | N | Y | N | N |
| High - Power Microscopic Inspection | Y | Y | N | N | Y | Y | Y | N |
| Infrared Scanning | N | N | N | Y | Y | Y | N | N |
| Electron Microprobe X-Ray Analysis | N | N | N | Y | Y | Y | Y | N |
| Scanning Electron Microscopy | N | N | N | Y | Y | Y | N | N |
| Anion Reaction Tests | N | N | N | N | Y | Y | N | Y |
| Microsectioning | N | N | Y | N | Y | Y | Y | Y |
| Environmental (Mechanical) | N | N | Y | N | N | Y | Y | N |

The point of departure from this general manufacturing flow is that the screening acceptance test provisions must begin at internal visual inspection. The entire acceptance provisions are listed in the order in which they must be performed:

- Internal Visual Inspection (before Sealing)
- Marking Requirements
- External Visual and Mechanical Inspection
- Marking Permanency Test
- Stabilization Bake
- Electrical Tests
  - General
  - Noise Margin
  - Fan-Out (Loading) and Fan-In
  - Detail Parameter
  - Dynamic Parameter
- Thermal Cycling (Shock)
- Mechanical
  - Centrifuge
  - Vibration (Variable Frequency Monitored)
- X-Ray
- Burn-In (With Variables Data)
- Hermeticity Tests
- Final Electrical
- Lot Provision

The importance of test sequence cannot be overstated if the user is to prevent the development of an elaborate (and costly) test procedure which loses its effectiveness because the tests are performed at the wrong point in the schedule. This is especially true when considering the environmental test sequence. For example, the leak test should be done late in the program to uncover any seal defects which are aggravated by the temperature and mechanical stresses encountered during other parts of the environmental test schedule.

The approach taken to develop each portion of the acceptance test provisions is detailed in the following paragraphs:

### 1.2.1 Internal Visual Inspection

For a high-reliability screening program, the user's control must begin at internal visual inspection. Thus, the general test specification begins at this stage and defines the internal visual inspection requirements in great detail.

An internal visual inspection consists of an optical examination of an integrated circuit prior to sealing to evaluate workmanship, process uniformity, and dimensional conformity, in addition to revealing contamination and foreign matter. All other screening for these defects represents tests performed "after the fact". Thus, the user's surveillance should definitely include visits to the manufacturer to control this operation. This represents the one best chance to control what goes into the package. This is especially necessary where X-ray is ineffective due to the use of aluminum bonding wires.

The criterion chosen for this inspection was to specify an absolute minimum dimension where defects or poor design could cause shorting or low breakdown voltages. Generally, a well-designed integrated circuit provides at least a two to one overcurrent capacity. Thus, where percentage figures were necessary to define a reject criteria for metallization defects, the figure 50% was most often used.

Open bonds are one of the most prevalent failure modes for integrated circuits and bond strength is directly proportional to contact area. This, a high-reliability integrated circuit must have the entire bond within the periphery of the bonding pad. This criterion has the dual advantage of minimizing or eliminating the need for subjective judgments on the part of the operator, while assuring the highest reliability attainable for space system applications.

### 1.2.2 Marking Requirements

It was decided that each device should be identified and serialized immediately after sealing. In this way, all test results can be correlated to specific devices, and misorientation of markings will be detected.

The identifying number is broken into a lot number and a serial number within the lot. In this way, defects can be traced back to specific manufacturing process lines. Manufacturing and acceptance date codes may also be incorporated to allow enforcement of a storage time limit for the lot, and to determine whether retests are necessary before use of the devices.

1.2.3 External Visual and Mechanical Inspection

The purpose of this examination is to verify that materials, design, construction, marking, and workmanship are in accordance with all the applicable requirements. Most specifications throughout industry call out Method 2071 of MIL-STD-750 without any further elaboration. Method 2071 merely directs the reader to consult the detail specification. Thus it is meaningless. Detailed provisions for drawing conformance, marking and identification, finish, contamination, homogeneity, seals, and leads must be stated explicitly.

1.2.4 Marking Permanency Test

Most specifications have marking permanency requirements but they are rarely supported by a test to guarantee permanency. Thus, a sampling test for permanency was added to the specification to verify that all identification markings were permanent and resistant to removal by handling and subjection to the specified environmental conditions. NASA may substitute any other solvent for trichlorethylene and xylene depending on the severity of the actual system environments.

1.2.5 Stabilization Bake

These tests should be performed by the manufacturer to stabilize electrical characteristics, to allow subsequent tests to represent actual service performance. The manufacturers will usually perform stabilization bake since it is to his advantage, but it must also be included in a high-reliability specification to assure uniformity of testing conditions between different manufacturers.

Careful consideration should also be given to the choice of temperature limits. Temperatures above +175°C may have the effect of creating long-term failure mechanisms such as plague.

1.2.6 Electrical Tests

1.2.6.1 General - Provision has been made in the General Specification for a minimum standardized series of electrical parameters which are necessary to completely characterize digital integrated circuit devices. For this reason, worst-case temperature and loading conditions were specified to insure compliance with all electrical performance requirements.

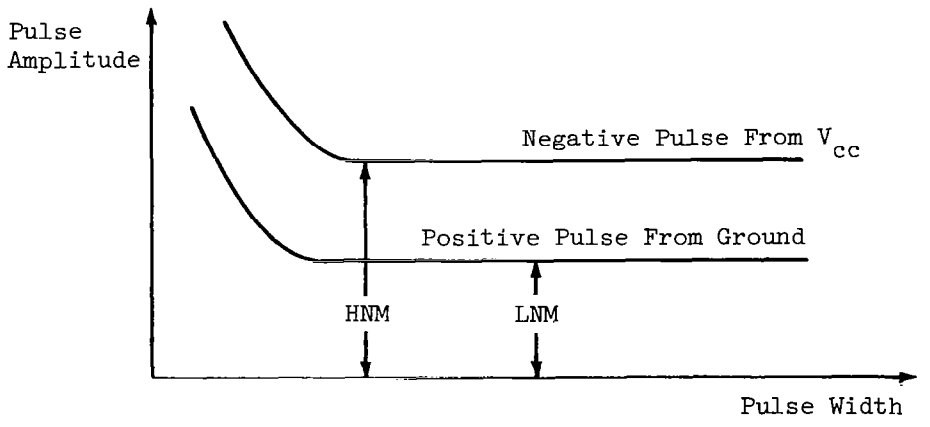
The viewpoint which must be continually stressed is that electrical data has a double significance, since it must be used by the system designer as well as the component engineer. For these reasons, it should include only realistic performance characteristics which will prevent weak designs. Manufacturers data sheets are usually inadequate in this area.

It is necessary to determine realistic absolute maximum ratings as early as possible to restrict the application of the devices to conservative levels of operation thus achieving a high system reliability. As an example of this approach, it is recommended that the absolute maximum rating for $V_{CC}$ be at least twice the value of the nominal operating voltage.

It is also recommended that noise margin be specified as an absolute minimum d-c noise immunity requirement for each logic form. Test data was developed during this Program for the purpose of establishing these minimum values of noise margin. For example, a minimum value of 400 mv is considered an achievable worst case d-c noise margin for diode-transistor logic (DTL).

1.2.6.2 Noise Margin - The next consideration in defining noise margin is whether to use A-C or D-C (or both) tests to derive high noise margin and low noise margin.

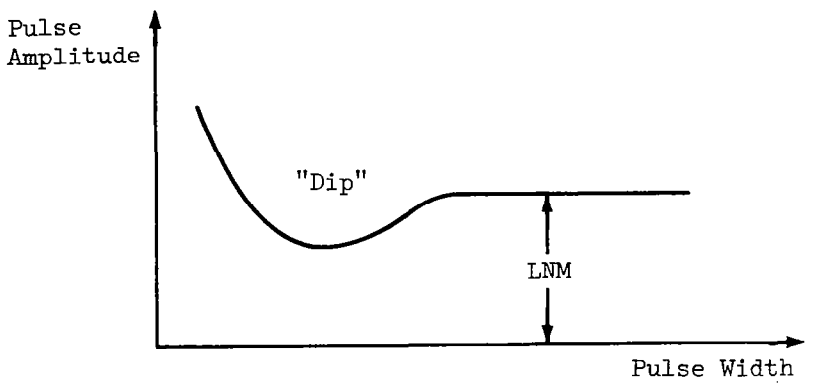
Tests were run on several microcircuit types (RTL, DTL, TTL, etc.) to determine the actual noise margins as a function of noise pulse width for both high and low levels. The test results indicated that for all but "forced capacitive" type microcircuits the noise margin increases with decreasing pulse width as shown in the following sketch:



Another way of stating this result is that when the noise pulse is wide the noise threshold of the microcircuit is voltage dependent. As the noise pulse becomes narrow, the noise threshold is more dependent on the total noise energy which equals the pulse amplitude times pulse width. This proves that the D-C or wide pulse noise threshold is the most critical case since a minimum voltage is required to false trigger the microcircuit.

While systems could be designed to take advantage of narrow-pulse, high noise thresholds, such a design approach is generally impractical because of the special A-C noise tests which would be necessary to screen the microcircuits for system use. A more logical approach is to design the system using the D-C noise margin as worst case and disregard the A-C factors. The exception to this procedure occurs when using RCTL type microcircuits which have "forced" or "speed-up" capacity in the input networks.

The following sketch shows that RCTL circuits are sensitive to narrow pulse widths. This has the effect of lowering the A-C noise threshold below the wide pulse of the D-C noise margin. Thus, an additional A-C noise test is required for RCTL circuits and the system design criteria must reflect the lower noise threshold.




1.2.6.3 Fan-Out (Loading) and Fan-In - Equivalent loading and fan-in requirements shall be developed for each logic form. These equivalent loads must be expressed as fixed combination of discrete components rather than a unit "live" load of the same logic type. The use of discrete equivalent loads in testing microcircuit parameters is extremely important, since data on a particular type of microcircuit can be directly compared to previous results only when the same equivalent load network is used.

The general approach to the development of suitable equivalent loads for microcircuit parameter testing varies for the different logic families. For example, Figure 1-1A shows a typical RTL stage, and its low frequency input equivalent is shown in Figure 1-1B. Resistance R in Figure 1-1B is the resistance in series with the base of the transistor. Diode D represents the base-emitter junction of the transistor. By using the Tektronix 575 Curve Tracer (Figure 1-2) the value of R and the equivalent discrete diode can be found. For silicon planar devices, it may be assumed that all diodes within the package exhibit the same V-I characteristic. Figure 1-3 shows a pair of V-I characteristics. Curve A shows the characteristics of the input to the RTL integrated circuit, and Curve B is its discrete component equivalent. R in this case was found to be 510 ohms and D is a IN914 diode. If multiple loading is desired, parallel combinations of Figure 1-1B can be used. However, for convenience and limitation of the number of components, a close approximation can be made by dividing the resistor R by the number of loads desired and a single series diode can be used.

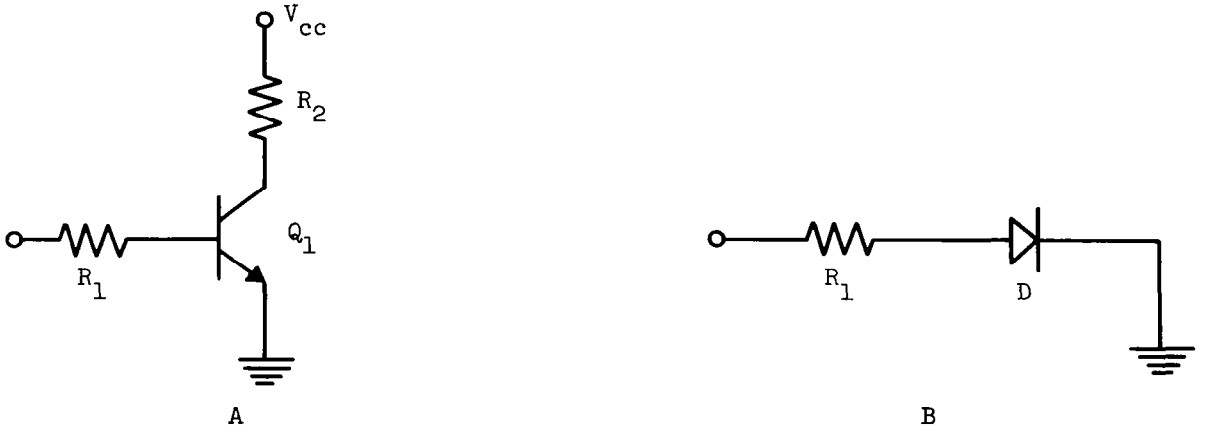



Figure 1-1 Typical RTL Stage (A) and Low Frequency Input Equivalent Network (B)

Similarly, a low frequency equivalent can be devised for DTL circuitry. Figure 1-4 shows a typical DTL integrated gate and its equivalent. Again, by use of the 575 curve tracer, the components can be characterized and matched with an equivalent discrete part. In Figure 1-5, curve A shows the integrated diode characteristic, and curve B shows the characteristic of a IN749 diode. Resistor $R_1$ can be determined with the curve tracer between the expander terminal and the +V terminal (Figure 1-6). The resistor $R_2$ in series with two diodes can be determined via the expander terminal E and the -V terminal. Traces A and B of Figure 1-7 show the characteristic of the integrated circuit (from E to -V) and its discrete equivalent, respectively.

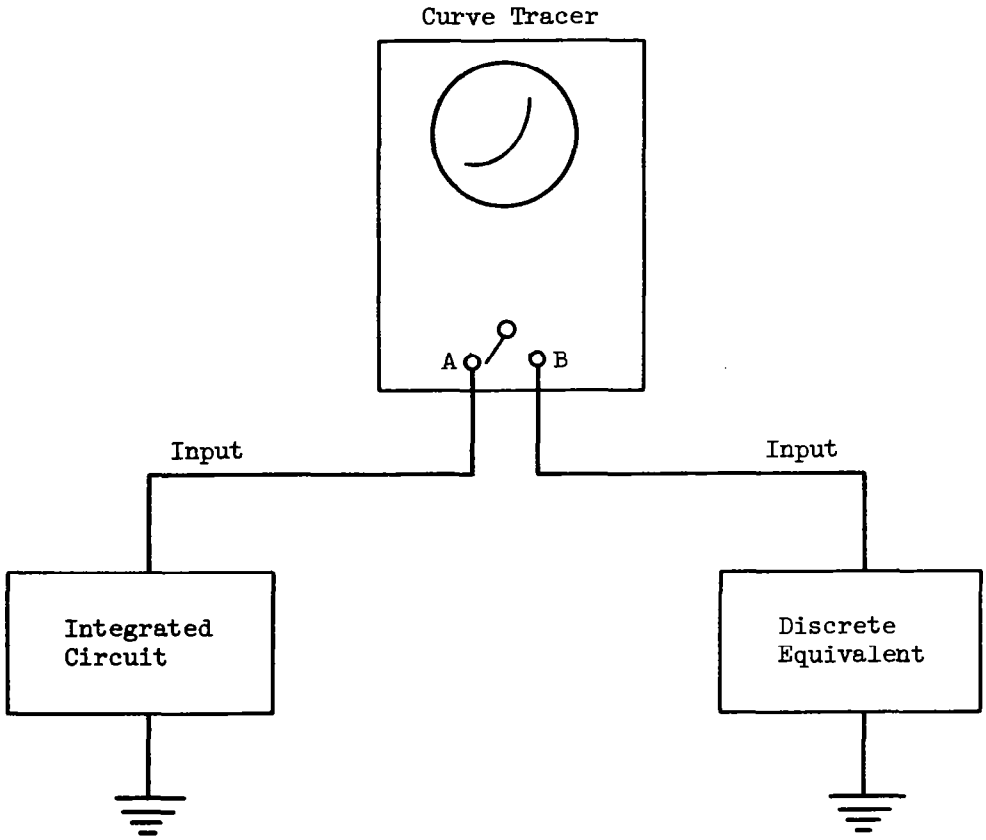



Figure 1-2 Low Frequency Input Equivalent Test Configuration

For the case of the DTL gate, the diodes were found to be similar to IN749 diodes, resistor $R_1$ was fround to equal 510 ohms, and $R_2$ was found to be 18K ohms. Therefore, the low frequency input characteristic of the DTL gate can be simulated by the configuration of Figure 1-4 where all diodes are type IN749, $R_1$ is 510 ohms, and $R_2$ equals 18K ohms. Multiple loading can be accomplished in the same way as RTL circuitry.

Synthesis of high frequency loads is accomplished in the same manner as low frequency, with the exception that the input capacity of the circuit must be accounted for. The input capacity of an actual load (circuit) can be measured by use of a Q-meter or other capacitance bridge. The capacitance required for N loads is N multiplied by the input capacitance of one circuit. This capacitance is measured from the input to the substrate of the circuit. The test configuration for measurement of the input capacity of an integrated

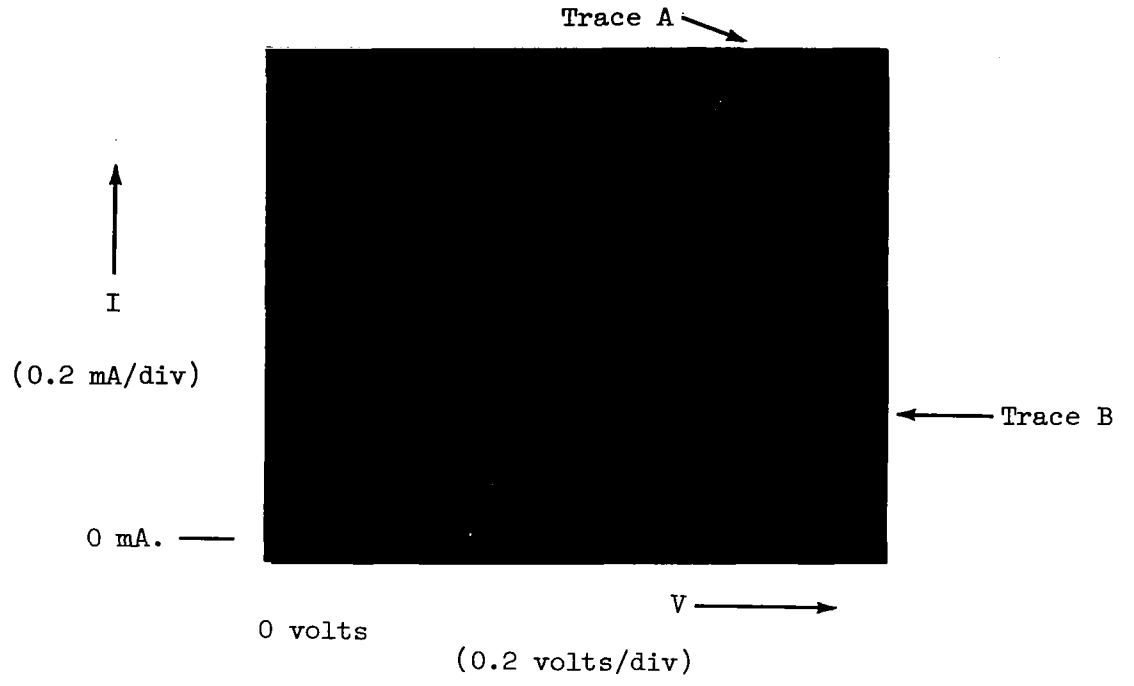



Figure 1-3 Input Characteristics for RTL Microcircuit (Trace A) and for Simulated Equivalent Load Network (Trace B)

circuit is shown in Figure 1-8. Care should be taken to account for stray capacity (leads, etc.) when making this measurement.

It is recommended that loading conditions be included in a "family" specification which defines the logic form (such as a basic RTL gate) and which includes all requirements common to devices in the specified family. Individual type specifications should then be generated for each device within the family to define such items as the interconnection pattern and electrical parameters which make that device unique.

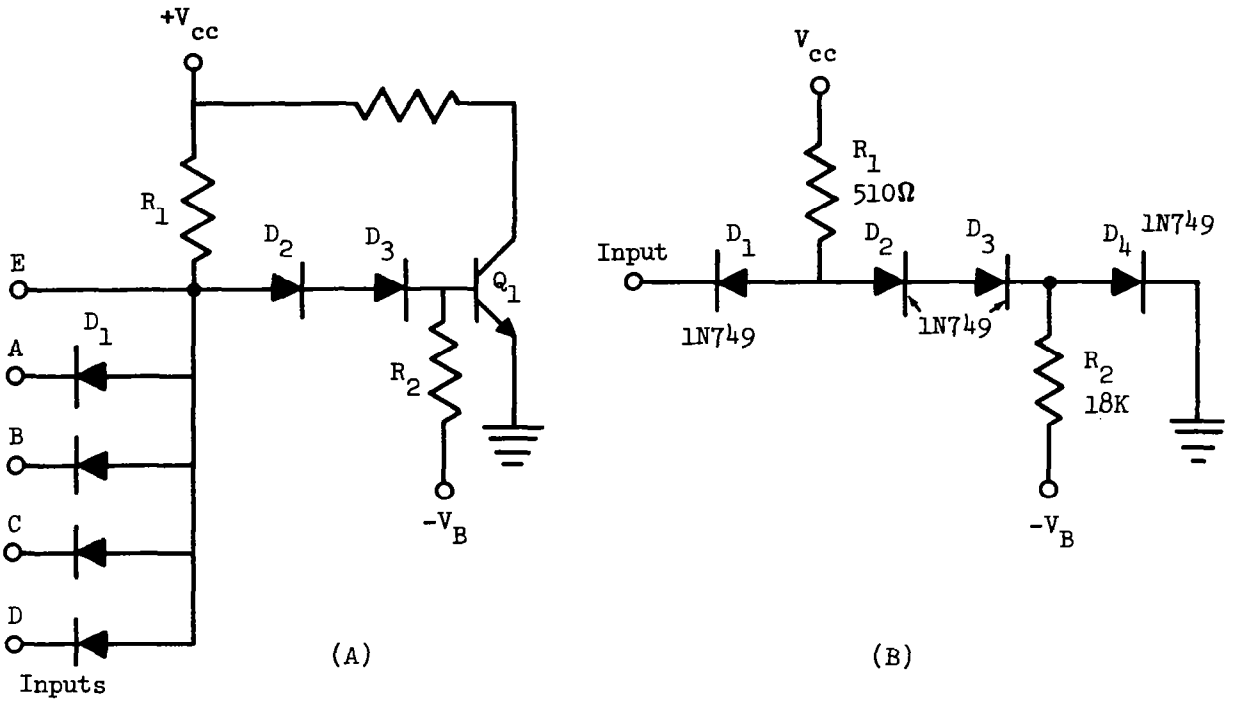



Figure 1-4 Schematic Diagram for DTL Logic (A) and Derived Equivalent Simulated Load Network (B)

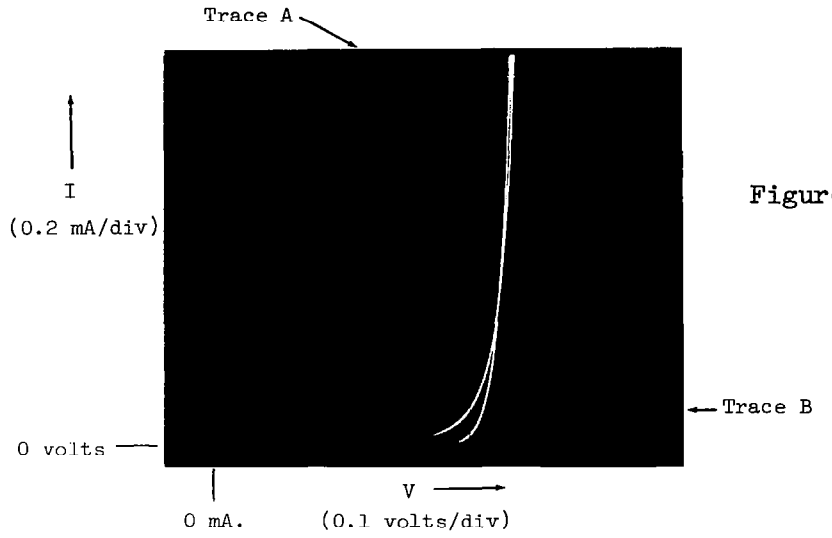



Figure 1-5 Input Characteristics of DTL Microcircuit (Trace A) and of 1N749 Diode Used for Simulated Load (Trace B)

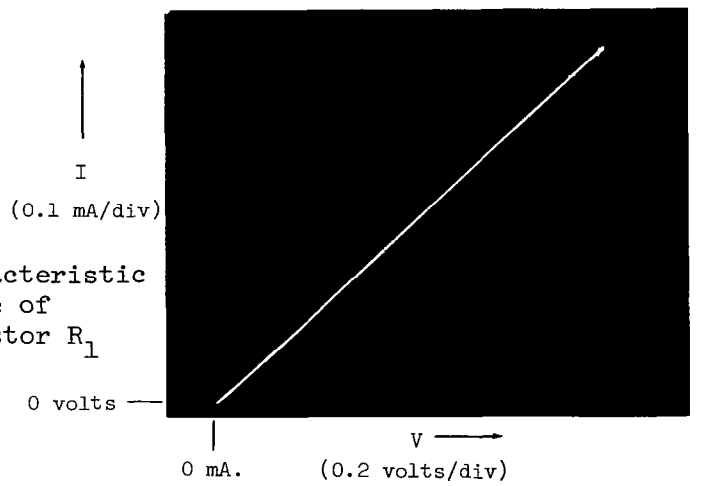



Figure 1-6 Characteristic Curve of Resistor $R_1$

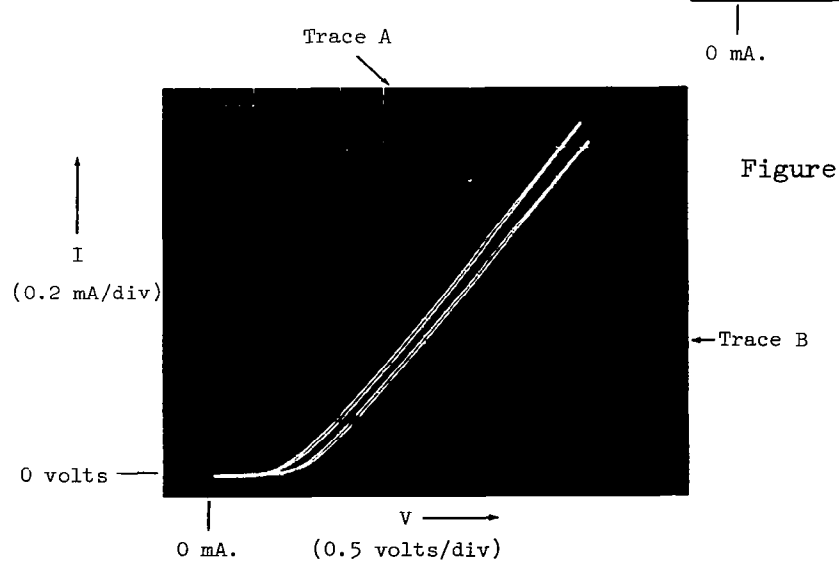



Figure 1-7 Input Characteristics of DTL Integrated Circuit (Trace A) and it Discrete Equivalent (Trace B)

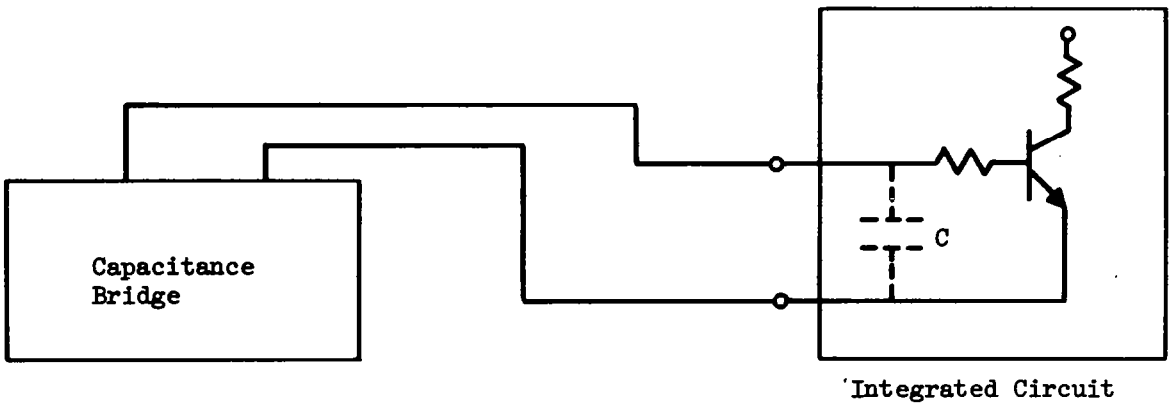



Figure 1-8 Test Configuration to Determine Input Capacitance

1.2.6.4 Detail Parameter Tests - The detail parameter portion of the General Specification requires that all D-C characteristics and dynamic parameters be tested over the temperature range from -55 to +125°C. The temperature range may be modified to include additional test temperatures dependent upon mission requirements. The temperature range may also be reduced if the mission requirements are less stringent.

All parameters must be monitored within specified limits to assure operation over the worst system environments allowing for end life component degradations. Large shifts in these parameters will show marginal devices. A criteria can then be set up using computerized variables analysis to pin down maximum allowable parameter deviations, and to project the reliability of each device type. Such analysis must be performed on a continuing basis, during which the data must be carefully and continuously reviewed, to insure that the test program is providing maximum effectiveness for the lowest possible cost.

1.2.6.5 Dynamic Parameter Tests - It is recommended in the General Specification that all dynamic parameters (including propagation delay time) be measured on a single device, rather than using a "two-stage" measurement. Tests performed during this program indicated that this is the best way to establish actual device performance, since it provides for complete standardization and stabilization of test conditions. With test conditions fixed, variations in performance can then be attributed directly to device variations.

1.2.7 Thermal Cycling

Thermal environmental tests serve the double function of stressing the packaging materials and lead seals, as well as the active device and attachment areas. Temperature cycling should always be performed before a hermetic seal test to derive the maximum benefit from the seal test. Temperature cycling should be directly followed by centrifuge and monitored vibration. This is a desirable sequence since mismatches in the thermal expansion coefficients will weaken the device structure causing failures under mechanical stress. Thus, devices which pass this rigid test sequence can be expected to perform over the full temperature range (-55 to +125°C) regardless of the rate of temperature changes within this range.

1.2.8 Mechanical Tests

1.2.8.1 General - Shock testing was not specified as part of acceptance testing because it is basically a median test lying between centrifuge and vibration. A shock test possesses both a force-frequency spectrum and a high acceleration. However, its acceleration cannot be achieved on a level comparable to that of a centrifuge, nor is the frequency spectrum as comprehensive as that of vibration testing. Thus, shock testing merely presents a

compromise containing weaker versions of the salient features of both centrifuge and vibration tests.

If the objective of screening were absolute economy, then shock would to some degree replace aspects of both tests. However for a high reliability space program where the force and frequency requirements are most stringent, both vibration and centrifuge tests must be used. Incorporation of shock tests in addition to vibration and centrifuge would merely constitute a redundancy and would not improve device reliability. This was substantiated during the study phase of this contract when several manufacturers expressed the viewpoint that "You will not activate a device failure through shock that you can't activate through centrifuge and vibration".

1.2.8.2 Centrifuge - Centrifuge yields the highest available acceleration and therefore permits the greatest probability of screening out incipient failures. Acceleration in the $Y_1$ axis will stress weak areas, since it will tend to lift marginal bonds off the bonding pads and separate a poorly adhered die from the header. Acceleration in the $Y_2$ axis will tend to compress bonding wires against their attachment points and stress unsupported substrates. Furthermore, resolution of $Y_2$ accelerative forces tends to produce a lateral force component which will slide the bond in a direction tangential to the pad.

1.2.8.3 Vibration - Monitored vibration reveals excessive flexibility from overlong leads or unsupported substrates evidencing itself as a modulation in the output signal. It also allows the detection of a number of failures caused by the acceleration tests. These include loosened particles, broken leads and opened or shorted bonds. The variable frequency vibration will cause loose particles or bonding wires to move within the package. Such movement will be evidenced by an electrical pulse in the monitored output signal.

Output voltages should be monitored in accordance with circuit topology and the schematic diagram, with the measuring circuit delineated in the detail specification. All inputs and outputs should be connected to power sources through current limiting resistors. In this way terminal voltages will be free to change as a function of internal shorts or opens. A noise output of 100-mv peak-to-peak or greater shall constitute a failure. This represents an appreciable fraction of the typical noise immunity level and will preclude triggering of the next in-line device by random vibration noise. It is essential that a true peak-to-peak reading instrument be provided since only one pulse may be necessary to overcome the noise margin of succeeding devices.

The frequency spectrum of 10 to 2000 cps was chosen since rocket noises have most of their energy at the low end of this frequency spectrum, while the internal resonances of intergrated circuits have most of their energy at the high end of this spectrum.

### 1.2.9 X-Ray

The conventional approach to X-ray specifications has been to define the equipment, facilities, and procedures rather than to emphasize the rejection criteria. The approach taken under this contract was to standardize the equipment requirements and to detail the specific defects which are detectable. A large number of device types were studied to develop comprehensive rejection criteria which would assure high reliability for space system applications.

It was decided that the 100% X-ray examination must follow the thermal and mechanical environmental tests to screen out any abnormalities caused by these stresses.

### 1.2.10 Burn-in

Burn-in and operating life tests should be directed at the evaluation of device performance levels with operating time as a parameter. Such tests will detect early failures and will allow projection of operating life expectancies for each device type.

A minimum burn-in requirement should consist of operation at the maximum rated temperature, with $V_{CC}$ applied, for at least 168 hours. Experience shows that if temperature voltage inversion is going to occur, it will usually occur within 96 hours and sometimes as much as 1000 hours. Thus 300 hours was chosen as the optimum amount of test time necessary to assure high reliability requirements for screening. One thousand hours was chosen as the test time for the qualification sampling tests to furnish an accurate prediction of device life expectancy. During operation, all devices should be switched "on" and "off" using a 50% duty cycle (square wave) at some nominal frequency in the audio range (1 to 100 KC) so that all components will be stressed at least half the time. The pre and post burn-in variables data requirements are necessary to reveal catastrophic failures, short term degradation and "plague" failures. It is extremely important to analyze all burn-in failures since this testing resembles actual service conditions and the failure modes are similar. Thus, significant reliability information can be obtained.

### 1.2.11 Hermeticity Tests

The hermeticity requirements of the general specification are capable of detecting seal leaks of any magnitude up to $1 \times 10^{-8}$ std cc/sec. To cover the complete range for leak detection, it is necessary to perform the hermeticity tests in three stages. The hot glycerin test should be used for gross leaks in the order of $10^{-5}$ std cc/sec (per MIL-STD-202). The helium leak (or radiflo) test is effective in the range of $10^{-6}$ to $10^{-8}$ std cc/sec.

However, in developing leak test requirements for the Apollo guidance and navigation computer, MIT has reported that "...after a series of correlation tests...it was determined that the standard fine and gross leak tests were insufficient for detecting the entire range of leakers..." For this reason it is essential that the nitrogen bomb test described in the General Specification be employed to cover the mid-range of leak detection.

Leak detection is an indispensable part of high reliability screening of integrated circuits since the most infinitesimal leak (less than $10^{-6}$ std cc/sec) can cause aluminum hydroxide formations resulting in the generation of insidious time dependent failure modes.

It should also be stressed that both fine and gross leak tests should follow any operation that may stress the integrated circuit seals. Such operations as normally performed by the user are lead forming, bending, and shearing.

1.2.12 Final Electrical Tests

At this point, electrical tests similar to those described (Paragraph 1.2.6) are performed again. This permits evaluation of changes in the electrical parameters which might result from the physical stresses applied in preceding tests.

1.2.13 Lot Provisions

As a final acceptance provision it was necessary to define production lot time, inspection lot quantity, and integrated circuit age to assure the timely shipment of required device quantities from approved lots. It was also necessary to specify the requirements for the rework and resubmission of lots, the storage requirements, and the packing and shipping of acceptable integrated circuits. It is important that these provisions be negotiated as soon as possible to allow the earliest approval of a manufacturer as a source for digital integrated circuits.

## 1.3 QUALIFICATION TEST REQUIREMENTS

Extensive qualification requirements must be performed prior to acceptance of the vendor as a source of supply. These are necessary to determine the full capability of the devices, and to highlight any weaknesses in the vendor's design, processing, or materials.

Based on the results of these tests on the initial lot, it may be necessary to incorporate some of these requirements on a sampling basis in addition to the acceptance tests to guard against marginal performance on future lots. Conversely, some of the acceptance test levels (such as monitored vibration) may be relegated to qualification requirements when and if sufficient data is accumulated to indicate significant improvements in device performance. However, since most of the qualification tests are geared towards controlling

basic design limitations of a specific device and are destructive in nature, they will generally be performed on samples from the initial lot only.

Procedures for the qualification tests are generally well defined by military specifications. However, in the case of the weldability requirements and the temperature-altitude tests, it was necessary to define these tests in greater detail as explained in the following paragraphs.

### 1.3.1 Weldability

The results of advanced study programs at Grumman have established the fact that a "use" test is not a practical method of establishing the weldability of integrated circuit leads. The reason for this is that all the elements in the welding operation (the gold plated leads, the printed circuit board pad material, the thickness of the printed circuit board plating, and the welding machine) constitute variables in the operation. Data obtained from one setup, therefore, could not be considered applicable to any other operation.

It is generally agreed upon with the industry that if leads are plated to a minimum of 100 microinches of gold, then they can be considered weldable. The maximum limit of 200 microinches placed on the gold plating thickness is necessary to be consistent with the solderability portion of the specification. Excessive gold plating on leads will cause solder joints of relatively poor peel strength. The upper limit is almost always acceptable to a manufacturer, since it is in keeping with his own economic considerations, in terms of plating schedule and material costs.

### 1.3.2 Temperature-Altitude

All space vehicles must meet comprehensive temperature-altitude requirements. However, this provision is not imposed at the component level, and is not referenced in any component specifications. Thus, it was felt that high reliability integrated circuits for space system applications must undergo these tests at the qualification level. All devices must be designed and controlled with the mission requirements in mind.

The tests chosen for this specification is the Grumman temperature-altitude tests for the Orbiting Astronomical Observatory which have been approved by NASA Goddard Space Flight Center.

## 2.0 NON-DESTRUCTIVE TEST RESULTS

The device investigation covered a cross-section of integrated circuits which are used in the LEM Program for space system applications. The complement of circuits studied is presented in Table 2-1.

It should be pointed out that all devices used for the test portion of this program were procured from local distributors, rather than from the circuit manufacturers. Furthermore, while all circuit types tested during this program are guaranteed for operation over the full temperature range, lot control provisions were not observed in purchasing them. The reason for this choice was the opinion that, while devices available from distributors should be expected to meet their electrical performance requirements, they might still contain latent failure mechanisms.

The results of the program completely justified the above decision. In addition to exhibiting a relatively low potential reliability, these circuits were found to contain many process defects and non-uniformities. However, it must also be stated that these results should in no way reflect on the manufacturer, but rather should show that if high-reliability integrated circuits are desired, they must be purchased to a specification which contains adequate high-reliability provisions.

In accordance with the program test plan, these circuits were initially subjected to a series of non-destructive tests, to evaluate their performance, develop general specification requirements and limits, and provide a basis for sample selection prior to destructive testing.

Tests performed will be described in the following pages. A summary of test methods, results (including photographs), and recommendations for application of these methods to the general integrated circuit screening - acceptance specification are included.

### 2.1 EXTERNAL VISUAL AND MECHANICAL INSPECTION

#### 2.1.1 Description of Equipment

Stereo Microscope (Bausch & Lomb) was the equipment used and included:

- Continuously variable magnification over a 4.3 to 1 range between 3.5 to 200 X
- Vertical illuminator and Nicholas light source
- Polaroid Camera

TABLE 2-1. INTEGRATED CIRCUITS STUDIED UNDER THIS PROGRAM

| Vendor | Series | Type | Function | Qty. |
|---|---|---|---|---|
| Texas Instruments | 51 | SN 5101 | R-S Flip Flop w/Presets | 5 |
| | 51 | SN 5111 | R-S Flip Flop w/Emitter Follower Outputs | 5 |
| | 51 | SN 5112 | R-S Flip Flop | 5 |
| | 51 | SN 512A | Single 6-input NAND/NOR Gate | 5 |
| | 51 | SN 513A | Single 6-input Gate W/Emitter Follower Output | 5 |
| | 51 | SN 514A | Dual 3-input NAND/NOR Gate | 5 |
| | 51 | SN 515A | EXCLUSIVE-OR Network | 5 |
| | 51 | SN 516A | Single input and Dual 2-input NAND/NOR Gates | 5 |
| | 51 | SN 5161 | Triple 2-input NAND/NOR Gate | 5 |
| | 51 | SN 5162 | Triple 2-input Gate w/Emitter Follower Outputs | 5 |
| | 53 | SN 530 | J-K Flip Flop w/Preset | 5 |
| | 53 | SN 531 | Single 5-input NAND/NOR Gate | 5 |
| | 53 | SN 5311 | Dual 5-input NAND/NOR Gate | 5 |
| | 53 | SN 532 | Single 5-input AND/OR Gate | 5 |
| | 53 | SN 533 | Dual 3-input NAND/NOR Gate | 5 |
| | 53 | SN 5331 | Triple 3-input NAND /NOR Gate | 5 |
| | 53 | SN 534 | Dual 2-input and 3-input NAND/NOR Gate | 5 |
| | 53 | SN 535 | Quad Inverter-Driver | 5 |
| | 53 | SN 5360 | Quad 2-Input NAND/NOR Gate | 5 |
| | 53 | SN 5370 | Dual EXCLUSIVE-OR Network | 5 |
| Signetics | SE-DTL | SE 101G | Single 4-input NAND/NOR Gate | 5 |
| | SE-DTL | SE 105G | Single 6-input Diode Expander Array | 5 |
| | SE-DTL | SE 110G | Single 3-input NAND/NOR Driver Gate | 5 |
| | SE-DTL | SE 115G | Dual 2-input NAND/NOR Gate | 5 |
| | SE-DTL | SE 124G | Clocked R-S Flip Flop | 5 |
| | SE-DTL | SE 150G | Single 2-input NAND/NOR Driver Gate | 5 |
| | SE-DTL | CS 700G | Dual 2-input and 3-input NAND/NOR Gate | 5 |
| | SE-DTL | CS 701G | Dual 2-input and 3-input Gate w/pull-up Resistor | 5 |
| | SE-DTL | CS 704G | Clocked R-S Flip Flop | 5 |
| Fairchild | DT,$\mu$L | UX3993051X | Dual 4-input NAND/NOR Gate | 5 |
| | DT,$\mu$L | UX3993251X | Dual 4-input NAND/NOR Driver Gate | 5 |
| | DT,$\mu$L | UX3993351X | Dual 4-input Diode Expander Array | 5 |
| | DT,$\mu$L | UX3994551X | Clocked Flip Flop | 5 |
| | DT,$\mu$L | UX3994651X | Quad 2-input NAND/NOR Gate | 5 |
| | DT,$\mu$L | UX3996251X | Triple 3-input NAND/NOR Gate | 5 |
| Fairchild | RTL | UX5991421X | Dual 2-input NAND/NOR Gate | 5 |
| | RTL | UX5991621X | J-K Flip Flop | 5 |

### 2.1.2 Discussion

Prior to testing, all of the devices procured for this program were examined under high magnification and any deviant or questionable indications were observed. Each circuit was examined at successive magnifications to determine the minimum magnification necessary to uncover the type of defects which are detectable by this method. The continuously variable feature of the stereo microscope was of great benefit in determining this minimum magnification.

A number of photographs were taken to display the areas of interest for subsequent evaluation and comparison. The circuits photographed are rejectable for the basic reason that they indicate process defects and non-uniformity. Furthermore, investigation of each failure soon reveals that these process defects will result in low-reliability situations.

For example, a circuit with external contamination is shown under 5X magnification in Figure 2-1 and under 50X magnification in Figure 2-2. The extraneous wire located on the microcircuit lead could loosen and cause shorting in a finished system. Figure 2-3 shows a glass package which is chipped near the lead seal. This weakening of the seal could cause a loss of hermeticity during future application of the device. A potential catastrophic service failure is shown in Figure 2-4. The extraneous wire on the lead would not have caused electrical test failure, but might short the leads under vibration conditions.

### 2.1.3 Recommendations

In photographing some of the external circuit defects for presentation in this report, it was considered desirable to employ magnifications up to 50X. However, for performing visual examination on an acceptance basis, it was concluded that a minimum of 20X would be sufficient to detect all of the specified conditions. All process defects and deviations observed during the external visual inspections, as well as all other conditions which could logically be expected to impair reliability, were incorporated into the General Specification.

## 2.2 X-RAY VIDICON ANALYSIS

### 2.2.1 Description of Equipment

X-Ray Vidicon System (Picker) including:

- X-Ray Source: 150 KVP, 4 ma, 0.3 mm. beryllium window tube
- TV Chain: 30 mc bandwidth, 1029 line, all solid-state with gamma control

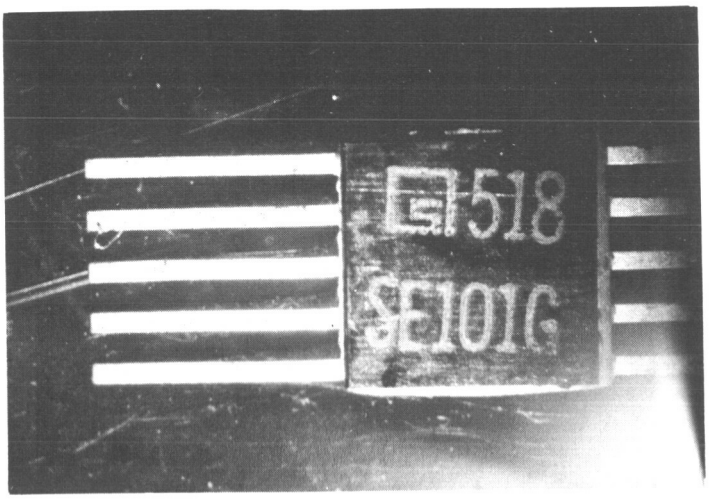



Figure 2-1 External Contamination
Under 5X Magnification

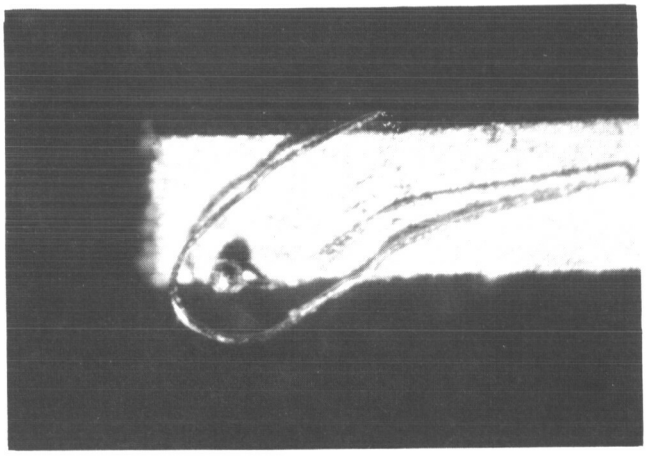


Figure 2-2 Detail View (50X) of Fig. 2-1

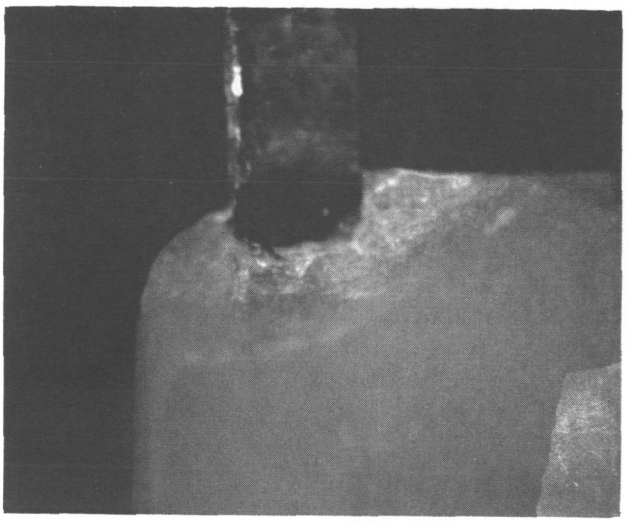


Figure 2-3 Chipped Glass Package

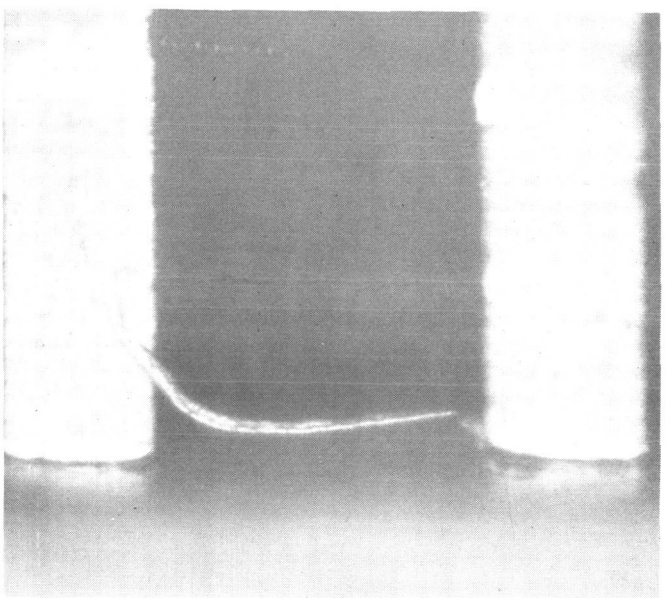


Figure 2-4 External Lead Contamination

- TV Camera Tube: Two types available:
  -Vidicon (presents dynamic view)
  -Intexicon (presents static, integrated view with enhanced resolution and contrast)
- Monitor: 17 inch, 30 mc., 1029 line, with dynamic focus and special high-resolution kinescope (Provides 30X magnification of device)
- Parts Manipulators: 3 types (interchangeable), motorized with remote control from operator's console:
  -Flat tray offers X, Y, Z axis translation and $\pm 15^{\circ}$ tilt
  -Tubular array contains 19 lucite tubes with X, Y, Z axis translation, $360^{\circ}$ rotation about axis of tubes, $\pm 15^{\circ}$ tilt
  Single-device "hand" offers same movement as tubular array
- Camera: 4" x 5" Graflex camera with Polaroid back swings down to record images from screen
- System Resolution: Better than 0.0005 inch

2.2.2 Discussion

A procedure for judging the visual acceptability of any semiconductor or microelectronic device was necessary to screen those units susceptible to failure. A technique capable of non-destructive internal inspection was essential since all such devices are sealed, rendering internal inspection impossible.

Recent advances in X-Ray sensitive vidicon technology have led to the development of television display units capable of magnifying an X-Ray image up to 30 times its size, with a resolution of image detail as small as 0.5 mil. Since the image is continuously visible, the device under examination can be manipulated by servo mechanisms and simultaneously viewed on screen for defects. Because contrast can be electronically enhanced, details that would not be visible if recorded photographically can now be discerned. Furthermore, a permanent record can still be obtained by photographing the image on the screen. Since the technique is nondestructive, it is ideally suited for inspection and evaluation of semiconductors, microcircuits, and small encapsulated

devices and modules. Any loose lands, broken or misplaced leads, small metallic inclusions, loose weld or solder splatters, and other contaminants could be readily detected.

The Picker XRV Vidicon X-Ray System was ideally suited for the magnification of radiographic information for inspection and analysis purposes. Thus, all test devices were subjected to an X-Ray Vidicon analysis. Defects due to the following were detected:

- Misbranded covers (upside-down marking)
- Offset covers
- Voids in the die to case adhesive
- Foreign material in the package
- Loose weld splatters
- Excess gold from gold preforms
- Weld particles on wires
- Double bonds on the leads and substrate pads
- Bonds near the edge of bonding pads and leads
- Excess slack in the bonding wires
- Excess wire at bond terminations (pigtails)
- Fine wires (0.0005 inch) plated on the external leads
- Process non-uniformities

The TV readout of all devices which deviated from the group or which showed questionable indications was photographed. The photographs were then examined and the effects of deviant indications on device reliability were assessed. When clarification or confirmation of the indications was necessary or desirable, the devices were decapsulated and microscopically examined.

The information thus gathered was assembled into the X-Ray portion of the General Specification. Figures 2-5 through 2-19 show X-Ray Vidicon photographs of some of the deviant devices and give explanations or references to the specific area of the General Specification which are violated.

The devices shown in Figures 2-20, 2-21, and 2-22 are of the same type number. They exhibit process non-uniformities in their bonding wire patterns and their package configurations. The packages were originally intended to have 14 leads and were modified in two different ways to yield 10 lead equivalency.

TO-5 devices accounted for 5% of the test lot, and no x-ray defects were discovered for this package configuration. The internal construction is clearly visible in Figures 2-23 and 24. The lack of deviant indications for TO-5 devices is assumed to be a result of the small size of the test lot. It should not be inferred that TO-5 construction is superior to flat-pack construction or that x-ray is inapplicable to TO-5 devices.

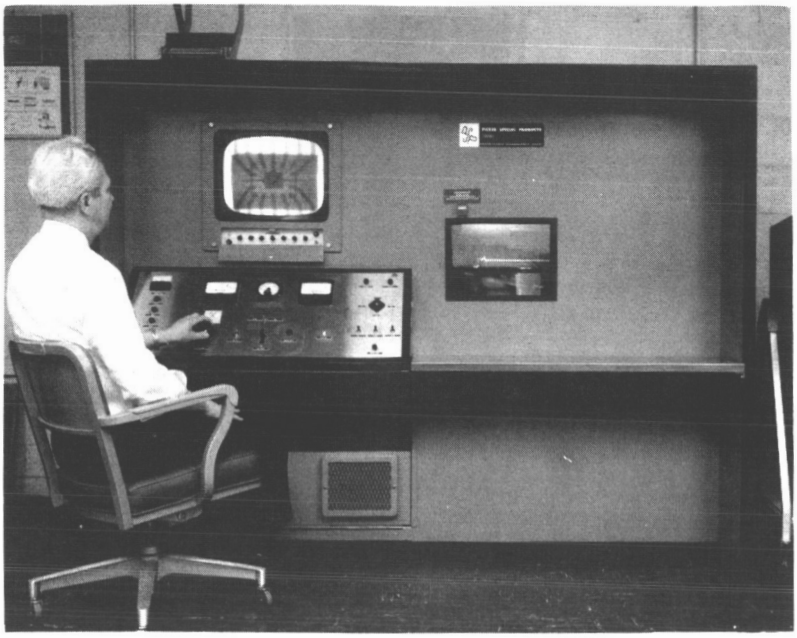


Figure 2-5 Picker X-Ray Vidicon System

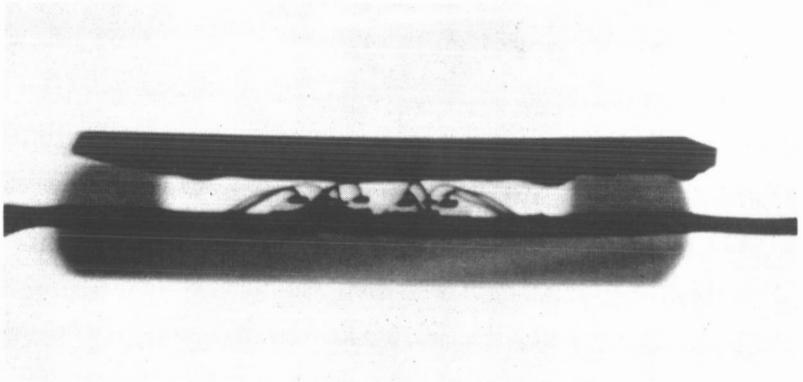


Figure 2-6 Inadequate Clearance Between Bonding Wires and Top of Case (Violates Section 6.10.2.q of General Specification)

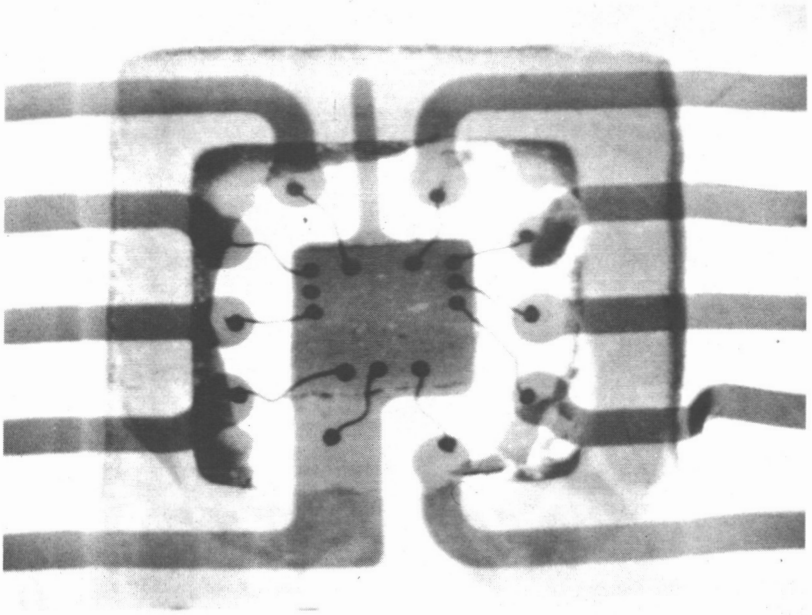


Figure 2-7 Misplaced Bond on Die (Violates Section 6.10.2.m of General Specification)

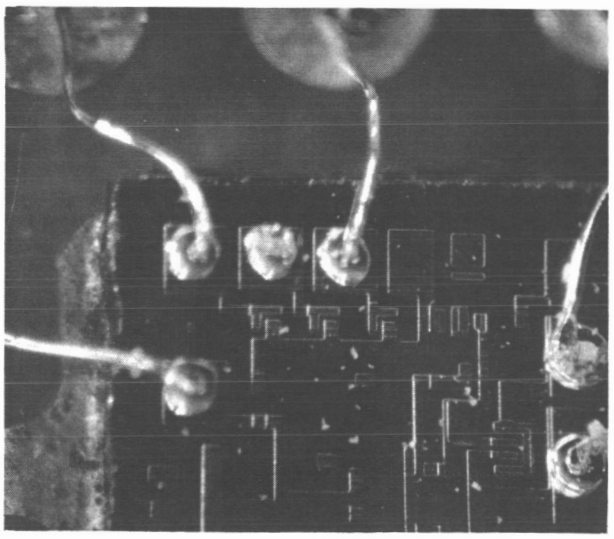


Figure 2-8 Optical Confirmation of Misplaced Bond in Figure 2-7

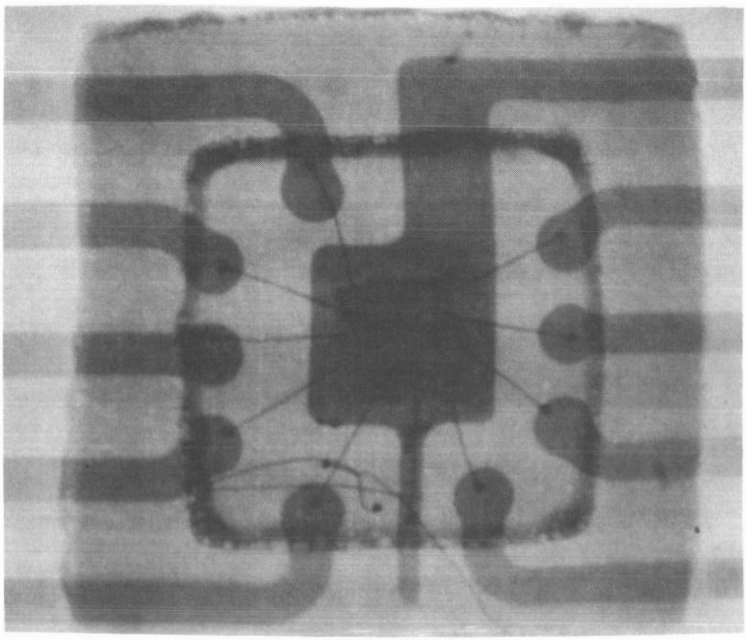


Figure 2-9 Extraneous Encapsulated Material (Violates Section 6.10.2.f of General Specification)

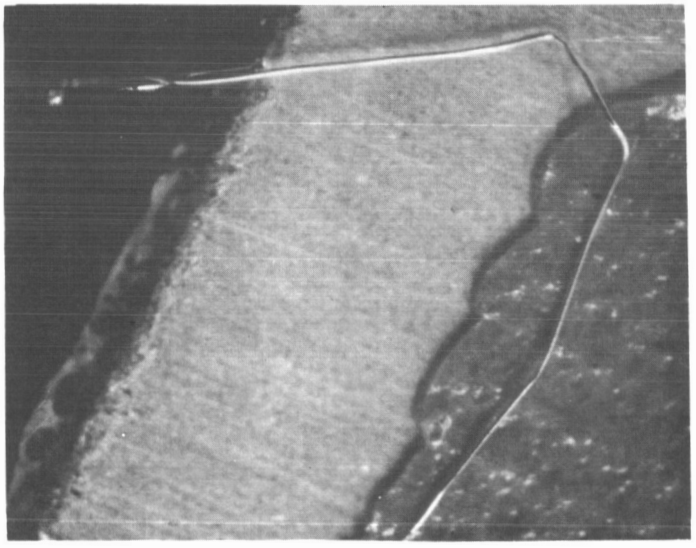


Figure 2-10 Optical Confirmation of Figure 2-9 (Extraneous Gold Wire Was Located Within Case and Between Lid and Case Body)

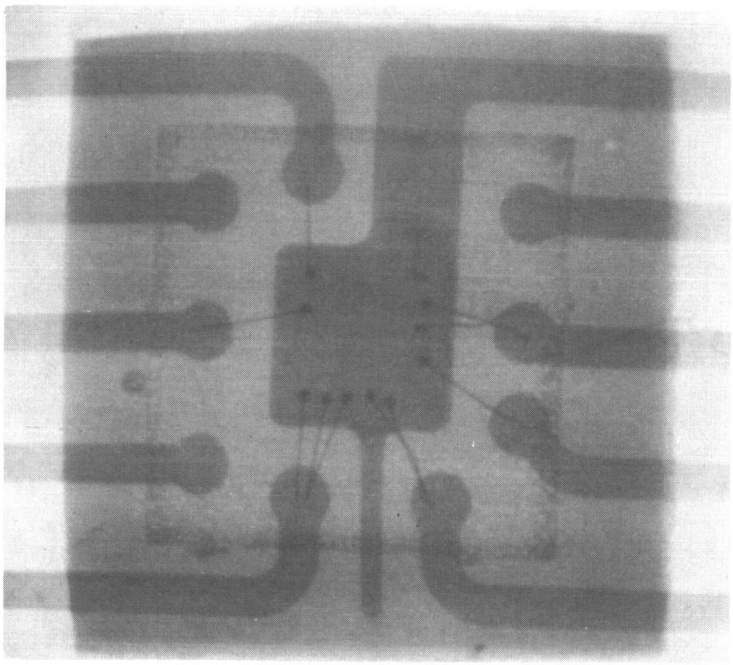


Figure 2-11 Bond Near Edge of Lead; Extra Wire; Contamination on External Lead. (Violates Sections 6.10.2.e, 6.10.2.o and 6.10.2.v of General Specification.

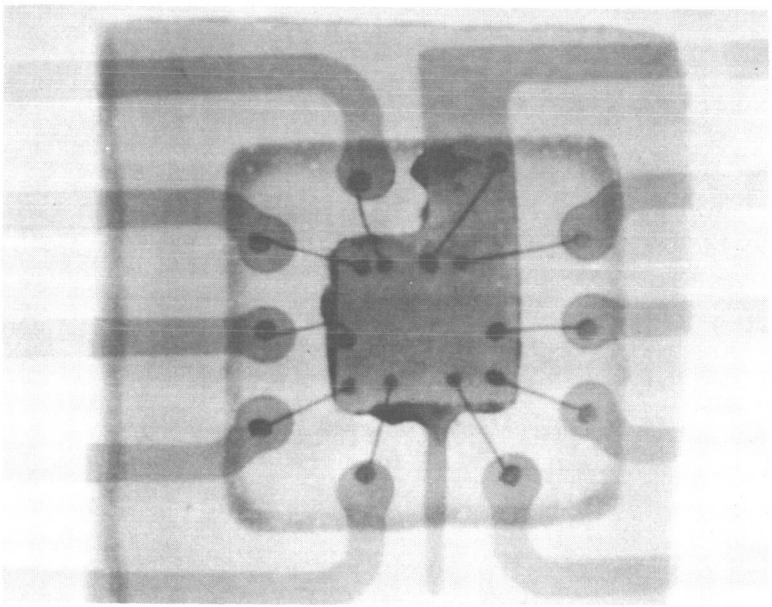


Figure 2-12 Excessive Build-Up of Gold Preform (Violates Section 6.10.2.i of the General Specification.

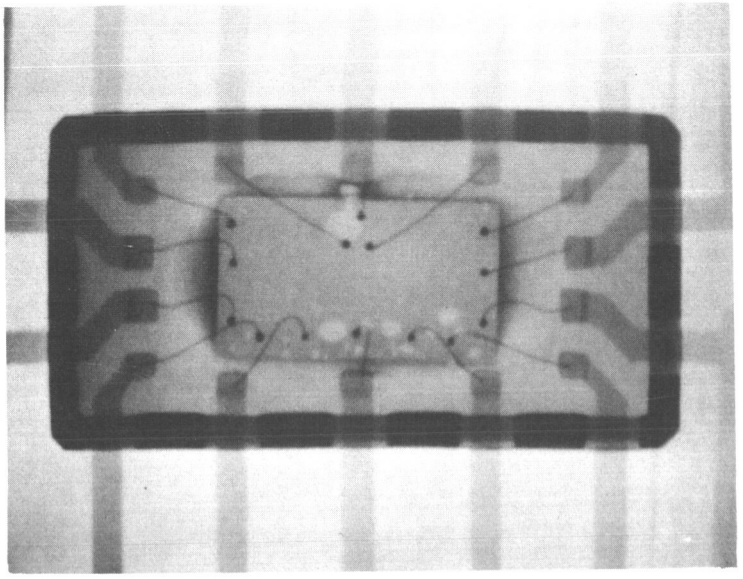


Figure 2-13 Excessively Long Bonding Wires are Capable of Shorting to Each Other, (Violates Section 6.10.2.r of the General Specification.

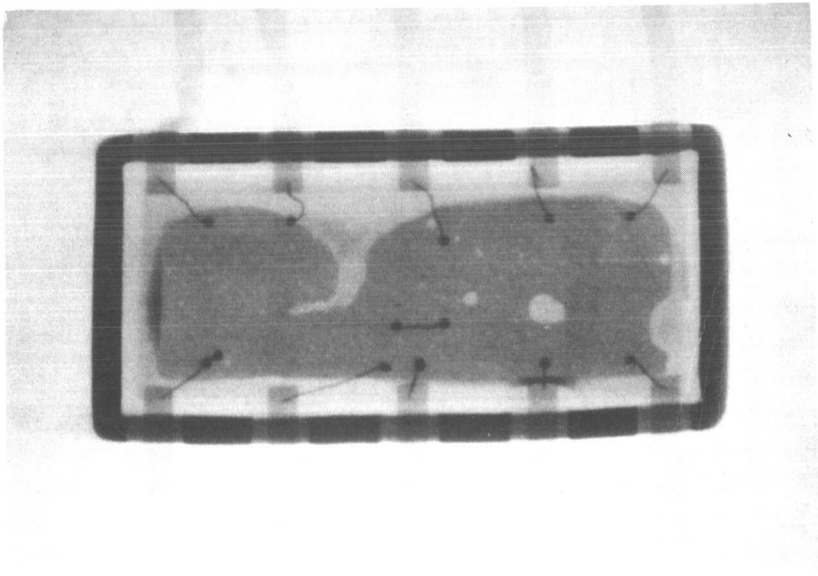


Figure 2-14 Double Bond on Substrate Pad and Extra Wire. (Violates Sections 6.10.2.n and 6.10.2.v of the General Specification)

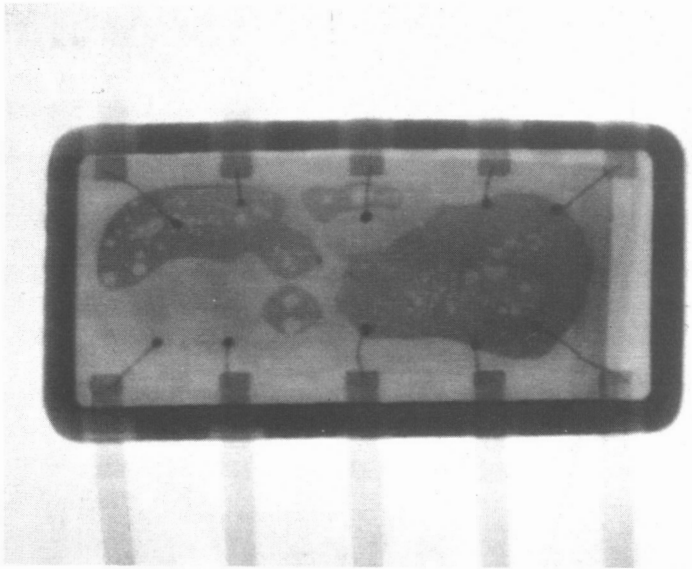


Figure 2-15 Voids in the Die-to-Case Adhesive Extending Over the Entire Substrate Width and Process Non-Uniformities When Compared to Figure 2-17, Which is of the Same Type Number. (Violates Sections 6.10.2.j and 6.10.2.y of the General Specification)

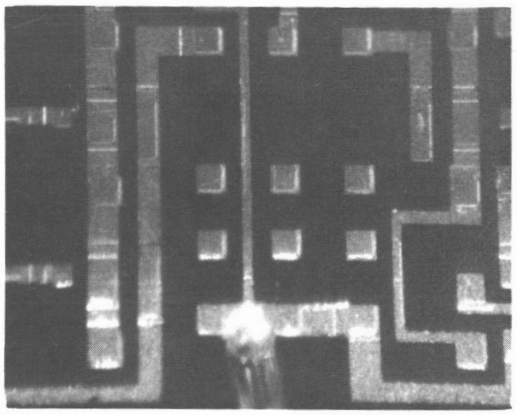


Figure 2-16 Optical Confirmation of Figure 2-15.

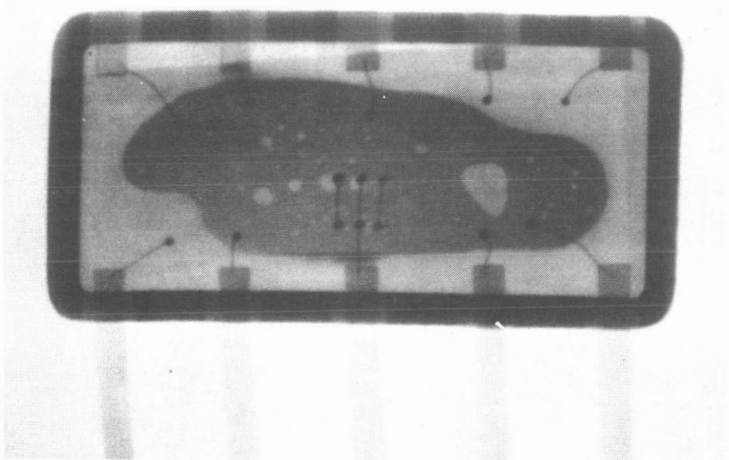


Figure 2-17 Extra Wires, Pigtail, and Process Non-Uniformity When Compared to Figure 2-15 (Violates Sections 6.10.2.u, 6.10.2.v and 6.10.2.y of the General Specification.

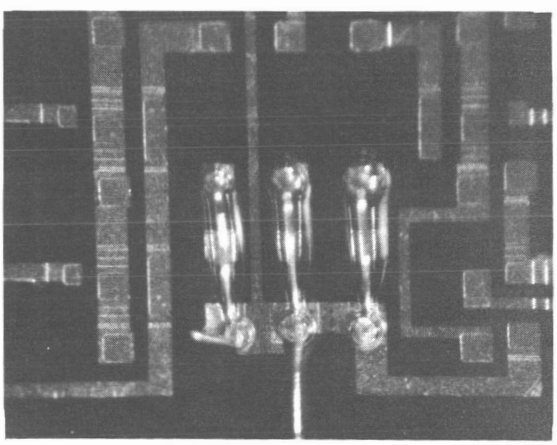


Figure 2-18 Optical Confirmation of Figure 2-17 Showing Extra (Resistance Trimming) Wires and Pigtail.

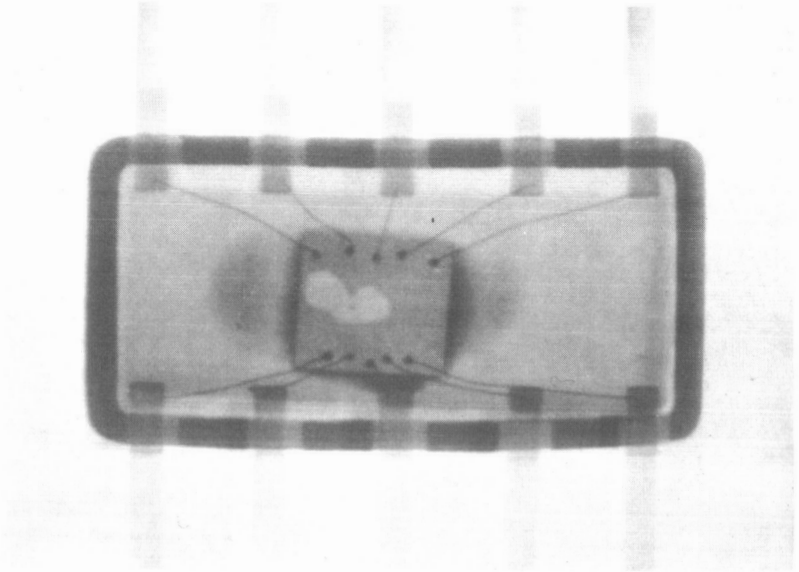


Figure 2-19 Excessively Long Bonding Wires Capable of Shorting to Leads (Violates Section 6.10.2.r of General Specification)

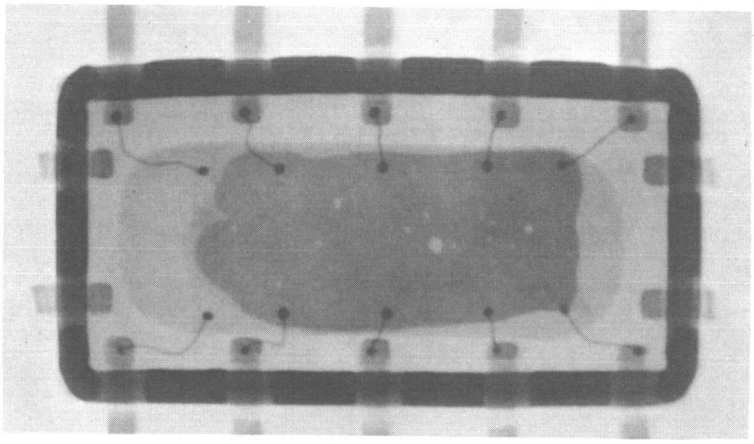


Figure 2-20 Process Non-Uniformity and Excessive Void in the Die-to-Case Adhesive (Violates Sections 6.10.2.j and 6.10.2.y of General Specification)

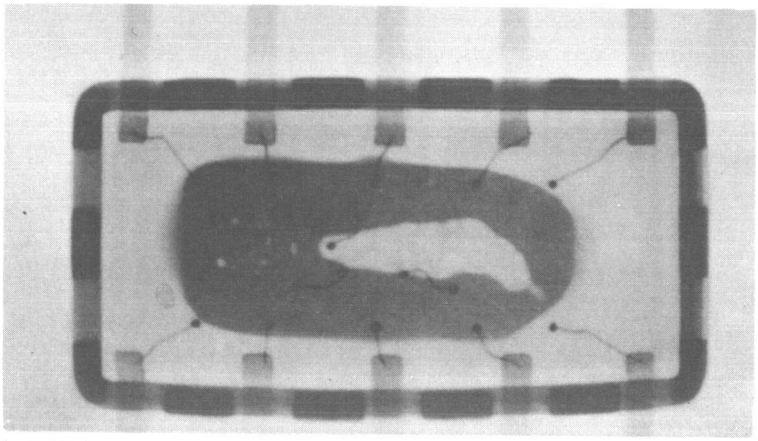


Figure 2-21 Process Non-Uniformity and Extra Bonding Wires (Violates Sections 6.10.2.v and 6.10.2.y of General Specification)

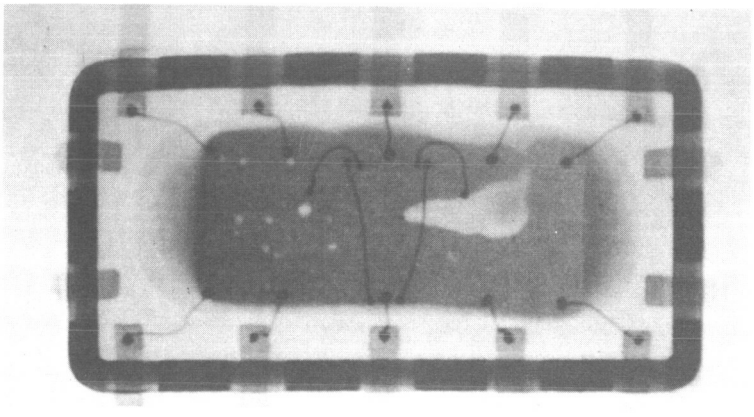


Figure 2-22 Process Non-Uniformity and Extra Bonding Wires (Violates Sections 6.10.2.v and 6.10.2.y of General Specification)

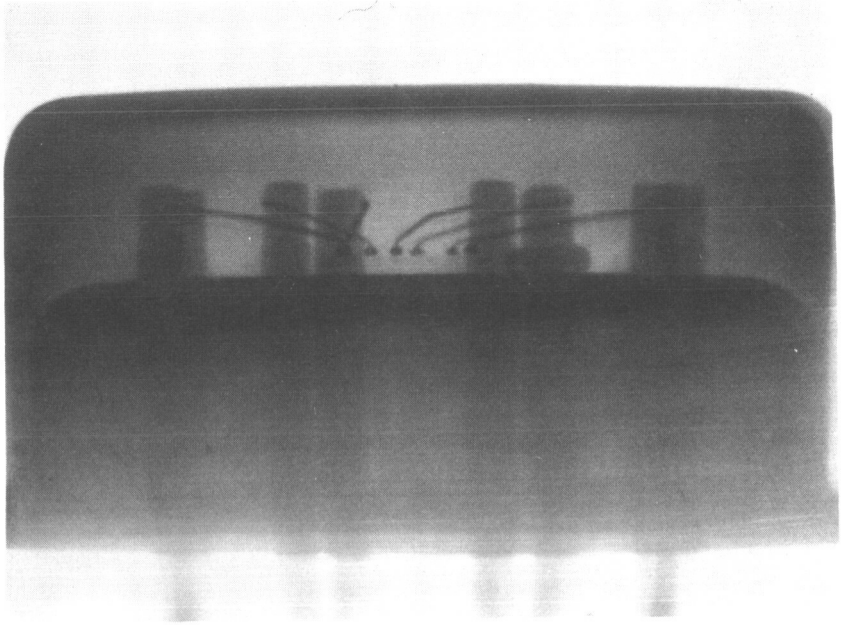


Figure 2-23 Radial View of TO-5 Package

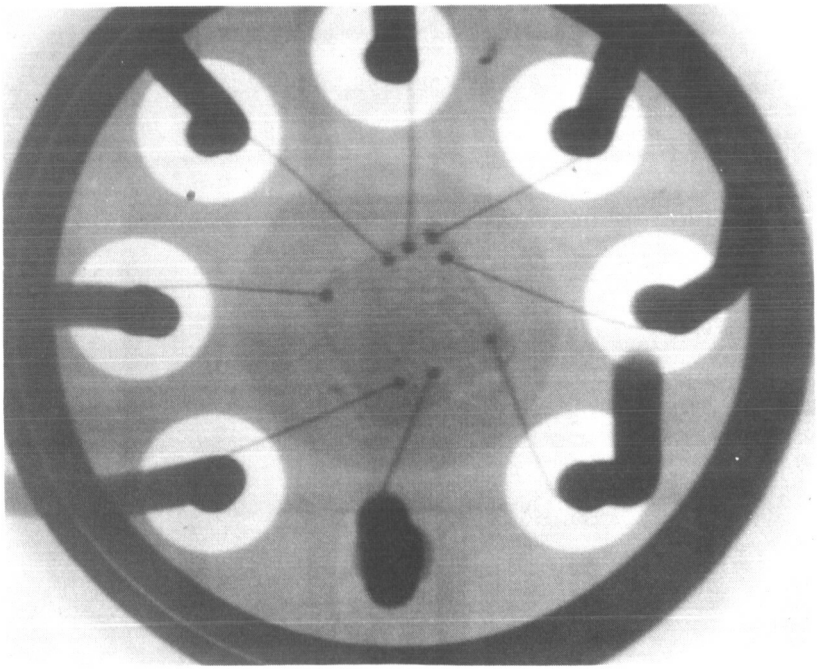


Figure 2-24 Axial View of TO-5 Package Showing Visible Substrate

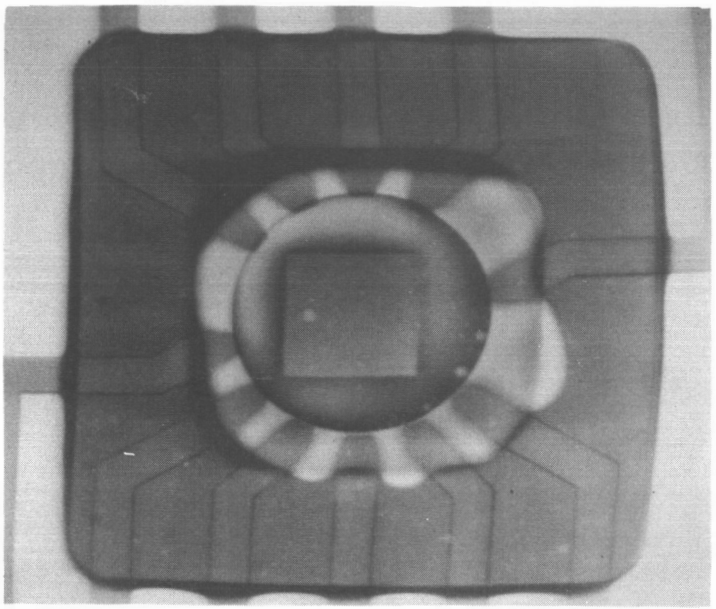


Figure 2-25 Fairchild Flat-Pack (Aluminum Bonding Wires are not Visible, Although the Substrate can be Seen)

Some microelectronic devices utilize aluminum bonding wires. Since the aluminum bonding wires have a very low density-thickness product, it was expected that such bonding wires would not be visible through the much denser case materials. Examination of the Fairchild flat-packs, which use aluminum wires, confirmed this expectation (Figure 2-25).

2.2.3 Recommendations

Devices can be tested to all 25 X-Ray requirements of the General Specification in a test time of several seconds per device. The wide range of low-reliability situations which can be detected in this test time makes X-Ray Vidicon analysis a highly valuable screening technique. Although its usefulness is impaired on devices utilizing aluminum bonding wires, it can still detect a wide range of non-bonding-wire defects and is sufficiently useful to warrant application to such devices.

For these reasons, X-Ray Vidicon analysis is specified on a 100% basis for all microelectronic devices.

## 2.3 ELECTRICAL PARAMETER TESTS

### 2.3.1 No-Load Functional Tests

2.3.1.1 Description of Equipment - Equipment used included:

- Dual-trace oscilloscope (Tektronix 545B with CA plug-in)
- Pulse Generator (Texas Instruments 6613)
- Power supplies (2), (Trygon HR-40-750)
- Oscilloscope Camera (Optional), (Hewlett-Packard 196A)
- Test Fixtures (AUGAT 8075 & 8117 Series)

2.3.1.2 Discussion - The basic function of any logic element is to provide discrete output voltage levels under specified input conditions. Unless the device fulfills this function, other performance and reliability considerations are meaningless. In addition to identifying circuits which do not adequately fulfill their logic function, this test readily verifies circuit type and terminal orientation, as well as providing a gross indication of room temperature noise immunity.

All devices procured for this program were functionally tested. This test is performed by introducing a linear ramp voltage into each input terminal, and observing the input-output transfer characteristic on a dual-trace oscilloscope.

Test equipment was connected as shown in Figure 2-26. The pulse generator was adjusted to provide a linear voltage ramp to each device input. When the ramp voltage is equal to the device's input switching level, the device output will change states. Since both the input and output are displayed on a single screen, the input voltage at which switching occurs is readily observable. In addition, the "1" and "0" output voltages can be read directly from the screen. An example of a gate's transfer characteristic is shown in Figure 2-27, while a diode's transfer characteristic is shown in Figure 2-28 and a flip-flop's transfer characteristic is shown in Figure 2-29.

2.3.1.3 Recommendations - No-Load Functional Testing will reveal whether a circuit is adequately performing its intended logic function, and will effect economy by readily identifying catastrophic failures, thereby eliminating the necessity for further testing of these devices. Two such catastrophic failures were found on test devices for this program. Subsequent failure analysis pinpointed the causes of failure as an open bond in one case and shorted bonding wires in the second case. For these reasons, it is recommended that functional testing be incorporated as part of future test programs and failure verification.

2.3.2 D-C Parameter and Noise Immunity Tests

2.3.2.1 Description of Equipment - Equipment used included:

- Pulse Generator (Texas Instruments 6613)
- Power Supplies (4), (Trygon HR-40-750)
- Temperature Chamber, (Statham SD-8 chamber modified to provide 24 test positions), Temperature Range: -73 to +273$^{o}$C
- Digital Voltmeter (Hewlett Packard 405 BR)
- Automatic Noise Immunity Test Set (Grumman designed equipment for automatic direct read-out of logic levels, threshold voltages and noise margins)
- Test Fixtures (Augat 8075 and 8076 Series)

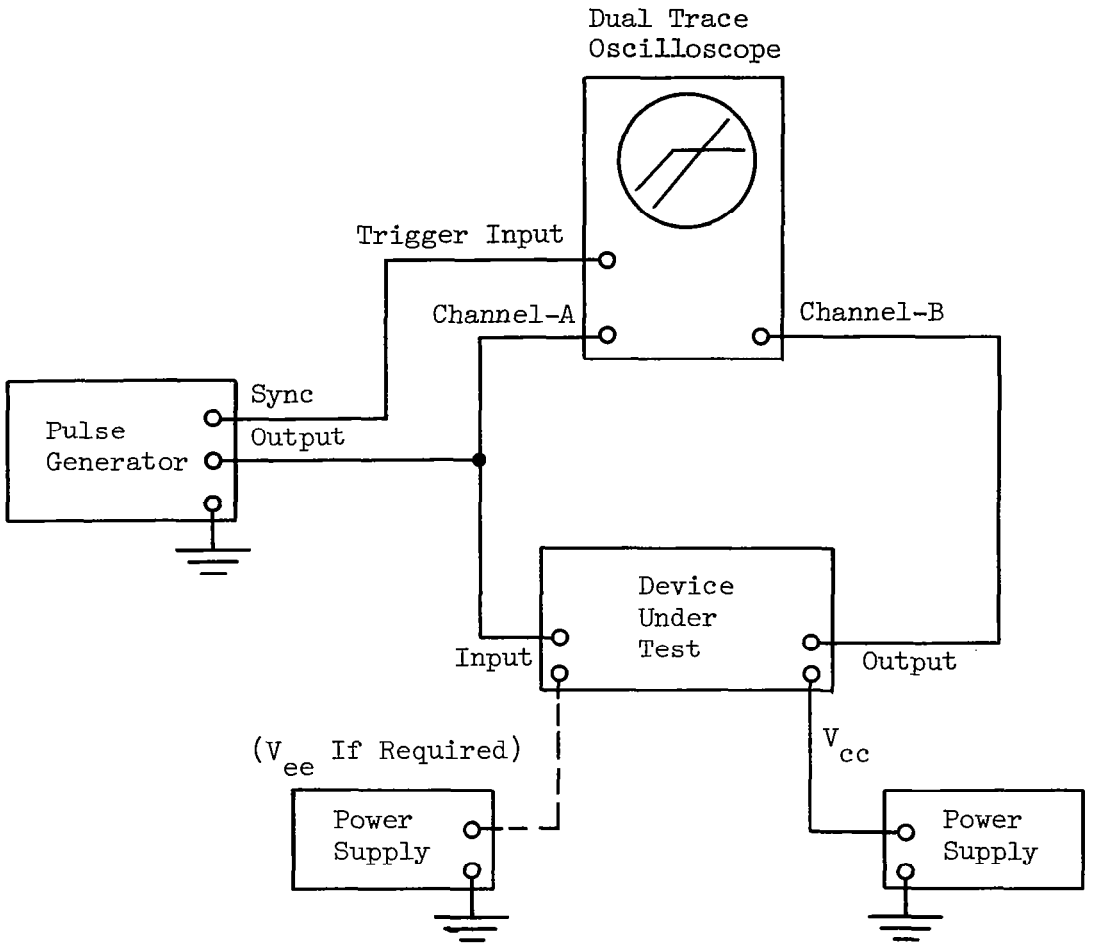



Figure 2-26 Functional Test Equipment Set-Up

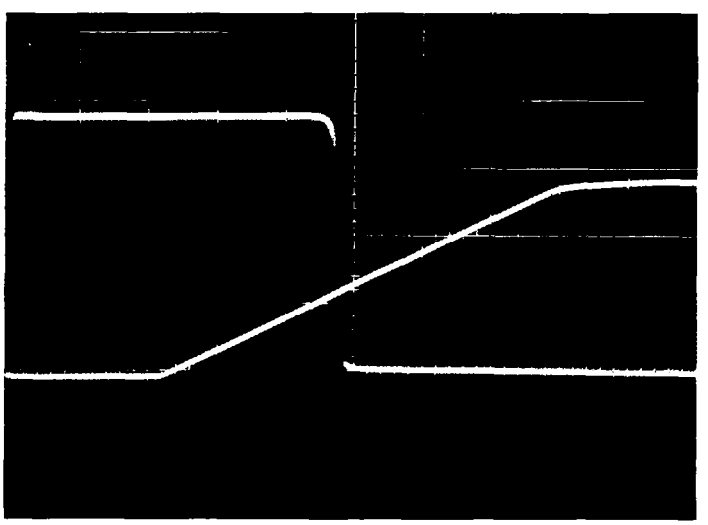


Figure 2-27 Gate Transfer Characteristic

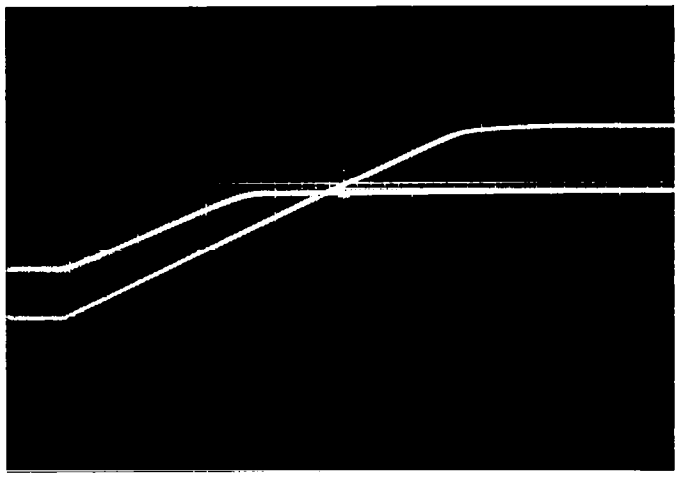


Figure 2-28 Diode Transfer Characteristic

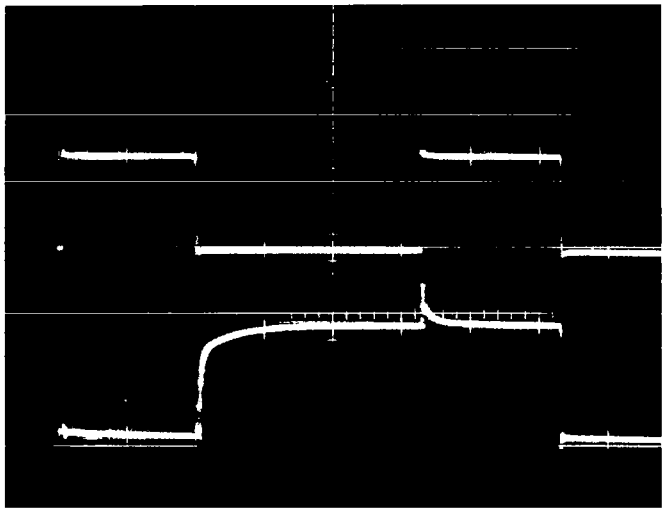


Figure 2-29 Flip-Flop Transfer Characteristic

2.3.2.2 Discussion - In a digital system, spurious pulses which are coupled into a circuit via the ground, signal, or supply voltage lines can result in false triggering of the affected circuit and the generation of false bits. It has also been shown that the value of noise voltage which will produce a change of state in a given circuit decreases as the pulse width increases. A D-C test for noise margin will therefore yield values indicative of the minimum, or worst-case, value for this parameter. D-C noise immunity testing is also necessary for the purpose of evaluating the logic levels and threshold voltages of a given device. Furthermore, by adjusting the loading, temperature, and supply voltages to simulate worst-case operating conditions, a complete description of the expected performance of the device under actual operating conditions can be established. D-C voltage levels and noise margins were measured on all digital logic gate circuits procured for this program. These circuits were tested at +25, -55, and +125°C under worst case loading conditions. These conditions had been established from either the manufacturer's data sheets, or from evaluations previously performed on samples of these devices. The noise immunity test set-up is shown in Figure 2-30.

The six readings taken for each device are: HNM, LNM, $V_{oh}$, $V_{ih}$, $V_{ol}$, $V_{il}$. These parameters were recorded directly from the Automatic Noise Immunity Tester. Definitions for these voltages are those indicated in the General Specification. These are described in the following sketches in detail.

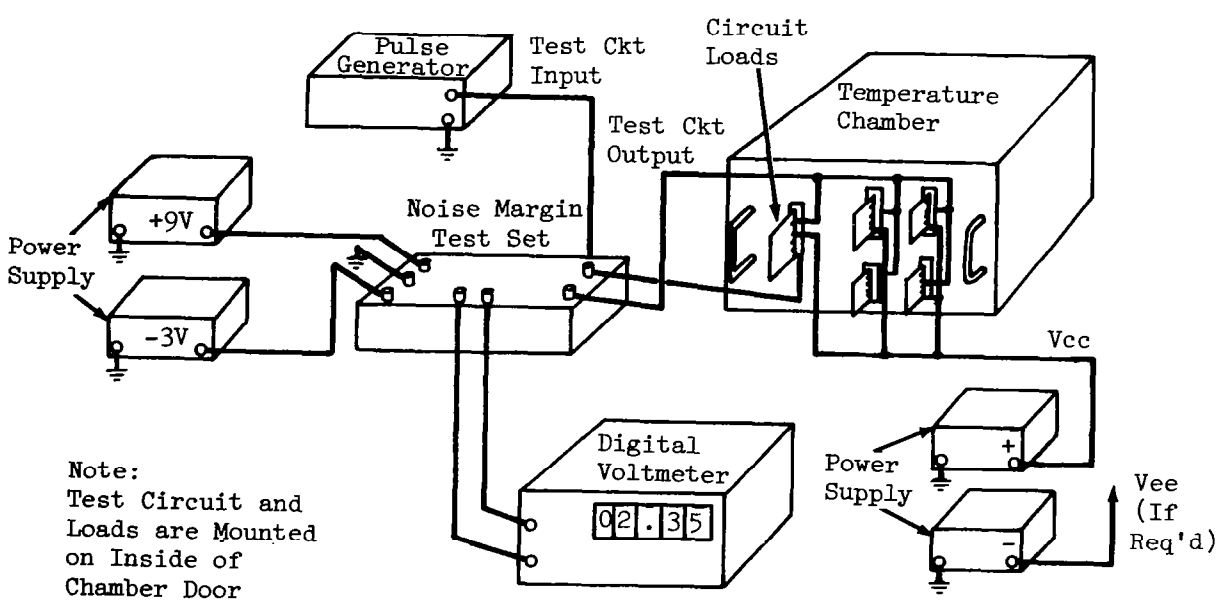
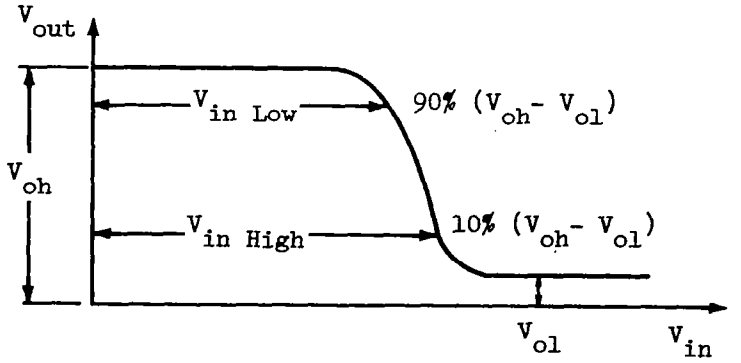



Figure 2-30 Noise Immunity Test Set-Up

- For an Inverting Gate:




$V_{oh}$ = Output voltage level for 0 input

$V_{ol}$ = Output voltage level for 1 input

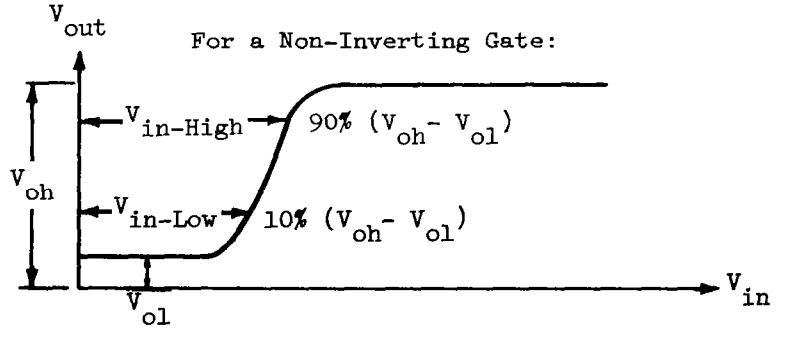
$V_{il}$ = Input threshold voltage required to drive output to its 90% voltage amplitude value

$V_{ih}$ = Input threshold voltage required to drive output to its 10% voltage amplitude value

HNM = High level D-C noise margin = $V_{oh} - V_{ih}$

LNM = Low level D-C noise margin = $V_{il} - V_{ol}$

- For an Non-Inverting Gate:




$V_{oh}$ = Output voltage level for a 1 input

$V_{ol}$ = Output voltage for a 0 input

$V_{il}$ = Input threshold voltage required to drive output to its 10% voltage amplitude value

$V_{ih}$ = Input threshold voltage required to drive output to its 90% voltage amplitude value

HNM = High level D-C noise margin = $V_{oh} - V_{ih}$

LNM = Low level D-C noise margin = $V_{il} - V_{ol}$

D-C voltage levels and noise margins were also measured at room temperature following burn-in. Computerized variables analysis was then employed to derive the expected standard deviations, and to develop performance limits to be used in specifying future burn-in and variables data requirements for these devices.

2.3.2.3 Recommendations - D-C voltage levels and noise margins are essential measurements of device performance and have been incorporated as basic requirements in the General Specification. Data generated for these parameters can also be used as an indicator in selecting devices for internal visual inspection (destructive testing), rather than sampling on a purely random basis.

2.3.3 Dynamic Parameter Tests

2.3.3.1 Description of Equipment - Equipment used includes:

- Digital Read-Out Sampling Oscilloscope (Tektronix 567 with 6RIA Digital Unit and 3S76, 3T77 Plug-In Units; and Tektronix 262 Dynamic Programmer)
- Power Supplies (Trygon HR-40-750)
- Pulse Generator (Texas Instruments 6613)
- Test fixtures (Augat 8075 and 8117 series)
- Camera (Hewlett-Packard 196A)
- Diode switching time tester (Tektronix 291)
- Pulse Generator (Tektronix Model 109)
- Temperature Chamber (Statham SD-8 Chamber, modified to provide 24 test positions).

2.3.3.2 Discussion - Dynamic parameters of integrated circuits are rarely guaranteed at conditions other than those of room temperature and optimum loading. However, it it essential to the designer of high-reliability space equipment that the worst-case temperature and loading conditions be tested and guaranteed if the system is to perform reliably to the actual timing requirements.

Complete dynamic parameter measurements were made for all digital integrated circuits procured for this program. This testing for the diode arrays was limited to measuring reverse recovery time for each diode in the array. All the circuits were tested at -55, +25, and +125°C for their dynamic parameters in accordance with the definitions of MIL-S-19500D. These tests included: delay time ($t_d$), rise time ($t_r$), storage time ($t_s$), and fall time ($t_f$).

Propagation delay time ($t_{pd}$) was also measured under worst-case temperature and loading conditions. This parameter is defined as the average of the turn-on delay time ($t_1$), measured from 50% of the input leading edge to 50% of the output leading edge, and the turn-off delay time ($t_2$), measured from 50% of the input trailing edge to 50% of the output trailing edge. Thus $t_{pd} = (t_1+t_2)/2$. Figure 2-31 shows a diagram of the dynamic parameter test set-up and Figure 2-32 shows the dynamic parameter definitions.

To obtain an input pulse which will be representative of the voltage waveform seen by the circuits during operation, it is preferable to specify accurately controlled ramps (from pulse generators which are repeatable) as inputs to the microcircuit under tests, rather than driving the test circuit from another of the same logic family. In this manner, the requirements for fixed test conditions will be met.

The data on all dynamic parameter measurements were recorded for all of the circuits and are included in the Appendix A.

2.3.3.3 Recommendation - Data obtained during this program show that readings for the same dynamic parameter tend to group very closely for devices of the same type. This confirmed anticipated results and indicates that it will generally be possible to perform dynamic parameter testing on a sample basis at the indicated conditions. However, it is doubtful whether it will be possible to predict high- and low-temperature performance from data obtained at room temperature. For this reason it should be re-stated that dynamic parameters must be measured and guaranteed under worst-case loading and temperature conditions. These measurements are essential to insure that systems employing these circuits will meet their timing requirements under actual operating conditions.

## 2.4 BURN-IN WITH VARIABLES DATA

### 2.4.1 Description of Equipment

Equipment used included:

- High Temperature - Low Temperature Test Chamber (Associated Testing Laboratories, Inc., Model 3-LH-20-LC)
- Oscilloscope (Tektronix, Model 545A)
- D-C Power Supply (Lambda, Model LH-121-FM)
- D-C Power Supply (Kepco Inc., Model ABC 10-075)

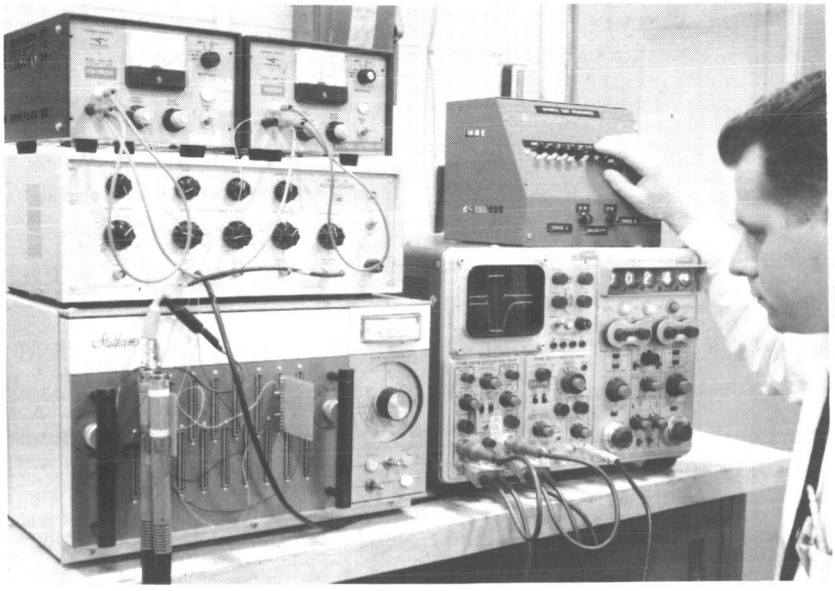


Figure 2-31 Dynamic Parameter Test Set-Up

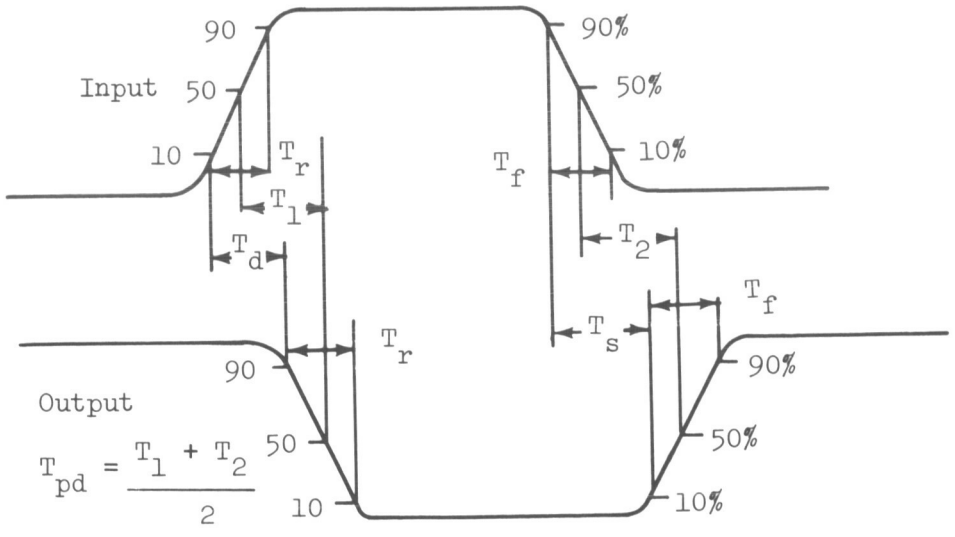



Figure 2-32 Dynamic Parameter Definitions

## 2.4.2 Discussion

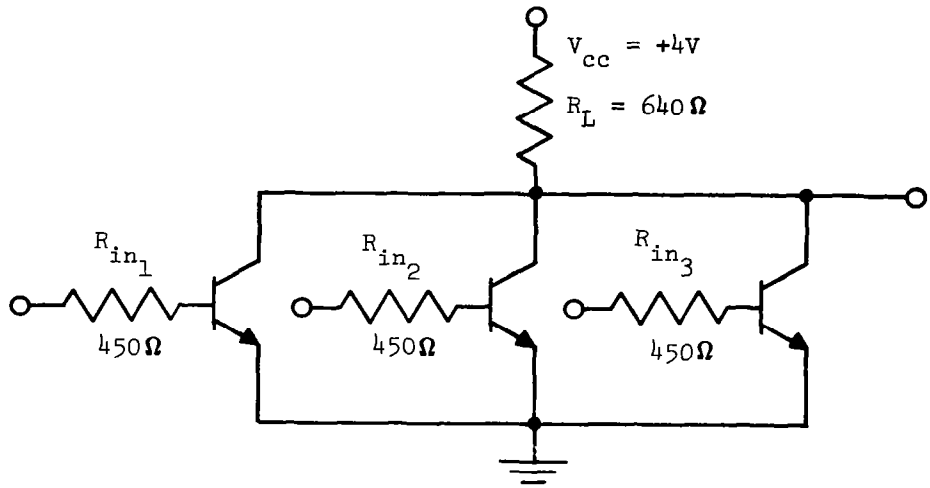
All the circuits were subjected to a burn-in test in accordance with the program plan. Figure 2-33 shows the burn-in set up. The circuits were sealed in a temperature chamber and allowed to stabilize at a temperature of $+125^{o}C$ which was then maintained for a period of 168 hours. The circuits were operated with 4 volts DC being applied between those pins designated as $V_{cc}$ and the ground pins, and 3 volts DC being applied between the input and ground pins. Table 2-2 identifies all circuits and pin connections used for this test. At the completion of the 168 hour period, the circuits were removed from the chamber and allowed to stabilize before proceeding with the post burn-in electrical tests.

Figure 2-33 Burn-In Set-Up

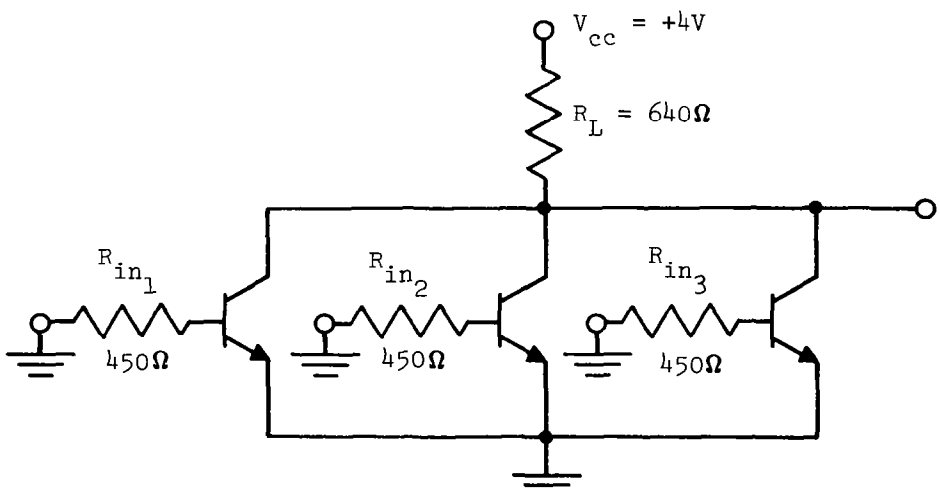
TABLE 2-2. IDENTIFICATION OF CIRCUITS AND PIN CONNECTIONS

| Circuit Type No. | Circuit Serial No. | $V_{cc}$ | Ground | Pin Designations Inputs |
|---|---|---|---|---|
| SN 5311 | 1 - 5 | 11 | 4 | 1, 2, 3, 5, 6, 7, 8, 10, 12, 14 |
| SN 5360 | 6 - 10 | 11 | 4 | 1, 3, 5, 7, 9, 10, 12, 13 |
| SN 535 | 11 - 15 | 3 | 8 | 6, 7, 9, 10 |
| SN 5370 | 16 - 20 | 11 | 4 | 1, 2, 3, 5, 8, 9, 10, 12 |
| SN 5331 | 21 - 25 | 11 | 4 | 2, 3, 5, 7, 8, 10, 12, 13, 14 |
| SN 531 | 26 - 29 | 3 | 8 | 2, 4, 5, 9, 10 |
| SN 533 | 30 - 34 | 3 | 8 | 2, 4, 6, 7, 9, 10 |
| SN 512 | 35 - 39 | 3 | 7 | 1, 2, 4, 5, 6, 10 |
| SN 513 | 40 - 44 | 3 | 7 | 1, 2, 4, 5, 6, 10 |
| SN 514 | 45 - 49 | 3 | 7 | 1, 2, 4, 5, 6, 10 |
| SN 515 | 50 - 54 | 3 | 7 | 1, 2, 4, 5 |
| SN 516 | 55 - 59 | 3 | 7 | 1, 6, 5, 9, 10 |
| SN 5161 | 60 - 64 | 11 | 3 | 13, 14, 6, 9, 1, 5 |
| SN 5162 | 65 - 69 | 11 | 3 | 13, 14, 6, 9, 1, 5 |
| SE 101G | 71 - 75 | 6 | 1 | 7, 8, 9, 10 (In addition Pins 3 and 4 were connected) |
| SE 110G | 76 - 80 | 6 | 1 | 7, 8, 9, (In addition Pin 3 was connected to Pin 6 through a 2 kilohm resistor) |
| SE 115G | 81 - 85 | 6 | 1 | 3, 4, 7, 8 (In addition Pins 2 and 9 were connected; Pin 10 was connected to Pin 6 through a 2 kilohm resistor) |
| SE 150G | 86 - 90 | 6 | 1 | 8, 10 (In addition Pins 3 and 4 were connected) |
| CS 700G | 91 - 95 | 6 | 1 | 3, 4, 7, 8, 9, (In addition Pins 2 and 10 were were each connected to Pin 6 through a 2 kilohm resistor) |
| CS 701G | 96 - 100 | 6 | 1 | 3, 4, 7, 8, 9 |
| DT µL 962 | 101 - 105 | 14 | 7 | 1, 2, 3, 4, 5, 9, 10, 11, 13 |
| DT µL 946 | 106 - 110 | 14 | 7 | 1, 2, 4, 5, 9, 10, 12, 13 |
| DT µL 932 | 111 - 115 | 14 | 7 | 1, 2, 4, 5, 9, 10, 12, 13 |
| DT µL 930 | 116 - 120 | 14 | 7 | 1, 2, 4, 5, 9, 10, 12, 13 |

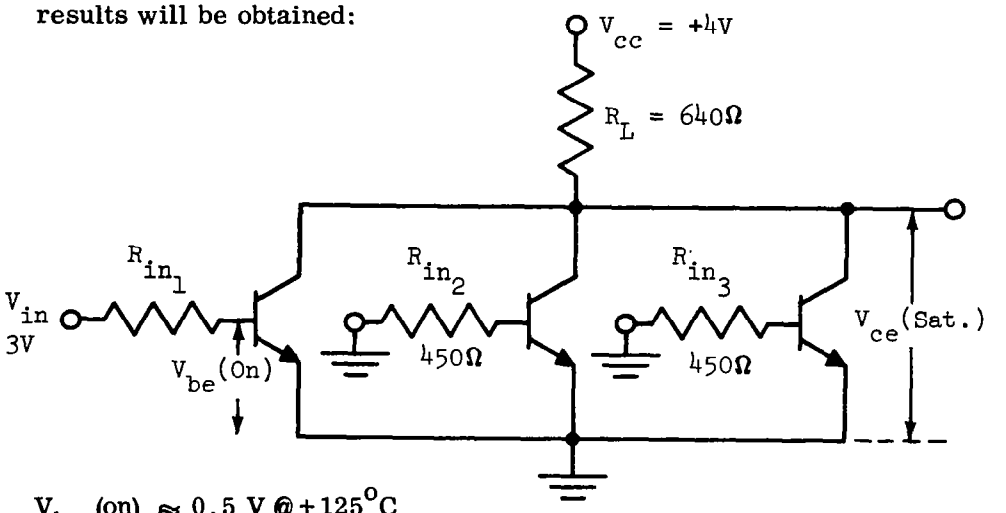
In the selection of operating conditions for the burn-in test, it was established that a unique condition of worst-case power dissipation existed for each circuit type. As an example consider the three variations of the following circuit:




- Variation 1 : If all the inputs are grounded then power dissipation (Pd) will be low. Essentially $P_d = ICEO_{total} \times V_{cc}$. Since the magnitude of ICEO is in the order of microamps at +125°C, the power dissipation will be in the order of microwatts. The resulting circuit is as follows:



- Variation 2: With one input at +3 V and the others grounded, the following results will be obtained:




$V_{be}$ (on) ≈ 0.5 V @ +125°C

$V_{ce}$ (sat) ≈ 0.1 V @ +125°C

$$PR_L = \frac{(V_{cc} - V_{ce})^2}{R_L} = 23.8 \text{ mw}$$

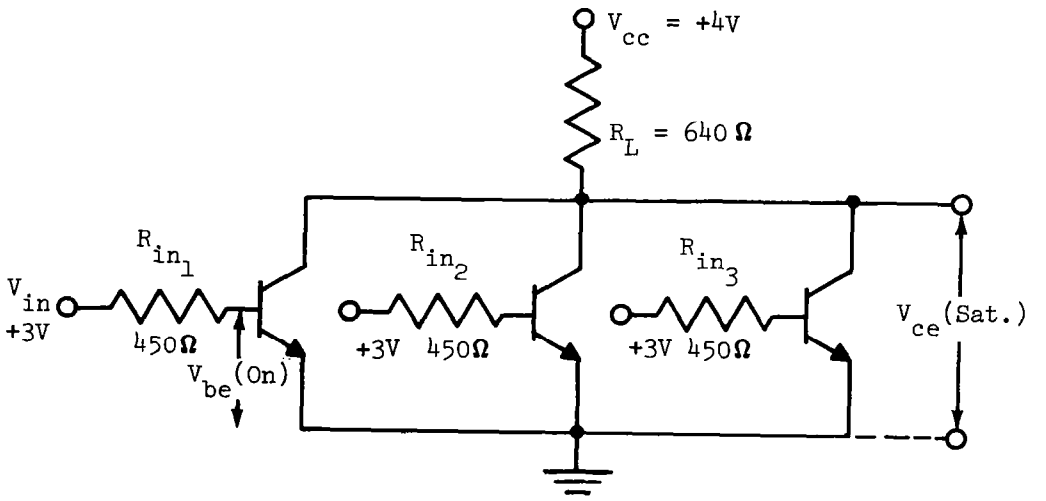
$$PR_{in} = \frac{(V_{in} - V_{be})^2}{R_{in}} = 13.9 \text{ mw}$$

$$IQ_1 = \frac{V_{cc} - V_{ce})}{R_L} = 6.1 \text{ ma}$$

$PQ_1 = V_{ce} \times IQ1 = 0.6$ mw

$P_{Total} = PR_L + PR_{in} + PQ_1 = 38.3$ mw

o Variation 3: With all inputs at +3 V, the following results will be obtained:



$V_{be}$ (on) $\approx$ 0.5 V @+125°C

$V_{ce}$ (sat $\approx$ 0.1 V @+125°C

$P_{RL}$ = 23.8 mw (as above)

3 X $PR_{in}$ = 3 X 13.9 mw = 41.7 mw

P ($Q_1$ + $Q_2$ + $Q_3$) = 3 ($PQ_1$) = 1.8 mw

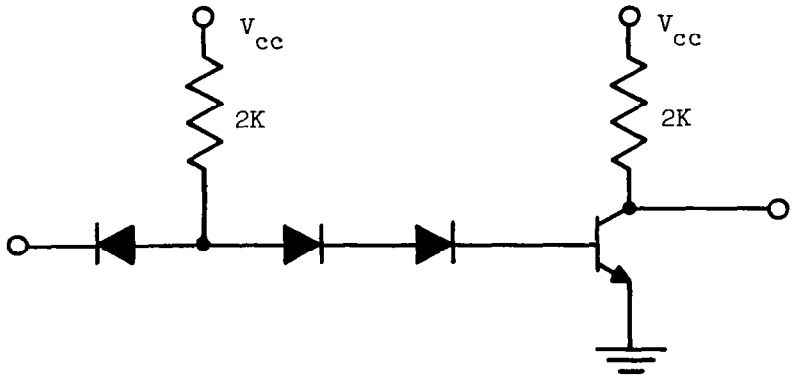
$P_{Total}$ = $PR_1$ + 3 ($PR_{in}$) + P ($Q_1$ + $Q_2$ + $Q_3$) = 67.3 mw

Thus, the worst-case steady state condition results from Variation 3. Each of the circuit types was analyzed in the above fashion to determine the conditions which would provide the worst-case power dissipation burn-in.

Following burn-in all D-C voltage levels and noise margins were measured at room temperature. Computerized variables analysis was employed to measure expected standard deviations, and to develop limits to be used in specifying device degradation.

2.4.3 Recommendations

The above worst-case approach results in the highest power dissipation for RTL gates. However, for other logic forms all circuit components are not stressed. For example, consider the following basic DTL gate:




The worst-case condition for the highest power dissipation is with the input at a high level. However, in this condition the input diode would be turned "off" and will not draw any current. Thus for DTL and $T^2L$ Logic, some components would not be power-stressed during burn-in.

Thus it was recommended that all devices should be switched "ON" and "OFF" using a 50% duty cycle (square wave) so that all components would be stressed at least half of

the time. It was also recommended that 10% be used as the maximum allowable degradation between pre and post burn-in electrical readings.

### 2.5.1 COMPUTERIZED VARIABLES ANALYSIS

#### 2.5.1 Description of Equipment

The equipment used was a GE 265 Time-Sharing Computer consisting of Datanet 30 and GE 235 Computers.

#### 2.5.2 Discussion

The electrical test data generated during this program becomes more meaningful when subjected to suitable analysis of variables. To set acceptability levels and to detect those devices exhibiting substandard performance, it was necessary to utilize statistical techniques in the data analysis. The complexity of the statistical methods and the large amount of data needed to make the analysis meaningful made the use of electronic data processing desirable.

A statistical computer program was written specifically for the data gathered during this project. Each electrical measurement had been made on families of approximately 50 devices. The devices within each family had been manufactured by identical processes. Each family of 50 was subdivided into 10 specific types. A computer program which would make maximum use of such data was sought.

Since identical processes are utilized within each family, it is reasonable to assume that the variations caused by process tolerances will be uniform throughout the family. However, each type will exhibit a different mean value, since its electrical interconnections are unique within the family.

From these considerations, it can be expected that although each type will have a different mean value, all types will show the same standard deviation when normalized to their mean values.

The computer program takes the mean value for each type and then normalizes each test value to its type-mean. All 50 normalized data are then used to calculate a normalized standard deviation for the entire family. When each type-mean is multiplied by the family normalized standard deviation, a projected standard deviation for that type is obtained. The significance of the computation is that 50 pieces of data are available for calculating each type's standard deviation, yielding a higher statistical significance than could be obtained by straightforward computation using the 5 pieces of data obtained for each type.

The actual standard deviations for each type were also calculated through the computer program for comparison.

Examples of the computations for the pre and post burn-in values of one measured parameter for one device family are shown in Tables 2-3 and 2-4. (The complete computer program and samples of the data obtained through its use are contained in Appendix A.) The computations were utilized by defining minimum and maximum levels for each measured value of ±1.5 projected standard deviations from the mean value for each device type. Devices which were beyond these limits were then subjected to failure analysis. Tables 2-5 and 2-6 show the results of applying this criterion to the computerized data previously presented. High and low limits are detailed and three deviant devices are subsequently identified.

### 2.5.3 Recommendations

Computerized Variables Analysis was found to be highly effective for detecting deviant devices in the course of this program. This technique has numerous potential applications in high reliability screening programs, including:

- Selection of samples to be destructively tested in preference to random selection. The samples selected by this process should yield more specific information on manufacturing errors than could otherwise be obtained.
- Minimum and maximum values for each parameter included in detail specifications can be set by a method similar to the one utilized in this program. The values so obtained would be more meaningful than arbitrarily selected values. They would realistically reflect the performance to be expected in the devices procured and would allow a high level of conformance to the specification.
- The standard deviations of incoming lots could be plotted to yield an early indication of looseness in manufacturing process controls.
- Conditioning methods can be optimized by computerized evaluation of their effects on device performance. For example, the effects of various time and temperature levels for stabilization baking can be evaluated to determine the optimum combination for use in a specification.

TABLE 2-3

COMPUTER ANALYSIS OF TI SERIES 53 PRE BURN-IN NOISE IMMUNITY ($V_{in}$-High)

Input Data:

| | | | | | | |
|---|---|---|---|---|---|---|
| SN 5311 | Serial No. | 1 | 2 | 3 | 4 | 5 |
| | Value | 1.51 | 1.13 | 1.26 | 1.09 | 1.09 |
| SN 5360 | Serial No. | 11 | 12 | 13 | 14 | 15 |
| | Value | 1.00 | 1.11 | 1.07 | .982 | .971 |
| SN 535 | Serial No. | 16 | 17 | 18 | 19 | 20 |
| | Value | 1.12 | 1.10 | 1.12 | 1.14 | 1.11 |
| SN 5370 | Serial No. | 21 | 22 | 23 | 24 | 25 |
| | Value | .965 | 1.07 | .970 | .998 | 1.09 |
| SN 5331 | Serial No. | 26 | 27 | 28 | 29 | 30 |
| | Value | 1.24 | 1.07 | 1.22 | 1.04 | 1.18 |
| SN 531 | Serial No. | 32 | 33 | 34 | 35 | No input catastrophic failure |
| | Value | 1.34 | 1.46 | 1.60 | 1.44 | |
| SN 533 | Serial No. | 41 | 42 | 43 | 44 | 45 |
| | Value | 1.34 | 1.39 | 1.28 | 1.20 | .974 |

Output Data:

Standard Deviation of Normalized Group = 8.12%
Family mean value = 1.175 volts

| Type No. | No. in Group | Mean | Std. Dev. | Projected SD |
|---|---|---|---|---|
| SN 5311 | 5 | 1.216 | .1597 | .0987 |
| 5360 | 5 | 1.027 | .0541 | .0833 |
| 535 | 5 | 1.118 | .0133 | .0907 |
| 5370 | 5 | 1.019 | .0518 | .0827 |
| 5331 | 5 | 1.150 | .0805 | .0933 |
| 531 | 4 | 1.460 | .0927 | .1185 |
| 533 | 5 | 1.237 | .1459 | .1004 |

TABLE 2-4

COMPUTER ANALYSIS OF TI SERIES 53 POST BURN-IN NOISE IMMUNITY ($V_{in}$-High)

Input Data:

| | | | | | | |
|---|---|---|---|---|---|---|
| SN 5311 | Serial No. | 1 | 2 | 3 | 4 | 5 |
| | Value | 1.35 | .979 | 1.10 | .921 | .908 |
| SN 5360 | Serial No. | No input - catastrophic failure | 12 | 13 | 14 | 15 |
| | Value | | .992 | .954 | .845 | .850 |
| SN 535 | Serial No. | 16 | 17 | 18 | 19 | 20 |
| | Value | .887 | .869 | .908 | .924 | .870 |
| SN 5370 | Serial No. | 21 | 22 | 23 | 24 | 25 |
| | Value | .820 | .937 | .803 | .845 | .964 |
| SN 5331 | Serial No. | 26 | 27 | 28 | 29 | 30 |
| | Value | 1.06 | .864 | 1.02 | .824 | .994 |
| SN 531 | Serial No. | 32 | 33 | 34 | 35 | No input - catastrophic failure |
| | Value | .985 | 1.05 | 1.20 | 1.11 | |
| SN 533 | Serial No. | 41 | 42 | 43 | 44 | 45 |
| | Value | .982 | 1.08 | 1.01 | .942 | .790 |

Output Data:

Standard Deviation of normalized group =9.37%
Family mean value = .961 volts

| Type No. | No. in Group | Mean | Std. Dev. | Projected SD |
|---|---|---|---|---|
| SN 5311 | 5 | 1.052 | .1639 | .0986 |
| 5360 | 4 | .910 | .0642 | .0853 |
| 535 | 5 | .892 | .0215 | .0836 |
| 5370 | 5 | .874 | .0646 | .0819 |
| 5331 | 5 | .952 | .0918 | .0893 |
| 531 | 4 | 1.086 | .0792 | .1018 |
| 533 | 5 | .961 | .0965 | .0900 |

TABLE 2-5 LIMITS (1.5 Projected Standard Deviations) FOR TI SERIES 53 PRE BURN-IN NOISE IMMUNITY ($V_{in}$-High)

| TYPE NO. | MEAN VALUE | LIMITS | | FAILURES (serial no. and value) |
|---|---|---|---|---|
| | | MINIMUM | MAXIMUM | |
| SN 5311 | 1.216 | 1.068 | 1.364 | S/N 1 = 1.51 |
| 5360 | 1.027 | .902 | 1.152 | none |
| 535 | 1.118 | .982 | 1.254 | none |
| 5370 | 1.019 | .895 | 1.143 | none |
| 5331 | 1.150 | 1.010 | 1.290 | none |
| 531 | 1.460 | 1.282 | 1.638 | none |
| 533 | 1.237 | 1.086 | 1.388 | S/N 42 = 1.39<br>S/N 45 = 0.974 |

TABLE 2-6 LIMITS (1.5 Projected Standard Deviations) FOR TI SERIES 53 POST BURN-IN NOISE IMMUNITY ($V_{in}$-High)

| TYPE NO | MEAN VALUE | LIMITS | | FAILURES (serial no. and value) |
|---|---|---|---|---|
| | | MINIMUM | MAXIMUM | |
| SN 5311 | 1.052 | .904 | 1.200 | S/N 1 = 1.35 |
| 5360 | .910 | .782 | 1.038 | none |
| 535 | .892 | .767 | 1.017 | none |
| 5370 | .874 | .751 | .997 | none |
| 5331 | .952 | .818 | 1.086 | none |
| 531 | 1.086 | .933 | 1.239 | none |
| 533 | .961 | .826 | 1.096 | S/N 45 = 0.790 |

## 3.0 DESTRUCTIVE TEST STUDIES

The following analytical techniques were studied during this program:

- Decapsulation
- Microscopic Examination
- Electrical Probing
- Infrared Scanning
- Microsectioning
- Electron Probe Microanalysis and Scanning Electron Microscopy.

The equipment used for each technique, the results obtained on selected devices, and recommendations for incorporation in high-reliability programs are discussed in detail in this section.

### 3.1 DECAPSULATION

#### 3.1.1 Description of Equipment

The equipment used included:

- Motorola Can Opener
- Miniature Vise
- Razor Knife
- Tweezers
- Specimen Mounting Molds
- Epoxy (room temperature curing)
- Polishing Paper (320 grit)

#### 3.1.2 Discussion

Prior to failure analysis or internal testing, the device cases must be opened allowing access to the internal structure. Because of the lack of standardized packaging, decapsulation methods keyed to each package are necessary. The specific techniques used for this program are described below. Packages not studied under this contract can be opened by similar methods.

- TO-5 Packages: The Motorola Can Opener is specifically designed for these packages. The device is inserted between the cutting wheel and the two idler wheels until the package flange seats on the wheels (Figure 3-1). The cutting wheel is turned by the hand crank until the case is severed. One of the idler wheels is spring-loaded to maintain pressure between the device and the cutting wheel.

- Flat-Pack (Signetics): The kovar lid of the Signetics package is offset such that it extends slightly beyond the edge of the glass case. Inward pressure from a sharp blade (razor knife) will break the glazed seal and will allow the lid to be peeled off (Figure 3-2).

- Flat-Pack (Fairchild): Because of normal manufacturing nonuniformities, the fairchild package has an offset lid similar to that of the Signetics package. However, since its glass-to-glass seal is stronger than the glass-to-metal Signetics, the lid cannot be pried off. Instead, pressure from a vise on the edges of the lid will cause it to bow, thus breaking the seal (Figure 3-3). The lid can then be picked off the case.

- Flat-Pack (Texas Instruments): The kovar lid of the Texas Instruments package is stitch-welded to the kovar body. Unlike the other flat-packs, there is no protrusion to which pressure can be applied. The only practicable way to open this package is to mount it in epoxy with the lid of the case at the surface of the mounting material. The assembly is then polished on 320-grit paper. Since the edges of the lid are the only areas supported by the case, they will be ground away more quickly than the center of the lid. Once a fine crack appears around the edges, the lid can be removed with tweezers. Figures 3-4 and 3-5 show a mounted and decapsulated device.

### 3.1.3 Recommendations

Only the methods described above are recommended for decapsulation prior to internal studies. Other methods were rejected because of potential damage to the device and the subsequent masking of failure modes. Heat could have been used to melt package seals, but damage to the device elements was possible. Lids could have been ground or milled off,

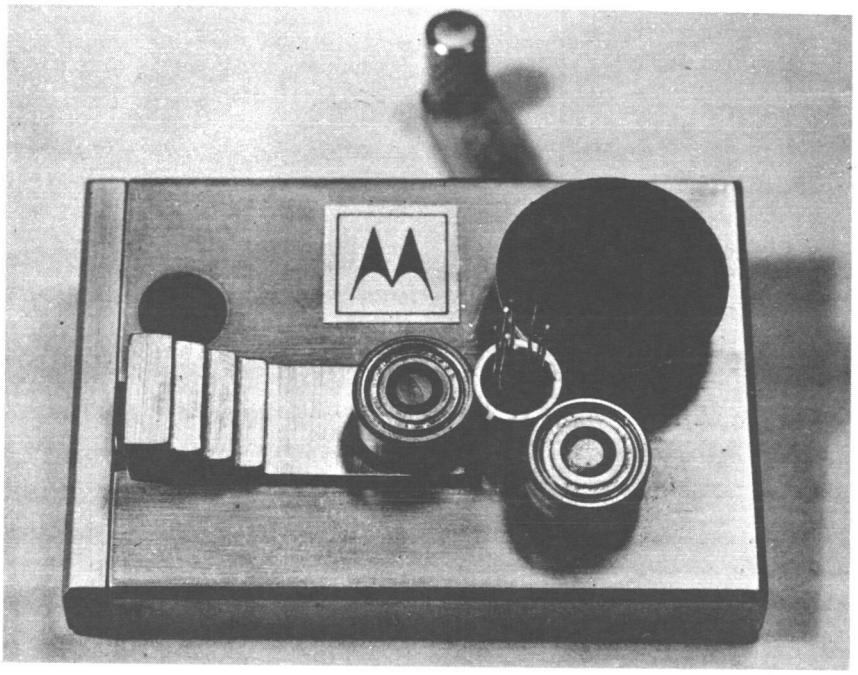


Figure 3-1 Motorola Can Opener

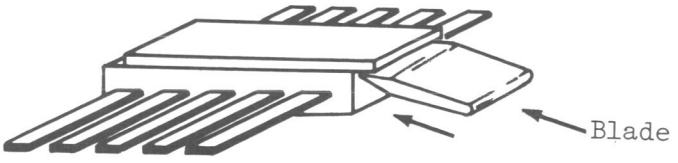



Figure 3-2 Decapsulation of Signetics Package

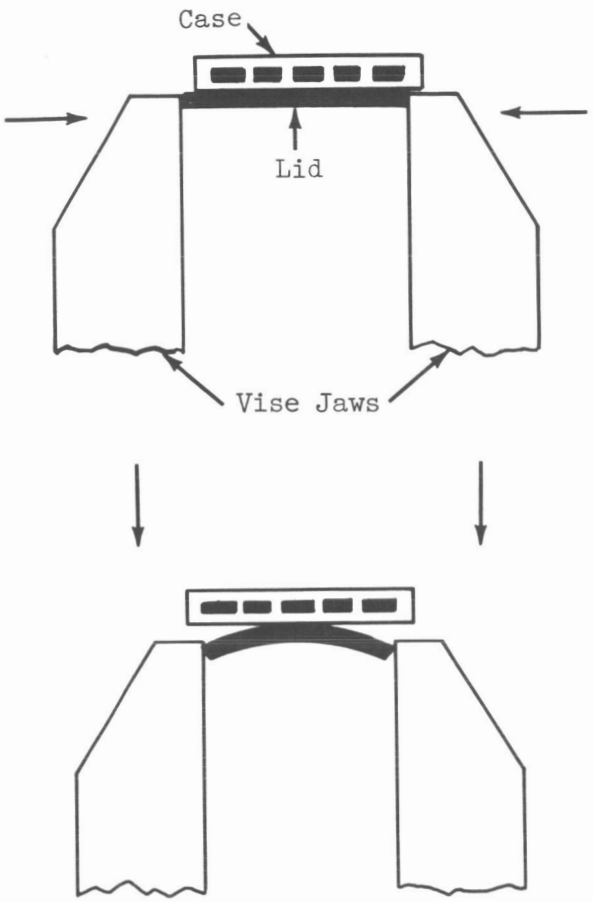



Figure 3-3 Decapsulation of Fairchild Flat-Pack.

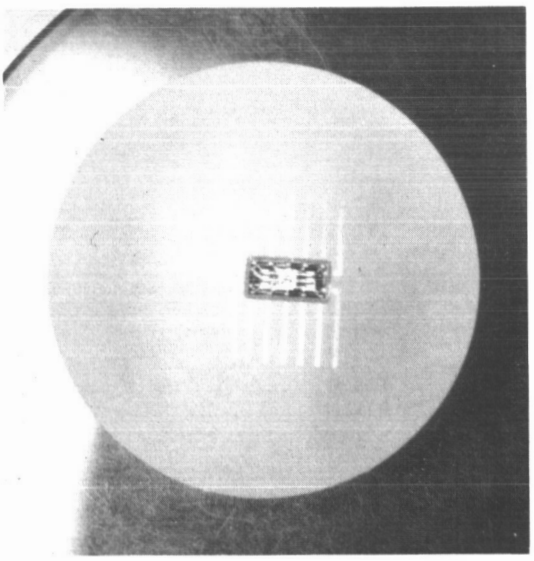


Figure 3-4 Mounted and Decapsulated T.I. Flat Pack.

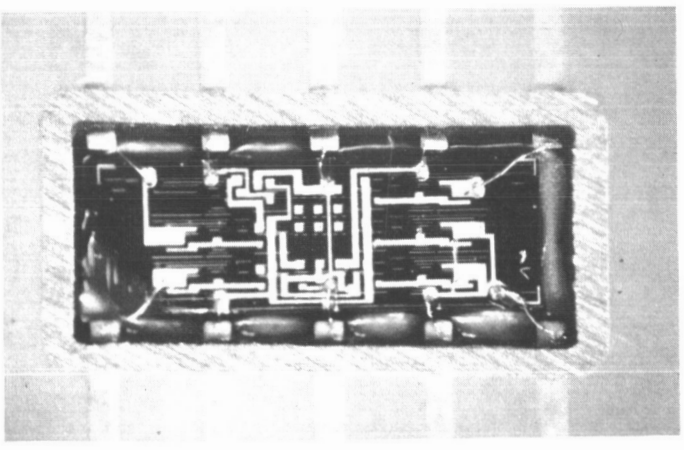


Figure 3-5 Detail View of Device in Figure 3-4

but particles injected into the case would mask pre-existing contamination. The recommended methods all leave the internal structure intact.

## 3.2 MICROSCOPIC EXAMINATION

### 3.2.1 Description of Equipment

The equipment used included:

- Stereo Microscope (Bausch & Lomb)
  - Magnification is continuously variable over a 4.3 to 1 range. Ranges cover 3.5 to 200 X
  - Vertical illuminator and Nicholas light source
  - Polaroid camera
- Optical Comparator (Nikon)
  - Provides magnifications of 20, 50, 100 and 200 X
  - Readout is on 12-inch diameter screen
  - Vertical (variable brightness) illumination
  - Camera (A Graflex back with Polaroid adapter replaces the viewing screen)
  - Stage is 1 by 1 inch with X-Y micrometer adjustments and rotation vernier-calibrated to 0.1 degree
- Research Metallograph (Bausch & Lomb)
  - Provides magnifications to 4000X
  - Vertical illumination
  - Light source with provision for polarized and monochromatic light
  - Polaroid camera

3.2.2 Discussion

Internal microscopic examination was used to clarify x-ray deviations, locate the areas of failure on discrepant devices identified through variables analysis, reveal surface topology, and examine the actual failure region.

To clarify or verify the significance of x-ray indications, all questionable devices were opened and optically examined. When the x-ray indication correlated to a known low-reliability situation, it was incorporated in the General Specification. Examples of x-ray/optical correlations are shown in Figures 2-8, 2-10, 2-16, and 2-18.

When analyzing catastrophic failures, optical examination often revealed the region of failure through such indicators as the open metalization shown in Figures 3-6. 3-7. and 3-8. Once such an indication was found, surface topology and the schematic diagram implied which circuit element was responsible for the failure. In other cases, electrical probing under a microscope was necessary to reveal the failed circuit element.

When the failure mode of the circuit element was not obvious, microsectioning was utilized. High-power microscopic examination (200 to 4000X) under a research metallograph was applied to sectioned junctions, metalization or bonds. A microsection is illustrated in Figure 3-22.

The test devices were also examined microscopically on a sample basis to determine surface topology tolerances, bond quality, internal contamination levels and construction techniques.

All significant results were incorporated in the writing of the Internal Visual Inspection section of the General Specification. Figure 3-9 shows a low-reliability bonding arrangement which violates Section 6.1.3.3 of the Specification (bond not completely on pad). Figure 3-10 illustrates a violation of section 6.1.2 (laquer on device surface), and Figure 3-11 shows a violation of Section 6.1.3.4 (open bond).

It should be noted that microscopes can be used in coordination with a dial indicator to measure depths or heights. The dial indicator is attached to the head or stage, whichever is moved for focusing. The microscope is then focused on the area of interest and upon a reference area. The difference in the corresponding dial indicator readings is the

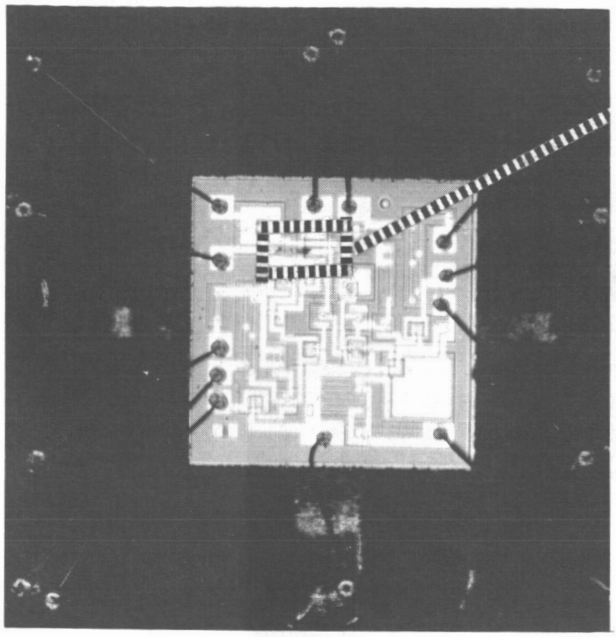


Figure 3-6 Open Metallization Shown Under 20X Magnification.

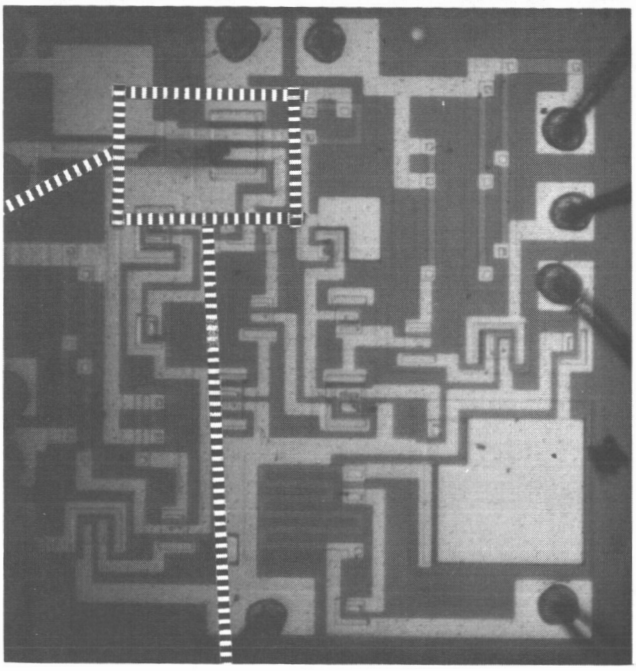


Figure 3-7 Device in Figure 3-6 Under 50X Magnification.

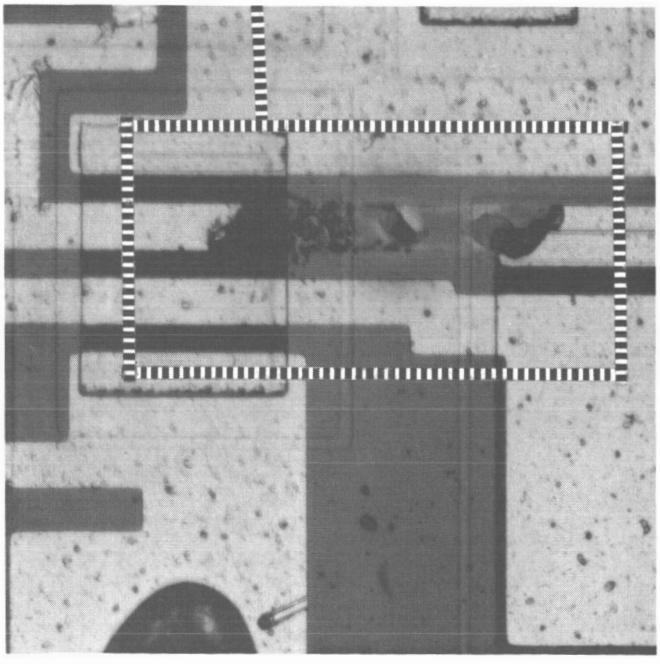


Figure 3-8 Device in Figure 3-6 Under 200X Magnification.

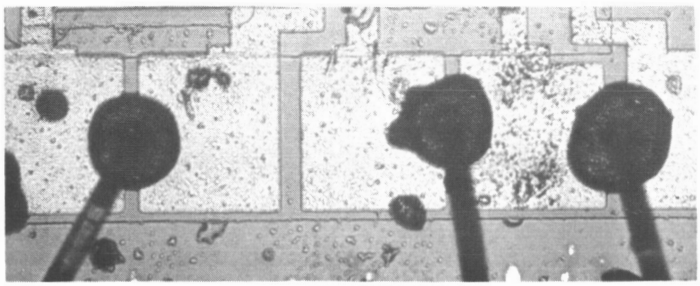


Figure 3-9 Low Reliability Bonding Arrangement. Strength of Bond to Each Pad Depends Upon Perfect Location of Bond. (Violates section 6.1.3.3 of the General Specification).

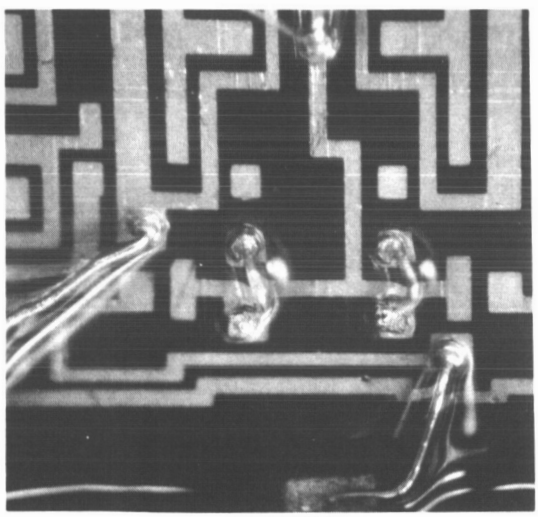


Figure 3-10 Lacquer on the Die Surface. (Violates section 6.1.2 of the Specification).

measured height. This technique was used to measure die-to-header bonding material thickness and the height of excessive gold preform build-ups.

### 3.2.3 Recommendations

Depending upon the magnification required different equipment is recommended.

- 3.5 to 60X: The inexpensive stereo microscope yields a three-dimensional view and allows continuously variable magnification. It takes little bench space and is unaffected by room lighting, and is recommended for this magnification range.

- 50 to 200X: The stereo microscope lacks mechanical stability and definition above 60X, and the optical comparator is recommended for 50 to 200X. Dimensional measurements can be made directly from the screen and group viewing is possible. Room ambient lighting must be minimized for easy viewing.

- 200 to 6000X: Since microsection examination is the primary work conducted in this magnification range, the Research Metallograph is recommended. It is specifically designed for such high magnification examinations and it provides the polarized, monochromatic light often needed. It possesses high resolution and high mechanical stability.

Vertical illumination should be provided on all optical microscopic instrumentation, as it allows optical interference patterns to form within the devices diffusion and oxide layers. Each layer thickness will exhibit a different color under tungsten light, thereby delineating different circuit elements by their color. This illumination technique effectively adds an extra dimension to visual examinations. An example of the gain in information provided by vertical illumination as compared with off-axis illumination is shown in Figures 3-12 and 3-13.

It is recommended that post-sealing internal inspection be performed only after burn-in. In this way, maximum non-destructive electrical test data is available for analysis prior to destruction of the device. Furthermore, devices should be selected for examination on the basis of non-destructive test results. A random sample would only serve to minimize the usefulness of this technique.

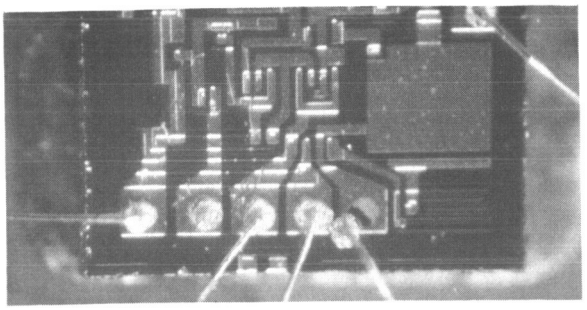


Figure 3-11 Open Bond. (Violates section 6.1.3.4 of General Specification)

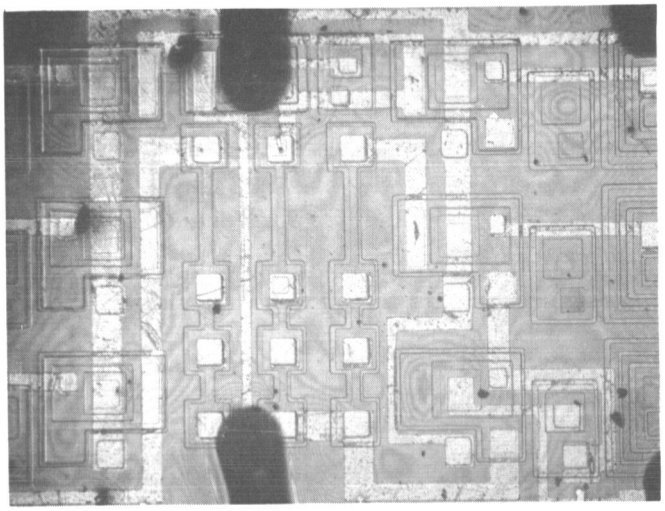


Figure 3-12 Microcircuit Under Vertical Illumination.

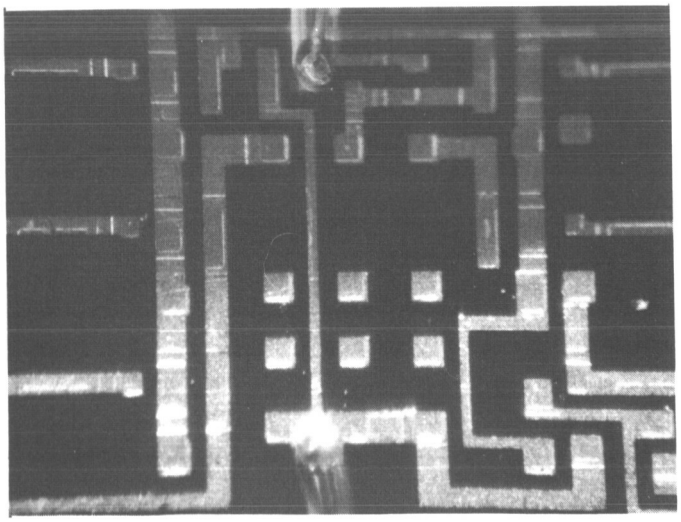


Figure 3-13 Microcircuit of Figure 3-12 With Off-Axis Illumination.

## 3.3 ELECTRICAL PROBING

### 3.3.1 Description of Equipment

- Needle Point Probe (Dumas)
  - Probe stations with "joysticks" for X-Y orientation and knobs for height control. (Four stations were provided, but as many as necessary are available from the manufacturer.)
  - Probes with 1/4 mil diameter tips
  - Vacuum chuck
  - Connection points are provided by banana jacks
- Microscope (Bausch & Lomb)
- Curve Tracer (Tektronix 575)

### 3.3.2 Discussion

Electrical probing was used for failure analysis and for the evaluation of individual circuit elements (Figure 3-14). The needle point probes were placed on the metallization of circuit elements with the aid of a stereo microscope (Figure 3-15). Care was necessary to avoid scratching the device surface, breaking the bonding wires, or bending the probe tips. The probes were then connected to the curve tracer and the appropriate parameters were measured. When applicable, the following measurements were made:

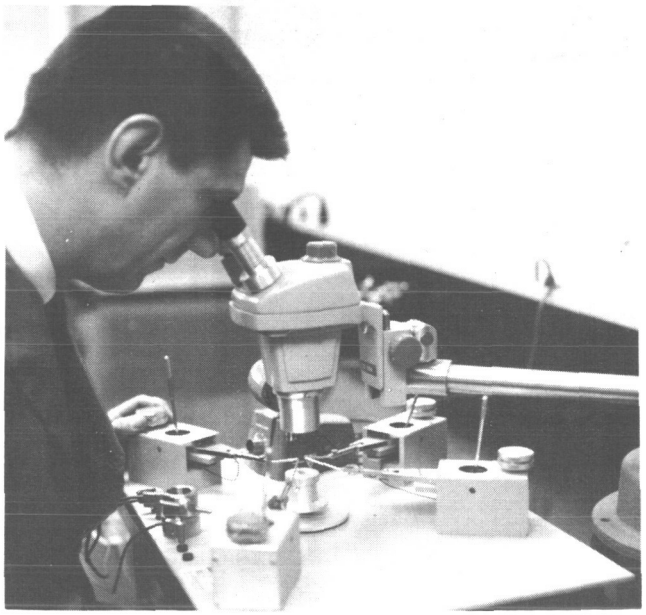


Figure 3-14 Electrical Probing Station.

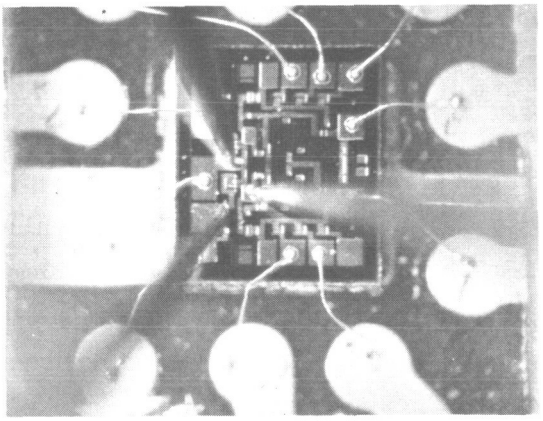


Figure 3-15 Microscope View Showing Placement of Probes.

- Transistors
  - Collector voltage-current curve families
  - ICEO
- Diodes
  - Forward voltage-current curves
  - Reverse voltage breakdown
  - Reverse leakage current
- Resistors
  - Resistance
  - Voltage breakdown

Before such measurements can reveal the failed component, standards for comparison must be obtained. To obtain such standards, a number of circuits were decapsulated and probed. An example of the results of such an evaluation is shown in Table 3-1 for five Fairchild $\mu$ L 914 devices. The data from this study lot were treated statistically to obtain the mean values and standard deviations for $h_{fe}$ and $h_{FE}$ of the transistors within each device, as well as calculations for all the transistors within the group. In addition, each measured value was normalized to the mean value for its corresponding individual device, and a normalized standard deviation for the entire group was calculated. These computations are presented in Table 3-2.

The normalized standard deviation of approximately 8% implies that most circuit elements will have values within a $\pm$ 8% range when compared to an average value within an individual device. This narrow range is not applicable when a circuit element is compared with elements within another device, as evidenced by a 41% standard deviation for the elements of all five devices. The low standard deviation within individual circuits is to be expected, since all the elements are formed during the same process. The process variables are prominent only when comparing two complete devices.

These results imply that individual circuit element failures are most readily revealed by comparison with similar elements within the same device. The low standard deviations for such comparisons will make any failure readily apparent. However, circuits also fail when all the components have the similar substandard values. In this case, the failed device must be compared to known high-quality devices. The most fruitful approach is to compare the components within a device and, if that is not successful, to compare two or more devices. As an example, Table 3-2 shows a criterion of 2.5 normalized standard

TABLE 3-1 INDIVIDUAL CIRCUIT ELEMENT VALUES FOR FAIRCHILD, $\mu$L 914

| Measurement | | Serial Number 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|
| $h_{fe}$ ($V_{ce}$ = 3.0V; $I_c$ = 2.0m A) | $Q_1$ | 65 | 120 | 50 | 50 | 110 |
| | $Q_2$ | 55 | 130 | 65 | 65 | 110 |
| | $Q_3$ | 60 | 140 | 50 | 50 | 110 |
| | $Q_4$ | 60 | 130 | 50 | 50 | 110 |
| $h_{FE}$ ($V_{ce}$ = 0.8V; $I_c$ = 2.0m A) | $Q_1$ | 38 | 90 | 40 | 46 | 90 |
| | $Q_2$ | 38 | 95 | 47 | 47 | 97 |
| | $Q_3$ | 42 | 105 | 37 | 43 | 98 |
| | $Q_4$ | 42 | 100 | 42 | 35 | 85 |
| $R_L$ | Section 1 | 571 | 570 | 570 | 615 | 500 |
| | Section 2 | 571 | 570 | 570 | 615 | 530 |
| $R_{in}$ | Input 1 | 400 | 400 | 380 | 421 | 380 |
| | Input 2 | 400 | 400 | 380 | 412 | 420 |
| | Input 3 | 400 | 400 | 380 | 412 | 412 |
| | Input 4 | 400 | 400 | 380 | 412 | 470 |

deviations (approximately 20%) applied to each device's mean value to yield high and low limits for individual circuit elements within the device.

An example of this approach was the analysis of a Signetics SE 101 (S/N 1) which exhibited low noise immunity after burn-in. A sufficient number of elements were available to allow comparison within the individual device. Table 3-3 presents the test results. The shorted base input diode is readily apparent, as all the other diodes had a reverse breakdown voltage of approximately 18.1 volts.

A Fairchild $\mu$ L 930 (S/N4) which also showed low noise immunity after burn-in was similarly analyzed. Table 3-4 shows that one of the input diodes had a 1.0-volt reverse breakdown voltage, while all the other diodes had breakdown voltages above 6.0 volts.

Once the failed elements were located, it was possible to apply further analytical techniques (such as microsectioning) for the determination of specific failure modes.

TABLE 3-2 STATISTICAL TREATMENT OF INDIVIDUAL CIRCUIT ELEMENT VALUES FOR FAIRCHILD $\mu$ L 914

| | | Serial No. | | | | | |
|---|---|---|---|---|---|---|---|
| | | 6 | 7 | 8 | 9 | 10 | Group |
| $h_{fe}$ | Mean | 60 | 130 | 53.8 | 53.8 | 110 | 81.5 |
| | Std Dev | 3.5 | 7.1 | 6.5 | 6.5 | 0 | 32.6 (40%) |
| | Proj SD | 5.07 | 11.0 | 4.55 | 4.55 | 92.8 | 8.44% * |
| | Limits | 47/73 | 103/157 | 42/65 | 42/65 | 87/133 | --- |
| $h_{FE}$ | Mean | 40 | 97.5 | 41.5 | 45.3 | 92.5 | 63.4 |
| | Std Dev | 2 | 5.6 | 3.6 | 5.3 | 5.3 | 26.7 (42%) |
| | Proj SD | 3.14 | 7.64 | 3.25 | 3.55 | 7.25 | 7.84% * |
| | Limits | 32/48 | 78/117 | 33/50 | 36/54 | 74/111 | --- |

* These values are the group standard deviation calculated from data which have been normalized to the mean value for their corresponding individual device. The projected standard deviations are calculated by multiplying this group normalized standard deviation by each device's mean value.

TABLE 3-3 INDIVIDUAL DIODE VALUES FOR SIGNETICS SE 101 (Serial No. 1)

| Measurement | Input Diodes - Section 1 | | | | Base Diodes | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 1 | 2 |
| Turn-on voltage (50 $\mu$a) | 0.60 | 0.60 | 0.60 | 0.60 | 0.59 | 0.34* |
| Breakdown voltage (10 $\mu$a) | 18.1 | 18.1 | 18.1 | 18.1 | 18.2 | 0.5 v* at 58 $\mu$a |

* These values yield an equivalent forward resistance of 6800 ohms and a reverse resistance of 8620 ohms, indicating a shorted diode.

TABLE 3-4 INDIVIDUAL DIODE VALUES FOR FAIRCHILD $\mu$L930 (Serial No. 4)

| Measurement | Input Diodes - Section 1 | | | | Input Diodes - Section 2 | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 1 | 2 | 3 | 4 |
| Turn-on voltage (50 $\mu$a) | 0.64 | 0.64 | 0.68 | 0.64 | 0.64 | 0.64 | 0.64 | 0.64 |
| Breakdown voltage (50 $\mu$a) | 6.1 | 6.1 | 1.0 | 6.0 | 6.0 | 6.0 | 6.0 | 6.0 |

### 3.3.3 Recommendations

Needle point probing is a basic tool for the location and analysis of specific circuit elements causing substandard microcircuit performance or failure. Its usefulness is enhanced by the availability of standards of comparison for each device type. It is recommended that such standards include the percent standard deviation of circuit element values to be expected within each individual device, as well as the mean value and standard deviation that each circuit element will exhibit over a number of devices of a given type. This data can be economically obtained with the aid of computerized variables analysis.

Needle point probing can be used to extensively correlate device reliability to circuit element performance during future high-reliability programs. The information gained could be computer-analyzed and used to write individual circuit element evaluation (on a sampling basis) into high-reliability specifications.

## 3.4 INFRARED SCANNING

### 3.4.1 Description of Equipment

The equipment used included:

- Thermal Plotter (Philco)
  - Detector: Indium antimonide cooled by liquid nitrogen for low signal-to-noise ratio.
  - Electronics: Pre-detector mechanical chopping with audio frequency amplification and uncalibrated meter readout.
  - Stages: Manual stage with micrometer adjustment or full automatic stage with X-Y (raster) scan.
  - Resolution: Approximately 0.3-mm spot diameter.
  - Sensitivity: 0.5°C with a 40°C minimum detectable temperature threshold.
  - Calibrator: Temperature-monitored black-body aperture.
- Quantizer (Grumman)
  - Input: Signal is taken from Thermal Plotter meter circuit.
  - Comparators: Triggered by input signal at any of 6 preset temperatures.
  - Indicators: 2 of 7 lights indicate which temperature range the input signal is within.
  - Output: Fed by all 6 comparator circuits, an output signal is provided when the input is at any of the preset temperatures.

- Recorder (Mosely)
  - Used with Quantizer.
- Constant Emissivity Coatings
  - 3M or Krylon flat black spray coatings.

3.4.2 Discussion

The spatial temperature distribution of a microcircuit can be used to locate failed components or to reveal poor layout or construction. However, the microscopic mass of the areas to be investigated precludes any contacting (probe) form of measurement. Instead, the thermal radiation must be measured.

The basic Thermal Plotter consists of reflecting optics which focus the radiation on an indium antimonide detector whose signal is amplified and displayed on a meter. The detector is cooled in liquid nitrogen to maintain a low signal-to-noise ratio, and the signal is mechanically chopped to permit low-drift a-c amplification. The device, with operating voltages applied, is manipulated with X-Y micrometer adjustments. An optical microscope using the same objective lens as the infrared section is used to view the area under examination.

A calibration curve (Figure 3-16) which correlates actual temperature and meter readout units is obtained with a monitored black-body. However, this curve is accurate only for a surface with approximately 100% emissivity. The actual temperature for a test device will be readout temperature divided by the surface emissivity.

An example is the thermal plot of a carbon resistor (Figure 3-17), where the colored identification bands result in steps in the readout. Since the surface emissivities are not generally known, a constant (approximately .95) emissivity coating such as 3M or Krylon flat black is used. The meter readout and the calibration curve then show a close correspondence with actual surface temperatures. Once calibration is achieved, the device can be manually scanned and the temperatures plotted on an X-Y isothermal map for comparison with known acceptable devices. However, this manual process is so time-consuming that it is impractical for any non-research use. For this reason, a Quantizer was designed and constructed to permit automatic plotting of isothermal maps.

The Quantizer is fed by the output of the thermal plotter and provides an output signal when the temperature is at any of six preset values. An automatic substage moves the device in

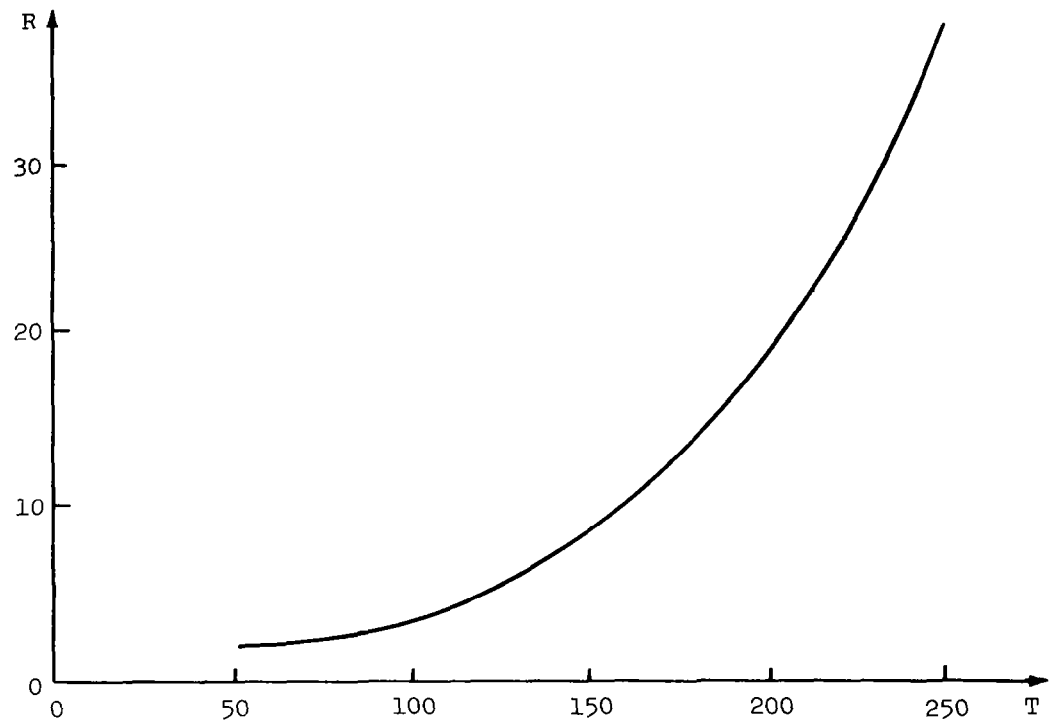



Figure 3-16 Calibration Curve Correlating Temperature T to Meter Readout Units R.

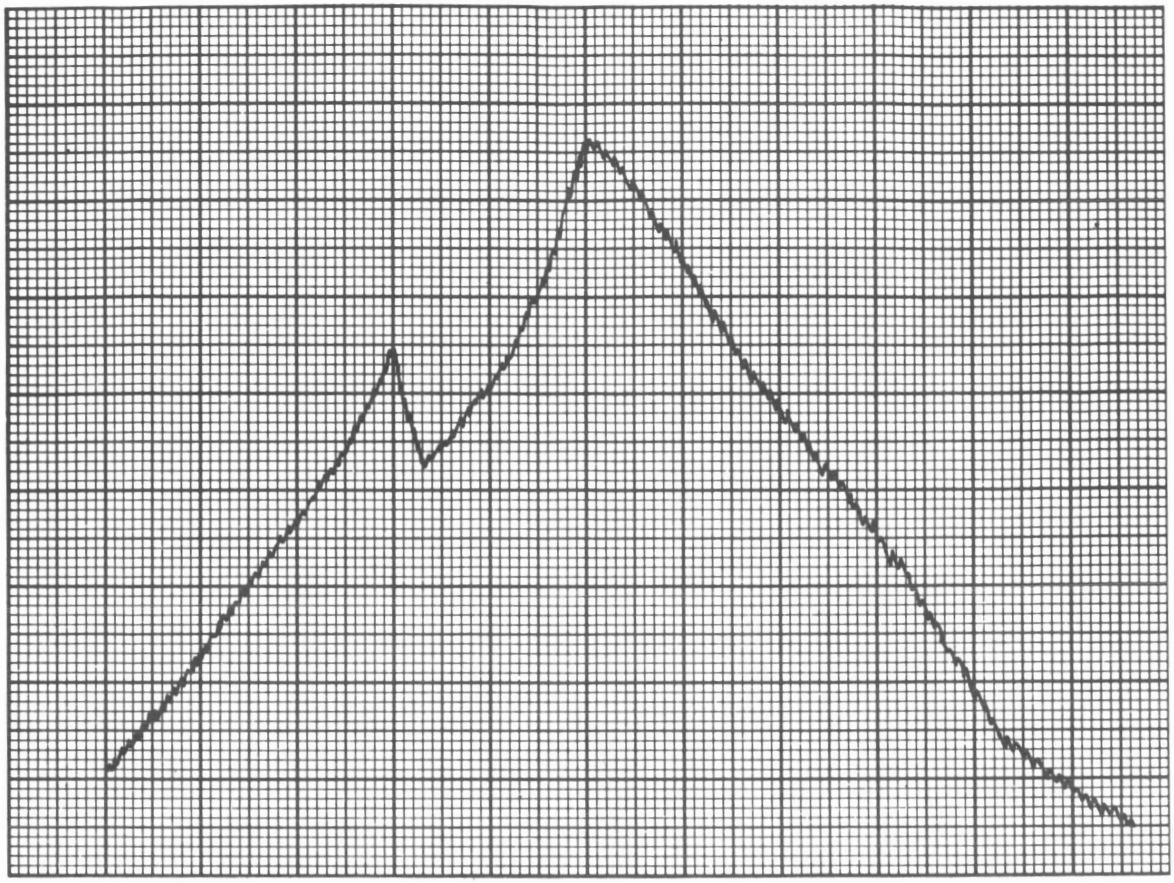


Figure 3-17 Transcribed Thermal Plot of Carbon Resistor.

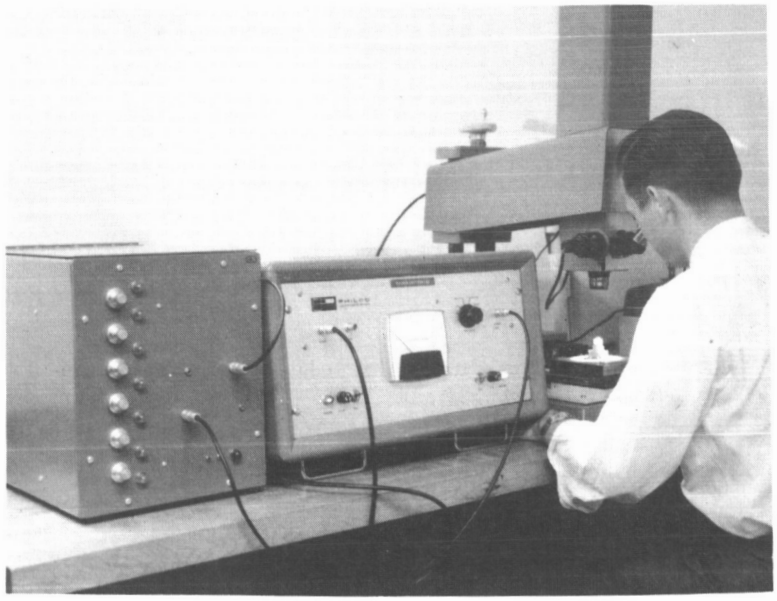


Figure 3-18 Thermal Plotter Instrumentation.

a raster pattern, and an X-Y recorder controlled by the substage moves in a matching pattern. The recorder pen is controlled by the Quantizer and produces a dot at any of the six preset temperatures. These dots will form a series of up to six isotherms. The finished maps can then be compared to standards previously obtained.

The finished system (Figure 3-18) was first applied to this program by mapping the TI series 51 devices. This low-power series was chosen to test whether this system would be applicable in a General Specification for all microcircuits. However, the low (7 mw) power level did not yield a sufficient temperature rise to permit detection above system noise. Increasing the power levels above the rated valves would not improve the situation, as the relationship between the temperatures of resistive elements and semiconductor elements would be distorted. (The temperature of resistors would increase as the square of the applied voltage, while the semi-conductor elements would increase approximately linearly with applied voltage.)

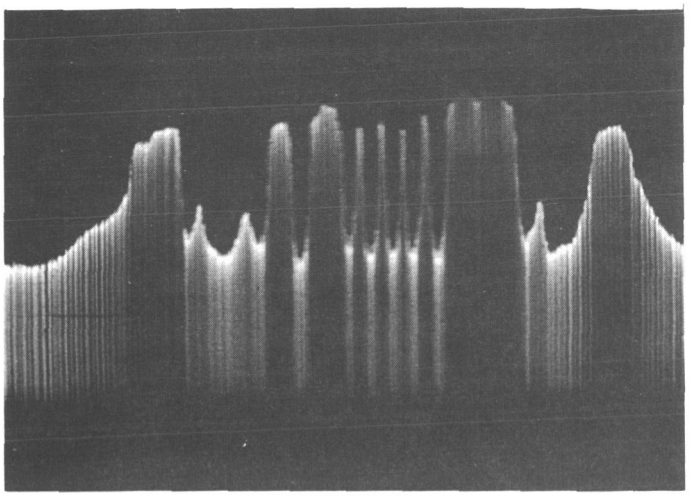
In addition, the reliability of the instrumentation seriously impairs its application, as mechanical problems result in large down-time figures. It is anticipated that further development of this relatively new instrumentation will remedy this situation.

### 3.4.3 Recommendations

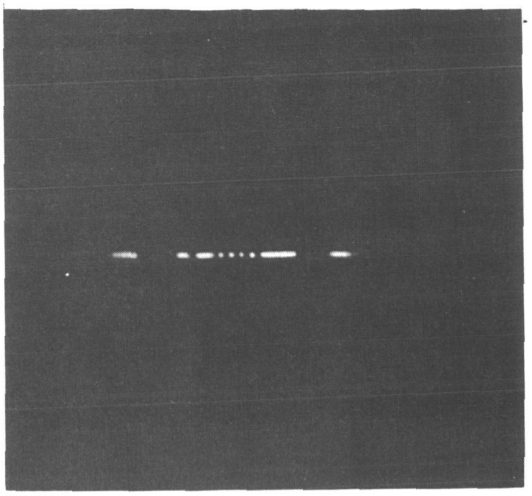
Most of the information yielded by thermal plotting can be obtained from the less expensive and more highly developed electrical probing technique. In addition, the low power densities found in digital circuits combine with the present lack of equipment reliability to preclude the incorporation of thermal plotting in the General Specification. However, it is anticipated that the equipment reliability will be improved. Thermal plotting should then prove useful with high power-density devices, particularly for design and process evaluation or user destructive testing.

Work performed by Philco in synthesizing infrared plots and displaying them on an oscilloscope is shown in Figure 3-19. This analysis could be valuable for obtaining information applicable to the indicated processing and testing areas. It should be noted, however, that the operating power level for the circuit under analysis was 60 mw. This represents a minimum power level at which infrared scanning can be applied.

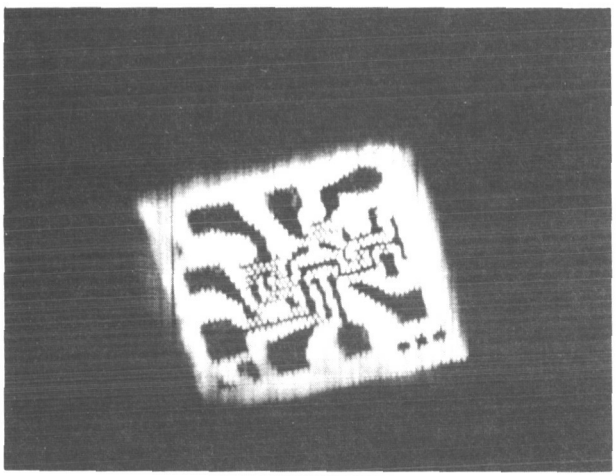
For this reason, the Thermal Plotter will be applied by Grumman for future work in large-scale integration, dielectric isolation construction and for large arrays.



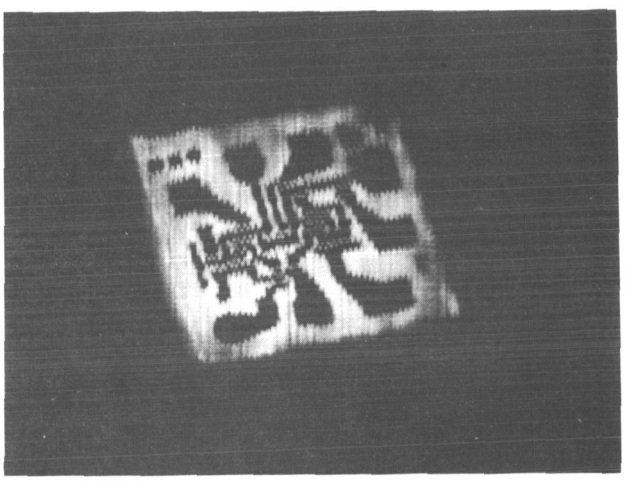
A. Plot of a single line through center of circuit made by modulating 750 cycle sine wave carrier with output of Philco Thermal Plotter.



B. Same scan line as in A quantized and fed into Z-axis of oscilloscope.



C. Radiation plot of entire circuit formed by 150 scan lines. Grey scale is concentrated on aluminum metallization to highlight ball-bond areas.



D. Radiation plot of same circuit with gray scale concentrated on silicon. Maximum temperature of circuit is +80°C (at brightest areas). Temperature on dark edges of silicon is approx. +70°C.

Figure 3-19 Steps in Synthesizing Infrared Plot of Fairchild Dual 2-Input NOR Gate Integrated Circuit. Chip Size is 0.050" Square. Circuit is Being Operated at Worst-Case Power Level of 60 mW.

## 3.5 MICROSECTIONING

### 3.5.1 Description of Equipment

The equipment used included

- Specimen Molds
- Room Temperature-setting Epoxy
- Glass Slides
- Polishing Wheel
- Diamond Paste (medium and fine)
- Acids ($HNO_3$ and HF)

### 3.5.2 Discussion

Once the locations of failures were determined, the devices were subjected to microsectioning, as necessary, to determine the exact physical nature of the failure.

Since the areas of interest were quite small, angle microsectioning was usually necessary. This technique yields an apparent magnification on the order of 10X, since the specimens are sectioned at an angle of 5 to 10° to the surface.

The technique used consisted of the molding of prefabricated cylindrical epoxy plugs with a flat surface at the desired angle to the axis (Figure 3-20). Each opened circuit was cemented in place near the apex of a plug and the assembly inserted in a cylindrical mold, keeping the top of the circuit level with the top of the mold.

Room-temperature-curing epoxy was then poured into the mold and a glass slide placed over it (Figure 3-21). When cured, the assembly was removed from the mold, leaving a mirror surface at the desired angle to the device.

This surface was polished using 2-micron diamond paste until the surface of the chip was approached. A finer grade of diamond paste was then used with frequent microscopic checks until the area of interest was reached. The surface was then etched with 20 parts $HNO_3$ and 1 part HF for 1/2 second before the final metallographic examination.

After microsectioning, the junctions, bonds, and other structures were clearly defined. Flaws in the crystal were detectable, circuit element dimensions and diffusion depths were

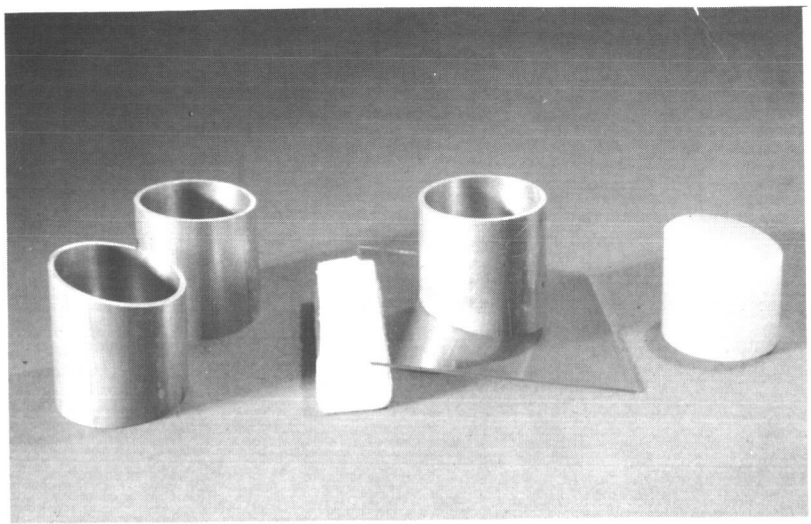


Figure 3-20 Prefabrication of Angle Mounts for Sectioning.

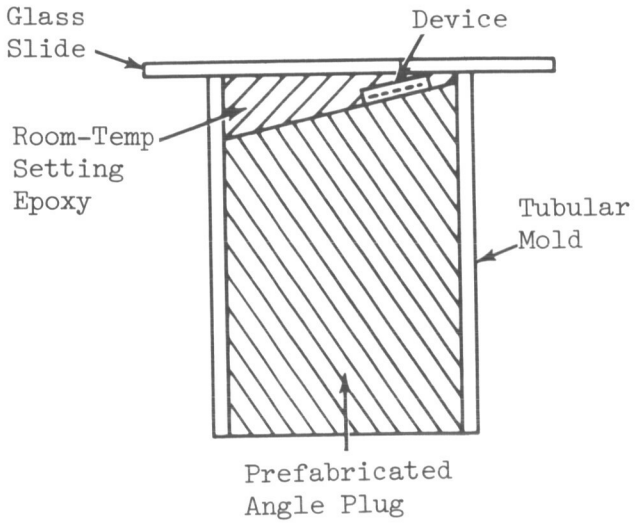



Figure 3-21 Final Encapsulation of Microcircuit for Angle Sectioning.

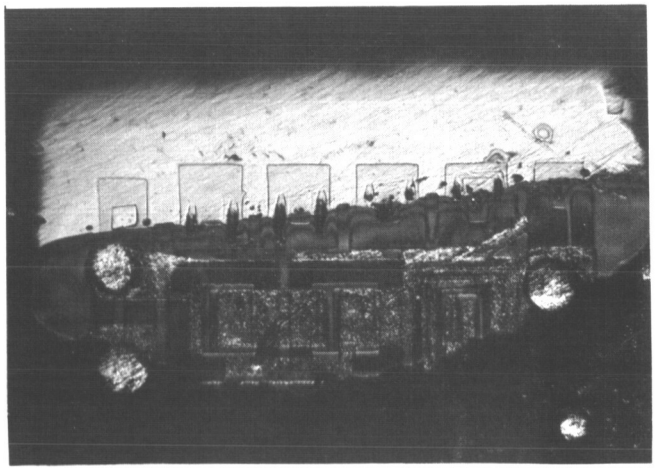


Figure 3-22 Metallograph of Microsectioned Device.

measurable, and any foreign materials within the structure was apparent. Figure 3-22 shows a multiple diode array with flaws in the crystalline structure which were visible under metallographic examination. When optical investigations are fruitless, the sectioned sample can also be subjected to electron microprobing for a microscopic chemical analysis.

### 3.5.2 Recommendations

Although it is only sometimes necessary, microsectioning yields information not obtainable from any other technique. For this reason, it should be an integral part of any failure analysis or design review program. It is the only method which will produce information on a physical fault (or characteristic being investigated) which is not visible under microscopic examination because of a subsurface location.

Microsectioning is worthwhile only if simpler techniques do not yield adequate information. It is not recommended that it be performed as a screening test on a statistical (random) basis. Instead, only selected deviant devices should be microsectioned.

## 3.6 ELECTRON PROBE MICROANALYSIS AND SCANNING ELECTRON MICROSCOPY

### 3.6.1 Discussion

The electron probe microanalyzer and the scanning electron microscope are basically similar, with their major differences being in the types of signals detected and the detection systems employed. For this reason, both instruments will be discussed in this section.

The basic electron-optical principle of both instruments is shown in Figure 3-23. High-voltage electrons (5 to 50 kv) from an electron source are focused into a sub-micron spot on the sample surface by means of two magnetic lenses, each successively forming a de-magnified image of the electron source (filament). The sample is generally in a vacuum of $10^{-5}$ to $10^{-7}$ torr, depending upon the instrument and the signal to be detected. By placing electric or magnetic scanning plates or coils between the two lenses the beam can be swept over the sample surface in a television-like raster. The signal, which is simultaneously detected, can be displayed on an oscilloscope which scans in synchronism with the beam. The oscilloscope display is thus a map of the signal being detected as it appears upon the sample surface. The image is magnified by the ratio of the sizes of the two rasters. Magnifications of up to 5000 diameters are practical with instruments available today.

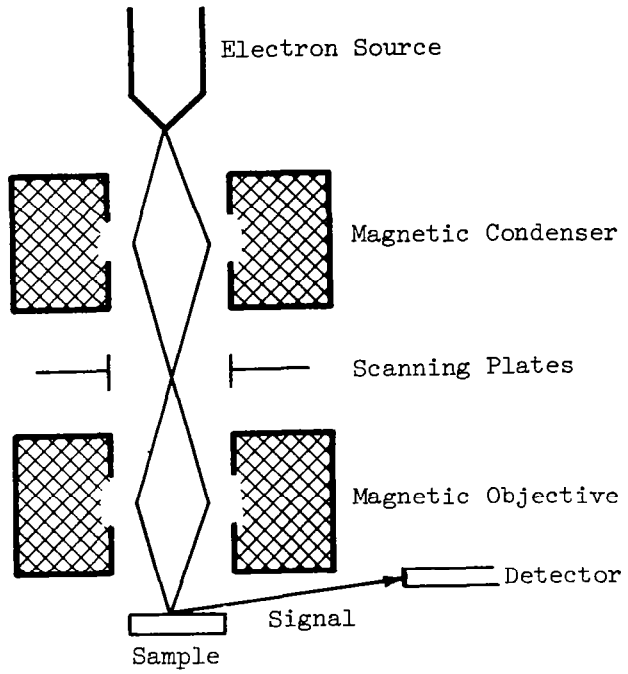



Figure 3-23 Basic Functional Diagram of Electron Beam Instruments.

The signals that are detected are caused by the interaction of the electron beam with the sample under bombardment. The following signals can presently be detected with a modern electron beam instrument:

- Characteristic X-Rays (from the elements present in the sample area under bombardment) These originate from a sample volume of the order of one cubic micron, even if the beam diameter is less than a micron, due to the subsurface diffusion of the electrons from the beam. By selecting specific X-ray lines, an image of the microscopic distribution of any chemical element can be obtained. Although the Scanning Electron Microscope can be modified to detect X-rays, this is principally the domain of the Electron Probe Microanalyzer.
- Backscattered Electrons: These are beam electrons that have undergone high-angle scattering within the sample and re-emerge in a backward direction. They retain a large fraction of their original energy (of the order of 80%) depending upon the target material and original energy.

- Secondary Electrons: These are low energy electrons (less than 50v) that originate from a surface layer of the order of 50 Å thick, in the area directly affected by the electron beam. Extremely fine resolution is possible in scanning images if a fine beam is used and only the secondary electron signal is used to form the image. This is the principal operating mode of the Scanning Electron Microscope, although Electron Probe Microanalyzers can be modified to detect such signals.
- Target Current: This is what is left of the beam current after the back-scattered and secondary electrons are subtracted from it.
- Electron-Beam-Induced-Current (EBIC): This current can be collected in a circuit involving a semiconductor under electron bombardment. It is due to the creation of electron-hole pairs by the action of the beam as the high-energy beam electrons penetrate the semiconductor material.
- Cathodoluminescence (or emission of visible light under electron bombardment): The best-known cathodoluminescent device is the television screen. Many oxides, nitrides, and semiconducting compounds luminesce under electron bombardment.

Historically, electron probe microanalysis was originally concerned only with the detection and analysis of the characteristic X-ray spectrum of the sample, and scanning electron microscopy only with the detection of secondary electrons coming from the specimen. However, the electron probe has been improved to the point where current instruments can detect all but the secondary electron signal listed above, and there are a few exceptions even to this rule. In contrast, scanning electron microscopes are generally confined to the detection of secondary electrons, target current, EBIC, and (in some cases) backscattered electrons.

The principal function which the Scanning Electron Microscope performs more adequately than the Electron Probe is the detection of secondary electrons. What makes this detection mode valuable for microelectronic device studies is its ability to show up "voltage contrast" between functional parts of a planar device when potentials are applied to the device terminals. Voltage distributions on resistive elements or junctions result in changes in the effective work function of the surfaces and thus control the number of secondary electrons emitted. The brightness of any point in the presentation then represents the voltage at the corresponding point on the sample (Figure 3-24).

However, the same potential difference results in voltage contrast when sample current scans are made on an electron probe microanalyzer. While the scanning electron

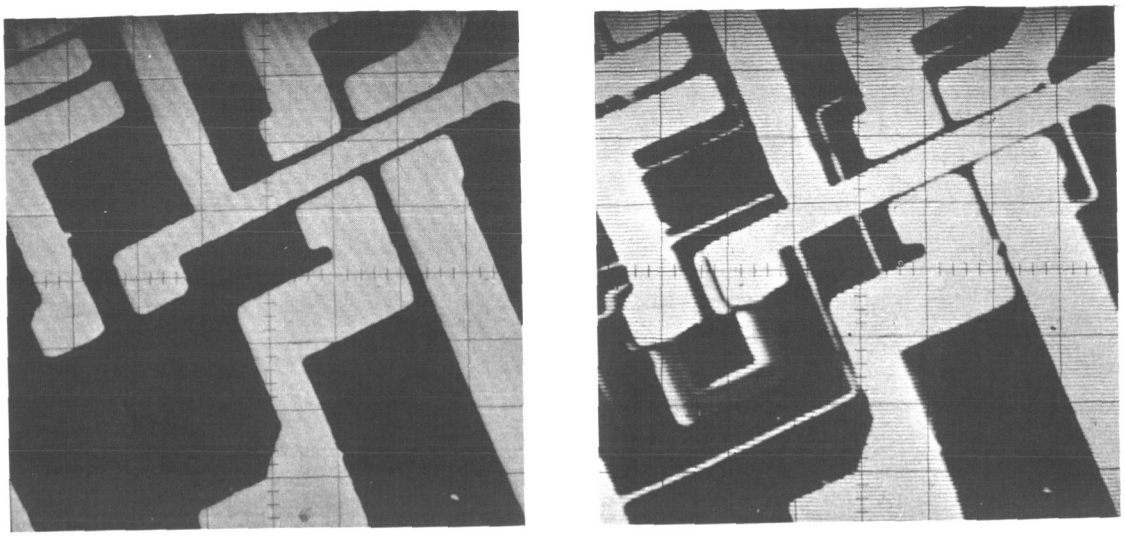


Figure 3-24 Secondary Electron Presentation Showing Voltage Contrast.

microscope is optimized for the secondary electron mode and thus possesses a higher resolution than the electron probe for voltage contrast presentation, the higher resolution is unnecessary for microelectronic devices. As an example, a target current picture of an integrated circuit obtained with a Phillips electron probe microanalyzer is shown in Figure 3-25. The resolution is obviously perfectly adequate for this device, which is typical of current circuits. In addition, the electron probe permits X-ray identification of the sample's exact chemical distributions. The device discussed above was scanned for aluminum X-rays. Figure 3-26 shows the electron probe's capability for displaying the device chemistry without destroying the specimen.

Any electron beam instrument will change the electrical characteristics of a semiconductor device under bombardment. Although this change can be controlled to some extent by the potentials applied to the circuit, any circuit that has been examined under an electron beam must be subjected to a bake-out following this step to restore its electrical performance to normal values.

### 3.6.2 Recommendations

Scanning Electron Microscopy and Electron Probe Microanalysis can be used to visually display the junction structures of any microcircuit when reverse bias is applied across the junction. Precise shapes of junctions and other structures are readily observable in sub-micron detail as are steps in the oxide layers, discontinuities and steps in the evaporated

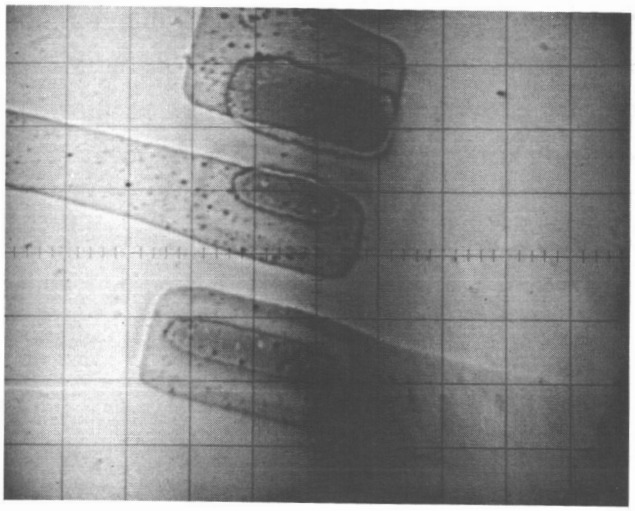


Figure 3-25 Sample Current Presentation of Microcircuit.

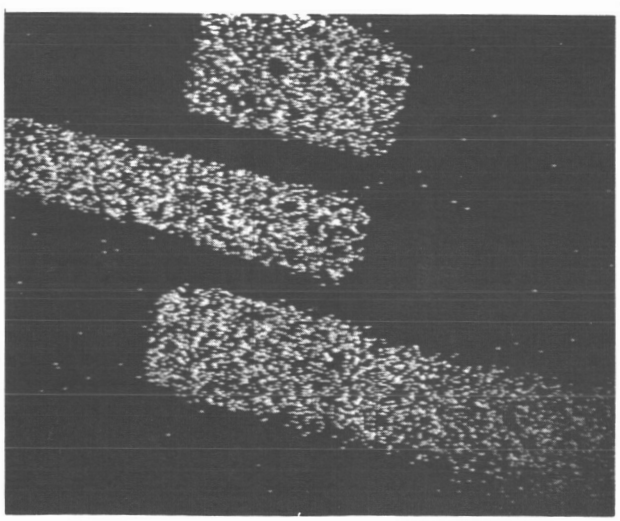


Figure 3-26 Aluminum $K_{\alpha}$ X-Ray Presentation of Microcircuit in 3-25.

leads, and dependence of junction boundaries upon biasing voltage. In addition, X-ray spectrochemical analysis using the electron probe can determine the composition of all the major structural materials; the extent of diffusion in welded or thermocompressed bonded lead attachments; the extent of overdoped junction areas; the identity of intermetallic phases formed when leads are attached to the land pads on the substrates; and the composition of all contaminants and impurities. Localization of structures and spatial resolution of such chemical analysis is approximately within 1 or 2 microns, while the localization of junction structures and surface topography for which sample current signal is employed is within a fraction of a micron.

The Electron Probe Microanalyzer is recommended for failure analysis and evaluation uses where less sophisticated techniques would not yield the information desired. It possesses the capabilities of a scanning electron microscope for showing the surface structure of any microelectronic circuit in submicron detail, with the added ability for X-ray spectrochemical analysis of the device. In many instances, it is the only technique which will permit a complete and unambiguous failure analysis.

# APPENDIX A

## TEST DATA

Samples of the test data on Fairchild, Signetics and Texas Instruments integrated circuits are contained in this appendix. This includes measurements of D.C. parameters and noise margin, post-burn-in measurements and measurements of dynamic parameters.

The large volume of data collected in the course of this study was more meaningful when subjected to suitable analysis of distributions and variables. The use of statistical programs in a computerized data analysis materially enhanced the determination of acceptability levels, evaluation of reliability, and detection of substandard devices. The computer program developed for this study, as well as a sample of the data analysis is also contained in the appendix. The program was run on a G.E. #265 Time-Sharing Computer using BASIC as the computer language.

## DYNAMIC PARAMETER TESTS ON FAIRCHILD μL930 CIRCUITS

INPUTS - Freq. - 0.5 MC
Ampl. - 2.0 V
Rise - 40 NS
Fall - 40 NS
Width - 300 NS
Pin # - 9
VCC - +4.0 V

OUTPUTS - Fan Out - 10
Load μL946
Pin #8

| Ckt. No. | Temp. | Ampl. | Rise (NS) | Fall (NS) | Storage(NS) | Delay (NS) | P.D.-1(NS) | P.D.-2(NS) |
|---|---|---|---|---|---|---|---|---|
| 1 | +25°C | 3.47 | 22 | 722 | 13 | 30 | 22 | 146 |
| 2 | | 3.62 | 25 | 690 | 14 | 32 | 26 | 133 |
| 3 | | 3.56 | 22 | 679 | 13 | 32 | 24 | 135 |
| 4 | | 3.55 | 24 | 745 | 20 | 32 | 24 | 170 |
| 5 | | 3.56 | 22 | 700 | 14 | 32 | 24 | 139 |
| | | | | | | | | |
| 1 | -55°C | 3.53 | 54 | 686 | 4 | 40 | 38 | 118 |
| 2 | | 3.59 | 70 | 666 | 6 | 45 | 46 | 111 |
| 3 | | 3.56 | 60 | 645 | 6 | 42 | 40 | 110 |
| 4 | | 3.54 | 54 | 662 | 10 | 40 | 39 | 113 |
| 5 | | 3.61 | 48 | 655 | 6 | 40 | 38 | 108 |
| | | | | | | | | |
| 1 | +125°C | 3.33 | 20 | 749 | 26 | 22 | 12 | 130 |
| 2 | | 3.57 | 20 | 718 | 28 | 24 | 14 | 115 |
| 3 | | 3.47 | 19 | 705 | 25 | 24 | 12 | 118 |
| 4 | | 3.47 | 22 | 753 | 30 | 23 | 14 | 155 |
| 5 | | 3.48 | 20 | 718 | 22 | 22 | 14 | 117 |

## WORST-CASE NOISE IMMUNITY TESTS FOR FAIRCHILD μL930 CIRCUITS

INPUTS - Freq. - 1.0 KC
Ampl. - 0 to 3.0 V
Duty Cycle - 50%
Rise Time - 10 NS
VCC = +4.0 V

OUTPUTS - Fan Out - 10
Load μL946

| Ckt. No. | Temp. | High | Low | 1 | 2 | 3 | 4 |
|---|---|---|---|---|---|---|---|
| 1 | +25°C | 2.29 | .927 | 3.85 | .221 | 1.15 | 1.53 |
| 2 | | 2.30 | 1.02 | 3.85 | .120 | 1.15 | 1.54 |
| 3 | | 2.29 | .980 | 3.85 | .179 | 1.16 | 1.65 |
| 4 | | 2.28 | 1.01 | 3.84 | .135 | 1.15 | 1.54 |
| 5 | | 2.30 | .980 | 3.84 | .167 | 1.15 | 1.54 |
| | | | | | | | |
| 1 | -55°C | 1.99 | 1.26 | 3.84 | .218 | 1.48 | 1.83 |
| 2 | | 2.00 | 1.34 | 3.85 | .141 | 1.47 | 1.83 |
| 3 | | 1.99 | 1.28 | 3.84 | .203 | 1.49 | 1.84 |
| 4 | | 1.98 | 1.32 | 3.83 | .160 | 1.48 | 1.86 |
| 5 | | 2.01 | 1.30 | 3.84 | .173 | 1.47 | 1.83 |
| | | | | | | | |
| 1 | +125°C | 2.62 | .519 | 3.81 | .243 | .775 | 1.19 |
| 2 | | 2.65 | .629 | 3.83 | .121 | .761 | 1.17 |
| 3 | | 2.62 | .579 | 3.81 | .188 | .776 | 1.20 |
| 4 | | 2.62 | .612 | 3.80 | .135 | .755 | 1.16 |
| 5 | | 2.64 | .568 | 3.81 | .175 | .751 | 1.16 |
| | | | POST BURN IN 3-4-66 | | | | |
| 1 | +25°C | 1.70 | .857 | 3.30 | .261 | 1.14 | 1.51 |
| 2 | | 1.73 | .997 | 3.35 | .138 | 1.15 | 1.62 |
| 3 | | 1.73 | .927 | 3.35 | .204 | 1.15 | 1.63 |
| 4 | | 1.78 | .675 | 3.31 | .166 | .835 | 1.52 |
| 5 | | 1.75 | .929 | 3.35 | .194 | 1.16 | 1.60 |

## DYNAMIC PARAMETER TESTS ON SIGNETICS SE101G CIRCUITS

INPUTS - Freq. - 200 KC
Ampl. - 2.0 V
Rise - 30 NS
Fall - 35 NS
Width - 1000 NS
Pin # - 8
VCC - +4.0 V
VEE - -2.0 V

OUTPUTS - Fan Out -5
Load SE180J
Pin #3

| Ckt. No. | Temp. | Ampl. | Rise (NS) | Fall (NS) | Storage (NS) | Delay (NS) | P.D.-1 (NS) | P.D.-2 (NS) |
|---|---|---|---|---|---|---|---|---|
| 1 | +25°C | 3.70 | 50 | 230 | 15 | 30 | 40 | 80 |
| 2 | | 3.65 | 55 | 219 | 10 | 28 | 45 | 65 |
| 3 | | 3.69 | 45 | 223 | 15 | 30 | 45 | 70 |
| 4 | | 3.69 | 45 | 225 | 16 | 25 | 40 | 75 |
| 5 | | 3.69 | 50 | 240 | 15 | 30 | 45 | 75 |
| | | | | | | | | |
| 1 | -55°C | 3.72 | 80 | 227 | 6 | 50 | 71 | 65 |
| 2 | | 3.66 | 95 | 212 | 7 | 45 | 70 | 60 |
| 3 | | 3.72 | 75 | 220 | 9 | 45 | 70 | 64 |
| 4 | | 3.73 | 65 | 220 | 9 | 40 | 65 | 65 |
| 5 | | 3.72 | 70 | 243 | 7 | 45 | 70 | 65 |
| | | | | | | | | |
| 1 | +125°C | 3.58 | 49 | 274 | 20 | 25 | 40 | 90 |
| 2 | | 3.52 | 50 | 255 | 18 | 25 | 40 | 81 |
| 3 | | 3.58 | 45 | 252 | 20 | 25 | 40 | 85 |
| 4 | | 3.58 | 45 | 249 | 25 | 20 | 35 | 90 |
| 5 | | 3.58 | 50 | 283 | 20 | 25 | 45 | 90 |

Note: Pin #3 was connected to #4.

## WORST-CASE NOISE IMMUNITY TESTS ON SIGNETICS SE101G CIRCUITS

INPUTS - Freq. - 1.0 KC
Ampl. - 0 to 3.0 V
Duty Cycle - 50%
Rise Time – 10 NS
VCC =+4.0 V

OUTPUTS - Fan Out - 5
Load SE180J

| Ckt. No. | Temp. | High | Low | 1 | 2 | 3 | 4 |
|---|---|---|---|---|---|---|---|
| 1 | +25°C | 2.32 | .572 | 3.88 | .179 | .772 | 1.68 |
| 2 | | 2.19 | .847 | 3.87 | .240 | 1.10 | 1.69 |
| 3 | | 2.23 | .871 | 3.88 | .192 | 1.07 | 1.64 |
| 4 | | 2.29 | .845 | 3.87 | .187 | 1.04 | 1.59 |
| 5 | | 2.27 | .843 | 3.88 | .202 | 1.05 | 1.61 |
| | | | | | | | |
| 1 | -55°C | 2.05 | .832 | 3.87 | .163 | 1.00 | 1.82 |
| 2 | | 1.96 | 1.19 | 3.87 | .210 | 1.42 | 1.91 |
| 3 | | 1.98 | 1.22 | 3.87 | .165 | 1.40 | 1.89 |
| 4 | | 2.00 | 1.21 | 3.87 | .156 | 1.38 | 1.87 |
| 5 | | 1.99 | 1.20 | 3.88 | .169 | 1.38 | 1.87 |
| | | | | | | | |
| 1 | +125°C | 2.61 | .408 | 3.79 | .212 | .626 | 1.15 |
| 2 | | 2.53 | .460 | 3.78 | .276 | .746 | 1.24 |
| 3 | | 2.55 | .491 | 3.78 | .224 | .726 | 1.21 |
| 4 | | 2.59 | .447 | 3.77 | .225 | .680 | 1.17 |
| 5 | | 2.56 | .443 | 3.76 | .242 | .695 | 1.18 |
| | | | | | | | |
| | | | POST BURN IN 3-4-66 | | | | |
| 1 | +25°C | 2.41 | .308 | .388 | .160 | .467 | 1.47 |
| 2 | | 2.32 | .777 | .388 | .207 | .998 | 1.55 |
| 3 | | 2.36 | .797 | .388 | .151 | .977 | 1.51 |
| 4 | | 2.40 | .767 | .387 | .158 | .940 | 1.47 |
| 5 | | 2.38 | .767 | .388 | .173 | .957 | 1.49 |

## DYNAMIC PARAMETER TESTS ON TEXAS INSTRUMENTS SN5311 CIRCUITS

INPUTS - Freq. - 1.0 MC
Ampl. - 3.0 V
Rise - 40 NS
Fall - 40 NS
Width - 250 NS
Pin# - 10
VCC - +4.0V

OUTPUTS - Fan Out - 10N+, 10N-
Load SN535
SN531
Pin #9

| Ckt. No. | Temp. | Ampl. | Rise (NS) | Fall (NS) | Storage (NS) | Delay (NS) | P. D. -1(NS) | P. D. -2(NS) |
|---|---|---|---|---|---|---|---|---|
| 1 | +25°C | 2.84 | 121 | 65 | 34 | 21 | 71 | 56 |
| 2 | | 2.94 | 106 | 62 | 49 | 21 | 54 | 64 |
| 3 | | 2.85 | 118 | 64 | 44 | 22 | 71 | 63 |
| 4 | | 2.97 | 105 | 61 | 52 | 21 | 53 | 65 |
| 5 | | 2.98 | 106 | 63 | 50 | 20 | 54 | 63 |
| | | | | | | | | |
| 1 | -55°C | 2.74 | 166 | 54 | 30 | 25 | 87 | 51 |
| 2 | | 2.96 | 136 | 46 | 30 | 18 | 76 | 44 |
| 3 | | 2.99 | 163 | 54 | 38 | 23 | 94 | 58 |
| 4 | | 2.99 | 131 | 45 | 32 | 20 | 76 | 45 |
| 5 | | 2.95 | 134 | 46 | 35 | 21 | 79 | 49 |
| | | | | | | | | |
| 1 | +125°C | 2.95 | 139 | 78 | 34 | 17 | 58 | 60 |
| 2 | | 3.03 | 126 | 84 | 36 | 16 | 48 | 80 |
| 3 | | 2.97 | 135 | 80 | 46 | 18 | 57 | 71 |
| 4 | | 3.07 | 123 | 82 | 60 | 16 | 48 | 80 |
| 5 | | 3.07 | 122 | 83 | 56 | 16 | 45 | 79 |

WORST-CASE NOISE IMMUNITY TESTS ON TEXAS INSTRUMENTS SN5311 CIRCUITS

INPUTS - Freq. - 1.0 KC
Ampl. - 0 to 3.0 V
Duty Cycle - 50%
Rise Time - 10 NS
VCC = +4.0 V

OUTPUTS - Fan Out - 10N+10N-
Load - SN535
SN533

| Ckt. No. | Temp. | High | Low | 1 | 2 | 3 | 4 |
|---|---|---|---|---|---|---|---|
| 1 | 25°C | 1.55 | .555 | 3.07 | .071 | .631 | 1.51 |
| 2 | | 1.96 | .483 | 3.10 | .068 | .556 | 1.13 |
| 3 | | 1.79 | .509 | 3.06 | .067 | .583 | 1.26 |
| 4 | | 2.03 | .458 | 3.12 | .066 | .530 | 1.09 |
| 5 | | 2.02 | .469 | 3.11 | .056 | .534 | 1.09 |
| | | | | | | | |
| 1 | -55°C | .798 | .754 | 2.92 | .047 | .812 | 2.07 |
| 2 | | 1.54 | .700 | 2.96 | .029 | .733 | 1.45 |
| 3 | | 1.35 | .725 | 2.91 | .033 | .758 | 1.54 |
| 4 | | 1.68 | .676 | 2.99 | .031 | .703 | 1.29 |
| 5 | | 1.65 | .688 | 2.96 | .022 | .715 | 1.37 |
| | | | | | | | |
| 1 | 125°C | 1.73 | .363 | 3.21 | .096 | .466 | 1.47 |
| 2 | | 2.21 | .288 | 3.24 | .094 | .388 | 1.02 |
| 3 | | 2.02 | .324 | 3.20 | .093 | .424 | 1.17 |
| 4 | | 2.29 | .269 | 3.26 | .092 | .367 | 0.960 |
| 5 | | 2.30 | .274 | 3.26 | .082 | .361 | 0.955 |
| | | | POST BURN IN 3-2-66 | | | | |
| 1 | 25°C | 1.93 | .608 | 3.03 | .096 | .747 | 1.35 |
| 2 | | 2.19 | .531 | 3.06 | .098 | .674 | 0.979 |
| 3 | | 2.00 | .585 | 3.02 | .099 | .704 | 1.10 |
| 4 | | 2.26 | .537 | 3.02 | .098 | .648 | 0.921 |
| 5 | | 1.98 | .587 | 3.07 | .087 | .642 | 0.908 |

MICROCIRCUIT VARIABLES ANALYSIS COMPUTER PROGRAM

```
1   PRINT"                MICROCIRCUIT STATISTICAL ANALYSIS"
2   PRINT
3   PRINT
4   PRINT
5   PRINT
10  LET H=0
10  DIM M(50)
10  DIM N(50)
10  DIM D(50)
10  READ C
10  IF C=0 THEN 300
10  LET H=H+1
15  LET N(H)=C
20  LET S1=0
20  LET S2=0
20  FOR T=1 TO C
20  READ X
20  LET S1=S1+X
20  LET S2=S2+X*X
20  NEXT T
20  LET M(H)= S1/C
20  LET V=(S2-M(H)*S1)/C
25  LET D(H)=SQR(V)
20  GO TO 160
30  RESTORE
30  LET B=0
30  LET G=0
30  LET L=0
30  LET K=0
30  READ G
30  IF G=0 THEN 460
30  LET K=K+G
30  LET L=L+1
```

```
30  FOR U=1 TO G
40  READ X
40  LET Y=X/M(L)
40  LET Z=Y*Y
40  LET B=B+Z
40  NEXT U
40. GO TO 350
40  LET E=B/K-1
40  LET F=SQR(E)
40  PRINT"       STANDARD DEVIATION OF NORMALIZED GROUP="F
40  PRINT
50  PRINT
50  PRINT" TYPE NO.", "NO. IN GROUP", "MEAN", "STD. DEV.", "PROJECTED S.D."
50  PRINT
50  PRINT
50  FOR W=1 TO L
51  LET A=M(W)
52  LET O=D(W)
53  LET A=INT(10↑3*A+.5)/10↑3
54  LET P=M(W)
50  PRINT" ";W, N(W), A, INT(10↑4*0+.5)/10↑4, INT(10↑4*P*F+.5)/10↑4
50  PRINT
50  NEXT W
50  PRINT
50  PRINT
60  PRINT
60  PRINT
60  PRINT"                              INPUT DATA:"
61  PRINT
62  PRINT
63  PRINT
65  RESTORE
60  LET I=0
60  LET I=I+1
```

```
60  READ C
65  IF C=0 THEN 9999
60  PRINT "  TYPE NO."; I
60  PRINT
60  PRINT "  NUMBER OF THIS TYPE:"; C
60  PRINT
70  PRINT "  MEASURED VALUE:"
75  PRINT
70  FOR J=1 TO C
70  READ X
70  PRINT "  ",X
70  NEXT J
70  PRINT
70  PRINT
70  GO TO 640
9999  END
```

## COMPUTER DATA ANALYSIS OF T.I. SERIES 53 PRE BURN IN NOISE IMMUNITY FOR $V_{IN}$ - HIGH READINGS

RUN 13:24 NY FRI 04/15/66

MICROCIRCUIT STATISTICAL ANALYSIS

INPUT DATA:

```
100  DATA 5, 1.51, 1.13, 1.26, 1.09, 1.09, 5, 1.00, 1.11, 1.07, .982, .971
101  DATA 5, 1.12, 1.10, 1.12, 1.14, 1.11, 5, .965, 1.07, .970, .998, 1.09
102  DATA 5, 1.24, 1.07, 1.22, 1.04, 1.18, 4, 1.34, 1.46, 1.60, 1.44
103  DATA 5, 1.34, 1.39, 1.28, 1.20, .974, 0
```

OUTPUT DATA:

STANDARD DEVIATION OF NORMALIZED GROUP= 8.11562 E-2

| TYPE NO. | NO. IN GROUP | MEAN | STD. DEV. | PROJECTED S.D. |
|---|---|---|---|---|
| 1 | 5 | 1.216 | .1597 | .0987 |
| 2 | 5 | 1.027 | .0541 | .0833 |
| 3 | 5 | 1.118 | .0133 | .0907 |
| 4 | 5 | 1.019 | .0518 | .0827 |
| 5 | 5 | 1.15 | .0805 | .0933 |
| 6 | 4 | 1.46 | .0927 | .1185 |
| 7 | 5 | 1.237 | .1459 | .1004 |

## COMPUTER DATA ANALYSIS OF T.I. SERIES 53 POST BURN IN NOISE IMMUNITY FOR $V_{IN}$ - HIGH READINGS

RUN 13:37 NY FRI 04/15/66

MICROCIRCUIT STATISTICAL ANALYSIS

INPUT DATA

```
100  DATA 5, 1.35, .979, 1.10, .921, .908, 4, .992, .954, .845, .850
101  DATA 5, .887, .869, .908, .924, .870, 5, .820, .937, .803, .845, .964
102  DATA 5, 1.06, .864, 1.02, .824, .994, 4, .985, 1.05, 1.20, 1.11
103  DATA 5, .982, 1.08, 1.01, .942, .790, 0
```

OUTPUT DATA

STANDARD DEVIATION OF NORMALIZED GROUP= 9.37187 E-2

| TYPE NO. | NO. IN GROUP | MEAN | STD. DEV. | PROJECTED S.D. |
|---|---|---|---|---|
| 1 | 5 | 1.052 | .1639 | .0986 |
| 2 | 4 | .91 | .0642 | .0853 |
| 3 | 5 | .892 | .0215 | .0836 |
| 4 | 5 | .874 | .0646 | .0819 |
| 5 | 5 | .952 | .0918 | .0893 |
| 6 | 4 | 1.086 | .0792 | .1018 |
| 7 | 5 | .961 | .0965 | .09 |

## APPENDIX B

## BIBLIOGRAPHY

The following bibliography contains a listing of all reliability data, technical reports and specifications which were used as basic reference documents throughout this program. Part of this material was gathered prior to the contract, and provided background information and justifications for the selection of companies to be visited as part of the study phase. The balance was obtained as a result of the visits and contacts made during the study phase.

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