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NONDISSIPATIVE OPTIMUM CHARGE REGULATOR ADVANCED STUDY

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AEROSPACE GROUP

HUGHES

HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

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TABLES

1.0 INTRODUCTION

This report summarizes the work accomplished during the first six months of a one-year program in the design, development, and testing of multiphase, nondissipative optimum charge regulators. This program is a continuation of the work done on Contract NAS 5-9210. This previous effort was concerned with the development of the basic circuits required for the efficient transfer of power from a spacecraft solar array to a spacecraft type battery. The continuation of effort during the present program is for the purpose of improving the basic designs in order to improve their efficiency and reliability.

Extension of the level of research and development effort from the previous program includes the following:

1. Construction of a two- and a four-phase optimum charge regulator to demonstrate the feasibility for improved efficiency and reliability.
2. Study all aspects of multiple phase regulators with particular attention to continued operation in the event of one phase becoming inoperative.
3. Perform worst case and failure mode analysis on all circuits in order to determine reliability problem areas.
4. Construct mathematical models for each circuit block to indicate critical design areas and demonstrate where redundancy may best be employed.
5. Study third-electrode charge control devices and their application to optimum charge controllers.

1.1 SUMMARY OF EFFORT DURING THE FIRST HALF OF THE PROGRAM

During the first six months of development, the 50-watt, single-phase regulator, and the 250-watt, two-phase regulator, which were designed for Contract NAS5-9210, were redesigned. These units were modified to include a two-phase switching circuit for the 50-watt unit, and a four-phase switching circuit for the 250-watt unit. Photographs

of these breadboards are shown in Figure 1-1 and 1-2. The basic switching circuit and duty factor modulator circuit operation is the same as in the original design except for the additional phases. The balance of the circuits in the control loop were simplified to increase reliability and reduce total parts count.

The switching transformers were redesigned in an effort to reduce the core losses which contributed to the overall system inefficiency in the original design.

1.2 SUMMARY OF RESULTS

Testing of the 50-watt and 250-watt regulators at room temperature indicated satisfactory operation over all the extremes of input and output conditions, including the -30 percent power transient. Stable tracking of the maximum power point during this condition was observed. A decrease in the losses due to hunting was also found.

Efficiency measurements indicated the 50-watt regulator exceeded its goal of 85 percent. The 250-watt regulator came very close to its goal of 90 percent; an additional change in the construction of the switching transformer could possibly result in reaching this goal. The major reason for the efficiency improvement in both units was traced to the improved switching transformer design. Use of powdered iron cores in the transformer construction allowed the switching circuits to be compensated, so as to provide a resistive switching load line instead of the previously inductive load line. This allowed the switching losses to be reduced by a factor of about six. The increase in the number of phases also aided in the efficiency improvement by reducing the peak currents drawn by the switching circuit.

A battery study has been proposed to determine the best means of operating a third electrode charge control device with the optimum charge regulator. Results will be available in the final report.

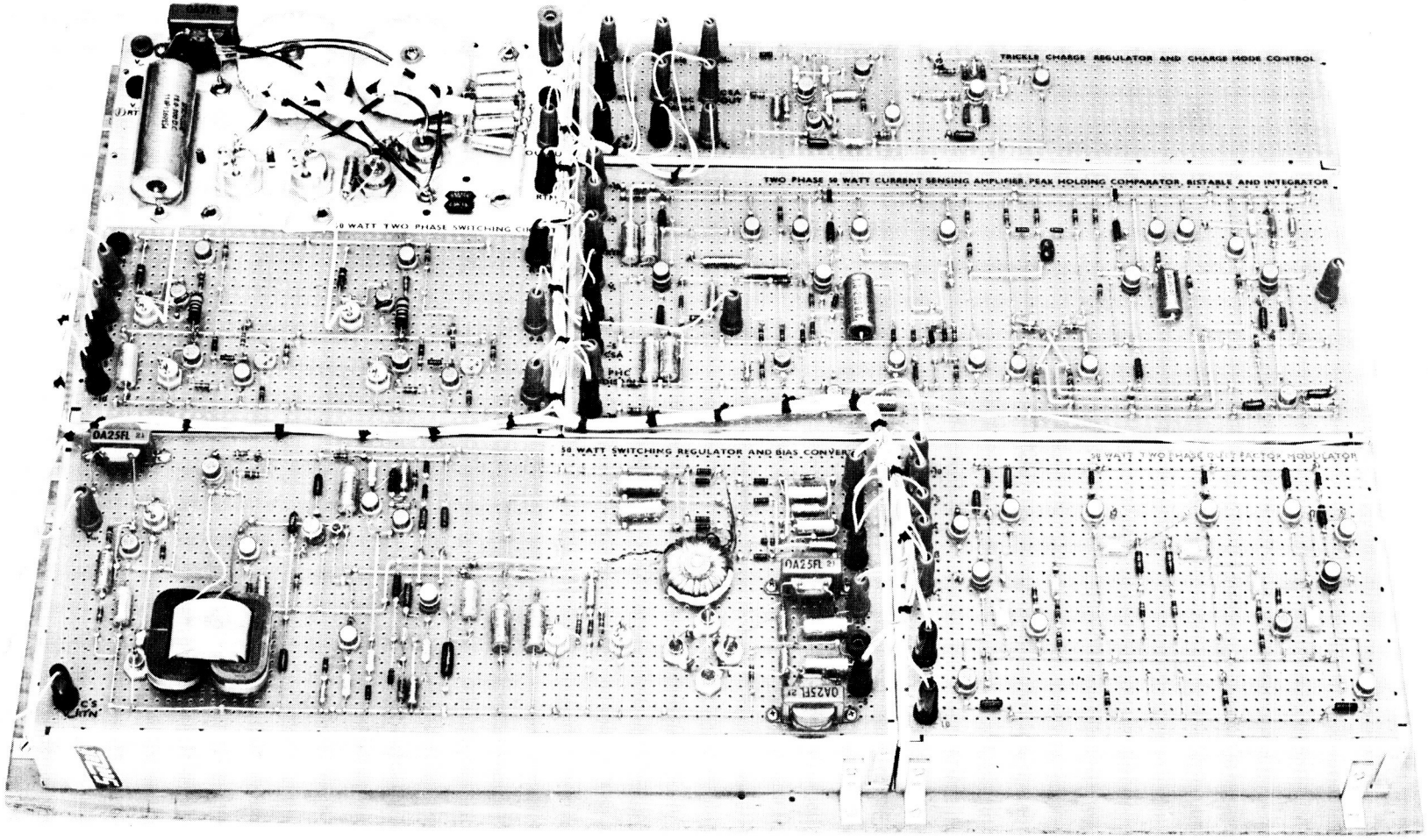


Figure 1-1. Fifty-watt, two-phase optimum charge regulator breadboard. (HAC Photo R113900)

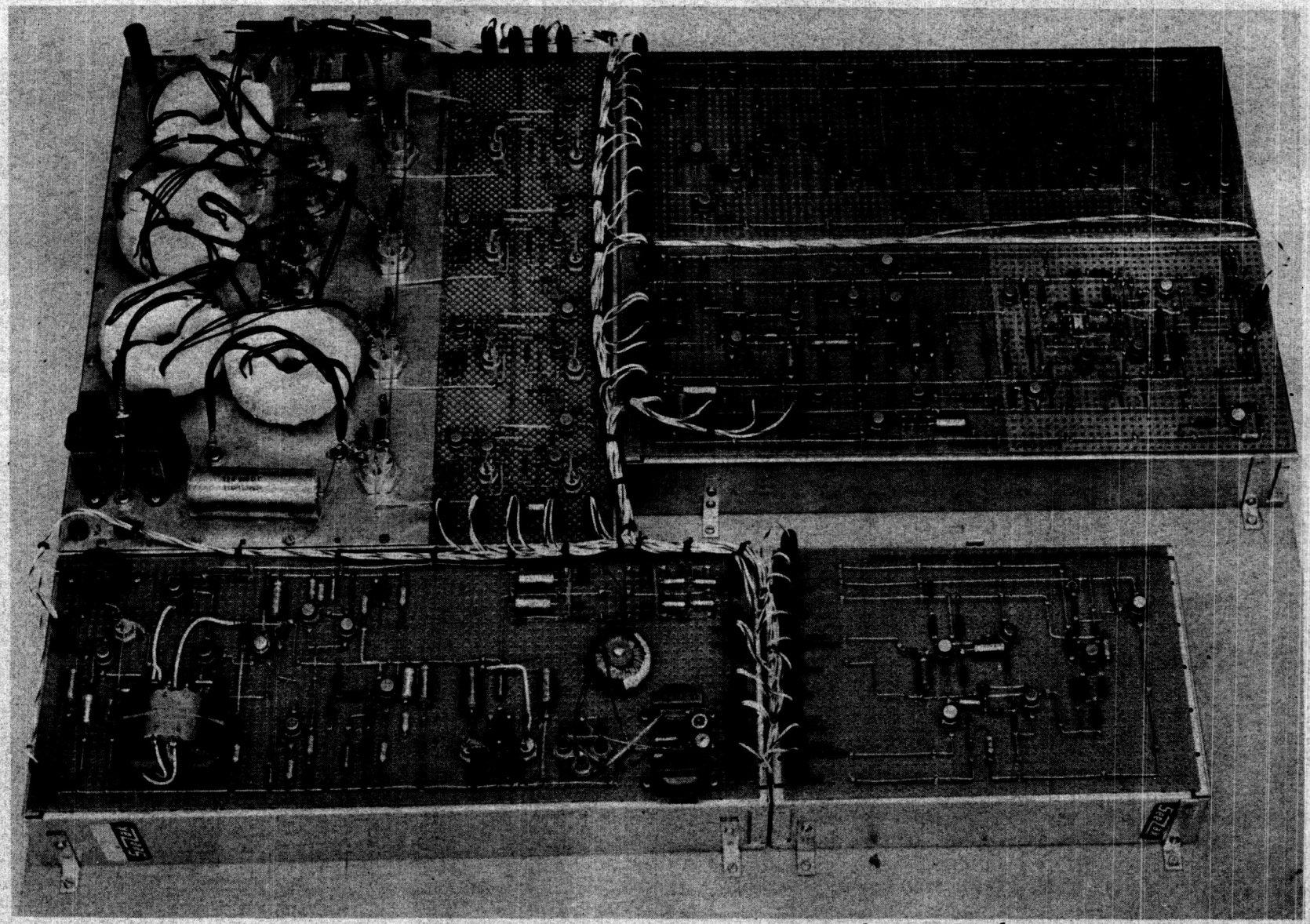


Figure 1-2. 250-watt, four-phase optimum charge regulator breadboard. (HAC Photo R113899)

1.3 PROPOSED EFFORT FOR THE REMAINDER OF THE PROGRAM

There are several tasks that will be performed during the second half of the program. They will verify whether the reliability and stability goals, as well as the efficiency goals, required for the assurance of long lifetime mission success, have been accomplished. The following is a work schedule that will be performed during the next six months:

1.3.1 Mathematical Models and Block Diagrams

Mathematical models and block diagrams will be developed to indicate critical design areas and demonstrate where redundancy may be employed to improve reliability. The current sensing amplifier was chosen as the first circuit block to be analyzed. Work has started on the derivation of its transfer function in order to determine the gain and phase characteristics under all conditions.

1.3.2 Worst Case Analysis

Worst case analysis will be performed on all circuits in an effort to determine whether normal operation can proceed under all worst case solar panel, battery, temperature and aging variations. (This analysis will be performed for the following conditions: Maximum and minimum semiconductor parameter variations; ±20 percent resistance variation for all ±5 percent resistors; ±5 percent resistance variation for all ±1 percent resistors; +20 percent and -50 percent variation in capacitance for all capacitors; ±10 percent in inductance variation for all inductors; twice the maximum and minimum specified variation for all other components.)

1.3.3 Failure Mode Analysis

Failure mode analysis will determine the effect on mission success of the different components used in the optimum charge regulator. This will indicate which modes of circuit failures are more likely to occur and which components directly affect these failures. This analysis will indicate where redundancy might best be employed to improve circuit reliability. These modifications will be discussed in detail in the final report but no actual breadboard modifications are expected to be required.

1.3.4 Temperature Testing

Temperature testing will be completed on the 50-watt and 250-watt regulators to verify whether the efficiency goals were attained over the temperature range of -40°C to +70°C, and to ensure proper operation over the temperature extremes.

1.3.5 Third Electrode Battery Study

The third electrode battery study will determine a means of operating a third electrode charge control device with the optimum charge regulator. The first phase of the study will be to test third electrode batteries to determine their output signal characteristics for various charging rates. The final phases will be concerned with the design of the OCR control circuitry and its evaluation.

1.3.6 Multiphase Operation

The final goal of the program is the development of the necessary circuit modifications that are required to maintain normal, reliable operation of multiphase regulators if one or more phases become inoperative.

2.0 EFFICIENCY DISCUSSION

2.1 TWO-PHASE, 50-WATT REGULATOR

Efficiency and dissipation measurements were made on the two-phase, 50-watt unit to determine how much of an improvement was made in going from the original single-phase design to a two-phase system. Measurements were made at room temperature. The temperature evaluation will be completed during the final portion of the program. Data was taken over several days to ensure accurate and consistent readings. The methods used to make the power loss measurements are detailed in the following paragraphs. The major dissipation areas are discussed and the techniques used for measuring the power loss are detailed. A summary of all major dissipation areas is shown in Table 2-1. This table compares the power loss in the present two-phase unit to that of the original single-phase unit. Figure 2-1 is a block diagram of the OCR, and it indicates the dissipation in each major circuit block of the regulator.

2.1.1 Efficiency Measurement Technique

The solar panel simulator was set at an open circuit voltage (temperature) of 30 volts, and a short circuit current (illumination) of approximately 2.2 amperes. Current limiting of the simulator was set at its maximum. Degradation and rounding was set at their minimum values.

The battery simulator was adjusted for a battery voltage of 12 volts. A Hewlett-Packard digital voltmeter Model 3440A was used to measure the battery and solar panel voltages.

With the OCR optimum charging the battery, the solar panel output current was adjusted for 2.0 amperes. This was accomplished by monitoring the voltage across resistor R_A, as shown in Figure 2-2. A Calibration Standards Corporation precision differential dc voltmeter, model DC-110B, was used to measure V_{RA} and V_{RB} (see Figure 2-2). Resistors R_A and R_B were both about 20 milliohms and were calibrated before any testing was done.

Dissipation Area	Power Loss, watts	Power Loss, watts
	Two-Phase OCR	Single-Phase OCR
Switching circuit bias power	0.79	1.20
Total saturation	0.22	0.68
Total switching	0.70	2.63
Input filter inductor	0.24	0.80
Fly back diode	0.26	0.68
Sensing resistor	0.52	0.68
Switching transformers		
Copper	0.12	1.36
Core	2.95	1.54
Duty factor modulator	0.06	0.14
Current sensing amplifier, peak holding comparator, bistable and integrator	0.17	0.16
Switching regulator bias converter	0.85	1.63
Hunting loss	0.12	0.50
Total	7.00	12.00
Efficiency = η = 86 percent		η = 76 percent
Maximum available power = 50 watts		

Table 2-1. Summary and comparison of major dissipation areas for the 50-watt, two-phase OCR and the 50-watt, single-phase OCR.

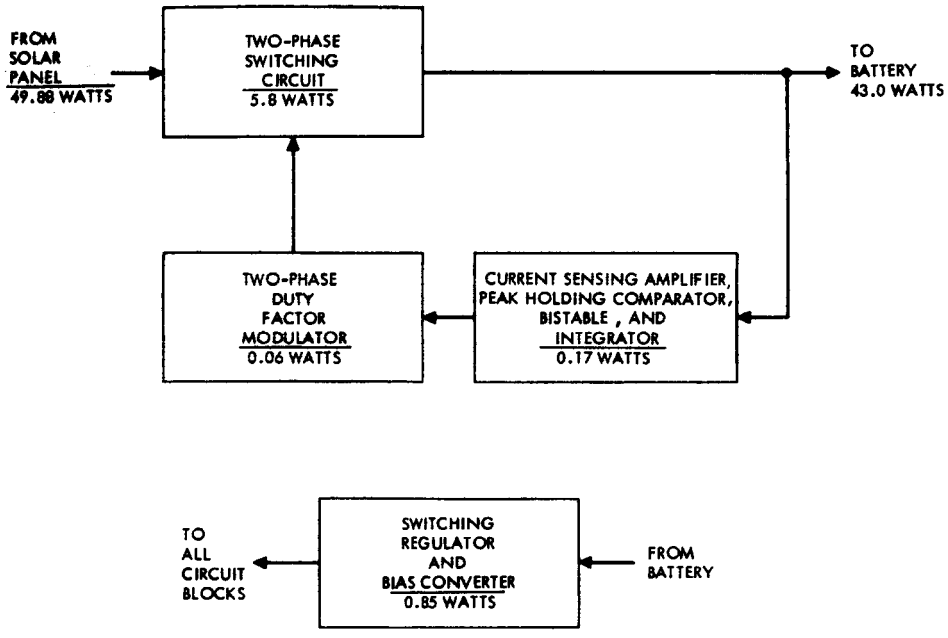


Figure 2-1. Fifty-watt, two-phase OCR block diagram and dissipation summary.

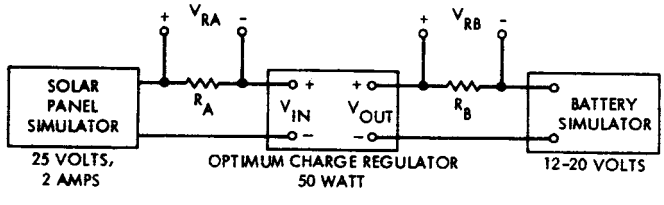


Figure 2-2. Efficiency measurement test setup.

Efficiency was computed using the following relationship:

$$\text{Efficiency percent} = \left[\frac{V_{RB} \times V_{BAT}}{R_B} \Big/ \frac{V_{RA} \times V_{SP}}{R_A} \right] \times 100$$

$$= \frac{V_{RB} \times V_{BAT}}{V_{RA} \times V_{SP}} \times 100 \qquad (2\text{-}1)$$

where

V_{SP} = solar panel voltage

V_{BAT} = battery voltage

V_{RA} = voltage across R_A

V_{RB} = voltage across R_B

R_A, R_B = current sensing resistor

(Note: Due to the difference in the exact resistances of R_A and R_B, a correction was made in the final calculation of power losses.)

The procedure was repeated at battery voltages of 14, 16, 18, and 20 volts. Readings were repeated several times at each battery voltage to ensure accuracy. The results can be found in Table 2-2.

V_{Bat}, volts	Efficiency, percent
12	83.4
14	84.4
16	84.9
18	85.2
20	86.1

Table 2-2. Fifty-watt, two-phase regulator efficiency for varying battery voltage.

As shown by this table, the efficiency is maximum at maximum battery voltage and decreases as the battery voltage is lowered. This is due to the increase in average battery current as the battery voltage decreases. This increased current results in greater I^2R losses in the switching circuit secondary. For this reason, the efficiency is best at high battery.

2.1.2 Hunting Loss Measurement

Upon completion of the efficiency measurements, the loss due to hunting was then measured.

A 20K trimpot was connected between the +5 volt and -5 volt bias inputs to the duty factor modulator with the center tap connected to the integrator input.

The integrator input to the duty factor modulator was disconnected and the trimpot was adjusted until the current delivered to the battery was at a maximum.

The hunting loss was computed by taking the difference between the power delivered to the battery during normal OCR operation and the power delivered when the OCR was manually adjusted to operate at the maximum power point.

2.1.3 Switching Regulator and Bias Converter

In order to determine where the power in the optimum charge regulator was being dissipated, it was necessary to know how much bias current was being drawn from the bias converter, and also how much power was being dissipated within the switching regulator and bias converter. The dissipation was found by subtracting the total output bias power from the total input power. The input power measurement was made at a battery voltage of 20 volts, since this represents the worst case input for the switching regulator.

2.1.4 Switching Circuit Losses

Since this circuit dissipates over 80 percent of the total power lost, a detailed discussion of each component loss is included in this

paragraph. Figure 2-3 is a basic schematic diagram of this circuit, and it summarizes each power loss for the individual components.

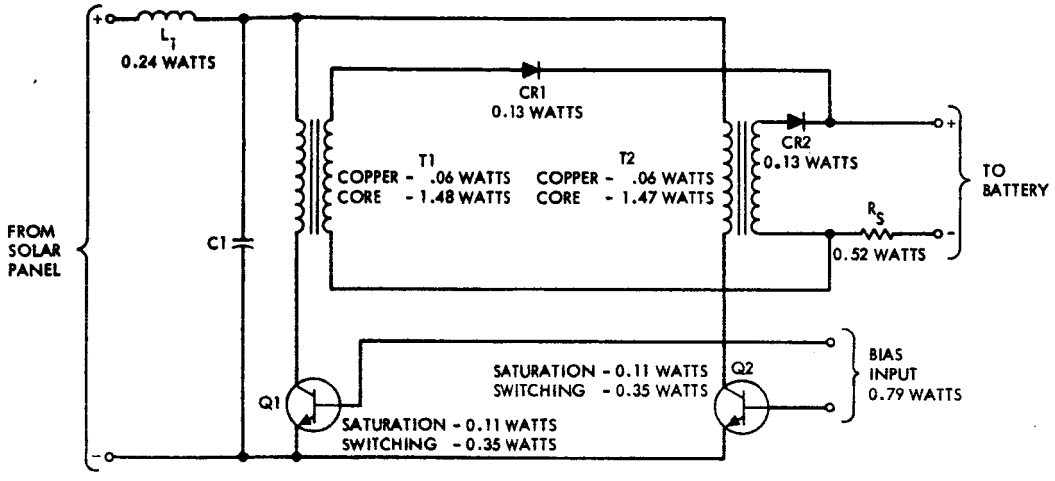


Figure 2-3. Fifty-watt, two-phase switching circuit basic schematic diagram and dissipation summary.

2.1.4.1 Bias Power. The total power delivered by the bias converter to the switching circuit and to the duty factor modulator (DFM), current sensing amplifier (CSA), peak holding comparator (PHC), bistable and integrator circuits was found to be 1.02 watts. This is 0.48 watt less total bias power loss than in the single-phase circuit. The two-phase switching circuit was found to dissipate 0.79 watt This is a total of 0.41 watts less than in the previous design. This is due to the fact that less base drive is required for the two-phase switching circuit power transistors, because of their higher current gain at the lower peak currents which are now drawn.

2.1.4.2 Switching Transistor Saturation Losses. The total saturation losses of Q1 and Q2 were found to be 0.22 watt. This is 0.46 watts less than the previous single-phase system. This is a result of reducing the peak primary current in the switching transformers from 18 amperes to 6 amperes. A saturation resistance of 0.03 ohm for Q1 and Q2, and a duty factor of 0.3 was used in Equation 2-3 to derive a total saturation loss of 0.22 watt.

$$P_{SAT} = \frac{RI_P^2 D\phi}{3} \qquad (2-3)$$

where

R = saturation resistance

I_P = peak primary current

D = duty factor

ϕ = number of phases

2.1.4.3 Switching Transistor Switching Losses. This loss was approximated using the switching waveforms shown in the photograph of Figure 2-4. The photograph shows the collector-emitter voltage and the collector current of both Q1 and Q2 at the moment of "turn-off".

The power is approximated by breaking the waveforms into segments. For transistor Q1, the voltage begins rising at t = 0.375 microsecond. It rises to about 20 volts in the next 0.05 microsecond while the current remains at 6 amperes.

Therefore

$$P(0.375 - 0.425 \text{ microsecond}) = \frac{10 \times 6 \times 0.05}{100} = 0.03 \text{ watts}$$

For the next 0.05 microsecond, the voltage rises to 50 volts while the current drops to about 5 amps.

Therefore

$$P(0.425 - 0.475 \text{ microsecond}) = \frac{35 \times 5.5 \times 0.05}{100} = 0.096 \text{ watt}$$

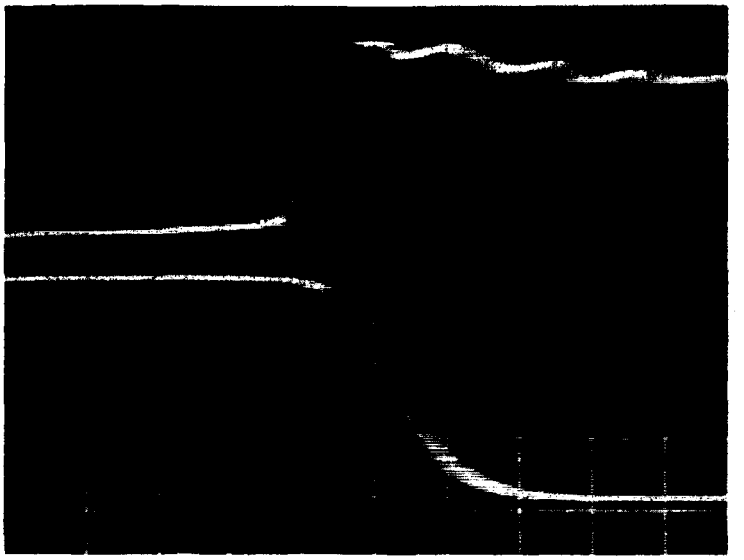
Finally, the voltage remains at 50 volts while the current drops to zero during the next 0.20 microsecond.

Therefore

$$P(0.475 - 0.675 \text{ microsecond}) = \frac{50 \times 2.25 \times 0.2}{100} = 0.225 \text{ watt} \quad .$$

(a) V_{ce} (Q1)

(b) I_c (Q1)



(c) V_{ce} (Q2)

(d) I_c (Q2)

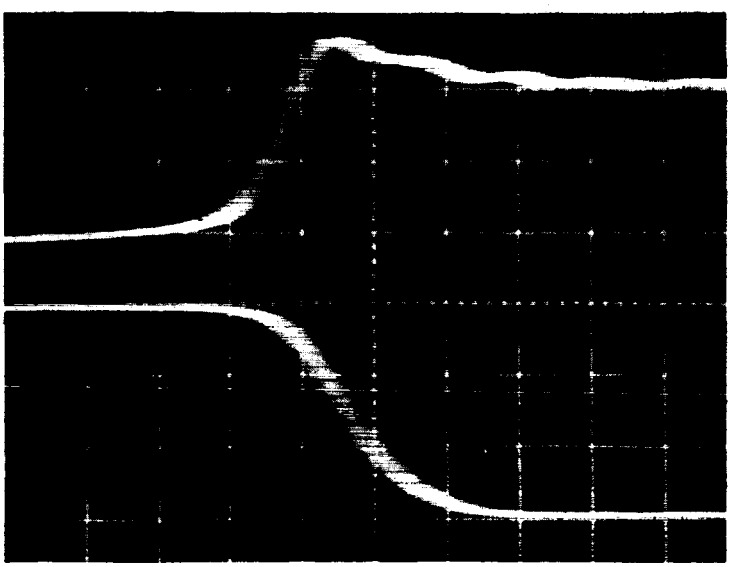


Figure 2-4. Voltage and current waveforms for calculating the switching losses of switching transistors Q1 and Q2 in the 50-watt, two-phase OCR.

Vertical: (a) and (c) - 20 volts per centimeter
(b) and (d) - 2 amperes per centimeter

Horizontal: 0.1 microsecond per centimeter

The power lost due to switching in Q1 is 0.35 watt. If Q2 is assumed to have approximately the same waveforms, then the total switching loss is found to be 0.7 watt. This is considerably less than the switching loss incurred in the single-phase OCR. These losses were about four times greater. The improvement can be attributed to the reduction in the peak current seen by the switching transistors, and to the improved transformer design. The reduction of the peak current and the use of the powdered iron core aided in reducing the switching time by about a factor of two. The reduction of the peak current also reduced the switching losses, which are a function of the V-I product.

2.1.4.4 Input Filter Inductor - L1. The dc drop across L1 was determined to be 0.12 volt at a current of 2 amperes. The power dissipated is thus 0.24 watts. A savings of 0.56 watts was obtained by reducing the series resistance of L1. This design area can be optimized with regard to both power loss and size as discussed in paragraph 3.6.2.

2.1.4.5 Flyback diode - CR1 and CR2. This loss can be approximated using Equation 2-3. Using the values R = 0.03 , I_p = 6 amperes, and D = 0.36, the power loss is found to be 0.26 watts. The peak current was reduced from 12 amperes in the single-phase OCR to 6 amperes in the two-phase OCR, which reduced the power losses in the flyback diodes by 0.42 watt.

2.1.4.6 Sensing Resistor - R_S. The power lost in the sensing resistor, R_S, is twice the total power lost in CR1 and CR2, since the resistance of each diode is about the same as R_S, and each diode handles one-half the current. The power dissipated in R_S is 0.52 watt.

2.1.4.7 Switching Transformer - Copper. The series resistance of the switching transformer is 0.015 ohm in the primary and 0.015 ohm in the secondary. Therefore, it will have one-half the losses for the combination of the saturated Q1 and Q2 condition and the losses found for

CR1 and CR2. The total copper loss was found to be 0.12 watt, or an improvement of 1.24 watts over the single-phase OCR.

This savings was due mainly to the lower currents in the primary and secondary windings, and to the reduced series resistance of the switching transformers.

2.1.4.8 Switching Transformer - Core Loss. The core loss is determined by taking the difference between the measured losses and the total power loss as determined from $P_{IN} - P_{OUT}$. This is the technique presently employed for measuring this loss. The core loss was determined to be 2.95 watts.

2.1.5 Switching Regulator/Bias Converter Losses

The losses in the switching regulator and bias converter are determined by taking the difference between the input and output power of this circuit. The total power dissipated in the switching regulator and bias converter was found to be 0.85 watt. This is approximately one-half the power that was previously lost in the single-phase system. The savings is primarily due to less total bias power required by the duty factor modulator, and decreased drive required for Q1 and Q2.

2.1.6 Summary

A comparison of the results of the original single-phase OCR and the new two-phase system (Table 2-1) clearly shows that less power is dissipated in most of the major areas within the two-phase OCR. The total power loss is 7.00 watts compared to 12.0 watts in the original design. As a result, 5.0 watts additional power can be delivered to the battery, which represents an efficiency increase of 10 percent over the single-phase design. The original design goal of 85 percent was met at room ambient temperature. It is felt that 85 percent is attainable over the entire temperature range. Further temperature testing will be conducted during the next part of the program.

2.2 FOUR-PHASE 250-WATT REGULATOR

The original design goal of 90 percent was nearly achieved with a measured efficiency of 88.0 percent. The switching transformer redesign resulted in a net reduction of over 6 watts in core loss. It is felt that further reduction in losses in this major dissipation area can be achieved in further studies to be conducted as explained in paragraph 3.4.

The method of efficiency measurements in the four-phase, 250-watt regulator is basically the same as performed for the two-phase, 50-watt regulator. The open circuit voltage was set at 50 volts, and the short circuit current adjusted for approximately 6.5 amperes. Efficiency measurements were taken at battery voltages of 25, 30, 35, and 40 volts. Efficiency was computed using Equation 2-1. Table 2-3 summarizes the unit efficiency for various battery voltages. The decreased efficiency at low battery was found to be caused by the increased I^2R losses due to the higher battery current drawn during this condition.

V_{BAT}, volts	Efficiency, percent
25	87.1
30	87.6
35	87.7
40	88.0

Table 2-3. 250-Watt, four-phase regulator efficiency for varying battery voltage.

Hunting loss measurements were also taken in the same manner as for the 50-watt unit. Table 2-4 summarizes the major dissipation areas and compares them to the original 250-watt, two-phase design.

Dissipation Area	Power Loss, watts	Power Loss, watts
	Four-Phase OCR	Two-Phase OCR
Switching circuit bias power	4.12	3.10
Total saturation	1.15	1.00
Total switching	2.25	2.80
Input filter inductor	1.19	2.10
Output filter inductor		1.70
Flyback diode	0.82	1.10
Sensing resistor	1.64	2.10
Switching transformers		
Copper	1.00	4.20
Core	13.88	20.00
Duty factor modulator	0.11	0.10
Current sensing amplifier, peak holding comparator, bistable and integrator	0.17	0.10
Switching regulator and bias converter	2.75	1.70
Hunting loss	0.92	4.00
Total	30.00	44.00
Power input = 250 watts		
	η = 88 percent	η = 82.5 percent

Table 2-4. Summary and comparison of major dissipation areas for the 250-watt, two-phase OCR and the 250-watt, four-phase OCR.

3.0 CIRCUIT DESIGN DESCRIPTION

The three basic areas of modification within the new 50-watt and 250-watt optimum charge regulators are the following:

a. A two-phase and four-phase switching circuit and duty factor modulator for the 50-watt and 250-watt OCR, respectively
b. The use of redesigned switching transformers
c. Simplification of the circuitry within the balance of the optimum controller

The three areas mentioned above have contributed to both increased efficiency and reliability. A worst case and failure mode analysis will be performed during the next portion of the program to show in detail the OCR operation under worst case conditions. These conditions include variations in solar panel and battery voltages, and changes in the temperature.

3.1 TWO-PHASE SWITCHING CIRCUIT - 50-WATT OCR

The switching circuit is the most important block within the optimum charge regulator in terms of efficiency, because it is this circuit that transfers the power from the solar panel to the battery. Figure 3-1 is a schematic diagram of this circuit.

The two-phase switching circuit employs two single-phase switching circuits in tandem. Each of these circuits transfers only one-half of the total power. They are operated 180 degrees out of phase so as to reduce the input and output ripple. This causes the effective ripple frequency, due to switching, to be twice the primary switching frequency rate, allowing for considerable reduction in input filter size.

The two-phase design uses an improved switching transformer design with a turns ratio of 1:1 (see Table 3-1). The old design had a 1:1.5 turns ratio. By employing two phases, and with the transformer improvement, the peak current in the primary is reduced from 18 amperes to 6 amperes. A 1:1 turns ratio is the optimum design, since maximum coupling between windings can be achieved.

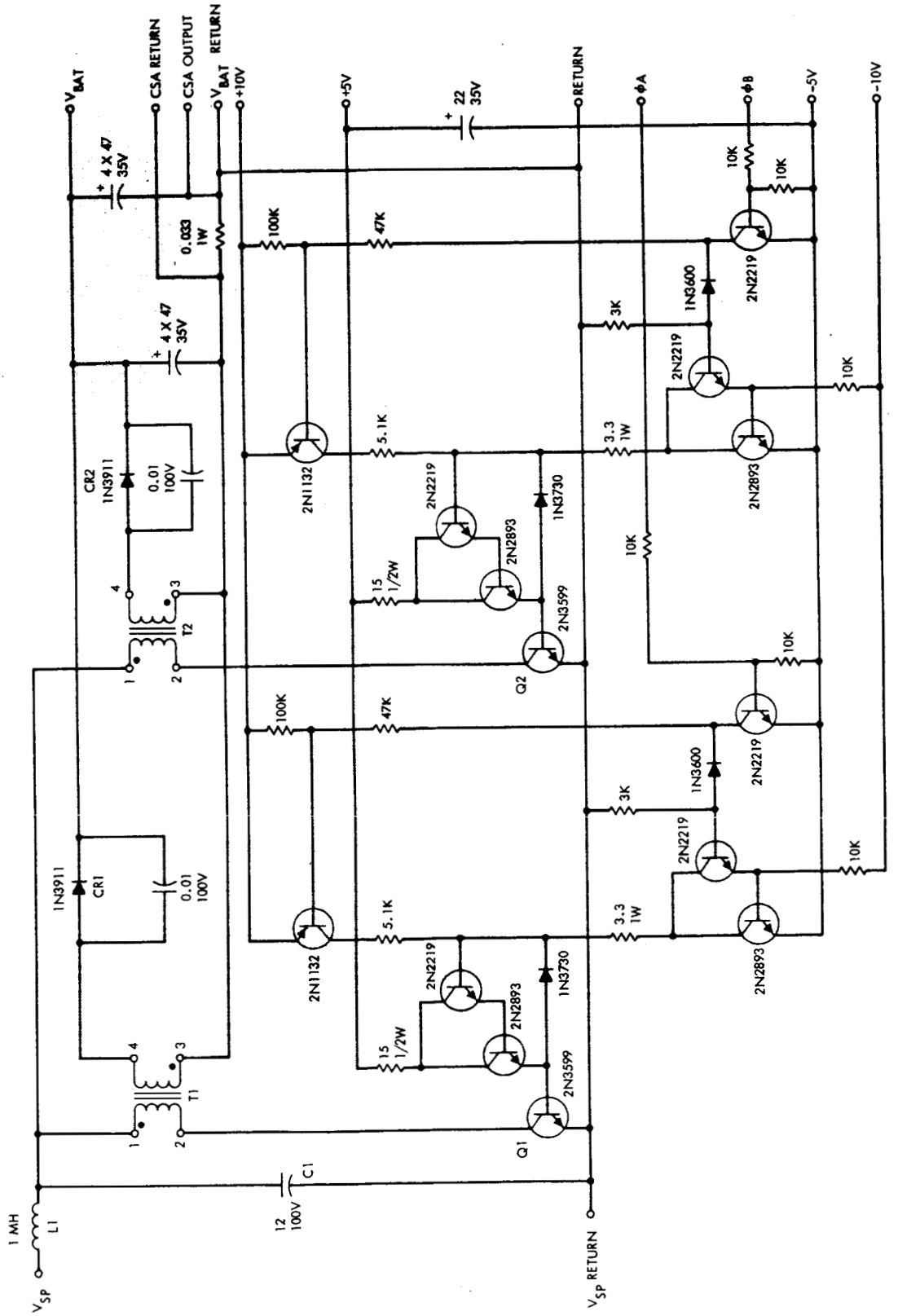


Figure 3-1. Fifty-watt, two-phase OCR switching circuit schematic diagram.

Transformer Parameters	Two-Phase OCR	Single-Phase OCR
Primary inductance	110 uh	30 uh
Secondary inductance	110 uh	67.5 uh
Turns ratio (N)	1:1	1:1.5
Peak primary current	6 amperes	18.3 amperes
Peak secondary current	6 amperes	12.2 amperes
Primary resistance	15 milliohms	15 milliohms
Secondary resistance	15 milliohms	15 milliohms
Core material	Powdered iron	Ferrite

Table 3-1. Fifty-watt switching transformer parameters.

Figure 3-2 shows the typical normalized current gain versus collector current characteristics of the 2N3599 transistor. This device is used as the main switching transistor in the switching circuit. It indicates that operating at a collector current of 6 amperes, the minimum beta (h_{FE}) of the device is about twice as high as when the device is operated at I_C = 18 amperes. Less drive is necessary to saturate the device, and consequently an overall savings in bias power is accomplished, as shown in the efficiency discussion in paragraph 2.1.4.

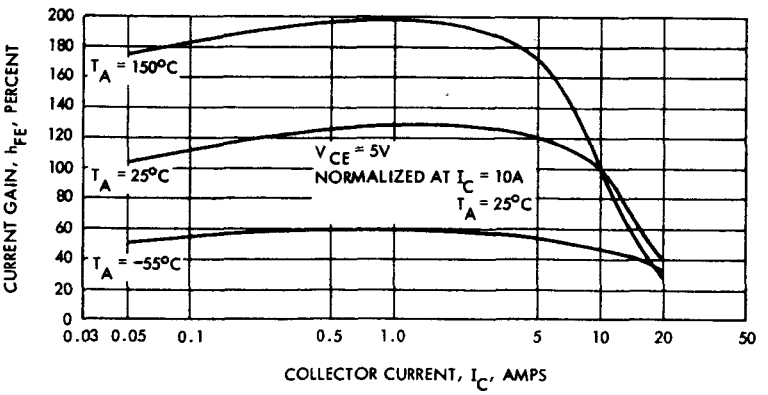


Figure 3-2. Normalized current gain versus collector current for the 2N3599.

From the photograph of the waveforms of Figure 3-3, the actual peak currents can be seen to be very close to the predicted values.

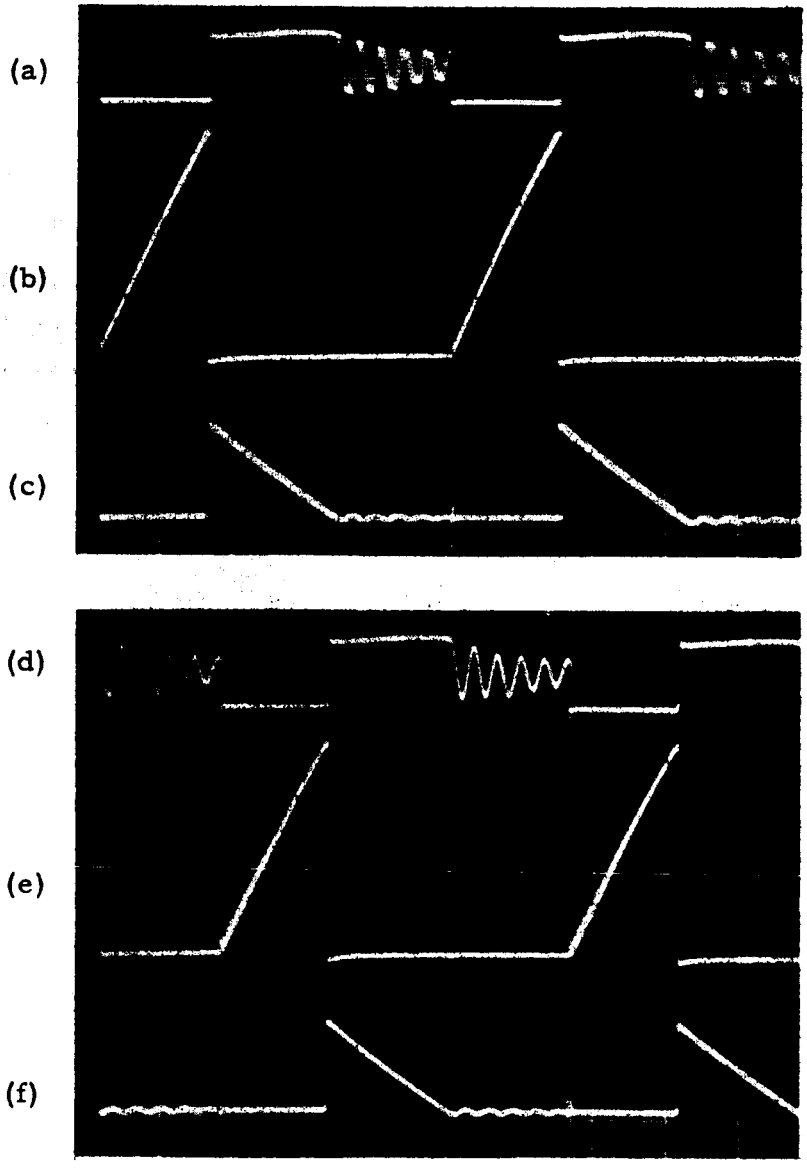


Figure 3-3. Fifty-watt, two-phase OCR switching circuit waveforms.

Vertical: (a) and (d) - 20 volts per centimeter
(b) and (e) - 2 amperes per centimeter
(c) and (f) - 5 amperes per centimeter

Horizontal: 20 microseconds per centimeter

The second major advantage of the two-phase switching circuit is that the peak-to-peak ripple of the battery current, I_{BAT}, has been reduced by doubling the phases. Figure 3-4 compares the battery ripple current of the single- and two-phase, 50-watt OCR. The peak-to-peak ripple has been reduced by a factor of 4.5 in the two-phase system.

(a)

(b)

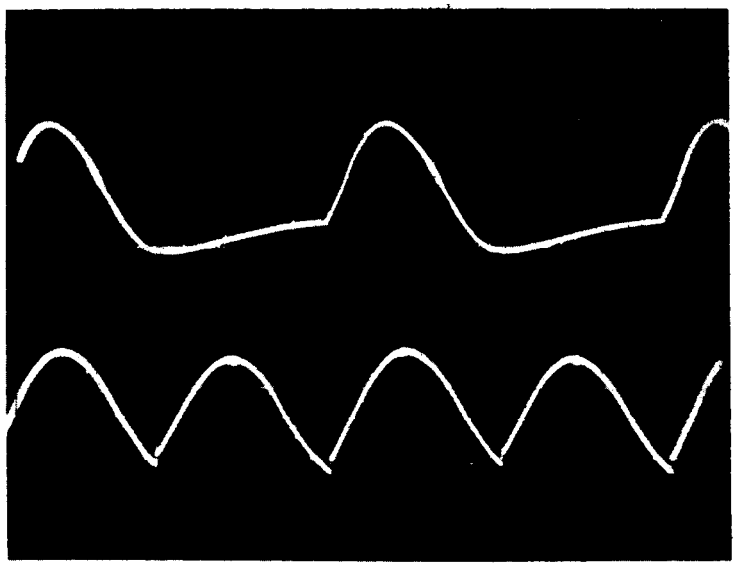


Figure 3-4. Battery ripple current — single-phase versus two-phase, 50-watt OCR.

Vertical: (a) - 4.0 amps per centimeter — single phase
(b) - 1.0 amp per centimeter — two phase

Horizontal: 20 microseconds per centimeter

Moreover by increasing the phases, the frequency of the harmonic is higher, and consequently, it is possible to reduce the size of the input and output filters.

3.2 TWO-PHASE DUTY FACTOR MODULATOR — 50-WATT OCR

The function of the two-phase duty factor modulator (DFM) is to generate two outputs which are 180 degrees out of phase. Figure 3-5 is a functional block diagram of this circuit. The 10 kHz oscillator generates two outputs, A and $\overline{A}$, which are 180 degrees out of phase. These outputs are then used to trigger ramp generators for phase A and phase B. These ramps are then compared to the integrator input. This comparison produces a duty factor variable square wave which is the final DFM output.

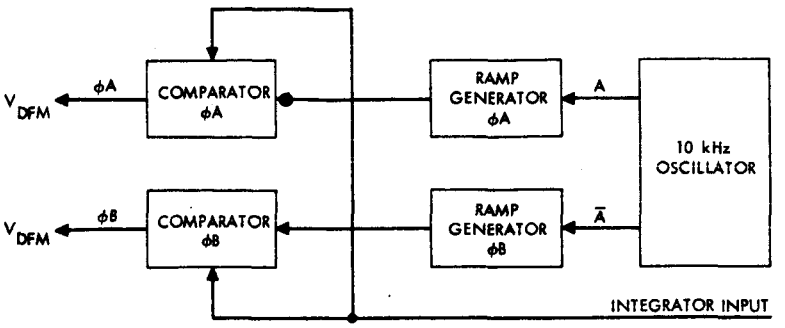


Figure 3-5. Two-phase duty factor modulator functional block diagram.

Figure 3-6 is a schematic diagram of this circuit. Transistors Q1 and Q2 comprise the 10 kHz oscillator. Ramp generator ϕA is composed of Q3 and Q4, while ramp generator ϕB is made up of Q5 and Q6. The comparators are Q7, Q8, and Q9 for ϕA, and Q10, Q11, and Q12 for ϕB.

3.3 FOUR-PHASE SWITCHING CIRCUIT - 250-WATT OCR

This circuit is identical in operation to the 50-watt switching circuit except for the two additional phases. The four phases are now 90 degrees apart.

The major difference in the four-phase system is the fact that the primary switching current now increases linearly with time to a peak current of 13 amperes compared to 27 amperes in the original two-phase system. The turns ratio of the four-phase switching transformers is 1:2 (see Table 3-2) reducing the peak secondary current from 13.5 amperes to approximately 6.5 amperes.

The savings in power losses as a direct result of the decrease in the peak currents is discussed in more detail in paragraph 2.1.4.

The other major difference between the two-phase and four-phase, 250-watt switching circuit is the increase in the switching frequency from 2 kHz to 10 kHz. This allowed for a considerable size and weight reduction in the switching transformer, although four are used now compared to two previously.

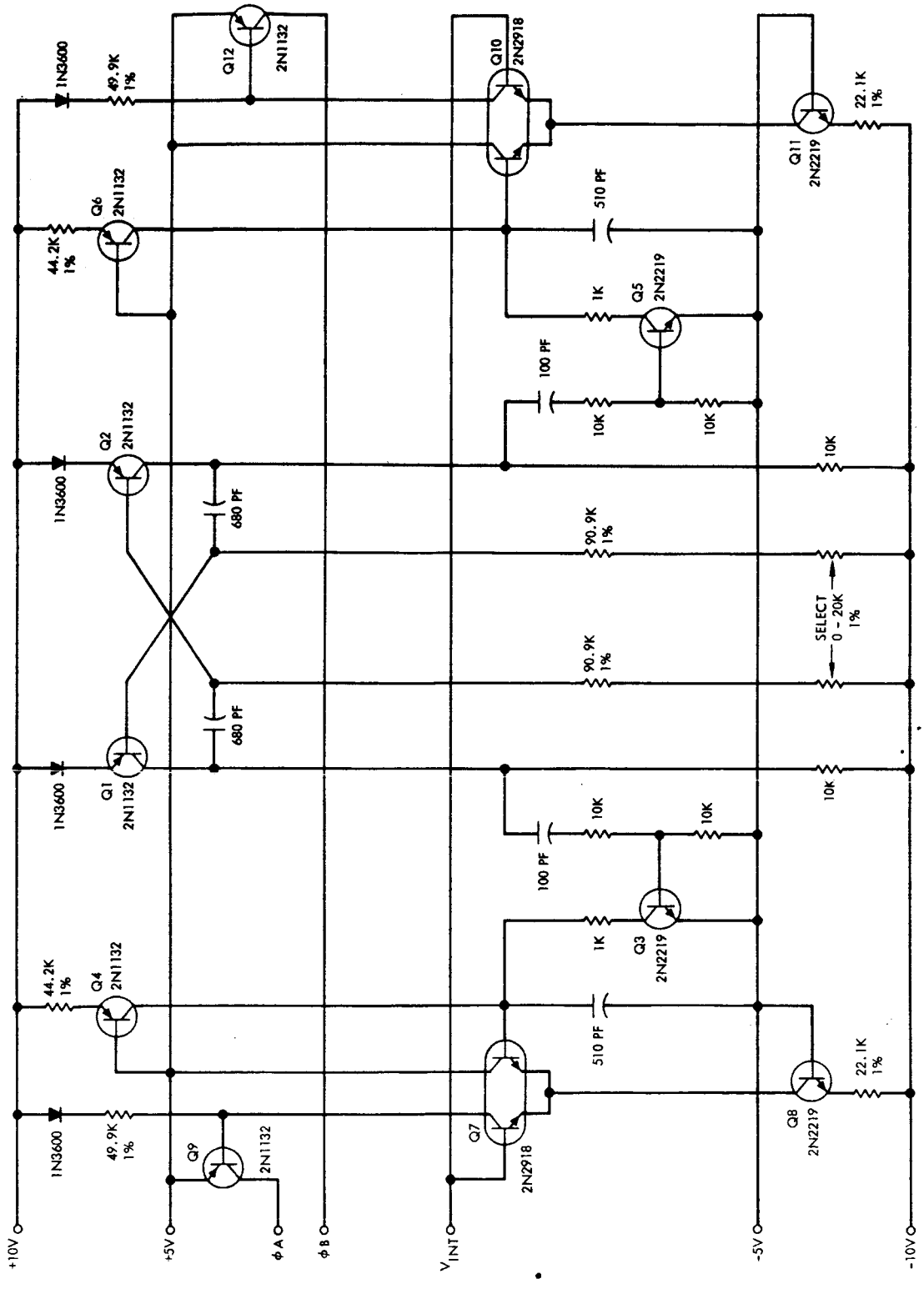


Figure 3-6. Fifty-watt, two-phase duty factor modulator schematic diagram.

Choke Parameters	Four-Phase OCR	Two-Phase OCR
Primary inductance	70 uh	170 uh
Secondary inductance	280 uh	680 uh
Turns ratio (N)	1:2	1:2
Peak primary current	13.0 amperes	27 amperes
Peak secondary current	6.5 amperes	13.5 amperes
Primary resistance	15 milliohms	15 milliohms
Secondary resistance	15 milliohms	15 milliohms
Core material	Powdered iron	Ferrite

Table 3-2. 250-watt switching transformer parameters.

3.4 FOUR-PHASE DUTY FACTOR MODULATOR - 250-WATT OCR

As in the two-phase duty factor modulator, the function of the four-phase DFM is to generate outputs to control the duty factor of the switching circuit, so that the regulator operates about the solar panel maximum power point. Four outputs are generated, each 90 degrees out of phase.

A block diagram of this circuit is shown in Figure 3-7. The circuit consists of two triggered flip-flops (FF1 and FF2), which are driven by a pulse generated by alternate half cycles of a 20 kHz oscillator. This causes the flip-flops to run at 10 kHz. The B output of FF1 leads the C output of FF2 by 90 degrees. The operation of the circuit from this point on is similar to that of the two-phase DFM. FF1 drives phase A and phase B, and FF2 drives phase C and phase D.

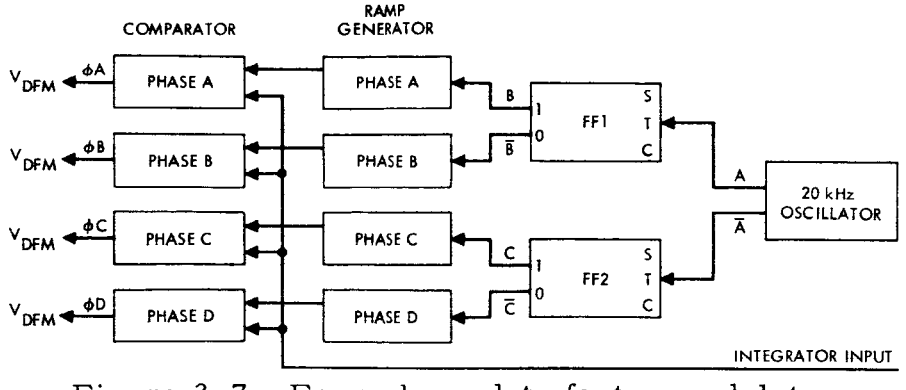


Figure 3-7. Four-phase duty factor modulator functional block diagram.

The 90-degree shift between FF1-B and FF2-C causes the comparator output for phase A to lead the comparator output for phase C by 90 degrees. Phase A is also 180 degrees shifted from phase B, and phase C is 180 degrees shifted from phase D.

A schematic of the four-phase duty factor modulator is shown in Figure 3-8. Transistors Q1 through Q4 comprise the flip-flops, FF1 and FF2. Transistors Q5 through Q16 make up the four comparators, and transistors Q17 through Q24 are the four ramp generators. The 20 kHz clock consists of transistors Q25 and Q26.

3.5 SWITCHING TRANSFORMER DESIGN

The switching transformer used for the single-phase, 50-watt, and 250-watt, two-phase OCR was fabricated from a ferrite material. Efficiency measurements determined that a major portion of the total losses in the OCR was due to core losses in the switching transformer. After extensive research into different types of cores that could possibly be used under the existing circuit conditions, it was determined that a powdered-iron (moly permalloy) core would have the minimum core loss for the same volume. In the four-phase, 250-watt unit, using the redesigned switching transformers, a reduction of 20 percent in core losses was attained.

The winding was also optimized to give a minimum leakage inductance (2.2 microhenrys) and a minimum distributed capacitance. This improved the rise time and minimized both the overshoot and ringing in the transformer.

A higher "Q" (60 compared to 20 for the ferrite transformer) was attained resulting in less I^2R losses, and a resistive rather than an inductive load-line characteristic for the switching transistors, thereby reducing the switching losses by a factor of about six.

Further study into the switching transformer design has resulted in a new theory that may reduce the losses even further. It is felt that the phenomenon known as the "proximity effect" could be an important contributor to losses in the switching transformer. When two or more adjacent conductors are carrying current, the current distribution in

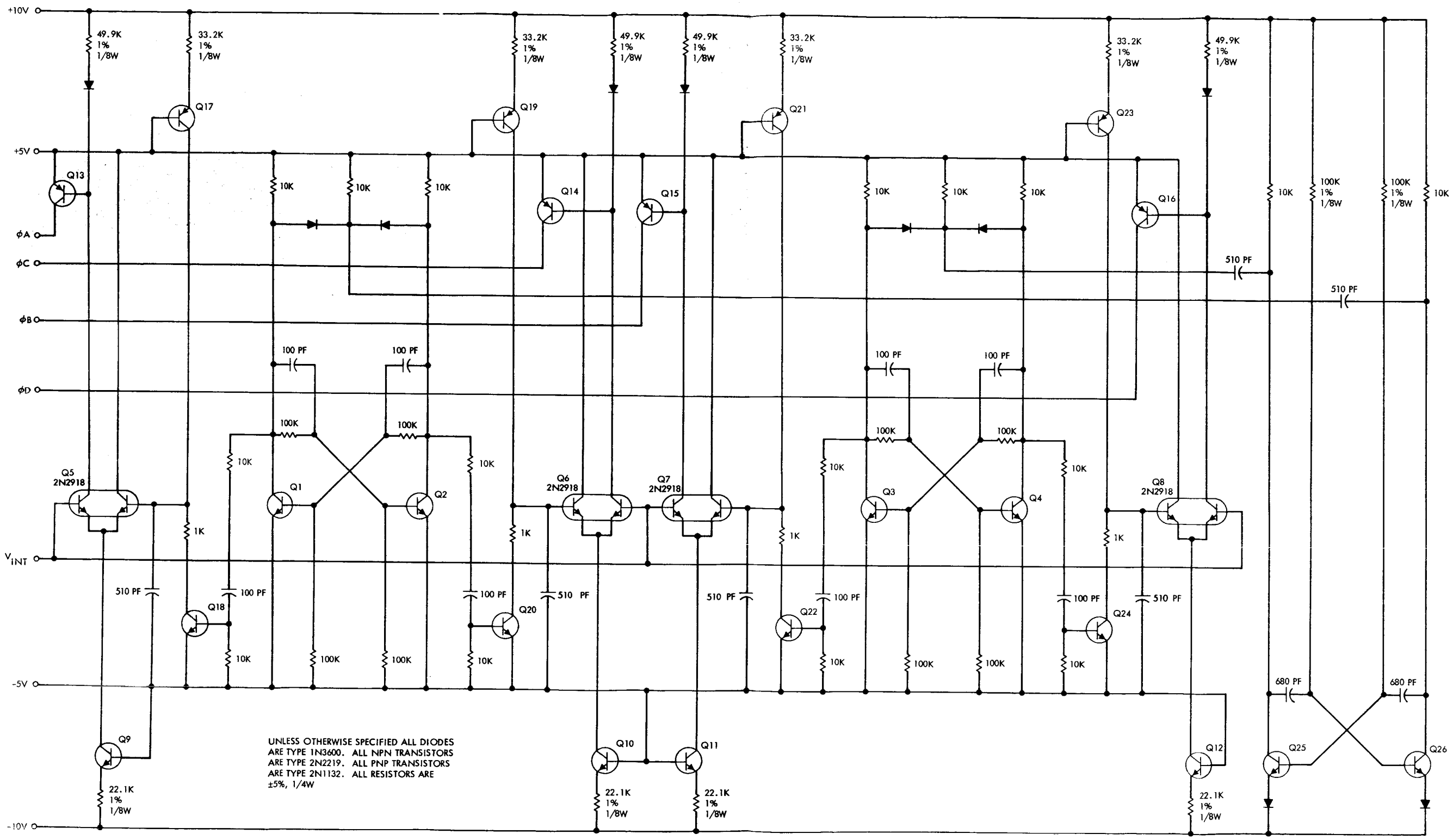


Figure 3-8. Four-phase duty factor modulator schematic diagram.

one conductor is affected by the magnetic flux produced by the adjacent conductors, as well as the magnetic flux produced by the current in the conductor itself. The effect is termed the proximity effect and ordinarily causes the resistance ratio, which is the ratio of the ac resistance to the dc resistance, to be greater than in the case of simple skin effect. Proximity effect is very important in inductance coils operating in the lower radio frequencies. The 10 kHz switching frequency of the optimum charge regulator is within the frequency range that the proximity effect could play a part.

The resistance ratio of a conductor can be made to approach unity very closely, at least at the lower radio frequencies, by use of a conductor consisting of a large number of strands of fine wire that are insulated from each other except at the ends, where the various wires are connected in parallel. Such a conductor is termed a "Litz" or Litzendraht conductor. The result of equalizing the reactances of the individual strands of wire is to cause the current to divide uniformly between strands. This will reduce the ac losses in the wire. Practical "Litz" conductors are very effective at frequencies below 500 kHz.

In the next part of the program, Litz wire will be used on the present moly permalloy core to try to reduce the losses in the switching transformers. Wire has been ordered and delivery is expected shortly.

3.6 SIMPLIFICATION OF CIRCUITRY

3.6.1 Two-Phase Duty Factor Modulator

In the single-phase duty factor modulator a flip-flop was used to generate the V_{DFM} output pulse. In the two-phase duty factor modulator, the flip-flop and its associated resistors, diodes, and capacitors were eliminated. The output pulse to control the switching circuit is now taken directly from the comparator.

Two (2) amplifiers on the outputs of the 10 kHz oscillator were replaced by two (2) diodes since the additional gain was not required. Several base-emitter resistors were also eliminated, wherever it was determined they were not required.

Comparing the total parts count of the redesigned two-phase duty factor modulator with the original one used on the two-phase, 250-watt OCR, it can be seen that there were forty-seven less components used in the more simplified redesigned circuit (refer to Table 3-3).

Component	Original Two-Phase DFM	Redesigned Two-Phase DFM
	Quantity	Quantity
Transistor	19	14
Diode	12	4
Resistor	48	18
Capacitor	20	16
Total	99	52

Table 3-3. Comparison of two-phase duty factor modulator parts count original versus redesigned.

3.6.2 Two-Phase Switching Circuit

The input filter capacitor was reduced in size because of the lower ripple of the two-phase switching circuit. Consequently, less filtering was required, which resulted in a major size and weight savings. The input filter could be reduced even smaller in size by increasing the switching frequency and this is now being studied.

Two driver transistors and their associated resistors were eliminated because there was sufficient gain in the circuit to switch Q1 and Q2 "on" and "off" rapidly.

Several base-emitter resistors were also eliminated, wherever it was determined they were not required.

3.6.3 Four-Phase Duty Factor Modulator

This circuit was simplified in the same manner as the 50-watt, two-phase duty factor modulator. By eliminating the counting flip-flops, a considerable number of components were saved. If the original circuits

were now used in the four-phase system, four more flip-flops and their associated components would be required, and the overall circuitry would be far more complicated.

3.6.4 Four-Phase Switching Circuit

By decreasing the primary peak current in each phase, it was no longer necessary to parallel two (2) 2N3599 transistors per phase. However, in the four-phase system four (4) 2N3599 transistors are still required. Also the IN3911 flyback diodes remained at a total of four (4) since paralleling was not necessary. A total of four (4) driver transistors were eliminated (one per phase) because of sufficient gain in the circuit.

The input filter was considerably reduced in size as the result of going to a four-phase system, the ripple being decidedly less.

Transformer size was reduced as a result of less current being drawn by each phase.

3.6.5 Balance of Circuits

Throughout the balance of the circuits (peak holding comparator, bistable, integrator, and current sensing amplifier) the transistors, resistors, capacitors and portions of circuits have been changed, and in some cases eliminated. The primary thought in mind is that of optimizing both circuit operation and efficiency, and at the same time simplifying the circuits in order to reduce size and increase reliability.

4.0 BATTERY STUDY PROGRAM

The intent of the battery study program is to determine the best means of operating a third electrode charge control device with the optimum charge regulator. Since an OCR can deliver the maximum power available from the solar array at any instant, it is necessary to be able to utilize this power as it becomes available to charge the battery. In this manner, the battery size and weight, as well as the solar array size and weight, can be minimized.

The major problem involved with coupling an OCR to a battery is that of the high charging rates to the battery as the solar panel maximum power point increases. This can be especially evident, for example, in the case of a satellite which has just emerged from earth shadow. At this point its solar array is very cold, and the battery voltage is low, due to maximum use during this eclipse period. The characteristics of an OCR are such that a constant power is delivered to the battery at all times that the OCR is operating in its optimum charging mode. The satellite array maximum power would be about twice its normal value because of the cold nature of the panel. Since the battery voltage was low, the charging current would be very high. This high charging rate would tend to cause pressure build-up in sealed spacecraft cells as they neared full charge. Use of third electrode cells under these conditions would be advantageous as they would allow maximum power charging of the battery with a controlled cutoff when the battery reached full charge.

In order to properly couple the OCR to the third electrode battery, determination of the third electrode output signal with respect to the constant power charging characteristics of the OCR is of prime importance.

The cells on hand for this testing program are thirty 12AH Gulton nickel cadmium cells, six of which are third electrode cells. The testing will have three phases. The first will be to determine the characteristics of the third electrode output signal for various

charging rates. These rates have been arbitrarily chosen as C/10, C/5, and C/2. The purpose of these tests is to determine if there is any variation of third electrode output as a function of charging rate. This is necessary, due to the variation of the charge rate of the OCR, because of its constant power output characteristic.

The second phase of the program will be concerned with designing the necessary OCR control circuitry. This circuitry will be designed to be compatible with the results of the phase-one testing. A major goal in the design will be simplicity, so that parts count may be kept to a minimum, thereby maximizing reliability and minimizing size and weight.

The final phase will be concerned with evaluation of the third electrode battery with the OCR, and its control circuitry. In this phase, a 27-cell battery will be constructed. This battery will contain a minimum of three third-electrode cells. This battery will then be coupled to the 250-watt, four-phase OCR. This circuit can supply charging rates of approximately C at very low battery voltage, to approximately C/2 at or near full charge. The third-electrode characteristics will be observed under these conditions, and various optimization techniques for the control circuitry will be examined.

SEMIANNUAL REPORT

(Contract NAS 5-10225)

NONDISSIPATIVE CHARGE REGULATOR ADVANCED STUDY

P67-4

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National Aeronautics and Space Administration
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Greenbelt, Maryland

Research and Development Division

AEROSPACE GROUP

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1.0 INTRODUCTION

This report summarizes the work accomplished during the first six months of a one-year program in the design, development, and testing of multiphase, nondissipative optimum charge regulators. This program is a continuation of the work done on Contract NAS 5-9210. This previous effort was concerned with the development of the basic circuits required for the efficient transfer of power from a spacecraft solar array to a spacecraft type battery. The continuation of effort during the present program is for the purpose of improving the basic designs in order to improve their efficiency and reliability.

Extension of the level of research and development effort from the previous program includes the following:

1. Construction of a two- and a four-phase optimum charge regulator to demonstrate the feasibility for improved efficiency and reliability.
2. Study all aspects of multiple phase regulators with particular attention to continued operation in the event of one phase becoming inoperative.
3. Perform worst case and failure mode analysis on all circuits in order to determine reliability problem areas.
4. Construct mathematical models for each circuit block to indicate critical design areas and demonstrate where redundancy may best be employed.
5. Study third-electrode charge control devices and their application to optimum charge controllers.

1.1 SUMMARY OF EFFORT DURING THE FIRST HALF OF THE PROGRAM

During the first six months of development, the 50-watt, single-phase regulator, and the 250-watt, two-phase regulator, which were designed for Contract NAS5-9210, were redesigned. These units were modified to include a two-phase switching circuit for the 50-watt unit, and a four-phase switching circuit for the 250-watt unit. Photographs

of these breadboards are shown in Figure 1-1 and 1-2. The basic switching circuit and duty factor modulator circuit operation is the same as in the original design except for the additional phases. The balance of the circuits in the control loop were simplified to increase reliability and reduce total parts count.

The switching transformers were redesigned in an effort to reduce the core losses which contributed to the overall system inefficiency in the original design.

1.2 SUMMARY OF RESULTS

Testing of the 50-watt and 250-watt regulators at room temperature indicated satisfactory operation over all the extremes of input and output conditions, including the -30 percent power transient. Stable tracking of the maximum power point during this condition was observed. A decrease in the losses due to hunting was also found.

Efficiency measurements indicated the 50-watt regulator exceeded its goal of 85 percent. The 250-watt regulator came very close to its goal of 90 percent; an additional change in the construction of the switching transformer could possibly result in reaching this goal. The major reason for the efficiency improvement in both units was traced to the improved switching transformer design. Use of powdered iron cores in the transformer construction allowed the switching circuits to be compensated, so as to provide a resistive switching load line instead of the previously inductive load line. This allowed the switching losses to be reduced by a factor of about six. The increase in the number of phases also aided in the efficiency improvement by reducing the peak currents drawn by the switching circuit.

A battery study has been proposed to determine the best means of operating a third electrode charge control device with the optimum charge regulator. Results will be available in the final report.

1.3 PROPOSED EFFORT FOR THE REMAINDER OF THE PROGRAM

There are several tasks that will be performed during the second half of the program. They will verify whether the reliability and stability goals, as well as the efficiency goals, required for the assurance of long lifetime mission success, have been accomplished. The following is a work schedule that will be performed during the next six months:

1.3.1 Mathematical Models and Block Diagrams

Mathematical models and block diagrams will be developed to indicate critical design areas and demonstrate where redundancy may be employed to improve reliability. The current sensing amplifier was chosen as the first circuit block to be analyzed. Work has started on the derivation of its transfer function in order to determine the gain and phase characteristics under all conditions.

1.3.2 Worst Case Analysis

Worst case analysis will be performed on all circuits in an effort to determine whether normal operation can proceed under all worst case solar panel, battery, temperature and aging variations. (This analysis will be performed for the following conditions: Maximum and minimum semiconductor parameter variations; ±20 percent resistance variation for all ±5 percent resistors; ±5 percent resistance variation for all ±1 percent resistors; +20 percent and -50 percent variation in capacitance for all capacitors; ±10 percent in inductance variation for all inductors; twice the maximum and minimum specified variation for all other components.)

1.3.3 Failure Mode Analysis

Failure mode analysis will determine the effect on mission success of the different components used in the optimum charge regulator. This will indicate which modes of circuit failures are more likely to occur and which components directly affect these failures. This analysis will indicate where redundancy might best be employed to improve circuit reliability. These modifications will be discussed in detail in the final report but no actual breadboard modifications are expected to be required.

1.3.4 Temperature Testing

Temperature testing will be completed on the 50-watt and 250-watt regulators to verify whether the efficiency goals were attained over the temperature range of -40°C to +70°C, and to ensure proper operation over the temperature extremes.

1.3.5 Third Electrode Battery Study

The third electrode battery study will determine a means of operating a third electrode charge control device with the optimum charge regulator. The first phase of the study will be to test third electrode batteries to determine their output signal characteristics for various charging rates. The final phases will be concerned with the design of the OCR control circuitry and its evaluation.

1.3.6 Multiphase Operation

The final goal of the program is the development of the necessary circuit modifications that are required to maintain normal, reliable operation of multiphase regulators if one or more phases become inoperative.

2.0 EFFICIENCY DISCUSSION

2.1 TWO-PHASE, 50-WATT REGULATOR

Efficiency and dissipation measurements were made on the two-phase, 50-watt unit to determine how much of an improvement was made in going from the original single-phase design to a two-phase system. Measurements were made at room temperature. The temperature evaluation will be completed during the final portion of the program. Data was taken over several days to ensure accurate and consistent readings. The methods used to make the power loss measurements are detailed in the following paragraphs. The major dissipation areas are discussed and the techniques used for measuring the power loss are detailed. A summary of all major dissipation areas is shown in Table 2-1. This table compares the power loss in the present two-phase unit to that of the original single-phase unit. Figure 2-1 is a block diagram of the OCR, and it indicates the dissipation in each major circuit block of the regulator.

2.1.1 Efficiency Measurement Technique

The solar panel simulator was set at an open circuit voltage (temperature) of 30 volts, and a short circuit current (illumination) of approximately 2.2 amperes. Current limiting of the simulator was set at its maximum. Degradation and rounding was set at their minimum values.

The battery simulator was adjusted for a battery voltage of 12 volts. A Hewlett-Packard digital voltmeter Model 3440A was used to measure the battery and solar panel voltages.

With the OCR optimum charging the battery, the solar panel output current was adjusted for 2.0 amperes. This was accomplished by monitoring the voltage across resistor R_A, as shown in Figure 2-2. A Calibration Standards Corporation precision differential dc voltmeter, model DC-110B, was used to measure V_{RA} and V_{RB} (see Figure 2-2). Resistors R_A and R_B were both about 20 milliohms and were calibrated before any testing was done.

Dissipation Area	Power Loss, watts	Power Loss, watts
	Two-Phase OCR	Single-Phase OCR
Switching circuit bias power	0.79	1.20
Total saturation	0.22	0.68
Total switching	0.70	2.63
Input filter inductor	0.24	0.80
Fly back diode	0.26	0.68
Sensing resistor	0.52	0.68
Switching transformers		
Copper	0.12	1.36
Core	2.95	1.54
Duty factor modulator	0.06	0.14
Current sensing amplifier, peak holding comparator, bistable and integrator	0.17	0.16
Switching regulator bias converter	0.85	1.63
Hunting loss	0.12	0.50
Total	7.00	12.00
Efficiency = η = 86 percent		η = 76 percent
Maximum available power = 50 watts		

Table 2-1. Summary and comparison of major dissipation areas for the 50-watt, two-phase OCR and the 50-watt, single-phase OCR.

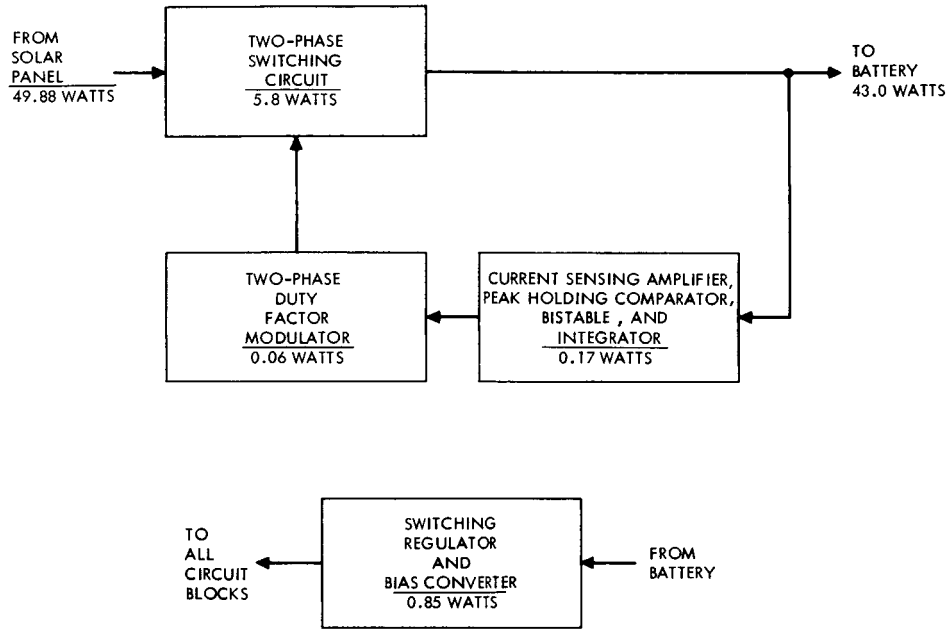


Figure 2-1. Fifty-watt, two-phase OCR block diagram and dissipation summary.

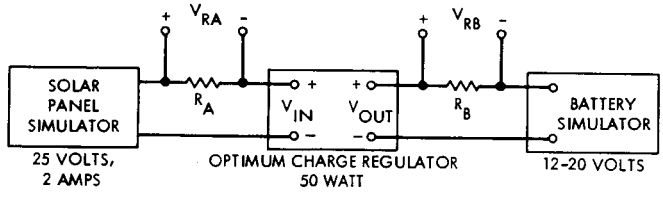


Figure 2-2. Efficiency measurement test setup.

Efficiency was computed using the following relationship:

$$\text{Efficiency percent} = \left[\frac{\frac{V_{RB} \times V_{BAT}}{R_B}}{\frac{V_{RA} \times V_{SP}}{R_A}} \right] \times 100$$

$$= \frac{V_{RB} \times V_{BAT}}{V_{RA} \times V_{SP}} \times 100 \qquad (2\text{-}1)$$

where

V_{SP} = solar panel voltage

V_{BAT} = battery voltage

V_{RA} = voltage across R_A

V_{RB} = voltage across R_B

R_A, R_B = current sensing resistor

(Note: Due to the difference in the exact resistances of R_A and R_B, a correction was made in the final calculation of power losses.)

The procedure was repeated at battery voltages of 14, 16, 18, and 20 volts. Readings were repeated several times at each battery voltage to ensure accuracy. The results can be found in Table 2-2.

V_{Bat}, volts	Efficiency, percent
12	83.4
14	84.4
16	84.9
18	85.2
20	86.1

Table 2-2. Fifty-watt, two-phase regulator efficiency for varying battery voltage.

As shown by this table, the efficiency is maximum at maximum battery voltage and decreases as the battery voltage is lowered. This is due to the increase in average battery current as the battery voltage decreases. This increased current results in greater I^2R losses in the switching circuit secondary. For this reason, the efficiency is best at high battery.

2.1.2 Hunting Loss Measurement

Upon completion of the efficiency measurements, the loss due to hunting was then measured.

A 20K trimpot was connected between the +5 volt and -5 volt bias inputs to the duty factor modulator with the center tap connected to the integrator input.

The integrator input to the duty factor modulator was disconnected and the trimpot was adjusted until the current delivered to the battery was at a maximum.

The hunting loss was computed by taking the difference between the power delivered to the battery during normal OCR operation and the power delivered when the OCR was manually adjusted to operate at the maximum power point.

2.1.3 Switching Regulator and Bias Converter

In order to determine where the power in the optimum charge regulator was being dissipated, it was necessary to know how much bias current was being drawn from the bias converter, and also how much power was being dissipated within the switching regulator and bias converter. The dissipation was found by subtracting the total output bias power from the total input power. The input power measurement was made at a battery voltage of 20 volts, since this represents the worst case input for the switching regulator.

2.1.4 Switching Circuit Losses

Since this circuit dissipates over 80 percent of the total power lost, a detailed discussion of each component loss is included in this

paragraph. Figure 2-3 is a basic schematic diagram of this circuit, and it summarizes each power loss for the individual components.

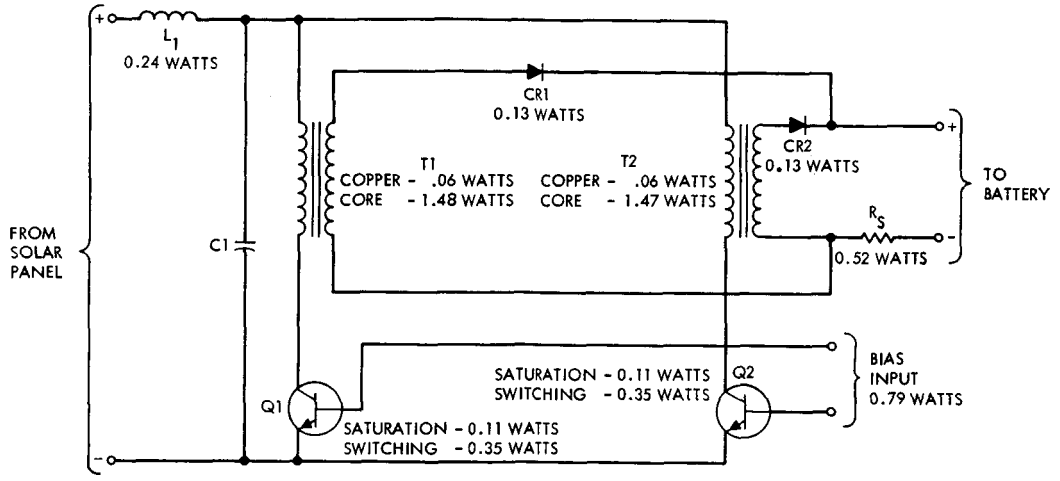


Figure 2-3. Fifty-watt, two-phase switching circuit basic schematic diagram and dissipation summary.

2.1.4.1 Bias Power. The total power delivered by the bias converter to the switching circuit and to the duty factor modulator (DFM), current sensing amplifier (CSA), peak holding comparator (PHC), bistable and integrator circuits was found to be 1.02 watts. This is 0.48 watt less total bias power loss than in the single-phase circuit. The two-phase switching circuit was found to dissipate 0.79 watt This is a total of 0.41 watts less than in the previous design. This is due to the fact that less base drive is required for the two-phase switching circuit power transistors, because of their higher current gain at the lower peak currents which are now drawn.

2.1.4.2 Switching Transistor Saturation Losses. The total saturation losses of Q1 and Q2 were found to be 0.22 watt. This is 0.46 watts less than the previous single-phase system. This is a result of reducing the peak primary current in the switching transformers from 18 amperes to 6 amperes. A saturation resistance of 0.03 ohm for Q1 and Q2, and a duty factor of 0.3 was used in Equation 2-3 to derive a total saturation loss of 0.22 watt.

$$P_{SAT} = \frac{RI_P^2 D\phi}{3} \qquad (2\text{-}3)$$

where

R = saturation resistance

I_P = peak primary current

D = duty factor

ϕ = number of phases

2.1.4.3 Switching Transistor Switching Losses. This loss was approximated using the switching waveforms shown in the photograph of Figure 2-4. The photograph shows the collector-emitter voltage and the collector current of both Q1 and Q2 at the moment of "turn-off".

The power is approximated by breaking the waveforms into segments. For transistor Q1, the voltage begins rising at t = 0.375 microsecond. It rises to about 20 volts in the next 0.05 microsecond while the current remains at 6 amperes.

Therefore

$$P(0.375 - 0.425 \text{ microsecond}) = \frac{10 \times 6 \times 0.05}{100} = 0.03 \text{ watts}$$

For the next 0.05 microsecond, the voltage rises to 50 volts while the current drops to about 5 amps.

Therefore

$$P(0.425 - 0.475 \text{ microsecond}) = \frac{35 \times 5.5 \times 0.05}{100} = 0.096 \text{ watt}$$

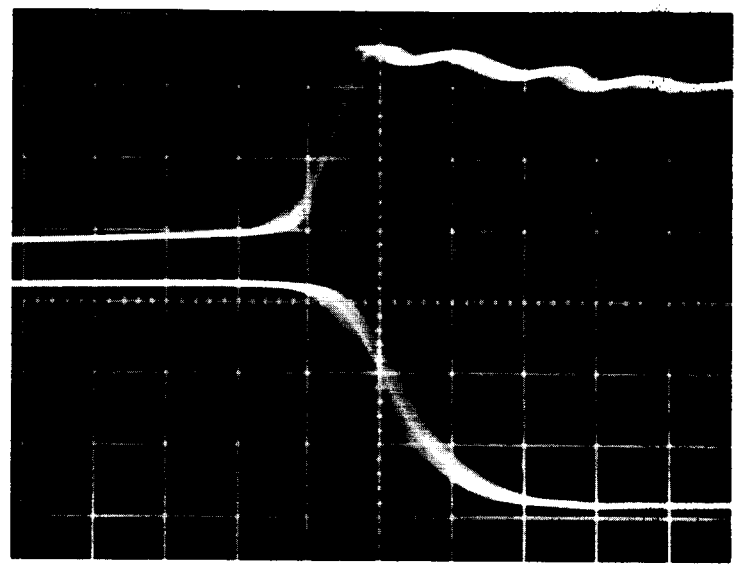
Finally, the voltage remains at 50 volts while the current drops to zero during the next 0.20 microsecond.

Therefore

$$P(0.475 - 0.675 \text{ microsecond}) = \frac{50 \times 2.25 \times 0.2}{100} = 0.225 \text{ watt} \quad .$$

(a) V_{ce} (Q1)

(b) I_c (Q1)



(c) V_{ce} (Q2)

(d) I_c (Q2)

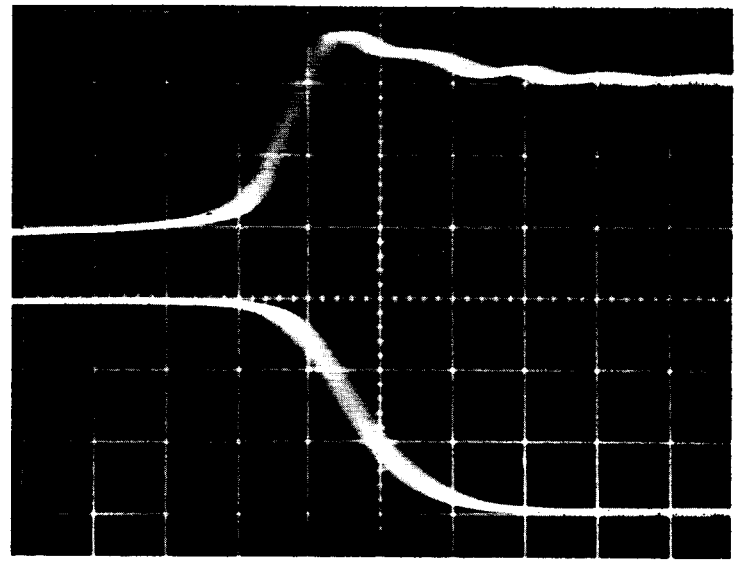


Figure 2-4. Voltage and current waveforms for calculating the switching losses of switching transistors Q1 and Q2 in the 50-watt, two-phase OCR.

Vertical: (a) and (c) - 20 volts per centimeter
(b) and (d) - 2 amperes per centimeter

Horizontal: 0.1 microsecond per centimeter

The power lost due to switching in Q1 is 0.35 watt. If Q2 is assumed to have approximately the same waveforms, then the total switching loss is found to be 0.7 watt. This is considerably less than the switching loss incurred in the single-phase OCR. These losses were about four times greater. The improvement can be attributed to the reduction in the peak current seen by the switching transistors, and to the improved transformer design. The reduction of the peak current and the use of the powdered iron core aided in reducing the switching time by about a factor of two. The reduction of the peak current also reduced the switching losses, which are a function of the V-I product.

2.1.4.4 Input Filter Inductor - L1. The dc drop across L1 was determined to be 0.12 volt at a current of 2 amperes. The power dissipated is thus 0.24 watts. A savings of 0.56 watts was obtained by reducing the series resistance of L1. This design area can be optimized with regard to both power loss and size as discussed in paragraph 3.6.2.

2.1.4.5 Flyback diode - CR1 and CR2. This loss can be approximated using Equation 2-3. Using the values R = 0.03 , I_p = 6 amperes, and D = 0.36, the power loss is found to be 0.26 watts. The peak current was reduced from 12 amperes in the single-phase OCR to 6 amperes in the two-phase OCR, which reduced the power losses in the flyback diodes by 0.42 watt.

2.1.4.6 Sensing Resistor - R_S. The power lost in the sensing resistor, R_S, is twice the total power lost in CR1 and CR2, since the resistance of each diode is about the same as R_S, and each diode handles one-half the current. The power dissipated in R_S is 0.52 watt.

2.1.4.7 Switching Transformer - Copper. The series resistance of the switching transformer is 0.015 ohm in the primary and 0.015 ohm in the secondary. Therefore, it will have one-half the losses for the combination of the saturated Q1 and Q2 condition and the losses found for

CR1 and CR2. The total copper loss was found to be 0.12 watt, or an improvement of 1.24 watts over the single-phase OCR.

This savings was due mainly to the lower currents in the primary and secondary windings, and to the reduced series resistance of the switching transformers.

2.1.4.8 Switching Transformer - Core Loss. The core loss is determined by taking the difference between the measured losses and the total power loss as determined from $P_{IN} - P_{OUT}$. This is the technique presently employed for measuring this loss. The core loss was determined to be 2.95 watts.

2.1.5 Switching Regulator/Bias Converter Losses

The losses in the switching regulator and bias converter are determined by taking the difference between the input and output power of this circuit. The total power dissipated in the switching regulator and bias converter was found to be 0.85 watt. This is approximately one-half the power that was previously lost in the single-phase system. The savings is primarily due to less total bias power required by the duty factor modulator, and decreased drive required for Q1 and Q2.

2.1.6 Summary

A comparison of the results of the original single-phase OCR and the new two-phase system (Table 2-1) clearly shows that less power is dissipated in most of the major areas within the two-phase OCR. The total power loss is 7.00 watts compared to 12.0 watts in the original design. As a result, 5.0 watts additional power can be delivered to the battery, which represents an efficiency increase of 10 percent over the single-phase design. The original design goal of 85 percent was met at room ambient temperature. It is felt that 85 percent is attainable over the entire temperature range. Further temperature testing will be conducted during the next part of the program.

2.2 FOUR-PHASE 250-WATT REGULATOR

The original design goal of 90 percent was nearly achieved with a measured efficiency of 88.0 percent. The switching transformer redesign resulted in a net reduction of over 6 watts in core loss. It is felt that further reduction in losses in this major dissipation area can be achieved in further studies to be conducted as explained in paragraph 3.4.

The method of efficiency measurements in the four-phase, 250-watt regulator is basically the same as performed for the two-phase, 50-watt regulator. The open circuit voltage was set at 50 volts, and the short circuit current adjusted for approximately 6.5 amperes. Efficiency measurements were taken at battery voltages of 25, 30, 35, and 40 volts. Efficiency was computed using Equation 2-1. Table 2-3 summarizes the unit efficiency for various battery voltages. The decreased efficiency at low battery was found to be caused by the increased I^2R losses due to the higher battery current drawn during this condition.

V_{BAT}, volts	Efficiency, percent
25	87.1
30	87.6
35	87.7
40	88.0

Table 2-3. 250-Watt, four-phase regulator efficiency for varying battery voltage.

Hunting loss measurements were also taken in the same manner as for the 50-watt unit. Table 2-4 summarizes the major dissipation areas and compares them to the original 250-watt, two-phase design.

Dissipation Area	Power Loss, watts	Power Loss, watts
	Four-Phase OCR	Two-Phase OCR
Switching circuit bias power	4.12	3.10
Total saturation	1.15	1.00
Total switching	2.25	2.80
Input filter inductor	1.19	2.10
Output filter inductor		1.70
Flyback diode	0.82	1.10
Sensing resistor	1.64	2.10
Switching transformers		
Copper	1.00	4.20
Core	13.88	20.00
Duty factor modulator	0.11	0.10
Current sensing amplifier, peak holding comparator, bistable and integrator	0.17	0.10
Switching regulator and bias converter	2.75	1.70
Hunting loss	0.92	4.00
Total	30.00	44.00
Power input = 250 watts		
	η = 88 percent	η = 82.5 percent

Table 2-4. Summary and comparison of major dissipation areas for the 250-watt, two-phase OCR and the 250-watt, four-phase OCR.

3.0 CIRCUIT DESIGN DESCRIPTION

The three basic areas of modification within the new 50-watt and 250-watt optimum charge regulators are the following:

a. A two-phase and four-phase switching circuit and duty factor modulator for the 50-watt and 250-watt OCR, respectively
b. The use of redesigned switching transformers
c. Simplification of the circuitry within the balance of the optimum controller

The three areas mentioned above have contributed to both increased efficiency and reliability. A worst case and failure mode analysis will be performed during the next portion of the program to show in detail the OCR operation under worst case conditions. These conditions include variations in solar panel and battery voltages, and changes in the temperature.

3.1 TWO-PHASE SWITCHING CIRCUIT - 50-WATT OCR

The switching circuit is the most important block within the optimum charge regulator in terms of efficiency, because it is this circuit that transfers the power from the solar panel to the battery. Figure 3-1 is a schematic diagram of this circuit.

The two-phase switching circuit employs two single-phase switching circuits in tandem. Each of these circuits transfers only one-half of the total power. They are operated 180 degrees out of phase so as to reduce the input and output ripple. This causes the effective ripple frequency, due to switching, to be twice the primary switching frequency rate, allowing for considerable reduction in input filter size.

The two-phase design uses an improved switching transformer design with a turns ratio of 1:1 (see Table 3-1). The old design had a 1:1.5 turns ratio. By employing two phases, and with the transformer improvement, the peak current in the primary is reduced from 18 amperes to 6 amperes. A 1:1 turns ratio is the optimum design, since maximum coupling between windings can be achieved.

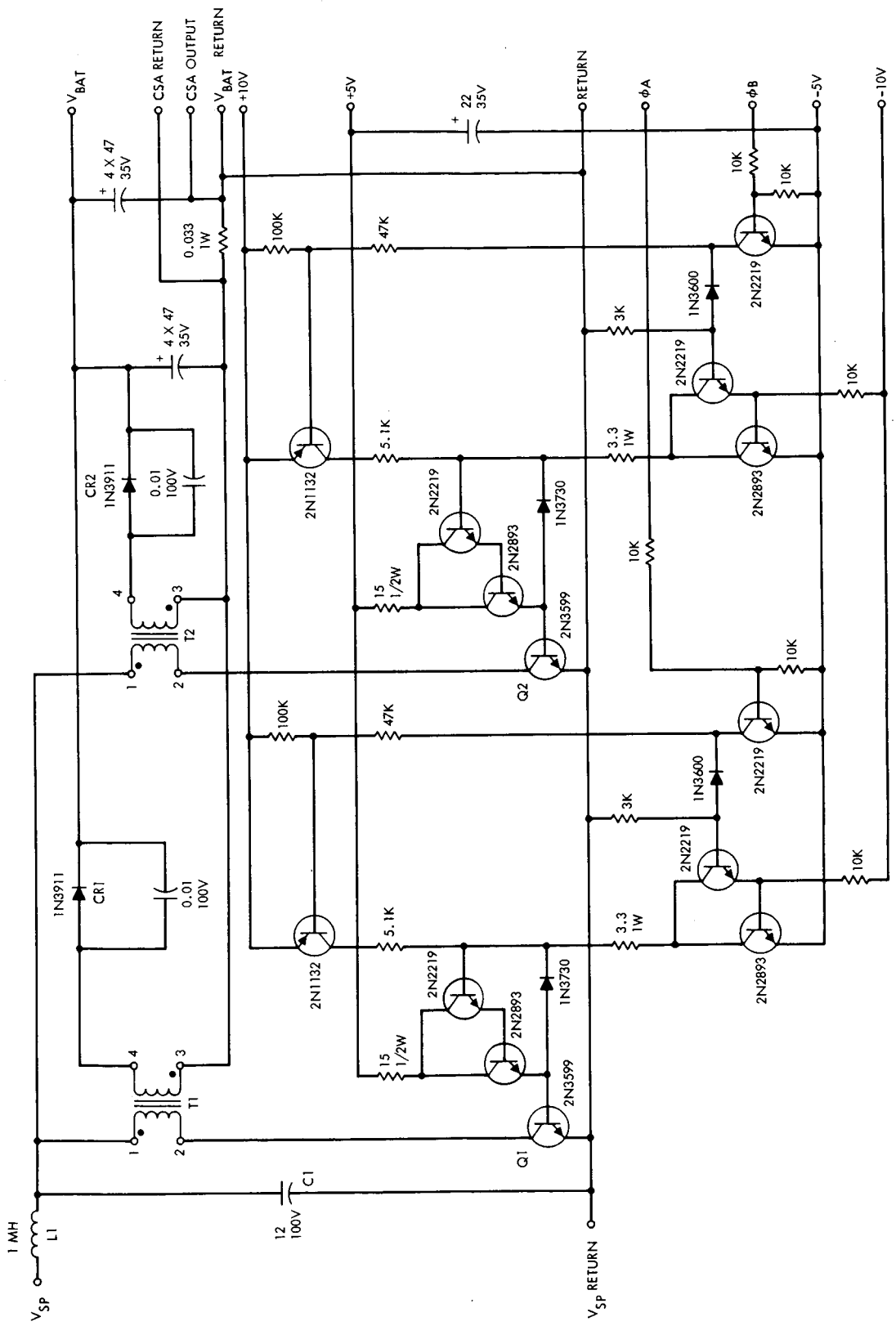


Figure 3-1. Fifty-watt, two-phase OCR switching circuit schematic diagram.

Transformer Parameters	Two-Phase OCR	Single-Phase OCR
Primary inductance	110 uh	30 uh
Secondary inductance	110 uh	67.5 uh
Turns ratio (N)	1:1	1:1.5
Peak primary current	6 amperes	18.3 amperes
Peak secondary current	6 amperes	12.2 amperes
Primary resistance	15 milliohms	15 milliohms
Secondary resistance	15 milliohms	15 milliohms
Core material	Powdered iron	Ferrite

Table 3-1. Fifty-watt switching transformer parameters.

Figure 3-2 shows the typical normalized current gain versus collector current characteristics of the 2N3599 transistor. This device is used as the main switching transistor in the switching circuit. It indicates that operating at a collector current of 6 amperes, the minimum beta (h_{FE}) of the device is about twice as high as when the device is operated at I_C = 18 amperes. Less drive is necessary to saturate the device, and consequently an overall savings in bias power is accomplished, as shown in the efficiency discussion in paragraph 2.1.4.

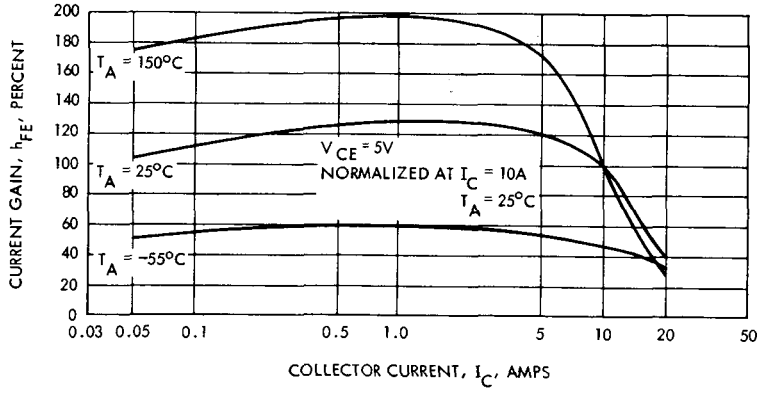


Figure 3-2. Normalized current gain versus collector current for the 2N3599.

From the photograph of the waveforms of Figure 3-3, the actual peak currents can be seen to be very close to the predicted values.

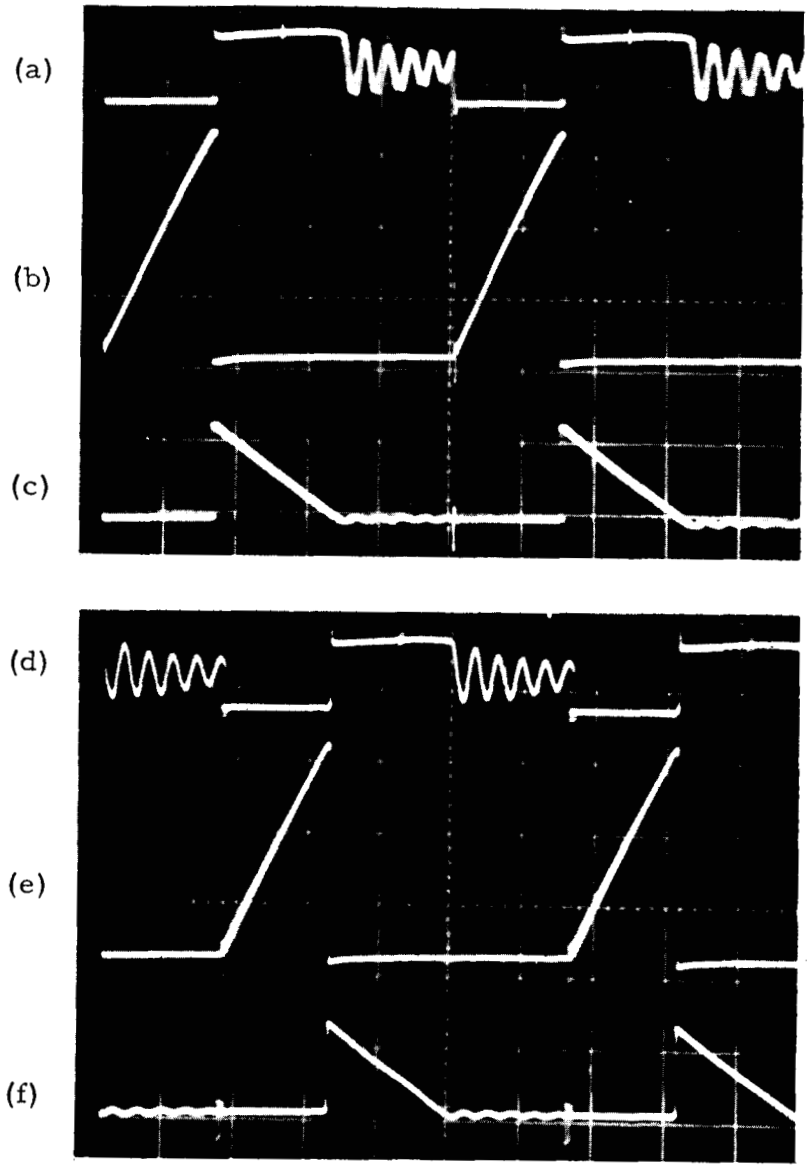


Figure 3-3. Fifty-watt, two-phase OCR switching circuit waveforms.

Vertical: (a) and (d) - 20 volts per centimeter
(b) and (e) - 2 amperes per centimeter
(c) and (f) - 5 amperes per centimeter

Horizontal: 20 microseconds per centimeter

The second major advantage of the two-phase switching circuit is that the peak-to-peak ripple of the battery current, I_{BAT}, has been reduced by doubling the phases. Figure 3-4 compares the battery ripple current of the single- and two-phase, 50-watt OCR. The peak-to-peak ripple has been reduced by a factor of 4.5 in the two-phase system.

(a)

(b)

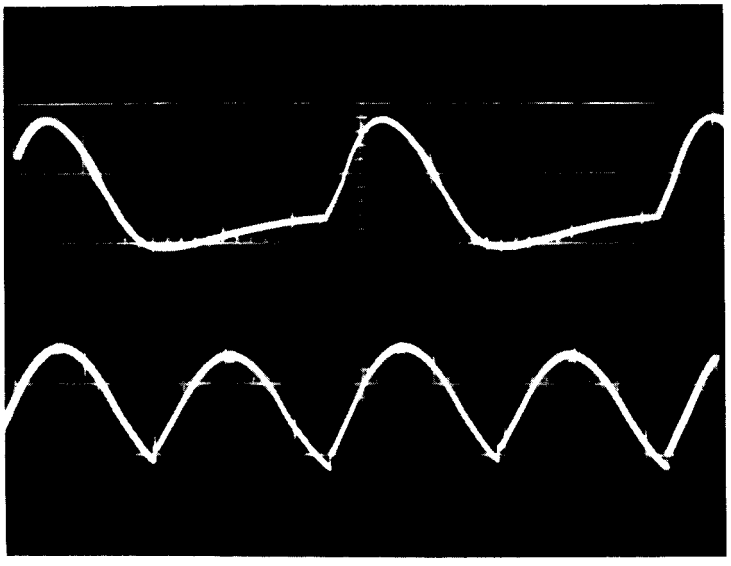


Figure 3-4. Battery ripple current — single-phase versus two-phase, 50-watt OCR.

Vertical: (a) - 4.0 amps per centimeter — single phase
(b) - 1.0 amp per centimeter — two phase

Horizontal: 20 microseconds per centimeter

Moreover by increasing the phases, the frequency of the harmonic is higher, and consequently, it is possible to reduce the size of the input and output filters.

3.2 TWO-PHASE DUTY FACTOR MODULATOR — 50-WATT OCR

The function of the two-phase duty factor modulator (DFM) is to generate two outputs which are 180 degrees out of phase. Figure 3-5 is a functional block diagram of this circuit. The 10 kHz oscillator generates two outputs, A and $\overline{A}$, which are 180 degrees out of phase. These outputs are then used to trigger ramp generators for phase A and phase B. These ramps are then compared to the integrator input. This comparison produces a duty factor variable square wave which is the final DFM output.

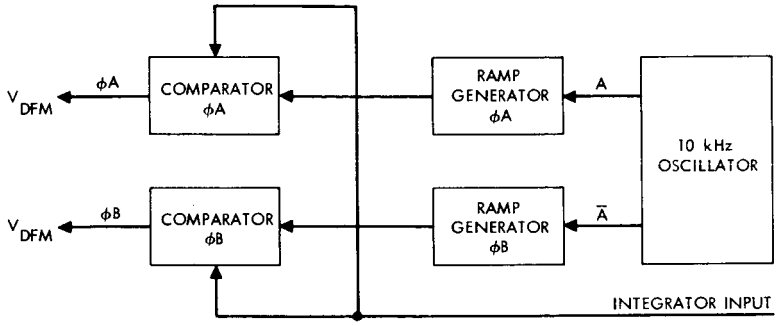


Figure 3-5. Two-phase duty factor modulator functional block diagram.

Figure 3-6 is a schematic diagram of this circuit. Transistors Q1 and Q2 comprise the 10 kHz oscillator. Ramp generator ϕA is composed of Q3 and Q4, while ramp generator ϕB is made up of Q5 and Q6. The comparators are Q7, Q8, and Q9 for ϕA, and Q10, Q11, and Q12 for ϕB.

3.3 FOUR-PHASE SWITCHING CIRCUIT - 250-WATT OCR

This circuit is identical in operation to the 50-watt switching circuit except for the two additional phases. The four phases are now 90 degrees apart.

The major difference in the four-phase system is the fact that the primary switching current now increases linearly with time to a peak current of 13 amperes compared to 27 amperes in the original two-phase system. The turns ratio of the four-phase switching transformers is 1:2 (see Table 3-2) reducing the peak secondary current from 13.5 amperes to approximately 6.5 amperes.

The savings in power losses as a direct result of the decrease in the peak currents is discussed in more detail in paragraph 2.1.4.

The other major difference between the two-phase and four-phase, 250-watt switching circuit is the increase in the switching frequency from 2 kHz to 10 kHz. This allowed for a considerable size and weight reduction in the switching transformer, although four are used now compared to two previously.

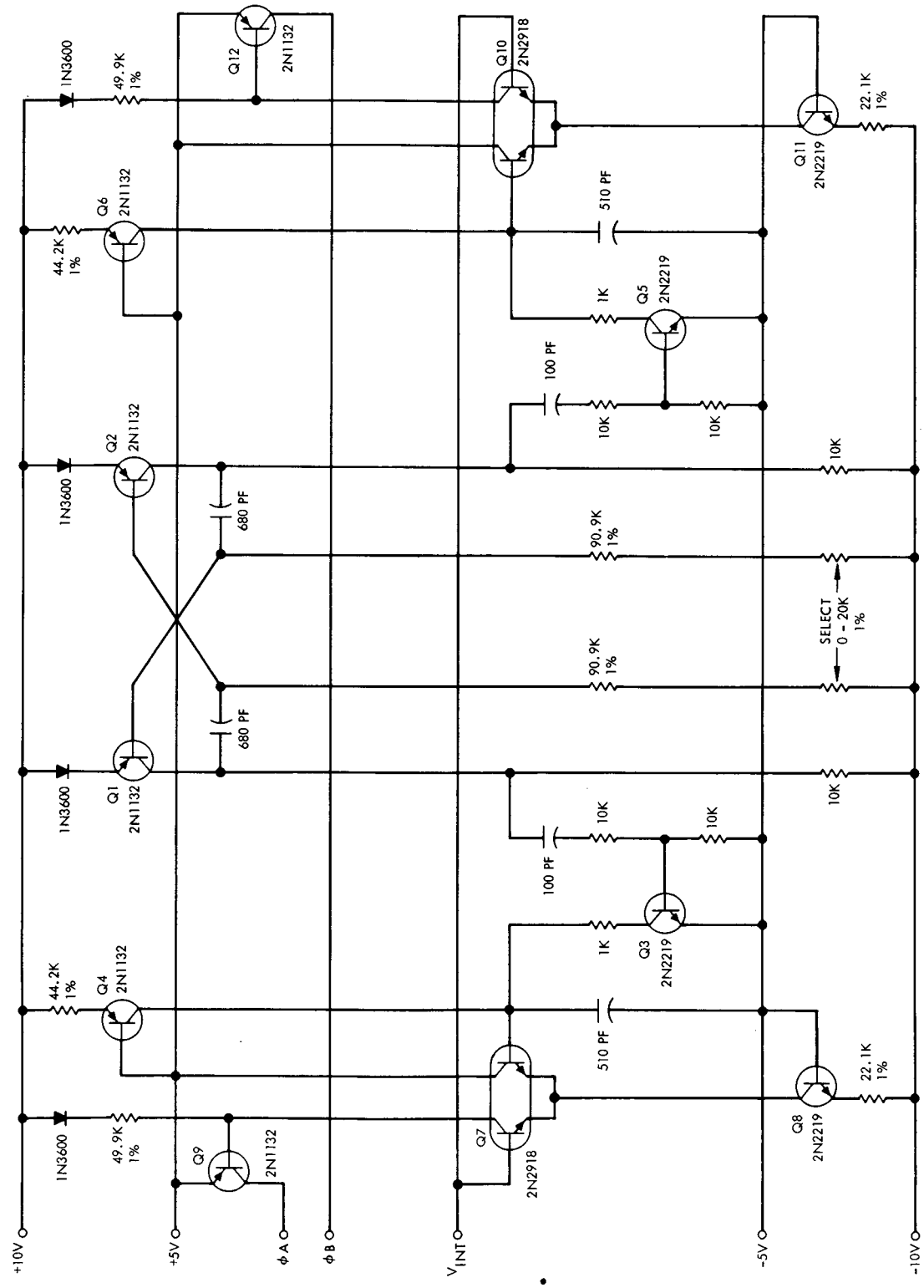


Figure 3-6. Fifty-watt, two-phase duty factor modulator schematic diagram.

Choke Parameters	Four-Phase OCR	Two-Phase OCR
Primary inductance	70 uh	170 uh
Secondary inductance	280 uh	680 uh
Turns ratio (N)	1:2	1:2
Peak primary current	13.0 amperes	27 amperes
Peak secondary current	6.5 amperes	13.5 amperes
Primary resistance	15 milliohms	15 milliohms
Secondary resistance	15 milliohms	15 milliohms
Core material	Powdered iron	Ferrite

Table 3-2. 250-watt switching transformer parameters.

3.4 FOUR-PHASE DUTY FACTOR MODULATOR - 250-WATT OCR

As in the two-phase duty factor modulator, the function of the four-phase DFM is to generate outputs to control the duty factor of the switching circuit, so that the regulator operates about the solar panel maximum power point. Four outputs are generated, each 90 degrees out of phase.

A block diagram of this circuit is shown in Figure 3-7. The circuit consists of two triggered flip-flops (FF1 and FF2), which are driven by a pulse generated by alternate half cycles of a 20 kHz oscillator. This causes the flip-flops to run at 10 kHz. The B output of FF1 leads the C output of FF2 by 90 degrees. The operation of the circuit from this point on is similar to that of the two-phase DFM. FF1 drives phase A and phase B, and FF2 drives phase C and phase D.

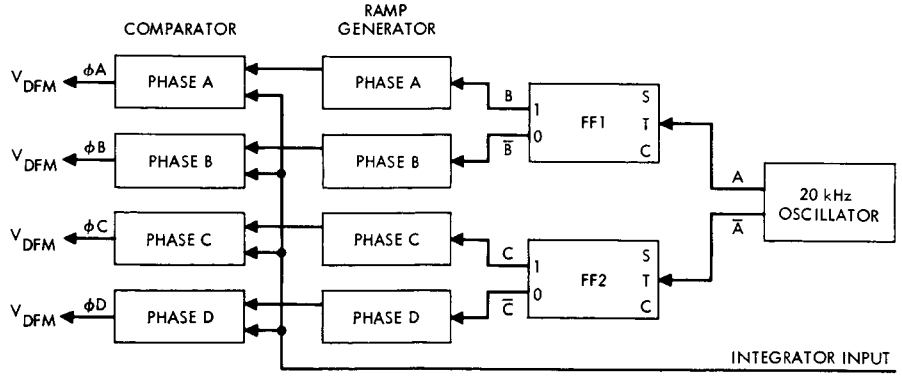


Figure 3-7. Four-phase duty factor modulator functional block diagram.

The 90-degree shift between FF1-B and FF2-C causes the comparator output for phase A to lead the comparator output for phase C by 90 degrees. Phase A is also 180 degrees shifted from phase B, and phase C is 180 degrees shifted from phase D.

A schematic of the four-phase duty factor modulator is shown in Figure 3-8. Transistors Q1 through Q4 comprise the flip-flops, FF1 and FF2. Transistors Q5 through Q16 make up the four comparators, and transistors Q17 through Q24 are the four ramp generators. The 20 kHz clock consists of transistors Q25 and Q26.

3.5 SWITCHING TRANSFORMER DESIGN

The switching transformer used for the single-phase, 50-watt, and 250-watt, two-phase OCR was fabricated from a ferrite material. Efficiency measurements determined that a major portion of the total losses in the OCR was due to core losses in the switching transformer. After extensive research into different types of cores that could possibly be used under the existing circuit conditions, it was determined that a powdered-iron (moly permalloy) core would have the minimum core loss for the same volume. In the four-phase, 250-watt unit, using the redesigned switching transformers, a reduction of 20 percent in core losses was attained.

The winding was also optimized to give a minimum leakage inductance (2.2 microhenrys) and a minimum distributed capacitance. This improved the rise time and minimized both the overshoot and ringing in the transformer.

A higher "Q" (60 compared to 20 for the ferrite transformer) was attained resulting in less I^2R losses, and a resistive rather than an inductive load-line characteristic for the switching transistors, thereby reducing the switching losses by a factor of about six.

Further study into the switching transformer design has resulted in a new theory that may reduce the losses even further. It is felt that the phenomenon known as the "proximity effect" could be an important contributor to losses in the switching transformer. When two or more adjacent conductors are carrying current, the current distribution in

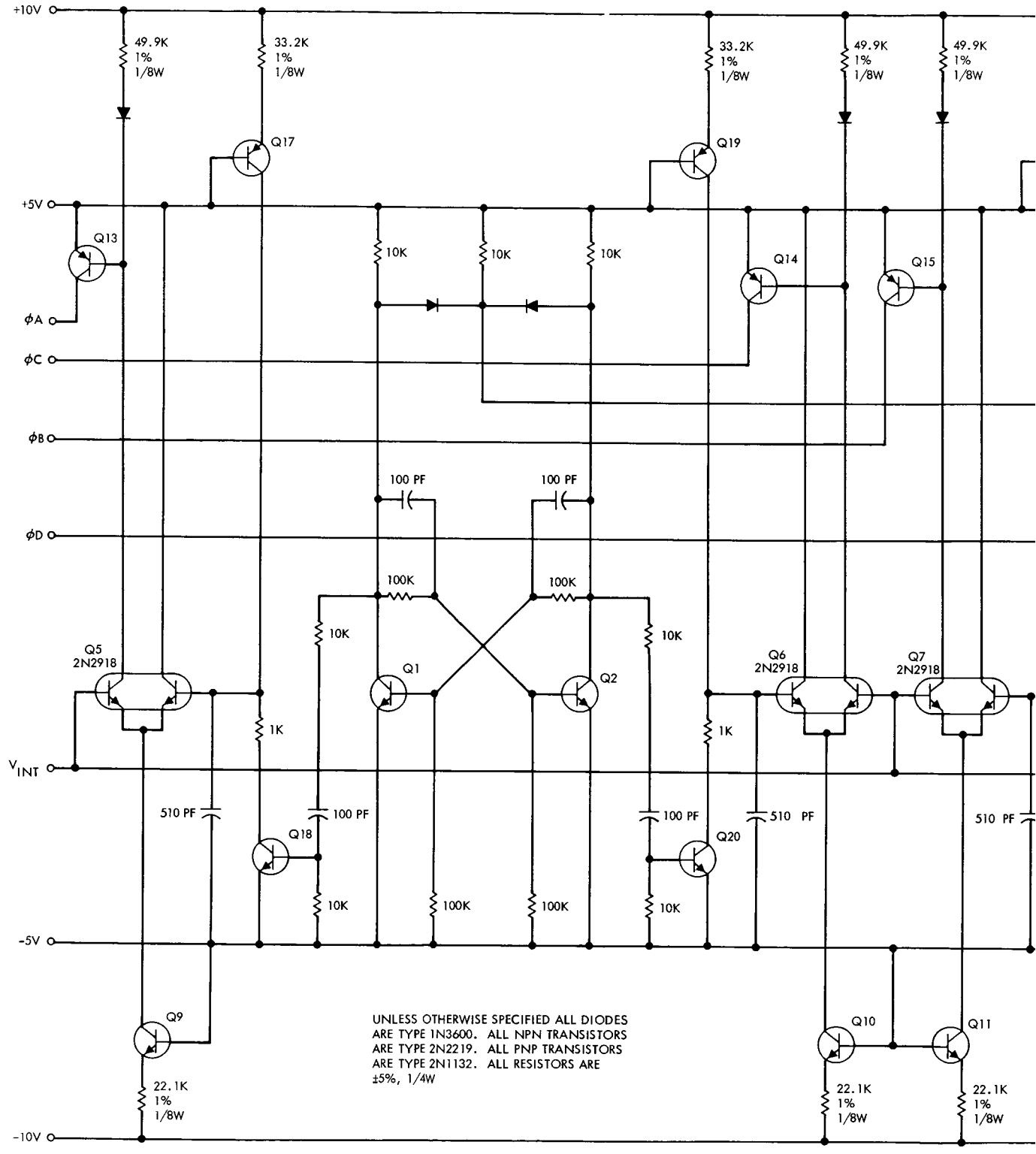
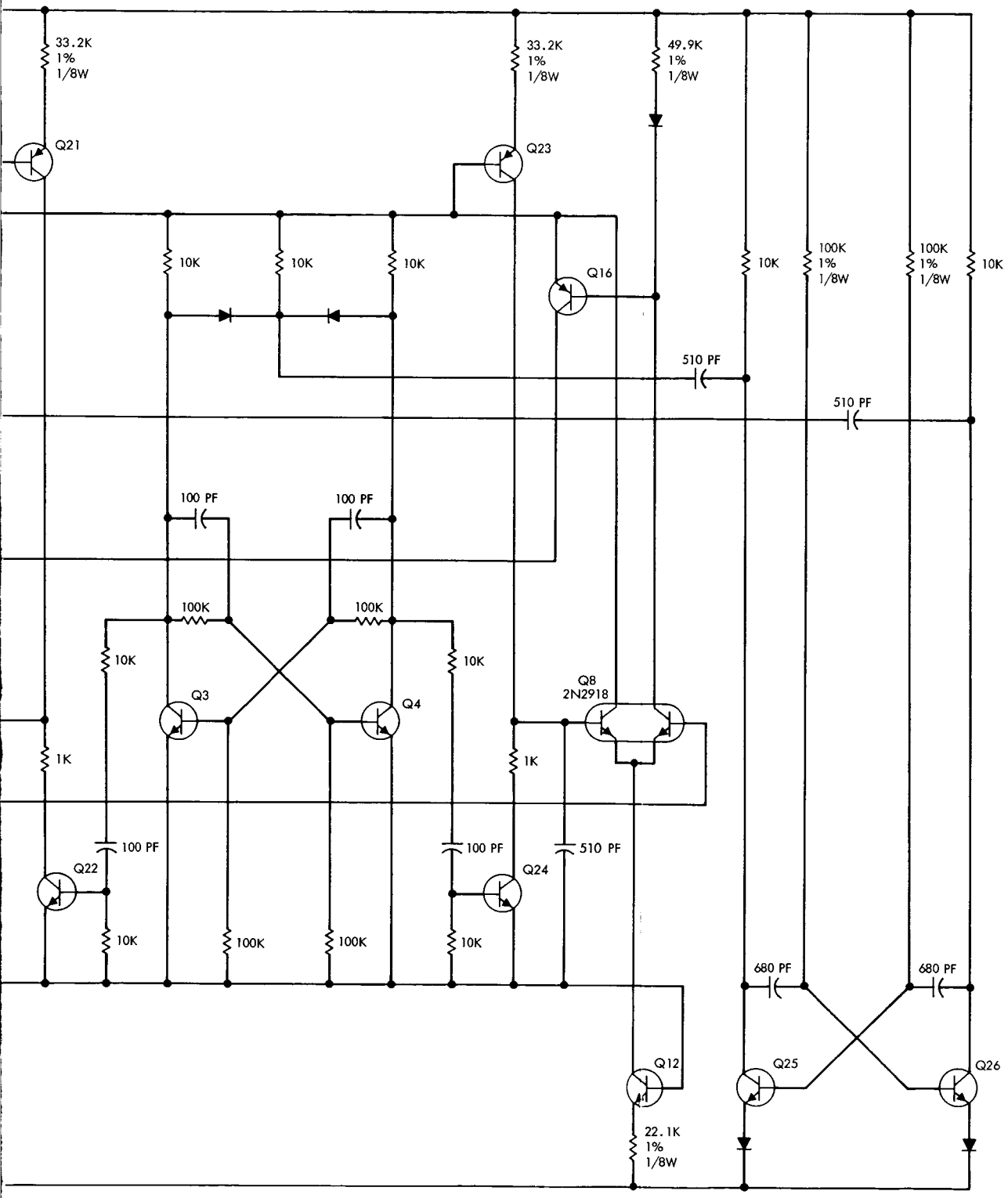


Figure 3-8. Four-phase duty factor modulator schematic diagram.


33.2K
1%
1/8W
Q21
33.2K
1%
1/8W
Q23
49.9K
1%
1/8W
10K
10K
10K
Q16
10K
100K
1%
1/8W
100K
1%
1/8W
10K
510 PF
510 PF
100 PF
100 PF
100K
100K
10K
10K
Q3
Q4
Q8
2N2918
1K
1K
100 PF
100 PF
510 PF
Q22
Q24
10K
100K
100K
10K
680 PF
680 PF
Q12
Q25
Q26
22.1K
1%
1/8W

one conductor is affected by the magnetic flux produced by the adjacent conductors, as well as the magnetic flux produced by the current in the conductor itself. The effect is termed the proximity effect and ordinarily causes the resistance ratio, which is the ratio of the ac resistance to the dc resistance, to be greater than in the case of simple skin effect. Proximity effect is very important in inductance coils operating in the lower radio frequencies. The 10 kHz switching frequency of the optimum charge regulator is within the frequency range that the proximity effect could play a part.

The resistance ratio of a conductor can be made to approach unity very closely, at least at the lower radio frequencies, by use of a conductor consisting of a large number of strands of fine wire that are insulated from each other except at the ends, where the various wires are connected in parallel. Such a conductor is termed a "Litz" or Litzendraht conductor. The result of equalizing the reactances of the individual strands of wire is to cause the current to divide uniformly between strands. This will reduce the ac losses in the wire. Practical "Litz" conductors are very effective at frequencies below 500 kHz.

In the next part of the program, Litz wire will be used on the present moly permalloy core to try to reduce the losses in the switching transformers. Wire has been ordered and delivery is expected shortly.

3.6 SIMPLIFICATION OF CIRCUITRY

3.6.1 Two-Phase Duty Factor Modulator

In the single-phase duty factor modulator a flip-flop was used to generate the V_{DFM} output pulse. In the two-phase duty factor modulator, the flip-flop and its associated resistors, diodes, and capacitors were eliminated. The output pulse to control the switching circuit is now taken directly from the comparator.

Two (2) amplifiers on the outputs of the 10 kHz oscillator were replaced by two (2) diodes since the additional gain was not required. Several base-emitter resistors were also eliminated, wherever it was determined they were not required.

Comparing the total parts count of the redesigned two-phase duty factor modulator with the original one used on the two-phase, 250-watt OCR, it can be seen that there were forty-seven less components used in the more simplified redesigned circuit (refer to Table 3-3).

Component	Original Two-Phase DFM	Redesigned Two-Phase DFM
	Quantity	Quantity
Transistor	19	14
Diode	12	4
Resistor	48	18
Capacitor	20	16
Total	99	52

Table 3-3. Comparison of two-phase duty factor modulator parts count original versus redesigned.

3.6.2 Two-Phase Switching Circuit

The input filter capacitor was reduced in size because of the lower ripple of the two-phase switching circuit. Consequently, less filtering was required, which resulted in a major size and weight savings. The input filter could be reduced even smaller in size by increasing the switching frequency and this is now being studied.

Two driver transistors and their associated resistors were eliminated because there was sufficient gain in the circuit to switch Q1 and Q2 "on" and "off" rapidly.

Several base-emitter resistors were also eliminated, wherever it was determined they were not required.

3.6.3 Four-Phase Duty Factor Modulator

This circuit was simplified in the same manner as the 50-watt, two-phase duty factor modulator. By eliminating the counting flip-flops, a considerable number of components were saved. If the original circuits

were now used in the four-phase system, four more flip-flops and their associated components would be required, and the overall circuitry would be far more complicated.

3.6.4 Four-Phase Switching Circuit

By decreasing the primary peak current in each phase, it was no longer necessary to parallel two (2) 2N3599 transistors per phase. However, in the four-phase system four (4) 2N3599 transistors are still required. Also the IN3911 flyback diodes remained at a total of four (4) since paralleling was not necessary. A total of four (4) driver transistors were eliminated (one per phase) because of sufficient gain in the circuit.

The input filter was considerably reduced in size as the result of going to a four-phase system, the ripple being decidedly less.

Transformer size was reduced as a result of less current being drawn by each phase.

3.6.5 Balance of Circuits

Throughout the balance of the circuits (peak holding comparator, bistable, integrator, and current sensing amplifier) the transistors, resistors, capacitors and portions of circuits have been changed, and in some cases eliminated. The primary thought in mind is that of optimizing both circuit operation and efficiency, and at the same time simplifying the circuits in order to reduce size and increase reliability.

4.0 BATTERY STUDY PROGRAM

The intent of the battery study program is to determine the best means of operating a third electrode charge control device with the optimum charge regulator. Since an OCR can deliver the maximum power available from the solar array at any instant, it is necessary to be able to utilize this power as it becomes available to charge the battery. In this manner, the battery size and weight, as well as the solar array size and weight, can be minimized.

The major problem involved with coupling an OCR to a battery is that of the high charging rates to the battery as the solar panel maximum power point increases. This can be especially evident, for example, in the case of a satellite which has just emerged from earth shadow. At this point its solar array is very cold, and the battery voltage is low, due to maximum use during this eclipse period. The characteristics of an OCR are such that a constant power is delivered to the battery at all times that the OCR is operating in its optimum charging mode. The satellite array maximum power would be about twice its normal value because of the cold nature of the panel. Since the battery voltage was low, the charging current would be very high. This high charging rate would tend to cause pressure build-up in sealed spacecraft cells as they neared full charge. Use of third electrode cells under these conditions would be advantageous as they would allow maximum power charging of the battery with a controlled cutoff when the battery reached full charge.

In order to properly couple the OCR to the third electrode battery, determination of the third electrode output signal with respect to the constant power charging characteristics of the OCR is of prime importance.

The cells on hand for this testing program are thirty 12AH Gulton nickel cadmium cells, six of which are third electrode cells. The testing will have three phases. The first will be to determine the characteristics of the third electrode output signal for various

charging rates. These rates have been arbitrarily chosen as C/10, C/5, and C/2. The purpose of these tests is to determine if there is any variation of third electrode output as a function of charging rate. This is necessary, due to the variation of the charge rate of the OCR, because of its constant power output characteristic.

The second phase of the program will be concerned with designing the necessary OCR control circuitry. This circuitry will be designed to be compatible with the results of the phase-one testing. A major goal in the design will be simplicity, so that parts count may be kept to a minimum, thereby maximizing reliability and minimizing size and weight.

The final phase will be concerned with evaluation of the third electrode battery with the OCR, and its control circuitry. In this phase, a 27-cell battery will be constructed. This battery will contain a minimum of three third-electrode cells. This battery will then be coupled to the 250-watt, four-phase OCR. This circuit can supply charging rates of approximately C at very low battery voltage, to approximately C/2 at or near full charge. The third-electrode characteristics will be observed under these conditions, and various optimization techniques for the control circuitry will be examined.