MS-I

Design and Develop Fast Scan Infrared Detection and Measuring Instrument

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REPORT ON PHASE IV: EXPERIMENTAL STUDY

R. Vanzetti
A. S. Dostoomian

Raytheon Company
Advanced Development Laboratory
Equipment Division
Wayland, Massachusetts

prepared for

G. C. Marshall Space Flight Center
National Aeronautics and Space Administration
Huntsville, Alabama

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

REPORT ON PHASE IV
EXPERIMENTAL STUDY

INTRODUCTION

Phase IV work was carried out in close conjunction with the program of Phase III, in view of the need to investigate technical areas where redesign could only be finalized after tentative changes yielded the necessary performance data.

Major areas of redesign evaluation were the following:

1. Target pedestal
2. Visual microscope
3. Optics alignment
4. Scanning elements
5. Detector aperture
6. Sync pulses
7. Signal processing electronics
8. Calibration devices
9. Optimum performance trade-off

For each of these areas, several solutions were tried and final changes were implemented only after having assembled enough data and experience to insure that the best solution had been identified.

The results of the instrument's operation after all final changes were incorporated have supplied the proof of the soundness of every decision made during this Phase of work.

A. Measurement of Dual 3 Input Nand Gate Integrated Circuits

Initial operation of the Fast Scan Infrared Microscope was performed in April 1965, with the helium-cooled CuGe detector. The first traces taken of the Dual 3 Input Nand Gate ICs were of a complete raster scan and of a single

line scan during transient conditions. Figure 1 shows schematic and layout of this unit, where the chip measures .050" x .050". Typical power dissipation of the various elements, as energized for IR scan, for one circuit are:

$$P_{CR5} \approx 15 \text{ mw}$$

$$P_{Q2} \approx 75 \text{ mw}$$

$$P_{R1} \approx 8 \text{ mw}$$

$$P_{CR3} \approx 1 \text{ mw}$$

$$P_{R3} \approx 1 \text{ mw}$$

P for CR1, CR2, CR4, R2, Q1, R4, Q3 is negligible. It is evident from these figures that most of the power is being dissipated by Q2, which is the area of highest infrared radiation in all of the experiments that are covered in this report.

The scan raster was made of 50 lines, spaced .0008" apart, and is shown in Figure 2. The infrared radiation emitted by each and every one of the active elements of the circuit is clearly visible, and there is a remarkable correlation between corresponding profiles of the two circuits that are supposedly identical. The scan was carried out in a steady-state condition.

Figure 3 shows a transient condition of a single line of the circuit described above. The different traces were taken at 7.2 seconds time intervals from each other and depict the warmup phase of the semiconductor device. We

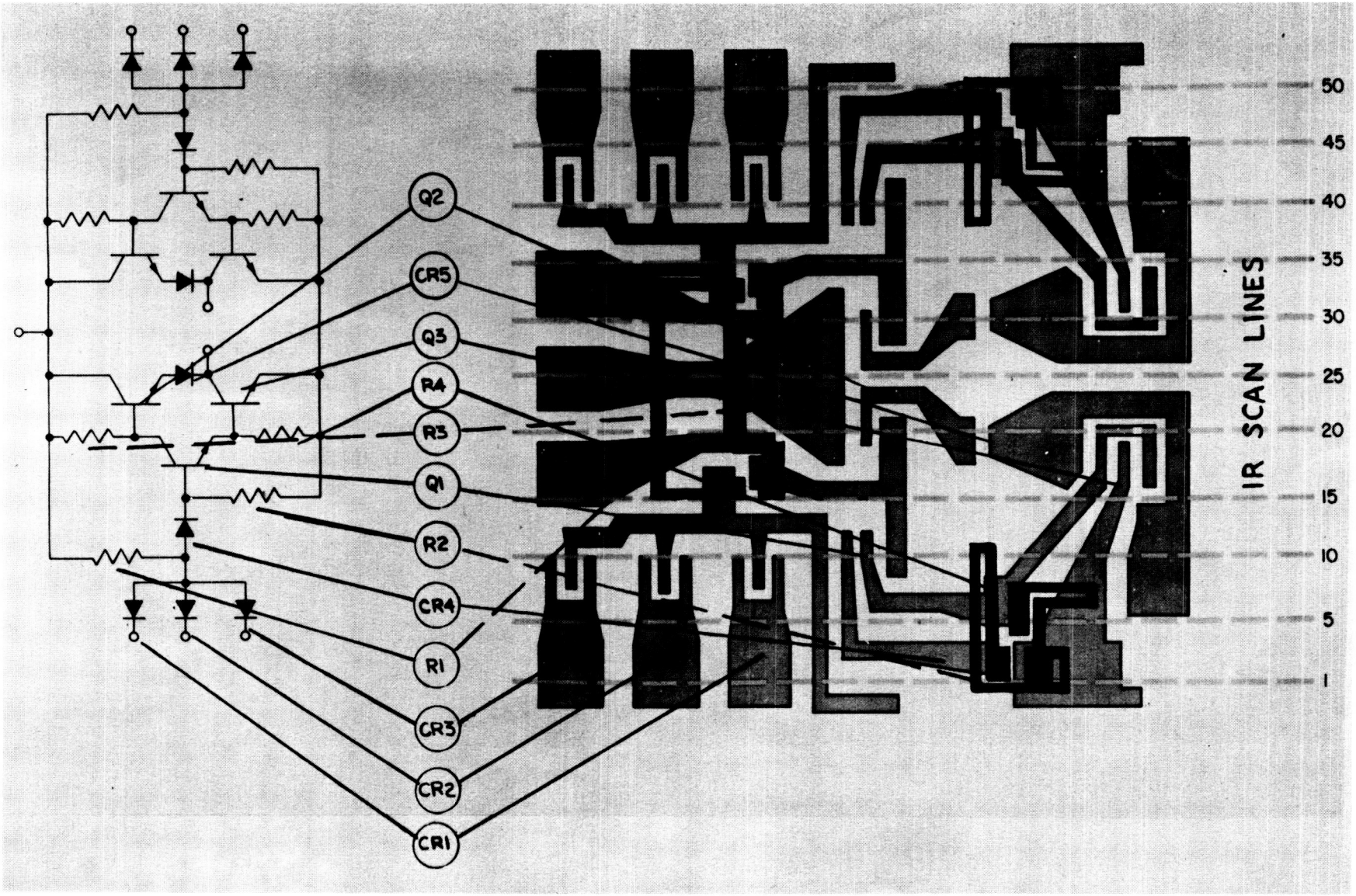


Figure 1. TWIN LINE DRIVER INTEGRATED CIRCUIT

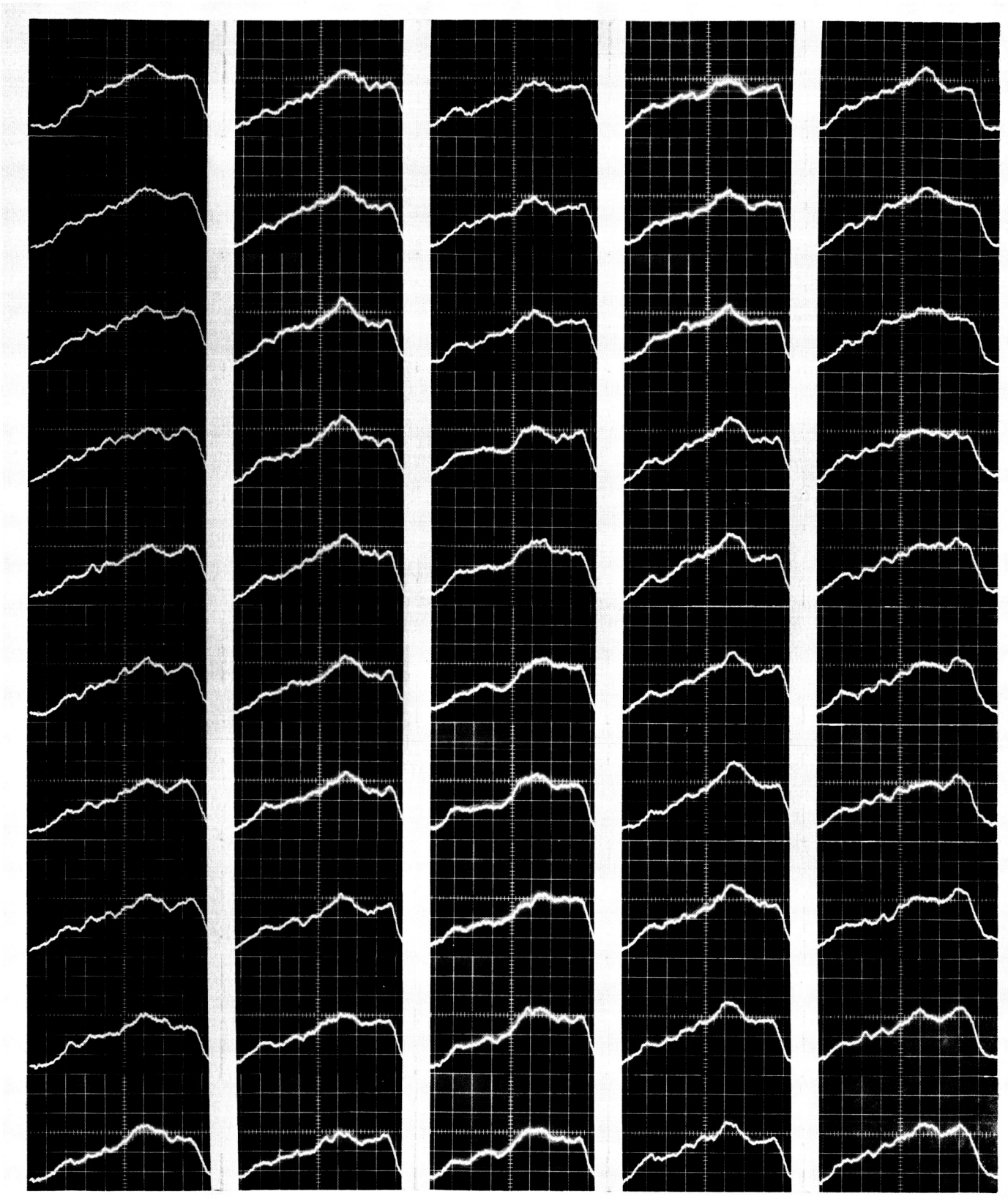


Figure 2. INFRARED PROFILES OF A 50-LINE SCAN OF IC

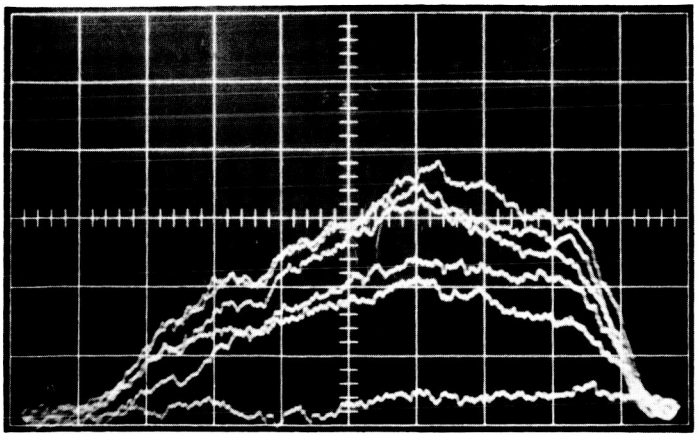


Figure 3. Transient Condition of a Single Line of IC

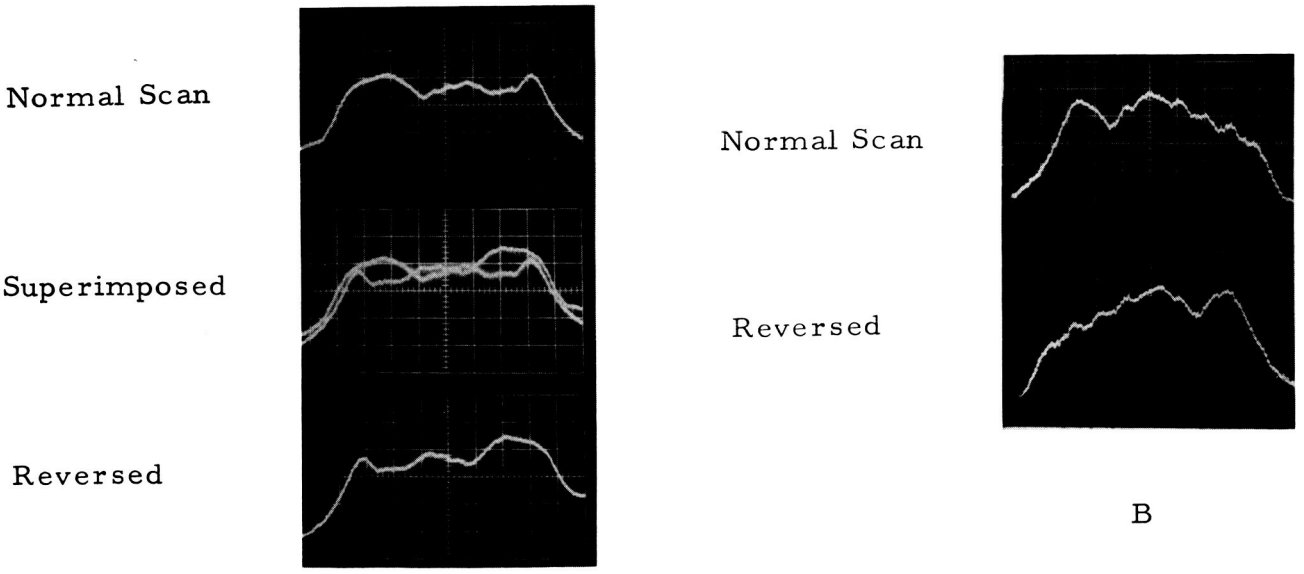


Figure 4. Alignment Tests

can see that heat build-up takes several seconds to reach the point of thermal equilibrium. This verifies the soundness of the decision to limit the scanning speed to approximately 30 lines per second. Counting the blank time at the beginning and at the end of each line, the scanning of a line takes place in approximately 10 milliseconds. At this speed, we have ample time to observe thermal buildup in every region of the target, and the higher amount of signal received by the detector allows an increase in the thermal resolution of the instrument.

During this work, the key to the occasional "slant" of the scope traces was found: imperfect axial centering of the target and untimely sync triggering of the scope were responsible. Figure 4 shows how a "slant" of the traces is detected and corrected: in A, the profile of a scan line taken clockwise is compared with the profile of the same line taken counter-clockwise. A difference in the amplitude of corresponding points is apparent. In B, this condition has been corrected, and the clockwise and counter-clockwise traces are mirror images of each other.

Figure 5 shows the line scan traces depicting the warmup characteristics of line #9 of the Dual 3 Input Nand Gate integrated circuit. The oscilloscope traces of Figure 5 show the thermal distribution along this line, taken 1 second, 6 seconds, 16 seconds, and 46 seconds, after initial energization. The temperature scale, corrected for emissivity, is approximately 20^{o}C per division, which gives a value of 75^{o}C above ambient for the highest peak of the recording. The ambient temperature is represented by the baseline. A comparison of Figure 5 and Figure 3 shows the finer resolution obtained through several stages of testing. By correction of the "slant" problem and improved alignment, the resolution (or definition) of the target was continually upgraded.

A number of scans were carried out, with the intention of establishing a "standard" profile for certain lines of the IC. It was found that thermal profiles

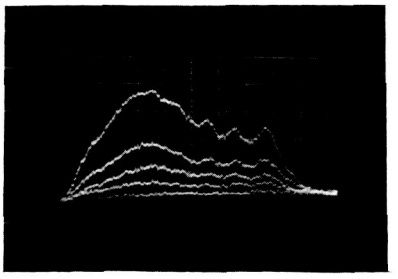


Figure 5. Transient Thermal Distribution Along Single Line of IC

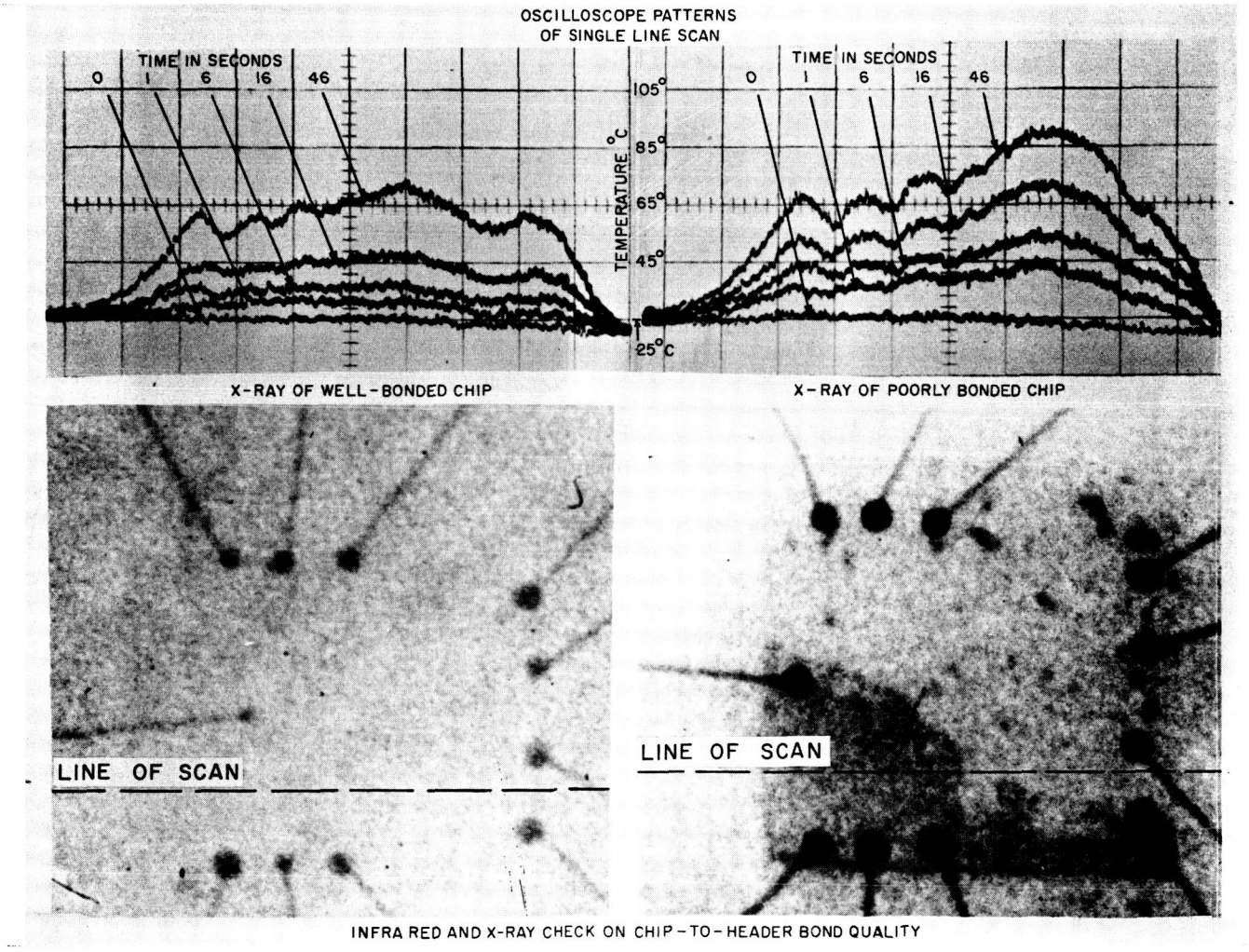


Figure 6. Evaluation of Semiconductor Chip Bonding

are consistent for "good" units identically energized, and that differences in the "elapsed time" parameter and differences in the "power dissipation" parameter produce marked changes. It was also found that "time" and "power" are somewhat interchangeable, in the sense that similar thermal buildup curves can be obtained either by holding the power dissipation level constant and taking the readings at longer time intervals, or by increasing the power dissipation level and reducing the length of time between readings. If further study should confirm these findings, it may be possible to slow down time by simply reducing the amount of power dissipation of the units under evaluation, at least within the limits imposed by the heat lateral transfer characteristics.

Chip Bonding to Header is normally done with a special cement applied with extreme care, in order to insure thorough adhesion. Bond discontinuities, such as voids or cracks, are a serious threat to semiconductor reliability, since their presence increases the thermal resistance and creates a larger thermal gradient between the chip and the heat sink. However, conventional test methods such as x-rays, visual inspection, and thermal resistance measurements, are not likely to detect these defects with 100% certitude. Infrared scanning seems to hold better promise. Figure 6 shows how the "standard" scan traces of a single line scan appear distorted by heat buildup generated by poor bonding. In the illustration on the left, the "standard" warmup traces are shown, along with an x-ray of the semiconductor chip, showing a thin, even bonding to the heat sink. On the right, the warmup traces show a large gradient toward the right side of the chip which, from the accompanying x-ray, appears cemented only through the lower edge and the left-hand corner. Thus, it seems that infrared scanning can point out the very area where a bond defect is located. Further work on this subject is needed, to determine the resolution limits of this technique.

Study of Target Coverage

Dual 3 Input Nand Gate integrated circuits were scanned in various

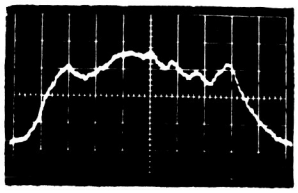


Figure 7A.
Line Scan With
1/2 inch Mirror

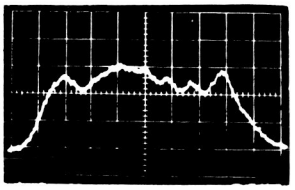


Figure 7B.
Line Scan With
1 inch Mirror

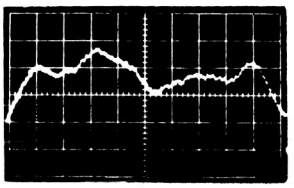


Figure 7C.
Diagonal Scan With
1/2 inch Mirror

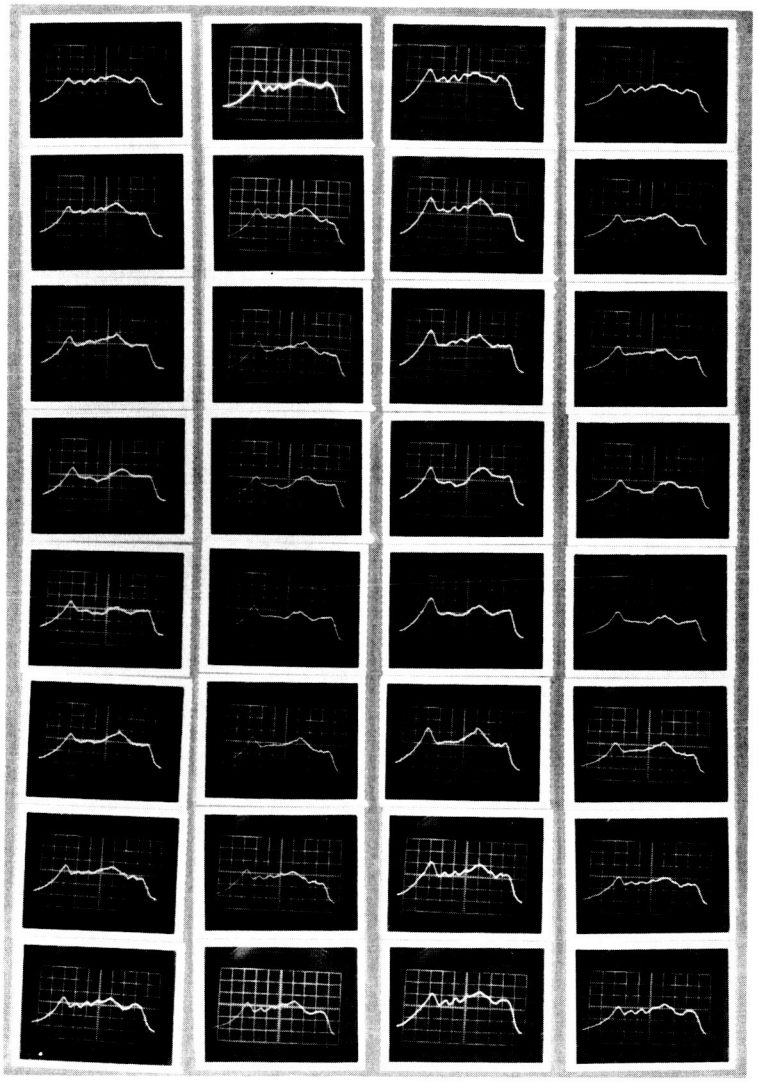


Figure 8. Power Dissipation Traces of 4 ICS

directions, in order to find the maximum area coverage of the microscope's optical system, as it was before the introduction of the last changes. Exact knowledge of the target area covered, with no distortion or loss of power, was needed for the selection of the optimum width of the mirrors in the polygon and the correlated height of the helices' pitch. Figure 7A shows the oscilloscope trace of scan line #8, taken with a polygon mirror 1/2" wide. Figure 7B shows the same trace taken with a mirror 1" wide. Figure 7C shows the trace of a scan taken diagonally across the semiconductor chip, which measures 0.072" from corner to corner. Figure 7C proves that the microscope can cover a target as large as 0.072" x 0.072", at least, without appreciable aberrations. Figures 7A and 7B seem to prove that an increase in the polygon mirror's size does not add any significant improvement.

Power Dissipation Variations

Four Dual 3 Input Nand Gate integrated circuits were raster scanned, with every fifth line being recorded on Polaroid film to minimize the amount of photographs. An analysis of the traces in Figure 8 shows the following results:

1) 8A and 8B have the same profile
2) 8C has the same basic shape as 8A and 8B, but is slightly higher in amplitude
3) 8D has the same basic shape as 8A and 8B, but is lower in amplitude.

From the power dissipation and the performance of the chip, the amplitude of the infrared profile correlates with the expected levels. There were no changes in the IR radiation level from one side of the chip to the other, even though the anomalies affected one side. This seems to indicate that the microscope is depicting the temperature profile of the chip, with difference in emissivity accounting for the shape of the curve superimposed on the basic radiation level.

Circuit Number	Volts One Circuit	Total Current	Watts	Electrical Characteristics
8A	3.0	63 ma	189 mw	Good
8B	3.0	63 ma	189 mw	Good
8C	6.0	63 ma	283.5 mw	Output shorted
8D	3.0	35 ma	94.5 mw	Output open

Figure 9 shows the power dissipation of one circuit of each chip. The other circuit was operated normally at 3.0 volts. In this particular instance, open or shorted output conditions can also be detected by conventional test methods, but in large scale integration this is impossible for those circuits that don't have outside connections. In this case, infrared scanning appears as the natural tool for power dissipation measurement.

A Dual 3 Input Nand Gate integrated circuit, meeting all electrical specifications and matching the standard profile, was scanned for all 50 lines. The pictures taken of the 50-line scans in Figure 10 were enlarged 10X and used as patterns to make a three-dimensional model of the radiation of this IC, shown in Figure 11.

It is evident from all the data and illustrations that the infrared profiles of a good Dual 3 Input Nand Gate IC consistently shows the same pattern. Other integrated circuits should also have an infrared profile that can be identified respectively with each type. Similarly, every failure condition has its own unique infrared profile, which is typical of that condition.

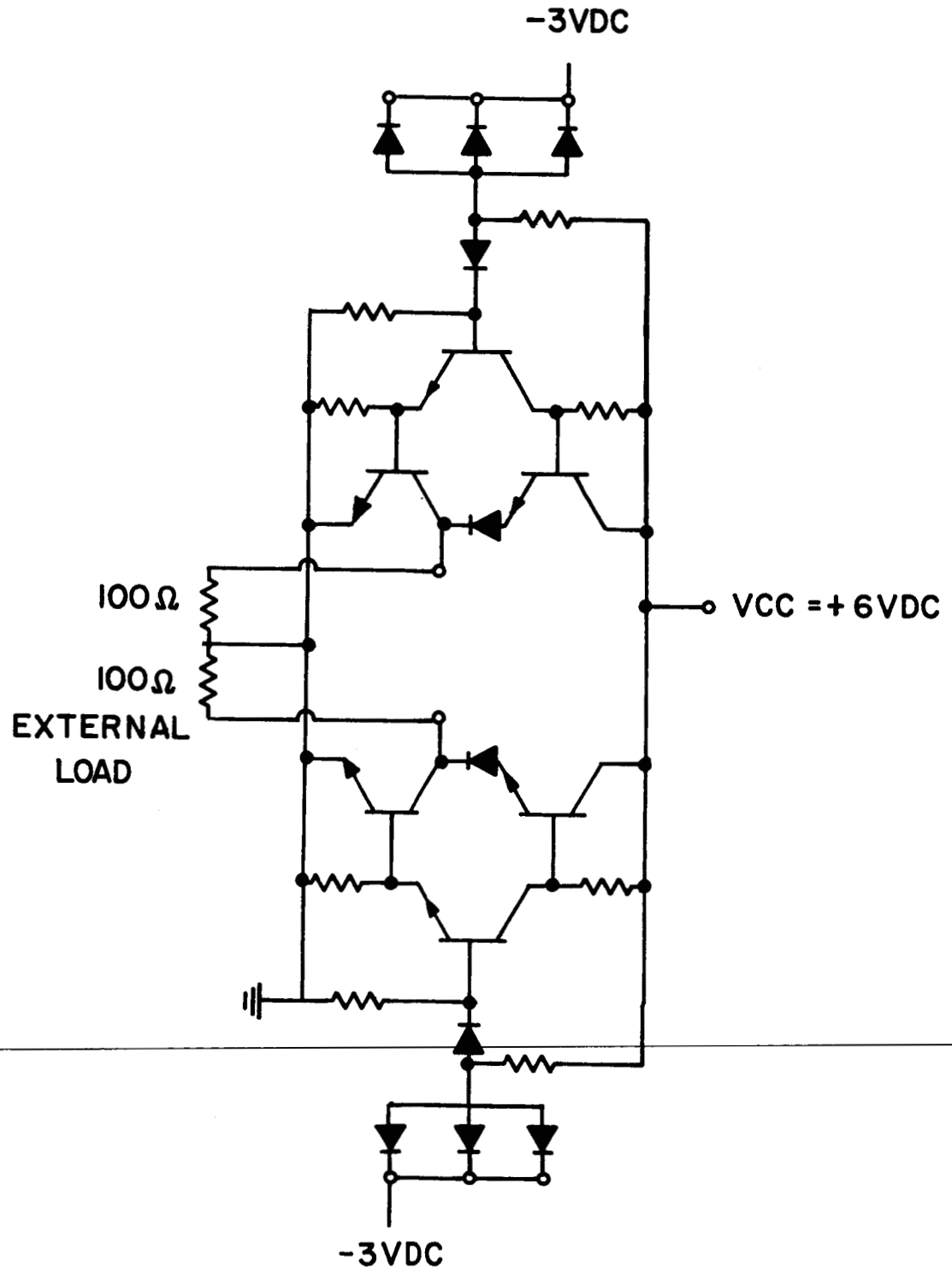


Figure 9. POWER DISSIPATION OF ONE CIRCUIT

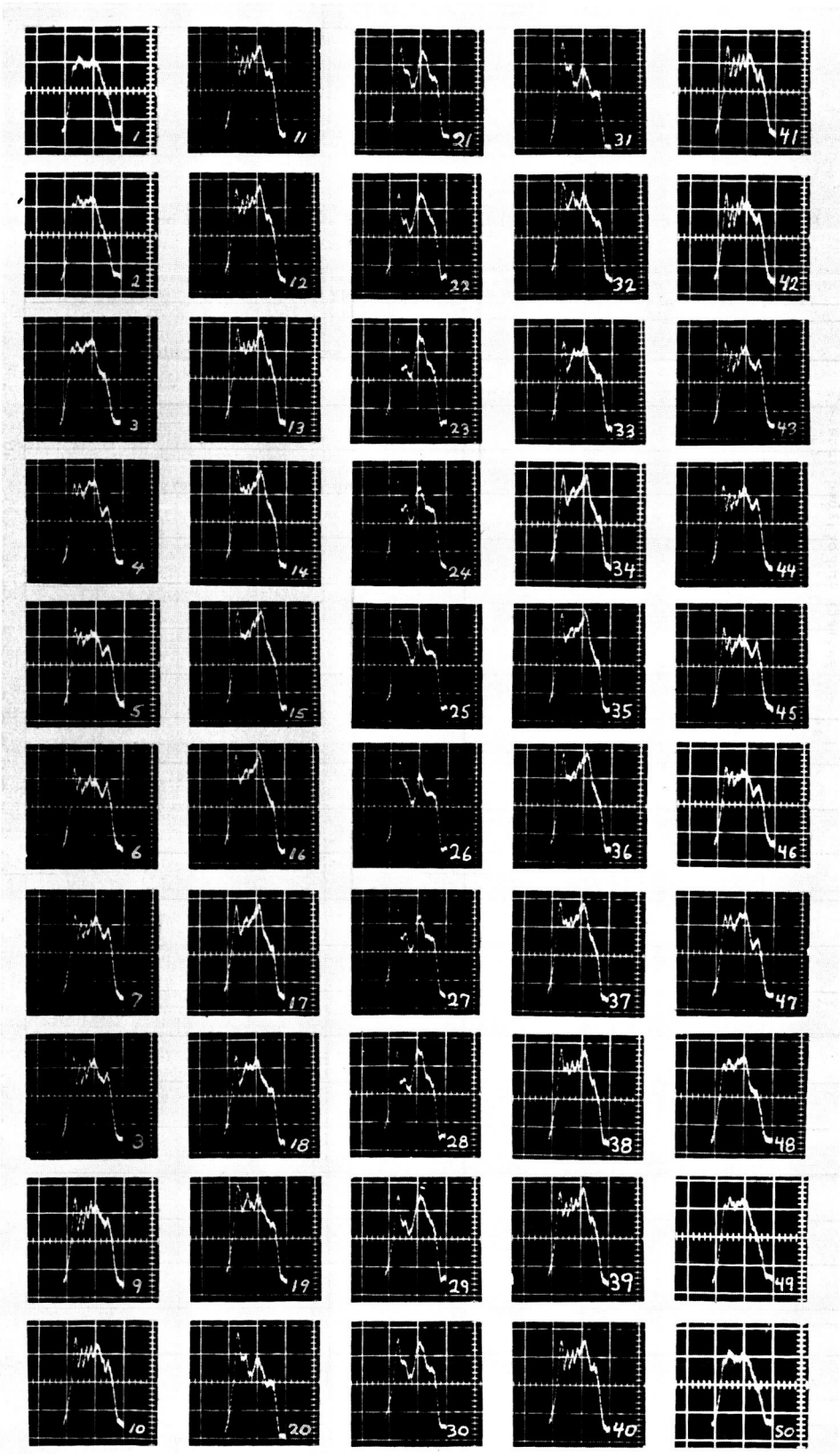


Figure 10. 50-Line-Scan Standard Profile for IC

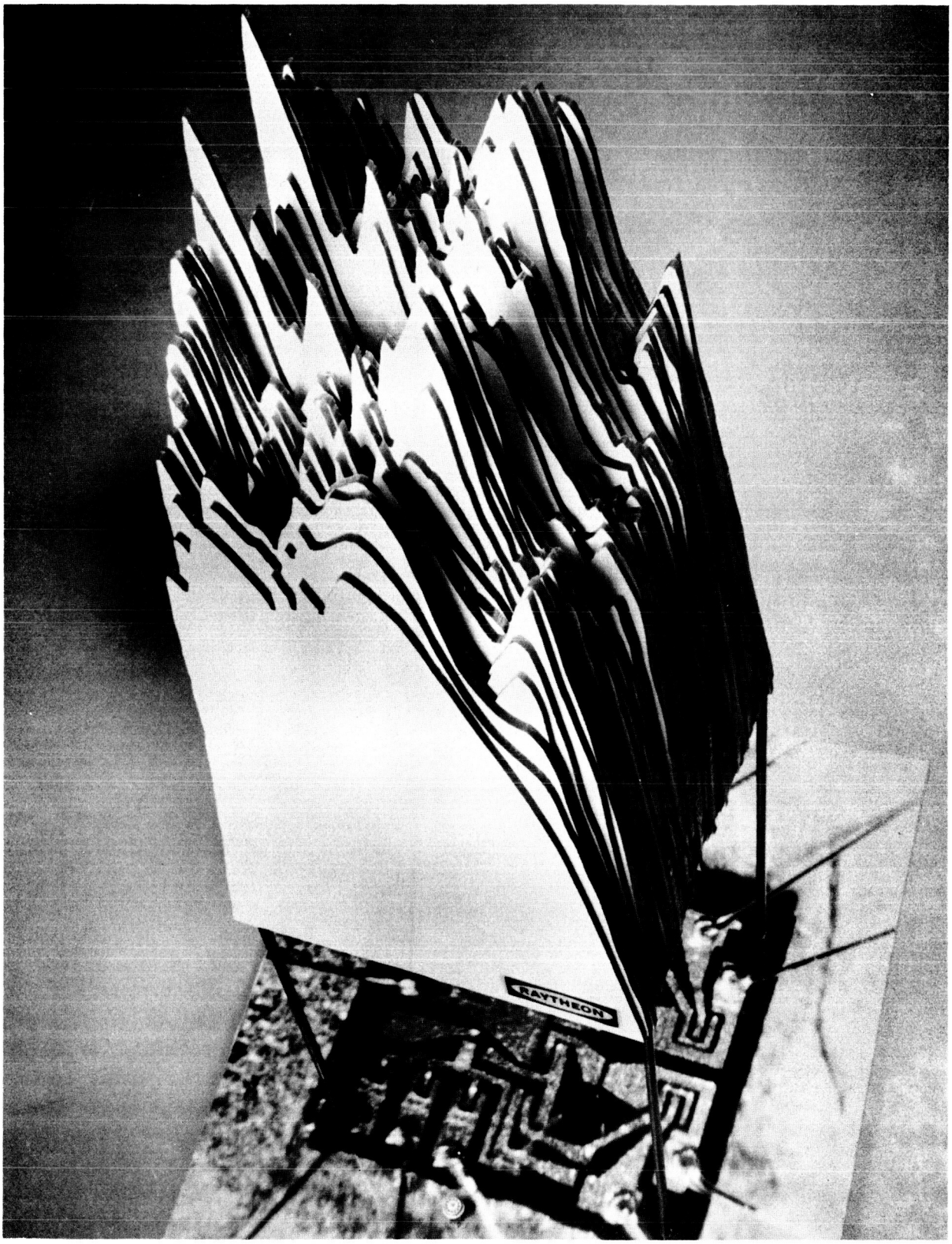


Figure 11. 3-D Model of Infrared Radiation

B. Analysis of Second Breakdown

The first attempts at testing power transistors for second breakdown, using infrared techniques, were made in May 1966. The effort was on NASA-supplied Type 2N1722 power transistors (Figure 12).

Since the physical size of these units is many times larger than the area covered by the field of view of the microscope, the target was moved in the focal plane in order to allow scanning of the whole surface one section at a time. During this operation, a condition of secondary breakdown was noticed. In the area contained within the A-B-C-D square shown in Figure 13, a transient high-radiation peak occurred at every pulse, when the unit was energized in a back-bias configuration by a Tektronix 565 Curve Tracer operating in the oscillator sweep mode.

Figure 14 shows in B the scope traces of two scan lines taken exactly at the same location, depicting the infrared profile when the point where the secondary breakdown takes place is in, or is out of, avalanche mode. Due to the frequency at which the energizing pulses occur (120 cps), thermal runaway is avoided and the transistor is electrically functional. This condition, discovered by Mr. Michael Nowakowski of NASA Huntsville while personally operating the microscope, could never previously be observed because of lack of detecting equipment capable of operating at adequate speed. Figure 14 shows in A the scope trace of the secondary breakdown condition, as generated by the Tektronix 575 Curve Tracer.

It seems superfluous to point out the importance of this discovery. The capability of identifying a secondary breakdown point, without seeing the semiconductor flashing to destruction in a fraction of a second, will permit the study of the condition that causes a secondary breakdown to occur. From this knowledge, the removal of the cause will be possible, thus eliminating the possibility of a whole class of semiconductor failures. Among the several causes for

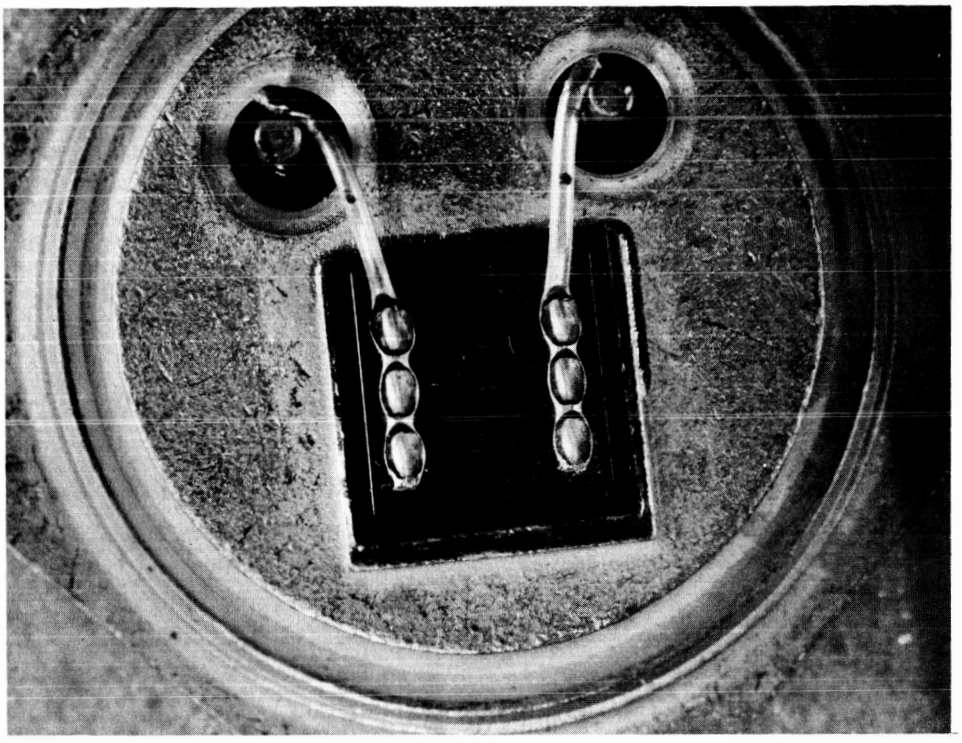


Figure 12. Power Transistor Type 2N1722

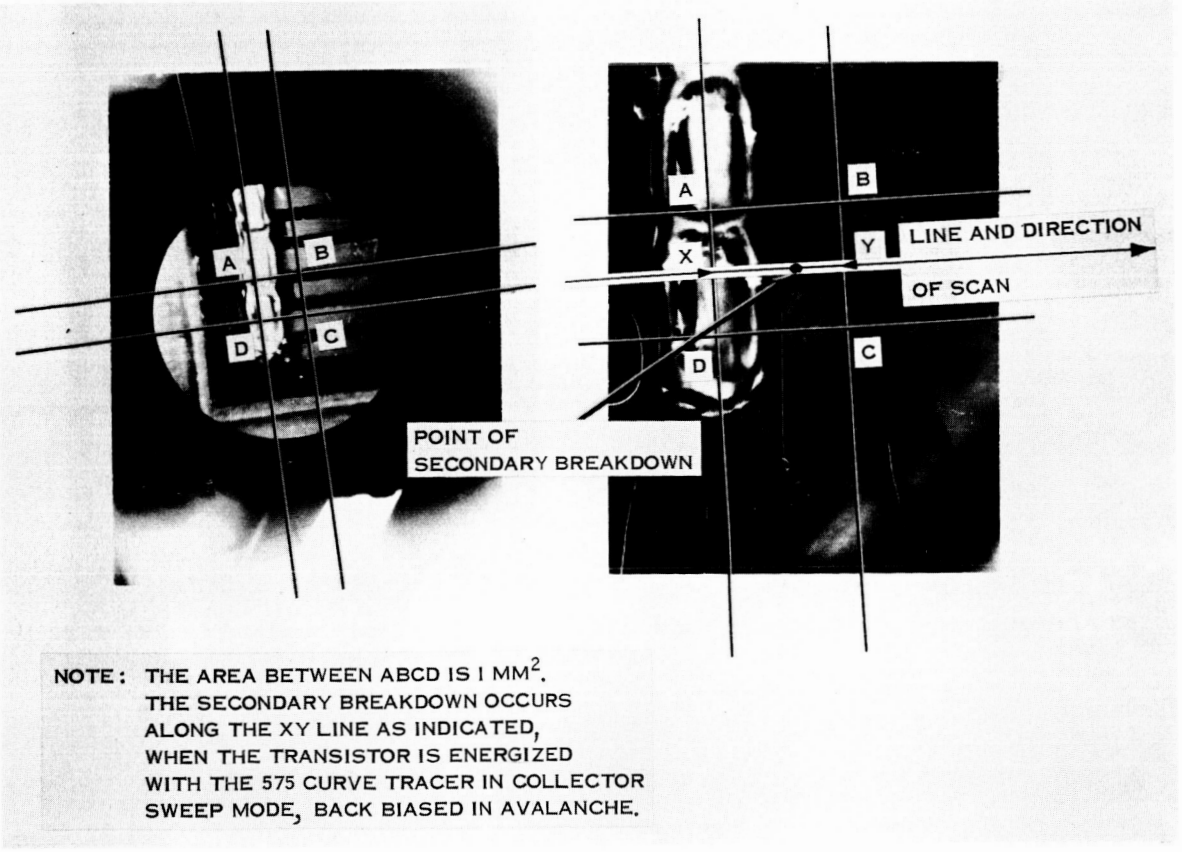
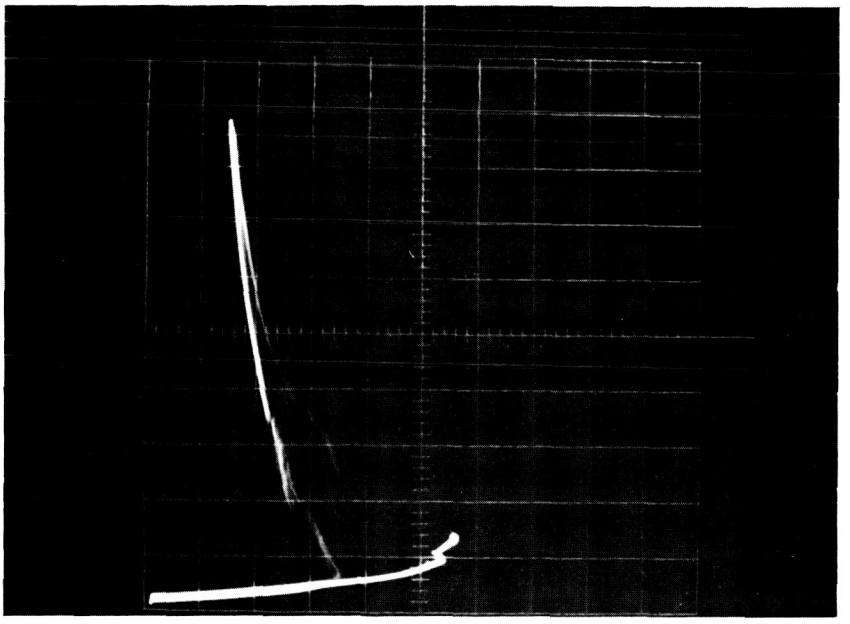


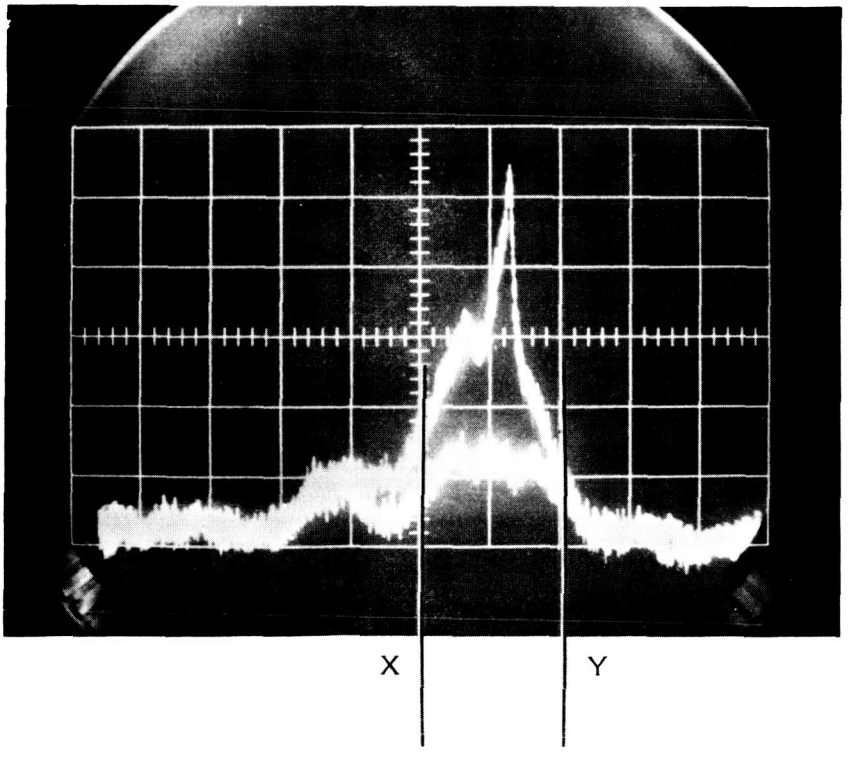
Figure 13. Area of Secondary Breakdown

A



TEKTRONIX 575 OSCILLOSCOPE TRACES OF 2N1722
BACK BIASED IN AVALANCHE MODE

B



LOWER TRACE: NORMAL OPERATION
UPPER TRACE: SECONDARY BREAKDOWN CONDITION

Figure 14. Transistor 2N1722 Traces of Secondary Breakdown

secondary breakdown, the following have been hypothesized: excessive localized doping, impurities, lattice deformation, physical spikes of the deposited material, crystal stresses, etc.

A matrix was made up as an overlay (Figure 15), in order to facilitate area identification on the transistor. Due to the large size of the chip, the surface was divided into five vertical rows from A to E, each of them 1-mm wide. The scanning took place at thermal equilibrium, moving the x-scan line along each row from top to bottom, and observing the oscilloscope trace. Polaroid pictures of these traces were taken at pre-programmed points, as shown in Figure 16, where the letters identify the rows, and the numbers indicate the distance in thousandths from the bottom of the chip. This unit exhibited thermal anomaly in the area where the avalanche process is located.

This thermal anomaly, detectable before the secondary breakdown (SB) takes place, became more and more conspicuous every time the unit was operated in the second breakdown condition. Evidently, the heat developed at the negative resistance point was progressively damaging the area around it. Figure 17 shows in pictures D-125, D-140, and D-150, the traces of this area before the SB condition is reached. Figure 18 shows the oscilloscope traces of this same area taken before, and during, the SB process. The V_{CE} readings in these two modes were respectively 50V and 55V. This same area was also scanned after it had been rotated 90^{o}, as shown by the pictures 0-D, 10-D, 20-D, 30-D, and 40-D. Since the beginning of the experiments, the transistor was operated approximately 15 times in the SB mode, for an average of 30 minutes each time. Finally, during a routine electrical check, the unit failed, because the deterioration of the SB area had reached such large proportions.

Figure 19 shows the oscilloscope traces of 14 selected line scans of another transistor investigated for SB. For each of these lines, rows 1 and 3 were taken with the transistor energized in the back-bias configuration, using

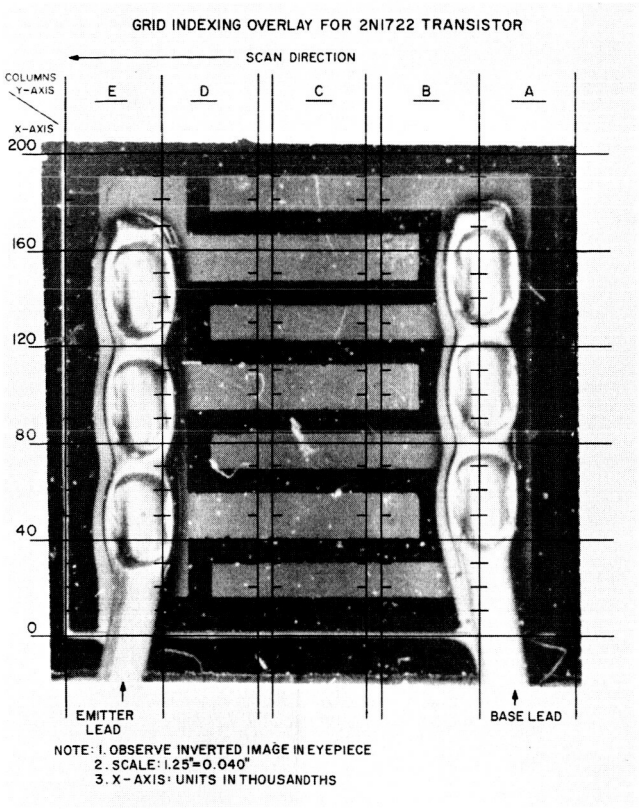


Figure 15. Method of Scanning

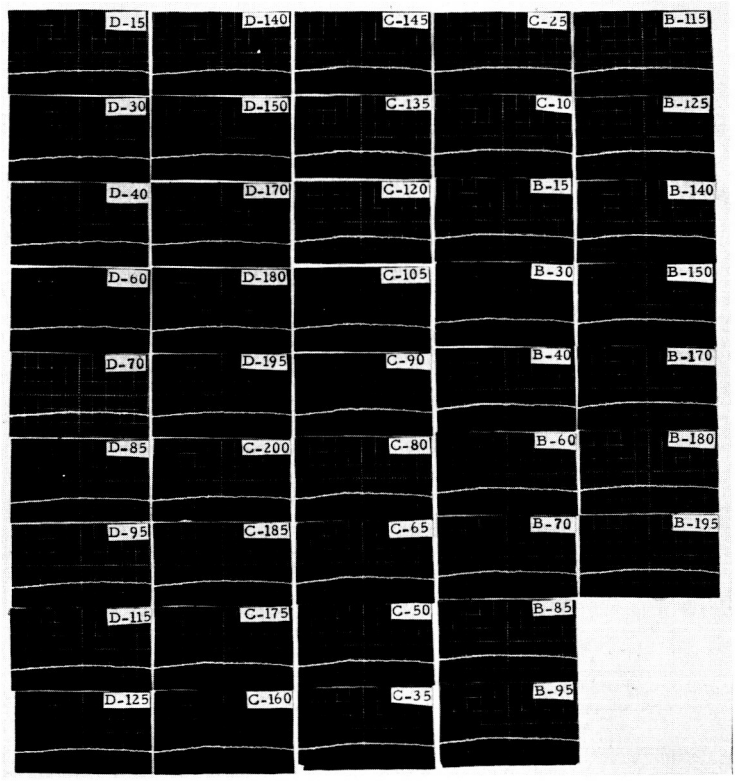


Figure 16. Scan Traces of Type 2N1722 Transistor

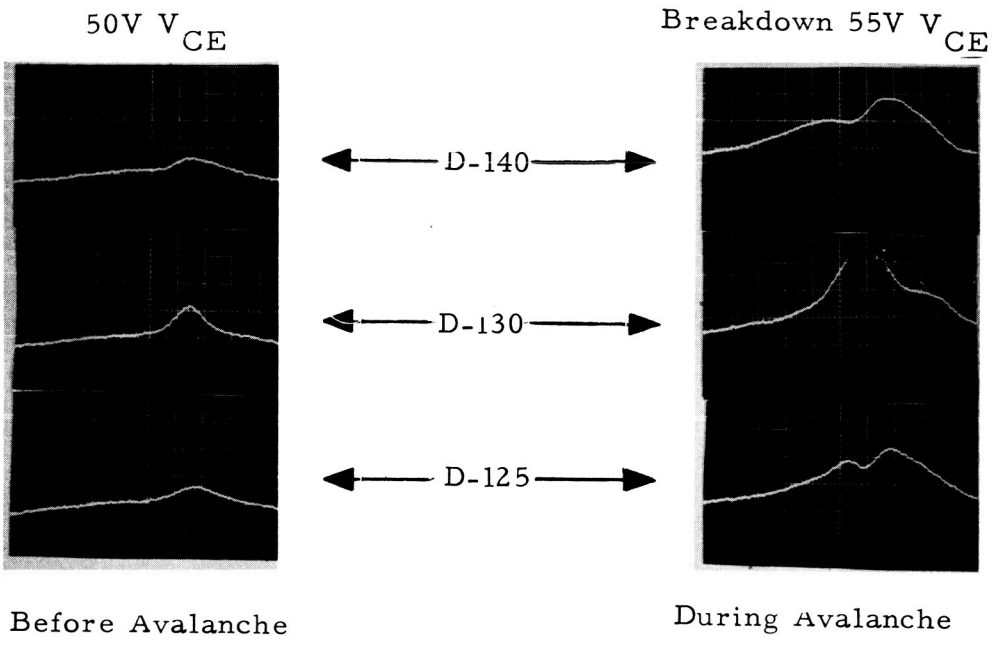


Figure 17. Scan Traces of Type 2N1722 Transistor with SB

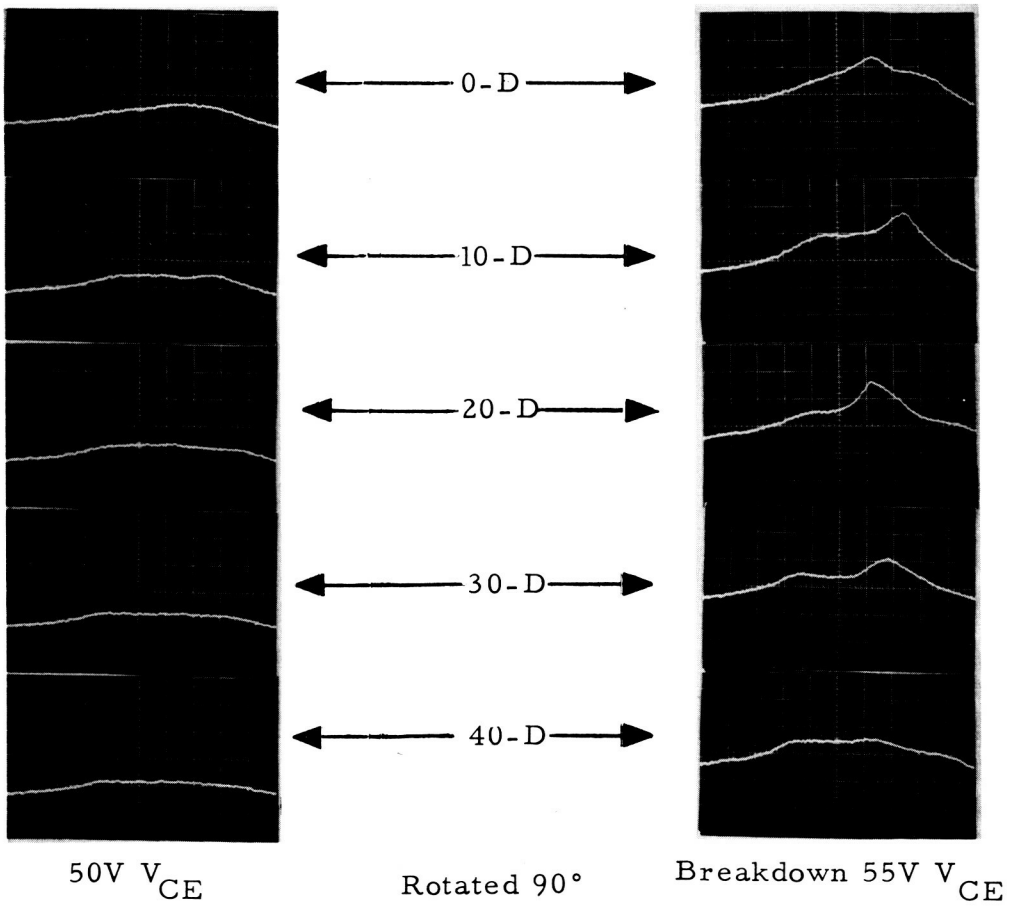


Figure 18. Scan Traces of SB Area of 2N1722 Transistor

Power Transistor 2N1722

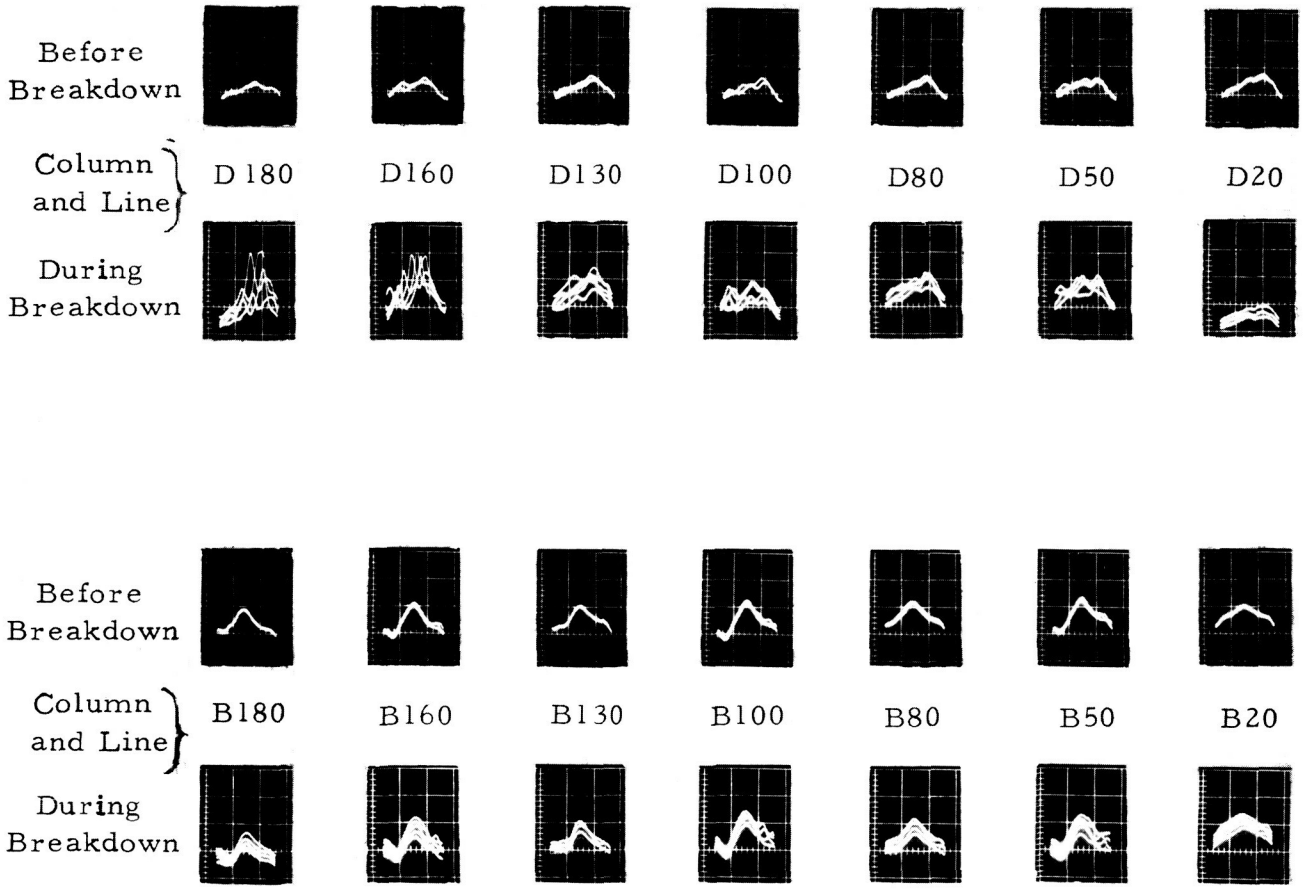


Figure 19. Infrared scan lines, before and during second breakdown

the Tektronix 575 Curve Tracer operating in the oscillator sweep mode, at a power level just below the breakdown point. The lower traces (rows 2 and 4) were taken on the same lines, at a power level just above the breakdown limit.

The breakdown condition shown in Figure 19 is quite interesting. Contrary to the usual configuration where only one point of breakdown is present, this unit is exhibiting several breakdown points, all located in the area of column D. Also of great interest is the capability of forecasting the general area where the breakdown is going to occur. This is accomplished by examining the scan traces at lower-than-breakdown power levels.

These traces are line scans of 10-millisecond duration, taken at 1-second intervals, and are depicting a fast semiconductor warmup, which would rapidly cause thermal runaway if allowed to continue. Where the thermal buildup shows scan traces neatly stacked above each other, breakdown is not going to occur. Where the thermal buildup curves are of different sizes and shapes, breakdown will take place, as evidenced by the curves in rows 2 and 4.

Careful analysis of the transistor in the breakdown area will probably disclose the cause; but even without this knowledge, infrared scanning can detect units prone to SB before the actual breakdown process takes place.

Another group of Type 2N1722 tested for SB had the following electrical characteristics:

Transistor	ICBO	IEBO	BUCEO	VBE	BCE	SB at
	μA	MA	Volts	Volts	Volts	Amps
#26	3	.7	124	.105	.219	0.15
#28	0	1.1	124	.108	.238	0.9
#29	2	.6	100	.107	.232	1.0
#30	1	1.0	108	.106	.228	*see page 9
#31	1	1.7	126	.115	.307	None

The first four units were tested during SB, and at a level below SB, to locate the point of breakdown. The following is a summary of the test data taken on the five transistors. Figures 20 through 24 are the oscilloscope traces of the 14 scan lines that are of interest, because they show variations related to the SB condition. For each of the lines B and D, scans were taken with the transistors energized in the back-bias condition, using a Tektronix 575 Curve Tracer operating in the oscillator sweep mode at the power designated in each figure.

Figure 20, Transistor #26. Breakdown occurred at approximately .2 amps and was evident on line D-60. There was a small hot spot on line D-50, but no breakdown occurred at that point. Tests were also run at .1 amperes, but no indication of impending breakdown was noticed.

Figure 21, Transistor #28. Breakdown occurred at approximately .7 amps and was evident on lines B-100 and B-160. The breakdown occurred from B-100 to B-160, but in some areas was not observable because hidden under the base land located between B-122 and B-138. Tests run below breakdown at .600 amps and at .4 amps showed hot spots at the same points.

Figure 22, Transistor #29. Breakdown occurred at approximately .9 amps and was evident on lines D-50, D-80, and D-100. Tests run below breakdown at .6 amps showed hot spots at D-50, D-80, and D-100. Tests run at .4 amps showed a detectable hot spot at D-50.

Figure 23, Transistor #30. Allegedly a good unit, it was run at .6 amperes and some thermal irregularity showed at line D-180. Current was increased to .9 amperes and after scanning lines D-20, D-50, D-80, and D-100, the transistor went into SB at approximately .15 amps. Scanning the remainder of the chip at .15 amp found D-180 to show a detectable hot spot. Further scanning showed E-180 to be the point of secondary breakdown. This point (E-180) is on the outer edge of the chip.

Figure 24, Transistor #31. This chip was scanned at .6 and .9 amperes, but no anomalies were found. This transistor also tested OK on conventional testing.

In scanning the above transistors, it was found that when the emitter was viewed, the traces showed 2 waveforms that alternated during warmup (see Figure 25d). It should be kept in mind that the pulses coming from the Tektronix Curve Tracer are occurring at a rate of 120 cps, while the scan traces are taken at 1-second intervals, for a duration of 10 milliseconds each.

Every other trace is photographed in Figures 25a and 25b, whereas 25d and 25e are every trace. Figure 25c shows lines 1, 2, 5, 6, 9, and 10--the alternating phenomenon spread out by eliminating some of the intermediate traces 3, 4, 7, and 8. The scanning speed was then slowed down, and similar pictures were taken. Figures 25a' and 25b' show every other scan, and 25c' shows every scan. This symmetry could be a phasing relationship of the pulsing of the transistor by the Curve Tracer to the scan speed of the polygon. The speed at which these curves are varying is indicative of the speed of the SB process and should allow a better understanding of this phenomenon.

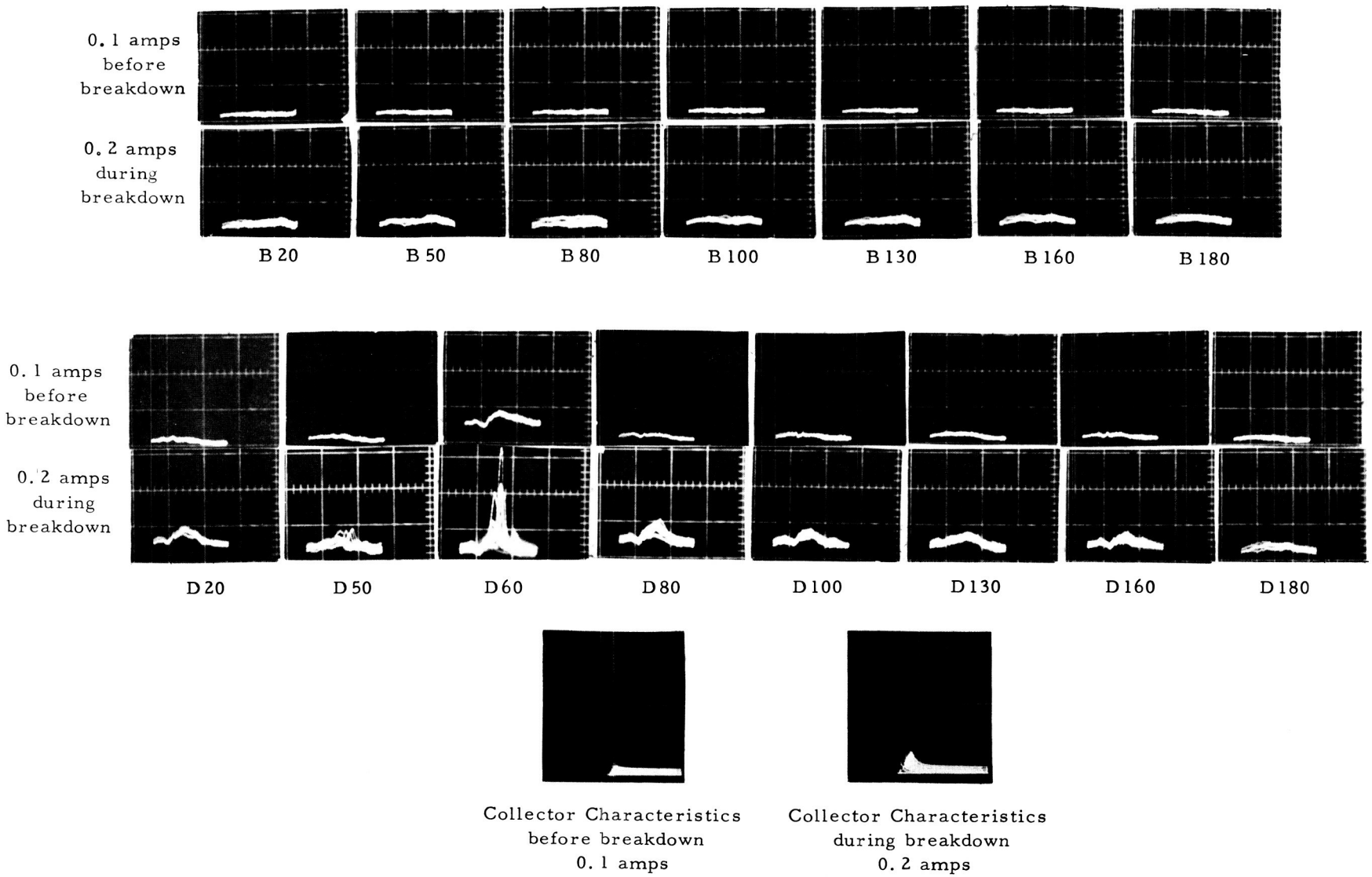


Figure 20. Second Breakdown Scan Lines of 2N1722 Transistor #26

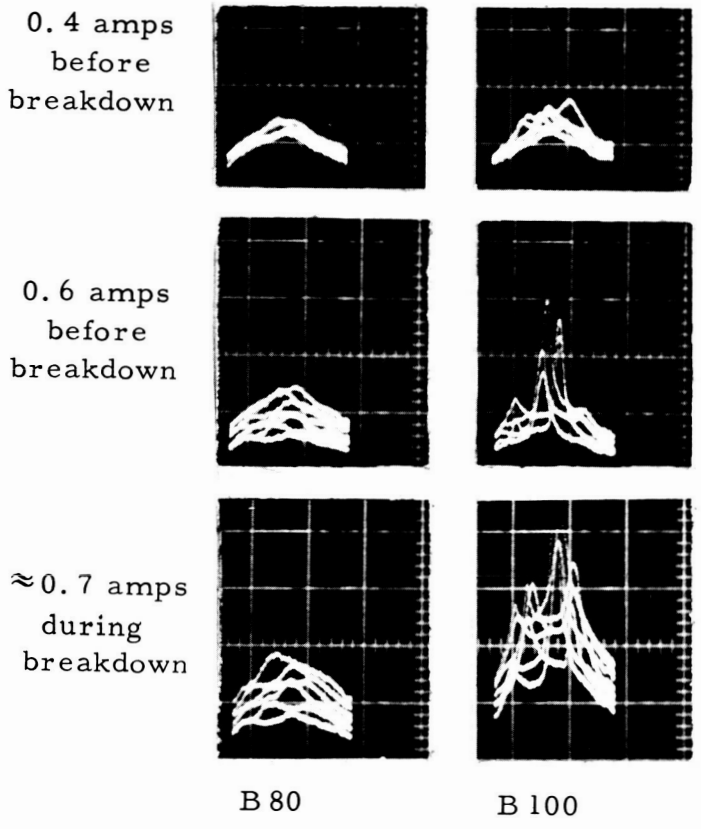


Figure 21. SB SCAN LINES OF 2N1722 TRANSISTOR #28

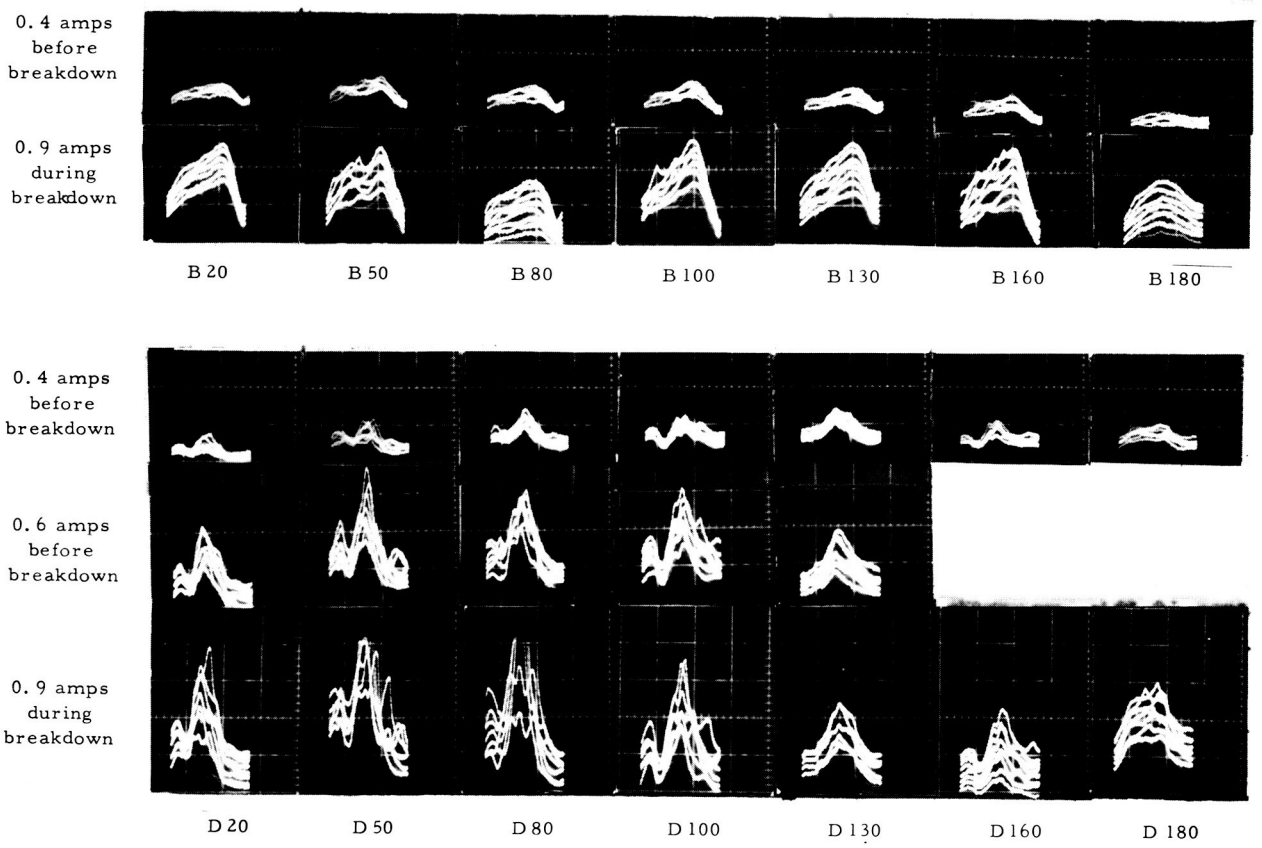
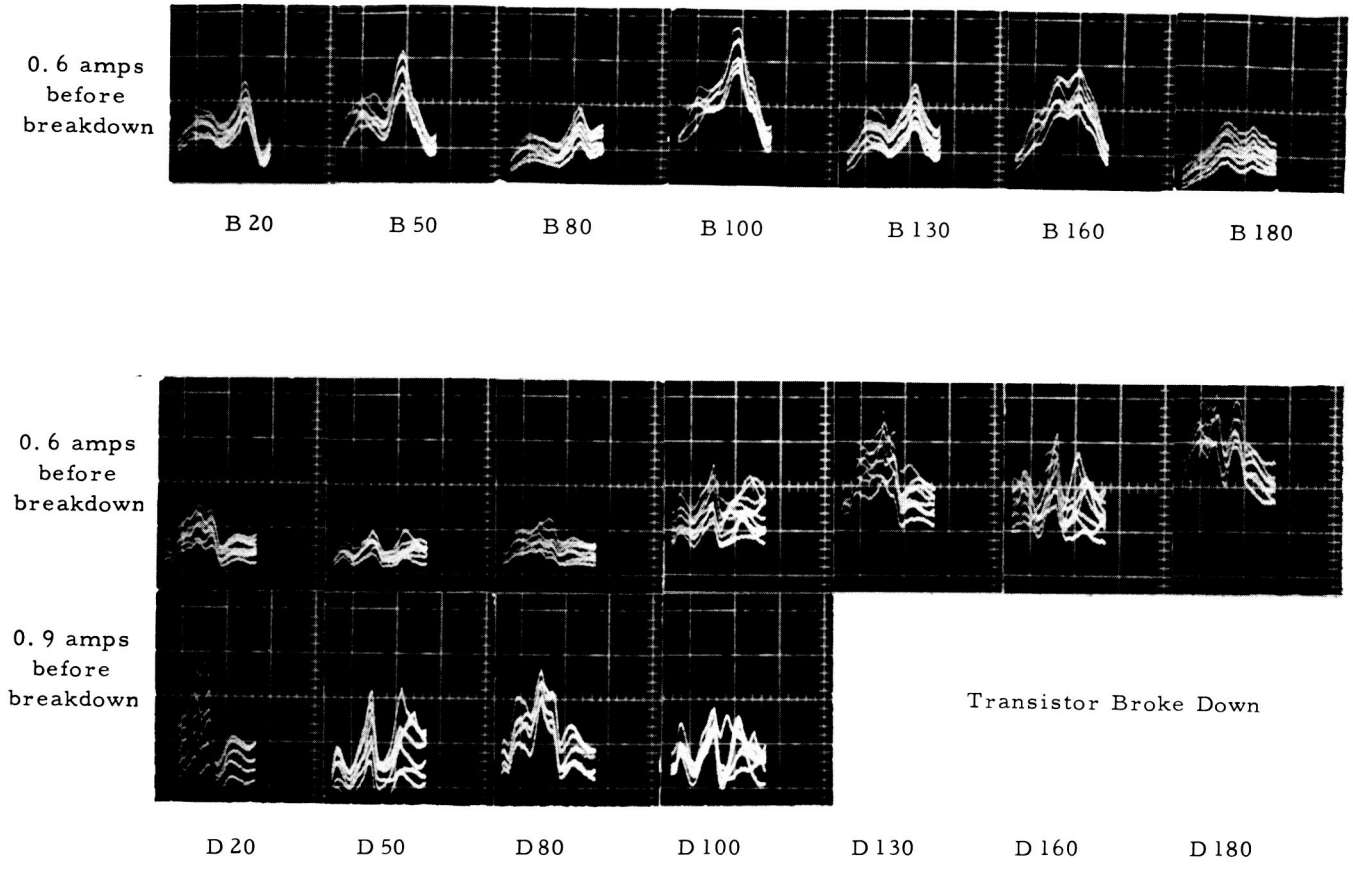
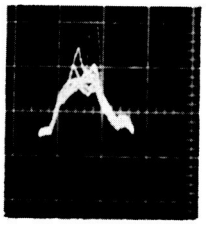
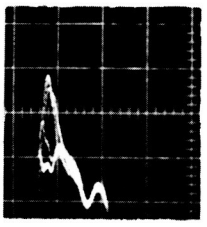


Figure 22. SB Scan Lines of 2N1722 Transistor #29

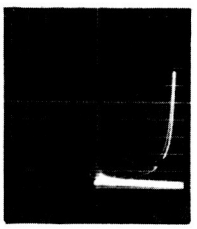




E 180
Breakdown
ⓐ 150ma

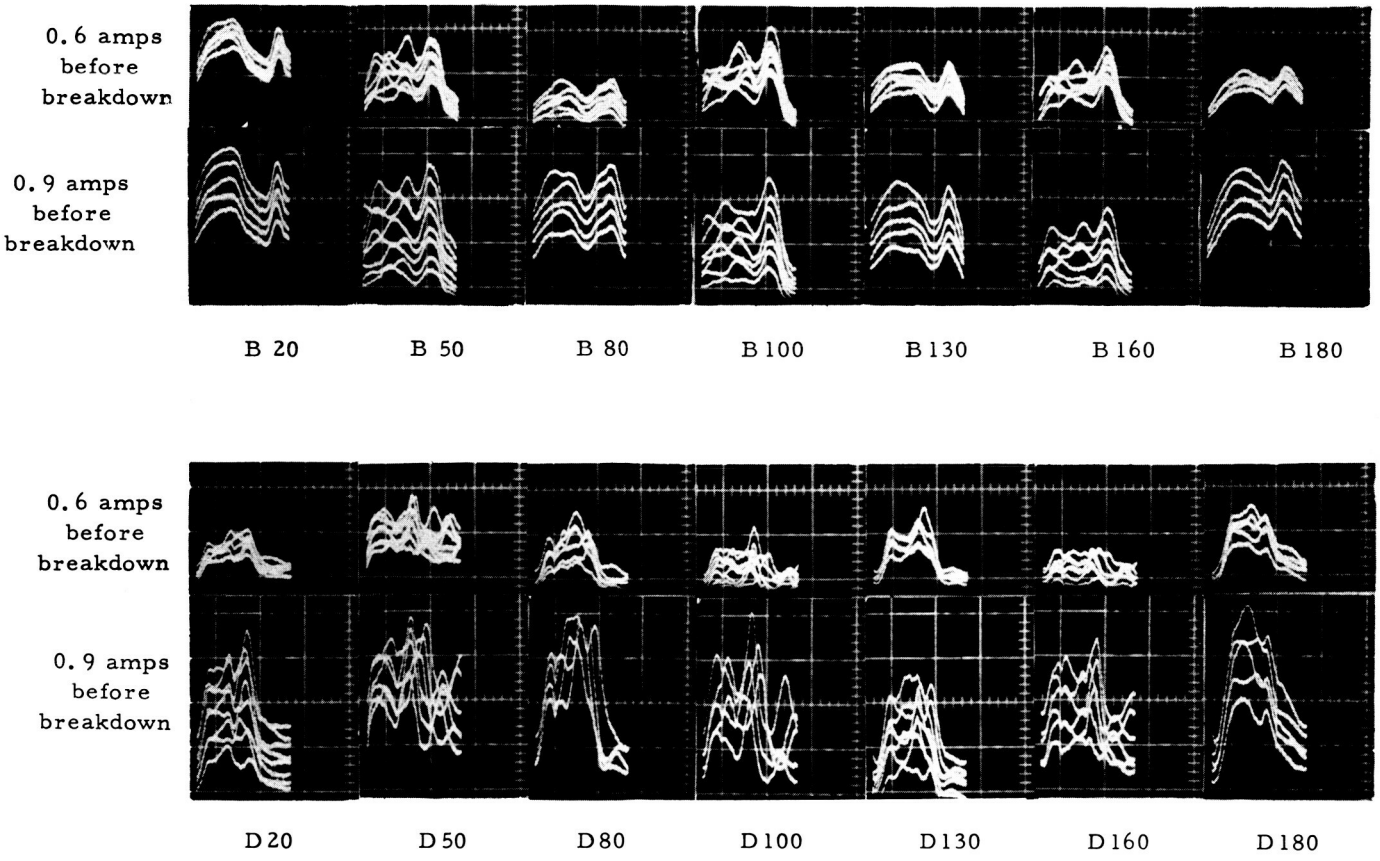


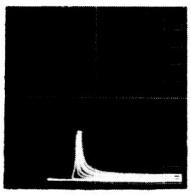
D 180
Breakdown
ⓐ 150ma



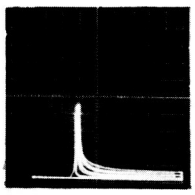
Collector Characteristics
during Breakdown
ⓐ 150ma

Figure 23. SB Scan Lines of 2N1722 Transistor #30



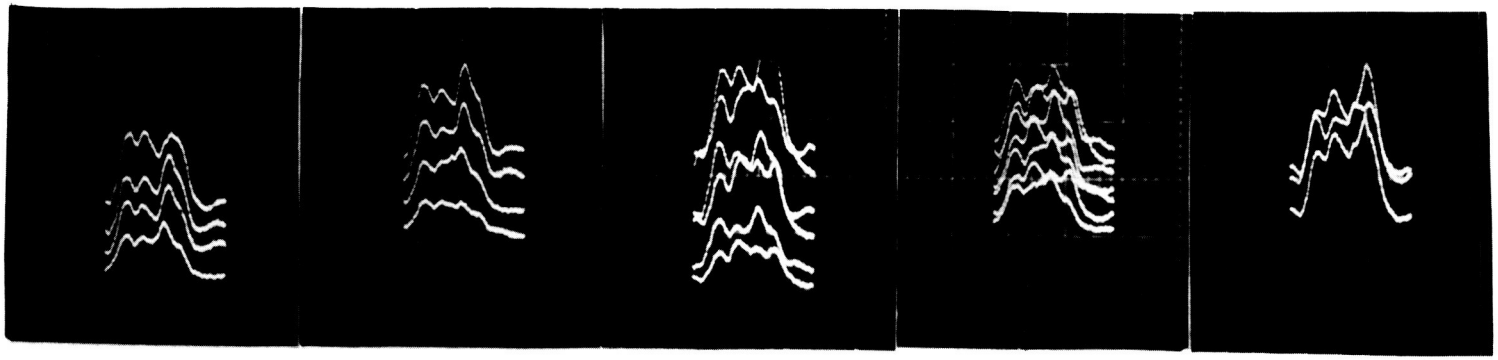


Collective Characteristics
0.6 amps
Before Breakdown



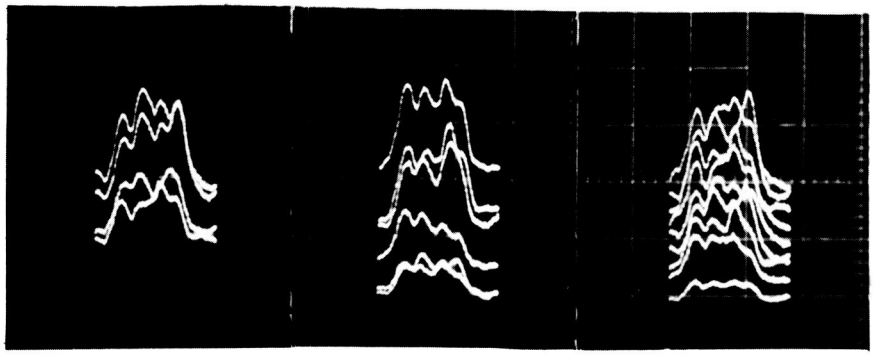
Collective Characteristics
0.9 amps
Before Breakdown

Figure 24. SB Scan Lines of 2N1722 Transistor #31



a b c d e

REGULAR



a' b' c'

SLOW

Figure 25. Scanning-Speed Test of Line D-180

C. Transistor Quality Evaluation

The microscope was used in the measurement of chip temperature in a vendor evaluation program of Type 2N930 transistors. These transistors, divided into seven lots of 50 each, made by seven different manufacturers, were individually energized at 1/4, 1/2, and full power. At every one of these levels, the case temperature was read by infrared means after thermal equilibrium was reached. Emissivity equalization of the case was achieved by applying a thin coat of Sylgard-182. The seven different manufacturers whose Type 2N930 transistors were evaluated are: Amelco, Fairchild, Motorola, Raytheon, Transitron, Texas Instruments, and Union Carbide. The results of this work are shown in Figures 26 through 32.

Figure 33 shows the electrical power setup used for this study. Care was taken to avoid differences in power dissipation from unit to unit. Once the case temperature measurements were completed, the lid of a limited number of units for each lot was cut away, exposing the chip to direct viewing. These units had been selected out of each one of the following groups: high case temperature, average case temperature, and low case temperature, for every manufacturer. The transistor chips, so exposed, were energized at full power and scanned with the microscope, and their maximum surface temperature was recorded. Figure 34 shows the results of these measurements.

It was found that the correlation between chip temperature and case temperature was good for some manufacturers and poor for others, as evidenced by the charts shown in Figures 35 through 41, detailed in the following:

Figure 35, Fairchild: shows good linear correlation of chip to case temperature. Visual analysis shows the higher level chip and case temperature transistors to have longer emitter leads in contrast to the low temperature transistors, which tend to have short emitter leads. (Emitter lead refers to lead from post to chip.)

Figure 36, Amelco: shows very little correlation of chip temperature and case temperature, but the grouping is fairly tight. Visual analysis shows no indication of temperature levels correlating to chip positioning.

Figure 37, Motorola: shows some correlation of chip temperature versus case temperature. Both chip temperature and case temperature frequency distribution show two levels: one high and one low, or average. Visual analysis shows that all the high temperature level transistors have a chip design of a certain type, while all the units of the "low" group are of a different design.

Figure 38, Union Carbide: shows some correlation of chip temperature versus case temperature. Visual analysis showed no apparent difference between transistors exhibiting different temperature levels.

Figure 39, Transitron: shows some correlation of chip temperature versus case temperature. Visual analysis showed no apparent difference between transistors.

Figure 40, Raytheon: shows a fairly good linear correlation of chip temperature versus case temperature. Visual analysis shows that the higher temperature transistors have the chip further from the emitter post, whereas the lower temperature transistors are closer to it. The chips are placed all over the header, in contrast with the other manufacturers' technique of keeping the chip location very constant.

Figure 41, Texas Instruments: shows some correlation of chip temperature versus case temperature. Visual analysis shows no correlation of position to temperature.

Two conclusions can be drawn from this study: (1) there is a limited correlation between chip temperature and case temperature, and (2) the spread of the infrared readings can give a fairly good idea of how tight the process control is for every manufacturer.

D. Temperature Versus Output Calibration Curves

Temperature calibration was done with the use of specially-designed blackbody cavities, whose radiation level was varied by controlling the power dissipated by a built-in heater, while the temperature was monitored by precision thermocouple.

Charts, correlating blackbody temperature with the magnitude of the infrared detector output, were plotted for various thermal ranges. Figure 42 shows one chart of this type. It can be seen that thermal resolution appears close to $2^{\circ}C$, at temperature levels between ambient and $100^{\circ}C$.

Before introducing the last changes in the microscope, temperature-versus-radiation curves (in volts out) were generated for an evaluation of the sensitivity of the CuGe detector, cooled with liquid helium, to that of the HgGe detector, cooled by the cryogenic generator. Figure 43 shows the two responses.

It is evident from these curves in Figure 43, that the HgGe detector, cooled by the cryogenic generator, is not as sensitive as the CuGe detector, cooled with liquid helium. The primary reason for running these tests was to evaluate the cryogenic generator prior to disassembly, so that any problems with the generator could be corrected in parallel with the re-assembly effort.

E. Low Power Transistors Type 2N3781 (1-Watt Without Heat Sink)

The low power transistor Type 2N3781 was scanned because it has a fine structural pattern of known physical dimension (Figure 44). It was tested during an investigation to evaluate the diameter of the area being viewed, and of the microscope's resolving capability.

The results were rather consistent and indicated that the diameter of the area viewed by the detector is approximately 0.005", with the capability of resolving elements three- to four-time smaller. Figure 45 shows the oscilloscope traces of line scan # 20 of the transistor of Figure 44. In the comb structure of this unit, the width of the "teeth" belonging to the base and to the emitter regions is approximately 35 microns. The scope trace shows that the system can resolve these areas from each other and from the junction area in between, by giving a separate measurement of the infrared radiation emitted by each one of them. The three traces shown in the Polaroid picture are corresponding to three different levels of power dissipation.

On the basis of these results, a consultation was held with Dr. Walther of Diffraction Limited, Inc., in order to devise ways and means to achieve finer resolution. The insertion of a "cold stop" diaphragm was indicated as the change most likely capable of producing this result. This change has been implemented in the final modification of the microscope.

Emissivity correction factor was derived by applying a thin layer of an inert coating having blackbody emissivity (Sylgard-182) over the semiconductor surface, and measuring the increase in radiation level so derived. Figure 46 shows in the lower trace the energy level of the infrared radiation emitted by the naked semiconductor surface, and in the upper trace, the increased level due to the applied coating. It is apparent that the emissivity index of the uncoated surface is approximately 0.5. Further study on this subject is continuing.

Measurement programs on medium power transistors (Type 2N3781) and integrated circuits were carried on, with the intent of refining our operating techniques and of finding the scanning procedure capable of yielding the most significant information.

CONCLUSION

The extensive calibration and measurement work carried out during Phase IV has made it possible to achieve the following goals:

1) develop sophisticated techniques for the alignment of the optics of the microscope;
2) confirm that the best practical trade-off between speed, spot-size and thermal resolution is in the vicinity of 30 lines per second, 30 microns and $2^{o}C$;
3) develop convenient aiming and focusing techniques;
4) perfect scanning techniques;
5) allow good understanding of the readings;
6) prove that future failures can be forecasted by infrared scanning.

CASE TEMPERATURE DATA

AMELCO 2N930 NPN

No.	¼Power	½Power	Full Power		No.	¼Power	½Power	Full Power
1	38.0	45.6	67.0		26			
2	35.0	42.3	67.5		27	35.0	46.3	67.0
3	35.8	42.0	62.0		28	35.8	45.6	68.0
4	37.0	41.5	67.0		29	38.2	49.5	70.6
5	37.4	48.0	71.0		30	37.0	49.0	73.0
6	36.0	47.6	69.5		31	37.0	50.0	75.6
7	35.0	44.0	64.5		32	36.0	47.4	72.0
8	37.0	49.0	77.0		33	38.2	51.8	77.0
9	38.4	49.4	72.0		34	37.0	49.0	74.4
10	37.0	49.0	73.0		35	33.4	44.4	74.4
11	36.0	45.5	68.0		36	34.8	45.6	74.4
12	37.0	47.5	66.5		37	34.8	47.4	70.6
13	39.4	50.0	76.0		38	33.4	46.5	73.1
14	37.0	47.4	74.4		39	36.0	50.0	75.0
15	37.0	46.5	70.7		40	36.0	51.0	73.0
16	32.4	43.5	69.4		41	35.0	45.6	70.6
17	33.4	47.4	73.3		42	33.4	43.4	69.4
18	33.5	45.6	69.4		43	33.5	46.5	72.0
19	33.4	47.5	74.4		44	35.0	50.0	72.0
20	34.8	43.4	72.0		45	35.0	54.3	75.0
21	32.4	42.5	63.5		46	35.0	47.4	74.4
22	29.5	45.5	72.0		47	36.0	49.0	74.4
23	36.0	47.4	69.5		48	36.0	47.4	77.0
24	33.5	44.0	65.5		49	35.0	51.0	74.0
25	35.8	46.5	69.4		50	36.0	52.0	74.0
				Notes: No. 26 showed a short				

Figure 26.

CASE TEMPERATURE DATA
MOTOROLA 2N930 NPN

No.	¼Power	½Power	Full Power		No.	¼Power	½Power	Full Power
1	32.0	38.0	68.0		26	34.5	43.5	70.5
2	32.0	41.0	66.5		27	32.0	40.5	69.2
3	33.5	43.5	69.0		28	34.5	52.0	72.0
4	37.0	59.0	94.0		29	33.4	43.5	69.2
5	34.0	42.3	73.4		30	31.5	45.5	80.5
6	33.4	45.5	69.0		31	34.5	45.5	73.4
7	38.0	59.0	91.0		32	33.4	45.0	69.0
8	33.4	39.0	69.2		33	33.4	42.0	72.0
9	34.0	40.0	69.2		34	35.7	50.5	84.5
10	34.7	50.0	68.6		35	33.8	50.0	88.5
11	33.0	41.4	74.4		36	32.0	42.3	66.5
12	33.4	43.4	72.0		37	32.0	39.0	69.2
13	34.5	39.5	69.2		38	33.4	38.0	66.5
14	32.0	39.0	66.5		39	33.4	41.4	70.0
15	32.5	42.3	69.2		40	34.0	39.0	74.5
16	33.0	41.4	68.0		41	33.6	37.5	66.5
17	32.0	37.5	68.6		42	32.5	41.5	70.5
18	33.4	42.3	74.4		43	32.5	43.5	71.5
19	33.0	38.0	69.2		44	33.4	39.0	68.0
20	33.4	43.0	70.0		45	32.0	41.0	67.2
21					46	32.5	39.0	66.5
22	33.4	43.0	69.2		47	34.0	39.0	67.2
23	34.5	38.0	66.5		48	32.5	39.5	66.5
24	34.5	38.0	69.0		49	33.4	41.4	68.0
25	32.5	37.0	66.5		50	33.4	47.5	79.5
				Note: No. 21 shorted				

Figure 27.

CASE TEMPERATURE DATA

FAIRCHILD 2N930 NPN

No.	¼Power	½Power	Full Power		No.	¼Power	½Power	Full Power
1	85.8	96.5	98.2		26			
3	34.5	46.5	72.3		27	34.5	45.0	63.8
5	36.4	50.9	78.8		28	36.4	51.0	70.0
6	36.4	44.0	74.4		29	36.4	51.7	71.8
7	36.4	45.7	74.4		30	35.8	49.2	68.2
8	37.4	49.2	71.2		31	35.7	51.7	73.0
9	34.5	44.0	71.1		32	34.8	51.7	71.8
10	33.5	44.0	74.4		33	33.6	46.4	64.3
11	34.5	51.0	70.0		34	35.8	48.3	72.0
13	34.5	45.6	73.2		35	36.0	50.0	74.4
14	34.5	51.0	71.0		36	33.4	49.0	72.0
15	35.5	52.5	74.4		37	34.8	51.0	78.0
16	35.3	51.8	72.2		38	34.8	49.0	73.0
17	34.0	50.0	72.2		39	34.8	51.0	74.4
18	34.5	51.0	76.5		40	36.0	45.4	69.0
19	36.5	50.0	74.4		41	34.4	51.0	75.5
20	37.8	51.0	74.2		42	39.2	51.0	79.0
21	36.8	51.0	70.8		43	38.3	49.0	76.2
22	36.0	47.0	70.8		44	34.8	43.5	66.4
23	36.8	51.0	71.8		45	38.0	49.0	78.0
24	35.8	49.0	69.5		46	37.0	49.0	75.5
25	38.0	51.0	72.0					
				Note: No. 2, 4, + 26 showed short				

Figure 28.

CASE TEMPERATURE DATA

RAYTHEON 2N930 NPN

No.	¼ Power	½ Power	Full Power		No.	¼ Power	½ Power	Full Power
1	35.8	43.4	57.5		26	35.2	40.2	54.5
2	35.8	44.5	63.0		27	34.5	41.0	77.5
3	36.4	43.4	63.8		28	32.4	41.0	69.2
4	34.5	39.0	63.8		29	33.2	45.5	85.6
5	36.4	43.4	78.8		30	32.4	38.0	66.4
6	35.8	40.6	56.0		31	33.5	39.6	57.5
7	34.5	40.6	57.3		32	34.0	43.0	79.5
8	35.2	41.0	57.5		33	32.4	39.0	59.7
9	38.2	50.0	83.0		34	32.4	39.0	62.0
10	33.0	39.0	56.0		35	32.4	38.0	63.8
11	33.5	43.0	57.5		36	32.4	36.5	49.0
12	34.2	41.0	79.5		37	33.5	42.3	67.2
13	34.0	40.2	60.6		38	33.0	37.0	65.0
14	34.2	40.2	58.8		39	33.5	40.2	66.4
15	34.5	40.2	54.8		40	33.5	41.0	79.5
16	34.5	39.4	74.0		41	33.5	40.2	74.0
17	32.4	38.5	47.4		42	34.5	40.2	75.0
18	33.5	40.2	52.8		43	33.5	40.2	56.0
19	32.4	39.0	52.0		44	35.8	44.5	79.5
20	33.5	40.2	54.5		45	34.2	40.6	75.0
21	33.5	41.0	68.0		46	34.5	42.3	57.0
22	33.0	39.0	50.0		47	33.5	40.2	66.4
23	34.5	39.0	78.0		48	33.0	41.0	80.2
24	34.5	40.2	58.2		49	32.4	39.0	56.0
25	34.0	38.5	45.5		50			

Figure 29.

CASE TEMPERATURE DATA

TEXAS INSTRUMENTS 2N930 NPN

No.	¼ Power	½ Power	Full Power		No.	¼ Power	½ Power	Full Power	
1	34.5	51.0	73.5	*	26	33.5	49.0	84.5	
2	32.0	49.0	71.0	*	27	35.5	54.5	86.0	
3	33.5	44.5	73.0		28	33.5	45.5	66.5	*
4	35.0	52.0	81.7		29	34.5	46.5	73.5	*
5	33.5	51.0	84.0		30	34.5	51.0	75.5	*
6	32.5	49.0	77.0		31	34.5	53.5	76.0	*
7	33.5	52.0	77.0		32	35.0	46.5	72.0	*
8	32.0	44.5	73.0		33	32.5	45.5	72.0	
9	33.5	48.0	77.0		34	34.0	51.0	82.0	
10	35.0	52.0	77.0		35	35.0	53.0	85.5	
11	34.5	54.5	86.0		36	34.0	53.5	88.0	
12	36.0	56.5	83.0		37	33.5	51.0	82.0	
13	36.0	55.5	89.0		38	35.5	52.0	82.0	
14	36.0	53.5	86.0		39	34.0	53.0	84.5	
15	36.0	55.0	89.0		40	33.5	52.0	83.0	
16	34.5	50.0	83.0		41	34.5	54.0	85.0	
17	34.5	53.5	84.7		42	34.5	52.0	82.0	
18	35.0	47.5	80.0		43	37.0	53.5	87.0	
19	33.5	46.5	78.5		44	33.5	48.5	82.0	
20	34.5	52.0	86.0		45	36.5	53.0	87.0	
21	33.5	48.0	78.0		46	34.5	53.0	89.0	
22	32.5	49.0	80.0		47	34.5	49.5	79.5	
23	34.0	46.5	74.0						
24	33.5	47.5	78.0						
25	34.0	51.0	84.5						

* Short Leads

All of the remaining transistors listed above have standard length leads.

Figure 30.

CASE TEMPERATURE DATA

TRANSITRON 2N930 NPN

No.	¼Power	½ Power	Full Power		No.	¼Power	½ Power	Full Power
1	33.8	42.3	75.8		26	34.5	39.6	63.8
2	34.2	42.5	77.0		27	36.5	45.2	80.5
3					28	34.5	41.0	73.5
4	34.0	49.0	77.0		29	35.2	42.0	74.5
5	32.4	40.2	64.0		30	34.2	41.0	69.2
6	31.0	38.0	70.0		31	33.5	38.0	74.5
7	34.0	43.4	77.0		32	35.2	43.4	77.0
8	32.4	39.0	57.5		33	34.0	41.0	60.5
9	34.5	41.5	65.0		34	33.5	40.2	69.2
10	34.5	42.3	70.4		35	37.0	43.0	78.0
11	34.5	43.4	68.0		36	35.8	42.3	80.5
12	32.4	40.2	57.4		37	32.4	40.2	81.8
13	39.0	47.4	81.8		38	32.8	39.6	64.8
14	34.5	44.5	81.8		39	32.4	43.4	77.0
15	34.5	43.4	78.0		40	32.7	42.3	66.4
16	34.8	43.4	78.0		41	36.7	43.4	68.6
17	36.4	43.4	69.0		42	34.2	43.0	72.0
18	34.5	43.4	69.0		43	35.8	42.3	73.5
19	35.8	43.4	64.6		44	37.0	44.5	74.0
20	32.0	37.3	65.0		45	36.0	41.6	72.2
21	35.8	42.3	77.0		46	34.8	43.4	74.5
22	35.2	43.0	68.0		47	35.8	42.3	63.4
23	34.8	41.8	76.8		48	36.4	43.4	73.5
24	34.5	41.0	63.8		49	35.8	42.5	62.0
25	34.5	41.0	69.2					
				Note: No. 3 unstable				

Figure 31.

CASE TEMPERATURE DATA

UNION CARBIDE 2N930 NPN

No.	¼Power	½Power	Full Power		No.	¼Power	½Power	Full Power
1					26	32.4	39.0	73.5
2					27	33.5	41.0	73.5
3					28	33.5	38.5	69.0
4	37.0	45.5	74.5		29	32.4	39.5	77.0
5	32.4	40.2	70.8		30	33.5	41.0	81.8
6	32.4	41.0	71.2		31	32.0	42.0	81.8
7	32.4	41.0	70.8		32	32.4	41.0	73.5
8	33.5	42.3	75.8		33	33.0	39.0	68.0
9	32.4	40.2	69.2		34	33.5	42.3	76.8
10	33.0	40.2	74.0		35	33.5	41.0	81.8
11	32.4	40.2	69.0		36	33.5	41.0	80.5
12	31.5	40.2	72.0		37	33.0	39.0	74.5
13	32.5	39.0	70.0		38	33.8	40.2	80.5
14	31.5	39.5	70.8		39	33.5	41.0	76.4
15	32.4	38.0	69.0		40	34.2	41.0	79.5
16	32.4	38.0	69.2		41	33.5	40.0	78.0
17	32.4	40.2	68.0		42	34.5	41.0	74.5
18	32.4	40.2	76.8		43	34.2	40.2	69.2
19	33.5	38.5	68.0		44	33.0	41.0	77.0
20	33.5	40.2	70.8		45	34.5	41.5	76.8
21	33.5	40.2	68.6		46	34.2	40.2	75.8
22	32.8	39.0	71.0		47	34.0	42.3	77.0
23	32.4	40.6	79.5		48	33.0	39.0	73.5
24	33.5	39.5	70.0		49	34.5	42.3	77.0
25	32.4	40.6	79.5		50	34.5	39.5	70.8
				Note: No. 1, 2, + 3 showed short				

Figure 32.

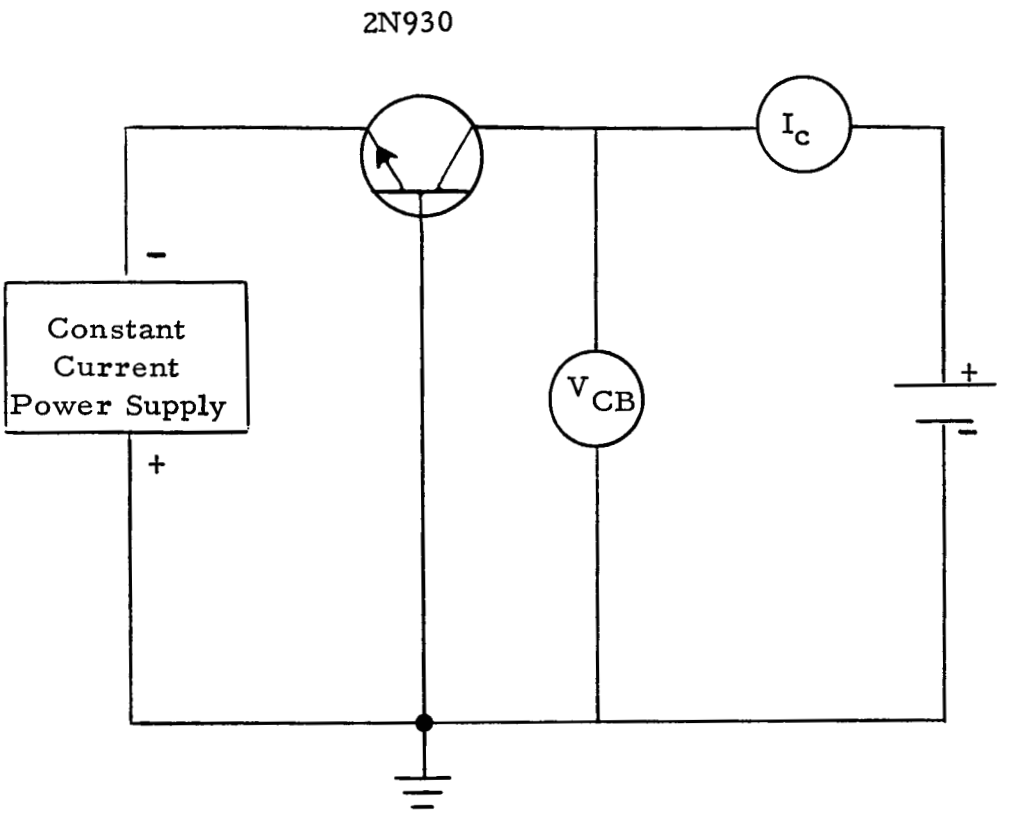


Figure 33. ELECTRICAL POWER SETUP FOR 2N930 TRANSISTOR STUDY

CHIP TEMPERATURE - FULL POWER

AMELCO		FAIRCHILD		MOTOROLA		RAYTHEON	
Trans. No.	Temp.	Trans. No.	Temp.	Trans. No.	Temp.	Trans. No.	Temp.
33	short	5	112	6	open	29	117
13	short	37	114	8	104	28	112
48	short	45	115	9	104	17	99
8	121	16	108	13	open	25	86
31	120	17	107	15	108	9	115
45	121	25	107	22	104	30	103
5	118	29	108	24	104	35	110
9	122	34	109	27	113	37	105
15	119	33	99	29	115	38	118
20	121	30	103	4	118	48	112
22	118	44	105	7	117	22	99
3	119			30	118		
7	119			34	121		
21	119			35	115		

TRANSITRON		TEXAS INSTRUMENTS		UNION CARBIDE	
Trans. No.	Temp.	Trans. No.	Temp.	Trans. No.	Temp.
13	117	36	117	30	115
14	118	43	104	31	118
27	112	46	113	35	114
7	118	16	97	4	113
10	113	34	113	10	112
17	110	37	104	26	112
18	112	38	97	27	114
28	113	23	96	32	115
26	97	33	97	17	110
33	110	8	104	19	108
49	105			33	110

Figure 34. 2N930 TRANSISTOR THERMAL STUDY

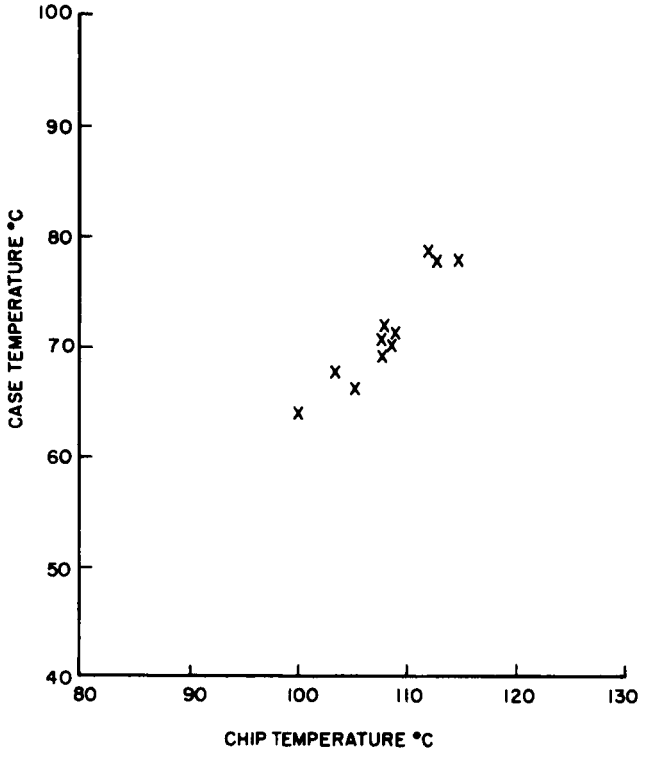


Figure 35. Graph - Case Temperature vs Chip Temperature - Fairchild

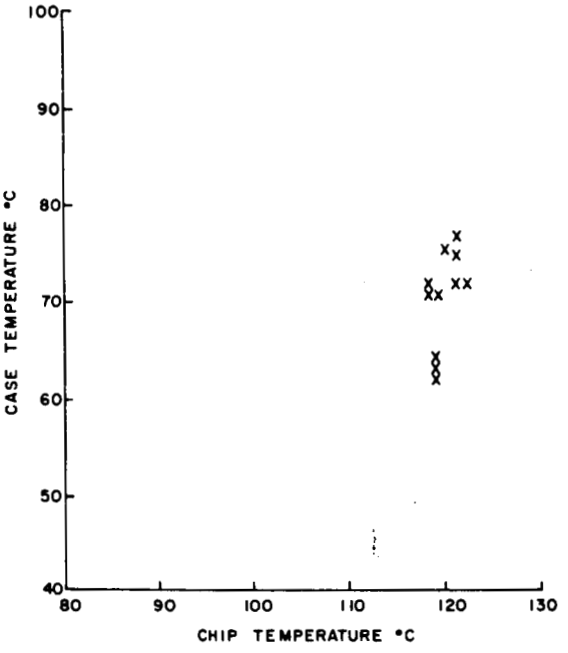


Figure 36. Graph - Case Temperature vs Chip Temperature - Amelco

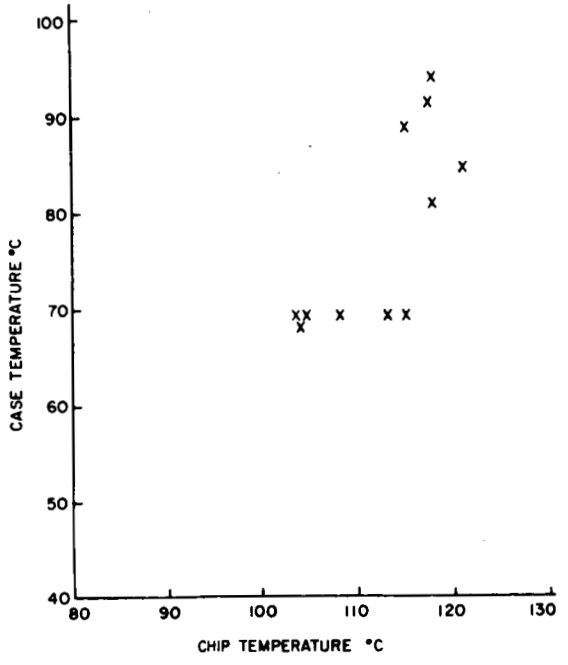


Figure 37. Graph - Case Temperature vs Chip Temperature - Motorola

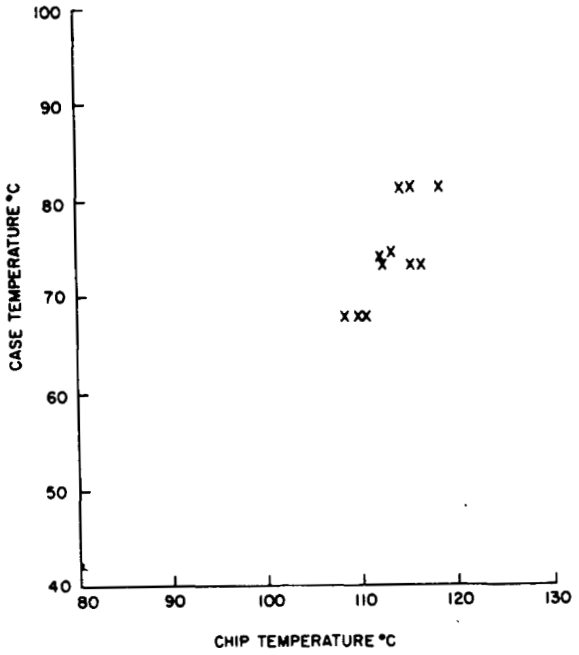


Figure 38. Graph- Case Temperature vs Chip Temperature - Union Carb.

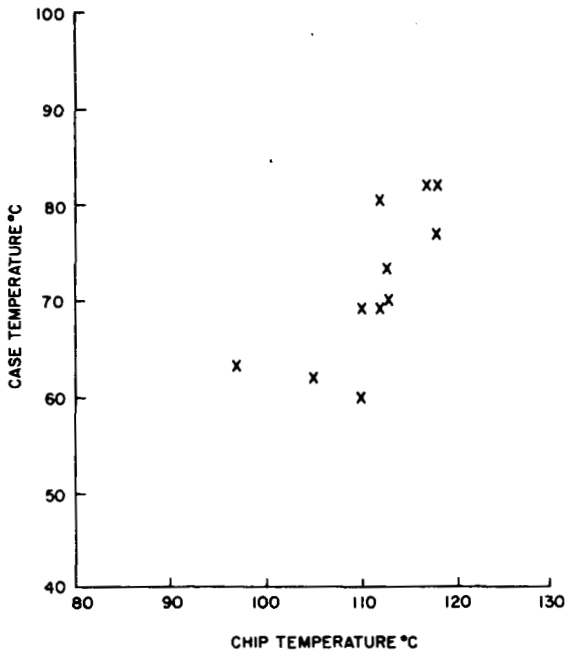


Figure 39. Graph - Case Temperature vs Chip Temperature - Transitron

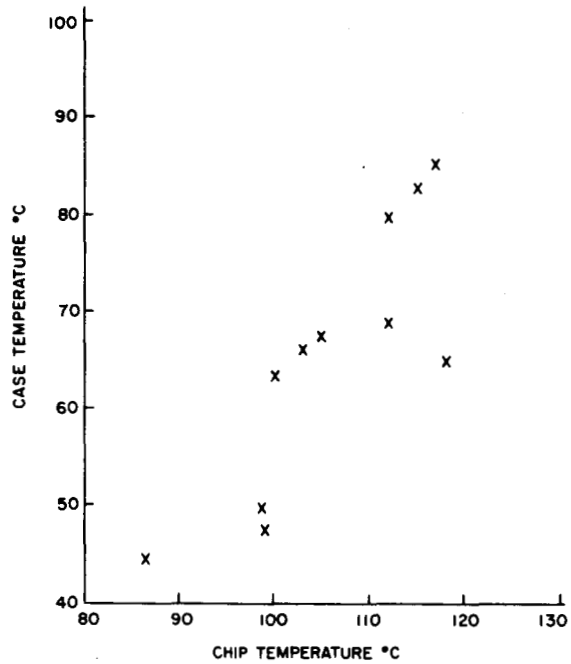


Figure 40. Graph - Case Temperature vs Chip Temperature - Raytheon

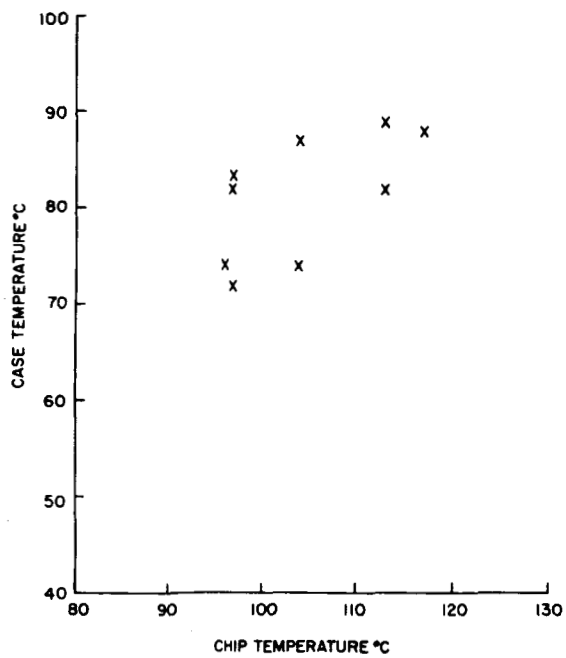


Figure 41. Graph - Case Temperature vs Chip Temperature - Texas Instr.

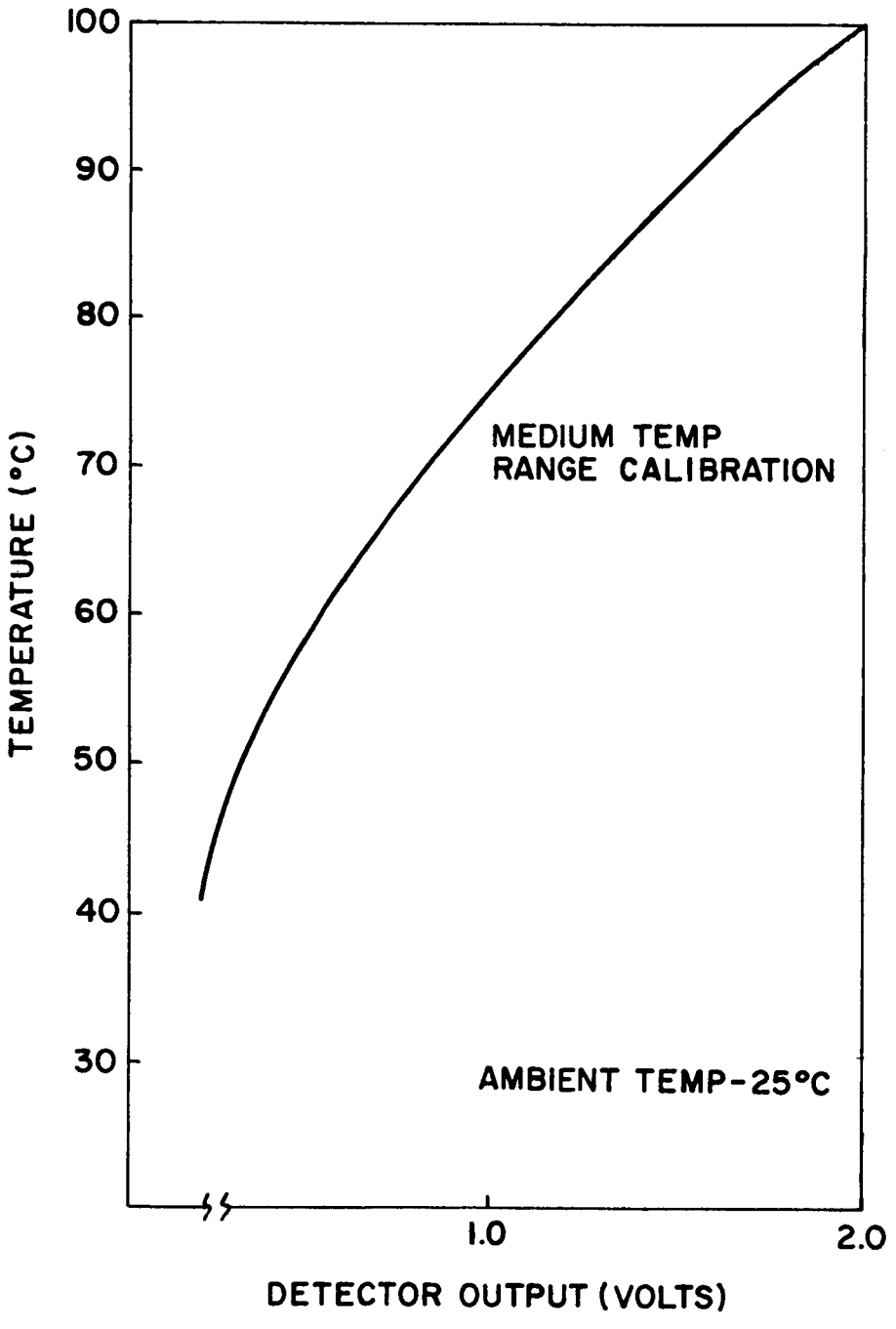


Figure 42. BLACKBODY TEMPERATURE CHART

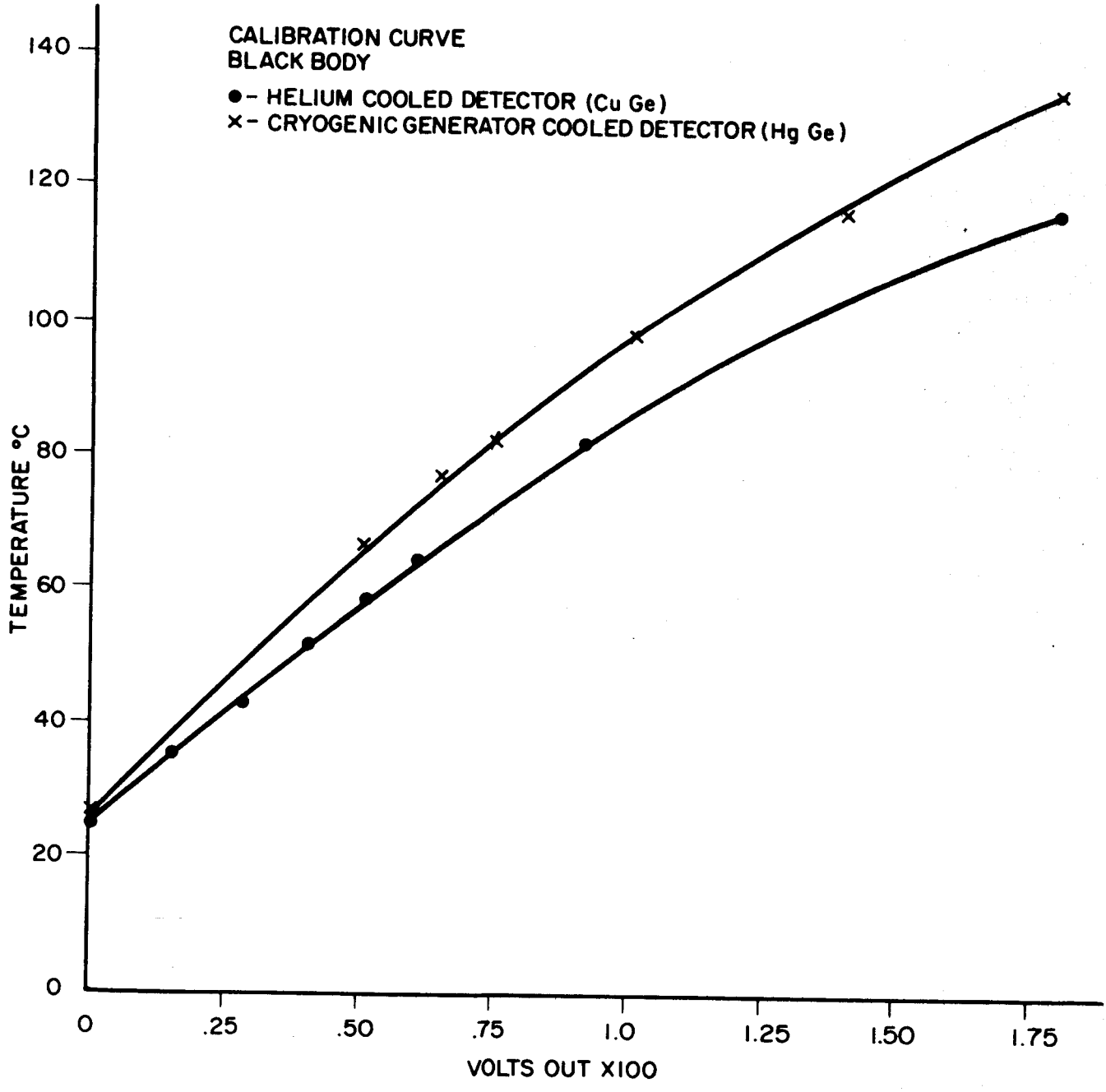


Figure 43. BLACKBODY CALIBRATION CURVES

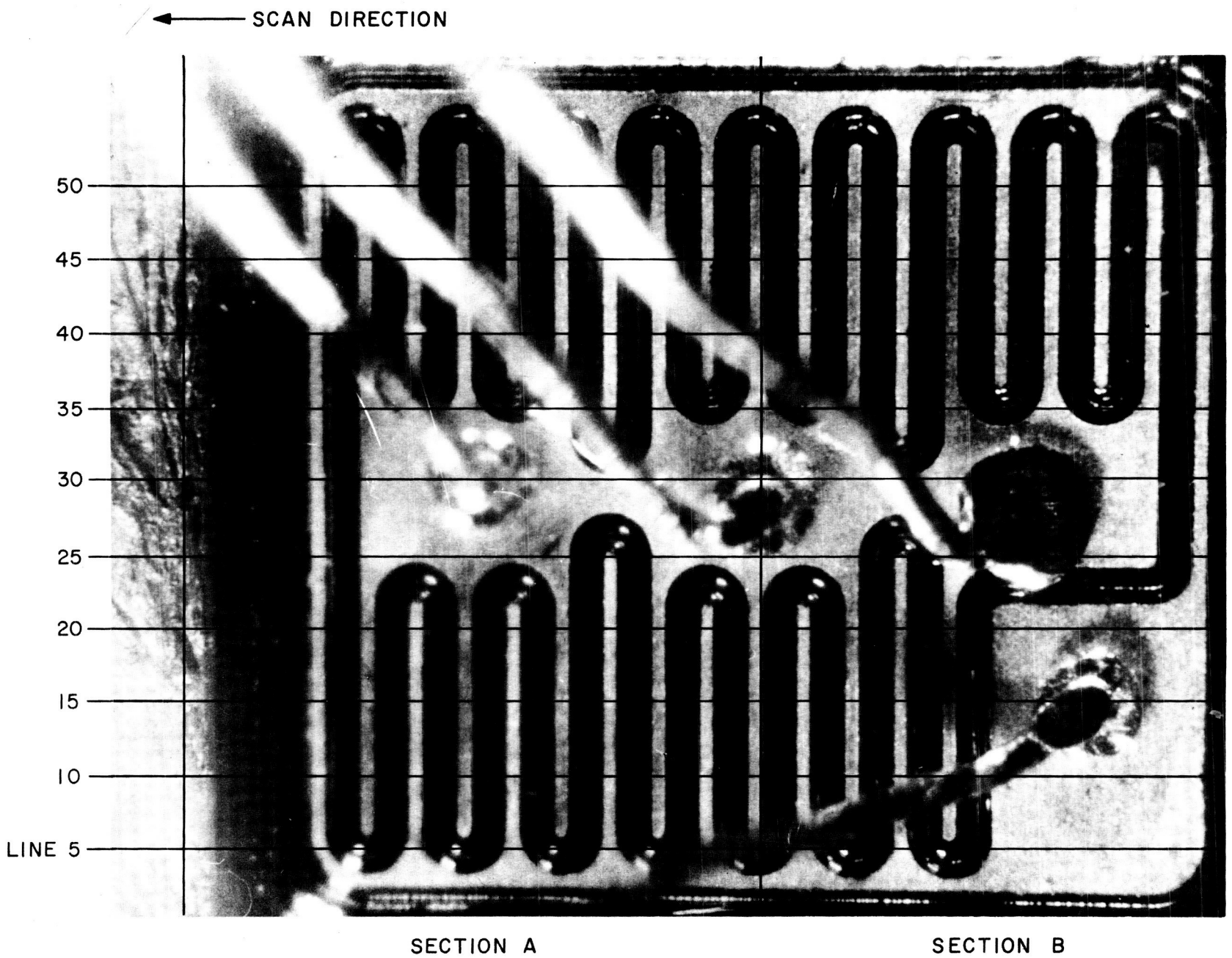


Figure 44. 2N3781 Transistor with Line Scan Raster

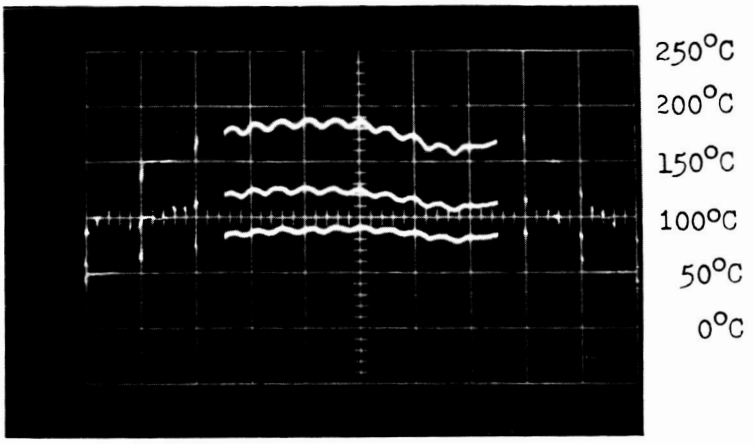
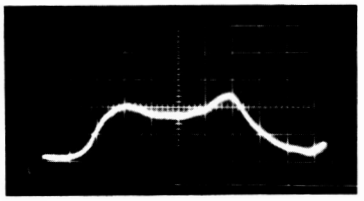
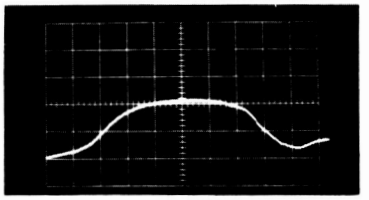


Figure 45. 2N3781 TRANSISTOR. SCAN TRACES OF LINE A20 AT VARIOUS POWER LEVELS



Vertical Scale
.5 v/cm

UNCOATED SURFACE



Vertical Scale
1 v/cm

COATED SURFACE

Figure 46. EMISSIVITY OF SURFACE COATING